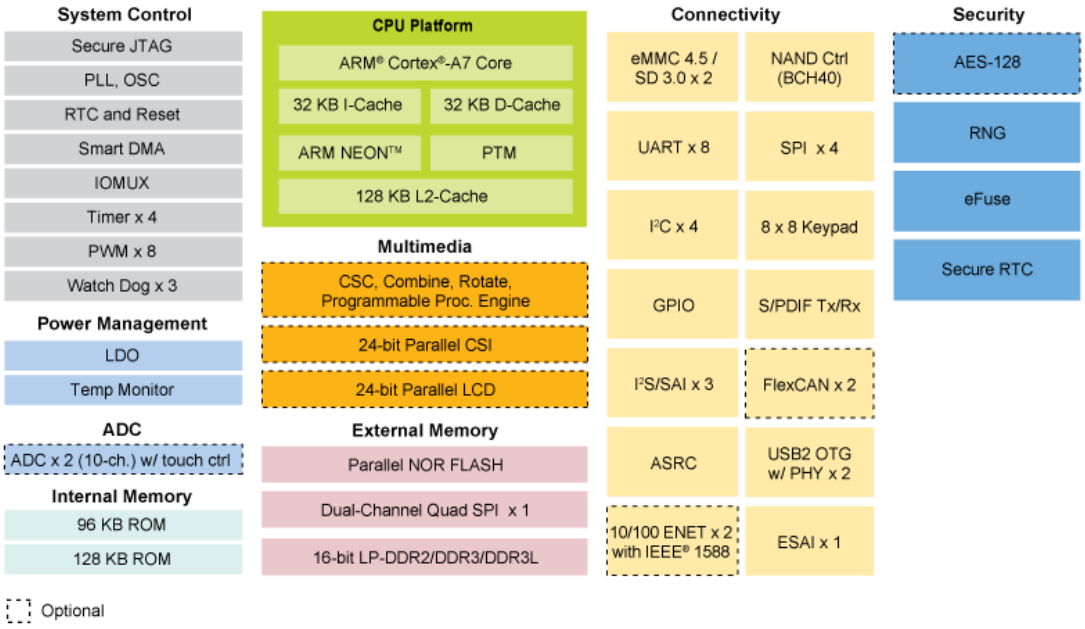
Content

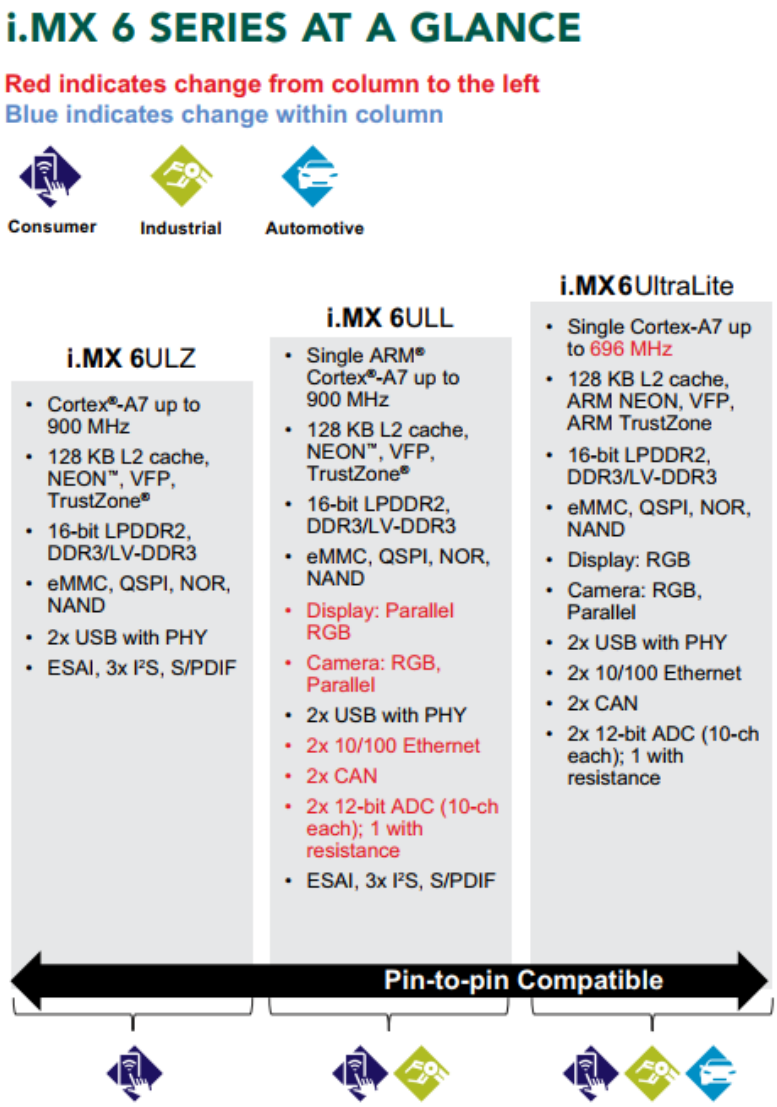
1．NXP i.MX6ULL chip introduction

i.MX6ULL is designed by NXP, high efficiency, cost effective application processor. With advanced implementations of single core ARM Cortex-A7 running up to 900MHz. i.MX 6ULL application processor includes an integrated power management module that reduce the complexity of the external power supply and simplifies power-up sequencing. Applications include:

- Automotive telematics
- IoT gateway
- HMI human machine interface
- Home power management system
- Intelligent energy information concentrator
- Intelligent industrial control system
- Electronic POS equipment
- Portable medical equipment
- Printer and 2D scanner, etc.



i.MX6ULL block diagram



i.MX6ULL Pin-to-Pin compatible chip and difference comparison

i.MX6ULL BGA289 package main chipset's part number and parameter comparison list:

Parts	MCIMX6Y2CVM05AA	MCIMX6Y2CVM08AB	MCIMX6Y2DVM09AB
Marketing Description	i.MX 32-bit MPU, ARM Cortex-A7 core, 528MHz, 289BGA	i.MX 32-bit MPU, ARM Cortex-A7 core, 800MHz, 289BGA	i.MX 32-bit MPU, ARM Cortex-A7 core, 900MHz, 289BGA
Package Type	LFBGA289	LFBGA289	LFBGA289
Core Type	Arm Cortex-A7	Arm Cortex-A7	Arm Cortex-A7
Operating Frequency [Max] (MHz)	528	800	900
External Memory Supported	DDR3 SDRAM, DDR3L SDRAM, LPDDR2 DRAM	DDR3 SDRAM, DDR3L SDRAM, LPDDR2 DRAM	DDR3 SDRAM, DDR3L SDRAM, LPDDR2 DRAM

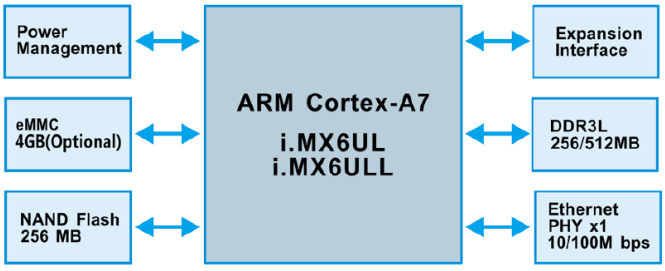
Video/Display features	RGB	RGB	RGB
Ethernet	2	2	2
SPI	4	4	4
I2C	4	4	4
UART	8	8	8
SAI	3	3	3
USB Controllers	2	2	2
CAN	2	2	2
Work Temperature (℃)	-40 ~ 105	-40 ~ 105	0 ~ 95
Camera Interfaces	CSI	CSI	CSI
Audio Specific Modules			SPDIF

WT-SOM6ULX supports i.MX6UltraLite and i.MX6ULL all BGA289 part numbers. Main production model is i.MX6ULL series **MCIMX6Y2CVM08AB,** Other models produced by order.

2. WT-SOM6ULX schematic and test instruction

2.1 WT-SOM6ULX core board block diagram and schematic

For most applications, WT-SOM6ULX designed the smallest system Power Management + DDR3L + NAND/EMMC+ LAN8720(Ethernet Phy).



WT-SOM6ULX smallest system block diagram

Core board schematic “wt-som6ulx-sch-v1.pdf”, you can get from sales representative.

2.2 WT-SOM6ULX core board's power management

According to i.MX6ULL power supply timing requirement, core board layout 4 power supply pins: VSNVS, VSYS_3V3, USB_OTG2_VBUS, USB_OTG1_VBUS.

VSNVS have to powered first, backup battery power can be used for button ON/OFF switch control, low power consumption, maintenance internal RTC power supply after shutdown, only consume 26uA.

VSYS_3V3 is the main power supply for the core board, full load current consumption <200mA.

USB_OTG2_VBUS and USB_OTG1_VBUS powered after VSYS_3V3. When you don't need to use the USB function, you don't need to supply power.

Power supply pin	Min	Max	Current	Power supply ripple requirement
VSYS_3V3	3.2V	3.4V	<200mA(full speed operation) <9mA (standby)	<30mVrms
VSNVS	2.8V	3.4V	<500uA	<30mVrms
USB_OTG2_VBUS	4.7V	5.2V	<50mA	<50mVrms
USB_OTG1_VBUS	4.7V	5.2V	<50mA	<50mVrms

2.3 i.MX6ULL related power domain ripple test

WT-SOM6ULX adopts single-sided layout, which performs a lot of power integrity simulation and optimization in the power supply part, and draws test points in the CPU-related power domain and performs power supply ripple test.

Test conditions: DDR stress test status,

Test method: oscilloscope, 10X probe, AC coupling, 20mV, 1mS, bandwidth 20M

Test point	Power network	Ripple amplitude (peak to peak)	Voltage (V)
TP18	VDD_ARM_CAP	29mV	1.272
TP12	VSYS_3V3	24mV	3.3
TP11	VDD_ARM_SOC_IN	22mV	1.348
TP19	DRAM_1V35	30mV	1.351
TP17	VDD_SOC_CAP	20mV	1.273
TP14	VDD_SNVS_CAP	20mV	1.107
TP15	NVCC_PLL_OUT	19mV	1.118
TP13	VDD_SNVS_3V3	24mV	3.297
TP16	VDD_HIGH_CAP	22mV	2.521

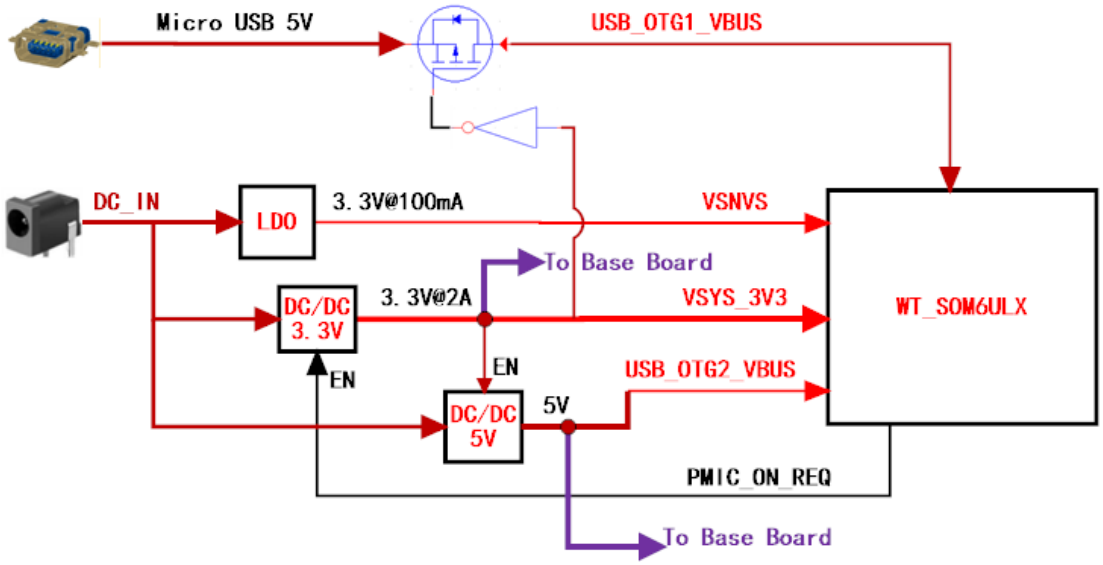
TP20	DRAM_VREF	20mV	0.677

3． Based on WT-SOM6ULX’s baseboard power system design

3.1 Core board power sequencing and typical power supply circuit

- SNVS should be powered first and can be powered by LDO or backup battery separately. SNVS should be powered first and can be powered separately by LDO or backup battery. SNVS can be used for button ON/OFF switch control, low current consumption, maintenance of internal RTC power supply after shutdown, only consumes 26uA.
- After the SNVS is powered on, the core board pin PMIC_ON_REQ output is used to control the VSYS_3V3 power switch. When the CPU enters the shutdown state, PMIC_ON_REQ will be pulled low to turn off the entire board except the other SNVS part. The 3.3V power supply for the baseboard and core board should use the same power supply output to avoid potential risks due to level differences or inconsistent power-up timing.
- 5V power supply (USB_OTG1_VBUS, USB_OTG2_VBUS, CAN, RS485, etc.) should be powered after the 3.3V power supply’s stable.
- For all IO pins, ensure that there is no high level input before VSYS_3V3 is powered on.

The above is the power-on timing requirements of the NXP i.MX6ULL chip to ensure long-term stable operation of the whole circuit board. If the timing requirements are violated, the power-on behavior of the chip may be affected, resulting in a small probability of chip damage or startup failure.

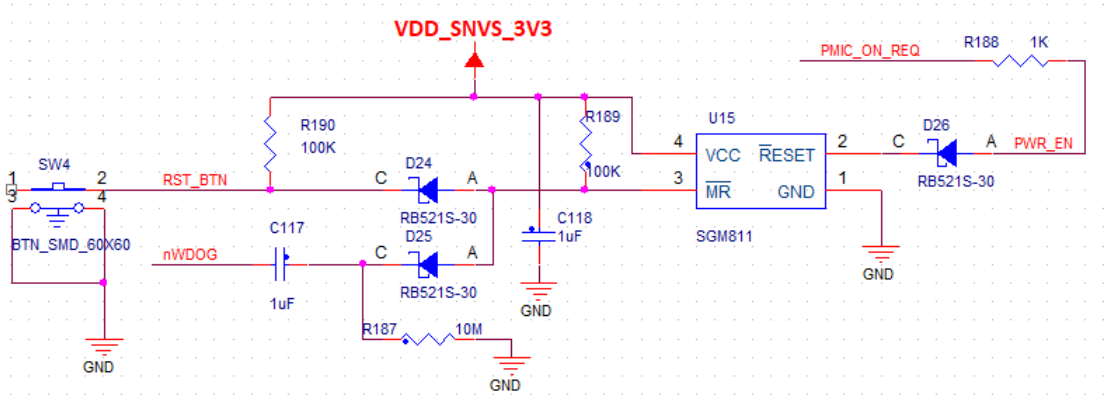


WT-SOM6ULX typical power supply scheme

Power/GND pin	Pin number	Description
VSNVS	96	Have to be powered on first, and have to be powered on when switch power management is required.
VSYS_3V3	97	Main power supply. Power supply is enabled via PMIC_ON_REQ. It is recommended that the string power supply use a magnetic bead (such as 120R 3A) and then place a 2x22uF ceramic capacitor near the pin to form an LC filter. Use low ripple DC/DC power supply. Ripple <30mVrms.
USB_OTG1_VBUS	77	The MicroUSB VBUS input can be connected, also can be disconnected, but it must be powered after VSYS_3V3 powered on.
USB_OTG2_VBUS	76	Disconnected if no need to use USB function. It must be powered after VSYS_3V3 is powered on, 5V. Add 10uF ceramic capacitors near the pin.
GND	5, 35, 42, 55, 73, 78, 81, 98, 115, 126	Totally 10 GND pins. The GND pin must be fully connected to the GND plane of the baseboard (multiple vias or copper) to optimize the return path for high speed signals.

3.2 About reset

In PWR_EN network control VSYS_3V3 的 DC/DC chip enable pin. The WT-SOM6ULX has a power-on reset chip on board, and the overall reset of the core board is recommended to use a power-off reset. Typical mode: the output of the MAX811 is used to control the VSYS_3V3 supply enable, which can be manually reset by a reset button or watchdog rest. Refer to the circuit below, where the PWR_EN network controls the VSYS_3V3's DC/DC chip enable pin.



3.3 Switch and wake up

i.MX6ULL chip provides the switch of power management function. It is connected to the touch button through the ONOFF pin. When the VSNVS is powered, press about six seconds to pull low the ONOFF. The PMIC_ON_REQ will be pulled low through the above circuit. Connecting PMIC_ON_REQ to the enable of the VSYS_3V3 DC/DC chip will cause VSYS_3V3 to power down. Therefore, the whole board will be powered off except VSNVS. In the off state, short press the switch button to pull the ONOFF pin low for about 2 seconds, PMIC_ON_REQ will output a high level, then the whole board is powered on.

Sleep and wake up
Executing commands under Linux can put the system into a sleep state. At this time, PMIC_STBY_REQ is pulled high. The power management circuit on the core board reduces the core voltage VDD_SOC_IN to about 1.0V, and the core board VSYS_3V3 consumes <=9mA. In the standby status, through IO or other interrupt wake-up (requires software setting), PMIC_STBY_REQ is pulled low, the system will resume normal operation within 1S, and the core voltage will be adjusted to about 1.3V.

4. Start related circuit design

4.1 start mode and boot device

i.MX6ULx family, the startup mode is determined by the level sampling of the BOOT_MODE[1:0] pins during a Power-on Reset.

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

When BOOT_MODE[1:0] is 00, From i.MX6ULX chip internal FUSE sonfigurartion specified device and parameters to start
WT-SOM6ULX core board supports both NAND FLASH and EMMC. For regular device models, FUSE parameters are provided to avoid cumbersome pin configurations. Therefore, it is recommended to use the “Boot From Fuses” mode in applications that are mass-produced or not ready to replace storage devices.

When BOOT_MODE[1:0] is 01, you can download and burn system image files including

u-boot, zImage, dtb, rootfs, etc. through the Mfgtools programming tool (installed on Windows system) provided by NXP official website.

When BOOT_MODE[1:0] is 10, the i.MX6ULx chip samples the level of LCD_DATA[23:0] during power-on reset to determine the startup device and parameters. The specific description is as follow:

The relationship between the level of LCD_DATA[23:0] during power-on and the internal boot eFuse register is as follows:

Package pin	Direction on reset	eFuse
LCD1_DATA00	Input	BOOT_CFG1[0]
LCD1_DATA01	Input	BOOT_CFG1[1]
LCD1_DATA02	Input	BOOT_CFG1[2]
LCD1_DATA03	Input	BOOT_CFG1[3]
LCD1_DATA04	Input	BOOT_CFG1[4]
LCD1_DATA05	Input	BOOT_CFG1[5]
LCD1_DATA06	Input	BOOT_CFG1[6]
LCD1_DATA07	Input	BOOT_CFG1[7]
LCD1_DATA08	Input	BOOT_CFG2[0]
LCD1_DATA09	Input	BOOT_CFG2[1]
LCD1_DATA10	Input	BOOT_CFG2[2]
LCD1_DATA11	Input	BOOT_CFG2[3]
LCD1_DATA12	Input	BOOT_CFG2[4]
LCD1_DATA13	Input	BOOT_CFG2[5]
LCD1_DATA14	Input	BOOT_CFG2[6]
LCD1_DATA15	Input	BOOT_CFG2[7]
LCD1_DATA16	Input	BOOT_CFG4[0]
LCD1_DATA17	Input	BOOT_CFG4[1]
LCD1_DATA18	Input	BOOT_CFG4[2]
LCD1_DATA19	Input	BOOT_CFG4[3]
LCD1_DATA20	Input	BOOT_CFG4[4]
LCD1_DATA21	Input	BOOT_CFG4[5]
LCD1_DATA22	Input	BOOT_CFG4[6]
LCD1_DATA23	Input	BOOT_CFG4[7]

The startup device and device parameters determined by the eFuse register configuration are as follows:

FUSE MAP <Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
	0/1	0/1	0/1	1	0	0	0	0
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High! 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
	0	0	0	0	1	0	0	0
QSPI	Reserved	HSPHS: Half Speed Phase Selection '0' - select sampling at non inverted clock '1' - select sampling at inverted clock	HSDLY: Half Speed Delay- selection '0' - one clock delay '1' - two clock delay	FSPHS: Full Speed Phase Selection '0' - select sampling at non inverted clock '1' - select sampling at inverted clock	FSDLY: Full Speed Delay- selection '0' - one clock delay '1' - two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDMC1 01 - eSDMC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1 bit 001 - 4 bit 010 - 8 bit 101 - 4-bit DDR (MMC 4.4) 110 - 8 bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDMC1 01 - eSDMC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 8 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 1/2ms '1' - 2/2ms (LBA Nand)	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE _DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU _DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENA 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

Note: When the boot device specified by FUSE does not have a boot program available (such as DCD command), i.MX6ULL will first jump to the MMC/SD1 device boot mode, try to boot from the SD/TF card, if no boot program is available, then finally enter "Serial Downloader" mode.

Therefore, after i.MX6ULL has internally programmed FUSE, you can still enter SD/TF card boot or "Serial Downloader" mode by setting BOOT_MODE[1:0] to 10, "Internal Boot" mode. In order to simplify the complexity of the LCD configuration and to avoid the LCD screen driver lead uncertainty into the LCD_DATA[23:0] level sampling, it is recommended to use the default boot mode from "Boot from fuse".

4.2 Other hardware considerations related to startup

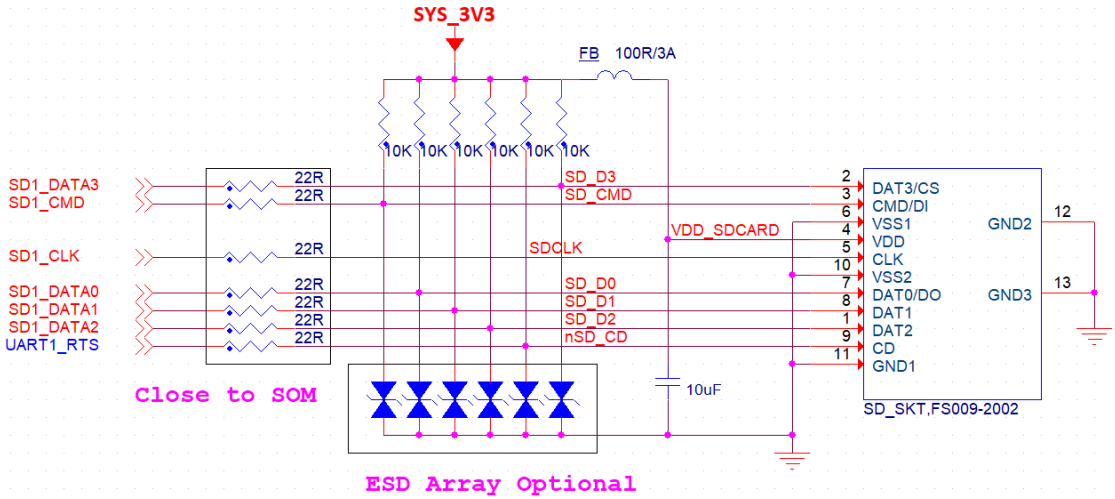
1) u-boot and Linux currently use UART1 as the debug serial port to print system messages. It should be layout from the baseboard and can be connected to the UART-USB bridge chip or connected to the PC via the RS232 interface convert chip.
2) Lead the SD1 interface to the SD card/TF card holder as much as possible. When the core board NAND FLASH/EMMC does not start the program, the system can be booted through SD1. Note that the UART1_RTS pin is used as the SD card detection pin by default. If the card is not detected, a 10K pull-down resistor can be added to the UART1_RTS pin.
3) Layout USB_OTG1_DN/USB_OTG1_DP to the MicroUSB holder as much as possible, and download the system software through NXP's Mfgtools tool.

5． TF/SD card circuit design

i.MX6ULL supports two high speed MMC/SD interfaces. Characters as follows:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The MMC/SD1 pin is fixed. When the default boot device fails to boot, it will attempt to boot from the SD1 connected SD/TF card.
The MMC/SD2 pin can be configured. When the core board adopts EMMC, the MMC/SD2 is used, and the pin is multiplexed with the NAND pin. When the core board adopts NAND FLASH, MMC/SD2 can be extended by multiplexing CSI or LCD pins, or connected to EMMC, or connected to SD/TF card, or connected to SDIO interface module (such as WIFI module).
The i.MX6ULL MMC/SD clock is up to 208MHz. In the design, the SDIO bus series matching resistor (usually 22R, placed close to the core board pin) must be used for the same length processing. The characteristic impedance is controlled at about 50 ohms.
The schematic diagram of the SD1 connection TF card holder reference is as follows:



MMC/SD1 connect SD card schematic diagram

MMC/SD2 pin assignment:

MMC/SD2 pin	Multiplex NAND pin group (core board solder EMMC)	Multiplex CSI pin group (core board solder NAND)	Multiplex LCD pin group(core board solder NAND)
SD2_CLK	NAND_RE_B	CSI_VSYNC	LCD_DATA19
SD2_CMD	NAND_WE_B	CSI_HSYNC	LCD_DATA18
SD2_DATA0	NAND_DATA00	CSI_DATA00	LCD_DATA20
SD2_DATA1	NAND_DATA01	CSI_DATA01	LCD_DATA21
SD2_DATA2	NAND_DATA02	CSI_DATA02	LCD_DATA22
SD2_DATA3	NAND_DATA03	CSI_DATA03	LCD_DATA23
SD2_DATA4	NAND_DATA04	CSI_DATA04	LCD_DATA14
SD2_DATA5	NAND_DATA05	CSI_DATA05	LCD_DATA15
SD2_DATA6	NAND_DATA06	CSI_DATA06	LCD_DATA16
SD2_DATA7	NAND_DATA07	CSI_DATA07	LCD_DATA17

6．LCD interface circuit

i.MX6ULL LCD interface characteristics:

- LCDIF supports one parallel 24-bit LCD display with up to WXGA (1366 x 768)
- resolution at 60 Hz
- 8/16/18/24/32 bit LCD data bus support available depending on I/O mux options.
- Support PXP 2D graphics acceleration

TFT LDC display is connected to RGB24 (RGB888) or RGB18 (RGB666). Pin definition as follows:

LCD pin	Core board pin number	RGB24 (RGB888)	RGB18 (RGB666)
LCD_DATA23	6	R7 red data MSB	-
LCD_DATA22	7	R6	-
LCD_DATA21	8	R5	-
LCD_DATA20	9	R4	-
LCD_DATA19	10	R3	-
LCD_DATA18	11	R2	-
LCD_DATA17	12	R1	R5 red data MSB
LCD_DATA16	13	R0 red data LSB	R4
LCD_DATA15	14	G7 green data MSB	R3
LCD_DATA14	15	G6	R2
LCD_DATA13	16	G5	R1
LCD_DATA12	17	G4	R0 red data LSB
LCD_DATA11	18	G3	G5green data MSB
LCD_DATA10	19	G2	G4
LCD_DATA9	20	G1	G3
LCD_DATA8	21	G0 green dataLSB	G2
LCD_DATA7	22	B7 blue dataMSB	G1
LCD_DATA6	23	B6	G0 green data LSB
LCD_DATA5	24	B5	B5 blue data MSB
LCD_DATA4	25	B4	B4
LCD_DATA3	26	B3	B3
LCD_DATA2	27	B2	B2
LCD_DATA1	28	B1	B1
LCD_DATA0	29	B0 blue data LSB	B0 blue data LSB
LCD_VSYNC	31	LCD vertical synchronization	
LCD_HSYNC	32	LCD horizontal synchronization	
LCD_PCLK	33	LCD pixel clock	
LCD_DE	34	LCD data enable	

LCD signal line design considerations:

- All signal lines in series with matched resistors (typically 22R) and placed close to the core board pins.
- It is recommended to use a trace with a characteristic impedance of 50 ohms.
- The length of the line is equal, and the relative length error is <=400mil

7．Touch screen interface circuit

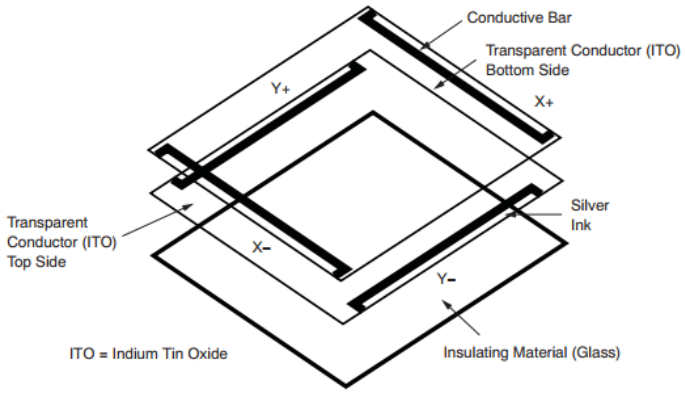
i.MX6ULL built in ADC controller, support 4-wire resistive touch screen. At the same time, the capacitive touch screen is supported through the I2C/USB interface.

7.1 resistance TP circuit

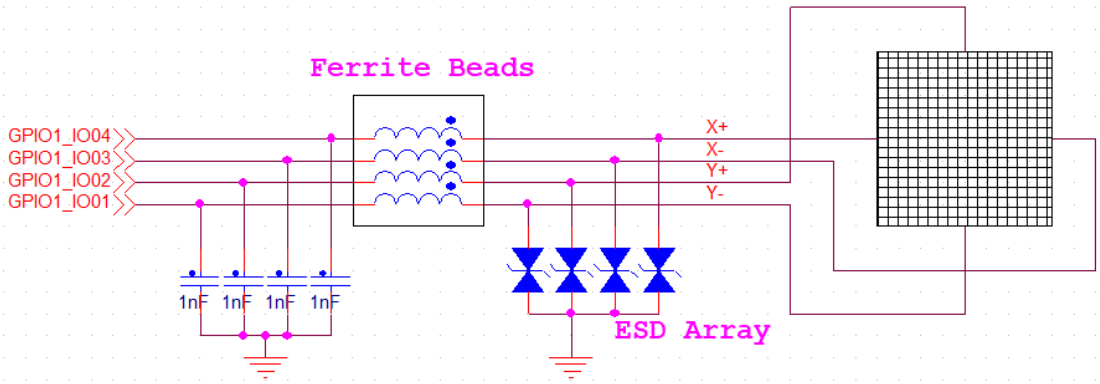
Resistance TP pin definition:

Core board pin definition	Core board pin number	Resistance TP definition
GPIO1_IO04	91	X+
GPIO1_IO03	92	X-
GPIO1_IO02	93	Y+
GPIO1_IO01	94	Y-

Resistance TP use and connection mode reference:



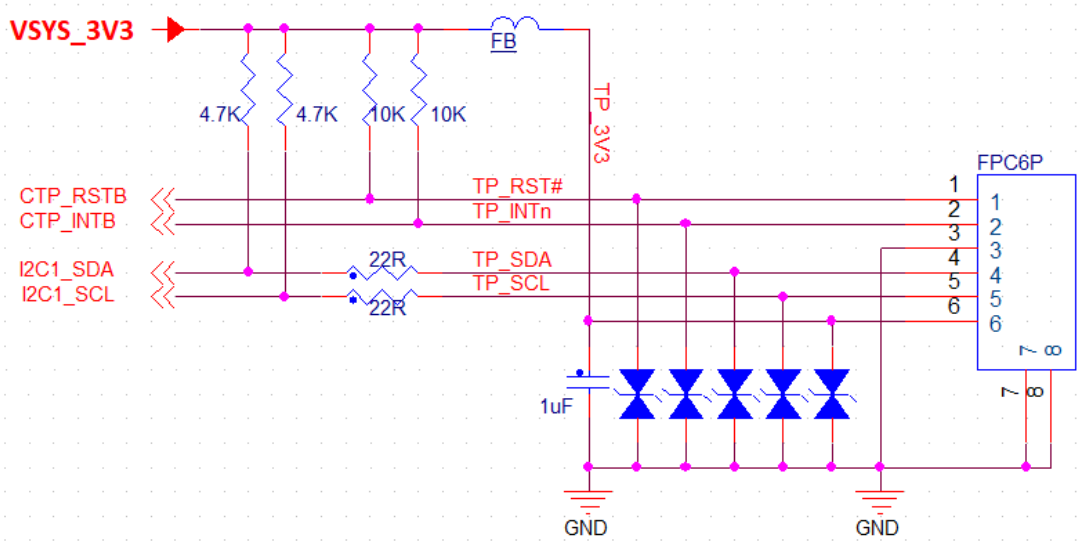
Resistance TP structure diagram



i.MX6ULL connect 4-wire resistance TP schematic

7.2 capacitance TP

A common capacitor TP circuit diagram based on I2C interface is as follows:



Capacitor TP interface circuit

Among them, the RST (reset pin) and INT (interrupt pin) of the capacitor TP can be configured as any pin with GPIO function.

8. IIC interface

i.MX6ULL provides up to 4 I2C interfaces. It can be flexibly allocated through pin multiplexing.

I2C1 signal reusable list

I2C1 signal	Core board pin name	Core board pin number
I2C1_SCL	CSI_PIXCLK	44
	GPIO1_IO02	93
	UART4_TX_DATA	112
I2C1_SDA	CSI_MCLK	43
	GPIO1_IO03	92
	UART4_RX_DATA	111

I2C2 signal reusable list

I2C2 signal	Core board pin name	Core board pin number
I2C2_SCL	CSI_HSYNC	46
	GPIO1_IO00	95
	UART5_TX_DATA	113
I2C2_SDA	CSI_VSYNC	45
	GPIO1_IO01	94
	UART5_RX_DATA	114

I2C3 signal reusable list

I2C3 signal	Core board pin name	Core board pin number
I2C3_SCL	ENET2_RXD0	119
	LCD_DATA1	28
	UART1_TX_DATA	102
I2C3_SDA	ENET2_RXD1	118
	LCD_DATA0	29
	UART1_RX_DATA	101

I2C4 signal reusable list

I2C4 signal	Core board pin name	Core board pin number
I2C4_SCL	ENET2_TXEN	121
	LCD_DATA3	26
	UART2_TX_DATA	106
I2C4_SDA	ENET2_TXD0	123
	LCD_DATA2	27
	UART2_RX_DATA	105

9. USB interface

i.MX6ULL have 2 way USB 2.0 controller. Each USB OTG controller core can operate in High Speed operation (480 Mbps), Full Speed operation (12 Mbps) and Low Speed operation (1.5 Mbps).

2 way USB related pin

USB signal name	**Function description**	**Reusable pin**	**Pin number**
USB_OTG2_VBUS	USB power supply pin (5V input)	-	76
USB_OTG2_DP	USB Differential signal	-	72
USB_OTG2_DN	USB Differential signal	-	71
USB_OTG2_ID	USB ID signal	ENET2_TX_CLK	120
		GPIO1_IO05	90
		SD1_DATA3	38
USB_OTG2_OC	USB power overcurrent signal (input)	ENET2_TXEN	121
		GPIO1_IO03	92
		SD1_DATA2	39
USB_OTG2_PWR	USB power output control signal	ENET2_TXD1	122
		GPIO1_IO02	93
		SD1_DATA1	40
USB_OTG1_VBUS	VBUS power input（5V）	-	77
USB_OTG1_DP	USB differential signal	-	74

USB_OTG1_DN	USB differential signal	-	75
USB_OTG1_ID	OTG ID signal	GPIO1_IO00	95
		SD1_DATA0	41
		UART3_TX_DATA	110
USB_OTG1_OC	USB power overcurrent signal (input)	ENET2_RXD1	118
		GPIO1_IO01	94
		SD1_CLK	36
USB_OTG1_PWR	USB power output control signal	ENET2_RXD0	119
		GPIO1_IO04	91
		SD1_CMD	37

USB interface circuit design notice

About USB power supply, USB_OTG2_VBUS and USB_OTG1_VBUS may not be powered if the USB function is not used. If the USB function is used, the USB_OTG2_VBUS must be powered by 5V, and the power-on sequence is after VSYS_3V3. USB_OTG1_VBUS can be used as an OTG VBUS input, it have to ensure to allow USB_OTG1_VBUS input power after VSYS_3V3.

The system defaults OTG1 as a USB Device to facilitate the Mfgtools tool to download and program system programs.

When more than 2 USB Hosts are required, they are generally extended by a USB Hub chip (such as USB2514).

10. Ethernet interface

i.MX6ULL implements a dual-speed 10/100-Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100-Mbit/s Ethernet LANs.

A LAN8720A Ethernet physical chip has been installed on the WT-SOM6ULX core board. It is connected to the ENET1 RMII interface and extends the ETH1 receive and transmit differential pair signal and LED indicator through the core board pins. The LAN8720A is a low-power 10/100Mbps adaptive Ethernet physical chip from MICROCHIP that supports HP Auto-MDIX features.

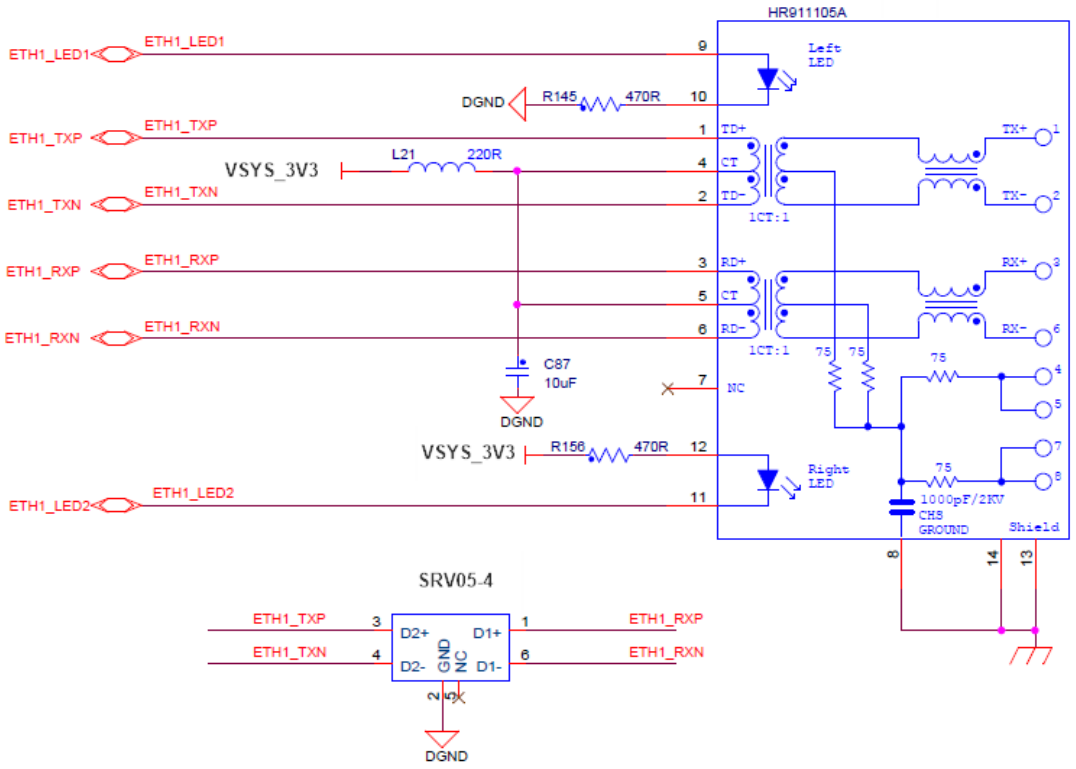
The WT-SOM6ULX core board extends the corresponding pins of the ENET2 RMII interface, as well as the MDIO/MDC pins. A LAN8720A can be extended on the baseboard to implement dual network port configuration.

ENET1 extended pin description

Pin name	Pin number	Pin description
ETH1_TXN	1	ENET1 transmit-/ data A-
ETH1_TXP	2	ENET1 transmit+/ data A+
ETH1_RXN	3	ENET1 receive-/ data B-
ETH1_RXP	4	ENET1 receive+/ data B+

ETH1X_LED1	128	Lan8720A Link activity LED **Active High**
ETH1X_LED2	127	LAN8720A Speed LED(100M or 10Mbps) **Active Low**

ENET1 connect RJ45 reference schematic as below:



ENET1 connect RJ45 schematic

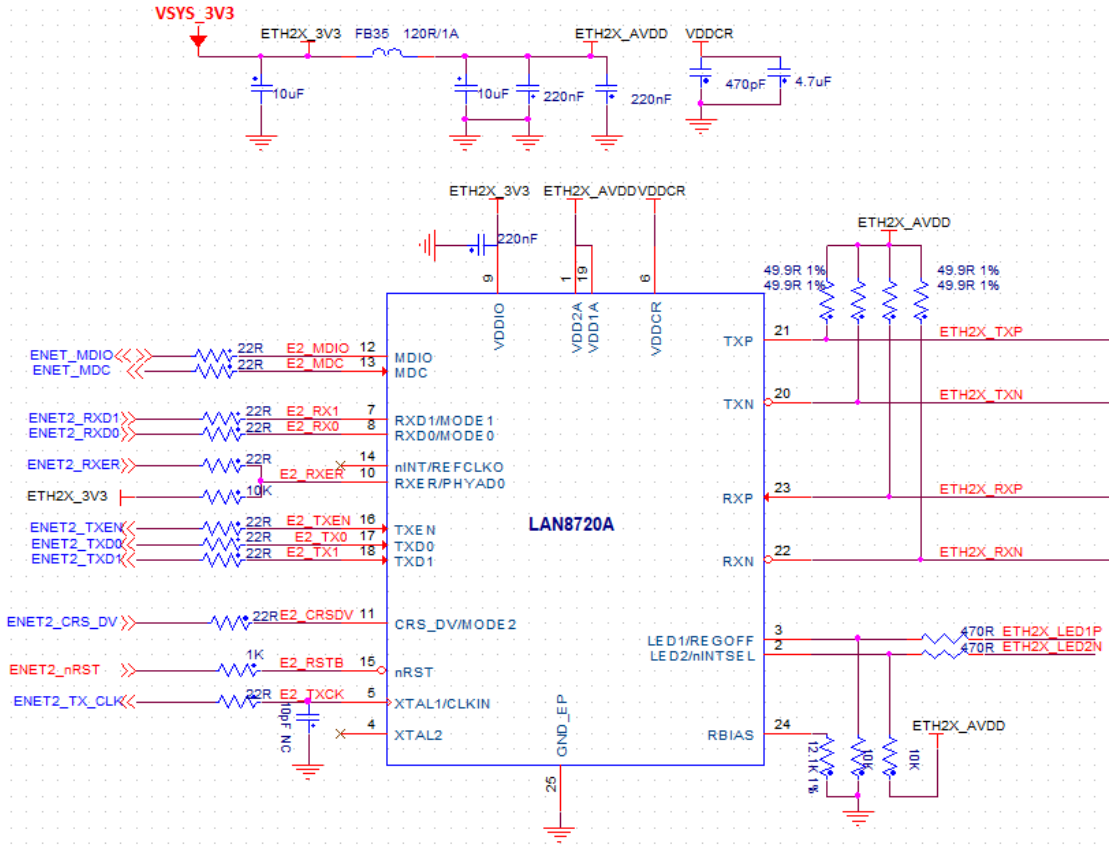
When there is a dual network port requirement, the ENET2 can be extended by connecting the LAN8720A through the ENET2 RMII interface.

ENET2 RMII interface signal definition and related pin list:

ENET2 RMII interface	Core board pin number	Description
ENET2_CRS_DV	116	RMII RX Enable
ENET2_RXER	117	RMII PHY error detect
ENET2_RXD1	118	RMII Data1 receive from PHY
ENET2_RXD0	119	RMII Data0 receive from PHY
ENET2_TX_CLK	120	RMII 50MHZ Clock from MAC to PHY
ENET2_TXEN	121	RMII TX Enable
ENET2_TXD1	122	RMII Data1 transmit to PHY
ENET2_TXD0	123	RMII Data0 transmit to PHY
ENET_MDC	**124**	**SMI Clock 2.5MHz**
ENET_MDIO	**125**	**SMI MDIO, already pulled up with 1.5K on**

Precautions:

1. The SMI serial bus ENET_MDC, ENET_MDIO is not configurable for other functions unless the core board LAN8720A is not installed. ENET_MDIO has been pulled up from 1.5K ohms to 3.3V on the core board.
2. ENET1 and ENET2 share the same set of SMI serial bus (ENET_MDC, ENET_MDIO), so the two PHY chips must be configured with different PHY addresses. The LAN8720A PHY address installed on the WT-SOM6ULX module default is configured to 0x00. Therefore, if ENET2 is extended on the baseboard, the PHY address can't be 0x00. If the LAN8720A is used to extend ENET2, the PHY address must be configured to 0x1, and the LAN8720A PHYAD0 configuration pin (pin 10) must be pulled up from 10K ohms to 3.3V.
3. ENET2 RMII interface should be connected in series with matching resistors (generally about 22R), the series match resistor must be close to the signal output pin. RMII routing should be treated as equal length.



ENET2 extended schematic (LAN8720A)

11. Serial port

i.MX6ULL support 8 UART. High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s。

UAR1T~UART8's signal definition and reusable pin list:

UART signal	Description	Direction	Core board pin	Pin number
UART1_CTS_B	Clear to send	Input	UART1_CTS	99
UART1_RTS_B	Request to send	Output	UART1_RTS	100
UART1_RX_DATA	Serial data receive	Input	UART1_RX_DATA	101
			GPIO1_IO03	92
UART1_TX_DATA	Serial data transmit	Output	UART1_TX_DATA	102
			GPIO1_IO02	93
UART2_CTS_B	Clear to send	Input	UART2_CTS	103
UART2_RTS_B	Request to send	Output	UART2_RTS	104
UART2_RX_DATA	Serial data receive	Input	UART2_RX_DATA	105
UART2_TX_DATA	Serial data transmit	Output	UART2_TX_DATA	106
UART3_CTS_B	Clear to send	Input	UART3_CTS	107
UART3_RTS_B	Request to send	Output	UART3_RTS	108
UART3_RX_DATA	Serial data receive	Input	UART3_RX_DATA	109
UART3_TX_DATA	Serial data transmit	Output	UART3_TX_DATA	110
UART4_CTS_B	Clear to send	Input	LCD_HSYNC	32
UART4_RTS_B	Request to send	Output	LCD_VSYNC	31
UART4_RX_DATA	Serial data receive	Input	UART4_RX_DATA	111
UART4_TX_DATA	Serial data transmit	Output	UART4_TX_DATA	112
UART5_CTS_B	Clear to send	Input	CSI_DATA03	50
			GPIO1_IO09	88
UART5_RTS_B	Request to send	Output	CSI_DATA02	49
			GPIO1_IO08	89
UART5_RX_DATA	Serial data receive	Input	CSI_DATA01	48
			GPIO1_IO05	90
			UART5_RX_DATA	114
UART5_TX_DATA	Serial data transmit	Output	CSI_DATA00	47
			GPIO1_IO04	91
			UART5_TX_DATA	113
UART6_CTS_B	Clear to send	Input	CSI_HSYNC	46
UART6_RTS_B	Request to send	Output	CSI_VSYNC	45
UART6_RX_DATA	Serial data receive	Input	CSI_PIXCLK	44
			ENET2_RXD1	118
UART6_TX_DATA	Serial data transmit	Output	CSI_MCLK	43
			ENET2_RXD0	119
UART7_CTS_B	Clear to send	Input	LCD_DATA6	23
UART7_RTS_B	Request to send	Output	LCD_DATA7	22

UART7_RX_DATA	Serial data receive	Input	ENET2_TXD0	123
			LCD_DATA17	12
UART7_TX_DATA	Serial data transmit	Output	ENET2_CRS_DV	116
			LCD_DATA16	13
UART8_CTS_B	Clear to send	Input	ENET2_TX_CLK	120
			LCD_DATA4	25
UART8_RTS_B	Request to send	Output	ENET2_RXER	117
			LCD_DATA5	24
UART8_RX_DATA	Serial data receive	Input	ENET2_TXEN	121
			LCD_DATA21	8
UART8_TX_DATA	Serial data transmit	Output	ENET2_TXD1	122
			LCD_DATA20	9

12. Audio interface

1) SAI interface

i.MX6ULL have 3 ESAI interfaces, The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs,Sony/Phillips Digital Interface (SPDIF) transceivers, and other DSPs.

SAI interface pin（IIS mode）definition（SAI2）

SAI2 pin signal	**Core board pin name**	**Core board pin number**	**Description**
SAI2_RXD	JTAG_TCK	82	Serial input data
SAI2_MCLK	JTAG_TMS	83	Main clock output
SAI2_TX_BCLK	JTAG_TDI	84	Data bit clock
SAI2_TX_SYNC	JTAG_TDO	85	Left and right channel sync signal
SAI2_TXD	JTAG_nTRST	86	Serial output data

2) SPDIF Interface

i.MX6ULL support SPDIF interface， The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio.

SPDIF output reusable pin list (default is JATG_MOD)

SPDIF output signal	**Reusable pin**	**Pin number**
SPDIF_OUT	GPIO1_IO08	89
	JTAG_MOD	**87**
	LCD_DATA5	24
	SD1_CMD	37
	UART1_TX_DATA	102

13. RTC circuit

i.MX6ULL built in RTC, the VSNVS pin is powered by the backup battery. After the main power is turned off, the RTC clock can still record the time, the VSNVS current consumption is about 20uA.

To maintain RTC time for a long time, consider using an external RTC chip such as PCF8563.

14. PWM

i.MX6ULL support 8 way PWM output

WT-SOM6ULX PWM signal's reusable pin list:

PWM signal	Reusable pin	Pin number of module
PWM1_OUT	GPIO1_IO08	89
	LCD_DATA0	29
PWM2_OUT	GPIO1_IO09	88
	LCD_DATA1	10
PWM3_OUT	GPIO1_IO04	91
	LCD_DATA2	27
PWM4_OUT	GPIO1_IO05	90
	LCD_DATA3	26
PWM5_OUT	LCD_DATA18	11
PWM6_OUT	JTAG_TDI	84
	LCD_DATA19	10
PWM7_OUT	CSI_VSYNC	45
	JTAG_TCK	82
PWM8_OUT	CSI_HSYNC	46
	JTAG_nTRST	86

15. SPI

i.MX6ULL support maximum 4 way ECSPI interface.

ECSPI1

ECSPI1 signal	Reusable pin	Pin number of module
ECSPI_MISO	CSI_DATA07	54
	LCD_DATA23	6
ECSPI_MOSI	CSI_DATA06	53
	LCD_DATA22	7
ECSPI_SCLK	CSI_DATA04	51
	LCD_DATA20	9

ECSPI_SS0	CSI_DATA05	52
	LCD_DATA21	8
ECSPI_SS1	LCD_DATA5	24
ECSPI_SS3	LCD_DATA6	23
ECSPI_SS4	LCD_DATA7	22

ECSPI2

ECSPI2 signal	Reusable pin	Pin number of module
ECSPI_MISO	CSI_DATA03	50
	UART5_RX_DATA	114
ECSPI_MOSI	CSI_DATA02	49
	UART5_TX_DATA	113
ECSPI_SCLK	CSI_DATA00	47
	UART4_TX_DATA	112
ECSPI_SS0	CSI_DATA01	48
	UART4_RX_DATA	111
ECSPI_SS1	LCD_HSYNC	32
ECSPI_SS3	LCD_VSYNC	31
ECSPI_SS4	LCD_RESET	30

ECSPI3

ECSPI3 signal	Reusable pin	Pin number of module
ECSPI_MISO	UART2_RTS	104
ECSPI_MOSI	UART2_CTS	103
ECSPI_SCLK	UART2_RX_DATA	105
ECSPI_SS0	UART2_TX_DATA	106

ECSPI4

ECSPI4 signal	Reusable pin	Pin number of module
ECSPI_MISO	ENET2_TX_CLK	120
ECSPI_MOSI	ENET2_TXEN	121
ECSPI_SCLK	ENET2_TXD1	122
ECSPI_SS0	ENET2_RXER	117

16. CAN bus

i.MX6ULL support 2 ways FLEXCAN bus interface, compliance with CAN 2.0B protocol.
WT-SOM6ULX support FLEXCAN reusable pin list:

FLEXCAN pin definition	reusable pin	Pin number of module
FLEXCAN1_RX	LCD_DATA9	20
	SD1_DATA1	40
	UART3_RTS	108
FLEXCAN1_TX	LCD_DATA8	21

	SD1_DATA0	41
	UART3_CTS	107
FLEXCAN2_RX	LCD_DATA11	18
	SD1_DATA3	38
	UART2_RTS	104
FLEXCAN2_TX	LCD_DATA10	19
	SD1_DATA2	39
	UART2_CTS	103

17. CSI camera interface

i.MX6ULL supports parallel CSI camera interface, supports CCIR656 standard format, supports 8/12/24 bit YUV/YCrCb / RGB data bits, and supports up to 5-Megapixel. Commonly used 8-bit CSI interface signal definition and reusable pins:

CSI signal definition	Direction	Core board pin	Pin number	Description
DATA2	Input	CSI_DATA00	47	Data Sensor Signal 2
DATA3	Input	CSI_DATA01	48	Data Sensor Signal 3
DATA4	Input	CSI_DATA02	49	Data Sensor Signal 4
DATA5	Input	CSI_DATA03	50	Data Sensor Signal 5
DATA6	Input	CSI_DATA04	51	Data Sensor Signal 6
DATA7	Input	CSI_DATA05	52	Data Sensor Signal 7
DATA8	Input	CSI_DATA06	53	Data Sensor Signal 8
DATA9	Input	CSI_DATA07	54	Data Sensor Signal 9
FIELD	Input	GPIO1_IO05	90	CSI Field Signal
HSYNC	Input	CSI_HSYNC	46	Horizontal Sync (Blank Signal)
MCLK	Output	CSI_MCLK	43	CMOS Sensor Master Clock
PIXCLK	Input	CSI_PIXCLK	44	Pixel Clock
VSYNC	Input	CSI_VSYNC	45	Vertical Sync (Start Of Frame)

Description:

- To connect with one 8-bit sensor, the sensor data interface should connect to
- CSI_DATA[9:2] .
- MCLK is provided by the CCM module directly, not from the CSI module itself
- Need to connect 10,16,24bit camera interface, please refer to i.MX6ULL Reference Manual.

18. ADC interface

i.MX6ULL internal have 2 ADC controller, ADC resolution ratio is 12bit. WT-SOM6ULX support 8 ways ADC input, of which ADC_VREFH reference voltage on board connected to 3.3V, so all ADC input signal voltages range from [0 , 3.3V]. ADC related signal definition and pinouts:

ADC input signal	Reusable pin	Pin number
ADC1_IN0/ADC2_IN0	GPIO1_IO00	95
ADC1_IN1/ADC2_IN1	GPIO1_IO01	94
ADC1_IN2/ADC2_IN2	GPIO1_IO02	93
ADC1_IN3/ADC2_IN3	GPIO1_IO03	92
ADC1_IN4/ADC2_IN4	GPIO1_IO04	91
ADC1_IN5/ADC2_IN5	GPIO1_IO05	90
ADC1_IN8/ADC2_IN8	GPIO1_IO08	89
ADC1_IN9/ADC2_IN9	GPIO1_IO09	88