REF Schematic for RK3568

Main Functions Introduction

1) PMIC: RK809-5+DiscretePower
2) RAM: DDR4 2x16Bit------------------Default
   Option:LPDDR4/4x 1X32bit(200ball)
   Option:DDR3 4x16bit
   Option:DDR3 4x16bit+2x16bit ECC
   Option:DDR4 2x16bit+1x16bit ECC
   Option:LPDDR3 1x32bit(178ball)
   Option:DDR4 4x16bit
3) ROM: eMMC--------------------------Default
   Option:Nand Flash
   Option:SPI Flash
4) Support:1 x Micro SD Card3.0
5) Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2 ----------Default
   Option:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
6) Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3 -- ------Default
7) Support:4G module Via MiniPCIe2.0 Slot With PCIE2.0 and USB2.0 HOST3 function------Option
8) Support:2 x 1Lane PCIe3.0 Connector (RC Mode) ------Default
   Option:1 x 2Lanes PCIe3.0 Connector (RC Mode)
   Option:1 x 2Lanes PCIe3.0 Connector (EP Mode)
9) Support:1 x HDMI2.0 TX
10) Support:1 x LCM MIPI DSI TX0 ----------Default
   Option:1 x LCM MIPI DSI TX1
   Option:1 x LCM LVDS TX
   Option:1 x LCM Dual MIPI DSI TX
   Option:1 x LCM eDP TX
11) Support:1 x VGA OUT ----------Default
12) Support:1 x 4Lanes Camera MIPI CSI RX ----------Default
   Option:2 x 2Lanes Camera MIPI CSI RX
   Option:1 x HDMI1.4 RX(HDMI to MIPI CSI)
13) Support:a/b/g/n/ac 2X2 SDIO WIFI5+BT5.0+PCM --------Default
   Option:a/b/g/n/ac 1X1 SDIO WIFI+BT+PCM
   Option:a/b/g/n/ac/ax 2X2 PCIe WIFI6+BT5.0+PCM
14) Support:1 x 10/100/1000M Ethernet(RGMII1_M1) -------Default
   Option:1 x 10/100/1000M Ethernet(RGMII0) or 1 x 10/100M Ethernet(RMII0)
   Option:1 x 10/100/1000M PCIe Ethernet Card or 2 x 10/100/1000 Ethernet(QSGMII) or 1 x 10/100/1000 Ethernet(SGMII)
15) Support:1 x Headphone output ----------Default
16) Support:1 x ECM MIC + 1 x Speaker out ----------Default
   Option:4 x MEMS MIC + 1 x Speaker out + Loopback or 2 x MEMS MIC + 1 x Speaker out + Loopback
   Option:4 x MEMS MIC + 2 x Speaker out + Loopback
17) Support:1 x IR Receiver ----------Default
18) Support:Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
19) Support:3 x UART + 1 x RS485 + 1 x CAN FD(Option)
20) Support:Debug UART and ARM JTAG

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File:	00.Cover Page				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
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Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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File:	01.Index and Notes				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 72

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-04	Zhangdz	1:Revision preliminary version	
V1.1	2021-06-11	Zhangdz	1:Change content Please Refer to: RK3568_AIoT_REF_SCH_V11_20210611_Modify_Notes	

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Project:	RK3568_AIoT_PC_SCH				
File:	02.Revision History				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
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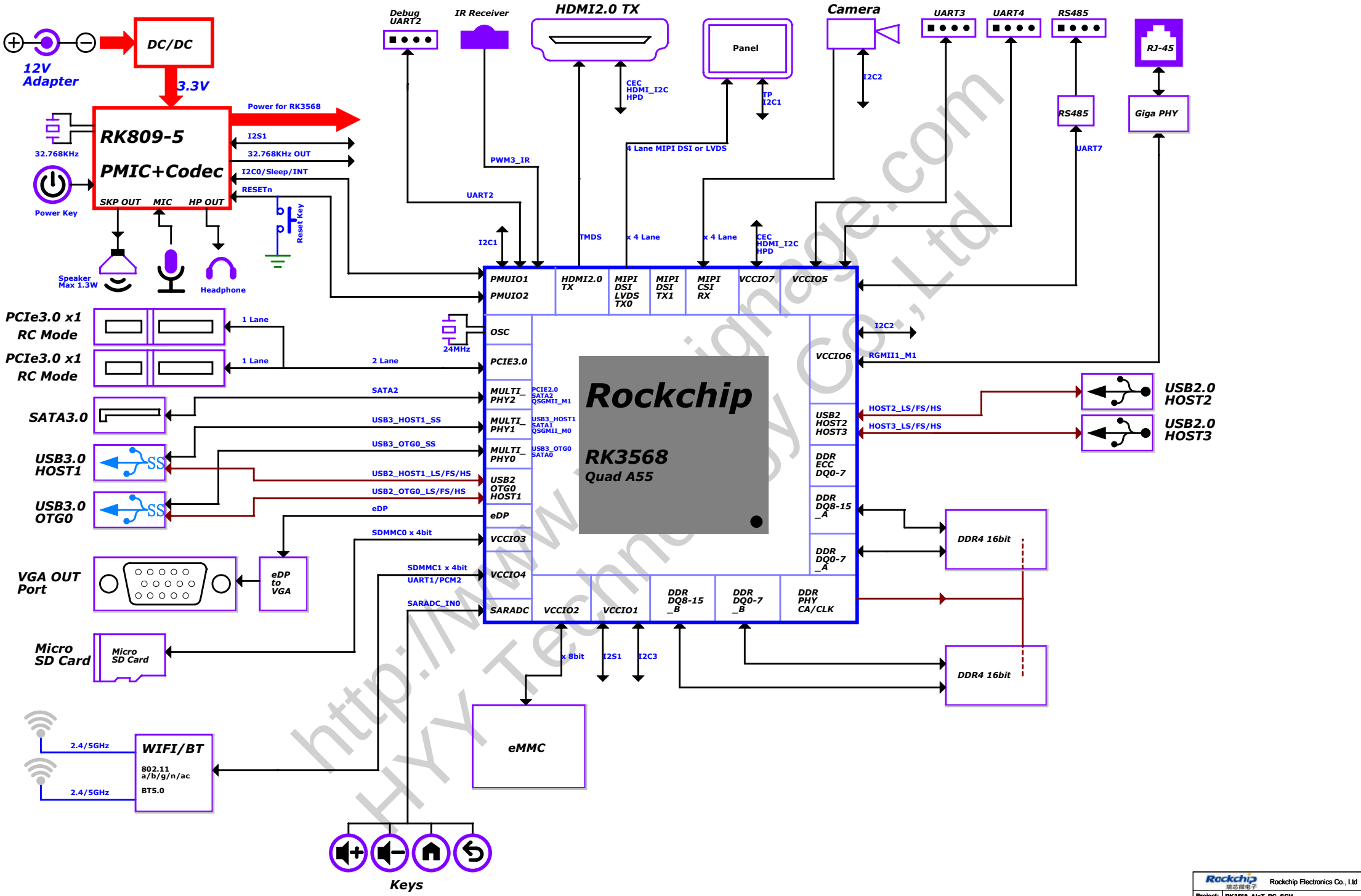
RK3568 Ref Block Diagram(Default configuration)



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File:	03.Block Diagram
Date:	Wednesday, June 08, 2022
Rev:	V1.1
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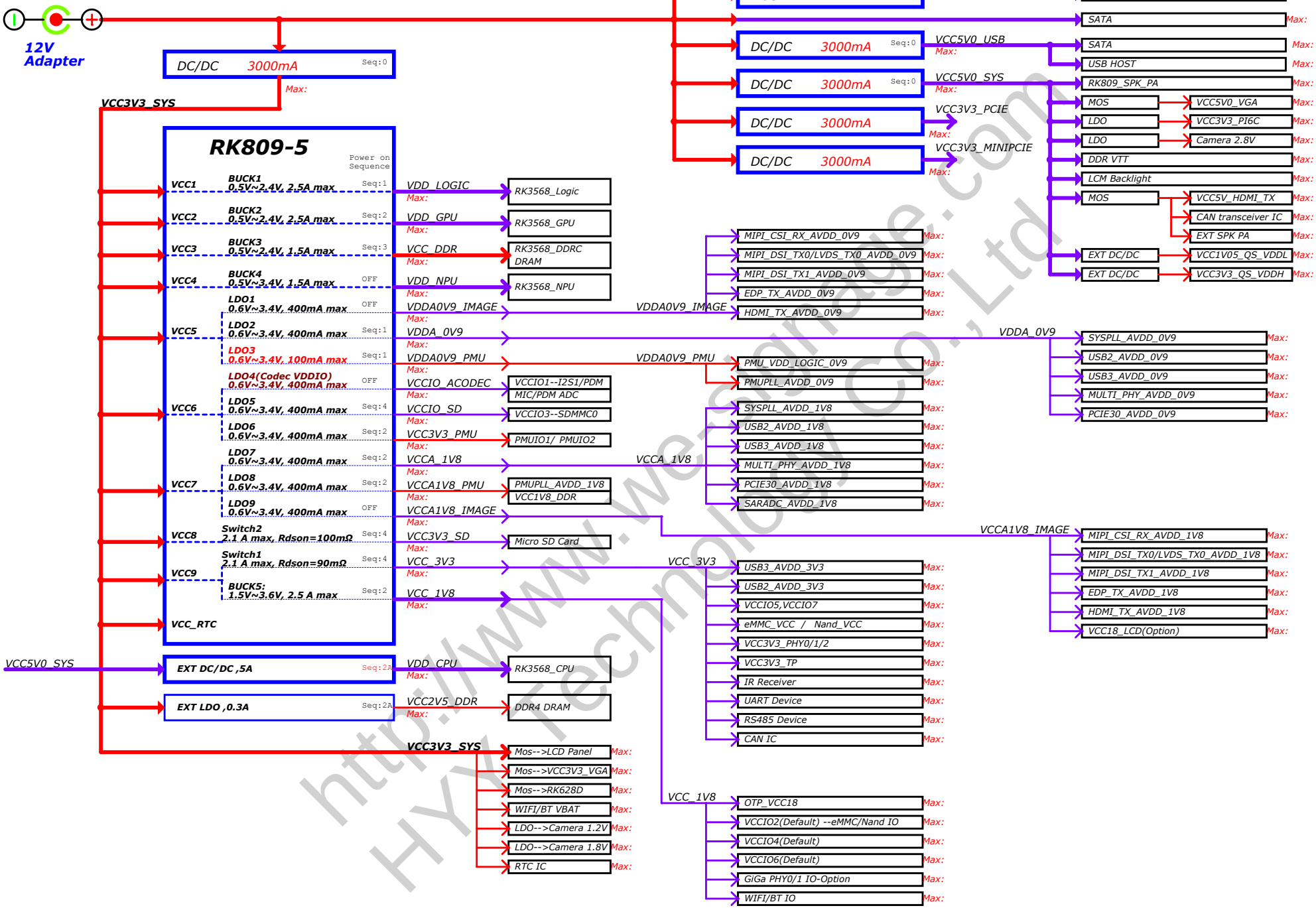
Sheet	4 of 72

Default Power Diagram



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File:	04.Power Diagram
Date:	Wednesday, June 08, 2022
Rev:	V1.1
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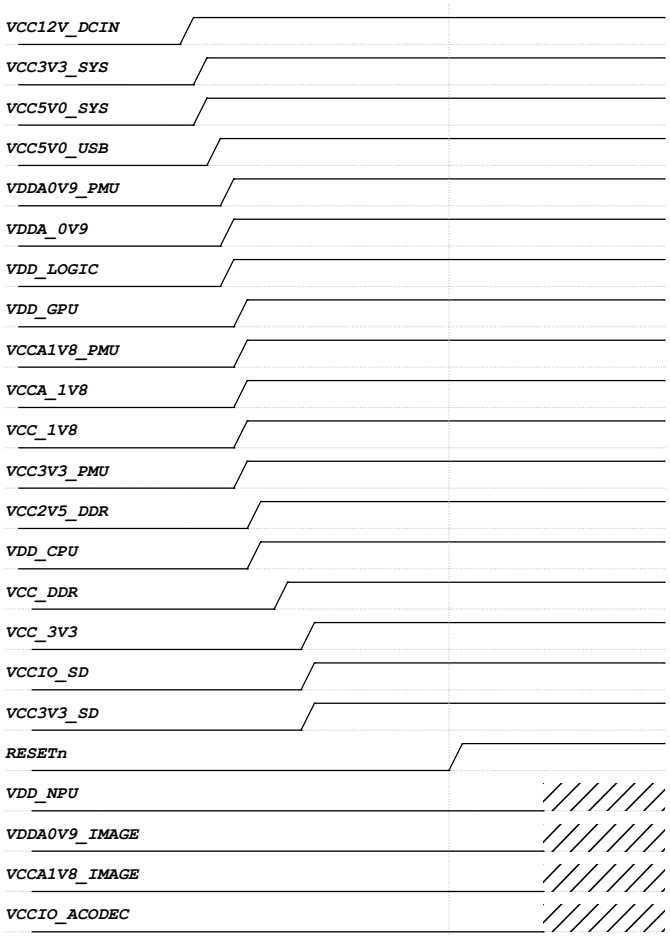
Sheet	5 of 72

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

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File:	05.Power Sequence				
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IO Power Domain Map

If IO domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

IO Domain	Pin Num	Support IO Voltage		Notes	Default IO Domain Voltage		
		3.3V	1.8V		Supply Power Net Name	Power Source	Voltage
PMUIO0 (PMUPLL_AVDD_1V8)	Pin Y21	✗	✓	PMUIO0 are fixed 1.8V level mode, which cannot be configured.	VCCA1V8_PMU	VCCA1V8_PMU	1.8V
PMUIO1	Pin Y20	✓	✗	PMUIO1 are fixed 3.3V level mode, which cannot be configured.	VCC3V3_PMU	VCC3V3_PMU	3.3V
PMUIO2	Pin W19	✓	✓	PMUIO2 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC3V3_PMU	VCC3V3_PMU	3.3V
VCCIO1	Pin H17	✓	✓	VCCIO1 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO_ACODEC	VCCIO_ACODEC	3.3V
VCCIO2	Pin H18	✓	✓	VCCIO2 supports 1.8V or 3.3V level mode Default is configured by hardware,namely PIN "FLASH_VOL_SEL" state determines which mode to work in.[1][2]	VCCIO_FLASH	VCC_1V8	1.8V
VCCIO3	Pin L22	✓	✓	VCCIO3 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2][3]	VCCIO_SD	VCCIO_SD	3.3V
VCCIO4	Pin J21	✓	✓	VCCIO4 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO4	VCC_1V8	1.8V
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO6	VCC_1V8	1.8V
VCCIO7	Pin V12	✓	✓	VCCIO7 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V

For example, the VCCIO4 hardware has been modified to 3.3V power supply, and the corresponding DTS must be modified to 3.3V configuration, otherwise the IO of VCCIO4 will be damaged.

If a board needs to be compatible with two voltage choices, recommended to enable BOM ID

Notes

[1]:When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

[2]:When the IO domain power supply voltage is 1.8V, the IO domain voltage configuration in DTS must be set to 1.8V mode.
If it is misconfigured to 3.3V mode, the IO function of this power domain will be abnormally;
When the IO domain power supply voltage is 3.3V, the IO domain voltage configuration in DTS must be set to 3.3V mode.
If it is misconfigured to 1.8V mode, the IO in this power domain will be in overvoltage state, and the IO will be damaged after long-term operation.

[3]:When VCCIO3 IO domain is assigned as SD card function,:
If SD3.0 mode is to be supported, VCCIO3 power supply voltage must be support configurable, 3.3V in SD2.0 mode and 1.8V in SD3.0 mode.
If only SD2.0 mode is supported (SD3.0 card only works in SD2.0 mode), VCCIO3 only needs fixed power supply of 3.3V.
When VCCIO3 IO domain is assigned as other function,:
Such as uart5 and uart6, then note [2] should be followed

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File:	06.IO Power Domain Map			
Date:	Wednesday, June 08, 2022		Rev:	V1.1
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	7 of 72

Default UART Map

RK3568

UART0

UART1 — Mux — M0: UART1_M0 → BT; M1

UART2 — Mux — M0: UART2_M0 → Debug UART2 Port; M1

UART3 — Mux — M0; M1: UART3_M1 → ●●●■

UART4 — Mux — M0; M1: UART4_M1 → ●●●■

UART5 — Mux — M0; M1

UART6 — Mux — M0; M1: UART6_M1 → ●●●■

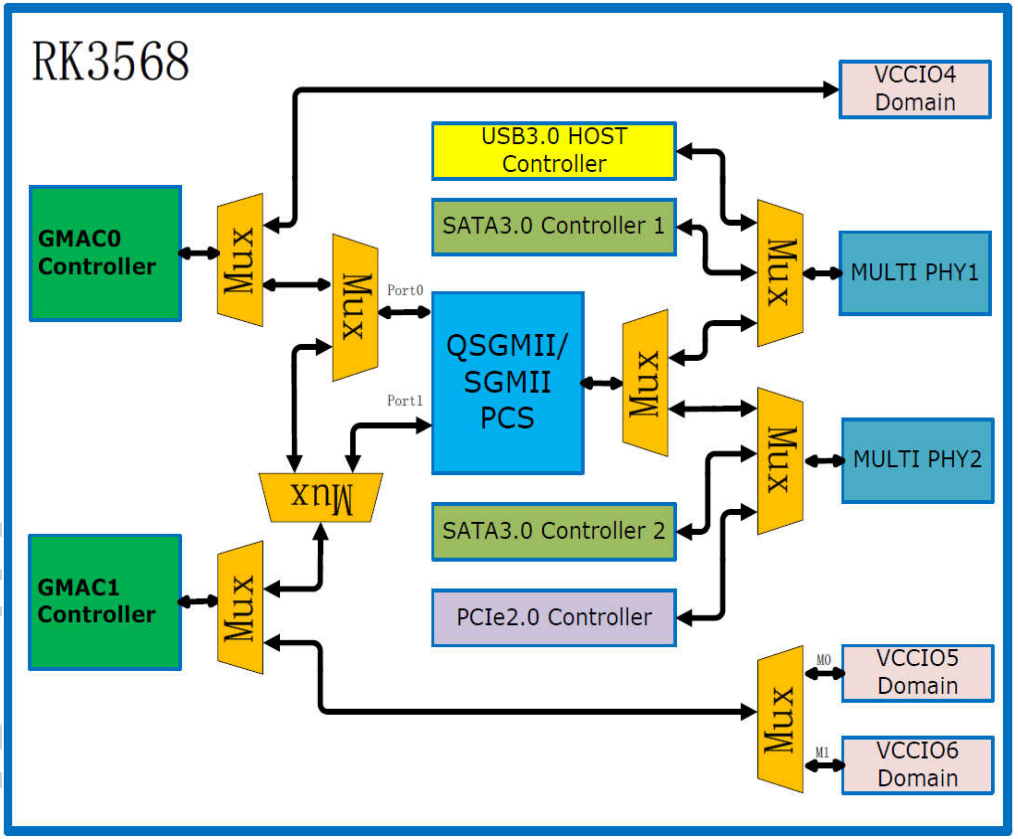
If no MicroSD Card function

UART7 — Mux — M0; M1: UART7_M1 → RS485 → RS485 → ●●●■; M2

UART8 — Mux — M0; M1

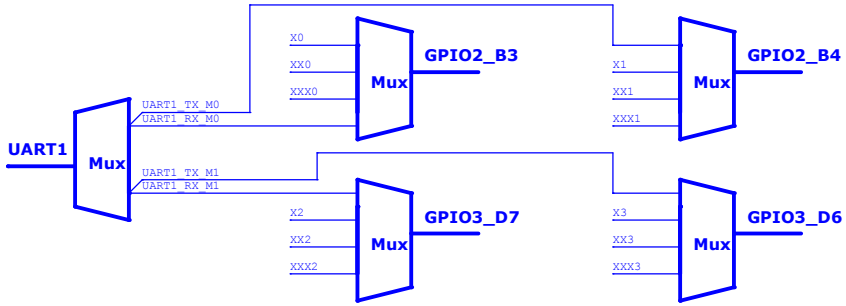
UART9 — Mux — M0; M1: UART9_M1 → ●●●■; M2

GMAC0/1 Path Map



Note:

M0 M1 M2 indicates that the same function is multiplexed to different IO
When selecting, only M0 or M1 or M2 can be selected
eg:Not supported UART1_TX_M0 and UART1_RX_M1 combination



It is suitable for other interfaces

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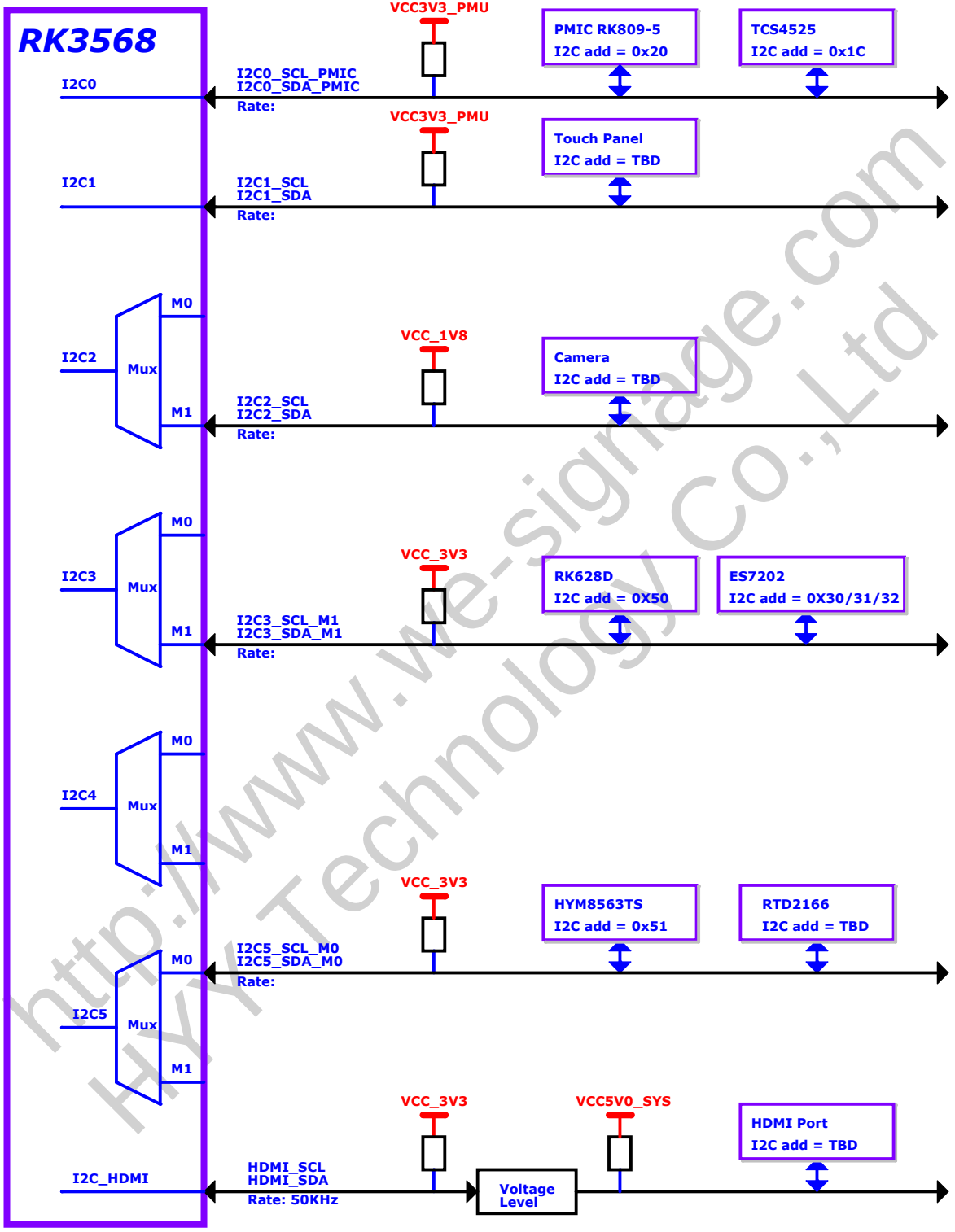
Project:	RK3568_AIoT_PC_SCH				
File:	07.UART Map/GMAC0/1 Path Map				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	8 of 72

Default I2C Map

Note:
M0 M1 M2 indicates that the same function is multiplexed to different IO. When selecting, only M0 or M1 or M2 can be selected
eg:
Not supported I2C1_SCL_M0 and I2C1_SDA_M1 combination



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File:	08.I2C Bus Map				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
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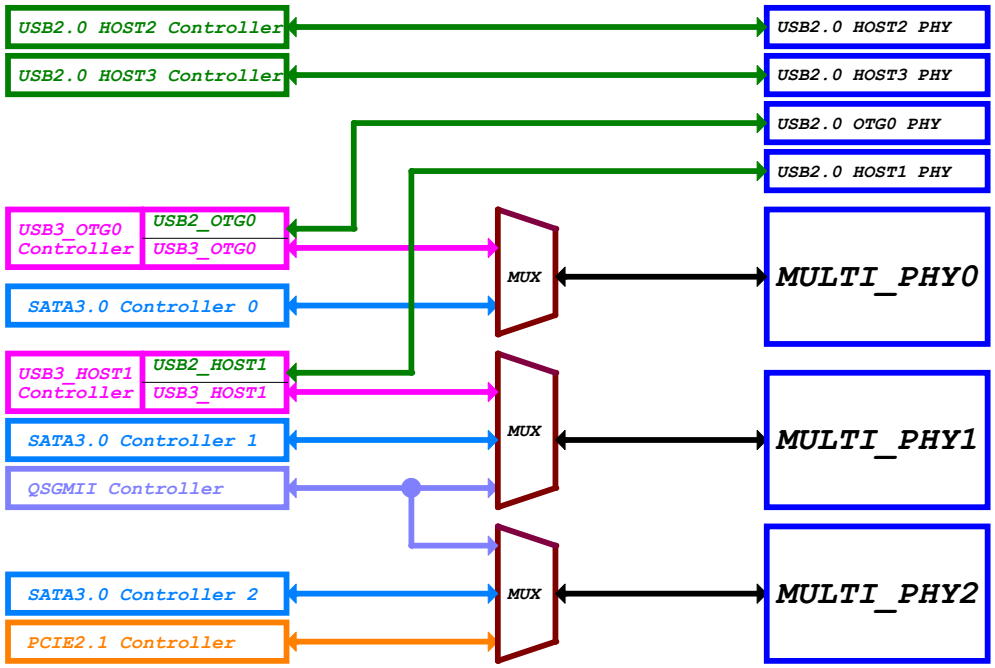
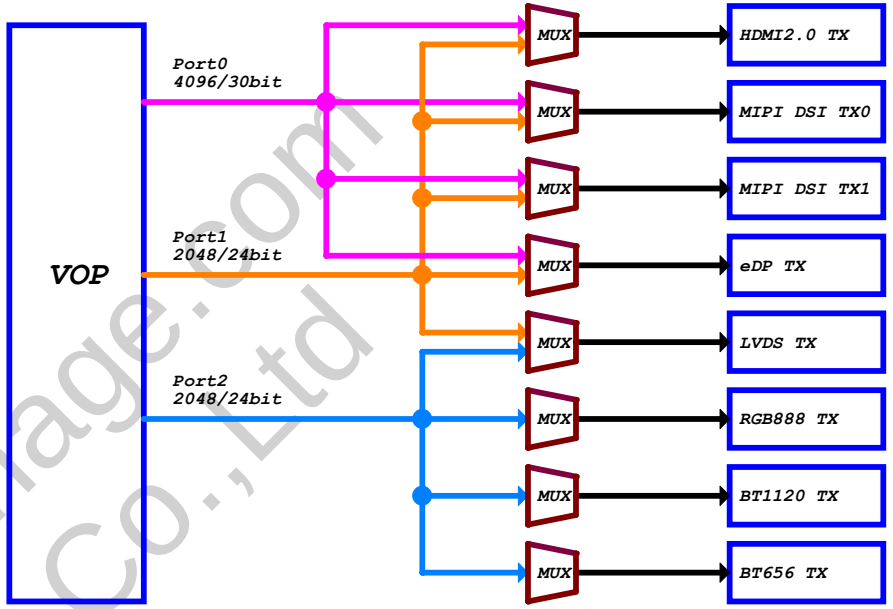
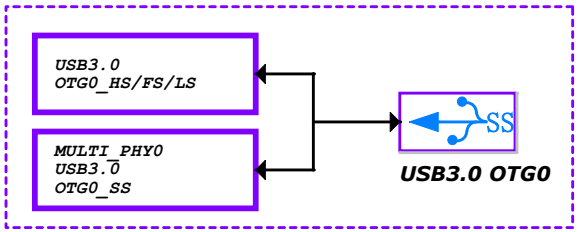
MULTI_PHY0/1/2 Path Map



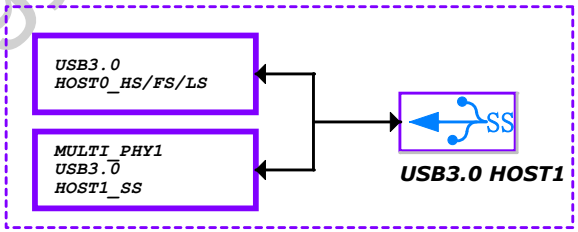
VOP Path Map



USB3.0 OTG0



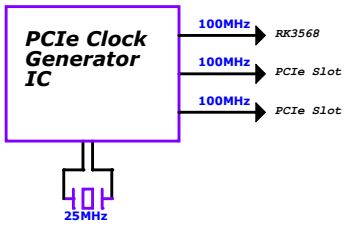
USB3.0 HOST1



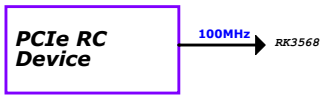
PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

PCIe3.0 REFCLK-RC Mode



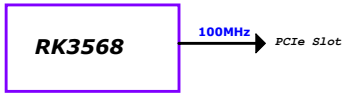
PCIe3.0 REFCLK-EP Mode



PCIe2.1 PHY

MULTI_PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

PCIe2.1 REFCLK-RC Mode



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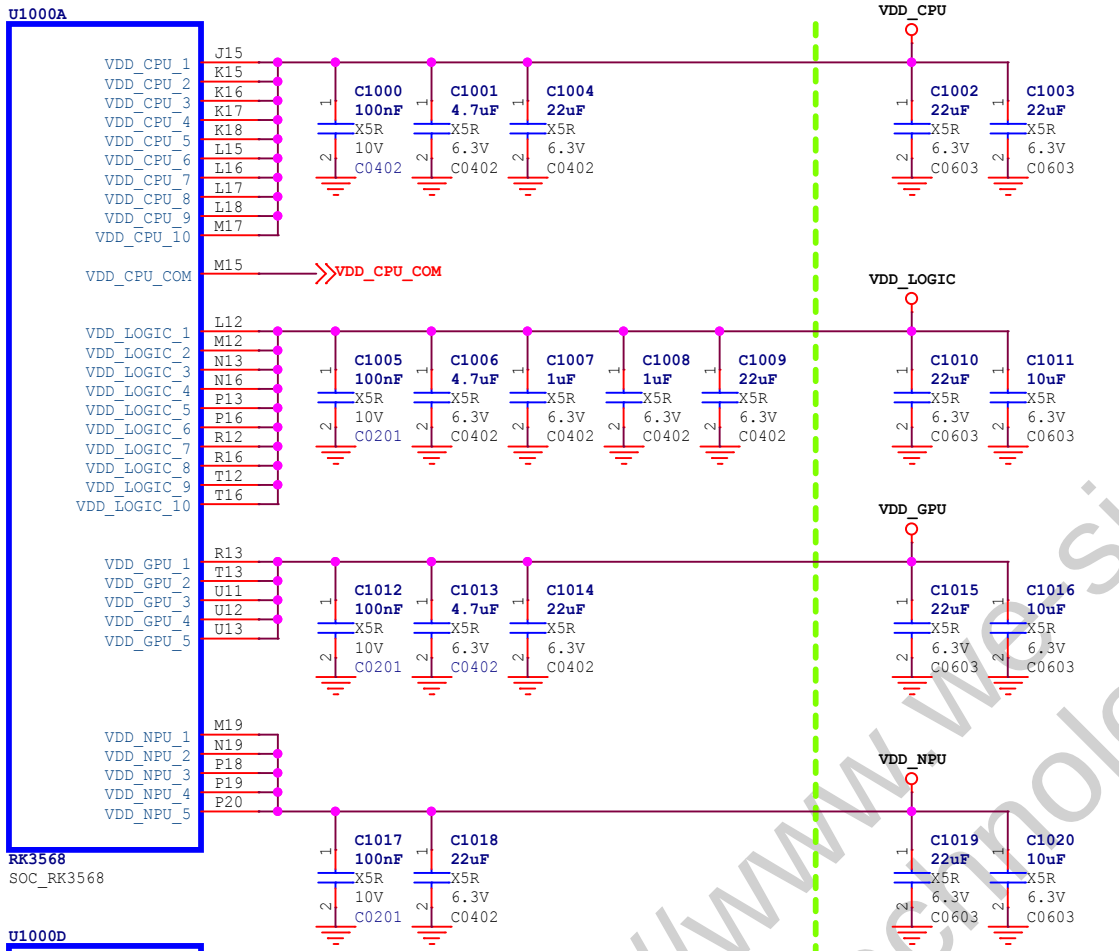
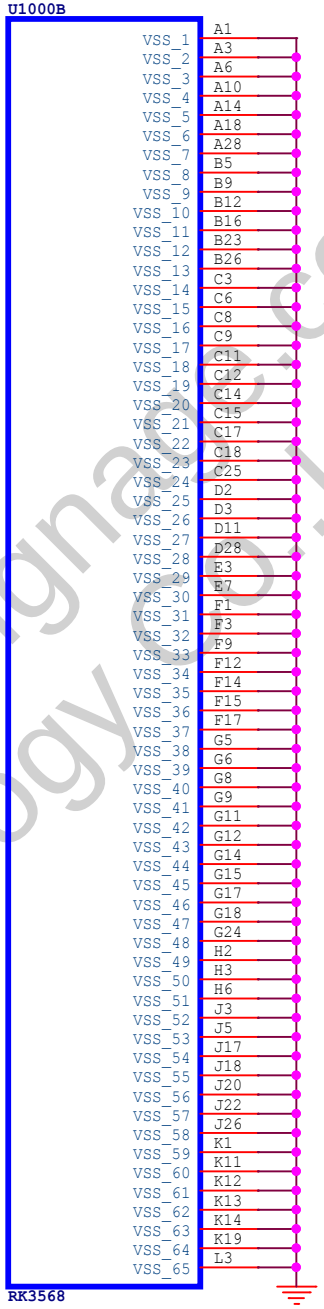
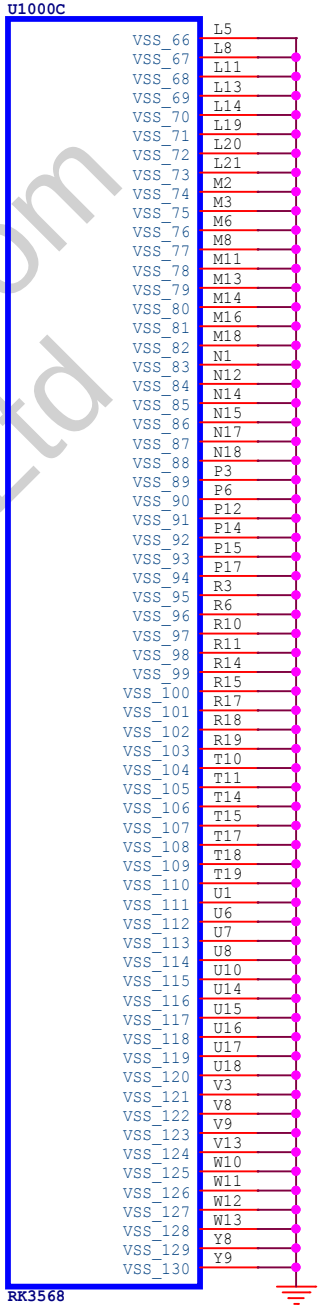
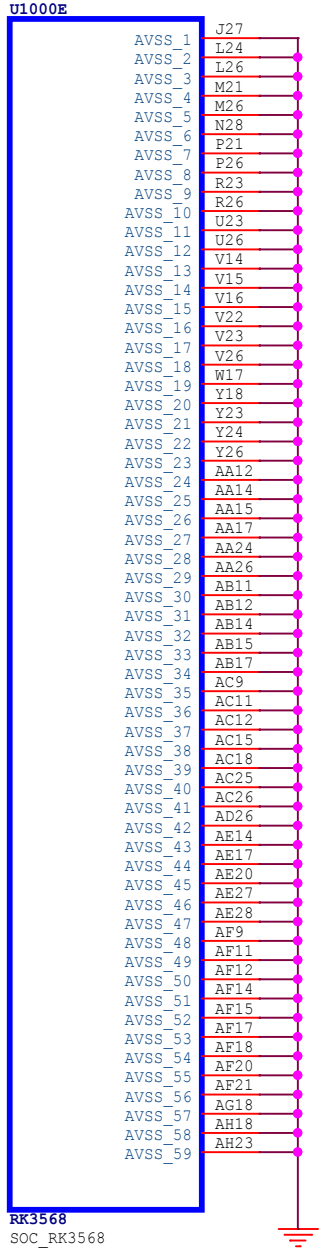
File:	09.PCIE30/MULTI_PHY/VOP Fun Map
Date:	Wednesday, June 08, 2022
Rev:	V1.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet	10 of 72

RK3568_ABCDE (Power&Gnd)









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Project:	RK3568_AIoT_PC_SCH				
File:	10.RK3568_Power/GND				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
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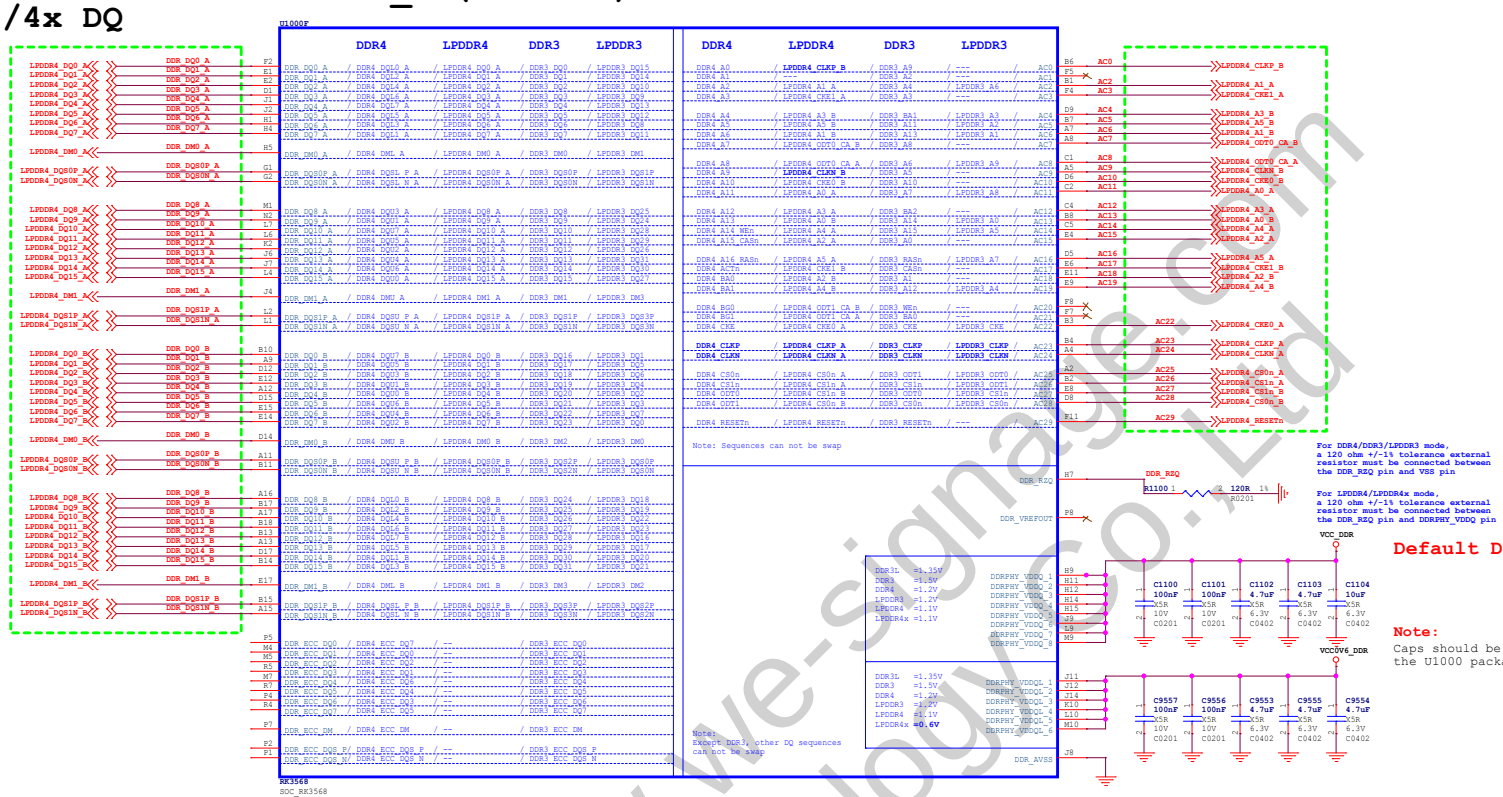
RK3568_F (DDR PHY)

LPDDR4/4x DQ



For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RSQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RSQ pin and DDRPHY_VDDQ pin

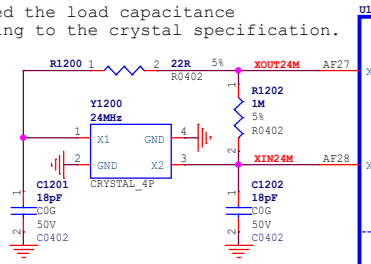
Default DDR4

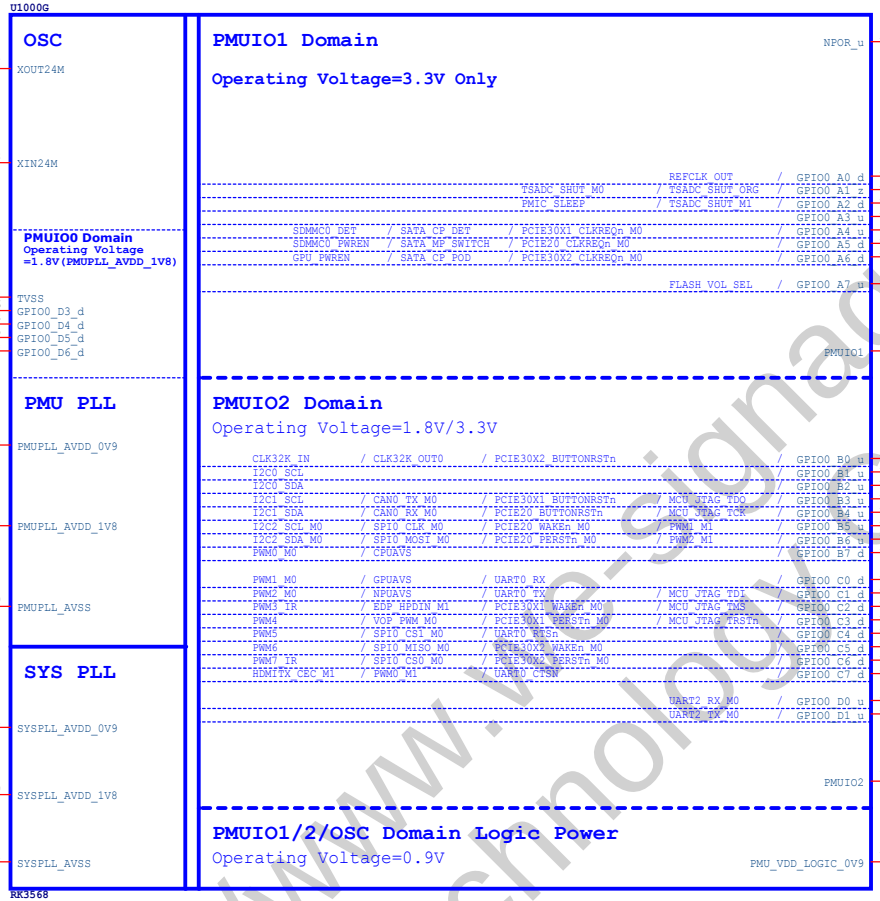
Note:
Caps should be placed under the U1000 package

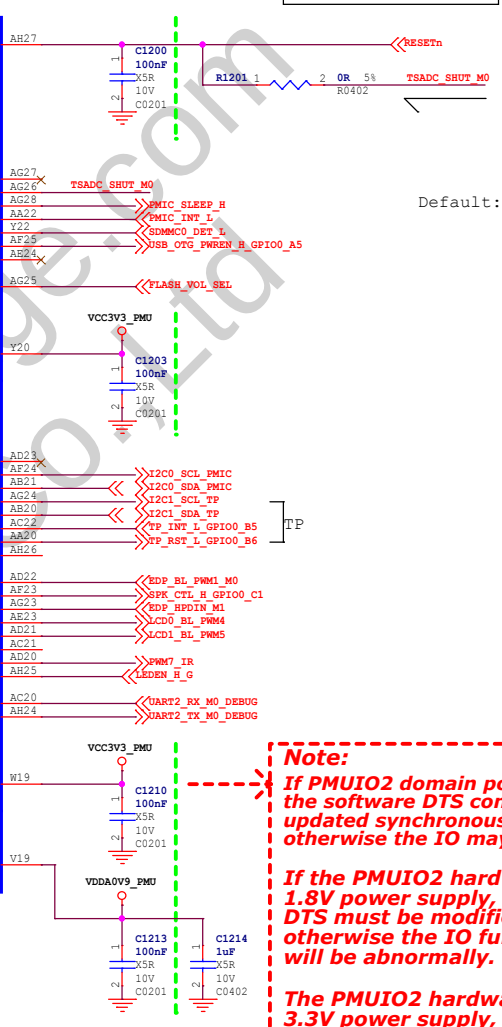
Rockchip Electronics Co., Ltd	
Project:	RK3568_AIoT_PC_SCH
File:	11.RK3568_DDR PHY
Date:	Wednesday, June 08, 2022
Rev:	V1.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet	12 of 72

RK3568_G(OSC/PLL/PMUIO1/2)

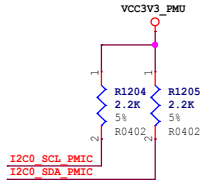
Note:
Adjusted the load capacitance according to the crystal specification.

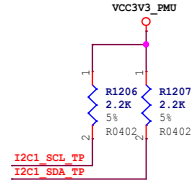


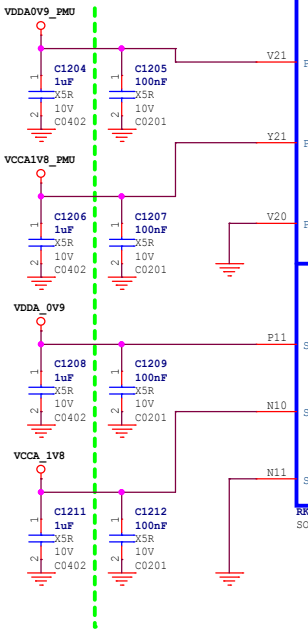


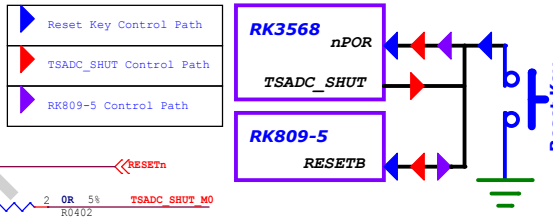


Default:24MHz









Note:
If PMUIO2 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the PMUIO2 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of PMUIO2 will be abnormally.

The PMUIO2 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of PMUIO2 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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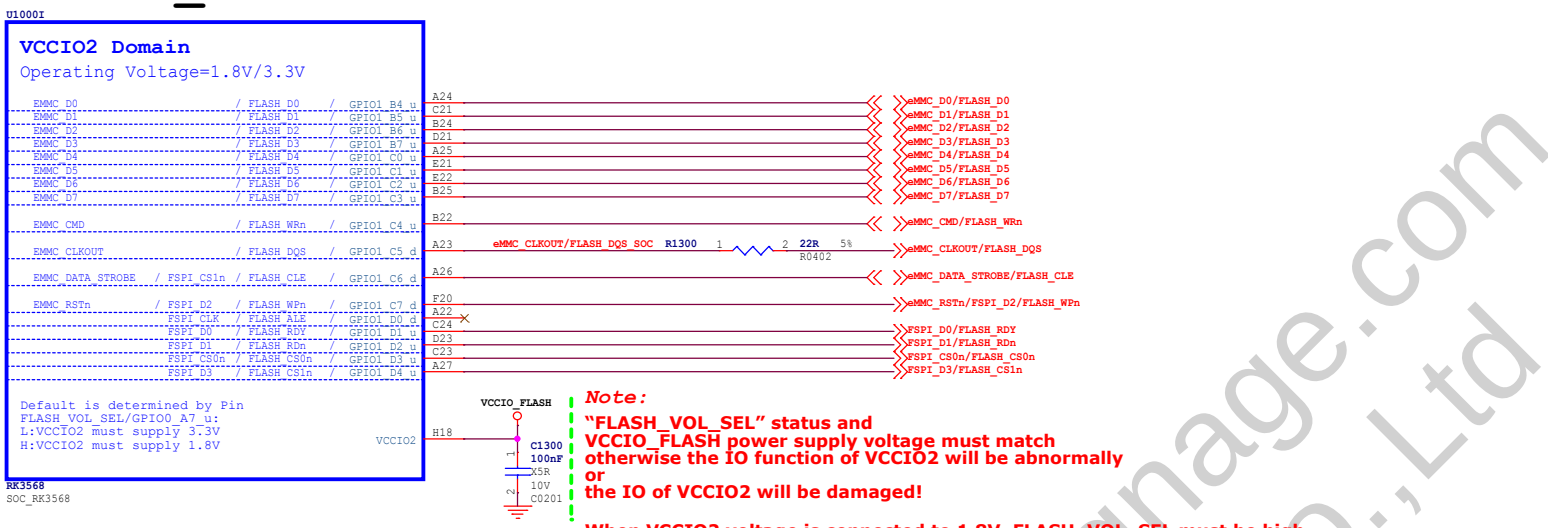
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RK3568_AIoT_PC_SCH			
File:	12.RK3568_OSC/PLL/PMUIO			
Date:	Wednesday, June 08, 2022		Rev:	V1.1
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	13 of 72

RK3568_I(VCCIO2 Domain)



Note:

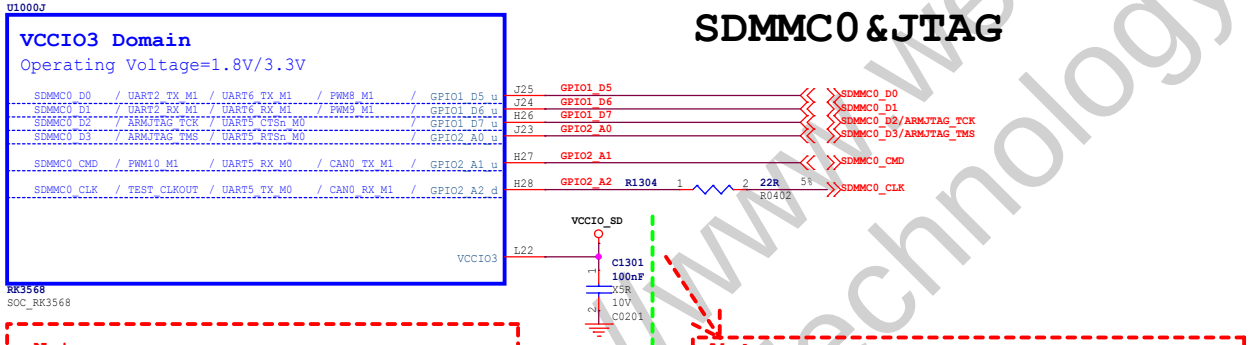
"FLASH_VOL_SEL" status and VCCIO_FLASH power supply voltage must match otherwise the IO function of VCCIO2 will be abnormally or the IO of VCCIO2 will be damaged!

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

RK3568_J(VCCIO3 Domain)

Default

SDMMC0&JTAG



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:

If VCCIO3 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

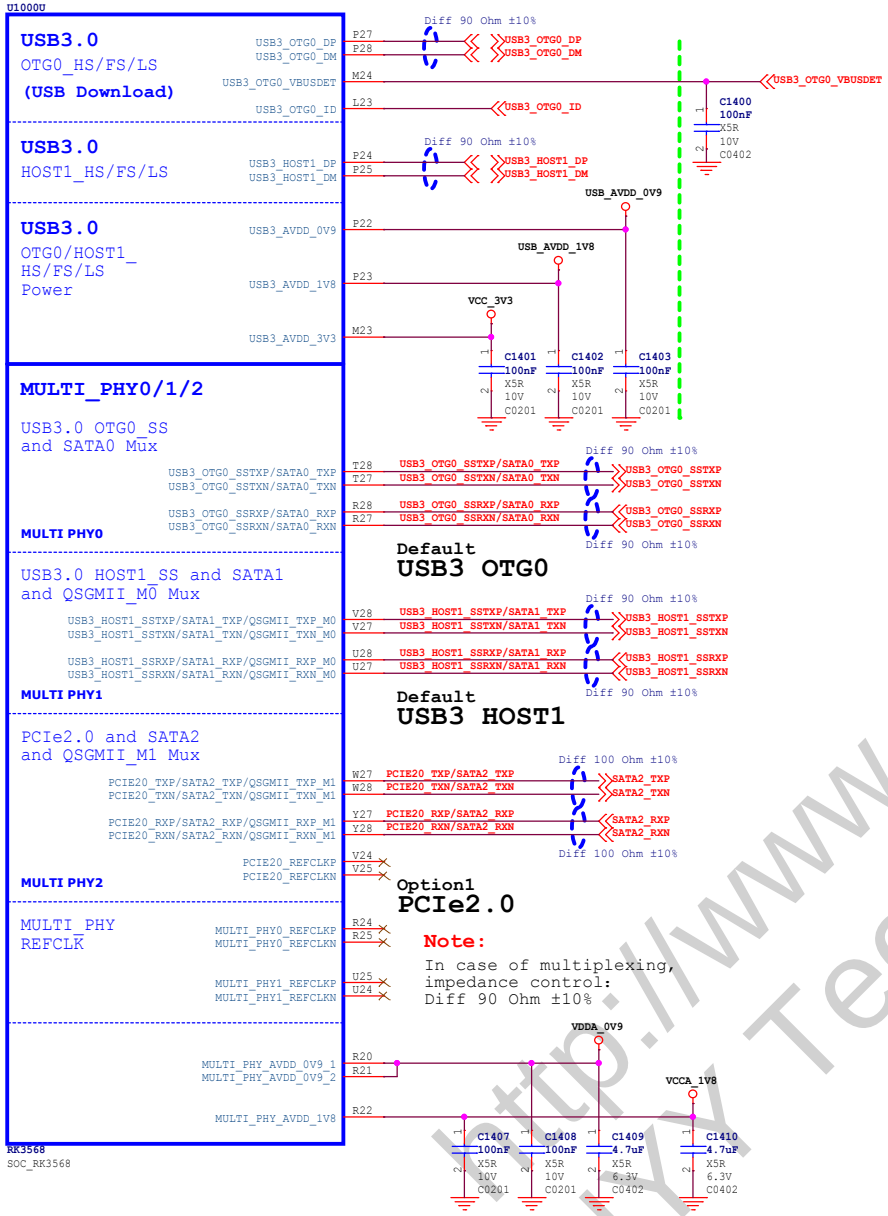
If the VCCIO3 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO3 will be abnormally.

The VCCIO3 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO3 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	13.RK3568_Flash/SD Controller				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 72

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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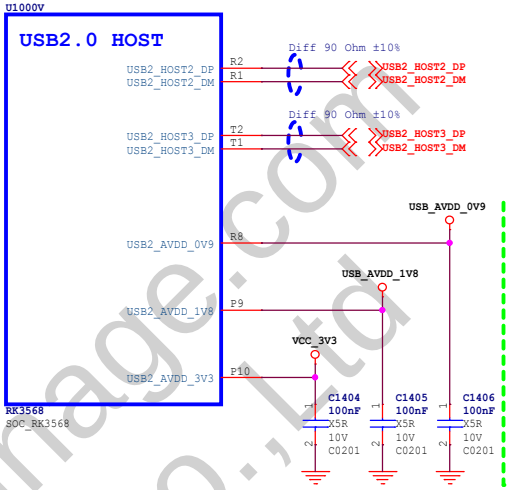
QSGMII can choose:
QSGMII_TXP_M0/QSGMII_TXN_M0
QSGMII_RXP_M0/QSGMII_RXN_M0
or
QSGMII_TXP_M1/QSGMII_TXN_M1
QSGMII_RXP_M1/QSGMII_RXN_M1

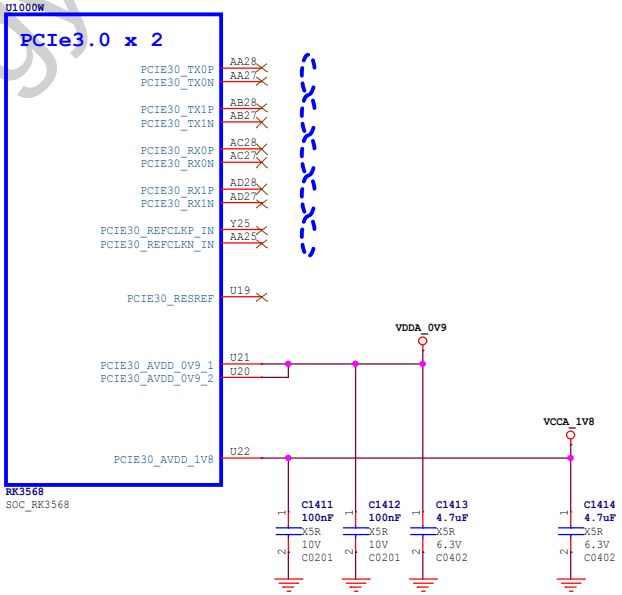
SGMII can choose:
SGMII_TXP_M0/SGMII_TXN_M0
SGMII_RXP_M0/SGMII_RXN_M0
or
SGMII_TXP_M1/SGMII_TXN_M1
SGMII_RXP_M1/SGMII_RXN_M1

See "07.UART Map/GMAC0/1 Path Map"
GMAC0/1 Path Map

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	14.RK3568_USB/PCIe/SATA PHY				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 72

RK3568_K(VCCIO4 Domain)

Note: *If VCCIO4 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!*
If the VCCIO4 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO4 will be abnormally.
The VCCIO4 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO4 will be damaged!

Default

U1000K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	/ GMAC0_RXD2	/ UART6_RX_M0			/ GPIO2_A3_u
SDMMC1_D1	/ GMAC0_RXD3	/ UART6_TX_M0			/ GPIO2_A4_u
SDMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0			/ GPIO2_A5_u
SDMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0			/ GPIO2_A6_u
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0			/ GPIO2_A7_u
SDMMC1_CLK	/ GMAC0_TXCLK	/ UART9_TX_M0			/ GPIO2_B0_d
SDMMC1_PWREN	/ I2C4_SDA_M1	/ UART8_RTSn_M0	/ CAN2_RX_M1		/ GPIO2_B1_d
SDMMC1_DET	/ I2C4_SCL_M1	/ UART8_CTSn_M0	/ CAN2_TX_M1		/ GPIO2_B2_u
	GMAC0_TXD0	/ UART1_RX_M0			/ GPIO2_B3_u
	GMAC0_TXD1	/ UART1_TX_M0			/ GPIO2_B4_u
	GMAC0_TXEN	/ UART1_RTSn_M0	/ SPI1_CLK_M0		/ GPIO2_B5_u
	GMAC0_RXD0	/ UART1_CTSn_M0	/ SPI1_MISO_M0		/ GPIO2_B6_u
I2S2_SCLK_RX_M0	/ GMAC0_RXD1	/ UART6_RTSn_M0	/ SPI1_MOSI_M0		/ GPIO2_B7_d
I2S2_LRCK_RX_M0	/ GMAC0_RXDV_CRS	/ UART6_CTSn_M0	/ SPI1_CS0_M0		/ GPIO2_C0_d
I2S2_MCLK_M0	/ ETH0_REFCLKO_25M	/ UART7_RTSn_M0	/ SPI1_CLK_M0		/ GPIO2_C1_d
I2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0	/ SPI2_MISO_M0		/ GPIO2_C2_d
I2S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0	/ SPI2_MOSI_M0		/ GPIO2_C3_d
I2S2_SDO_M0	/ GMAC0_MDIO	/ UART9_CTSn_M0	/ SPI2_CS0_M0		/ GPIO2_C4_d
I2S2_SDI_M0	/ GMAC0_RXER	/ UART8_TX_M0	/ SPI2_CS1_M0		/ GPIO2_C5_d
CLK32K_OUT1		/ UART8_RX_M0	/ SPI1_CS1_M0		/ GPIO2_C6_d

RK3568
SOC_RK3568

RGMII0

E27 GPIO2_A3 → GMAC0_RXD2
E28 GPIO2_A4 → GMAC0_RXD3
B28 GPIO2_A5 → GMAC0_RXCLK
C27 GPIO2_A6 → GMAC0_TXD2
C28 GPIO2_A7 → GMAC0_TXD3
D27 GPIO2_B0 → GMAC0_TXCLK
D26 GPIO2_B1 → UART8_CTSN_M0
E25 GPIO2_B2 → UART8_RTSn_M0 For BT
F28 GPIO2_B3 → GMAC0_TXD0
G27 GPIO2_B4 → GMAC0_TXD1
G28 GPIO2_B5 → GMAC0_TXEN
F27 GPIO2_B6 → GMAC0_RXD0
H25 GPIO2_B7 → GMAC0_RXD1
F24 GPIO2_C0 → GMAC0_RXDV_CRS
G23 ETH0_REFCLKO_25M_SOC — R9549 1 2 22R 5% R0402 → ETH0_REFCLKO_25M
F25 GPIO2_C2 → GMAC0_MCLKINOUT
H24 GPIO2_C3 → GMAC0_MDC
H23 GPIO2_C4 → GMAC0_MDIO
F26 GPIO2_C5 → UART8_TX_M0 For BT
E26 GPIO2_C6 → UART8_RX_M0

V1.1

VCCIO4 — R1509 1 2 0R 5% R0402 → VCC_1V8
R1511 1 DNP 2 0R 5% R0402 → VCC_3V3

Note:
According to the actual choice of mounted Cannot be mounted at the same time

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

VCCIO4 — J21 — C1500 100nF X5R 10V C0201

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

U1000N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	/ SPI3_CLK_M1	/ CAN1_RX_M1	/ PCIE30X2_CLKREQn_M2	/ I2S3_MCLK_M1	/ GPIO4_C2_d
PWM15_IR_M1	/ SPI3_MOSI_M1	/ CAN1_TX_M1	/ PCIE30X2_WAKEn_M2	/ I2S3_SCLK_M1	/ GPIO4_C3_d
EDP_HPDIN_M0	/ SPDIF_TX_M2	/ SATA2_ACT_LED	/ PCIE30X2_PERSTn_M2	/ I2S3_LRCK_M1	/ GPIO4_C4_d
PWM12_M1	/ SPI3_MISO_M1	/ SATA1_ACT_LED	/ UART9_TX_M1	/ I2S3_SDO_M1	/ GPIO4_C5_d
PWM13_M1	/ SPI3_CS0_M1	/ SATA0_ACT_LED	/ UART9_RX_M1	/ I2S3_SDI_M1	/ GPIO4_C6_d
HDMITX_SCL	/ I2C5_SCL_M1				/ GPIO4_C7_u
HDMITX_SDA	/ I2C5_SDA_M1				/ GPIO4_D0_u
HDMITX_CEC_M0	/ SPI3_CS1_M1				/ GPIO4_D1_u
					GPIO4_D2_d

AF8 I2S3_MCLK_M1
AA11 I2S3_SCLK_M1
AH7 I2S3_LRCK_M1
AD8 I2S3_SDO_M1
AE8 I2S3_SDI_M1
AG8 HDMITX_SCL
AG7 HDMITX_SDA
AH6 HDMITX_CEC_M0
AB9 GPIO4_D2_d

VCC_3V3 — V12 — VCCIO7 — C1509 100nF X5R 10V C0201

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

RK3568
SOC_RK3568

Note:
If VCCIO7 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO7 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO7 will be abnormally.

The VCCIO7 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO7 will be damaged!

RK3568_O(SARADC/OTP)

U1000O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C1501 1nF X5R 50V C0402
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C1502 1nF X5R 50V C0402
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK	C1503 1nF X5R 50V C0402
SARADC_VIN3	E23	SARADC_VIN3_LCD_ID	C1504 1nF X5R 50V C0402
SARADC_VIN4	G21	SARADC_VIN4	C1505 1nF X5R 50V C0402
SARADC_VIN5	F22	SARADC_VIN5	C1506 1nF X5R 50V C0402
SARADC_VIN6	G20	SARADC_VIN6	C1507 1nF X5R 50V C0402
SARADC_VIN7	F21	SARADC_VIN7	C1508 1nF X5R 50V C0402
SARADC_AVDD_1V8	H22		C1510 100nF X5R 10V C0201
OTP_VCC18	H20		C1511 100nF X5R 10V C0201

VCCA_1V8
VCC_1V8

OTP

RK3568
SOC_RK3568

Note:
Must be mounted

VCCA_1V8 — R1512 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY

Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

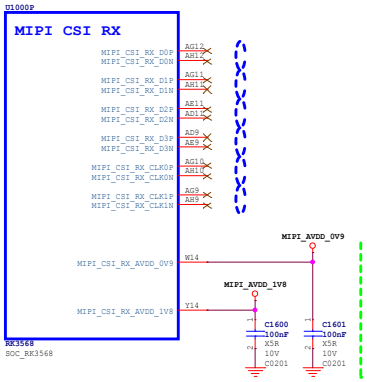
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_HP_HOOK
SARADC_VIN3_LCD_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

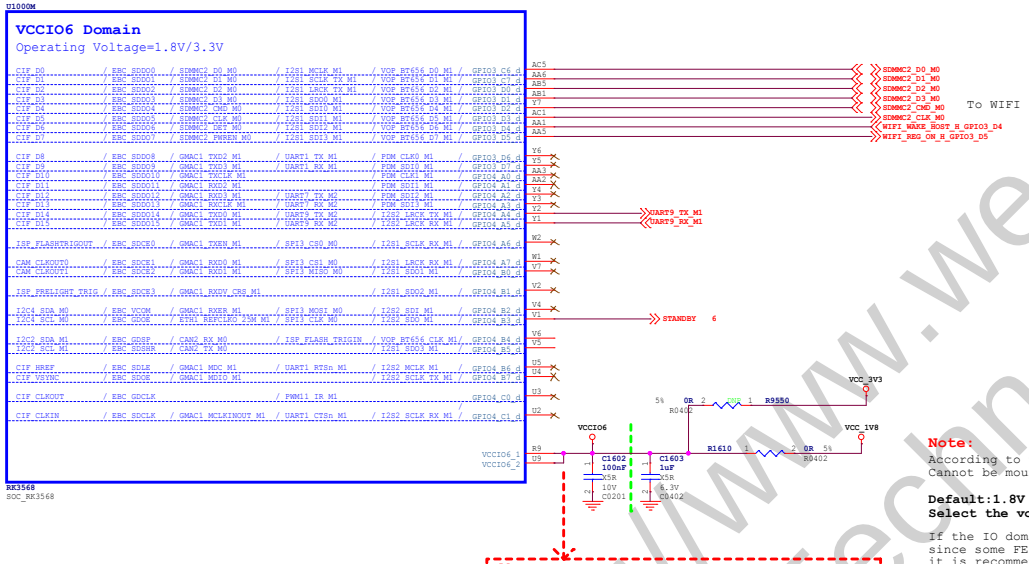
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	15.RK3568_SARADC/GPIO				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 72

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If VCCIO6 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO6 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO6 will be abnormally.

The VCCIO6 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO6 will be damaged!

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Default:1.8V
Select the voltage according to the application

If the IO domain is to be used as FEPHY,
since some FEPHY only support 3.3V IO,
it is recommended to reallocate GPIO
to reduce the cost of level conversion

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

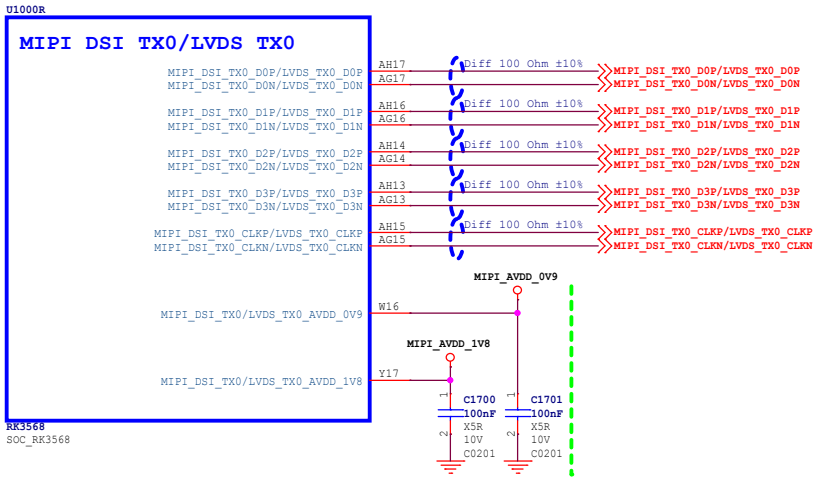
Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

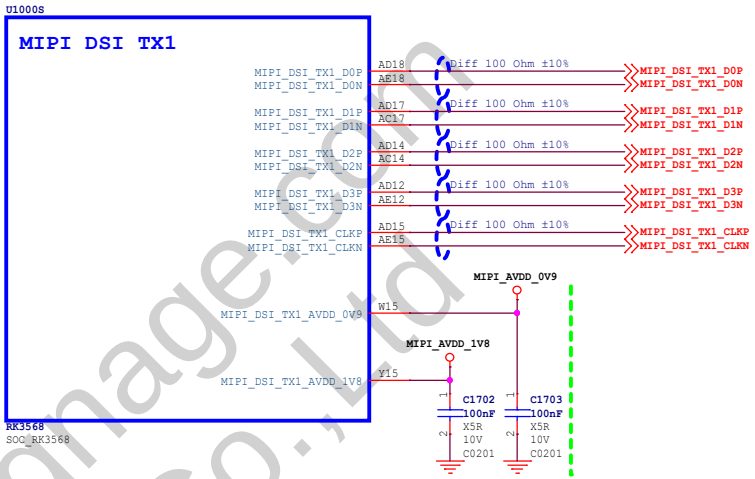
GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_CRS_DV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx OSC	ETHx_REFCLKO_25M	------->	PHYx OSC
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	<------->	PHYx_TXC
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_PC_SCH
File:	16.RK3568_V1 Interface
Date:	Wednesday, June 08, 2022
Rev:	V1.1
Designed by: Zhangdz	Reviewed by: Default
Sheet	17 of 72

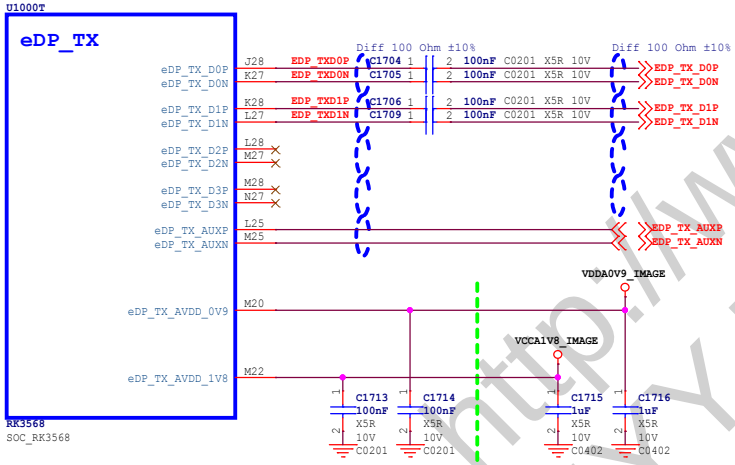
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



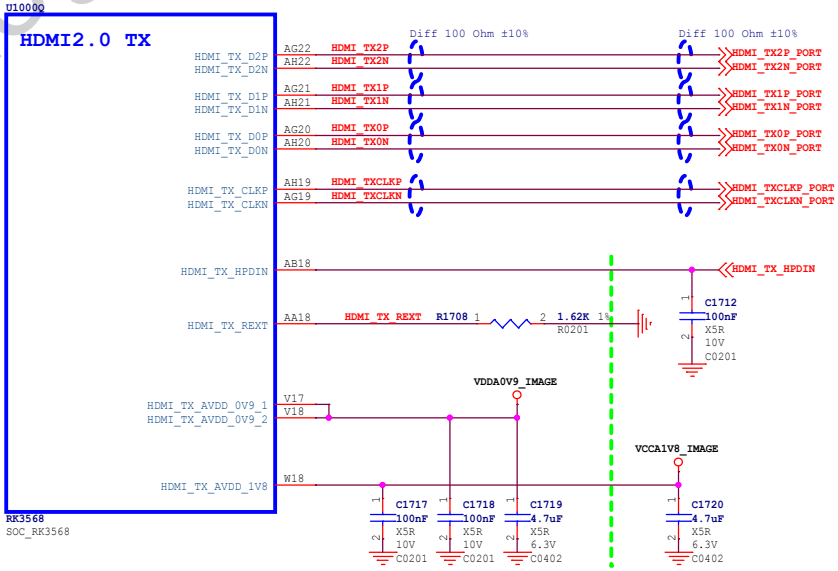
RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



RK3568_Q(HDMI2.0 TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	17.RK3568_VO Interface_1				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	18 of 72

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568

SOC_RK3568

AG6 AD7 AC8 AC7 AF5 AF6 AD6 AH5

GMAC0_INT/PMEB_GPIO2_D2

GMAC0_RSTn_GPIO2_D3

AH4

BT_REG_ON_H_GPIO3_A0

AB8 AE5 AG4 AF4 AH3 AG3 AH2

BT_WAKE_HOST_H_GPIO3_A1

HOST_WAKE_BT_H_GPIO3_A2

I2S3_SCLK_M0_PCM_CLK

I2S3_LRCK_M0_PCM_SYNC

I2S3_SDO_M0_PCM_TX

I2S3_SDI_M0_PCM_RX

for BT

AG2

BL_EN_GPIO3_B0

AG1 AF2 AF1 AE1 AE2 AE3

UART4_RX_M1

UART4_TX_M1

I2C5_SCL_M0

I2C5_SDA_M0

RS485_DIR_GPIO3_B5

AD4 AD2

UART3_TX_M1

UART3_RX_M1

AD1 AA7 AC4

HP_DET_L_GPIO3_C2

EDP_BL_EN

AC3 AC2

VGA_HPDIN_GPIO0_C0

SPDIF_TX_M1

V10 V11

VCCIO5_1

VCCIO5_2

VCC_3V3

C1800 100nF X5R 10V C0201

VCC_3V3

R1801 10K 5% R0402

od

GMAC0_INT/PMEB_GPIO2_D2

VCC_3V3

R1804 2.2K 5% R0402

R1805 2.2K 5% R0402

I2C5_SCL_M0

I2C5_SDA_M0

Note:

If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormally.

The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO5 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Default

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RK3568_AIoT_PC_SCH			
File:	18.RK3568_VO Interface_2			
Date:	Wednesday, June 08, 2022		Rev:	V1.1
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	19 of 72

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

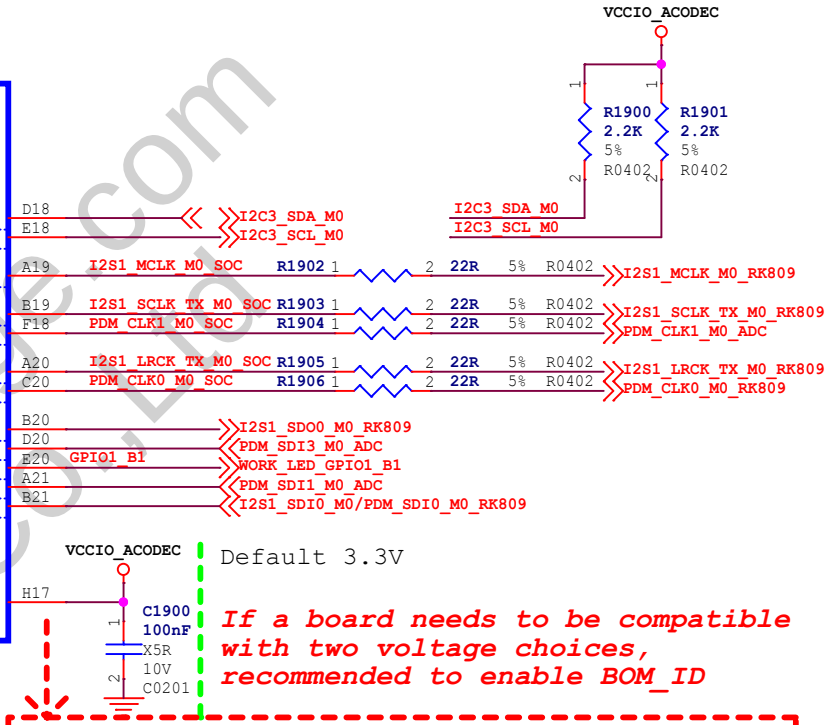
Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

VCCIO1

RK3568

SOC_RK3568



Note:

If VCCIO1 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO1 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO1 will be abnormally.

The VCCIO1 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO1 will be damaged!

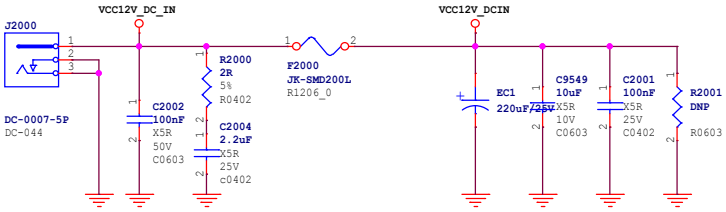
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

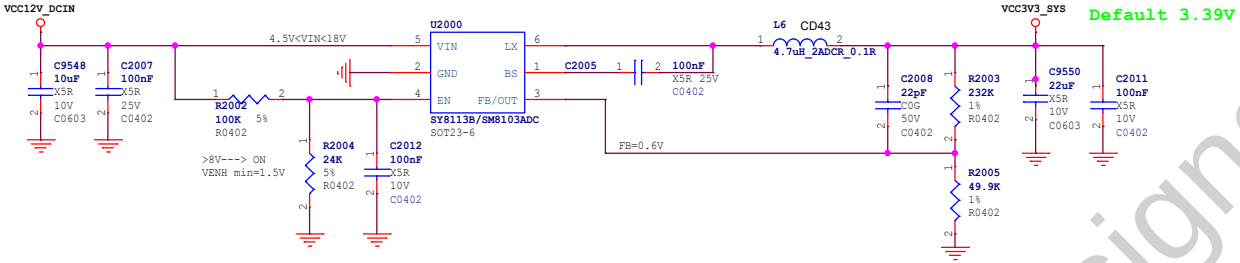
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	19.RK3568_Audio Interface				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 72

12V/3A DCIN

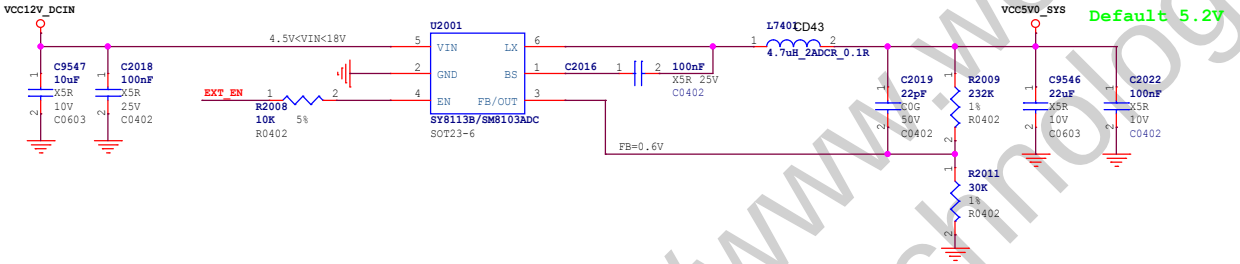
Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

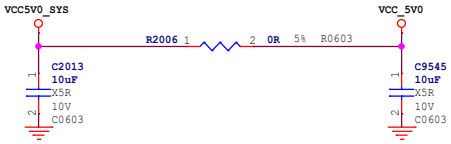


VCC3V3_SYS

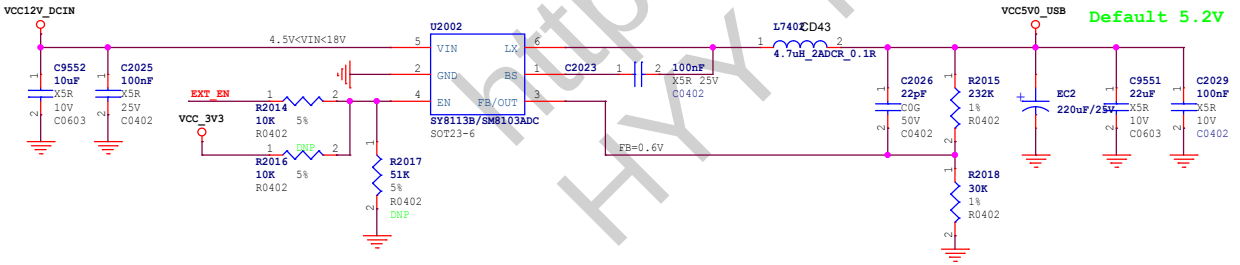


VCC5V0_SYS

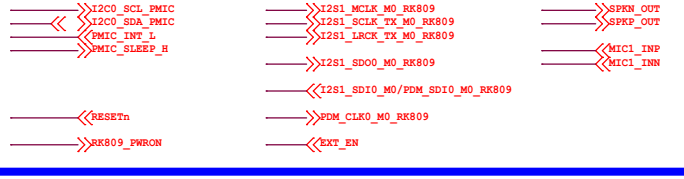


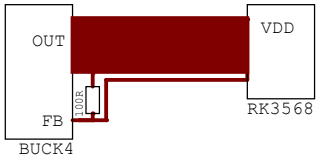


VCC5V0_USB

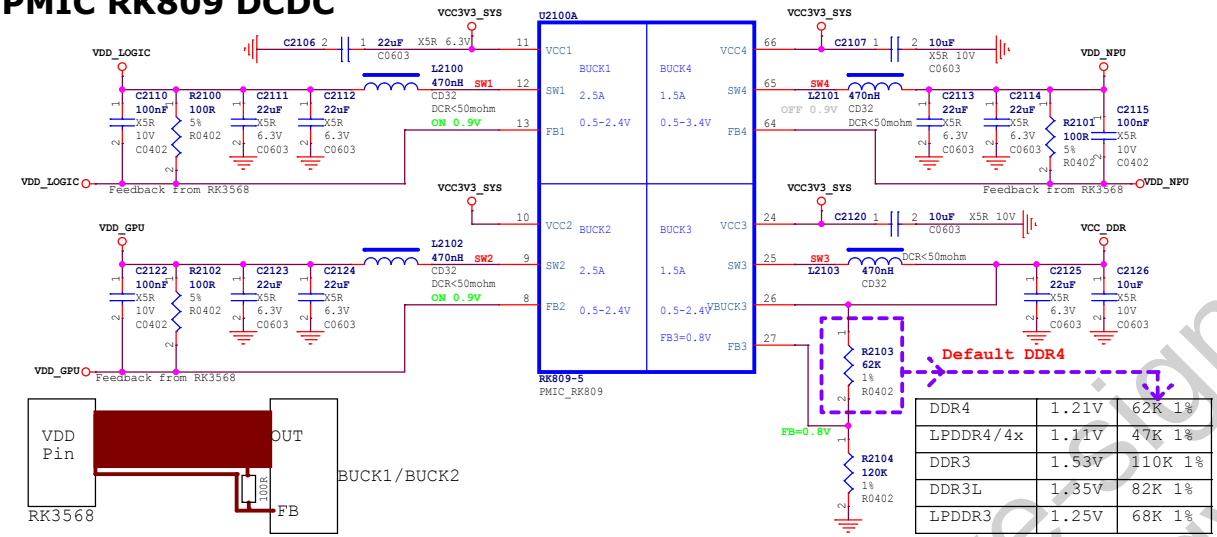


Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_PC_SCH				
File:	20.Power_DC IN				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	21 of 72



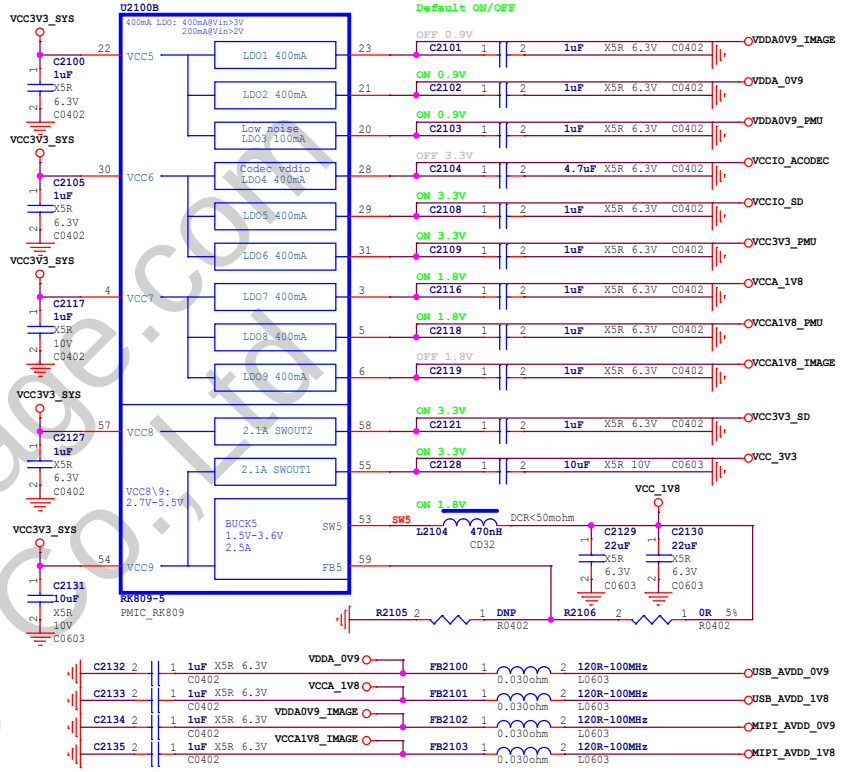


PMIC RK809 DCDC

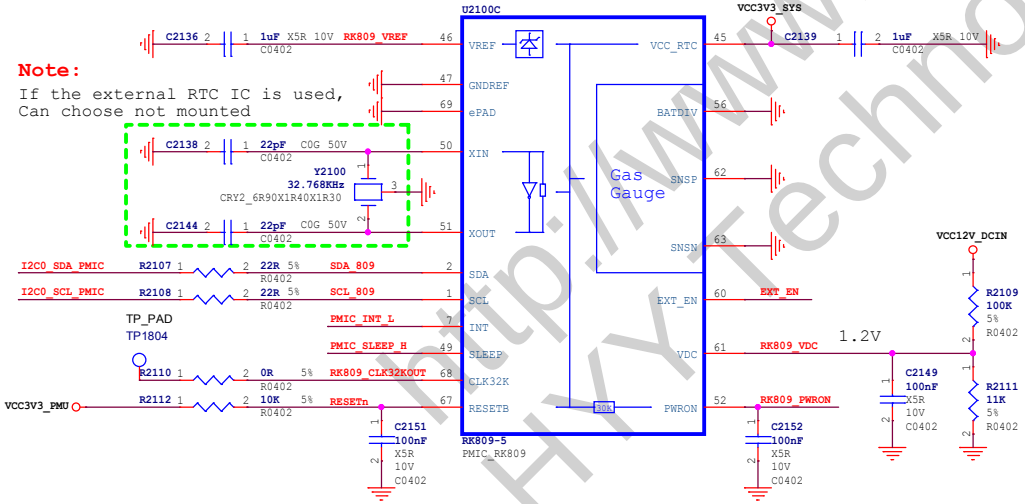


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

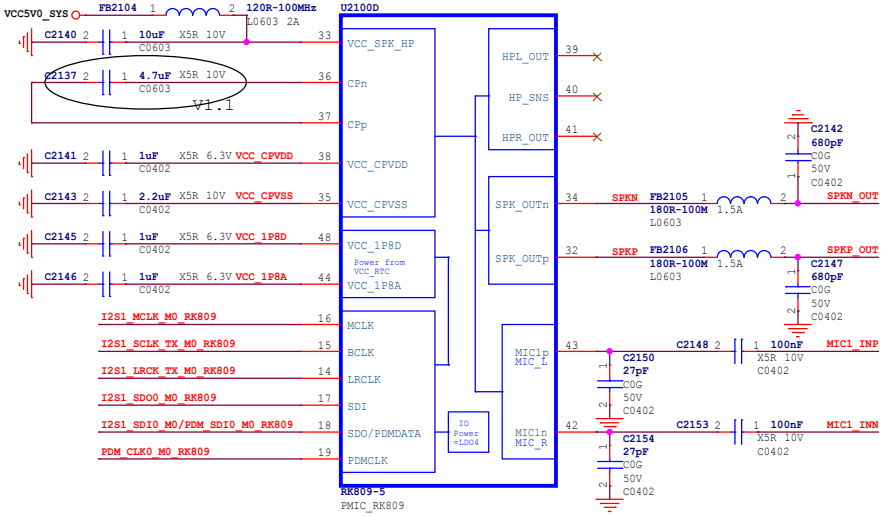
PMIC RK809 LDO



PMIC RK809 Managerment



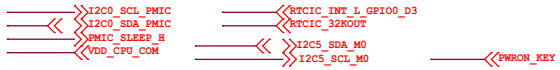
PMIC RK809 CODEC



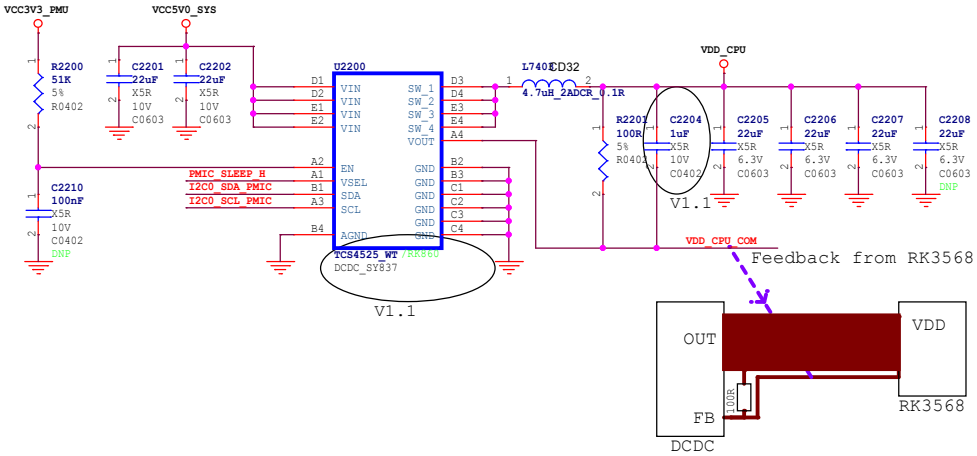
Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	21.Power_PMIC				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 72



VDD_CPU

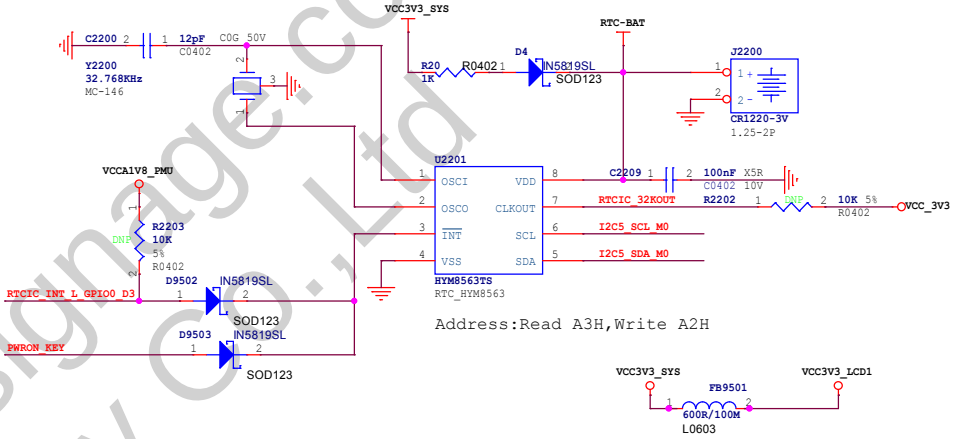


RTC IC --Option

Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC

But, it will not support the timing poweron function



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	22.Power_Ext Discrete/RTC IC				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 72

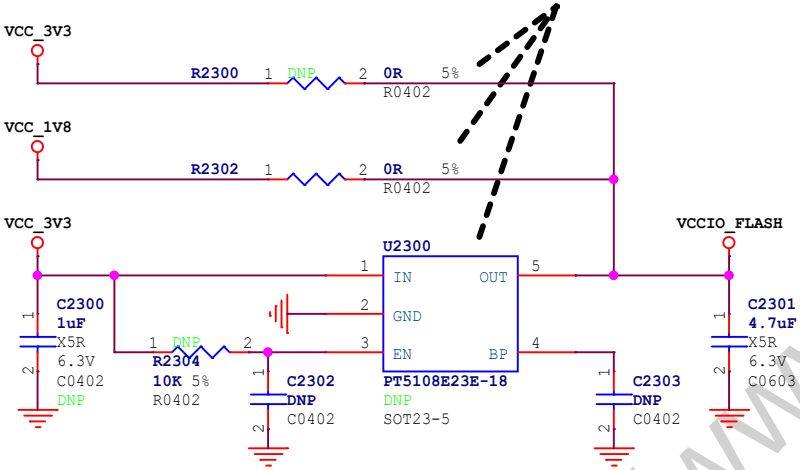
FLASH_VOL_SEL

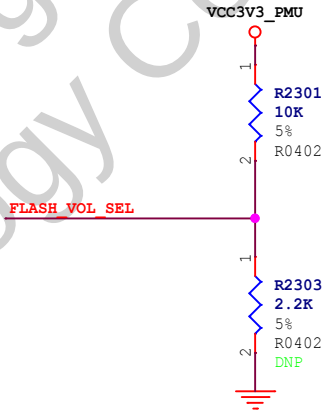
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time

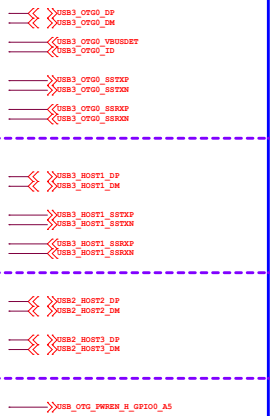


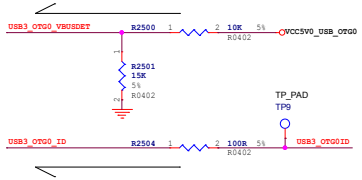


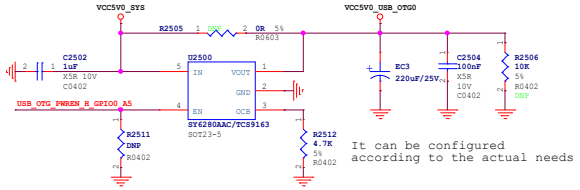
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

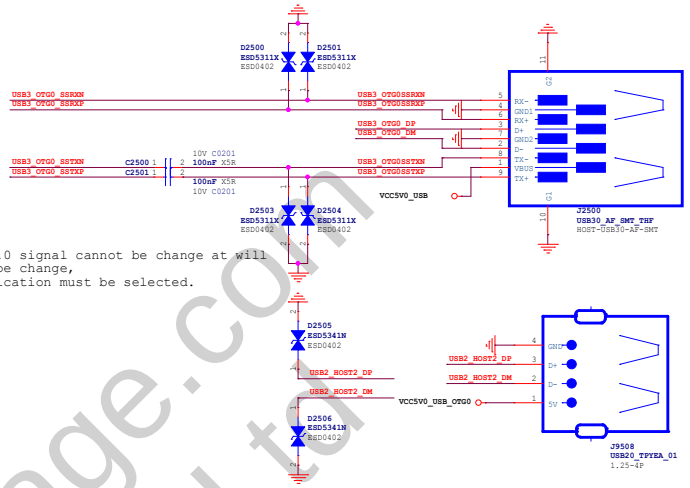
When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship,
its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	23.Power_Flash Power Manage				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	24 of 72









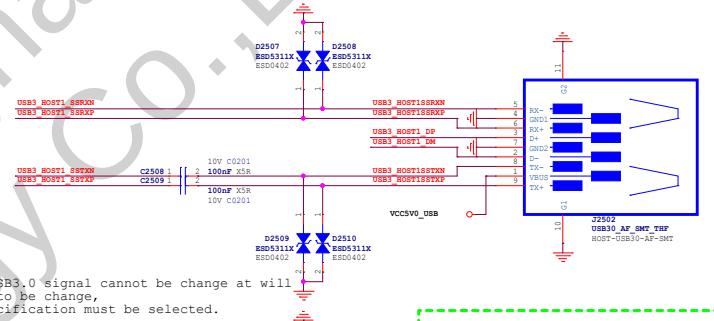
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.

Cj<=0.4pF

Default

USB3.0 OTG0

And SATA0 Option



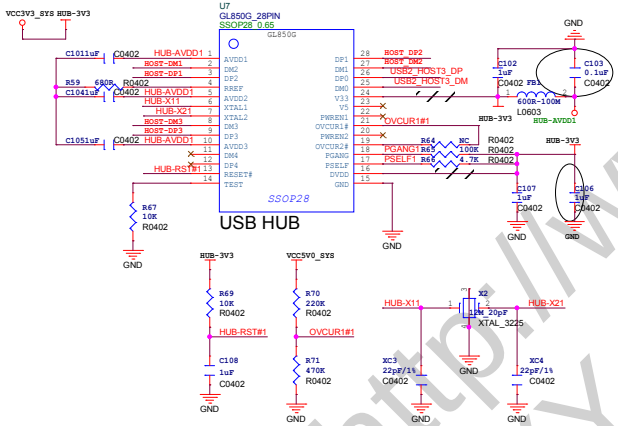
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.

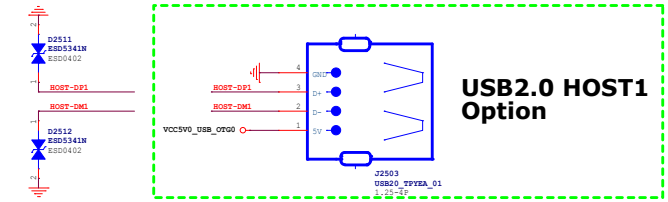
Cj<=0.4pF

Default

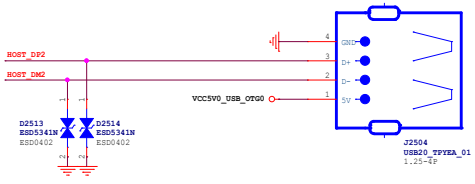
USB3.0 HOST1

And SATA1 Option

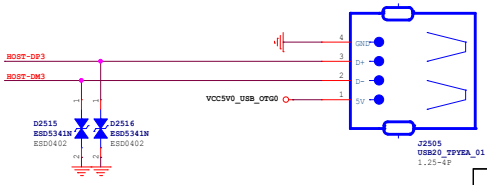




USB2.0 HOST1 Option



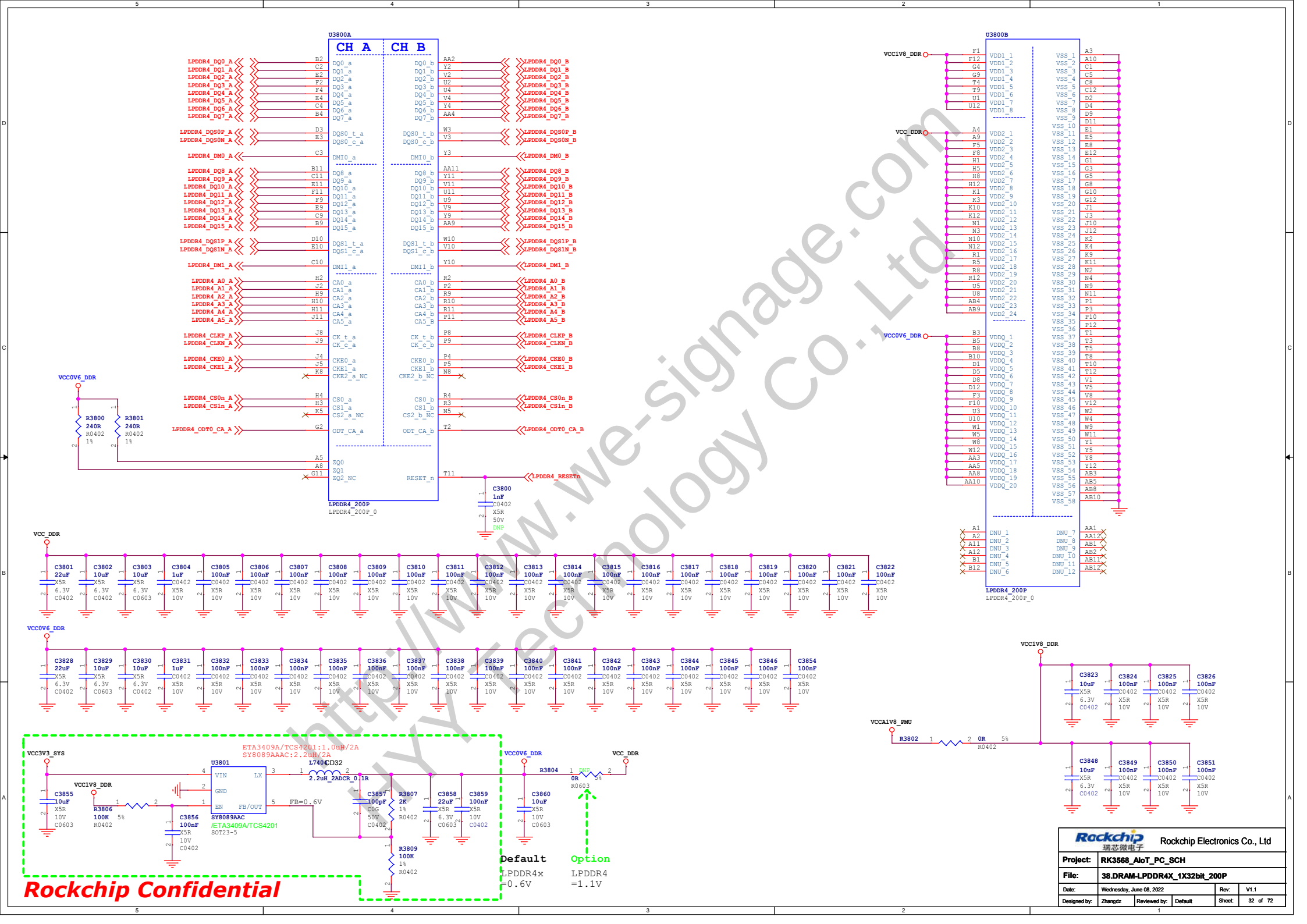
USB2.0 HOST2



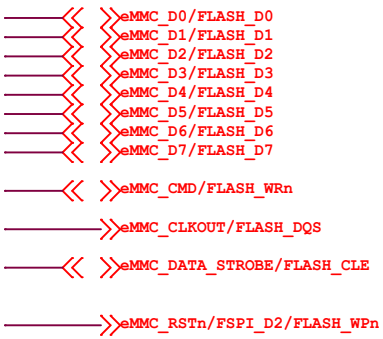
USB2.0 HOST3

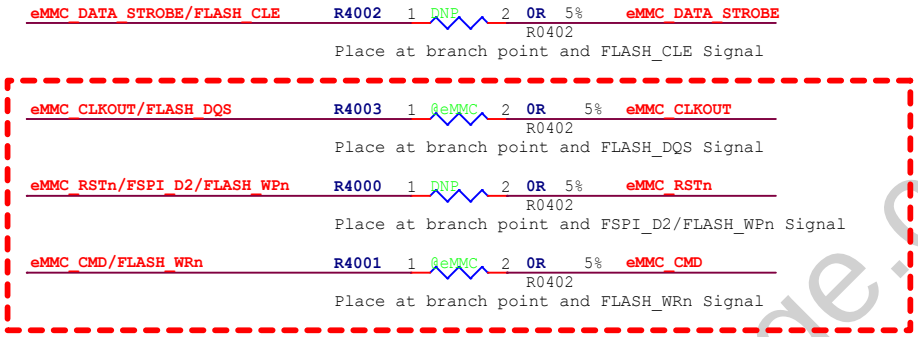
And 4G module Option

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_PC_SCH
File:	25.USB2/USB3 Port
Date:	Wednesday, June 08, 2022
Rev:	V1.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet	25 of 72



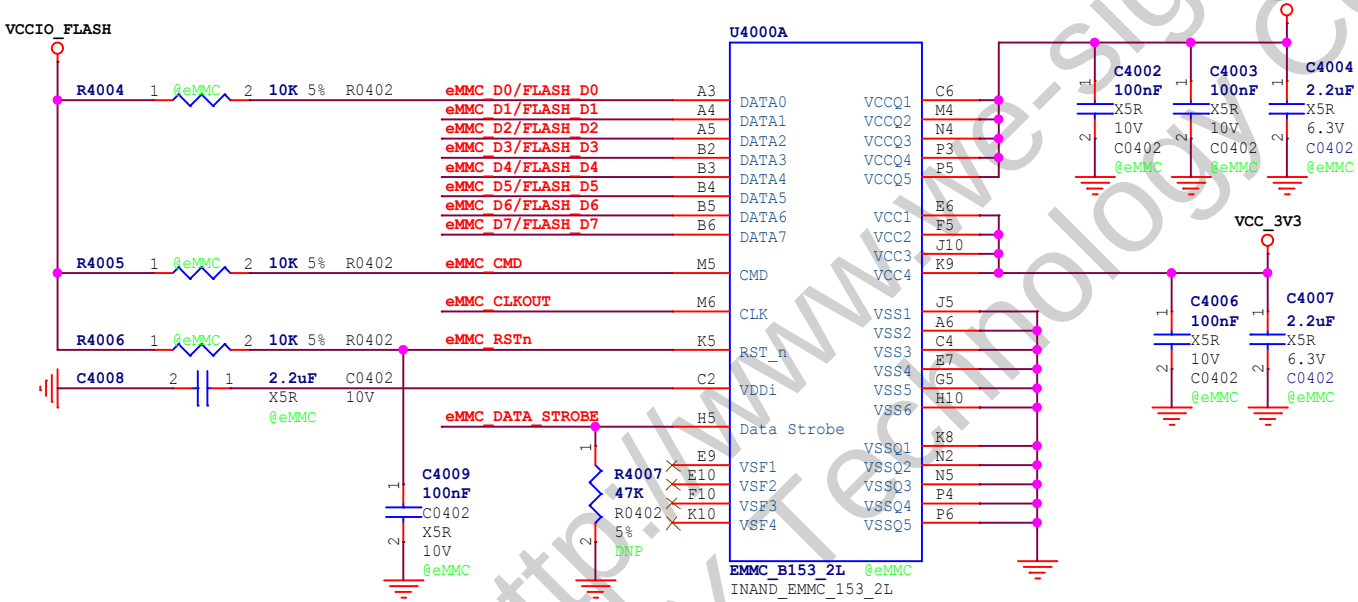
eMMC Flash

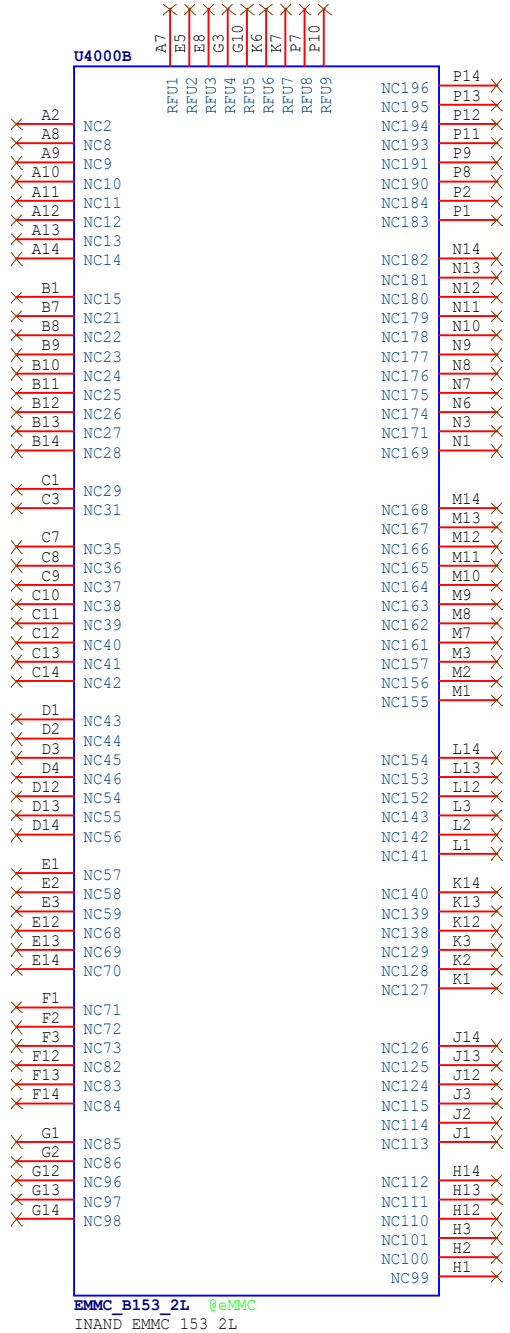




Note:

No need to double layout with Nand Flash, 0R resistor can be omitted





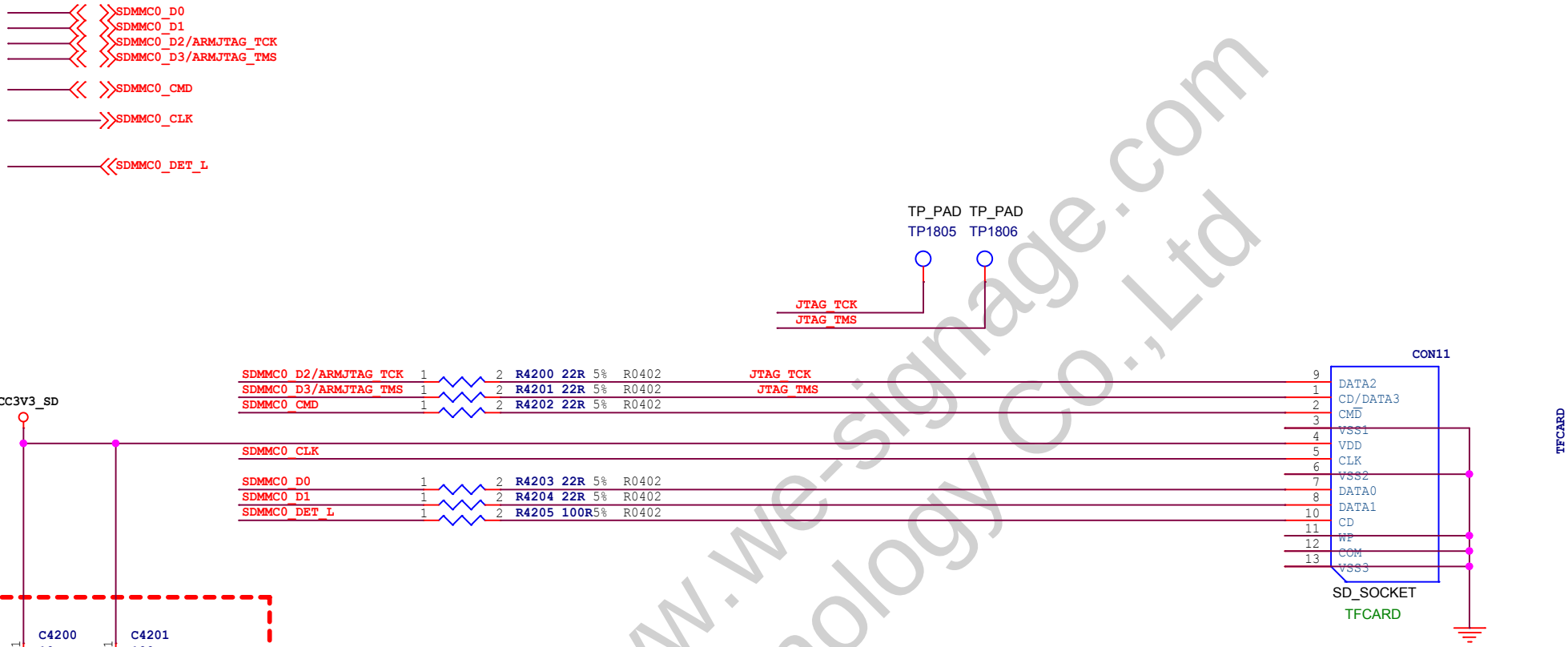
Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Rockchip Confidential

Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_PC_SCH				
File:	40.Flash-eMMC Flash				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	33 of 72

MicroSD Card



MicroSD Card

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	42.Flash-MicroSD Card				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 72

HDMI2.0 TX

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT

HDMITX_SCL
HDMITX_SDA

HDMITX_CEC_M0
HDMI_TX_HPDIN

HDMI TX DDC

VCC_5V0
D5000 B5819WS SOD123
VCC_3V3
R5000 10K 5% R0402
Q5000 2SK3018 SOT23
R5001 1.8K 5% R0402
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R5002 10K 5% R0402
Q5001 2SK3018 SOT23
R5003 1.8K 5% R0402
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

HDMI TX CEC

VCC_3V3
VCC_5V0
R5006 27K 5% R0402
Q5002 2SK3018 SOT23
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

HDMI TX HPD

HDMI_TX_HPDIN
R5005 1K 5% R0402
HDMI_TX_HPD_PORT
R5007 100K 5% R0402

F2001
HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
VCC5V_HDMI_TX
HDMI_TX_HPD_PORT
FPC-19

Cj<=0.4pF

U5000 ESD5344D RCLAMP0524P
U5001 ESD5344D RCLAMP0524P
IO1 IO2 GND IO3 IO4 NC_10 NC_9 NC_7 NC_6

ED5000 ESD5341N ESD0402
ED5001 ESD5341N ESD0402
ED5002 ESD5341N ESD0402
ED5003 ESD5341N ESD0402

C5000 1uF X5R 10V C0402

J5000 HDMI_TYPE_A HDMI
Type A
D2P D2_G D2N D1P D1_G D1N D0P D0_G D0N CLKP CLK_G CLKN CEC Utility SCL SDA GND +5V HPD

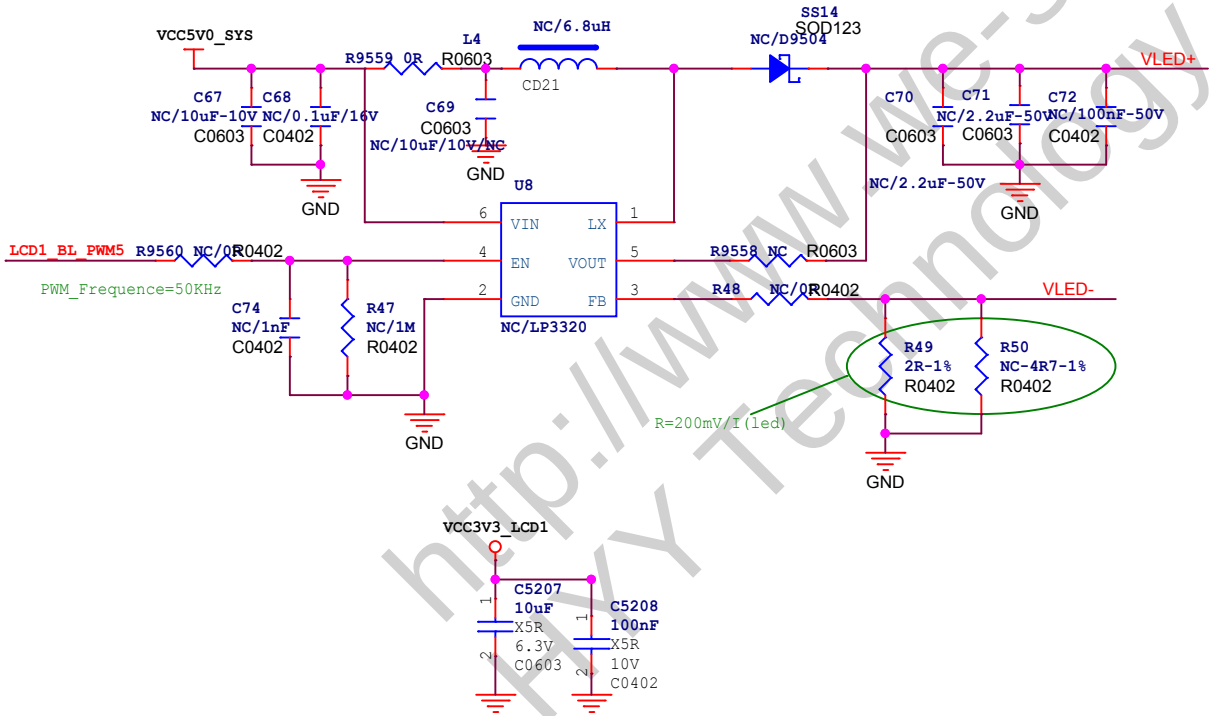
VCC_5V0
VCC5V_HDMI_TX
D5001 B5819W SOD123
R5004 DNP 0R 5% R0402

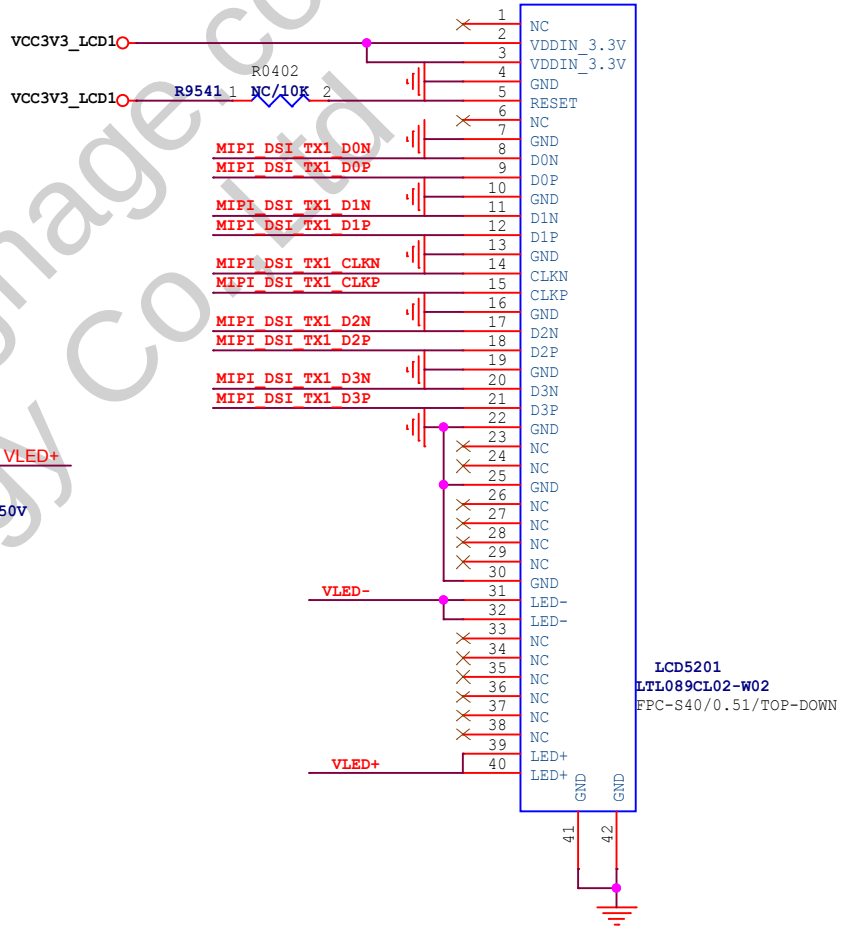
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_PC_SCH
File:	50.VO-HDMI2.0 TX
Date:	Wednesday, June 08, 2022
Rev:	V1.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet:	41 of 72

Single- MIPI1 LCM

MIPI_DSI_TX1_D0P
MIPI_DSI_TX1_D0N
MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_D1N
MIPI_DSI_TX1_D2P
MIPI_DSI_TX1_D2N
MIPI_DSI_TX1_D3P
MIPI_DSI_TX1_D3N
MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_CLKN
LCD1_BL_PWM5

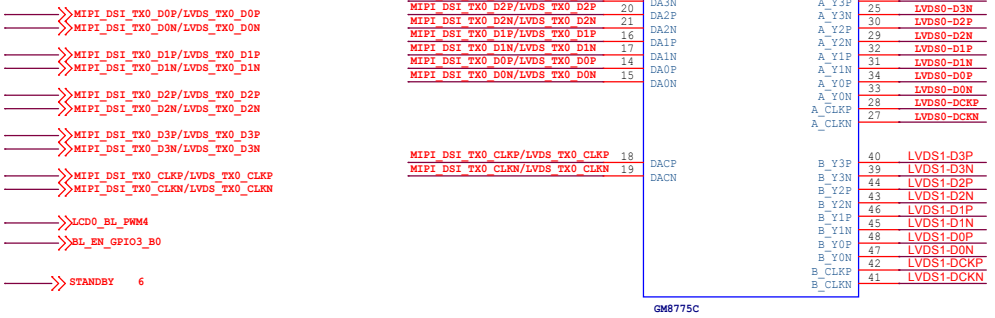
BACK LIGHT

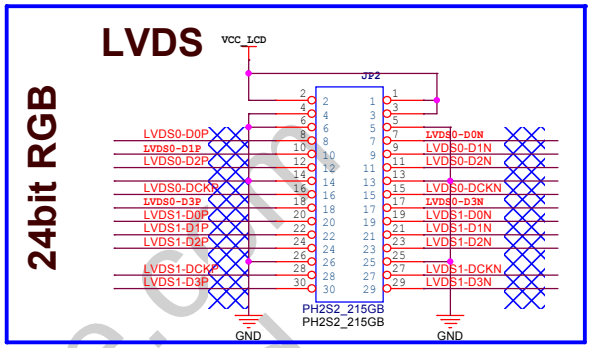


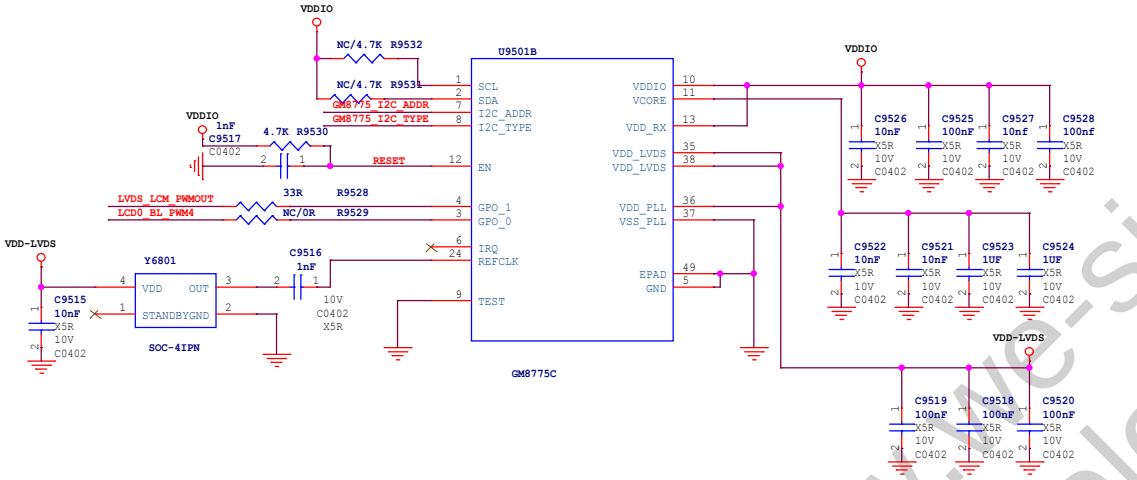


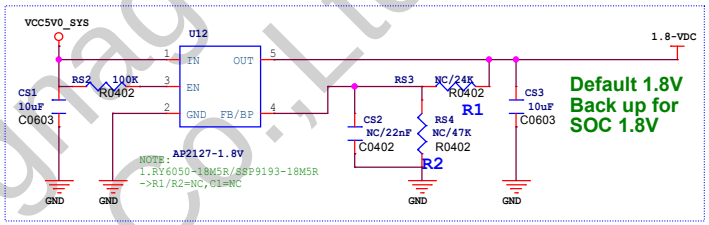
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	52.VO-LCM_MIPI_DSI_TX0/TX1				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	42 of 72

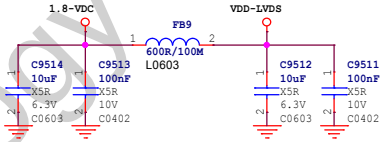
Single-LVDS LCM

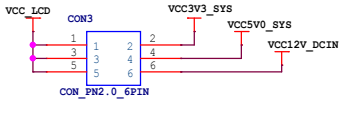


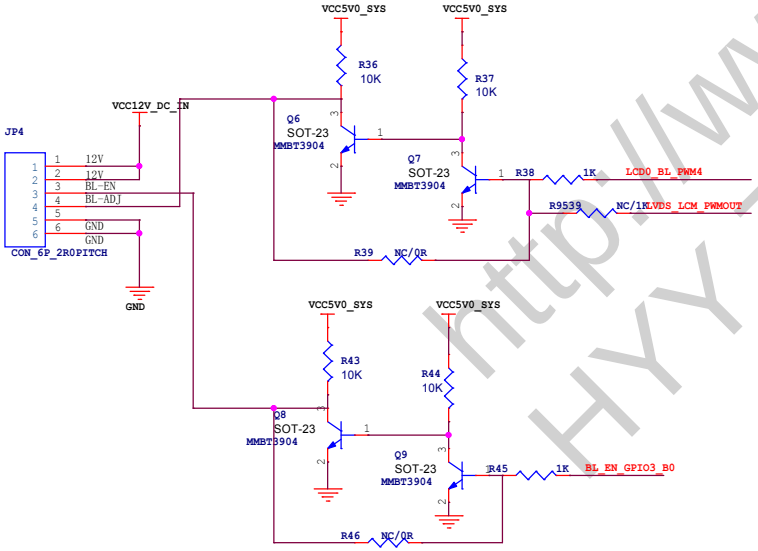


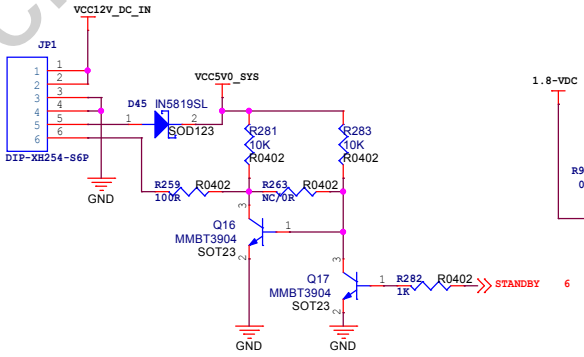


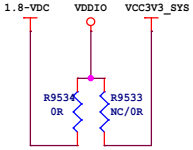


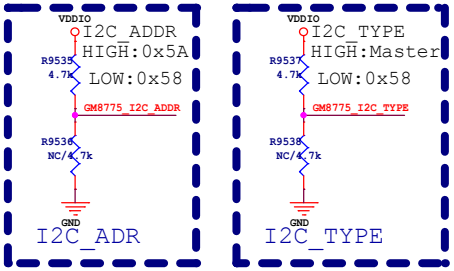








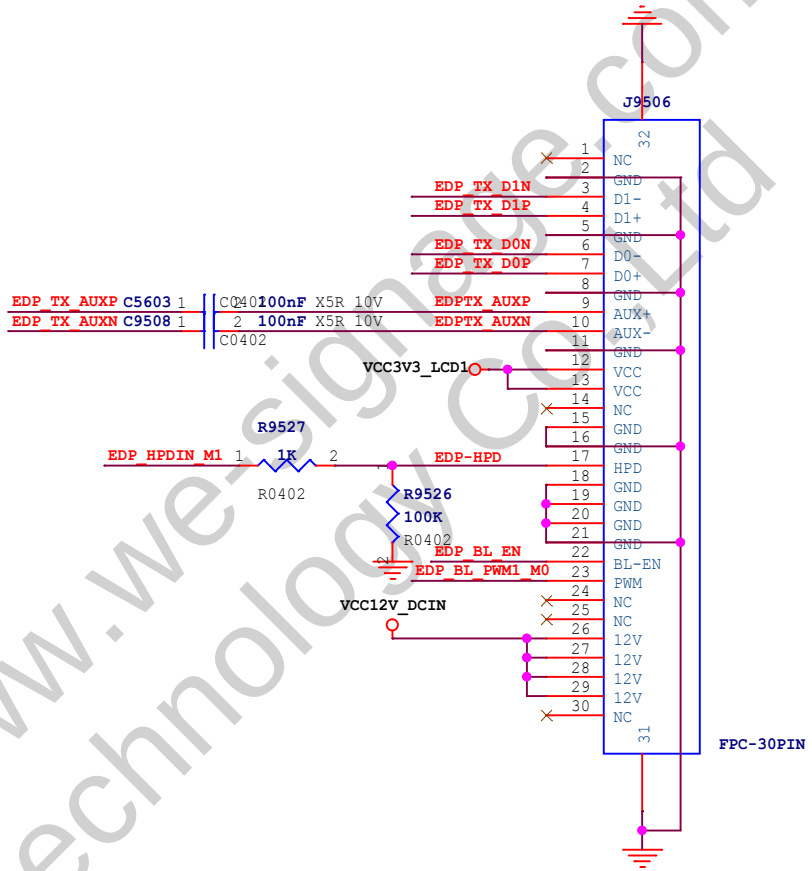


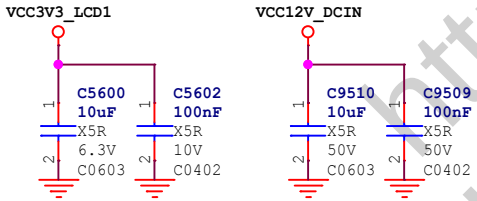


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	54.VO-LCM_LVDS TX				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	44 of 72

Single-eDP LCM

EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_AUXP
EDP_TX_AUXN
EDP_HPDIN_M1
EDP_BL_PWM1_M0
EDP_BL_EN

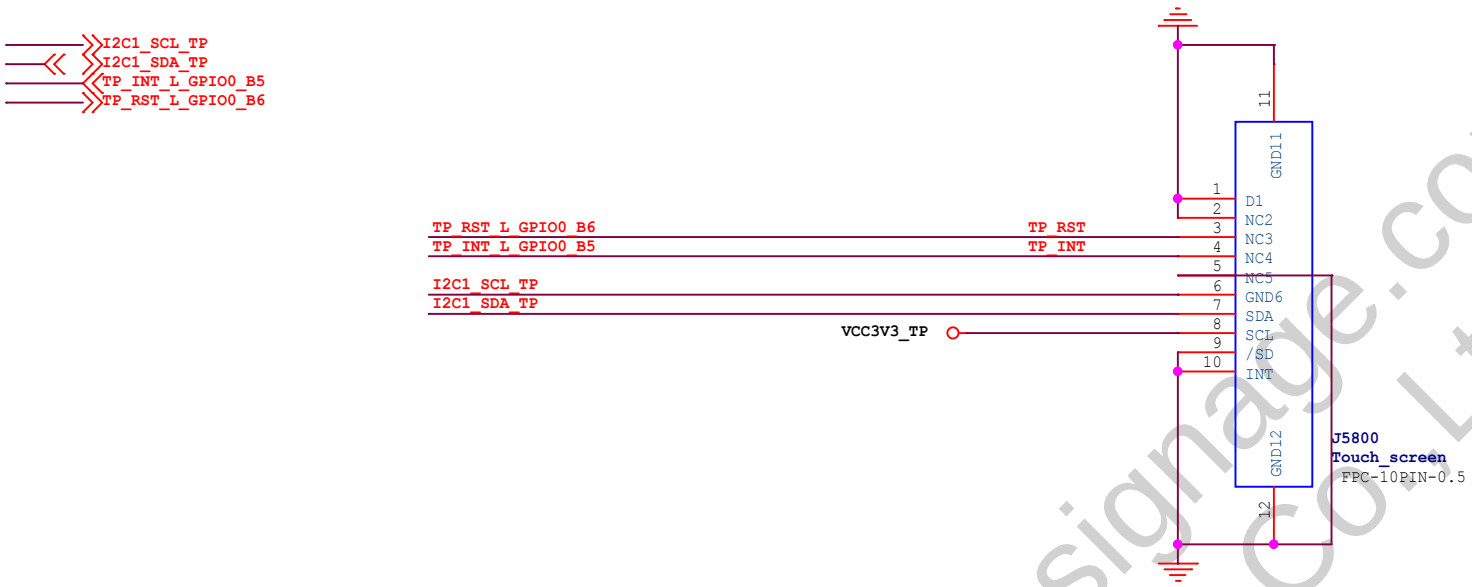




Rockchip Confidential

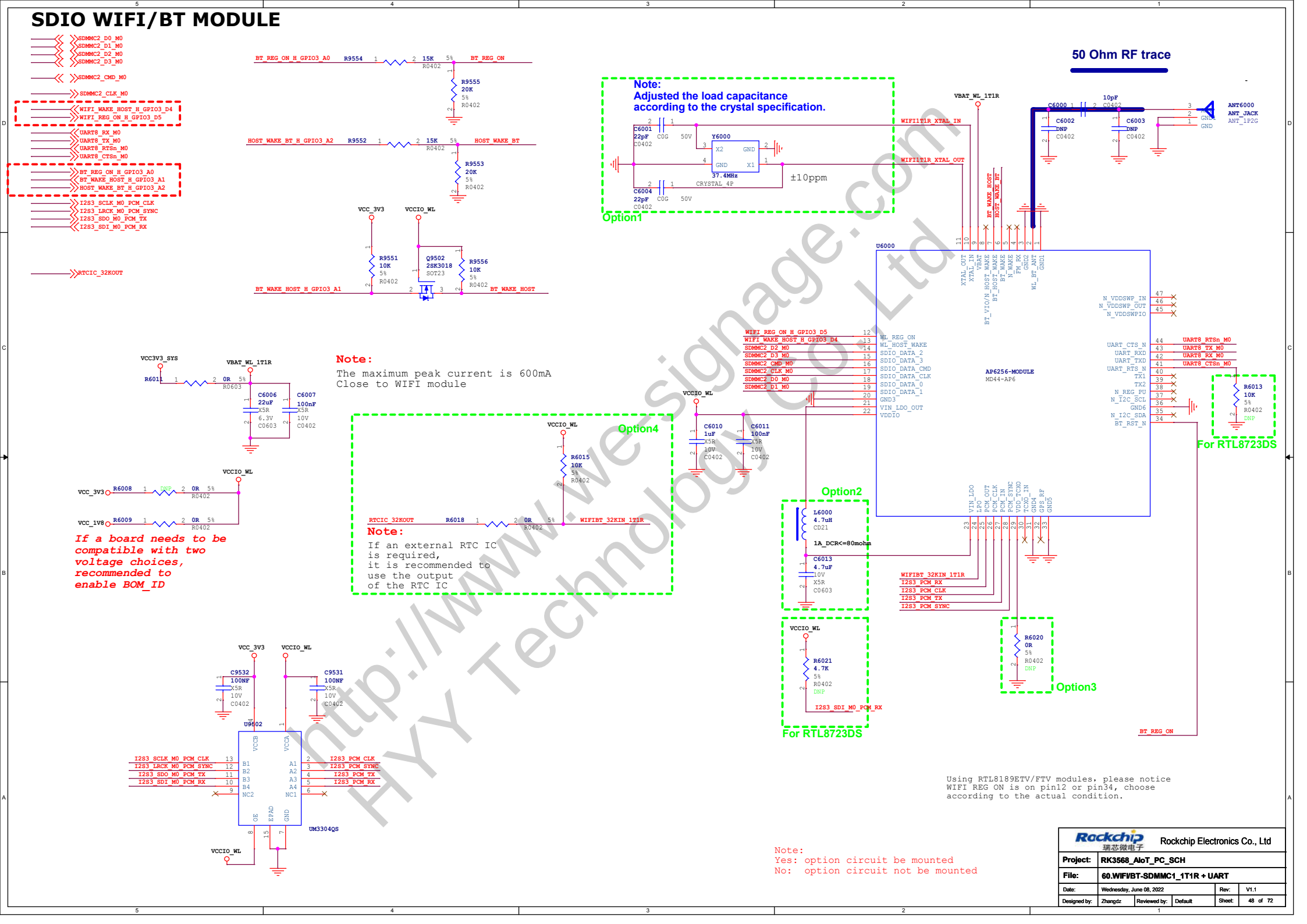
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	56.VO-LCM_eDP TX				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	45 of 72

Touch Panel connector



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	58.TP Connector_COF				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	46 of 72

SDIO WIFI/BT MODULE

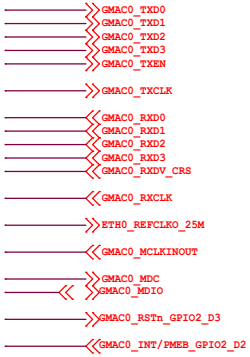


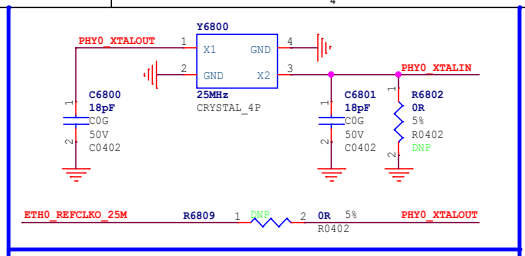
Using RTL8189ETV/FTV modules, please notice
WIFI_REG_ON is on pin12 or pin34, choose
according to the actual condition.

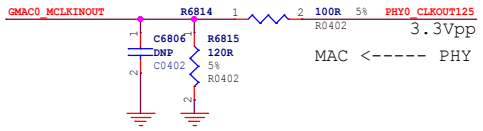
Note:
Yes: option circuit be mounted
No: option circuit not be mounted

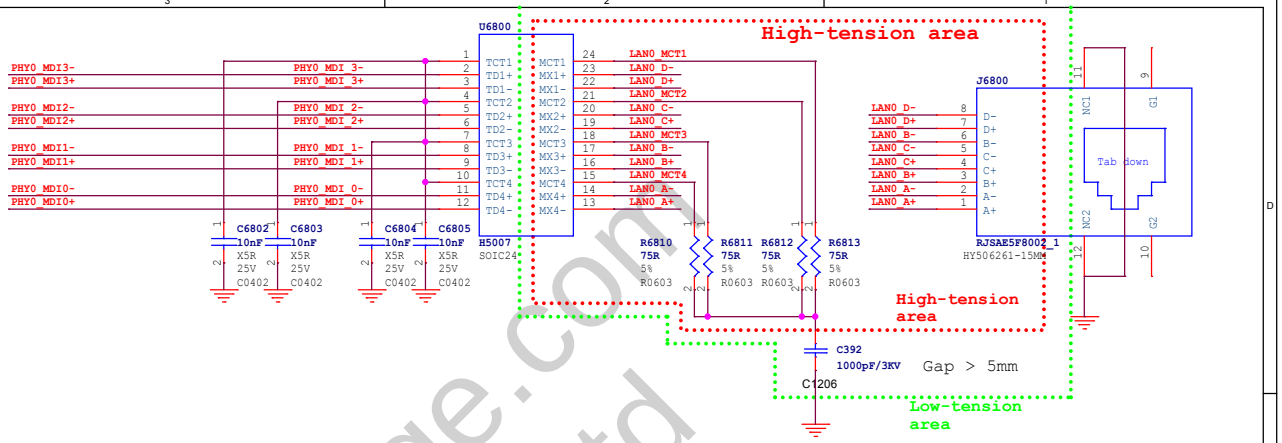
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	60.WIFI/BT-SDMMC1_1T1R + UART				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	48 of 72

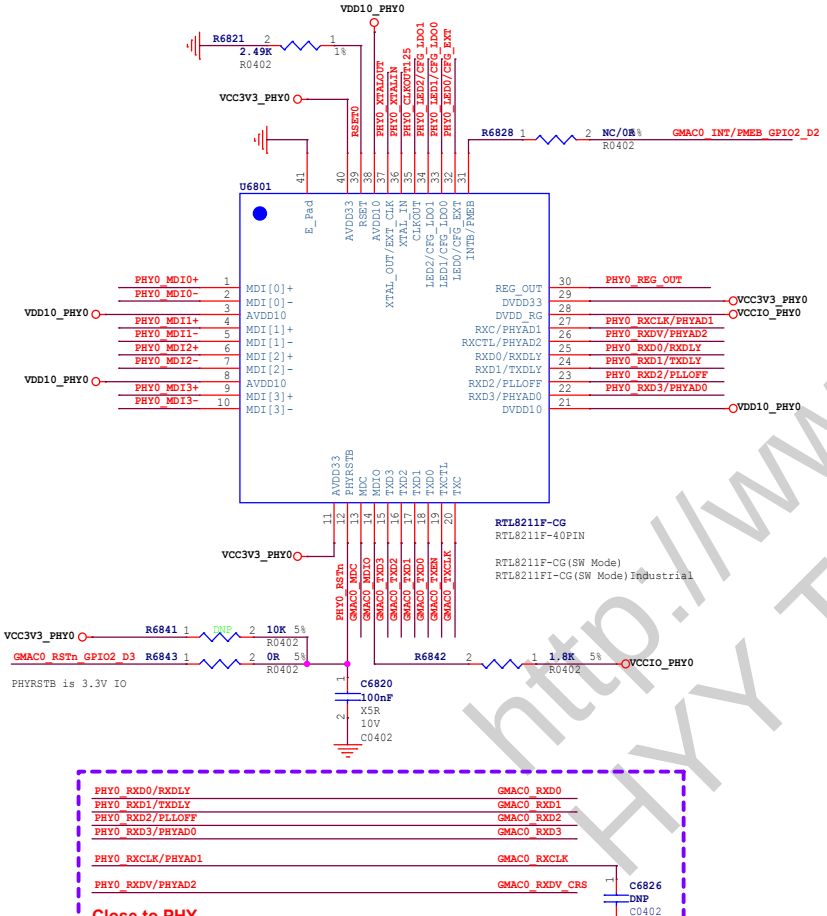
Giga PHY0

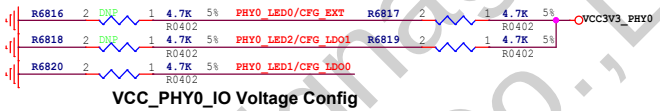


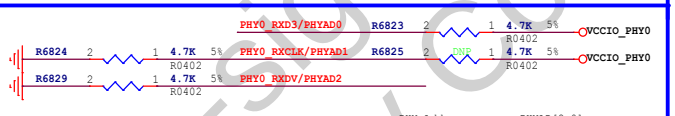


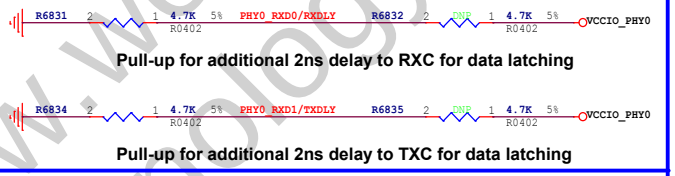


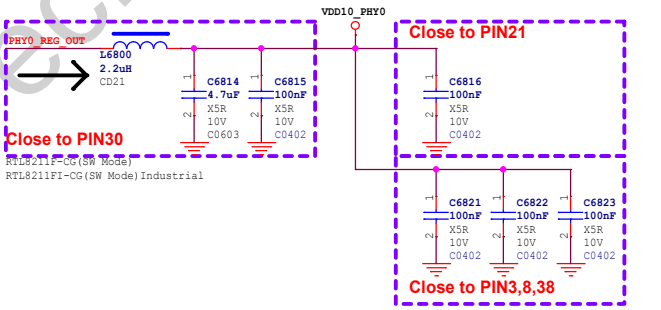






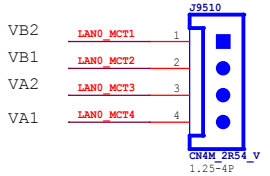




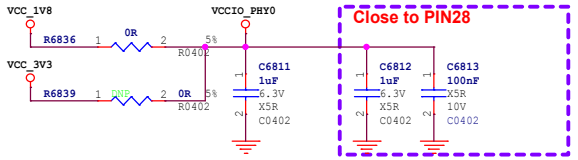


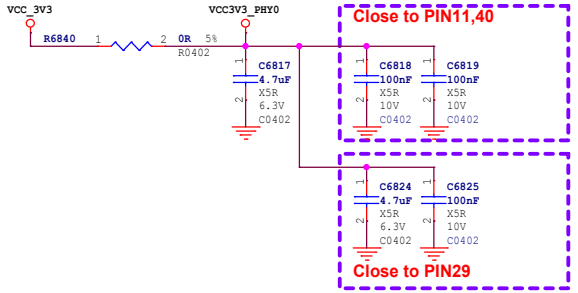
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

POE



Note:
According to the actual choice of mounted
Cannot be mounted at the same time





Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_PC_SCH				
File:	68.Ethernet-GEPHY_RGMII0				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	53 of 72

HP_DET_L_GPIO3_C2

MIC1_INN

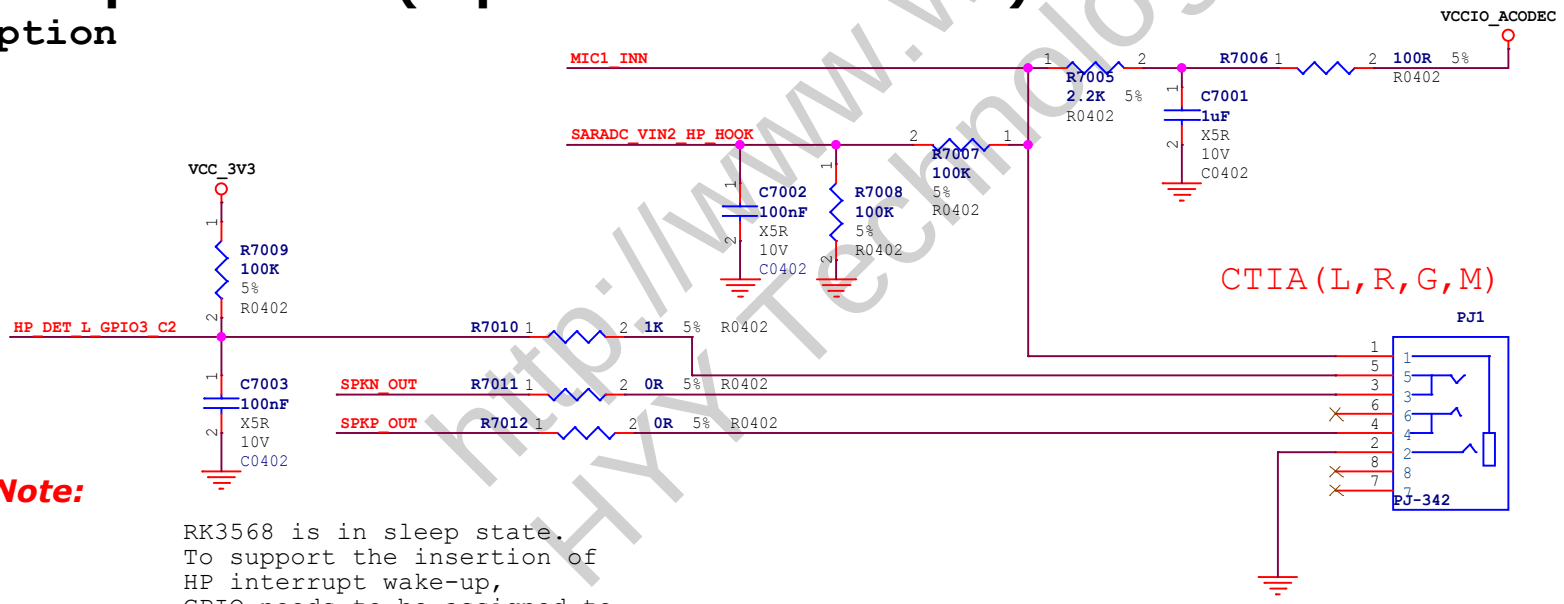
SARADC_VIN2_HP_HOOK

SPKN_OUT

SPKP_OUT

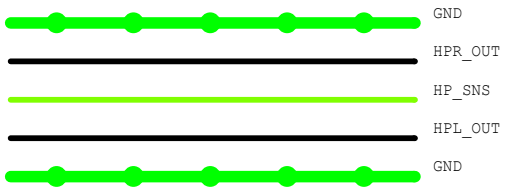
Headphone Jack(4-pole with DET & MIC)

Option



Layout note:

Place 0ohm resister close to GND pin of Headphone Jack ,
at layout,HP_SNS walks in the middle of HPL/HPR and acts as an accompanying line to avoid interference.



Note:

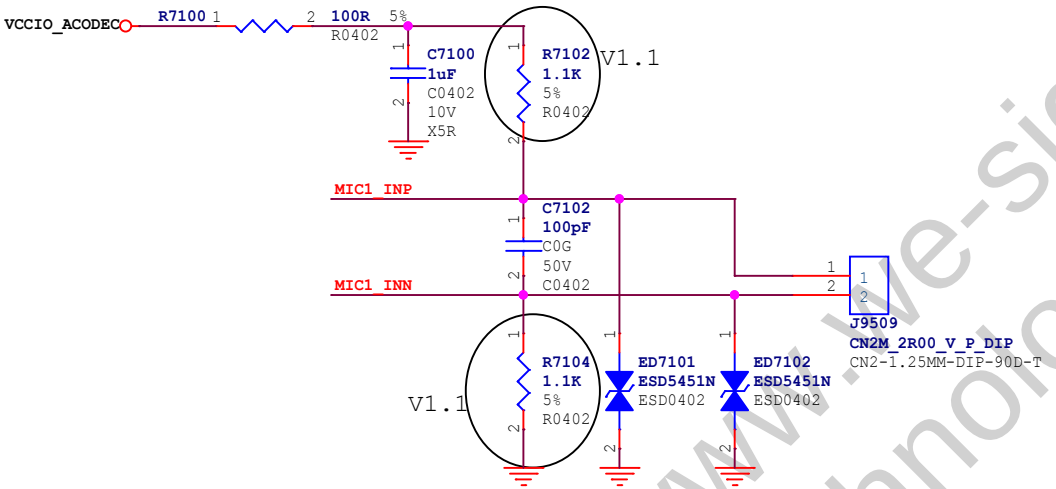
RK3568 is in sleep state.
To support the insertion of HP interrupt wake-up,
GPIO needs to be assigned to PMUIO0 or PMUIO1 or PMUIO2 domain

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	70.Audio-Headphone Port				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	55 of 72

MIC1_INP
MIC1_INN

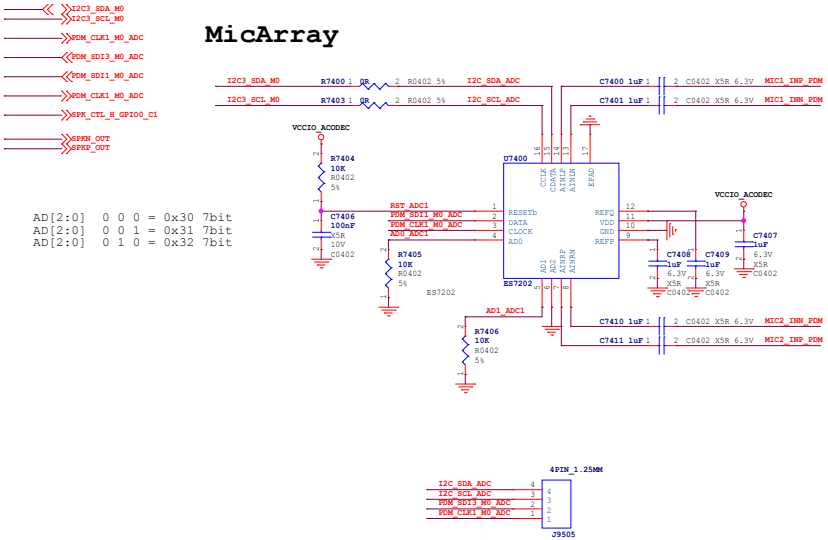
Default

MIC for 3-pole Headphone Jack

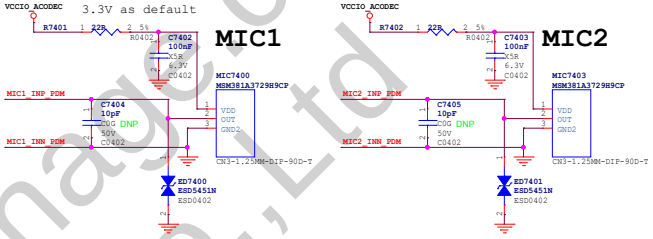


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	71.Audio-SingleMic+RK809_SPK				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	56 of 72

MicArray



MIC1

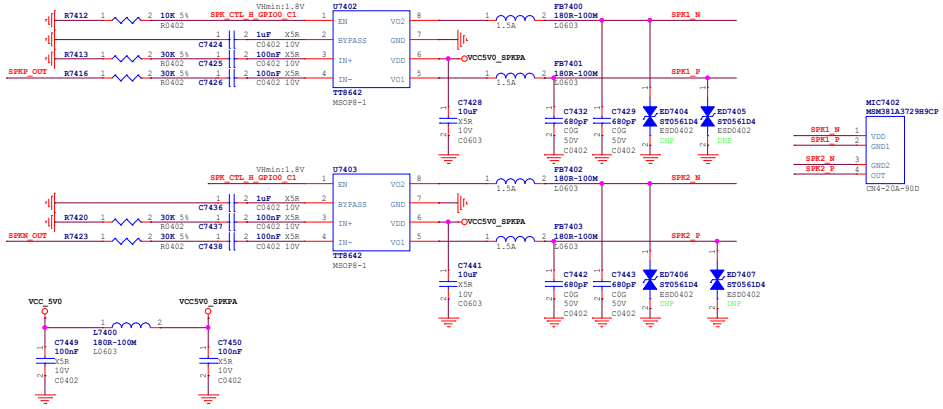


MIC2

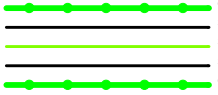
Loopback for Dual Speakers

Speaker Output

Note:4ohm/3W



Layout note:

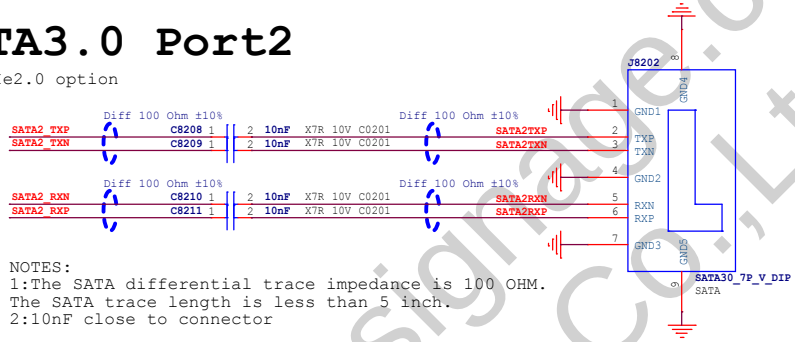


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_PC_SCH		
File:	74.Audio-MicArray+EXT Dual_SPK		
Date:	Wednesday, June 08, 2022	Rev:	V1.1
Designed by: Zhangdz	Reviewed by: Default	Sheet	58 of 72

SATA2_TXP
SATA2_TXN
SATA2_RXP
SATA2_RXN
I2S3_LRCK_M1

SATA3.0 Port2

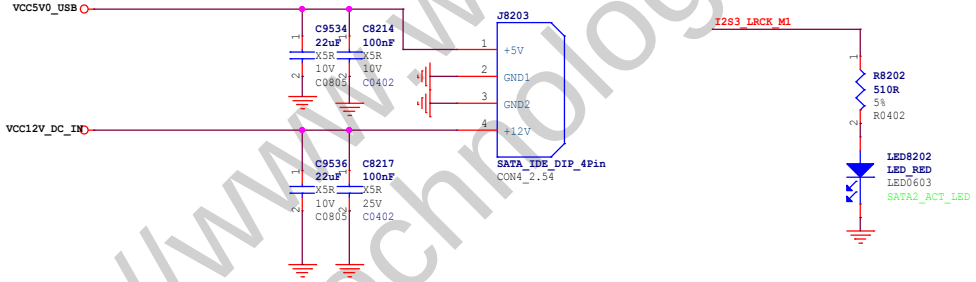
And PCIe2.0 option



NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA Power

The current is estimated according to the actual number of SATA
High power switching separate power supply is recommended for more than 2

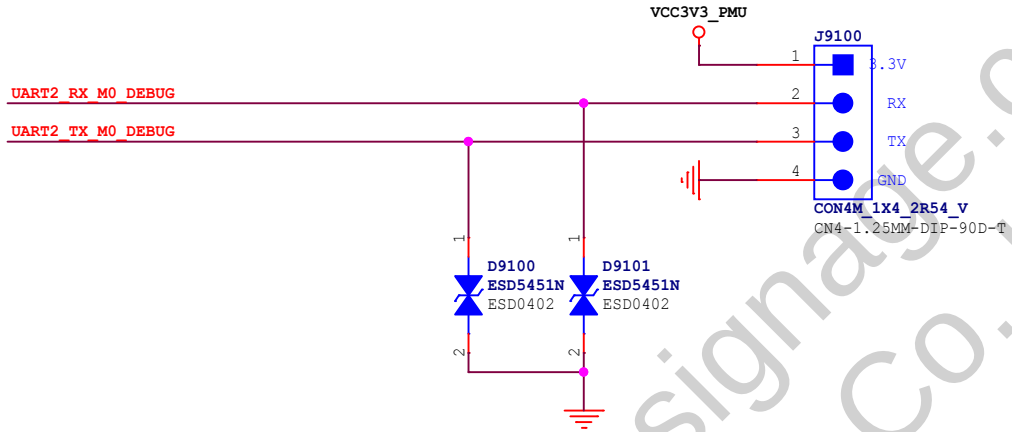


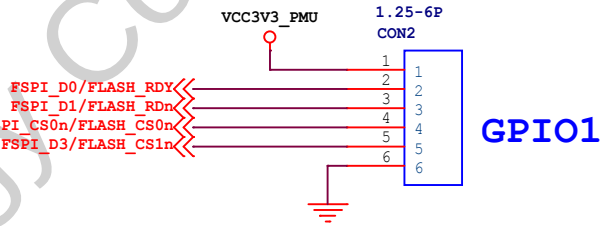
Rockchip Confidential

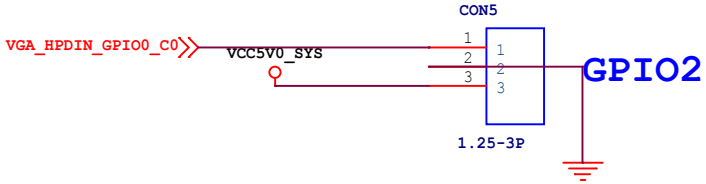
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	59 of 72

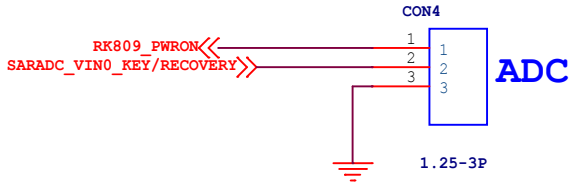
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2









Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	91.Debug UART/GPIO				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	68 of 72

Key Array

SARADC_VIN0_KEY/RECOVERY

SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

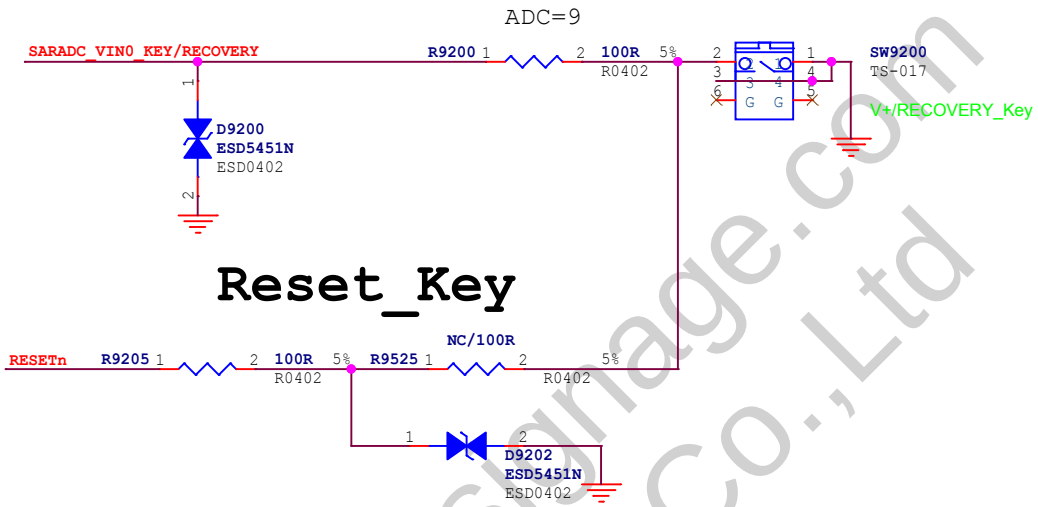
RESETn

RK809_PWRON

Note:

If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

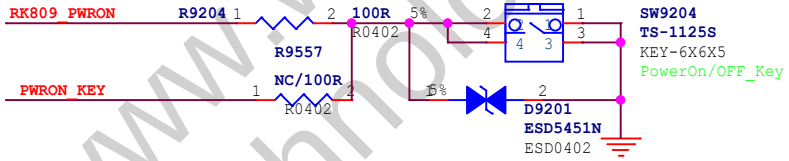
RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.



Reset_Key

PowerOn/OFF_Key

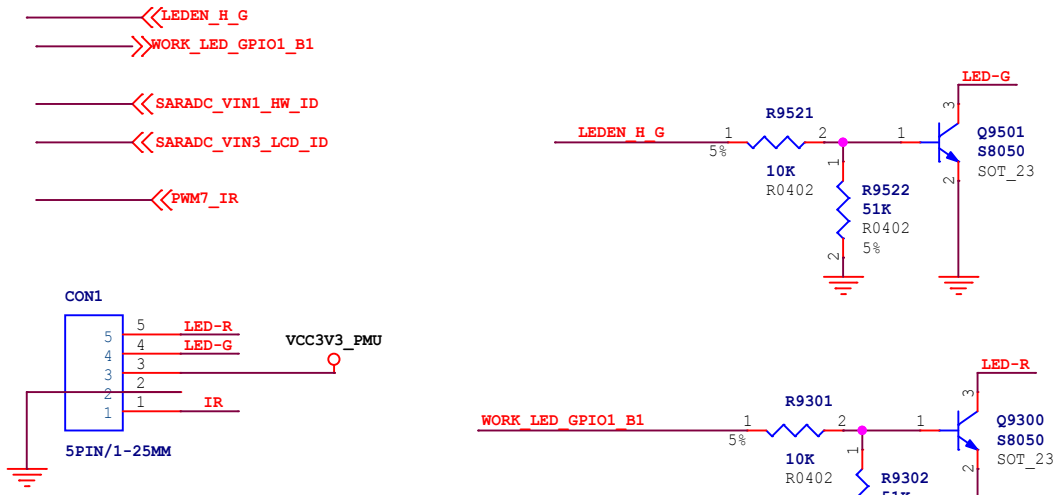
PWRON_KEY



SARADC

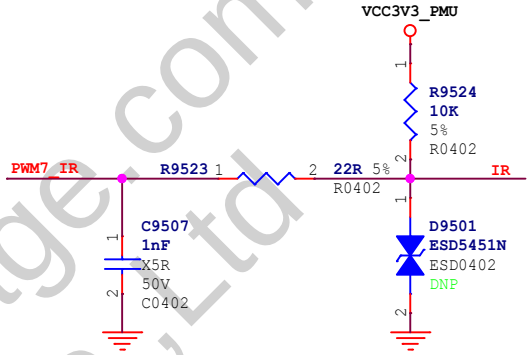
Voltage range:0v-1.8V

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	92.KEY Array/SARADC				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	69 of 72

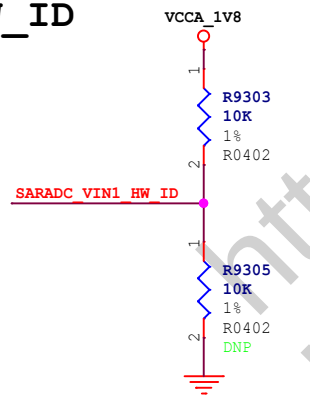


Working LED

IR Receiver

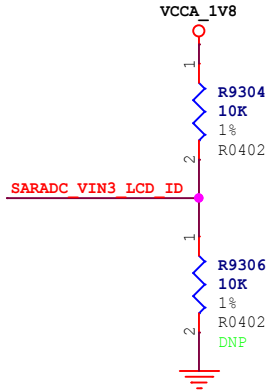


HW_ID



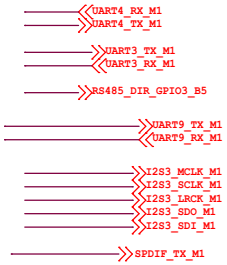
SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

BOM_ID

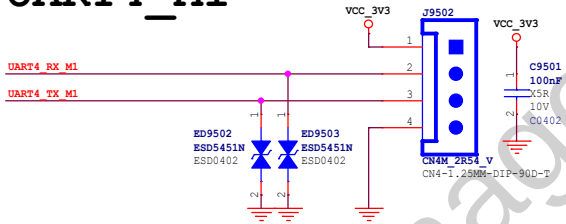


SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

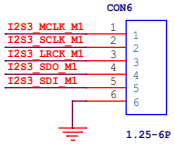
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	93.LED/HW_ID/BOM_ID/IR				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	70 of 72



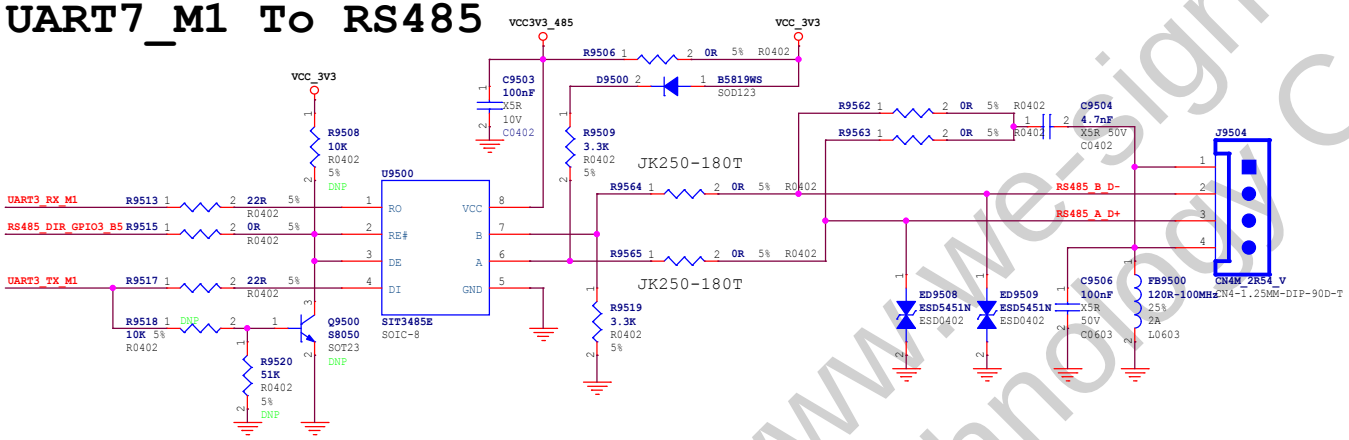
UART4_M1



I2S3_M1

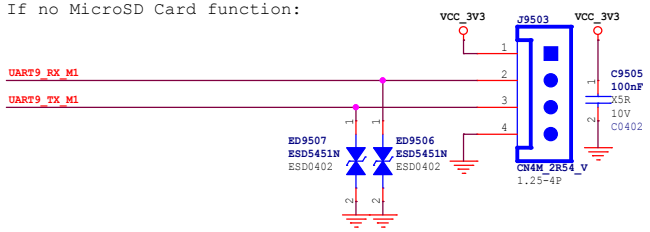


UART7_M1 To RS485



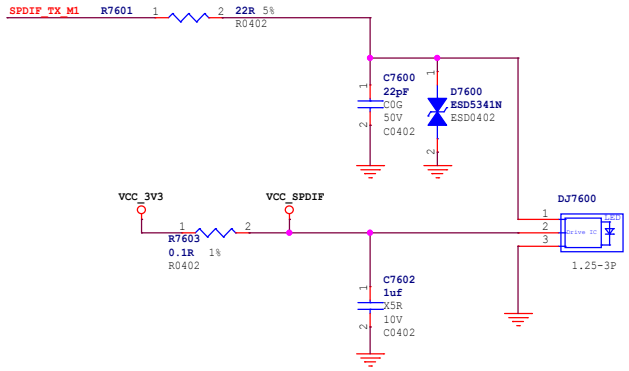
UART9_M1-Option

If no MicroSD Card function:



CAN0_M1-Option

If no MicroSD Card function:



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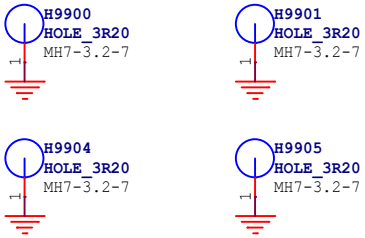
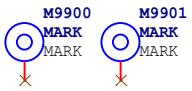
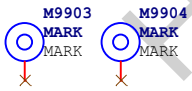
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_PC_SCH				
File:	95.UART/RS485/I2S3/SPDIF				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	71 of 72



TOP Mark



BOTTOM Mark



Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_PC_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Wednesday, June 08, 2022			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	72 of 72