EEL 4930/5934 - System-on-Chip Design

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Final Project Report

Problems Faced:

For Task 3, we encountered issues with audio playback. The audio sounded strange, with notes not sounding as they were intended. We discovered that the problem was due to the notes not lasting long enough. By adjusting the values written to the PWM IP's slave registers—specifically the pwm_period and duty_cycle—we were able to resolve the issue.

We also had problems with the interrupt logic used to trigger sounds. Sounds were playing at incorrect times, which we traced back to coding issues. One example was a bug with the point_scored_pending flag: it was only being set when the ball reached the far left of the screen, but not when it reached the far right. For other issues, we did some debugging with print statements and the debugger tool to fine tune the code.

For Task 4, we struggled with accessing the CDMA controller due to a misunderstanding of how Vitis handles platform updates. We failed to properly regenerate the platform and bitstream after modifying the block diagram, which meant our hardware changes weren't reflected in the software. We ultimately resolved this by redoing the block diagram and creating a new Vitis application from scratch. Once that was done, implementing the CDMA transfer logic was relatively simple—it just involved writing a few lines of code to replace what was previously a Xil_Out32 function.

What you learned:

We learned how to use PWM to output analog values with digital outputs, mostly through following the tutorial given in the course files. We improved our ability to use SoC tools (Vivado and Vitis) to make new IPs, integrate them into existing projects, and program applications with Vitis. We also learned how to debug applications better using the debugging tool and breakpoints supplied by the debug module in Vivado. We also learned how to use the CDMA module to control memory movement between different components of the same bus. Though we were already familiar with how DMA systems work, we had to learn how to incorporate it into a block diagram with other components properly with AMD's documentation.

Other:

N/A