Total No. of Questions : 4]

SEAT No. :

PC-448

[Total No. of Pages : 2

[6359]-569

S.E. (Computer Science and Engineering) (Data Science) (Insem.)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2019 Pattern) (Semester - III) (210644)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates :

1) *Answer Q.1 or Q.2, Q.3 or Q.4.*
2) *Assume suitable data, if necessary.*
3) *Draw neat diagrams wherever necessary.*
4) *Figures to the right indicate full marks.*

Q1) a) Convert the following expressions into their standard SOP form [5]
   i) Y = AB + AC + BC
   ii) Y = A + BC + ABC

b) Simplify the expression F (A, B, C, D) = Σm (3,4,5,7,9,13,14,15) using K-Map method. [5]

c) Represent following numbers [5]
   i) 396: 1. BCD 2. Excess -3 code.
   ii) Represent +40 and -40 decimal numbers using 2's complement.

OR

Q2) a) Convert the following numbers
   i) $(A72E)_{16} = (\ )_8$
   ii) $(247.36)_8 = (\ )_{16}$

b) Minimize the following expression using K-Map : [5]
$f(A, B, C, D) = \Pi M (4, 6, 10, 12, 13, 15)$ and Implement using logic gates.

c) Convert the expression Y = (A+B) (A+C) (B+C) into the Canonical POS form. [5]

Q3) a) Design and Implement the Full Adder using two half adder. [5]

b) Design and Implement 4 bit BCD to Excess-3 code converter circuit using logic gates. [5]

c) Implement the following Boolean function using 8 : 1 multiplexer [5]
F(A, B, C, D) = Σm (2, 4, 5, 7, 10, 14)

OR

P.T.O.

Q4) a) Implement the Full Subtractor using a 1:8 Demultiplexer. [5]

b) Design a 4 bit Gray to Binary code converter? State the application of Gray code. [5]

c) Design and Implement 2 bit Comparator. [5]

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