Low-Power 3T NAND Gate

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***Abstract*—Energy efficiency is one of the most sought features for modern electronic systems designed for high-performance and portable applications. NAND Gate is the most preferred universal gate since it occupies less area and offers minor delay than NOR when designed with CMOS Technology and is used numerous times in other gates and integrated circuits. This paper proposes the design of three transistor(3T)-based NAND gates with the same output logic as the primary CMOS NAND Gate. The proposed method will demonstrate better performance in low-power consumption, reduced area, and higher speeds, the characteristics most sought after in VLSI circuits for low-power System-on-Chip (SoC) applications.**

***Index Terms*—Low-power, CMOS, pass-transistor, NAND gate, energy-efficient**

I. Introduction

Over the past decade, the power problem has emerged as one of the fundamental limits facing the future of CMOS integrated circuit design. Depending upon the application, reduction of power consumption of VLSI circuits can use numerous methods. They can range from fundamental physics [1] to high-level measures such as clock-gating [2]. Past studies involve floating-gate for UltraLow-Voltage (ULV) and low-Power logic [3]. While considering low-power, balancing the trade-offs of the area and the technology node is well suited for low-power system-on-chip applications in the industry. Therefore, for optimum performance according to the requirements of low-power SoCs, the approach of 3T NAND is taken here [4].

II. 3T NAND

The basic NAND using CMOS only is 4T CMOS. The proposed design of three transistor NAND is based on modified CMOS inverter and PMOS pass-transistor logic. The new design of 3T NAND gate using three transistors is shown in Fig. 1. The schematic is implemented in 28nm technology.

When input A is at logic one, the inverter on the left (M1 and M3) functions as a normal CMOS inverter. Therefore, the output is the complement of input B. When the input A is at logic zero, the CMOS inverter output is at high impedance. However, the PMOS pass-transistor M2 is turned ON and the output gets the logic value as logic 1 (VDD). The operation of the circuit can be seen in the transient analysis of the circuit in Fig. 2.

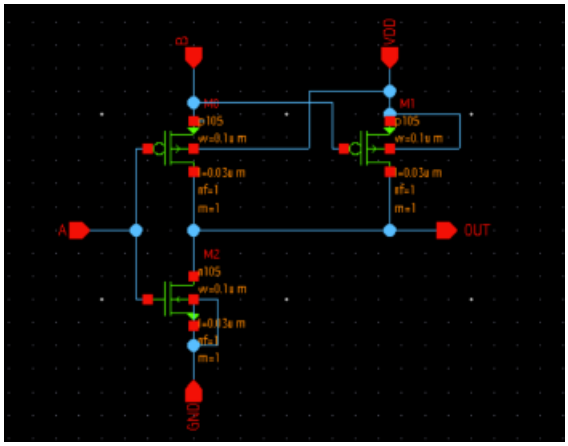

Fig. 1. 3T NAND gate schematic.

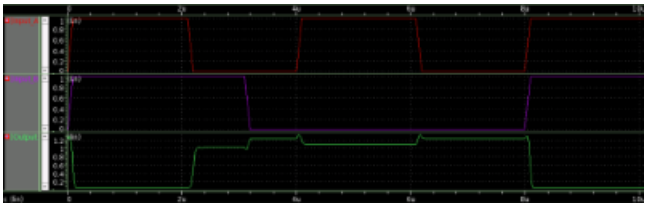

Fig. 2. I/O waveforms for 3T NAND gate at VDD=1.6 V

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