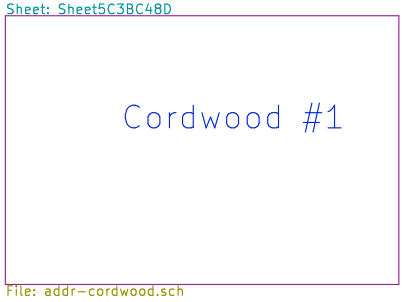
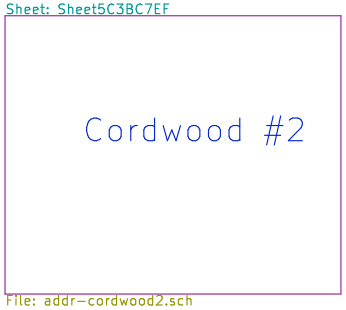

Sheet: Sheet5C3BC48D
Cordwood #1
File: addr-cordwood.sch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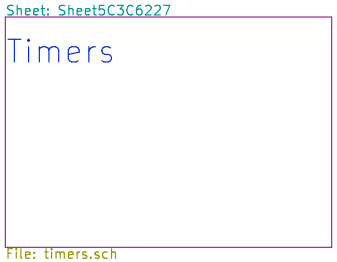
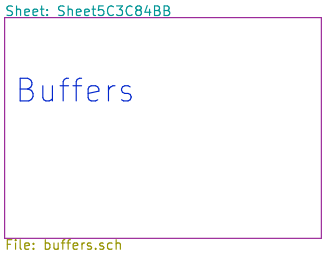
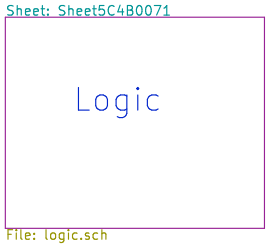
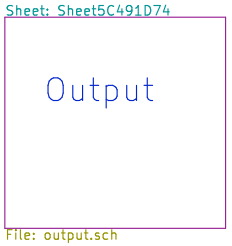
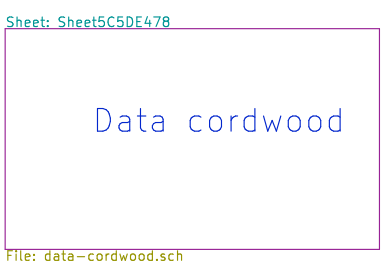
Cordwood #2
File: addr-cordwood2.sch

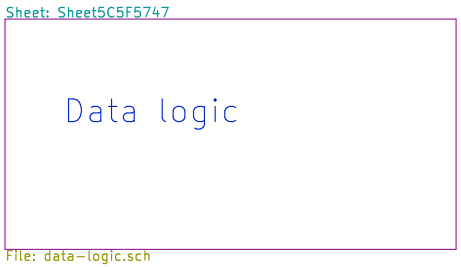

Sheet: Sheet5C3C6227
Timers
File: timers.sch

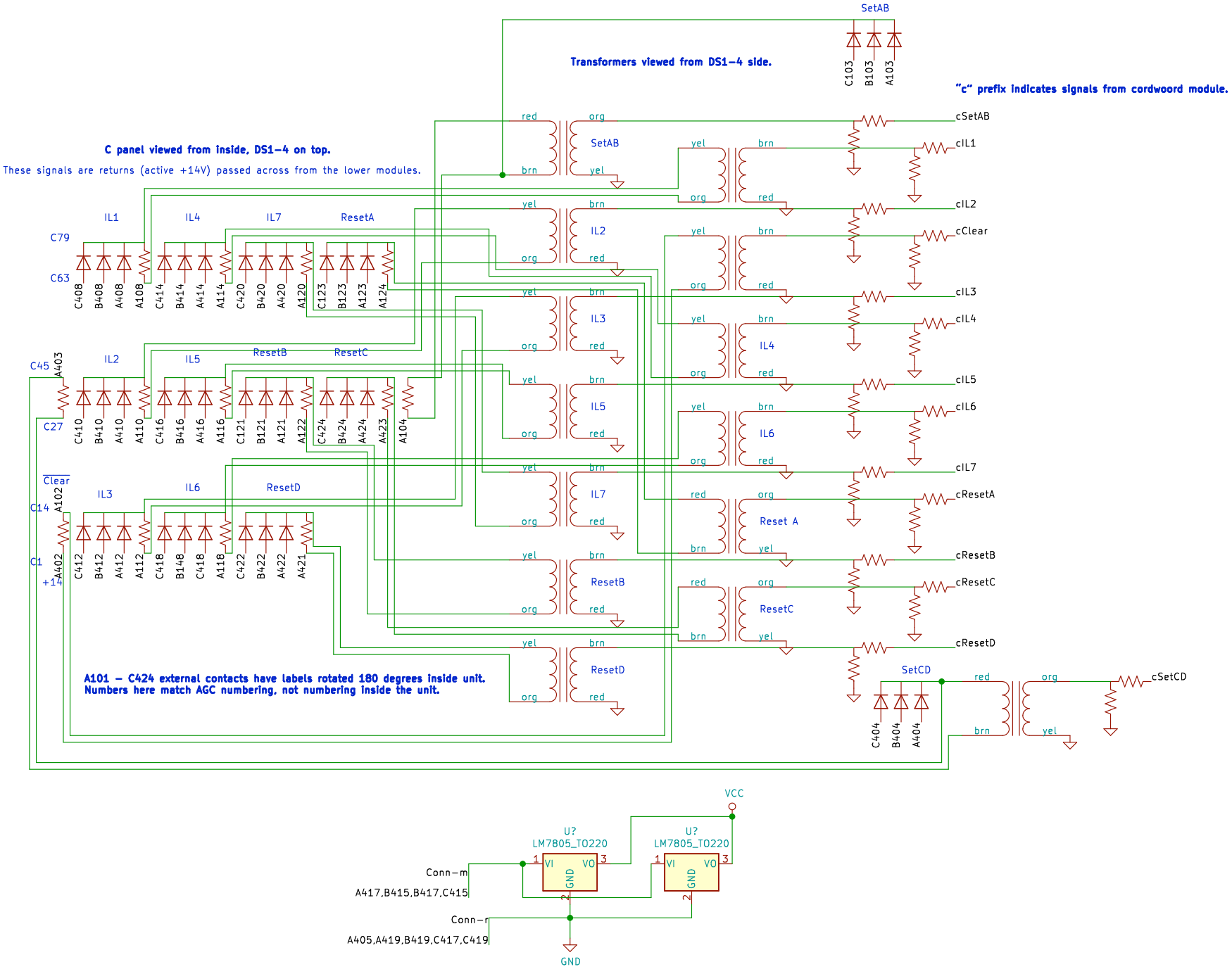

Sheet: Sheet5C3C84BB
Buffers
File: buffers.sch


Sheet: Sheet5C4B0071
Logic
File: logic.sch

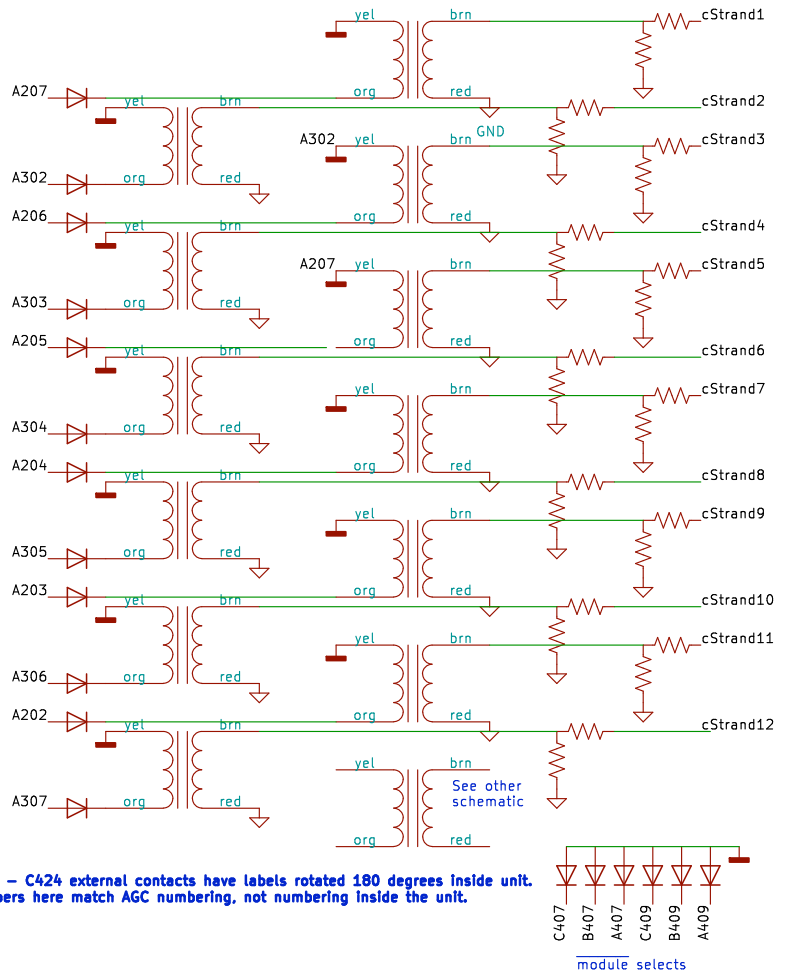

Sheet: Sheet5C491D74
Output
File: output.sch


Sheet: Sheet5C5DE478
Data cordwood
File: data-cordwood.sch

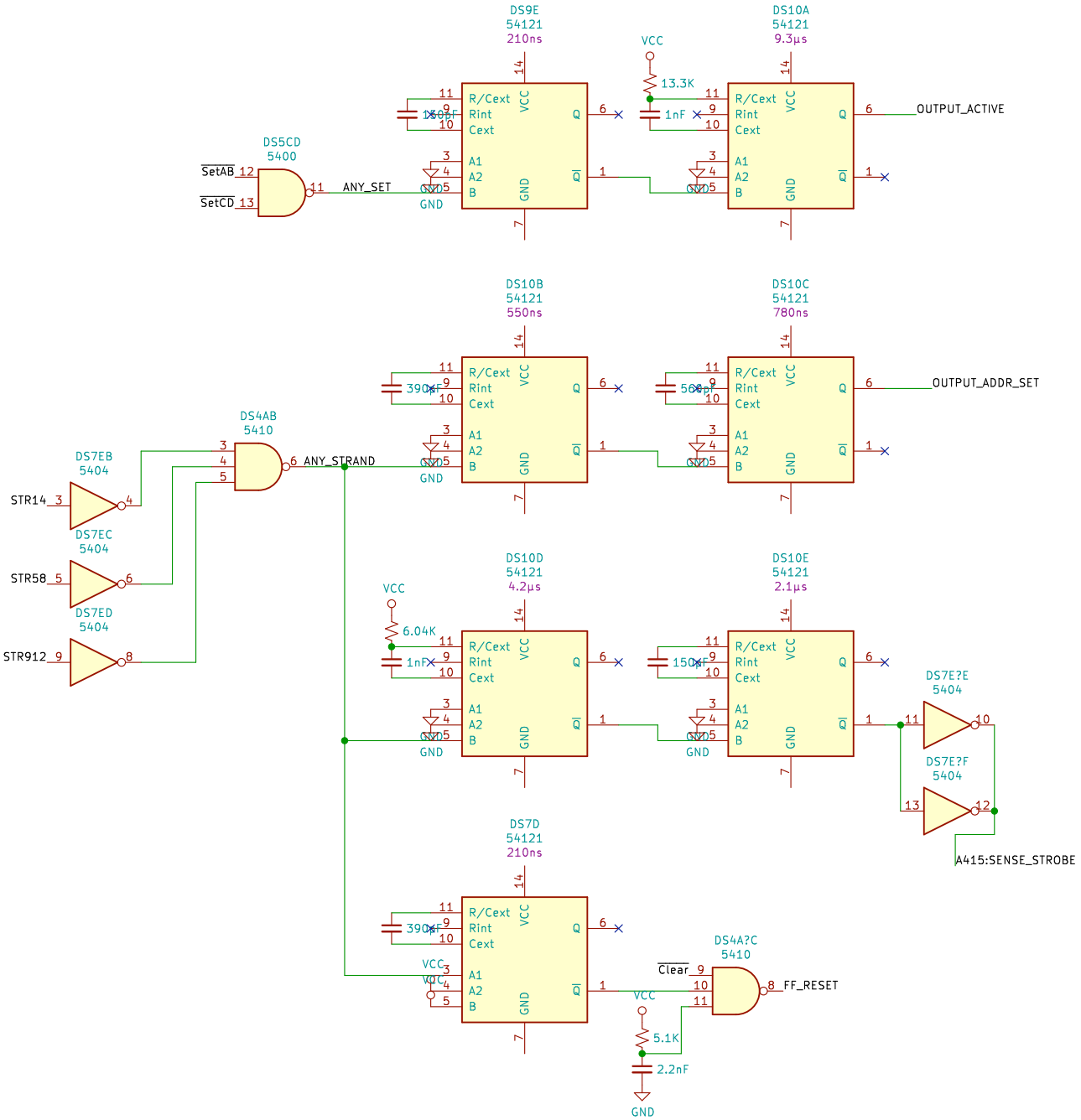

Sheet: Sheet5C5F5747
Data logic
File: data-logic.sch

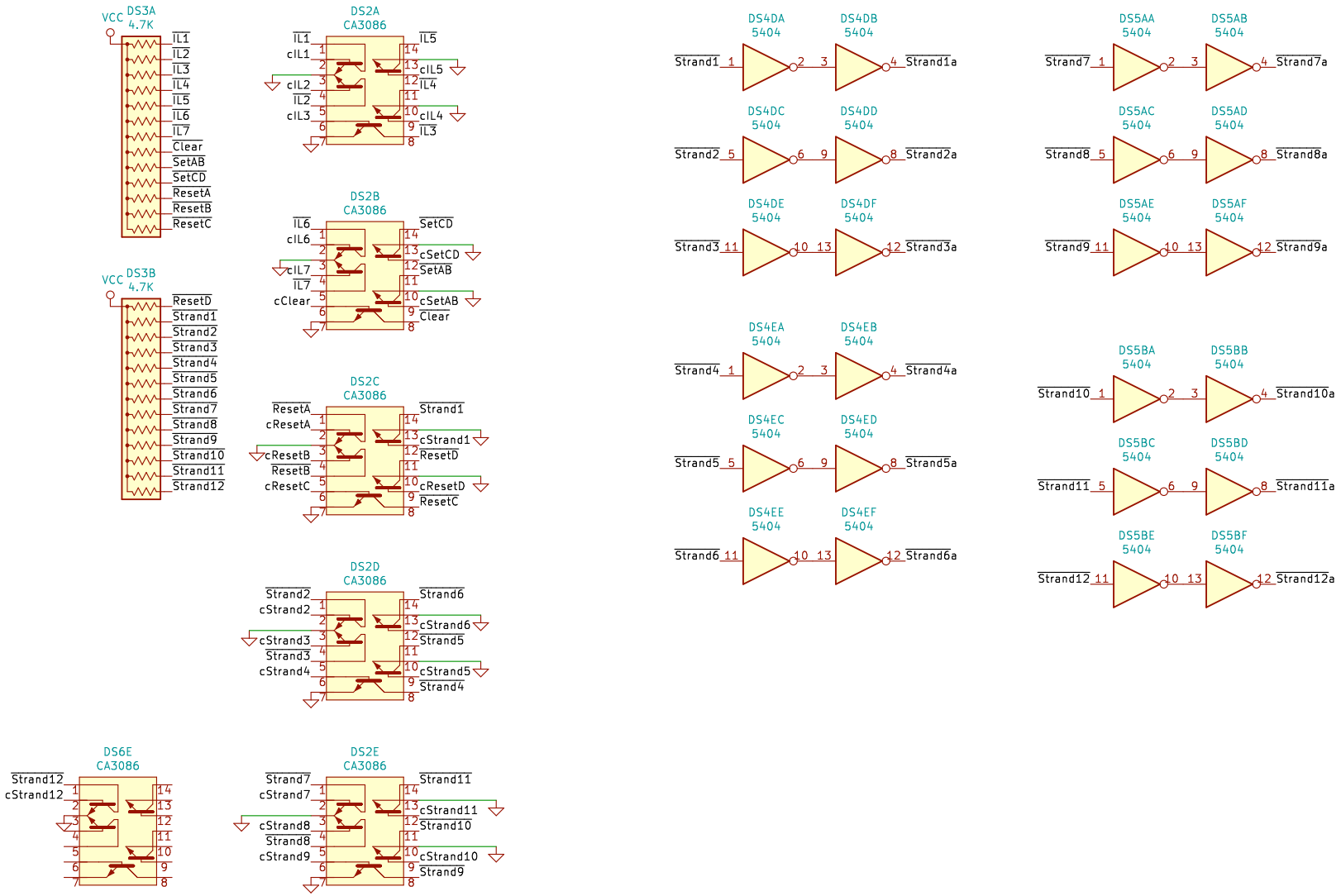

SetAB
C103
B103
A103
Transformers viewed from DS1–4 side.
"c" prefix indicates signals from cordwoord module.
C panel viewed from inside, DS1–4 on top.
These signals are returns (active +14V) passed across from the lower modules.
IL1
IL4
IL7
ResetA
C79
C63
C408
B408
A408
A108
C414
B414
A414
A114
C420
B420
A420
A120
C123
B123
A123
A124
IL2
IL5
ResetB
ResetC
C45
A403
C27
C410
B410
A410
A110
C416
B416
A416
A116
C121
B121
A121
A122
C424
B424
A424
A423
A104
Clear
IL3
IL6
ResetD
C14
A102
C1
A402
+14
C412
B412
A412
A112
C418
B148
C418
A118
C422
B422
A422
A421
A101 – C424 external contacts have labels rotated 180 degrees inside unit.
Numbers here match AGC numbering, not numbering inside the unit.
red
org
brn
yel
SetAB
IL1
IL2
IL3
IL4
IL5
IL6
IL7
ResetB
ResetC
ResetD
Reset A
cSetAB
cIL1
cIL2
cClear
cIL3
cIL4
cIL5
cIL6
cIL7
cResetA
cResetB
cResetC
cResetD
SetCD
C404
B404
A404
cSetCD
VCC
U?
LM7805_TO220
VI
VO
GND
Conn–m
A417,B415,B417,C415
Conn–r
A405,A419,B419,C417,C419
GND

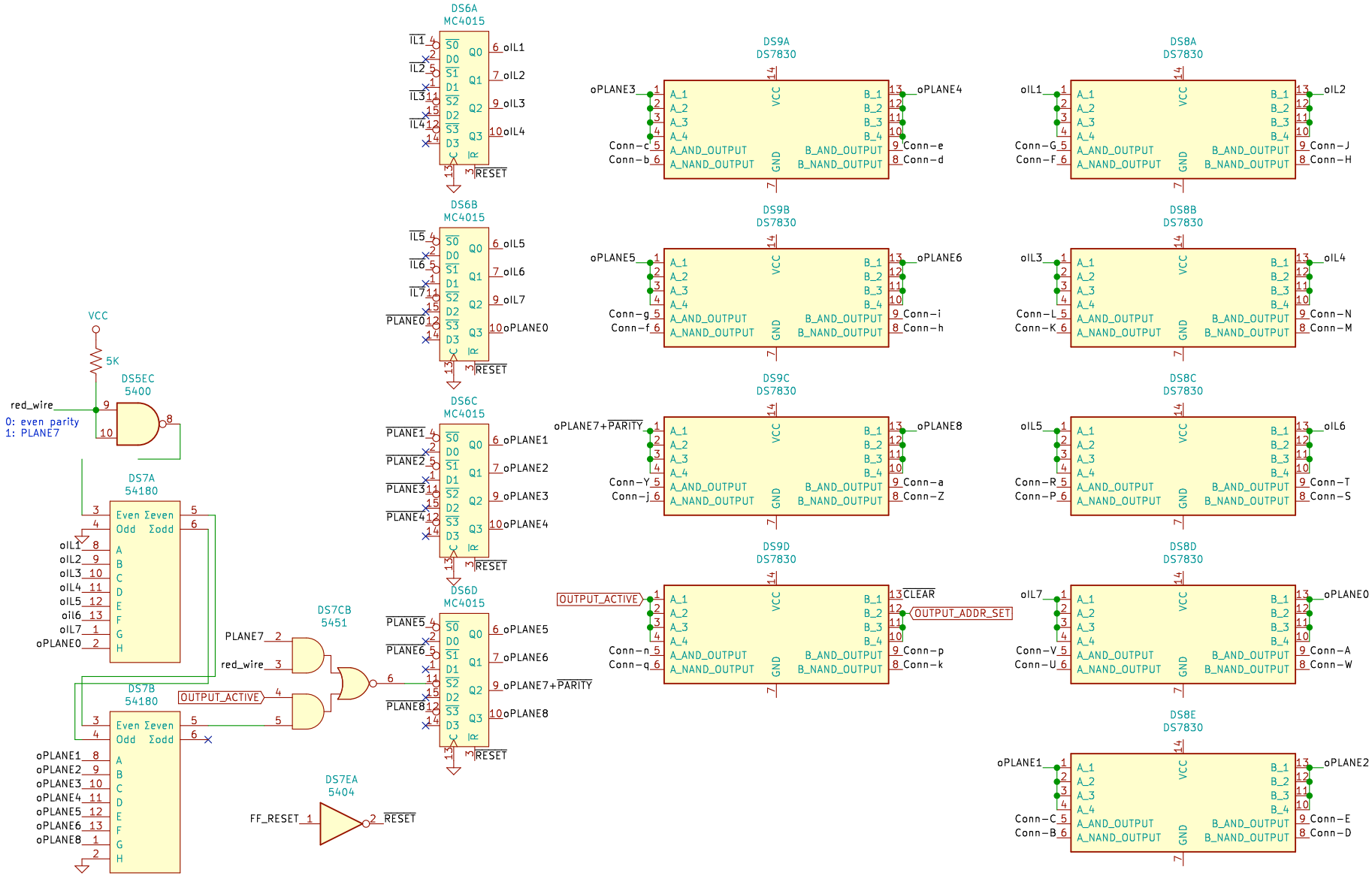
Transformers viewed from DS1–4 side.

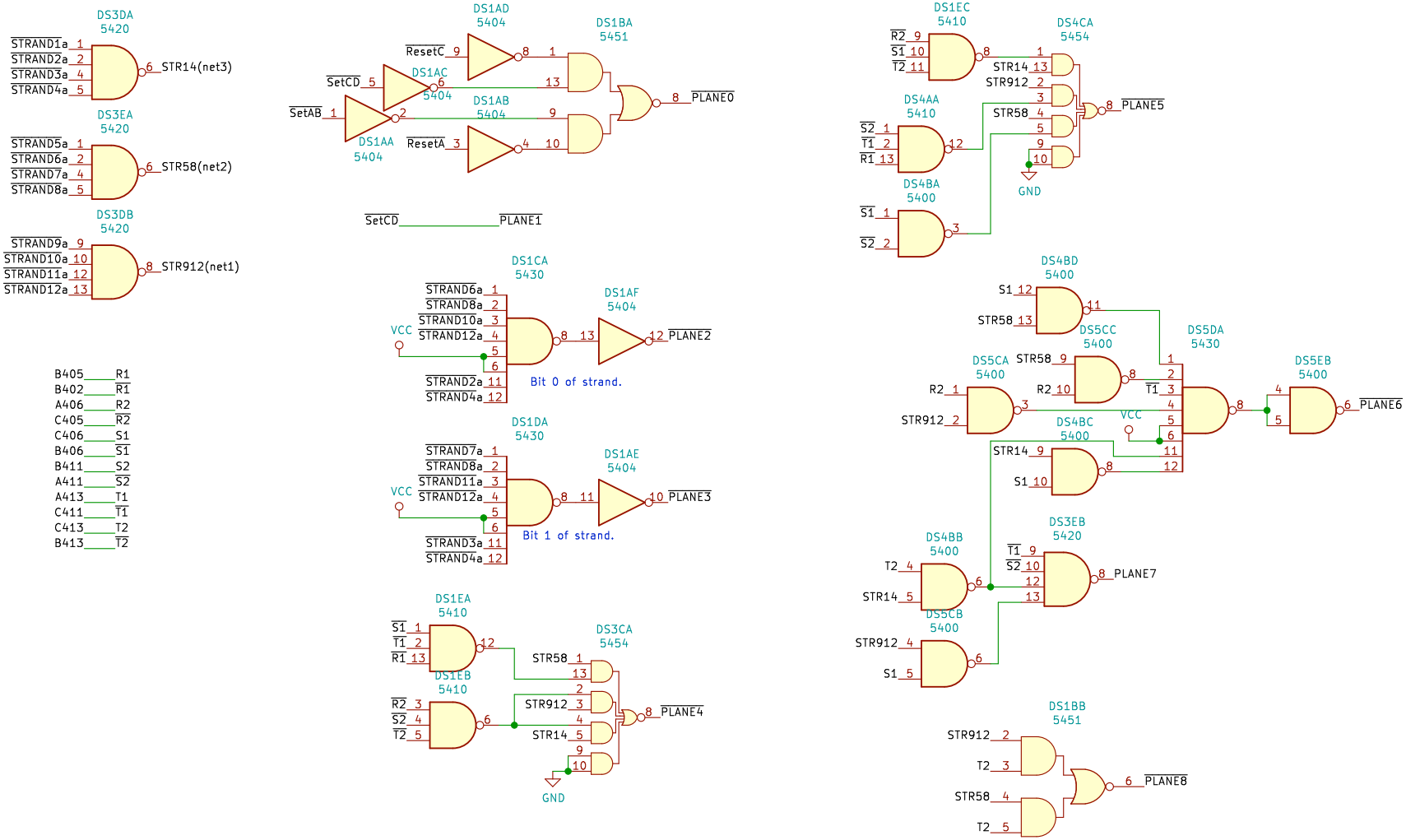


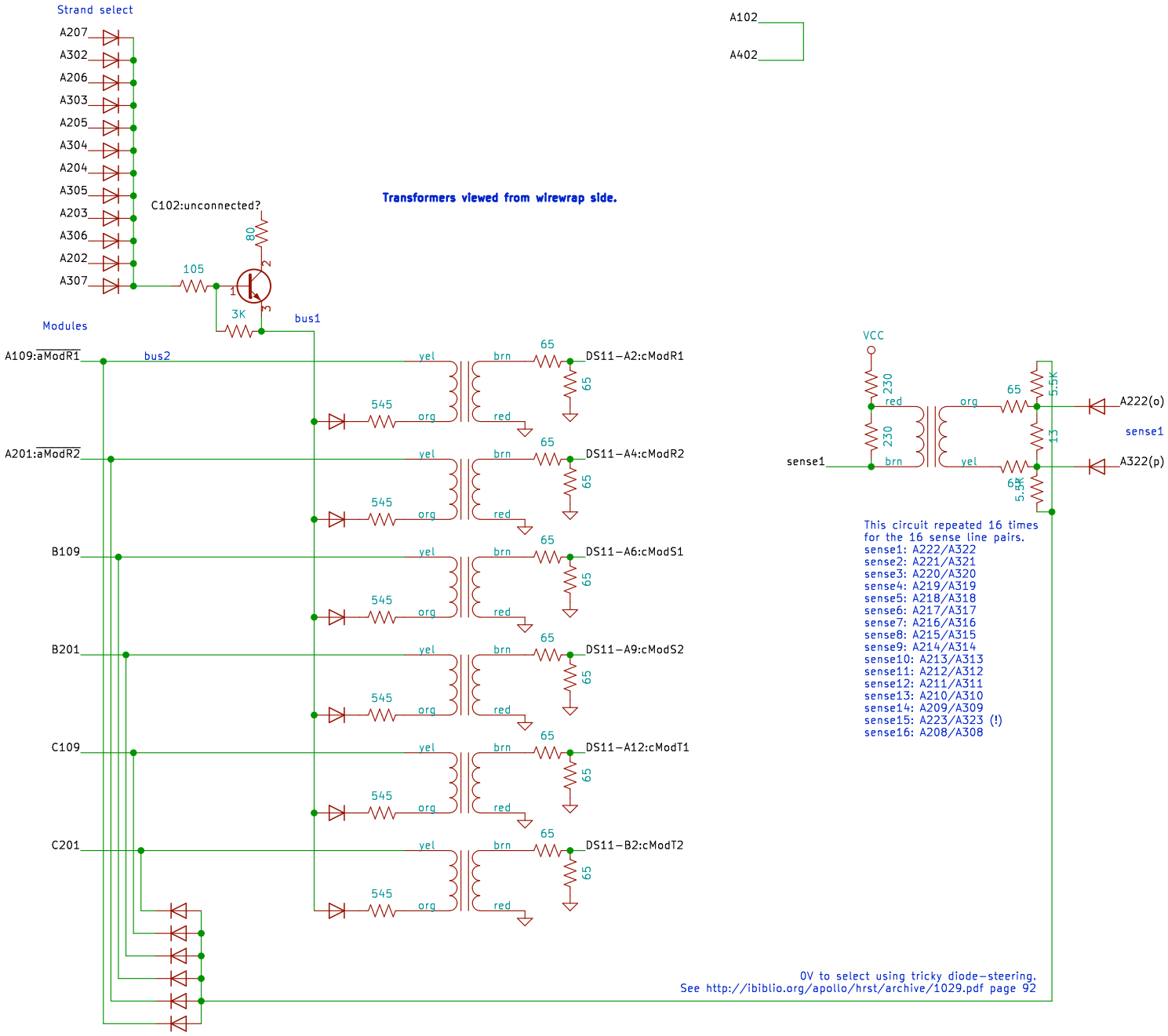
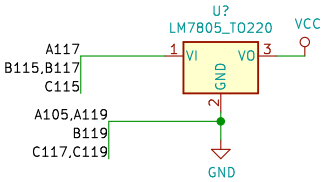
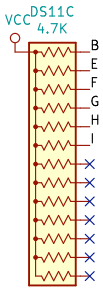
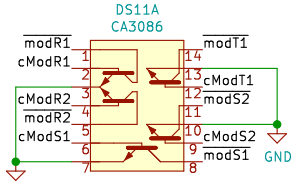
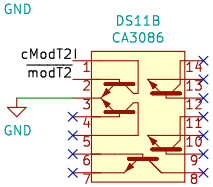
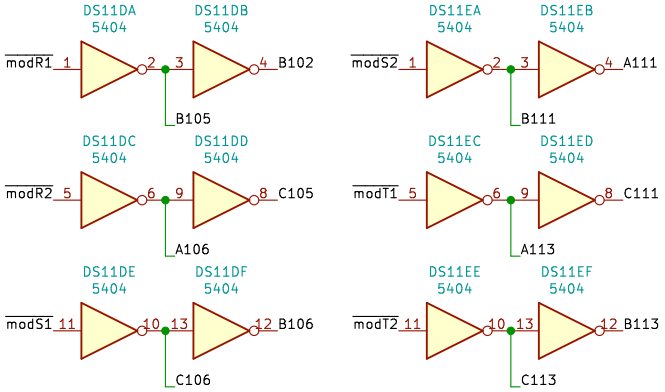
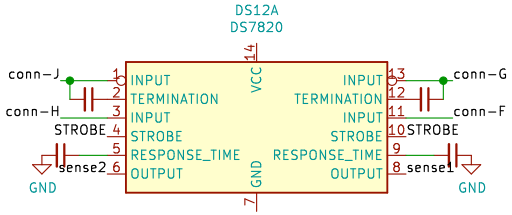
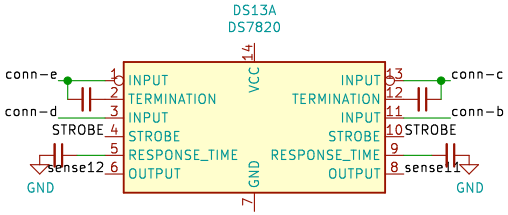
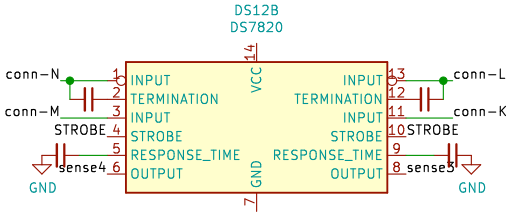
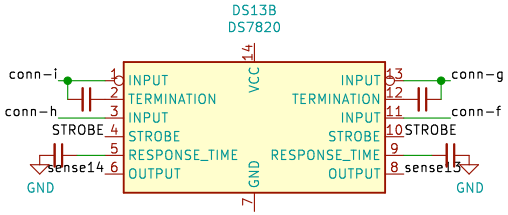
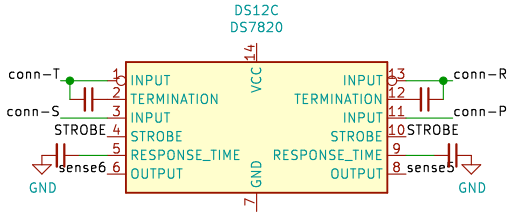
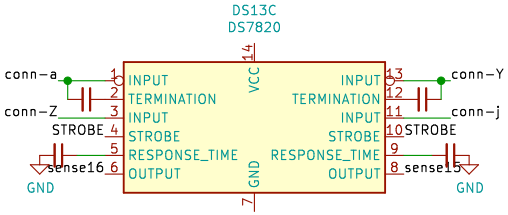
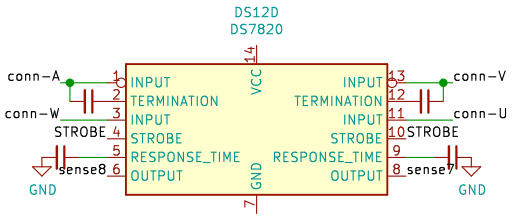
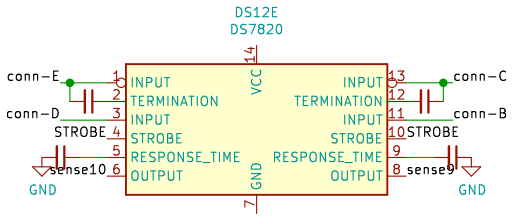
A101 – C424 external contacts have labels rotated 180 degrees inside unit.
Numbers here match AGC numbering, not numbering inside the unit.


DS9E
54121
210ns
DS10A
54121
9.3µs
VCC
13.3K
1nF
OUTPUT_ACTIVE
DS5CD
5400
SetAB
SetCD
ANY_SET
R/Cext
Rint
Cext
A1
A2
B
GND
VCC
Q
DS10B
54121
550ns
DS10C
54121
780ns
390pF
560pF
OUTPUT_ADDR_SET
DS4AB
5410
ANY_STRAND
DS7EB
5404
STR14
DS7EC
5404
STR58
DS7ED
5404
STR912
DS10D
54121
4.2µs
DS10E
54121
2.1µs
6.04K
1nF
150pF
DS7E?E
5404
DS7E?F
5404
A415:SENSE_STROBE
DS7D
54121
210ns
390pF
DS4A?C
5410
Clear
FF_RESET
5.1K
2.2nF


DS3A
4.7K
VCC
IL1
IL2
IL3
IL4
IL5
IL6
IL7
Clear
SetAB
SetCD
ResetA
ResetB
ResetC
DS3B
4.7K
VCC
ResetD
Strand1
Strand2
Strand3
Strand4
Strand5
Strand6
Strand7
Strand8
Strand9
Strand10
Strand11
Strand12
DS2A
CA3086
IL1
cIL1
cIL2
IL2
cIL3
IL5
cIL5
IL4
cIL4
IL3
DS2B
CA3086
IL6
cIL6
cIL7
IL7
cClear
SetCD
cSetCD
SetAB
cSetAB
Clear
DS2C
CA3086
ResetA
cResetA
cResetB
ResetB
cResetC
Strand1
cStrand1
ResetD
cResetD
ResetC
DS2D
CA3086
Strand2
cStrand2
cStrand3
Strand3
cStrand4
Strand6
cStrand6
Strand5
cStrand5
Strand4
DS6E
CA3086
Strand12
cStrand12
DS2E
CA3086
Strand7
cStrand7
cStrand8
Strand8
cStrand9
Strand11
cStrand11
Strand10
cStrand10
Strand9
DS4DA
5404
DS4DB
5404
Strand1
Strand1a
DS4DC
5404
DS4DD
5404
Strand2
Strand2a
DS4DE
5404
DS4DF
5404
Strand3
Strand3a
DS4EA
5404
DS4EB
5404
Strand4
Strand4a
DS4EC
5404
DS4ED
5404
Strand5
Strand5a
DS4EE
5404
DS4EF
5404
Strand6
Strand6a
DS5AA
5404
DS5AB
5404
Strand7
Strand7a
DS5AC
5404
DS5AD
5404
Strand8
Strand8a
DS5AE
5404
DS5AF
5404
Strand9
Strand9a
DS5BA
5404
DS5BB
5404
Strand10
Strand10a
DS5BC
5404
DS5BD
5404
Strand11
Strand11a
DS5BE
5404
DS5BF
5404
Strand12
Strand12a


DS6A
MC4015
DS6B
MC4015
DS6C
MC4015
DS6D
MC4015
DS9A
DS7830
DS9B
DS7830
DS9C
DS7830
DS9D
DS7830
DS8A
DS7830
DS8B
DS7830
DS8C
DS7830
DS8D
DS7830
DS8E
DS7830
VCC
5K
DS5EC
5400
red_wire
0: even parity
1: PLANE7
DS7A
54180
DS7B
54180
DS7CB
5451
DS7EA
5404
FF_RESET
RESET
OUTPUT_ACTIVE
OUTPUT_ADDR_SET
CLEAR
oPLANE7+PARITY


DS3DA
5420
STRAND1a 1
STRAND2a 2
STRAND3a 4
STRAND4a 5
6 STR14(net3)
DS3EA
5420
STRAND5a 1
STRAND6a 2
STRAND7a 4
STRAND8a 5
6 STR58(net2)
DS3DB
5420
STRAND9a 9
STRAND10a 10
STRAND11a 12
STRAND12a 13
8 STR912(net1)
B405 R1
B402 R1
A406 R2
C405 R2
C406 S1
B406 S1
B411 S2
A411 S2
A413 T1
C411 T1
C413 T2
B413 T2
DS1AD
5404
ResetC 9
8 1
DS1AC
5404
SetCD 5
6
13
DS1BA
5451
DS1AB
5404
SetAB 1
2
9
8 PLANE0
DS1AA
5404
ResetA 3
4 10
SetCD PLANE1
DS1CA
5430
STRAND6a 1
STRAND8a 2
STRAND10a 3
STRAND12a 4
VCC
5
6
STRAND2a 11
STRAND4a 12
8 13
DS1AF
5404
12 PLANE2
Bit 0 of strand.
DS1DA
5430
STRAND7a 1
STRAND8a 2
STRAND11a 3
STRAND12a 4
VCC
5
6
STRAND3a 11
STRAND4a 12
8 11
DS1AE
5404
10 PLANE3
Bit 1 of strand.
DS1EA
5410
S1 1
T1 2
R1 13
12
DS1EB
5410
R2 3
S2 4
T2 5
6
DS3CA
5454
STR58 1
13
2
STR912 3
4
STR14 5
9
10
8 PLANE4
GND
DS1EC
5410
R2 9
S1 10
T2 11
8
DS4CA
5454
1
STR14 13
STR912 2
3
STR58 4
5
9
10
8 PLANE5
GND
DS4AA
5410
S2 1
T1 2
R1 13
12
DS4BA
5400
S1 1
S2 2
3
DS4BD
5400
S1 12
STR58 13
11
DS5CC
5400
DS5DA
5430
DS5CA
5400
STR58 9
R2 1
R2 10
STR912 2
3
8
1
2
T1 3
4
5
6
11
12
DS5EB
5400
4
5
8
6 PLANE6
DS4BC
5400
VCC
STR14 9
S1 10
8
DS4BB
5400
T2 4
STR14 5
6
DS3EB
5420
T1 9
S2 10
12
13
8 PLANE7
DS5CB
5400
STR912 4
S1 5
6
DS1BB
5451
STR912 2
T2 3
STR58 4
T2 5
6 PLANE8


Strand select
A207
A302
A206
A303
A205
A304
A204
A305
A203
A306
A202
A307
C102:unconnected?
80
105
3K
bus1
Modules
A109:aModR1
bus2
A201:aModR2
B109
B201
C109
C201
yel
org
brn
red
545
65
DS11−A2:cModR1
DS11−A4:cModR2
DS11−A6:cModS1
DS11−A9:cModS2
DS11−A12:cModT1
DS11−B2:cModT2
Transformers viewed from wirewrap side.
A102
A402
VCC
230
5.5K
13
sense1
A222(o)
A322(p)
This circuit repeated 16 times
for the 16 sense line pairs.
sense1: A222/A322
sense2: A221/A321
sense3: A220/A320
sense4: A219/A319
sense5: A218/A318
sense6: A217/A317
sense7: A216/A316
sense8: A215/A315
sense9: A214/A314
sense10: A213/A313
sense11: A212/A312
sense12: A211/A311
sense13: A210/A310
sense14: A209/A309
sense15: A223/A323 (!)
sense16: A208/A308
0V to select using tricky diode−steering.
See http://ibiblio.org/apollo/hrst/archive/1029.pdf page 92

A115_____SENSE_STROBE