Amendment history of SSD1297 Product Specification

Revision	Description of any change	Issued	Effective
0.10 13-Nov-07	Initial release for product preview Approvers: Q&M Engineering – Kenneth Ho Design Engineering – PC Ke Product Engineering – Joe KW Chan TE – David Wan Marketing – Piony Yeung	CY Ng	20-Nov-07
0.11 24-Jan-08	R01h command update, TB = 0/1 correction on diagram Page 33 & 34 Update Figure 5-1 and 5-3 Application circuit added Package information added Approvers: Q&M Engineering – Kenneth Ho Design Engineering – PC Ke Product Engineering – Joe KW Chan TE – David Wan Marketing – Piony Yeung	CY Ng	25-Jan-08

SSD1297

Product Preview

240 RGB x 320 TFT LCD Controller Driver integrated Power Circuit, Gate and Source Driver with built-in RAM

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TABLES

FIGURES

1. GENERAL DESCRIPTION

SSD1297 is an all in one display driver that integrated the power circuits, source driver and gate driver into a single chip.

SSD1297 can drive a 262K/65K color a-TFT panel with resolution 240 RGB sources X 320 gates.

It also integrated the controller function and consists of 172,800 bytes (240 x 320 x 18 / 8) Graphic Display Data RAM (GDDRAM) such that it interfaced with common MPU through 8/9/16/-bits 6800-series / 8080-series compatible parallel Interface or serial peripheral interface and stored the data in the GDDRAM. Auxiliary 18-/16-/6- bit video interface (VSYNC, HSYNC, DOTCLK, ENABLE) are integrated into SSD1297 for animation image display. SSD1297 is MeSSI-8 or MeSSI-16 in 8080-series interface and ViSSI compatible in 16/18 line parallel RGB interface. LoSSI (3-wire 9bit serial interface) comes along with ViSSI.

SSD1297 embeds a high efficient DC-DC Converter and a Voltage Regulator to generate all necessary voltage level to the a-TFT panel with minimum external components required. The SSD1297 provides a 8-color power saving mode to reduce the energy consumption in portable devices. The sources and gate scan direction can be controlled by software command. An Integrated Gamma Control Circuit is also included that can be selected from 4 preset gamma curves to provide flexibility and optimal display quality.

2. FEATURES

- 240RGBx320 single chip controller driver IC for 262K/65K color amorphous TFT LCD
- Power Supply
  - VDDIO = 1.4V – 3.3V (I/O Interface)
  - VCI = 2.5V – 3.3V (power supply for internal analog circuit)
- Output Voltages
  - Gate Driver:
    - VGH-GND = 9V ~ 18V
    - VGL-GND = -6 ~ -15V
    - VGH-VGL = 32Vp-p
  - Source Driver:
    - V0 – V63 = 5.5V
    - Typical Source Output Voltage variation: ±10 mV
  - VCOM drive:
    - VCOMH = 3.0V ~ 5.0V
    - VCOML = -1.0V ~ -3.0V
    - VCOM amplitude = 5.5V
- System Interface
  - High-speed interface by 8-/9-/16-bit 6800-series / 8080-series parallel ports
  - Serial Peripheral Interface (SPI)
  - MeSSI-8 or MeSSI-16 interface in 8080 mode specified in **DMIF-S50AP-K124**.
  - LoSSI (3-wire 9bit serial interface) and ViSSI (16 or 18 line RGB interface) specified in **DMIF-S50AP-P01**.
  - VSYNC interface (system interface + VSYNC)
  - WSYNC interface (system interface + WSYNC)
- Support low power consumption
  - Low voltage supply
  - Low current sleep mode
  - 8-color display mode
  - Charge sharing function for step-up circuits
- High-speed RAM addressing functions
  - RAM write synchronization function
  - Window address function
  - Vertical scrolling function
  - Partial display mode
- Internal power supply circuit
  - Voltage generator
  - DC-DC converter up to 6x/-5x
- Built-in internal oscillator
- Internal GDDRAM capacity: 172,800 bytes (240x320x18/8)
- Support Frame and Line inversion AC drive
- TFT storage capacitance: Cs on common
- Support source and gate scan direction control
- Programmable Gamma Correction Curve
- 4 Preset gamma correction curve
- Tearing Effect Line Mode
- Built-in Non Volatile Memory for VCOM calibration and manufacturing ID
- Command status read function

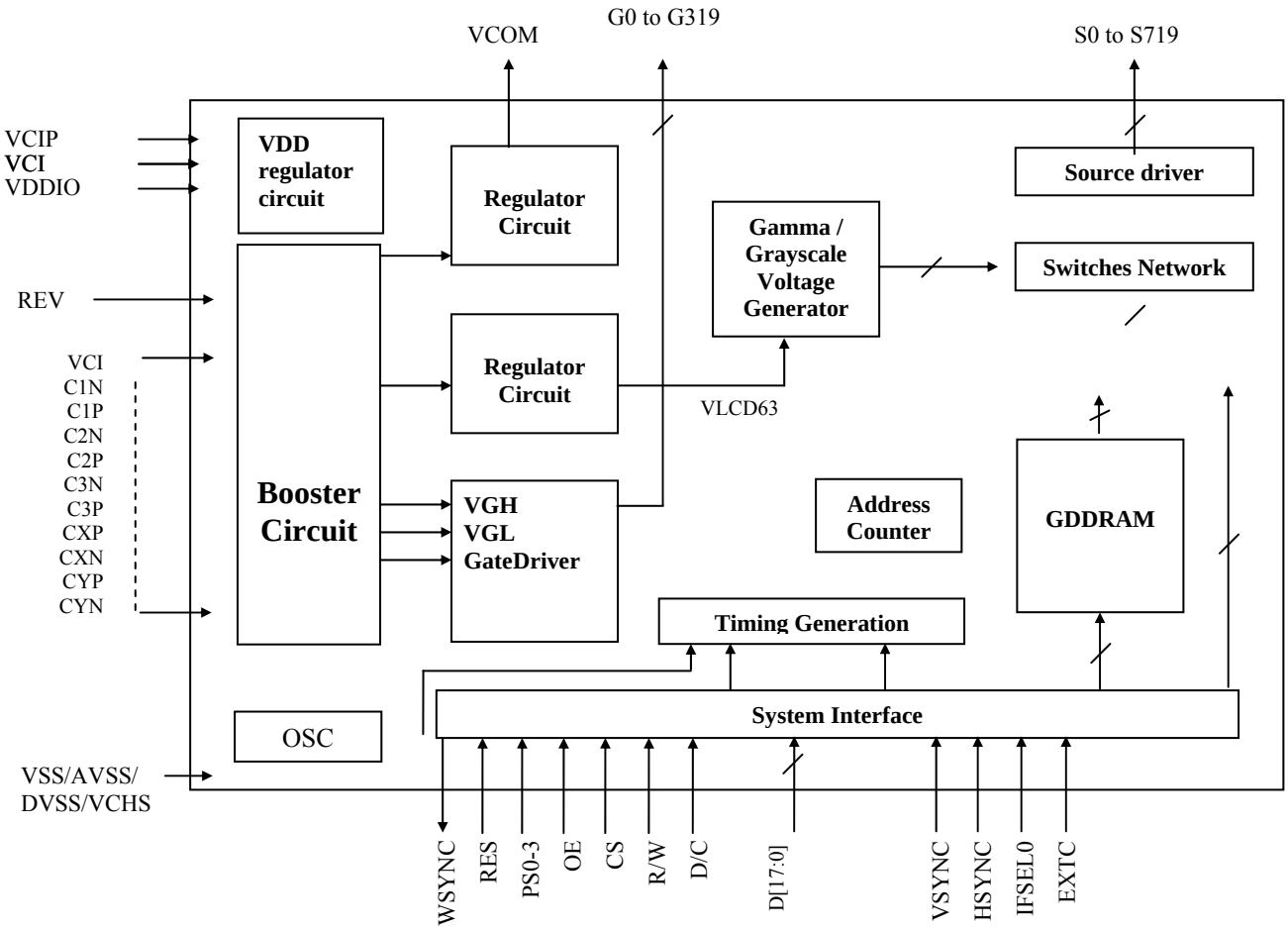
3. ORDERING INFORMATION

Table 3-1 Ordering Information

Ordering Part Number	Source	Gate	Package Form	Reference	Remark
SSD1297Z	240 x 3 (720)	320	Gold Bump Die		

4. BLOCK DIAGRAM

Figure 4-1 SSD1297 Block Diagram Description



5. DIE PAD FLOOR PLAN

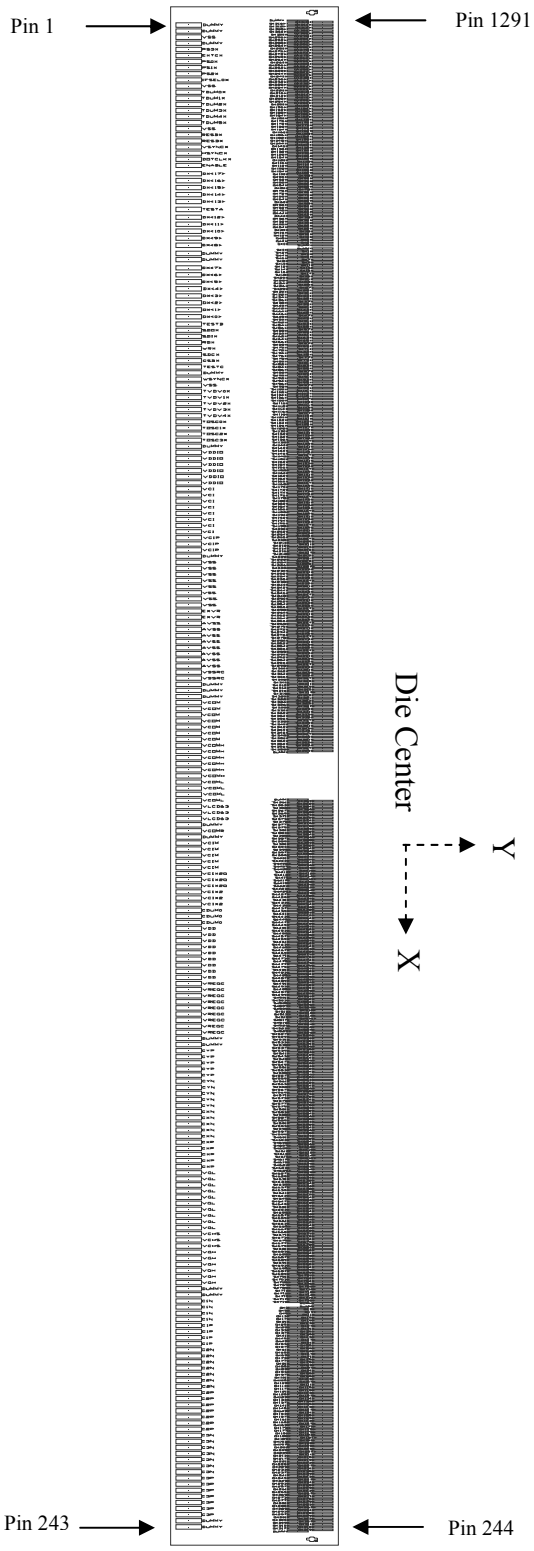


Figure 5-3 SSD1297Pad Arrangement (Bump face up)

Note

(1) Diagram showing the die face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold

Figure 5-1 Alignment Marks

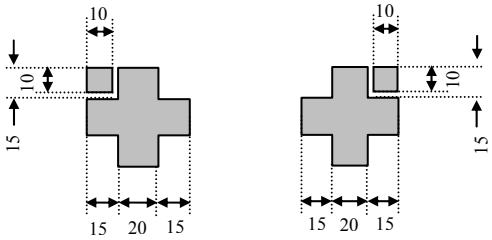


Figure 5-2 Output Pad Pitch

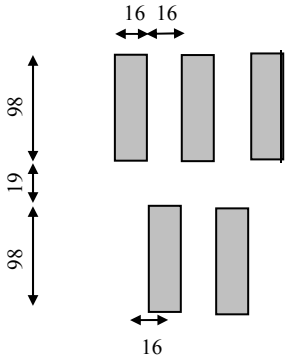


Table 5-1 Die Information

Die Size (no scribe)	17640 x 785 (in the range of 800-880) um^2
Die Thickness	300 ± 25 um
Typical Bump Height	15 um
Bump Co-planarity (within die)	≤ 2 um
Bump Size 1	50 x 120 μm^2 (Pin 1 – 243)
Pad Pitch 1	70 µm
Bump Size 2	16 x 98 μm^2 (Pin 244 – 1291)
Pad Pitch 2	16 µm stagger

Table 5-2 SSD1297 Bump Pad Coordinate (Bump Center)

Note: IC material temperature expansion factor is 2.6ppm, customer should take into account during panel design

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
1	DUMMY	-8610	-307.5	51	SDC	-4830	-307.5	101	AVSS	-1330	-307.5
2	DUMMY	-8540	-307.5	52	CSBX	-4760	-307.5	102	AVSS	-1260	-307.5
3	VSS	-8470	-307.5	53	TESTC	-4690	-307.5	103	VSSRC	-1190	-307.5
4	DUMMY	-8400	-307.5	54	DUMMY	-4620	-307.5	104	VSSRC	-1120	-307.5
5	PS3X	-8330	-307.5	55	WSYNCX	-4550	-307.5	105	DUMMY	-1050	-307.5
6	EXTCX	-8260	-307.5	56	VSS	-4480	-307.5	106	DUMMY	-980	-307.5
7	PS0X	-8190	-307.5	57	TVDV0X	-4410	-307.5	107	DUMMY	-910	-307.5
8	PS1X	-8120	-307.5	58	TVDV1X	-4340	-307.5	108	VCOM	-840	-307.5
9	PS2X	-8050	-307.5	59	TVDV2X	-4270	-307.5	109	VCOM	-770	-307.5
10	IFSEL0X	-7980	-307.5	60	TVDV3X	-4200	-307.5	110	VCOM	-700	-307.5
11	VSS	-7910	-307.5	61	TVDV4X	-4130	-307.5	111	VCOM	-630	-307.5
12	TDUM0X	-7840	-307.5	62	TOSC0X	-4060	-307.5	112	VCOM	-560	-307.5
13	TDUM1X	-7770	-307.5	63	TOSC1X	-3990	-307.5	113	VCOM	-490	-307.5
14	TDUM2X	-7700	-307.5	64	TOSC2X	-3920	-307.5	114	VCOM	-420	-307.5
15	TDUM3X	-7630	-307.5	65	TOSC3X	-3850	-307.5	115	VCOMH	-350	-307.5
16	TDUM4X	-7560	-307.5	66	DUMMY	-3780	-307.5	116	VCOMH	-280	-307.5
17	TDUM5X	-7490	-307.5	67	VDDIO	-3710	-307.5	117	VCOMH	-210	-307.5
18	VSS	-7420	-307.5	68	VDDIO	-3640	-307.5	118	VCOMH	-140	-307.5
19	RESBX	-7350	-307.5	69	VDDIO	-3570	-307.5	119	VCOMH	-70	-307.5
20	RESBX	-7280	-307.5	70	VDDIO	-3500	-307.5	120	VCOMH	0	-307.5
21	VSYNCX	-7210	-307.5	71	VDDIO	-3430	-307.5	121	VCOML	70	-307.5
22	HSYNCX	-7140	-307.5	72	VDDIO	-3360	-307.5	122	VCOML	140	-307.5
23	DOTCLKX	-7070	-307.5	73	VCI	-3290	-307.5	123	VCOML	210	-307.5
24	ENABLE	-7000	-307.5	74	VCI	-3220	-307.5	124	VCOML	280	-307.5
25	DX<17>	-6905	-307.5	75	VCI	-3150	-307.5	125	VLCD63	350	-307.5
26	DX<16>	-6825	-307.5	76	VCI	-3080	-307.5	126	VLCD63	420	-307.5
27	DX<15>	-6745	-307.5	77	VCI	-3010	-307.5	127	VLCD63	490	-307.5
28	DX<14>	-6665	-307.5	78	VCI	-2940	-307.5	128	DUMMY	560	-307.5
29	DX<13>	-6585	-307.5	79	VCI	-2870	-307.5	129	VCOMR	630	-307.5
30	TESTA	-6495	-307.5	80	VCI	-2800	-307.5	130	DUMMY	700	-307.5
31	DX<12>	-6405	-307.5	81	VCIP	-2730	-307.5	131	VCIM	770	-307.5
32	DX<11>	-6325	-307.5	82	VCIP	-2660	-307.5	132	VCIM	840	-307.5
33	DX<10>	-6245	-307.5	83	VCIP	-2590	-307.5	133	VCIM	910	-307.5
34	DX<9>	-6165	-307.5	84	DUMMY	-2520	-307.5	134	VCIM	980	-307.5
35	DX<8>	-6085	-307.5	85	VSS	-2450	-307.5	135	VCIM	1050	-307.5
36	DUMMY	-5990	-307.5	86	VSS	-2380	-307.5	136	VCIX2G	1120	-307.5
37	DUMMY	-5920	-307.5	87	VSS	-2310	-307.5	137	VCIX2G	1190	-307.5
38	DX<7>	-5825	-307.5	88	VSS	-2240	-307.5	138	VCIX2G	1260	-307.5
39	DX<6>	-5745	-307.5	89	VSS	-2170	-307.5	139	VCIX2	1330	-307.5
40	DX<5>	-5665	-307.5	90	VSS	-2100	-307.5	140	VCIX2	1400	-307.5
41	DX<4>	-5585	-307.5	91	VSS	-2030	-307.5	141	VCIX2	1470	-307.5
42	DX<3>	-5505	-307.5	92	VSS	-1960	-307.5	142	CDUM0	1540	-307.5
43	DX<2>	-5425	-307.5	93	EXVR	-1890	-307.5	143	CDUM0	1610	-307.5
44	DX<1>	-5345	-307.5	94	EXVR	-1820	-307.5	144	CDUM0	1680	-307.5
45	DX<0>	-5265	-307.5	95	AVSS	-1750	-307.5	145	VDD	1750	-307.5
46	TESTB	-5180	-307.5	96	AVSS	-1680	-307.5	146	VDD	1820	-307.5
47	SDOX	-5110	-307.5	97	AVSS	-1610	-307.5	147	VDD	1890	-307.5
48	SDIX	-5040	-307.5	98	AVSS	-1540	-307.5	148	VDD	1960	-307.5
49	RDX	-4970	-307.5	99	AVSS	-1470	-307.5	149	VDD	2030	-307.5
50	WRX	-4900	-307.5	100	AVSS	-1400	-307.5	150	VDD	2100	-307.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
151	VDD	2170	-307.5	201	VGH	5670	-307.5	251	G<307>	8547	319.5
152	VDD	2240	-307.5	202	VGH	5740	-307.5	252	G<305>	8531	202.5
153	VDD	2310	-307.5	203	VGH	5810	-307.5	253	G<303>	8515	319.5
154	VREGC	2380	-307.5	204	DUMMY	5880	-307.5	254	G<301>	8499	202.5
155	VREGC	2450	-307.5	205	DUMMY	5950	-307.5	255	G<299>	8483	319.5
156	VREGC	2520	-307.5	206	C1N	6020	-307.5	256	G<297>	8467	202.5
157	VREGC	2590	-307.5	207	C1N	6090	-307.5	257	G<295>	8451	319.5
158	VREGC	2660	-307.5	208	C1N	6160	-307.5	258	G<293>	8435	202.5
159	VREGC	2730	-307.5	209	C1N	6230	-307.5	259	G<291>	8419	319.5
160	VREGC	2800	-307.5	210	C1P	6300	-307.5	260	G<289>	8403	202.5
161	VREGC	2870	-307.5	211	C1P	6370	-307.5	261	G<287>	8387	319.5
162	VREGC	2940	-307.5	212	C1P	6440	-307.5	262	G<285>	8371	202.5
163	DUMMY	3010	-307.5	213	C1P	6510	-307.5	263	G<283>	8355	319.5
164	DUMMY	3080	-307.5	214	C2N	6580	-307.5	264	G<281>	8339	202.5
165	CYP	3150	-307.5	215	C2N	6650	-307.5	265	G<279>	8323	319.5
166	CYP	3220	-307.5	216	C2N	6720	-307.5	266	G<277>	8307	202.5
167	CYP	3290	-307.5	217	C2N	6790	-307.5	267	G<275>	8291	319.5
168	CYP	3360	-307.5	218	C2N	6860	-307.5	268	G<273>	8275	202.5
169	CYP	3430	-307.5	219	C2N	6930	-307.5	269	G<271>	8259	319.5
170	CYN	3500	-307.5	220	C2N	7000	-307.5	270	G<269>	8243	202.5
171	CYN	3570	-307.5	221	C2P	7070	-307.5	271	G<267>	8227	319.5
172	CYN	3640	-307.5	222	C2P	7140	-307.5	272	G<265>	8211	202.5
173	CYN	3710	-307.5	223	C2P	7210	-307.5	273	G<263>	8195	319.5
174	CYN	3780	-307.5	224	C2P	7280	-307.5	274	G<261>	8179	202.5
175	CXN	3850	-307.5	225	C2P	7350	-307.5	275	G<259>	8163	319.5
176	CXN	3920	-307.5	226	C2P	7420	-307.5	276	G<257>	8147	202.5
177	CXN	3990	-307.5	227	C2P	7490	-307.5	277	G<255>	8131	319.5
178	CXN	4060	-307.5	228	C3N	7560	-307.5	278	G<253>	8115	202.5
179	CXN	4130	-307.5	229	C3N	7630	-307.5	279	G<251>	8099	319.5
180	CXP	4200	-307.5	230	C3N	7700	-307.5	280	G<249>	8083	202.5
181	CXP	4270	-307.5	231	C3N	7770	-307.5	281	G<247>	8067	319.5
182	CXP	4340	-307.5	232	C3N	7840	-307.5	282	G<245>	8051	202.5
183	CXP	4410	-307.5	233	C3N	7910	-307.5	283	G<243>	8035	319.5
184	CXP	4480	-307.5	234	C3N	7980	-307.5	284	G<241>	8019	202.5
185	VGL	4550	-307.5	235	C3P	8050	-307.5	285	G<239>	8003	319.5
186	VGL	4620	-307.5	236	C3P	8120	-307.5	286	G<237>	7987	202.5
187	VGL	4690	-307.5	237	C3P	8190	-307.5	287	G<235>	7971	319.5
188	VGL	4760	-307.5	238	C3P	8260	-307.5	288	G<233>	7955	202.5
189	VGL	4830	-307.5	239	C3P	8330	-307.5	289	G<231>	7939	319.5
190	VGL	4900	-307.5	240	C3P	8400	-307.5	290	G<229>	7923	202.5
191	VGL	4970	-307.5	241	C3P	8470	-307.5	291	G<227>	7907	319.5
192	VGL	5040	-307.5	242	DUMMY	8540	-307.5	292	G<225>	7891	202.5
193	VGL	5110	-307.5	243	DUMMY	8610	-307.5	293	G<223>	7875	319.5
194	VGL	5180	-307.5	244	DUMMY	8659	202.5	294	G<221>	7859	202.5
195	VCHS	5250	-307.5	245	G<319>	8643	319.5	295	G<219>	7843	319.5
196	VCHS	5320	-307.5	246	G<317>	8627	202.5	296	G<217>	7827	202.5
197	VCHS	5390	-307.5	247	G<315>	8611	319.5	297	G<215>	7811	319.5
198	VGH	5460	-307.5	248	G<313>	8595	202.5	298	G<213>	7795	202.5
199	VGH	5530	-307.5	249	G<311>	8579	319.5	299	G<211>	7779	319.5
200	VGH	5600	-307.5	250	G<309>	8563	202.5	300	G<209>	7763	202.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
301	G<207>	7747	319.5	351	G<107>	6947	319.5	401	G<7>	6147	319.5
302	G<205>	7731	202.5	352	G<105>	6931	202.5	402	G<5>	6131	202.5
303	G<203>	7715	319.5	353	G<103>	6915	319.5	403	G<3>	6115	319.5
304	G<201>	7699	202.5	354	G<101>	6899	202.5	404	G<1>	6099	202.5
305	G<199>	7683	319.5	355	G<99>	6883	319.5	405	DUMMY	6083	319.5
306	G<197>	7667	202.5	356	G<97>	6867	202.5	406	DUMMY	6047	319.5
307	G<195>	7651	319.5	357	G<95>	6851	319.5	407	S<719>	6031	202.5
308	G<193>	7635	202.5	358	G<93>	6835	202.5	408	S<718>	6015	319.5
309	G<191>	7619	319.5	359	G<91>	6819	319.5	409	S<717>	5999	202.5
310	G<189>	7603	202.5	360	G<89>	6803	202.5	410	S<716>	5983	319.5
311	G<187>	7587	319.5	361	G<87>	6787	319.5	411	S<715>	5967	202.5
312	G<185>	7571	202.5	362	G<85>	6771	202.5	412	S<714>	5951	319.5
313	G<183>	7555	319.5	363	G<83>	6755	319.5	413	S<713>	5935	202.5
314	G<181>	7539	202.5	364	G<81>	6739	202.5	414	S<712>	5919	319.5
315	G<179>	7523	319.5	365	G<79>	6723	319.5	415	S<711>	5903	202.5
316	G<177>	7507	202.5	366	G<77>	6707	202.5	416	S<710>	5887	319.5
317	G<175>	7491	319.5	367	G<75>	6691	319.5	417	S<709>	5871	202.5
318	G<173>	7475	202.5	368	G<73>	6675	202.5	418	S<708>	5855	319.5
319	G<171>	7459	319.5	369	G<71>	6659	319.5	419	S<707>	5839	202.5
320	G<169>	7443	202.5	370	G<69>	6643	202.5	420	S<706>	5823	319.5
321	G<167>	7427	319.5	371	G<67>	6627	319.5	421	S<705>	5807	202.5
322	G<165>	7411	202.5	372	G<65>	6611	202.5	422	S<704>	5791	319.5
323	G<163>	7395	319.5	373	G<63>	6595	319.5	423	S<703>	5775	202.5
324	G<161>	7379	202.5	374	G<61>	6579	202.5	424	S<702>	5759	319.5
325	G<159>	7363	319.5	375	G<59>	6563	319.5	425	S<701>	5743	202.5
326	G<157>	7347	202.5	376	G<57>	6547	202.5	426	S<700>	5727	319.5
327	G<155>	7331	319.5	377	G<55>	6531	319.5	427	S<699>	5711	202.5
328	G<153>	7315	202.5	378	G<53>	6515	202.5	428	S<698>	5695	319.5
329	G<151>	7299	319.5	379	G<51>	6499	319.5	429	S<697>	5679	202.5
330	G<149>	7283	202.5	380	G<49>	6483	202.5	430	S<696>	5663	319.5
331	G<147>	7267	319.5	381	G<47>	6467	319.5	431	S<695>	5647	202.5
332	G<145>	7251	202.5	382	G<45>	6451	202.5	432	S<694>	5631	319.5
333	G<143>	7235	319.5	383	G<43>	6435	319.5	433	S<693>	5615	202.5
334	G<141>	7219	202.5	384	G<41>	6419	202.5	434	S<692>	5599	319.5
335	G<139>	7203	319.5	385	G<39>	6403	319.5	435	S<691>	5583	202.5
336	G<137>	7187	202.5	386	G<37>	6387	202.5	436	S<690>	5567	319.5
337	G<135>	7171	319.5	387	G<35>	6371	319.5	437	S<689>	5551	202.5
338	G<133>	7155	202.5	388	G<33>	6355	202.5	438	S<688>	5535	319.5
339	G<131>	7139	319.5	389	G<31>	6339	319.5	439	S<687>	5519	202.5
340	G<129>	7123	202.5	390	G<29>	6323	202.5	440	S<686>	5503	319.5
341	G<127>	7107	319.5	391	G<27>	6307	319.5	441	S<685>	5487	202.5
342	G<125>	7091	202.5	392	G<25>	6291	202.5	442	S<684>	5471	319.5
343	G<123>	7075	319.5	393	G<23>	6275	319.5	443	S<683>	5455	202.5
344	G<121>	7059	202.5	394	G<21>	6259	202.5	444	S<682>	5439	319.5
345	G<119>	7043	319.5	395	G<19>	6243	319.5	445	S<681>	5423	202.5
346	G<117>	7027	202.5	396	G<17>	6227	202.5	446	S<680>	5407	319.5
347	G<115>	7011	319.5	397	G<15>	6211	319.5	447	S<679>	5391	202.5
348	G<113>	6995	202.5	398	G<13>	6195	202.5	448	S<678>	5375	319.5
349	G<111>	6979	319.5	399	G<11>	6179	319.5	449	S<677>	5359	202.5
350	G<109>	6963	202.5	400	G<9>	6163	202.5	450	S<676>	5343	319.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
451	S<675>	5327	202.5	501	S<625>	4527	202.5	551	S<575>	3727	202.5
452	S<674>	5311	319.5	502	S<624>	4511	319.5	552	S<574>	3711	319.5
453	S<673>	5295	202.5	503	S<623>	4495	202.5	553	S<573>	3695	202.5
454	S<672>	5279	319.5	504	S<622>	4479	319.5	554	S<572>	3679	319.5
455	S<671>	5263	202.5	505	S<621>	4463	202.5	555	S<571>	3663	202.5
456	S<670>	5247	319.5	506	S<620>	4447	319.5	556	S<570>	3647	319.5
457	S<669>	5231	202.5	507	S<619>	4431	202.5	557	S<569>	3631	202.5
458	S<668>	5215	319.5	508	S<618>	4415	319.5	558	S<568>	3615	319.5
459	S<667>	5199	202.5	509	S<617>	4399	202.5	559	S<567>	3599	202.5
460	S<666>	5183	319.5	510	S<616>	4383	319.5	560	S<566>	3583	319.5
461	S<665>	5167	202.5	511	S<615>	4367	202.5	561	S<565>	3567	202.5
462	S<664>	5151	319.5	512	S<614>	4351	319.5	562	S<564>	3551	319.5
463	S<663>	5135	202.5	513	S<613>	4335	202.5	563	S<563>	3535	202.5
464	S<662>	5119	319.5	514	S<612>	4319	319.5	564	S<562>	3519	319.5
465	S<661>	5103	202.5	515	S<611>	4303	202.5	565	S<561>	3503	202.5
466	S<660>	5087	319.5	516	S<610>	4287	319.5	566	S<560>	3487	319.5
467	S<659>	5071	202.5	517	S<609>	4271	202.5	567	S<559>	3471	202.5
468	S<658>	5055	319.5	518	S<608>	4255	319.5	568	S<558>	3455	319.5
469	S<657>	5039	202.5	519	S<607>	4239	202.5	569	S<557>	3439	202.5
470	S<656>	5023	319.5	520	S<606>	4223	319.5	570	S<556>	3423	319.5
471	S<655>	5007	202.5	521	S<605>	4207	202.5	571	S<555>	3407	202.5
472	S<654>	4991	319.5	522	S<604>	4191	319.5	572	S<554>	3391	319.5
473	S<653>	4975	202.5	523	S<603>	4175	202.5	573	S<553>	3375	202.5
474	S<652>	4959	319.5	524	S<602>	4159	319.5	574	S<552>	3359	319.5
475	S<651>	4943	202.5	525	S<601>	4143	202.5	575	S<551>	3343	202.5
476	S<650>	4927	319.5	526	S<600>	4127	319.5	576	S<550>	3327	319.5
477	S<649>	4911	202.5	527	S<599>	4111	202.5	577	S<549>	3311	202.5
478	S<648>	4895	319.5	528	S<598>	4095	319.5	578	S<548>	3295	319.5
479	S<647>	4879	202.5	529	S<597>	4079	202.5	579	S<547>	3279	202.5
480	S<646>	4863	319.5	530	S<596>	4063	319.5	580	S<546>	3263	319.5
481	S<645>	4847	202.5	531	S<595>	4047	202.5	581	S<545>	3247	202.5
482	S<644>	4831	319.5	532	S<594>	4031	319.5	582	S<544>	3231	319.5
483	S<643>	4815	202.5	533	S<593>	4015	202.5	583	S<543>	3215	202.5
484	S<642>	4799	319.5	534	S<592>	3999	319.5	584	S<542>	3199	319.5
485	S<641>	4783	202.5	535	S<591>	3983	202.5	585	S<541>	3183	202.5
486	S<640>	4767	319.5	536	S<590>	3967	319.5	586	S<540>	3167	319.5
487	S<639>	4751	202.5	537	S<589>	3951	202.5	587	S<539>	3151	202.5
488	S<638>	4735	319.5	538	S<588>	3935	319.5	588	S<538>	3135	319.5
489	S<637>	4719	202.5	539	S<587>	3919	202.5	589	S<537>	3119	202.5
490	S<636>	4703	319.5	540	S<586>	3903	319.5	590	S<536>	3103	319.5
491	S<635>	4687	202.5	541	S<585>	3887	202.5	591	S<535>	3087	202.5
492	S<634>	4671	319.5	542	S<584>	3871	319.5	592	S<534>	3071	319.5
493	S<633>	4655	202.5	543	S<583>	3855	202.5	593	S<533>	3055	202.5
494	S<632>	4639	319.5	544	S<582>	3839	319.5	594	S<532>	3039	319.5
495	S<631>	4623	202.5	545	S<581>	3823	202.5	595	S<531>	3023	202.5
496	S<630>	4607	319.5	546	S<580>	3807	319.5	596	S<530>	3007	319.5
497	S<629>	4591	202.5	547	S<579>	3791	202.5	597	S<529>	2991	202.5
498	S<628>	4575	319.5	548	S<578>	3775	319.5	598	S<528>	2975	319.5
499	S<627>	4559	202.5	549	S<577>	3759	202.5	599	S<527>	2959	202.5
500	S<626>	4543	319.5	550	S<576>	3743	319.5	600	S<526>	2943	319.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
601	S<525>	2927	202.5	651	S<475>	2127	202.5	701	S<425>	1327	202.5
602	S<524>	2911	319.5	652	S<474>	2111	319.5	702	S<424>	1311	319.5
603	S<523>	2895	202.5	653	S<473>	2095	202.5	703	S<423>	1295	202.5
604	S<522>	2879	319.5	654	S<472>	2079	319.5	704	S<422>	1279	319.5
605	S<521>	2863	202.5	655	S<471>	2063	202.5	705	S<421>	1263	202.5
606	S<520>	2847	319.5	656	S<470>	2047	319.5	706	S<420>	1247	319.5
607	S<519>	2831	202.5	657	S<469>	2031	202.5	707	S<419>	1231	202.5
608	S<518>	2815	319.5	658	S<468>	2015	319.5	708	S<418>	1215	319.5
609	S<517>	2799	202.5	659	S<467>	1999	202.5	709	S<417>	1199	202.5
610	S<516>	2783	319.5	660	S<466>	1983	319.5	710	S<416>	1183	319.5
611	S<515>	2767	202.5	661	S<465>	1967	202.5	711	S<415>	1167	202.5
612	S<514>	2751	319.5	662	S<464>	1951	319.5	712	S<414>	1151	319.5
613	S<513>	2735	202.5	663	S<463>	1935	202.5	713	S<413>	1135	202.5
614	S<512>	2719	319.5	664	S<462>	1919	319.5	714	S<412>	1119	319.5
615	S<511>	2703	202.5	665	S<461>	1903	202.5	715	S<411>	1103	202.5
616	S<510>	2687	319.5	666	S<460>	1887	319.5	716	S<410>	1087	319.5
617	S<509>	2671	202.5	667	S<459>	1871	202.5	717	S<409>	1071	202.5
618	S<508>	2655	319.5	668	S<458>	1855	319.5	718	S<408>	1055	319.5
619	S<507>	2639	202.5	669	S<457>	1839	202.5	719	S<407>	1039	202.5
620	S<506>	2623	319.5	670	S<456>	1823	319.5	720	S<406>	1023	319.5
621	S<505>	2607	202.5	671	S<455>	1807	202.5	721	S<405>	1007	202.5
622	S<504>	2591	319.5	672	S<454>	1791	319.5	722	S<404>	991	319.5
623	S<503>	2575	202.5	673	S<453>	1775	202.5	723	S<403>	975	202.5
624	S<502>	2559	319.5	674	S<452>	1759	319.5	724	S<402>	959	319.5
625	S<501>	2543	202.5	675	S<451>	1743	202.5	725	S<401>	943	202.5
626	S<500>	2527	319.5	676	S<450>	1727	319.5	726	S<400>	927	319.5
627	S<499>	2511	202.5	677	S<449>	1711	202.5	727	S<399>	911	202.5
628	S<498>	2495	319.5	678	S<448>	1695	319.5	728	S<398>	895	319.5
629	S<497>	2479	202.5	679	S<447>	1679	202.5	729	S<397>	879	202.5
630	S<496>	2463	319.5	680	S<446>	1663	319.5	730	S<396>	863	319.5
631	S<495>	2447	202.5	681	S<445>	1647	202.5	731	S<395>	847	202.5
632	S<494>	2431	319.5	682	S<444>	1631	319.5	732	S<394>	831	319.5
633	S<493>	2415	202.5	683	S<443>	1615	202.5	733	S<393>	815	202.5
634	S<492>	2399	319.5	684	S<442>	1599	319.5	734	S<392>	799	319.5
635	S<491>	2383	202.5	685	S<441>	1583	202.5	735	S<391>	783	202.5
636	S<490>	2367	319.5	686	S<440>	1567	319.5	736	S<390>	767	319.5
637	S<489>	2351	202.5	687	S<439>	1551	202.5	737	S<389>	751	202.5
638	S<488>	2335	319.5	688	S<438>	1535	319.5	738	S<388>	735	319.5
639	S<487>	2319	202.5	689	S<437>	1519	202.5	739	S<387>	719	202.5
640	S<486>	2303	319.5	690	S<436>	1503	319.5	740	S<386>	703	319.5
641	S<485>	2287	202.5	691	S<435>	1487	202.5	741	S<385>	687	202.5
642	S<484>	2271	319.5	692	S<434>	1471	319.5	742	S<384>	671	319.5
643	S<483>	2255	202.5	693	S<433>	1455	202.5	743	S<383>	655	202.5
644	S<482>	2239	319.5	694	S<432>	1439	319.5	744	S<382>	639	319.5
645	S<481>	2223	202.5	695	S<431>	1423	202.5	745	S<381>	623	202.5
646	S<480>	2207	319.5	696	S<430>	1407	319.5	746	S<380>	607	319.5
647	S<479>	2191	202.5	697	S<429>	1391	202.5	747	S<379>	591	202.5
648	S<478>	2175	319.5	698	S<428>	1375	319.5	748	S<378>	575	319.5
649	S<477>	2159	202.5	699	S<427>	1359	202.5	749	S<377>	559	202.5
650	S<476>	2143	319.5	700	S<426>	1343	319.5	750	S<376>	543	319.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
751	S<375>	527	202.5	801	S<327>	-799	319.5	851	S<277>	-1599	319.5
752	S<374>	511	319.5	802	S<326>	-815	202.5	852	S<276>	-1615	202.5
753	S<373>	495	202.5	803	S<325>	-831	319.5	853	S<275>	-1631	319.5
754	S<372>	479	319.5	804	S<324>	-847	202.5	854	S<274>	-1647	202.5
755	S<371>	463	202.5	805	S<323>	-863	319.5	855	S<273>	-1663	319.5
756	S<370>	447	319.5	806	S<322>	-879	202.5	856	S<272>	-1679	202.5
757	S<369>	431	202.5	807	S<321>	-895	319.5	857	S<271>	-1695	319.5
758	S<368>	415	319.5	808	S<320>	-911	202.5	858	S<270>	-1711	202.5
759	S<367>	399	202.5	809	S<319>	-927	319.5	859	S<269>	-1727	319.5
760	S<366>	383	319.5	810	S<318>	-943	202.5	860	S<268>	-1743	202.5
761	S<365>	367	202.5	811	S<317>	-959	319.5	861	S<267>	-1759	319.5
762	S<364>	351	319.5	812	S<316>	-975	202.5	862	S<266>	-1775	202.5
763	S<363>	335	202.5	813	S<315>	-991	319.5	863	S<265>	-1791	319.5
764	S<362>	319	319.5	814	S<314>	-1007	202.5	864	S<264>	-1807	202.5
765	S<361>	303	202.5	815	S<313>	-1023	319.5	865	S<263>	-1823	319.5
766	S<360>	287	319.5	816	S<312>	-1039	202.5	866	S<262>	-1839	202.5
767	DUMMY	271	202.5	817	S<311>	-1055	319.5	867	S<261>	-1855	319.5
768	DUMMY	-271	202.5	818	S<310>	-1071	202.5	868	S<260>	-1871	202.5
769	S<359>	-287	319.5	819	S<309>	-1087	319.5	869	S<259>	-1887	319.5
770	S<358>	-303	202.5	820	S<308>	-1103	202.5	870	S<258>	-1903	202.5
771	S<357>	-319	319.5	821	S<307>	-1119	319.5	871	S<257>	-1919	319.5
772	S<356>	-335	202.5	822	S<306>	-1135	202.5	872	S<256>	-1935	202.5
773	S<355>	-351	319.5	823	S<305>	-1151	319.5	873	S<255>	-1951	319.5
774	S<354>	-367	202.5	824	S<304>	-1167	202.5	874	S<254>	-1967	202.5
775	S<353>	-383	319.5	825	S<303>	-1183	319.5	875	S<253>	-1983	319.5
776	S<352>	-399	202.5	826	S<302>	-1199	202.5	876	S<252>	-1999	202.5
777	S<351>	-415	319.5	827	S<301>	-1215	319.5	877	S<251>	-2015	319.5
778	S<350>	-431	202.5	828	S<300>	-1231	202.5	878	S<250>	-2031	202.5
779	S<349>	-447	319.5	829	S<299>	-1247	319.5	879	S<249>	-2047	319.5
780	S<348>	-463	202.5	830	S<298>	-1263	202.5	880	S<248>	-2063	202.5
781	S<347>	-479	319.5	831	S<297>	-1279	319.5	881	S<247>	-2079	319.5
782	S<346>	-495	202.5	832	S<296>	-1295	202.5	882	S<246>	-2095	202.5
783	S<345>	-511	319.5	833	S<295>	-1311	319.5	883	S<245>	-2111	319.5
784	S<344>	-527	202.5	834	S<294>	-1327	202.5	884	S<244>	-2127	202.5
785	S<343>	-543	319.5	835	S<293>	-1343	319.5	885	S<243>	-2143	319.5
786	S<342>	-559	202.5	836	S<292>	-1359	202.5	886	S<242>	-2159	202.5
787	S<341>	-575	319.5	837	S<291>	-1375	319.5	887	S<241>	-2175	319.5
788	S<340>	-591	202.5	838	S<290>	-1391	202.5	888	S<240>	-2191	202.5
789	S<339>	-607	319.5	839	S<289>	-1407	319.5	889	S<239>	-2207	319.5
790	S<338>	-623	202.5	840	S<288>	-1423	202.5	890	S<238>	-2223	202.5
791	S<337>	-639	319.5	841	S<287>	-1439	319.5	891	S<237>	-2239	319.5
792	S<336>	-655	202.5	842	S<286>	-1455	202.5	892	S<236>	-2255	202.5
793	S<335>	-671	319.5	843	S<285>	-1471	319.5	893	S<235>	-2271	319.5
794	S<334>	-687	202.5	844	S<284>	-1487	202.5	894	S<234>	-2287	202.5
795	S<333>	-703	319.5	845	S<283>	-1503	319.5	895	S<233>	-2303	319.5
796	S<332>	-719	202.5	846	S<282>	-1519	202.5	896	S<232>	-2319	202.5
797	S<331>	-735	319.5	847	S<281>	-1535	319.5	897	S<231>	-2335	319.5
798	S<330>	-751	202.5	848	S<280>	-1551	202.5	898	S<230>	-2351	202.5
799	S<329>	-767	319.5	849	S<279>	-1567	319.5	899	S<229>	-2367	319.5
800	S<328>	-783	202.5	850	S<278>	-1583	202.5	900	S<228>	-2383	202.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
901	S<227>	-2399	319.5	951	S<177>	-3199	319.5	1001	S<127>	-3999	319.5
902	S<226>	-2415	202.5	952	S<176>	-3215	202.5	1002	S<126>	-4015	202.5
903	S<225>	-2431	319.5	953	S<175>	-3231	319.5	1003	S<125>	-4031	319.5
904	S<224>	-2447	202.5	954	S<174>	-3247	202.5	1004	S<124>	-4047	202.5
905	S<223>	-2463	319.5	955	S<173>	-3263	319.5	1005	S<123>	-4063	319.5
906	S<222>	-2479	202.5	956	S<172>	-3279	202.5	1006	S<122>	-4079	202.5
907	S<221>	-2495	319.5	957	S<171>	-3295	319.5	1007	S<121>	-4095	319.5
908	S<220>	-2511	202.5	958	S<170>	-3311	202.5	1008	S<120>	-4111	202.5
909	S<219>	-2527	319.5	959	S<169>	-3327	319.5	1009	S<119>	-4127	319.5
910	S<218>	-2543	202.5	960	S<168>	-3343	202.5	1010	S<118>	-4143	202.5
911	S<217>	-2559	319.5	961	S<167>	-3359	319.5	1011	S<117>	-4159	319.5
912	S<216>	-2575	202.5	962	S<166>	-3375	202.5	1012	S<116>	-4175	202.5
913	S<215>	-2591	319.5	963	S<165>	-3391	319.5	1013	S<115>	-4191	319.5
914	S<214>	-2607	202.5	964	S<164>	-3407	202.5	1014	S<114>	-4207	202.5
915	S<213>	-2623	319.5	965	S<163>	-3423	319.5	1015	S<113>	-4223	319.5
916	S<212>	-2639	202.5	966	S<162>	-3439	202.5	1016	S<112>	-4239	202.5
917	S<211>	-2655	319.5	967	S<161>	-3455	319.5	1017	S<111>	-4255	319.5
918	S<210>	-2671	202.5	968	S<160>	-3471	202.5	1018	S<110>	-4271	202.5
919	S<209>	-2687	319.5	969	S<159>	-3487	319.5	1019	S<109>	-4287	319.5
920	S<208>	-2703	202.5	970	S<158>	-3503	202.5	1020	S<108>	-4303	202.5
921	S<207>	-2719	319.5	971	S<157>	-3519	319.5	1021	S<107>	-4319	319.5
922	S<206>	-2735	202.5	972	S<156>	-3535	202.5	1022	S<106>	-4335	202.5
923	S<205>	-2751	319.5	973	S<155>	-3551	319.5	1023	S<105>	-4351	319.5
924	S<204>	-2767	202.5	974	S<154>	-3567	202.5	1024	S<104>	-4367	202.5
925	S<203>	-2783	319.5	975	S<153>	-3583	319.5	1025	S<103>	-4383	319.5
926	S<202>	-2799	202.5	976	S<152>	-3599	202.5	1026	S<102>	-4399	202.5
927	S<201>	-2815	319.5	977	S<151>	-3615	319.5	1027	S<101>	-4415	319.5
928	S<200>	-2831	202.5	978	S<150>	-3631	202.5	1028	S<100>	-4431	202.5
929	S<199>	-2847	319.5	979	S<149>	-3647	319.5	1029	S<99>	-4447	319.5
930	S<198>	-2863	202.5	980	S<148>	-3663	202.5	1030	S<98>	-4463	202.5
931	S<197>	-2879	319.5	981	S<147>	-3679	319.5	1031	S<97>	-4479	319.5
932	S<196>	-2895	202.5	982	S<146>	-3695	202.5	1032	S<96>	-4495	202.5
933	S<195>	-2911	319.5	983	S<145>	-3711	319.5	1033	S<95>	-4511	319.5
934	S<194>	-2927	202.5	984	S<144>	-3727	202.5	1034	S<94>	-4527	202.5
935	S<193>	-2943	319.5	985	S<143>	-3743	319.5	1035	S<93>	-4543	319.5
936	S<192>	-2959	202.5	986	S<142>	-3759	202.5	1036	S<92>	-4559	202.5
937	S<191>	-2975	319.5	987	S<141>	-3775	319.5	1037	S<91>	-4575	319.5
938	S<190>	-2991	202.5	988	S<140>	-3791	202.5	1038	S<90>	-4591	202.5
939	S<189>	-3007	319.5	989	S<139>	-3807	319.5	1039	S<89>	-4607	319.5
940	S<188>	-3023	202.5	990	S<138>	-3823	202.5	1040	S<88>	-4623	202.5
941	S<187>	-3039	319.5	991	S<137>	-3839	319.5	1041	S<87>	-4639	319.5
942	S<186>	-3055	202.5	992	S<136>	-3855	202.5	1042	S<86>	-4655	202.5
943	S<185>	-3071	319.5	993	S<135>	-3871	319.5	1043	S<85>	-4671	319.5
944	S<184>	-3087	202.5	994	S<134>	-3887	202.5	1044	S<84>	-4687	202.5
945	S<183>	-3103	319.5	995	S<133>	-3903	319.5	1045	S<83>	-4703	319.5
946	S<182>	-3119	202.5	996	S<132>	-3919	202.5	1046	S<82>	-4719	202.5
947	S<181>	-3135	319.5	997	S<131>	-3935	319.5	1047	S<81>	-4735	319.5
948	S<180>	-3151	202.5	998	S<130>	-3951	202.5	1048	S<80>	-4751	202.5
949	S<179>	-3167	319.5	999	S<129>	-3967	319.5	1049	S<79>	-4767	319.5
950	S<178>	-3183	202.5	1000	S<128>	-3983	202.5	1050	S<78>	-4783	202.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
1051	S<77>	-4799	319.5	1101	S<27>	-5599	319.5	1151	G<40>	-6419	202.5
1052	S<76>	-4815	202.5	1102	S<26>	-5615	202.5	1152	G<42>	-6435	319.5
1053	S<75>	-4831	319.5	1103	S<25>	-5631	319.5	1153	G<44>	-6451	202.5
1054	S<74>	-4847	202.5	1104	S<24>	-5647	202.5	1154	G<46>	-6467	319.5
1055	S<73>	-4863	319.5	1105	S<23>	-5663	319.5	1155	G<48>	-6483	202.5
1056	S<72>	-4879	202.5	1106	S<22>	-5679	202.5	1156	G<50>	-6499	319.5
1057	S<71>	-4895	319.5	1107	S<21>	-5695	319.5	1157	G<52>	-6515	202.5
1058	S<70>	-4911	202.5	1108	S<20>	-5711	202.5	1158	G<54>	-6531	319.5
1059	S<69>	-4927	319.5	1109	S<19>	-5727	319.5	1159	G<56>	-6547	202.5
1060	S<68>	-4943	202.5	1110	S<18>	-5743	202.5	1160	G<58>	-6563	319.5
1061	S<67>	-4959	319.5	1111	S<17>	-5759	319.5	1161	G<60>	-6579	202.5
1062	S<66>	-4975	202.5	1112	S<16>	-5775	202.5	1162	G<62>	-6595	319.5
1063	S<65>	-4991	319.5	1113	S<15>	-5791	319.5	1163	G<64>	-6611	202.5
1064	S<64>	-5007	202.5	1114	S<14>	-5807	202.5	1164	G<66>	-6627	319.5
1065	S<63>	-5023	319.5	1115	S<13>	-5823	319.5	1165	G<68>	-6643	202.5
1066	S<62>	-5039	202.5	1116	S<12>	-5839	202.5	1166	G<70>	-6659	319.5
1067	S<61>	-5055	319.5	1117	S<11>	-5855	319.5	1167	G<72>	-6675	202.5
1068	S<60>	-5071	202.5	1118	S<10>	-5871	202.5	1168	G<74>	-6691	319.5
1069	S<59>	-5087	319.5	1119	S<9>	-5887	319.5	1169	G<76>	-6707	202.5
1070	S<58>	-5103	202.5	1120	S<8>	-5903	202.5	1170	G<78>	-6723	319.5
1071	S<57>	-5119	319.5	1121	S<7>	-5919	319.5	1171	G<80>	-6739	202.5
1072	S<56>	-5135	202.5	1122	S<6>	-5935	202.5	1172	G<82>	-6755	319.5
1073	S<55>	-5151	319.5	1123	S<5>	-5951	319.5	1173	G<84>	-6771	202.5
1074	S<54>	-5167	202.5	1124	S<4>	-5967	202.5	1174	G<86>	-6787	319.5
1075	S<53>	-5183	319.5	1125	S<3>	-5983	319.5	1175	G<88>	-6803	202.5
1076	S<52>	-5199	202.5	1126	S<2>	-5999	202.5	1176	G<90>	-6819	319.5
1077	S<51>	-5215	319.5	1127	S<1>	-6015	319.5	1177	G<92>	-6835	202.5
1078	S<50>	-5231	202.5	1128	S<0>	-6031	202.5	1178	G<94>	-6851	319.5
1079	S<49>	-5247	319.5	1129	DUMMY	-6047	319.5	1179	G<96>	-6867	202.5
1080	S<48>	-5263	202.5	1130	DUMMY	-6083	319.5	1180	G<98>	-6883	319.5
1081	S<47>	-5279	319.5	1131	G<0>	-6099	202.5	1181	G<100>	-6899	202.5
1082	S<46>	-5295	202.5	1132	G<2>	-6115	319.5	1182	G<102>	-6915	319.5
1083	S<45>	-5311	319.5	1133	G<4>	-6131	202.5	1183	G<104>	-6931	202.5
1084	S<44>	-5327	202.5	1134	G<6>	-6147	319.5	1184	G<106>	-6947	319.5
1085	S<43>	-5343	319.5	1135	G<8>	-6163	202.5	1185	G<108>	-6963	202.5
1086	S<42>	-5359	202.5	1136	G<10>	-6179	319.5	1186	G<110>	-6979	319.5
1087	S<41>	-5375	319.5	1137	G<12>	-6195	202.5	1187	G<112>	-6995	202.5
1088	S<40>	-5391	202.5	1138	G<14>	-6211	319.5	1188	G<114>	-7011	319.5
1089	S<39>	-5407	319.5	1139	G<16>	-6227	202.5	1189	G<116>	-7027	202.5
1090	S<38>	-5423	202.5	1140	G<18>	-6243	319.5	1190	G<118>	-7043	319.5
1091	S<37>	-5439	319.5	1141	G<20>	-6259	202.5	1191	G<120>	-7059	202.5
1092	S<36>	-5455	202.5	1142	G<22>	-6275	319.5	1192	G<122>	-7075	319.5
1093	S<35>	-5471	319.5	1143	G<24>	-6291	202.5	1193	G<124>	-7091	202.5
1094	S<34>	-5487	202.5	1144	G<26>	-6307	319.5	1194	G<126>	-7107	319.5
1095	S<33>	-5503	319.5	1145	G<28>	-6323	202.5	1195	G<128>	-7123	202.5
1096	S<32>	-5519	202.5	1146	G<30>	-6339	319.5	1196	G<130>	-7139	319.5
1097	S<31>	-5535	319.5	1147	G<32>	-6355	202.5	1197	G<132>	-7155	202.5
1098	S<30>	-5551	202.5	1148	G<34>	-6371	319.5	1198	G<134>	-7171	319.5
1099	S<29>	-5567	319.5	1149	G<36>	-6387	202.5	1199	G<136>	-7187	202.5
1100	S<28>	-5583	202.5	1150	G<38>	-6403	319.5	1200	G<138>	-7203	319.5

Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos	Pad No.	Pad Name	X-Pos	Y-Pos
1201	G<140>	-7219	202.5	1251	G<240>	-8019	202.5				
1202	G<142>	-7235	319.5	1252	G<242>	-8035	319.5				
1203	G<144>	-7251	202.5	1253	G<244>	-8051	202.5				
1204	G<146>	-7267	319.5	1254	G<246>	-8067	319.5				
1205	G<148>	-7283	202.5	1255	G<248>	-8083	202.5				
1206	G<150>	-7299	319.5	1256	G<250>	-8099	319.5				
1207	G<152>	-7315	202.5	1257	G<252>	-8115	202.5				
1208	G<154>	-7331	319.5	1258	G<254>	-8131	319.5				
1209	G<156>	-7347	202.5	1259	G<256>	-8147	202.5				
1210	G<158>	-7363	319.5	1260	G<258>	-8163	319.5				
1211	G<160>	-7379	202.5	1261	G<260>	-8179	202.5				
1212	G<162>	-7395	319.5	1262	G<262>	-8195	319.5				
1213	G<164>	-7411	202.5	1263	G<264>	-8211	202.5				
1214	G<166>	-7427	319.5	1264	G<266>	-8227	319.5				
1215	G<168>	-7443	202.5	1265	G<268>	-8243	202.5				
1216	G<170>	-7459	319.5	1266	G<270>	-8259	319.5				
1217	G<172>	-7475	202.5	1267	G<272>	-8275	202.5				
1218	G<174>	-7491	319.5	1268	G<274>	-8291	319.5				
1219	G<176>	-7507	202.5	1269	G<276>	-8307	202.5				
1220	G<178>	-7523	319.5	1270	G<278>	-8323	319.5				
1221	G<180>	-7539	202.5	1271	G<280>	-8339	202.5				
1222	G<182>	-7555	319.5	1272	G<282>	-8355	319.5				
1223	G<184>	-7571	202.5	1273	G<284>	-8371	202.5				
1224	G<186>	-7587	319.5	1274	G<286>	-8387	319.5				
1225	G<188>	-7603	202.5	1275	G<288>	-8403	202.5				
1226	G<190>	-7619	319.5	1276	G<290>	-8419	319.5				
1227	G<192>	-7635	202.5	1277	G<292>	-8435	202.5				
1228	G<194>	-7651	319.5	1278	G<294>	-8451	319.5				
1229	G<196>	-7667	202.5	1279	G<296>	-8467	202.5				
1230	G<198>	-7683	319.5	1280	G<298>	-8483	319.5				
1231	G<200>	-7699	202.5	1281	G<300>	-8499	202.5				
1232	G<202>	-7715	319.5	1282	G<302>	-8515	319.5				
1233	G<204>	-7731	202.5	1283	G<304>	-8531	202.5				
1234	G<206>	-7747	319.5	1284	G<306>	-8547	319.5				
1235	G<208>	-7763	202.5	1285	G<308>	-8563	202.5				
1236	G<210>	-7779	319.5	1286	G<310>	-8579	319.5				
1237	G<212>	-7795	202.5	1287	G<312>	-8595	202.5				
1238	G<214>	-7811	319.5	1288	G<314>	-8611	319.5				
1239	G<216>	-7827	202.5	1289	G<316>	-8627	202.5				
1240	G<218>	-7843	319.5	1290	G<318>	-8643	319.5				
1241	G<220>	-7859	202.5	1291	DUMMY	-8659	202.5				
1242	G<222>	-7875	319.5								
1243	G<224>	-7891	202.5								
1244	G<226>	-7907	319.5								
1245	G<228>	-7923	202.5								
1246	G<230>	-7939	319.5								
1247	G<232>	-7955	202.5								
1248	G<234>	-7971	319.5								
1249	G<236>	-7987	202.5								
1250	G<238>	-8003	319.5								

6. PIN DESCRIPTION

Remark:

I = Input;
O = Output;
IO = Bi-directional;
P = Power;,
GND = System VSS;

Table 6-1 Power Supply Pins

Pin Name	Type	Connect to	Function	Description	When not in use
VSS	P	GND	Ground of the Power Supply	System ground pin of the IC.	-
AVSS		GND		Grounding for analog circuit.	-
VCHS		AVSS		Grounding for booster circuit.	-
VCI	P	Power Supply	Power Supply for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V	-
VCIM	O	Stabilizing capacitor	Booster voltages	Negative voltage of VCI.	-
VCIX2		Stabilizing capacitor		Equals to 2x VCI	-
VCIX2G		VCIX2 on FPC			-
VCOMR	I	External voltage source or Open	External Reference	This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 set to "01111". - Connect to an external voltage source for reference	Open
VCOMH	O	Stabilizing capacitor	Voltages for VCOM Signal	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation.	-
VCOML		Stabilizing capacitor		This pin indicates a LOW level of VCOM generated in driving the VCOM alternation.	-
VLCD63	O	Stabilizing capacitor	LCD Driving Voltages	This pin is the maximum source driver voltage.	-
VGH		Stabilizing capacitor		A positive power output pin for gate driver and for MTP programming	-
VGL		Stabilizing capacitor		A negative power output pin for gate driver.	-
EXVR	I	GND	External Reference	External reference of internal gamma resistor - Connect to VSS	-
CXP	I	Booster capacitor	Booster and Stabilization Capacitors	- Connect a capacitor to CXN	-
CXN				- Connect a capacitor to CXP	-
CYP		Booster capacitor		- Connect a capacitor to CYN	-
CYN				- Connect a capacitor to CYP	-
C1P		Booster capacitor		- Connect a capacitor to C1N	-
C1N				- Connect a capacitor to C1P	-
C2P		Booster capacitor		- Connect a capacitor to C2N	-
C2N				- Connect a capacitor to C2P	-
C3P		Booster capacitor		- Connect a capacitor to C3N	-
C3N				- Connect a capacitor to C3P	-
CDUM0		Stabilizing capacitor	Stabilization Capacitors	- Connect a capacitor to VSS	Open
VCORE	P	Stabilizing capacitor	Power for Core Logic	Vdd for core use. Connect a capacitor for stabilization	-

Pin Name	Type	Connect to	Function	Description	When not in use
VREGC	P	VCORE	Regulator output for logic circuits	Regulator output for VCORE use.	-
VDDIO	P	Power Supply	Power for interface logic pins	Voltage input pin for logic I/O, connect to system VDD. - Connect to voltage source between 1.4V to 3.6V	-

Table 6-2 Interface Logic Pins

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>DC/SDC</td><td rowspan="3">I</td><td>MPU</td><td rowspan="3">Logic Control</td><td>Data or command</td><td>V_{DDIO} or V_{ss}</td></tr>
<tr><td>CS</td><td>MPU</td><td>Chip select pin for 6800/8080/SPI interface</td><td>-</td></tr>
<tr><td>RD</td><td>MPU</td><td>6800-system : E (enable signal)
8080-system : RD (read strobe signal)
Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}</td><td>V_{DDIO} or V_{ss}</td></tr>
<tr><td>RW</td><td>MPU</td><td>68-system : RW (indicates read cycle when High, write cycle when Low)
80-system : WR (write strobe signal)
Serial mode : SCL (serial clock input)</td><td>V_{DDIO} or V_{ss}</td></tr>
<tr><td>D0-D17</td><td>IO</td><td>MPU</td><td>Data bus</td><td>For parallel mode, 8/9/16/18 bit interface.
Please refer to Section 15 Interface Mapping for definition.
Unused pins should connect to V_{SS}.</td><td>V_{SS}</td></tr>
<tr><td>WSYNC</td><td>O</td><td>MPU</td><td>Logic Control</td><td>Ram Write Synchronization output</td><td>Open</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td rowspan="4">Display Timing Signals</td><td>Display enable pin from controller. Data will be treated as dummy regardless the ENABLE status during front/back porch setting at register R16 and R17</td><td>V_{SS}</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.</td><td>Vss</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>Line Synchronization input</td><td>V_{SS}</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>Frame/Ram Write Synchronization input</td><td>V_{SS}</td></tr>
<tr><td>RESB</td><td>I</td><td>MPU</td><td>System Reset</td><td>System reset pin.
- An active low pulse at this pin will reset the IC, Connect to V_{DDIO} in normal operation</td><td>-</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td rowspan="3">Serial interface</td><td>Data input pin in serial interface</td><td>V_{SS}</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Data output pin in serial interface</td><td>Open</td></tr>
<tr><td>SCL</td><td>I</td><td>MPU</td><td>Serial clock input</td><td></td></tr>
<tr><td>IFSEL0</td><td>I</td><td>MPU</td><td>Interface selection</td><td><table><tr><td>IFSEL0</td><td>Interface Format Selection</td></tr><tr><td>0</td><td>Command Parameter Interface Mode</td></tr><tr><td>1</td><td>Register content interface Mode</td></tr></table></td><td></td></tr>
<tr><td>EXTC</td><td>I</td><td>MPU</td><td>Interface selection</td><td>When operate in Register-content interface mode, the EXTC has to be connected to VDDIO or VSS.</td><td></td></tr>
</table>

Table 6-3 Mode Selection Pins

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>PS[3:0]</td><td>I</td><td>V_{DDIO} or V_{SS}</td><td>Interface Selection</td><td>
<table>
<tr><th>PS3</th><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit, 8080 parallel, 65K color</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16-bit, 8080 parallel, 262K color (TypeA)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-bit, 8080 parallel, 262K color</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit, 8080 parallel, 262K color</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit, 8080 parallel, 262K color</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit, 8080 parallel, 262K color</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Serial bus, 3-wire</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>18-bit Generic + serial 3-wire</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-bit, 6800 parallel, 65K color</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit, 6800 parallel, 262K color(TypeA)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit, 6800 parallel, 262K color</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-bit, 6800 parallel, 262K color</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>16-bit, 6800 parallel, 262K color</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>18-bit, 6800 parallel, 262K color</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Serial bus, 4-wire</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>18-bit Generic + serial 4-wire</td></tr>
</table>
</td><td>-</td></tr>
</table>

Table 6-4 Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
VCOM	O	LCD	LCD Driving Signals	A power supply for the TFT-display common electrode.	Open
G0-G319		LCD		Gate driver output pins. These pins output V_{GH}, V_{GL} or V_{GOFFH} level.	Open
S0-S719		LCD		Source driver output pins. S(3n) : display Red if BGR = LOW, Blue if BGR = HIGH. S(3n+1) : display Green. S(3n+2) : display Blue if BGR = LOW, Red if BGR = HIGH.	Open

Table 6-5 Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	-	-	-	These pins must be left open and cannot be connected together	Open
DUMMY	-	-	-	Floating pins and no connection inside the IC. These pins should be open.	Open
TESTAX	IO	FPC	IC Testing Signal	Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open
TESTBX		FPC		Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open
TESTCX		FPC		Test pin of the internal circuit. - Leave this pin open and insert test point in FPC	Open

7. FUNCTION BLOCK DESCRIPTIONS

System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series high speed parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 19.

MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], $R/\overline{W}$, $D/\overline{C}$, E and $\overline{CS}$. $R/\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. $R/\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of $D/\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

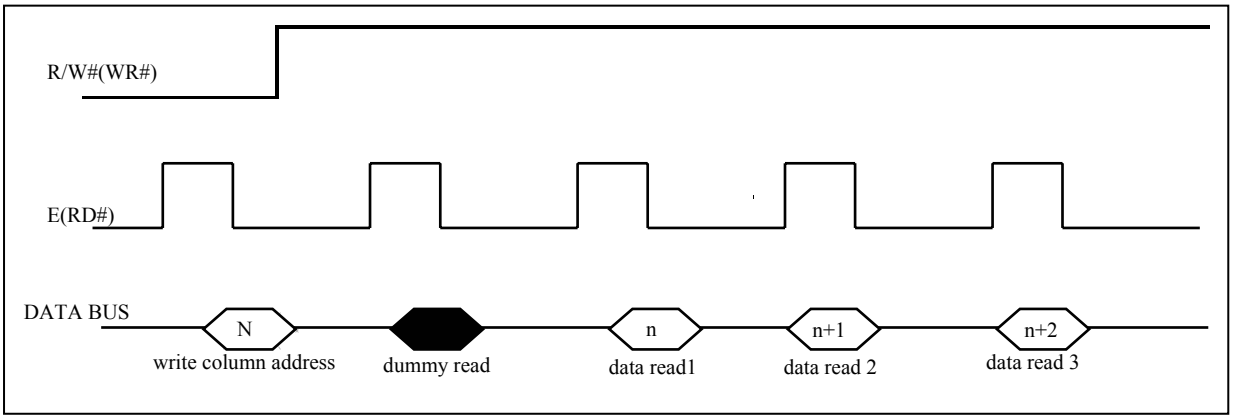


Figure 7-1 Read Display Data

MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D[17:0], RD, WR, DC and CSB. RD input serves as data read latch signal (clock) when low provided that CSB is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by DC. WR input serves as data write latch signal (clock) when low provided that CSB is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface. Please refer Figure 7-1.

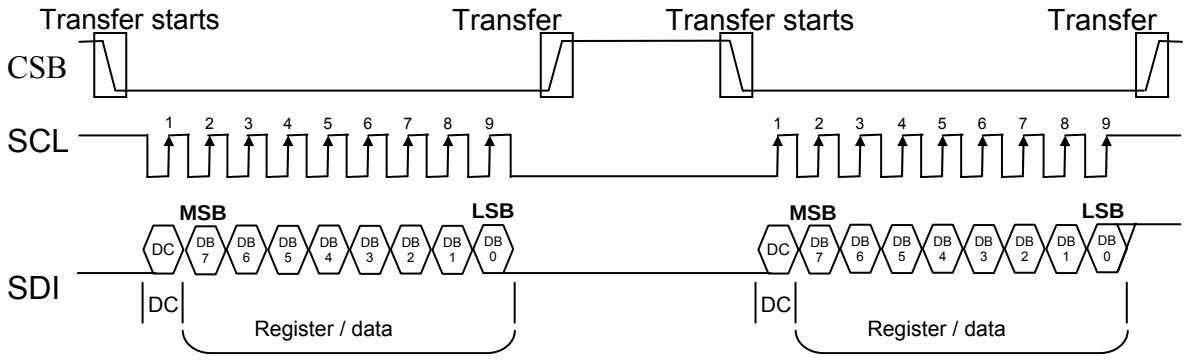
3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while DC is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).

	6800 – series Parallel Interface	8080 – series Parallel Interface	MCU Serial Interface
Data Read	18/16/9/8-bits	18/16/9/8-bits	Yes
Data Write	18/16/9/8-bits	18/16/9/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	8-bits

Table 7-1 Data bus selection modes

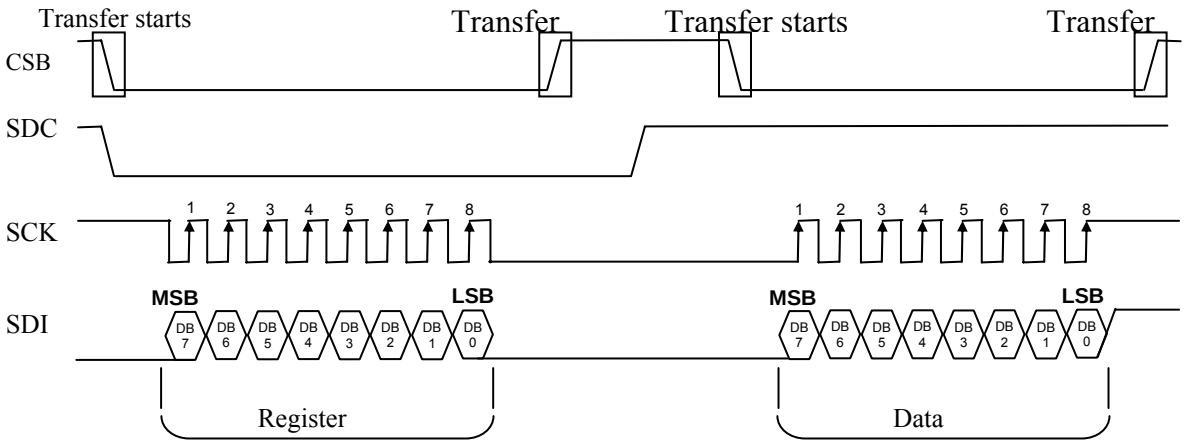
Figure 7-2 3-wire SPI interface (9 bits)



4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB.SDC determinate the data of SDI which is register or data.

Figure 7-3 4-wire SPI interface (8 bits)



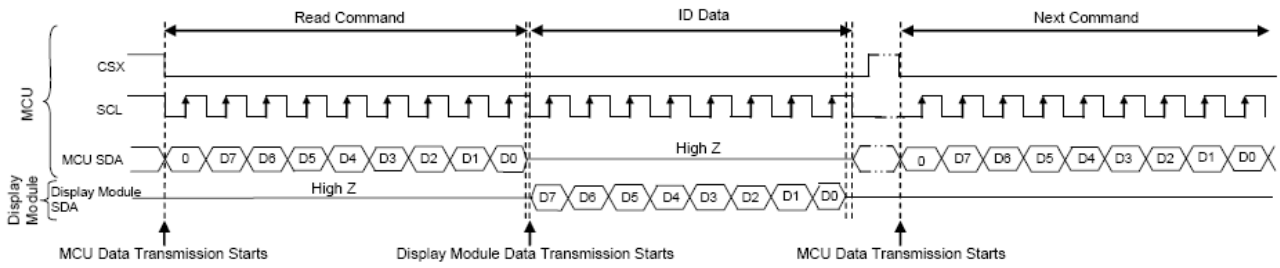
LoSSI(Low Speed Screen Interface)

The Low Speed Screen Interface (LoSSI) is a 3-wire 9-bit serial interface. Serial data must be input to SDA in the sequence of D/C, D7 to D0. The graphics controller reads the data at the rising edge of SCL signal. The first bit of serial data D/C is a data/command flag. When the D/C = "1", D7 to D0 bits are display RAM data or command parameters. When D/C = "0", D7 to D0 bits are commands. SCL signal is not a continuous clock and it can be stopped by the MCU when CL signal is low or high after a rising edge of SCL for D0. SCL and SDA can be high or low when there is a falling or rising edge of the /CS signal.

Command Write

The MCU drives the /CS pin low and starts by setting the D/C-bit on SDA. The bit is read by the display on the first rising edge of SCL. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the MCU. On the next falling edge of SCL, the next bit (D6) is set on the SDA. This continues until all 8 Data bits have been transmitted.

Figure 7-4 Read Function DAH, DBH, DCH, DFH



Note 1: Data length is 8bits.
Note 2: The read function is always terminated a high pulse of the CSX by the MCU.

Display Data Transfer Recovery

If there is a break in data transmission, while transferring a command, frame memory data or multiple parameter command data, before bit D0 of the byte being completed, the display module will reject

the previous bits and reset the interface such that it will be ready to receive the same byte to be retransmitted when the chip select line (/CS) is next activated.

If a command, with 1 or more parameters, is being sent and a break occurs while sending any parameter before the last one and the host then sends a new command rather than re-transmitting the parameter that was interrupted, the parameters that were successfully sent are stored and the broken parameter is rejected. The interface is then ready to receive the next byte.

Display Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then the display module will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select line is released after a whole byte of a command has been completed, then the display IC will receive either the command's parameters or a new command when the chip select line is next enabled. Four conditions are applied for the above cases:

Command-Pause-Command
Command-Pause-Parameter
Parameter-Pause-Command
Parameter-Pause-Parameter

Table 7-2 MODES OF OPERATION

	Serial
Data Read	No
Data Write	Yes
Command Read	Yes
Command Write	Yes

RGB Interface

SSD1297 supports RGB interface. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and ENABLE signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

Address Counter (AC)

The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 240 RGB x 320 x 18 / 8 = 172,800 bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command "Data Output/Scan direction" for detail description.

Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command "Set area Scroll" and "Set Scroll Start".

Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma adjustment resister. 262,144 possible colors can be displayed when 1 pixel = 18 bit. For details, see the gamma adjustment register.

Booster and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOM levels and VLCD0~63 which are necessary for operating a TFT LCD.

Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal RAM accessing, date output timing etc.

Oscillation Circuit (OSC)

This module is an on-chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the display timing generator.

Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

Liquid Crystal Driver Circuit

SSD1297 consists of a 720-output source driver (S0-S719) and a 320-output gate driver (G0-G319). The display image data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the RL bit and the shift direction of gate output from the gate driver can be changed by setting the TB bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the TB bit to select the operimal scan mode for the module.

8. COMMAND TABLE

Table 8-1 Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	0	BGR	SM	TB	MUX8	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	[0XXX][X0X1]3F			0	X	X	X	X	0	X	1	0	0	1	1	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6830h)			0	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0
R15h	Entry mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nMTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM MTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM MTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Vertical RAM address start position	0	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Vertical RAM address end position	0	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: In R01h, bits REV, BGR, TB, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

9. COMMAND DESCRIPTION

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

If this register is read forcibly, 9999h is read.

Oscillator (R00h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = 413Fh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	REV	GD	BGR	SM	TB	MUX8	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source Output level	
		Vcom = "L"	Vcom = "H"
0	00000H : 3FFFFH	V63 : V0	V0 : V63
1	00000H : 3FFFFH	V0 : V63	V63 : V0

BGR: Selects the order from RGB to BGR in writing 18-bit pixel data in the GDDRAM.
When BGR = "0" <R><G><B> color is assigned from S0.
When BGR = "1" <B><G><R> color is assigned from S0.

SM: Change scanning order of gate driver.

SM	Gate scan squence (GD='0')
0	G0, G1, G2, G3……G219 (left and right gate interlaced)
1	G0, G2, ……G318, G1, G3, ……G319

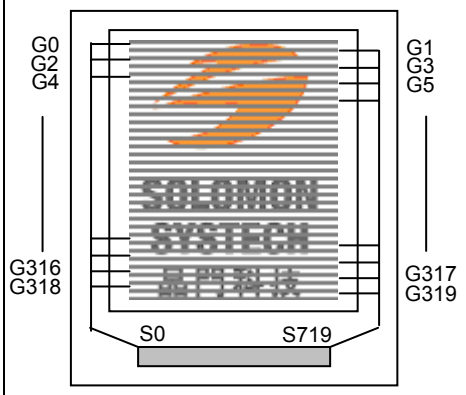
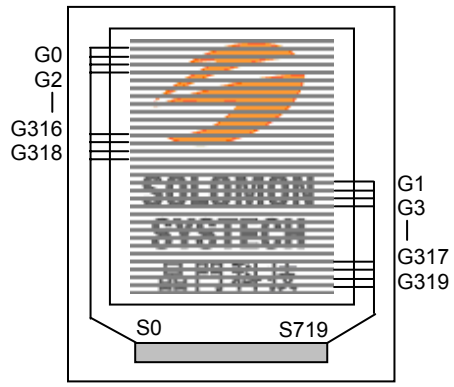
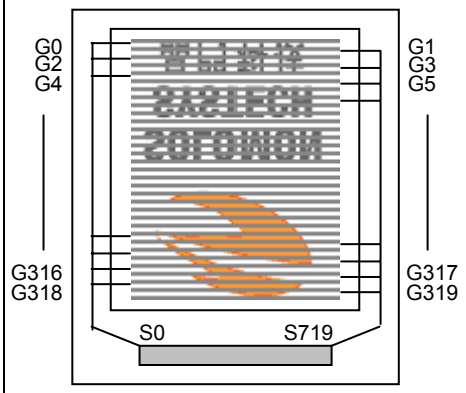
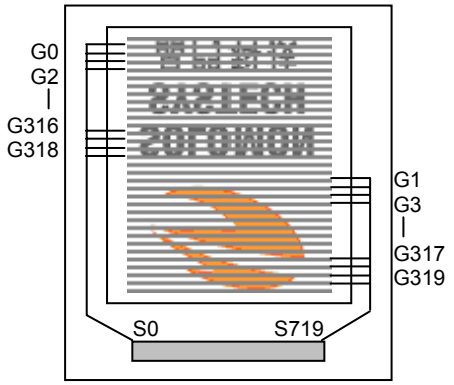
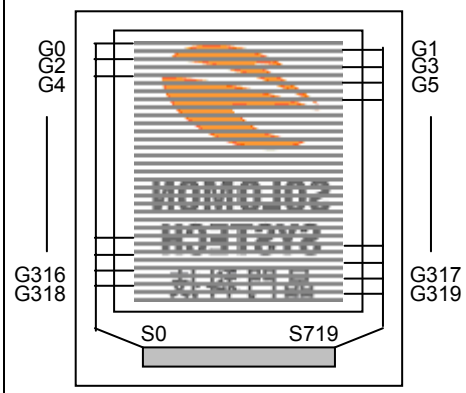
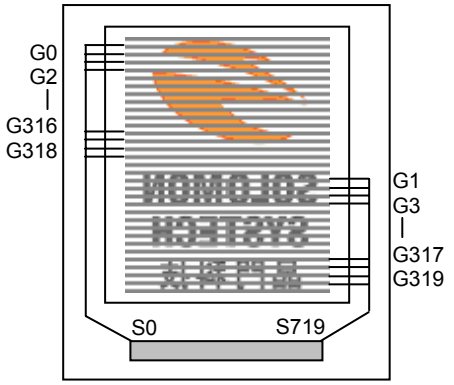
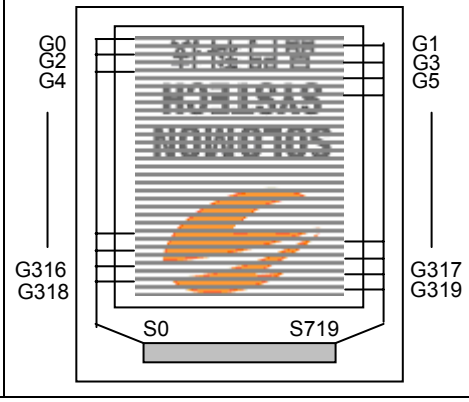
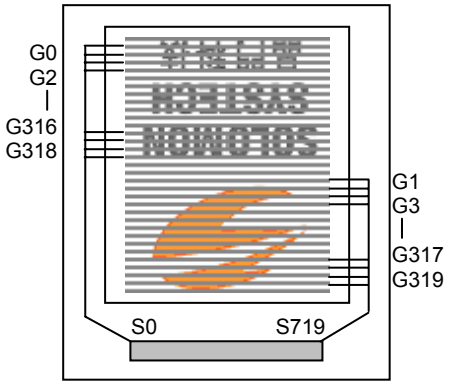
See "Scan mode setting" on next page.

TB: Selects the output shift direction of the gate driver.
When TB = 0, G0 shifts to G319.
When TB = 1, G319 shifts to G0.

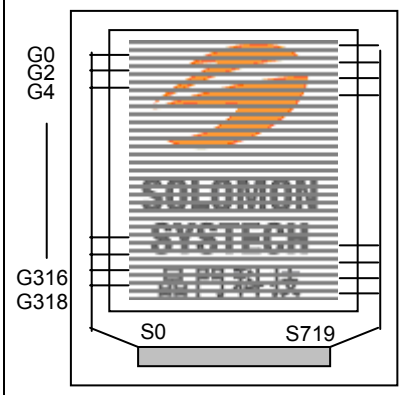
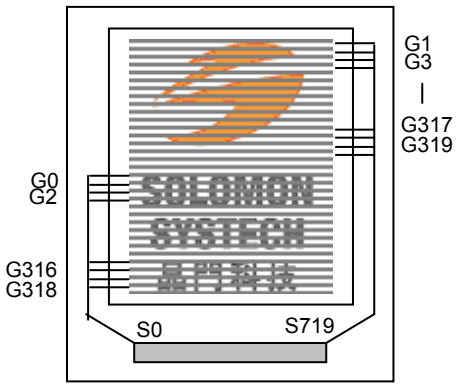
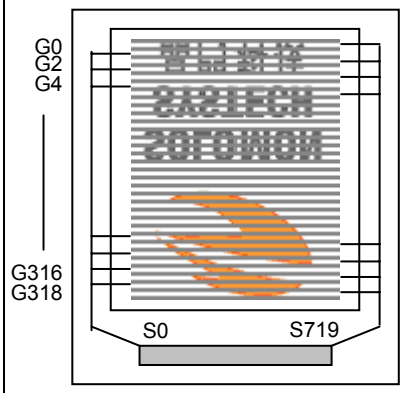
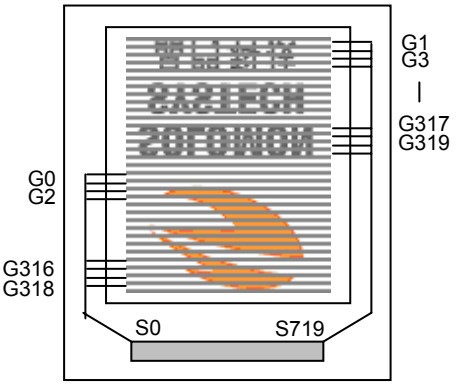
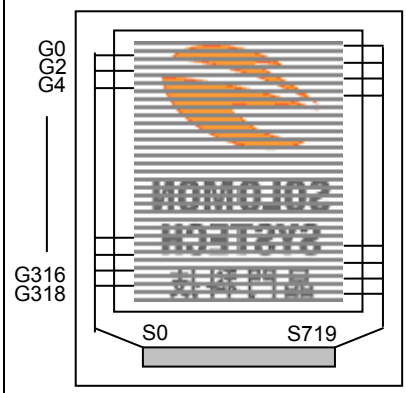
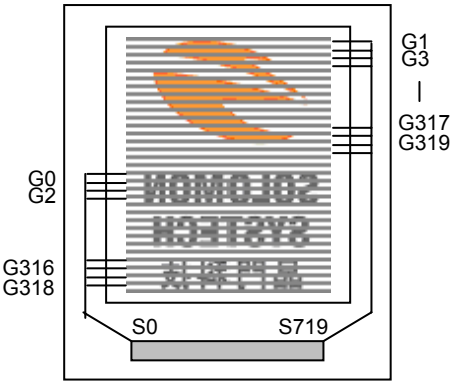
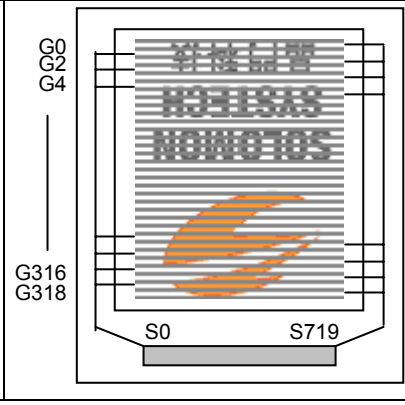
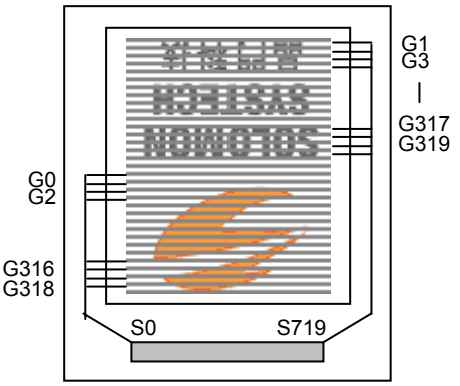
RL: Selects the output shift direction of the source driver.
When RL = "1", S0 shifts to S719 and <R><G><B> color is assigned from S0.
When RL = "0", S719 shifts to S0 and <R><G><B> color is assigned from S719.
Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode[1:0] = 00).

MUX[8:0]: Specify number of lines for the LCD driver. MUX[8:0] settings cannot exceed 319.
Remark: When using the partial display, the output for non-display area will be minimum voltage.

GD=’0’, G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, …, G318, G319.

	SM = 0	SM = 1
TB = 0 **RL = 1**		
TB = 1 **RL = 1**		
TB = 0 **RL = 0**		
TB = 1 **RL = 0**		

GD=’1’, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …, G319, G318.

	SM = 0	SM = 1
TB = 0 RL = 1		
TB = 1 RL = 1		
TB = 0 RL = 0		
TB = 1 RL = 0		

LCD-Driving-Waveform Control (R02h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

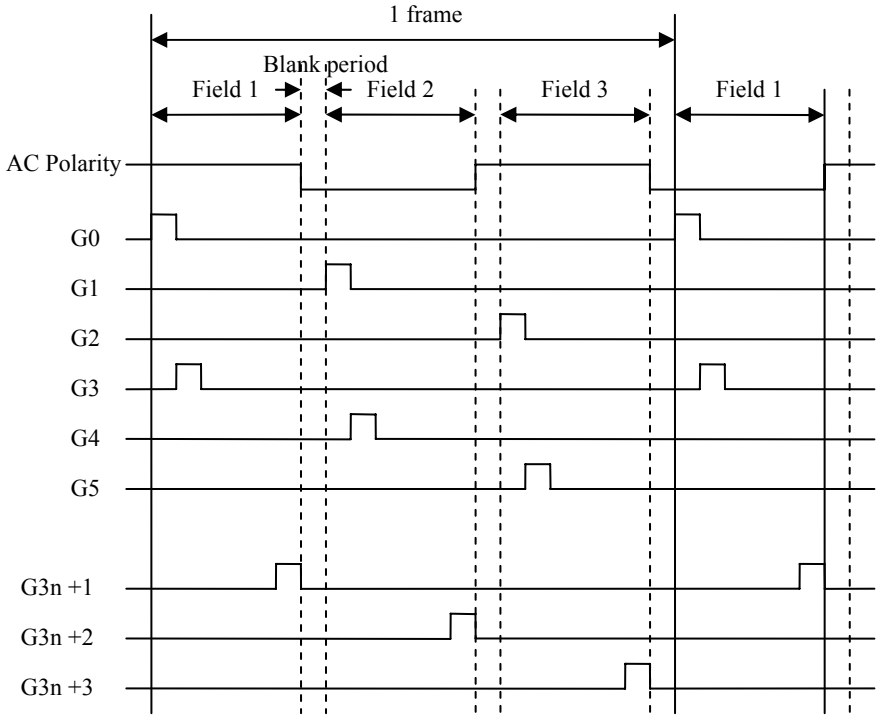
FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive.
When FLD = 1, it is 3 field driving, which also limit VBP = 1.
When FLD = 0, it is normal driving.

The following figure shows the gate selection when the 3-field invension is enabled and the output waveform of the 3-field interlaced driving.

Table 9-1 field interlace driving

TB = 1			TB = 0		
Gate	FLD = 0	FLD = 1	Gate	FLD = 0	FLD = 1
G0	X		G319	X	
G1	X		G318	X	
G2	X	X	G317	X	X
G3	X		G316	X	
G4	X		G315	X	
	X	X		X	X
	X			X	
	X			x	
G317	X		G2	X	
G318	X		G1	X	
G319	X	X	G0	X	X

Figure 9-1 gate output timing in 3-field interlacing driving



B/C: Select the liquid crystal drive waveform VCOM.

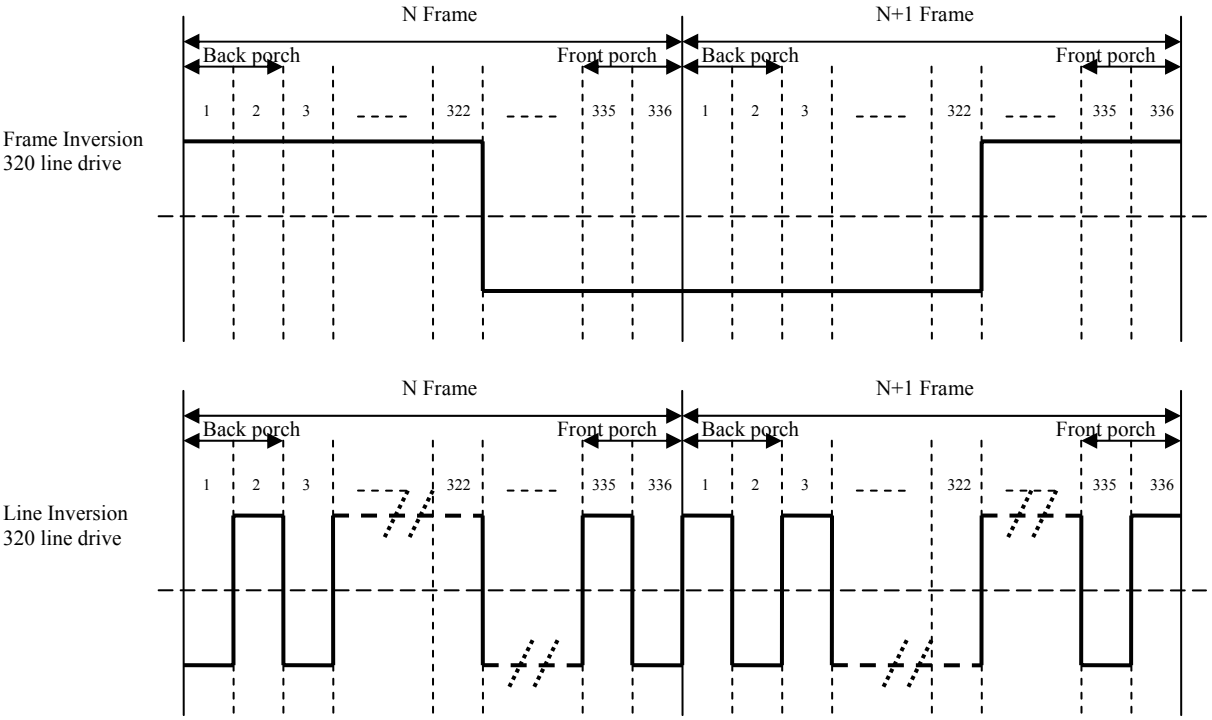
When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

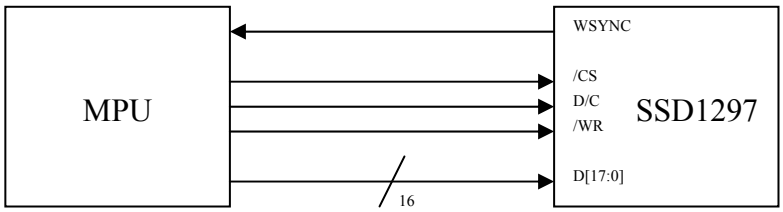
EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW[7:0]: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). N-line is equal to NW[7:0]+1.

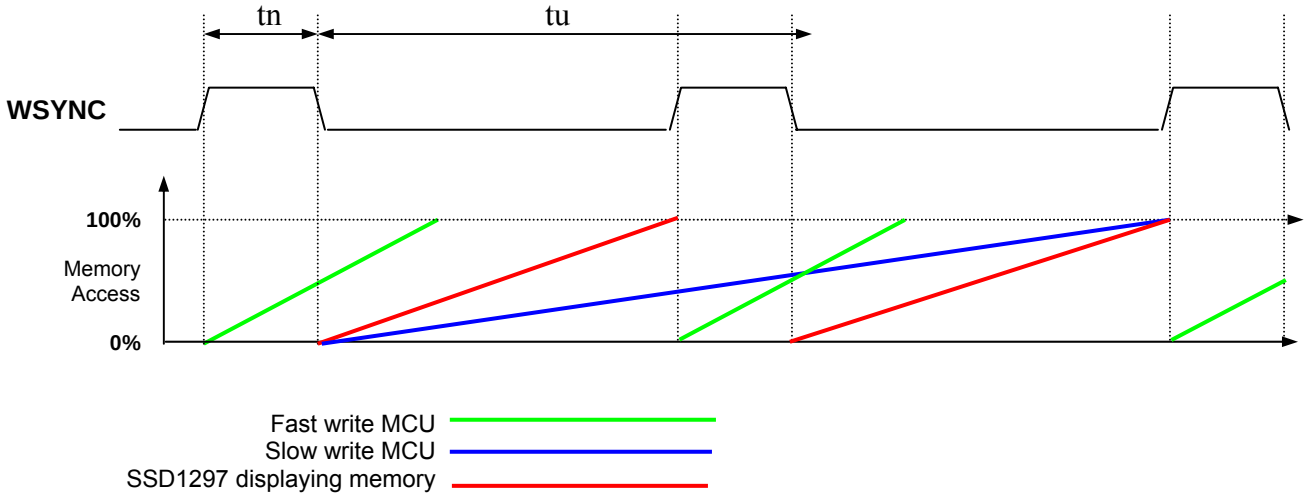
Figure 9-2 Line Inversion AC Driver



ENWS: When ENWS = 1, it enables WSYNC output pin. Mode1 or Mode2 is selected by WSMD. When ENWS = 0(POR), it disables WSYNC feature, the WSYNC output pin will be high-impedance.

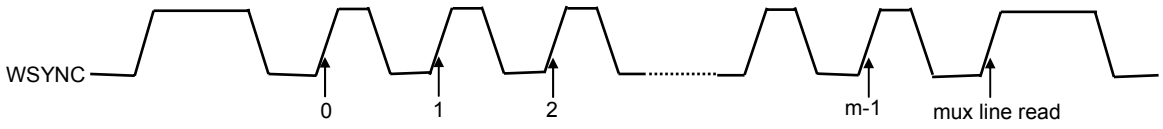


WSMD = 0 is **mode1**, the waveform of WSYNC output will be:



tn is the time when there is No Update of LCD screen from on-chip ram content.
tu is the time when the LCD screen is updating based on on-chip ram content.
e.g. fosc = 510KHz, for 320mux, tn = 282us (6 lines), tu =15.06ms (320 lines)

WSMD = 1 is **mode2**, the waveform of WSYNC output will be:



For fast write MCU: MCU should start to write new frame of ram data just after rising edge of long WSYNC pulse and should be finished well before the rising edge of the next long WSYNC pulse.
e.g. 5MHz 8 bit parallel write cycle for 18 bit color depth, or 3MHz 8 bit parallel write cycle for 16 bit color depth.

For slow write MCU (Half the write speed of fast write): MCU should start to write new frame ram data after the rising edge of the first short WSYNC pulse and must be finished within 2 frames time.
e.g. 2.5MHz 8 bit parallel write cycle for 18 bit color depth.
* Usually, **mode2** is for slower MCU, while **mode1** is for fast MCU.

Power control 1 (R03h) (POR = 6864h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
POR		0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0

DCT[3:0]: Set the step-up cycle of the step-up circuit for 8-color mode (CM = V_{DDIO}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
fosc = Internal oscillator frequency (~510KHz)

BT[2:0]: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	3 x V_{CIX2}	-(V_{GH}) + V_{CI}	+6	-5
0	0	1	3 x V_{CIX2}	-(V_{GH}) + V_{CIX2}	+6	-4
0	1	0	3 x V_{CIX2}	-(V_{CIX2})	+6	-2
0	1	1	2 x V_{CIX2} + V_{CI}	-(V_{GH})	+5	-5
1	0	0	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{CI}	+5	-4
1	0	1	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{Cix2}	+5	-3
1	1	0	2 x V_{CIX2}	-(V_{GH})	+4	-4
1	1	1	2 x V_{CIX2}	-(V_{GH}) + V_{CI}	+4	-3

DC[3:0]: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = V_{SS}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
fosc = Internal oscillator frequency (~510KHz)

AP[2:0]: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Display Control (R07h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PT[1:0]: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE[2:1]: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL17-0 in R41h register. When VLE1 = 1 and VLE2 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL1[8:0] and VL2[8:0] respectively.

SPT: When SPT = "1", the 2-division LCD drive is performed.

CM: 8-color mode setting.
When CM = 1, 8-color mode is selected.
When CM = 0, 8-color mode is disable.

GON: Gate off level becomes VGH when GON = "0".

DTE: When GON = "1" and DTE = "0", all gate outputs become VGL. When GON = "1" and DTE = "1", selected gate wire becomes VGH, and non-selected gate wires become VGL.

D[1:0]: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D[1:0] = "01", the internal display is performed although the display is off. When D[1:0] = "00", the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

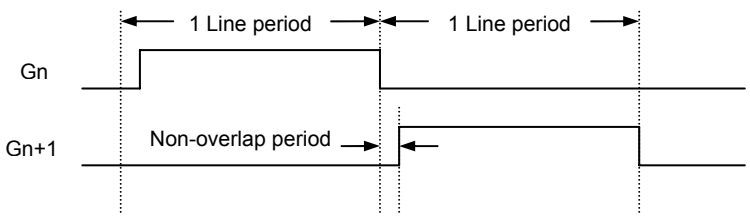
GON	DTE	D1	D0	Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	V_{GH}
0	0	0	1	Operation	GND	V_{GH}
1	0	0	1	Operation	GND	V_{GOFFL}
1	0	1	1	Operation	Grayscale level output	V_{GOFFL}
1	1	1	1	Operation	Grayscale level output	Selected gate line: V_{GH} Non-selected gate line: V_{GOFFL}

Frame Cycle Control (R0Bh) (POR = 5308h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
POR		0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0

NO[1:0]: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	reserved
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle

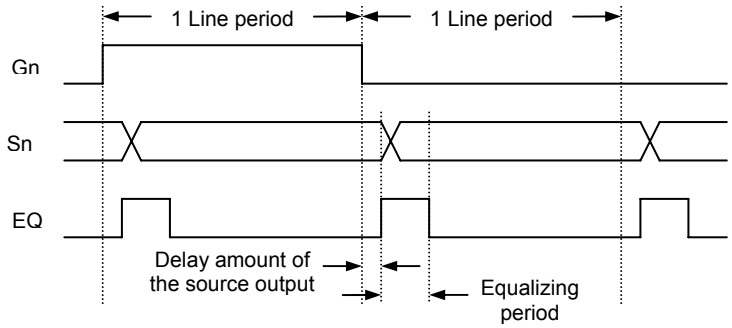


SDT[1:0]: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	0 clock cycle
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle

EQ[2:0]: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	2 clock cycle
0	1	0	3 clock cycle
0	1	1	4 clock cycle
1	0	0	5 clock cycle
1	0	1	6 clock cycle
1	1	0	7 clock cycle
1	1	1	8 clock cycle



DIV[1:0]: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV1-0 setting.

DIV1	DIV0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	8

* fosc = internal oscillator frequency, ~510kHz

SDIV: When SDIV = 1, DIV1-0 value will be count. When SDIV = 0, DIV1-0 value will be auto determined.

SRTN: When SRTN =1, RTN3-0 value will be count. When SRTN = 0, RTN3-0 value will be auto determined.

RTN[3:0]: Set the no. of clocks in each line. The total number will be the decimal value of RTN3-0 plus 16. e.g. if RTN3-0 = "1010h", the total number of clocks in each line = 10 +16 = 26 clocks.

Frame frequency calculation

For DMode[1:0] = '00'

$$Frame\_frequency = \frac{Fosc}{div \times (rtn + 16) \times (mux + vbp + vfp + 3)}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

for default values of SSD1297
Fosc = ~510KHz, DIV[1:0] = '00', RTN[3:0] = 8, MUX[8:0] = 319, VBP[7:0] = 3, VFP[7:0] = 1,

Frame frequency = $\frac{510K}{1 \times (8+16) \times (319+3+1+3)} = \frac{510K}{1 \times 24 \times 326} = 65Hz$

Power Control 2 (R0Ch) (POR = 0004h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	VCIX2 voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserve
1	1	1	Reserve

Note: The above setting is valid when VCI has high enough voltage supply for boosting up the required voltage. The above setting is assumed 100% booster efficiency. Please refer to DC Characteristics for detail.

Power Control 3 (R0Dh) (POR = 0009h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
POR*		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

VRH[3:0]: Set amplitude magnification of V_{LCD63}. These bits amplify the V_{LCD63} voltage 1.78 to 3.00. times the Vref voltage set by VRH[3:0].

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.810
0	0	0	1	Vref x 2.900
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

*****Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R0Eh) (POR = 3200h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
POR*		0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

VcomG: When VcomG = "1", it is possible to set output voltage of VcomL to any level, and the instruction (VDV4-0) becomes available. When VcomG = "0", VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV[4:0]: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.6 to 1.23 times the VLCD63 voltage. When VcomG = "0", the settings become invalid. External voltage at VcomR is referenced when VDV = "01111".

VCOML = 0.9475*VCOMH - VCOMA

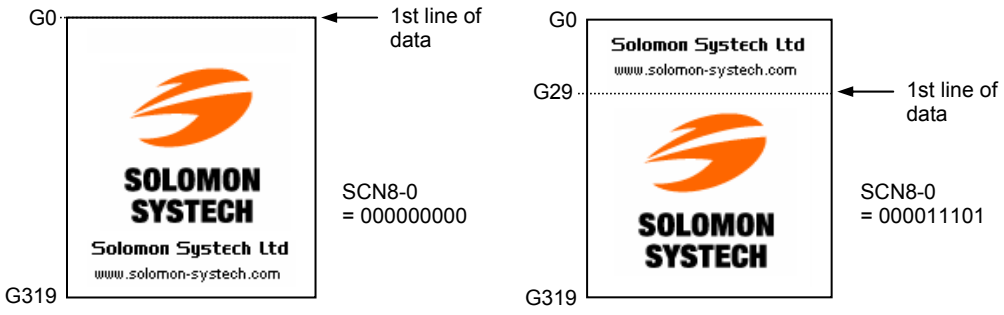
VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
0	0	0	1	0	VLCD63 x 0.66
		: : :			: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reference from external variable resistor
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		: : :			: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note: Vcom amplitude < 6V

Gate Scan Position (R0Fh) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[8:0]: Set the scanning starting position of the gate driver. The valid range is from 0 to 319.



Sleep mode (R10h) (POR = 0001h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

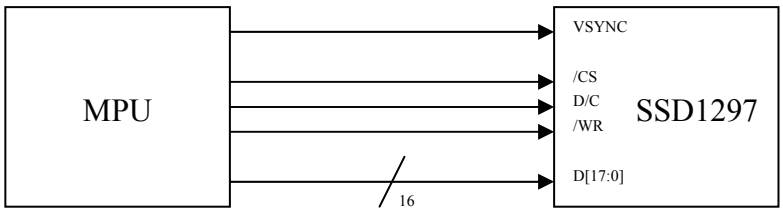
SLP: Sleep mode enable bit. In the sleep mode, the internal display operations are halted except the R-C oscillator to reduce current consumption. No change in the GDDRAM data or instructions during the sleep mode is made, although it is retained.

When SLP = 1, the driver enters into the sleep mode.
When SLP = 0, the driver leaves the sleep mode.

Entry Mode (R11h) (POR = 6230h)

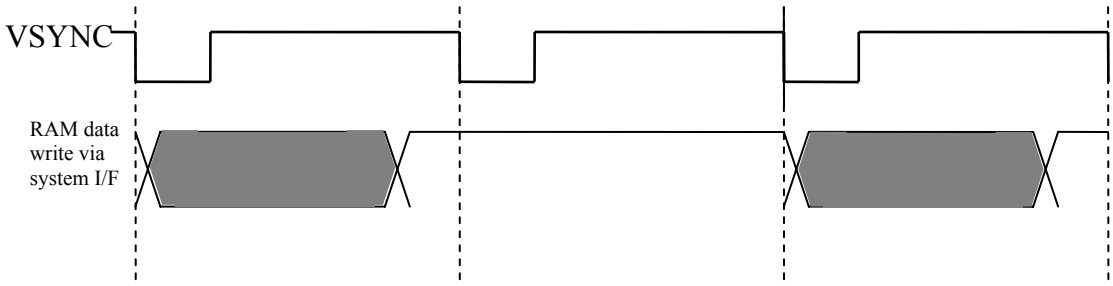
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSMode	DFM1	DFM0	0	DenMode	Wmode	Nosync	Dmode	TY1	TY0	ID1	ID0	AM	0	0	0
POR		0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0

VSMode: When VSMode = 1 at DMode[1:0] = "00", the frame frequency will be dependent on VSYNC.



In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display oerpation speed + buffer), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the SSD1297 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. Therefore, the SSD1297 can write data via VSYNC interface in high speed with low power consumption.



The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Fosc[Hz] = Frame\_frequency * (mux + vfp + vbp + 3) * (rtn + 16) * (div)$$

$$RAMWriteSpeed(min)[Hz] > \frac{240 * mux}{(vbp + mux - marginins) * (rtn + 16) * \frac{1}{fosc}}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

DFM[1:0]: Set the color display mode.

DFM1	DFM0	Color mode
1	1	65k color (POR)
1	0	262k color

DenMode:

DenMode=1 : RGB interface ignore HSYNC, VSYNC pin and HBP, VBP
DenMode=0 : RGB interface control by HSYNC, VSYNC pin and HBP, VBP

When DenMode=1, Generic mode will write each input rgb pixel into RAM buffer, the window of ram buffer to be written defined by command R44h (define X of window)m R45h (define Y start),R46 (define Y end), whenever the input RGB dimension is larger than the defined ram window, it wont have any effect.

WMode:

WMode=1 : Write RAM from Generic RGB data (POR, if PS:00xx)
WMode=0 : Write RAM from SPI interface

Nosync:

Nosync=1 : Dmode change immediately
Nosync=0 : Dmode change Sync with on chip frame start

Dmode:

Dmode=1 : Display engine will be clocked by on chip oscillator and ignore DOTCLK pin
Dmode=0 : Display engine will be clocked by DOTCLK pin and onchip oscillator will be off (POR, if PS:00xx)

TY[1:0]: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.

TY1	TY0	Writing mode
0	0	Type A
0	1	Type B
1	0	Type C

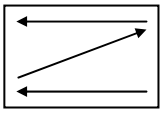
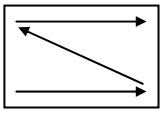
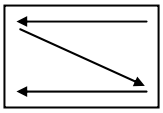
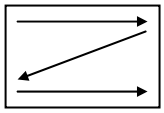
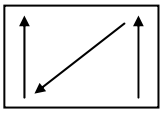
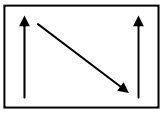
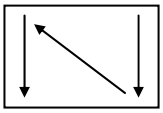
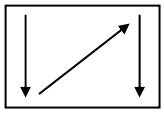
			Hardware pins																	
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16 bit	**262k Type A**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type B	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type C	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	

Remark : x Don't care bits

Not connected pins

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID[1:0] = "1". The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID[1:0] = "0". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = "0", the address counter is updated in the horizontal direction. When AM = "1", the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

	ID[1:0]="00" Horizontal: decrement Vertical: decrement	ID[1:0]="01" Horizontal: increment Vertical: decrement	ID[1:0]="10" Horizontal: decrement Vertical: increment	ID[1:0]="11" Horizontal: increment Vertical: increment
AM="0" Horizontal	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh
AM="1" Vertical	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh

Generic Interface Control (R15h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

INVDOT: sets the signal polarity of DOTCLK pin. When INVDOT = 0, data is latched at positive edge of DOTCLK. When INVDOT = 1, data is latched at negative edge of DOTCLK.

INVDEN: sets the signal polarity of DEN pin. When INVDEN = 0, DEN is active high. When INVDEN = 1, DEN is active low.

INVHS: sets the signal polarity of HSYNC pin. When INVHS = 0, HSYNC is active low. When INVHS = 1, HSYNC is active high.

INVVS: sets the signal polarity of VSYNC pin. When INVVS = 0, VSYNC is active low. When INVVS = 1, VSYNC is active high.

Power Control 5 (R1Eh) (POR = 0029h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nMTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
POR*		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

nMTP: nMTP equals to "0" after power on reset and VcomH voltage equals to programmed MTP value. When nMTP set to "1", setting of VCM[5:0] becomes valid and voltage of VcomH can be adjusted.

VCM[5:0]: Set the VcomH voltage if nMTP = "1". These bits amplify the VcomH voltage 0.36 to 0.99 times the VLCD63 voltage. Default value is "101001" when power on reset.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
			:			: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Write Data to GRAM (R22h)

R/W	DC	D[17:0]
W	1	WD[17:0] mapping depends on the interface setting

WD[17:0]: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD1297 selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

R/W	DC	D[17:0]
R	1	RD[17:0] mapping depends on the interface setting

RD[17:0]: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

Frame Frequency Control (R25h) (POR = 8000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
POR*		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSC[3:0]: Set the frame frequency by OSC[3:0]

OSC[3:0]	Internal Oscillator Frequency (Hz)	Corresponding Frame Freq (Hz) (other registers are at POR value)
0000	390K	50
0010	430K	55
0101	470K	60
1000	510K	65
1010	548K	70
1100	587K	75
1110	626K	80

Vcom MTP (R28h – R29h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R29h	W	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

When MTP is access, these registers must be set accordantly.

MTP programming sequence

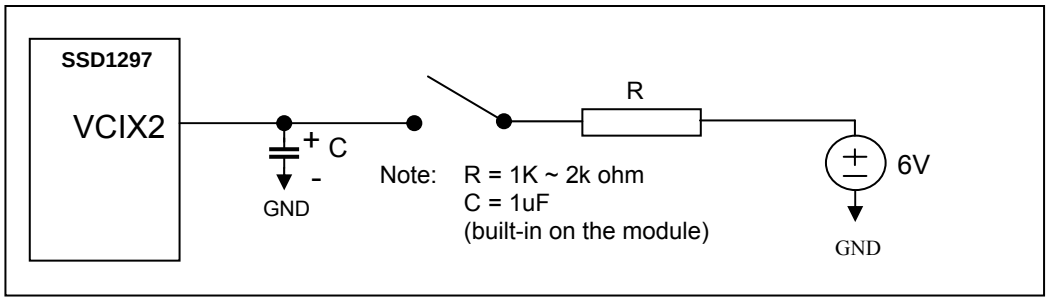
<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power up the module at VCI = 2.8V, VDDEXT = VDDIO = 1.8V.
Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any).</td></tr>
<tr><td>2</td><td>Set nMTP to “1” (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh).</td></tr>
<tr><td>3</td><td>Power down the whole module.</td></tr>
<tr><td>4</td><td>Connect a supply to the module at VCI = 2.8V, VDDEXT = VDDIO = 1.8V</td></tr>
<tr><td>5</td><td>Write below commands for OTP initialization and wait for 200ms for activate the MTP :
<table>
<tr><th>Index</th><th>Value</th></tr>
<tr><td>R00h</td><td>0x0001</td></tr>
<tr><td>R28h</td><td>0x0006</td></tr>
<tr><td>R03h</td><td>0x6664</td></tr>
<tr><td>R29h</td><td>0x80C0</td></tr>
</table>
Connect a 6V supply to VCIX2 and 0V to VSS/GND, see figure below.</td></tr>
<tr><td>6</td><td>Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nMTP to “1”.</td></tr>
<tr><td>7</td><td>Fire the MTP by write HEX code “000Ah” to register R28h.</td></tr>
<tr><td>8</td><td>Wait 600ms.</td></tr>
<tr><td>9</td><td>MTP complete. Power down the whole module and remove 6V VCIX2 supplies.</td></tr>
</table>

Note: nMTP must set to “0” to activate the MTP effect.

Precaution:

1. All capacitors on MTP machine should be discharged completely before placing the LCD module.
2. The MTP programming voltage should not be applied when placing and removing the LCD module.
3. The MTP programming voltage should not be applied before VDDIO/VDDEXT/VCI.
4. After MTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.

Figure 9-3 MTP circuitry



Gamma Control (R30h to R3Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30h	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: please refer to table 5 for POR values.

PKP[52:00]: Gamma micro adjustment register for the positive polarity output

PRP[12:00]: Gradient adjustment register for the positive polarity output

VRP[14:00]: Adjustment register for amplification adjustment of the positive polarity output

PKN[52:00]: Gamma micro adjustment register for the negative polarity output

PRN[12:00]: Gradient adjustment register for the negative polarity output

VRN[14:00]: Adjustment register for the amplification adjustment of the negative polarity output.
(For details, see the Section 11 Gamma Adjustment Function).

Vertical Scroll Control (R41h-R42h) (POR =0000h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R41h	W	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	W	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VL1[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 320th can be scrolled for the number of the raster-row. After 320th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1[8:0]) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE[2:1] = "00".

VL2[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL2[8:0]) is valid when VLE1 = "1" and VLE2 = "1".

Horizontal RAM address position (R44h) (POR = EF00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
POR		1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0

HSA[7:0]/HEA[7:0]: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by HEA[7:0] and HSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ HSA[7:0] ≤ HEA[7:0] ≤ "EF"h.

Vertical RAM address position (R45h-R46h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R45h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

VSA[8:0]/VEA[8:0]: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by VEA[8:0] and VSA[8:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ VSA[8:0] ≤ VEA[8:0] ≤ "13F"h.

1st Screen driving position (R48h-R49h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R48h	W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

SS1[8:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set gate driver, i.e. the first driving Gate is G0 if SS1[8:0] = 00H

SE1[8:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SS1[8:0] = "07"H and SE1[8:0] = "10"H are set, the LCD driving is performed from G7 to G16, and non-selection driving is performed for G1 to G6, G17, and others. Ensure that SS1[8:0] ≤ SE1[8:0] ≤ 13FH.

2nd Screen driving position (R4Ah-R4Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Ah	W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

SS2[8:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set gate driver. The second screen is driven when SPT = "1".

SE2[8:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SPT = "1", SS2[8:0] = "20"H, and SE2[8:0] = "2F"H are set, the LCD driving is performed from G32 to G47. Ensure that SS1[8:0] ≤ SE1[8:0] ; SS2[8:0] ≤ SE2[8:0] ≤ 13FH.

RAM address set (R4Eh-R4Fh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Eh	W	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	W	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD 3	YAD 2	YAD 1	YAD 0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

XAD[7:0]: Make initial settings for the GDDRAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the GDDRAM Y address in the address counter (AC).

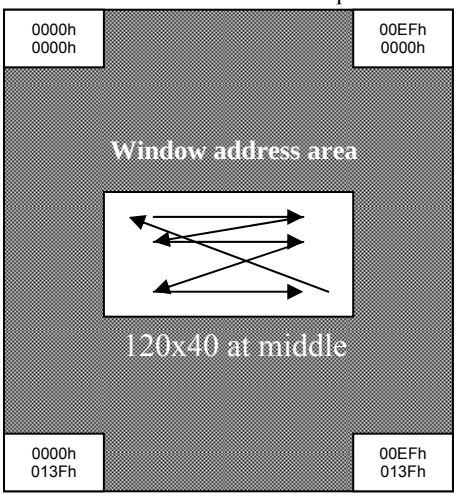
After GDDRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM. GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Window Address Function

The window address function enables writing display data sequentially in a window address area made in the internal GDDRAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and ID[1:0] bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the SSD1297 to write data including image data sequentially without taking the data wrap position into account. The window address area must be made within the GDDRAM address map area.

Condition:
00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ EFh
00h ≤ VSA[8:0] ≤ VEA[8:0] ≤ 13Fh
AM and ID[1:0] refer to R11h

GDDRAM address map

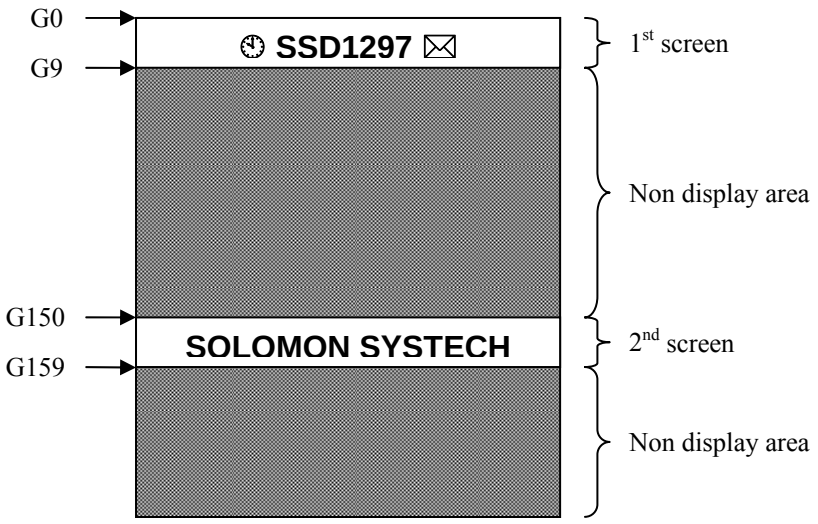


Window address setting area:
HSA[7:0] = 3Bh; HEA[7:0] = B3h
VSA[8:0] = 8Bh; VEA[8:0] = B3h
AM = “0” and ID[1;]] = “11”

Partial Display Mode

The SSD1297 enables to selectively drive two screens at arbitrary positions with the screen-driving position registers (R48h to R4Bh). Only the lines required to display two screens at arbitrary positions are selectively driven to reduce the power consumption.
The first screen driving position registers (R48 and R49) specifies the start line (SS18-10) and the end line (SE18-10) for displaying the first screen. The second screen driving position register (R4A) specifies the start line (SS28-20) and the end line (SE28-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of lines driven for displaying the first and second screens must be less than the number of lines to drive the LCD.

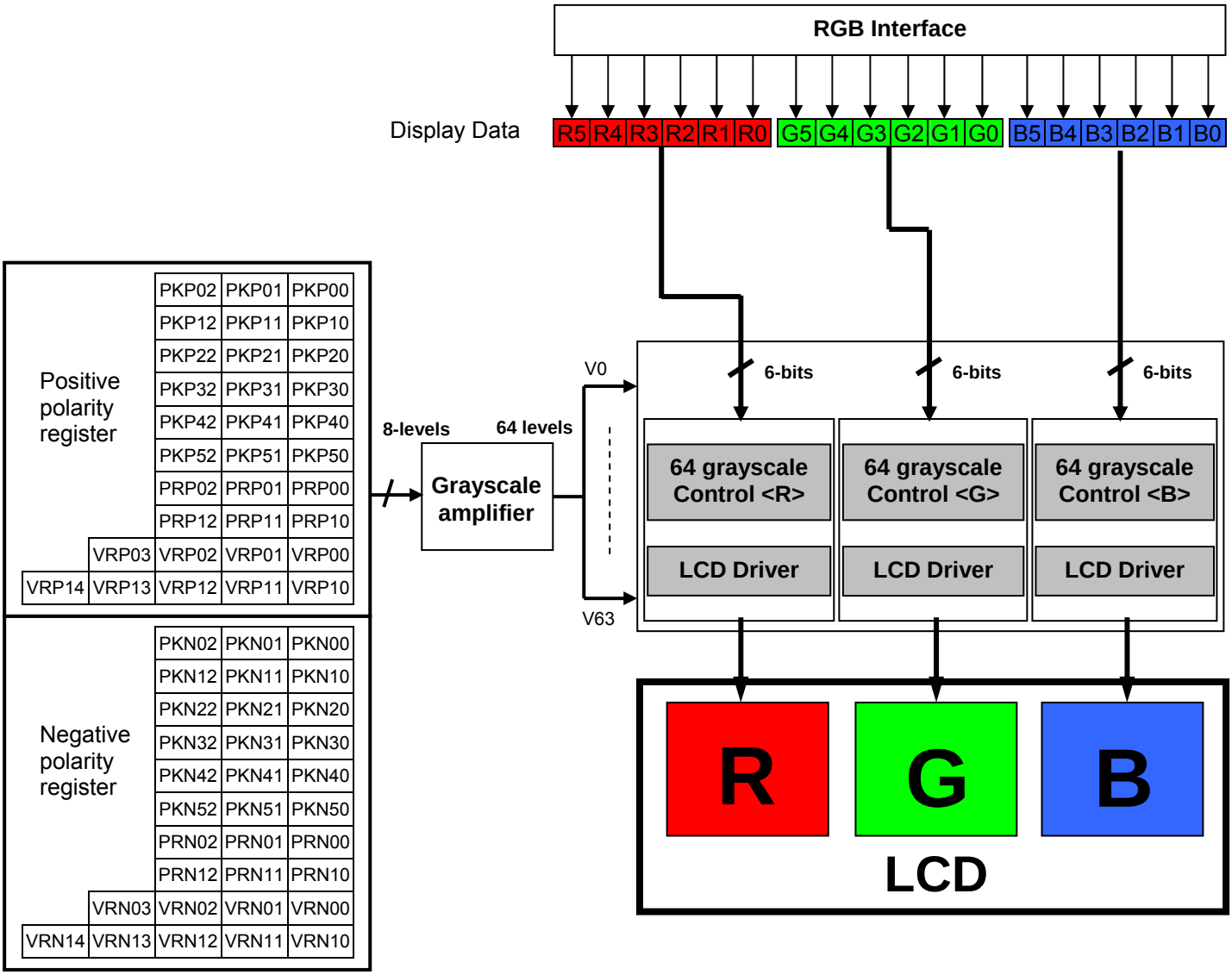
Condition:
SS1[8:0] ≤ SE1[8:0] ≤ 13FH
SS1[8:0] ≤ SE1[8:0]
SS2[8:0] ≤ SE2[8:0] ≤ 13FH



The number of driven display lines: MUX[8:0] = 13F (319+1 lines)
1st screen setting: SS[18:10] = 00h, SE[18:10] = 09h
2nd screen seeting: SS[28:10] = 96h, SE[28:10] = 9Fh

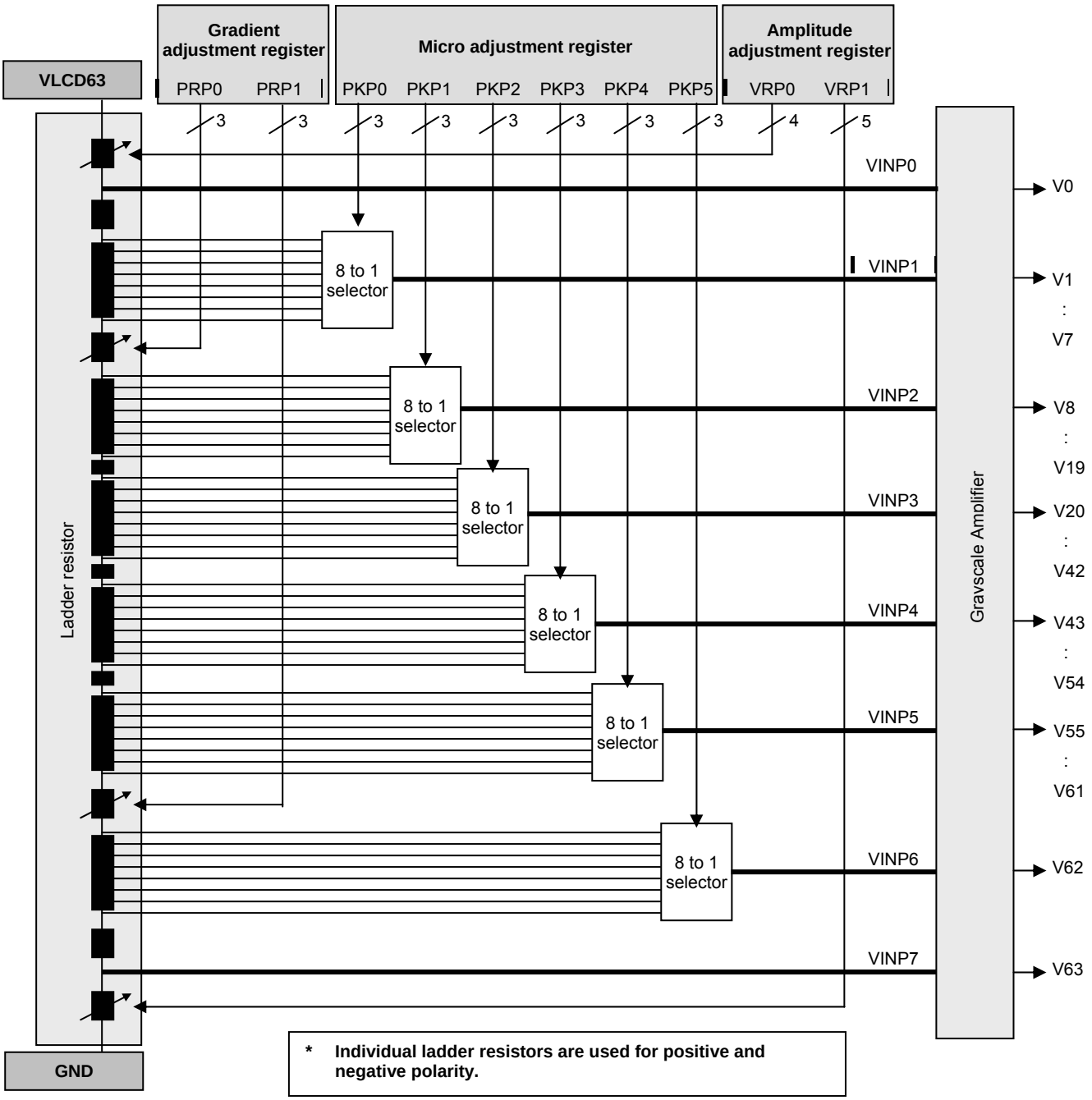
10. GAMMA ADJUSTMENT FUNCTION

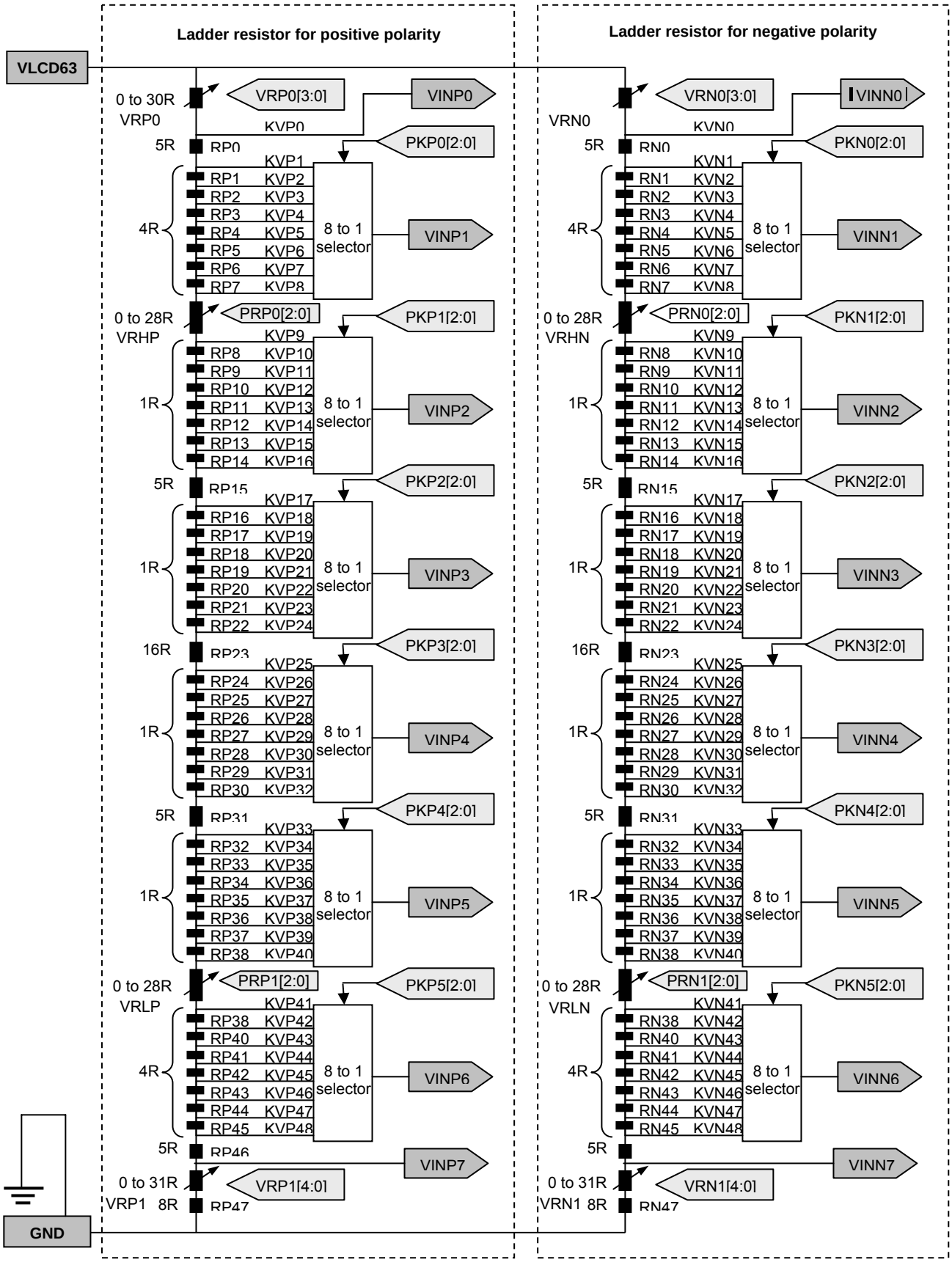
The SSD1297 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.



10.1Structure of Grayscale Amplifier

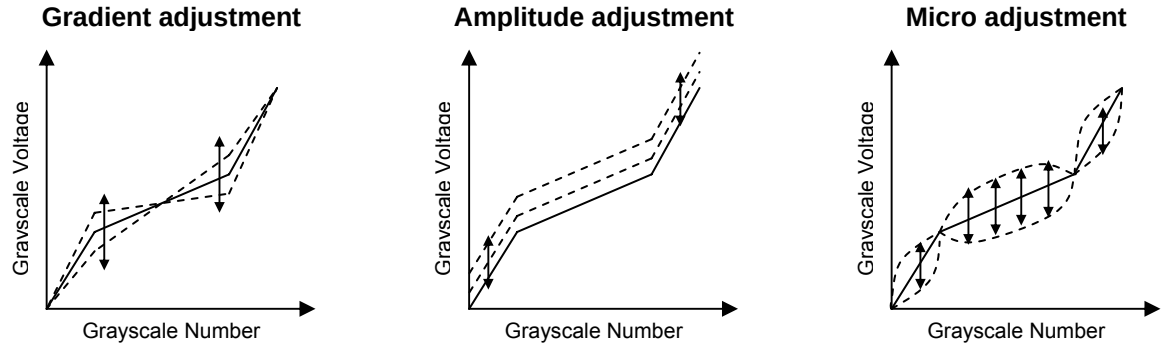
Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.




Ladder resistor for positive polarity
Ladder resistor for negative polarity
VLCD63
GND
0 to 30R
VRP0
5R
4R
1R
16R
0 to 28R
VRHP
VRLP
0 to 31R
VRP1
8R
VRP0[3:0]
VINP0
PKP0[2:0]
VINP1
PRP0[2:0]
PKP1[2:0]
VINP2
PKP2[2:0]
VINP3
PKP3[2:0]
VINP4
PKP4[2:0]
VINP5
PRP1[2:0]
PKP5[2:0]
VINP6
VINP7
VRP1[4:0]
VRN0
VRHN
VRLN
VRN1
VRN0[3:0]
VINN0
PKN0[2:0]
VINN1
PRN0[2:0]
PKN1[2:0]
VINN2
PKN2[2:0]
VINN3
PKN3[2:0]
VINN4
PKN4[2:0]
VINN5
PRN1[2:0]
PKN5[2:0]
VINN6
VINN7
VRN1[4:0]
8 to 1 selector

10.2Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.



10.2.1Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

10.2.2Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

10.2.3Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

10.3Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Postive polarity							Negative polarity						
Registor	Selected voltage						Registor	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(21/23)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(20/23)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(19/23)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(18/23)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(17/23)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(16/23)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(15/23)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(14/23)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(13/23)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(12/23)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(11/23)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(10/23)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(9/23)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(8/23)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(7/23)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(6/23)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(5/23)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(4/23)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(3/23)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(2/23)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(1/23)		
V21	V43+(V20-V43)*(22/23)	V43	VINP(N)4		

Reference voltage of positive polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63-ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1

ΔV: Voltage difference between VLCD63 and of GND.

Reference voltage of negative polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63-ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV: Voltage difference between VLCD63 and of GND.

11. MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDDIO	Supply Voltage	-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DDIO} and V_{SS}	25	mA
T_A	Operating Temperature	-20 to +70	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range $VSS < VDDIO \le VCI < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12. DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.65 to 3.6V, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF

R_{SON}	Source drivers output resistance			-	1	-	kΩ
R_{GON}	Gate drivers output resistance			-	5	-	kΩ
R_{CON}	Vcom output resistance			-	200	-	Ω
I_{dp}(262k)	Display current for 262k	Vddio= 1.8V, Vci = 2.8V. 5x/-5x booster ratio. Full color current consumption, without panel loading	Ivdd	-	150	300	uA
			Ivci	-	2.5	8	mA
I_{dp}(8 color)	Display current for 8 color mode	Current consumption for 8 color partial display, without panel loading	Ivdd	-	120	300	µA
			Ivci	-	1	5	mA
I_{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode), R00-0000 (stop osc)	Ivdd	-	30	100	µA
			Ivci	-	40	200	µA

Remark: Ivdd = Ivddio

13. AC CHARACTERISTICS

Table 13-1 Parallel 6800 Timing Characteristics

(T_A = -20 to 70°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

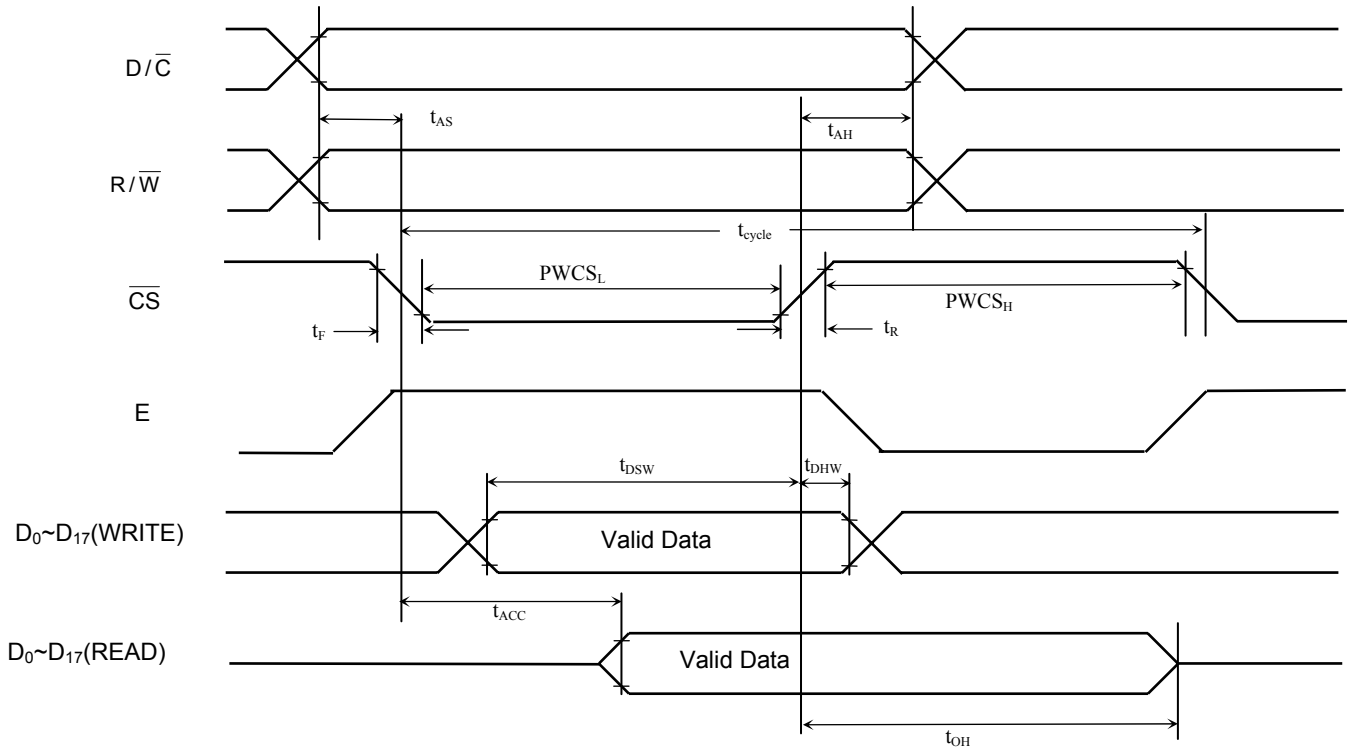


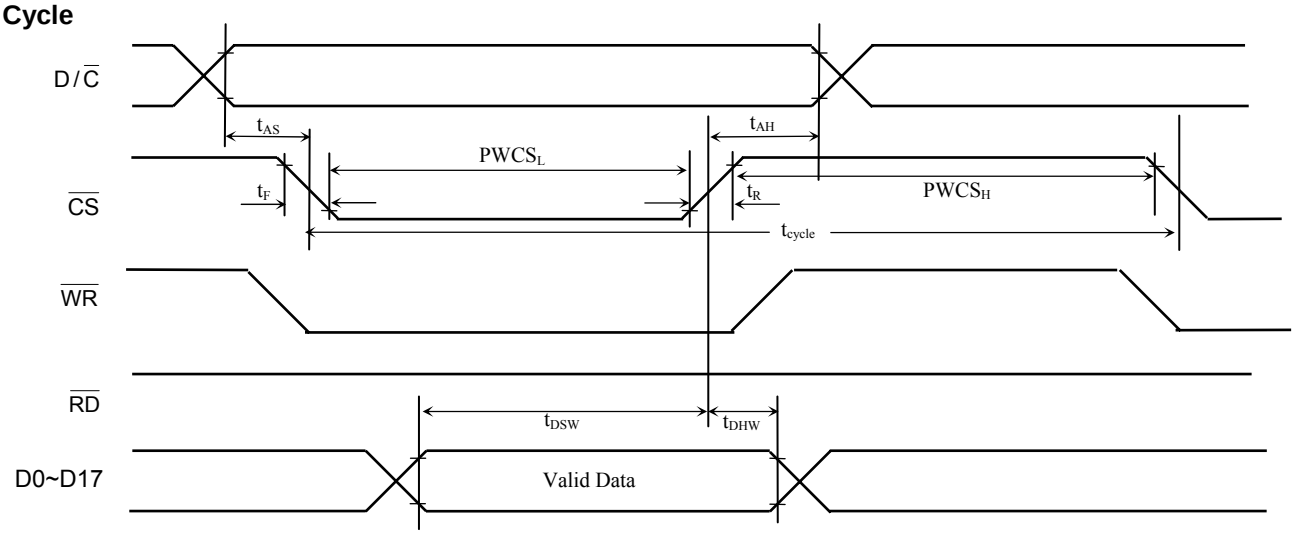
Figure 13-1 Parallel 6800-series Interface Timing Characteristics

Table 13-2 Parallel 8080 Timing Characteristics

(T_A = -20 to 70°C, V_{DDIO} = 1.65V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse Width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse Width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse Width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse Width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Write Cycle



Read Cycle

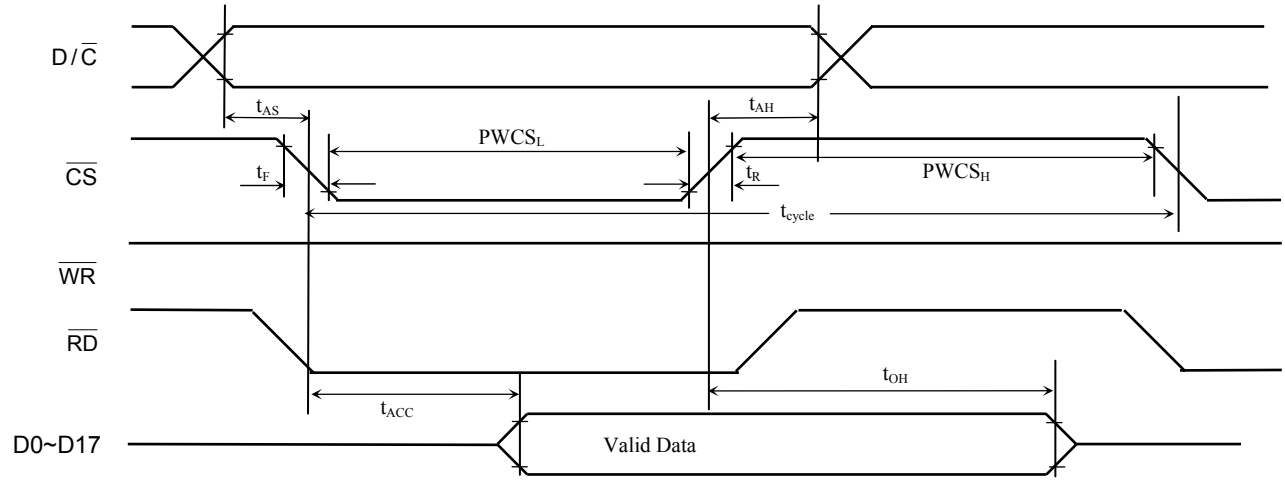


Figure 13-2 Parallel 8080-series Interface Timing Characteristics

Table 13-3 Serial Timing Characteristics

(T_A = -20 to 70°C, V_{DDIO} = 1.65V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	13	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

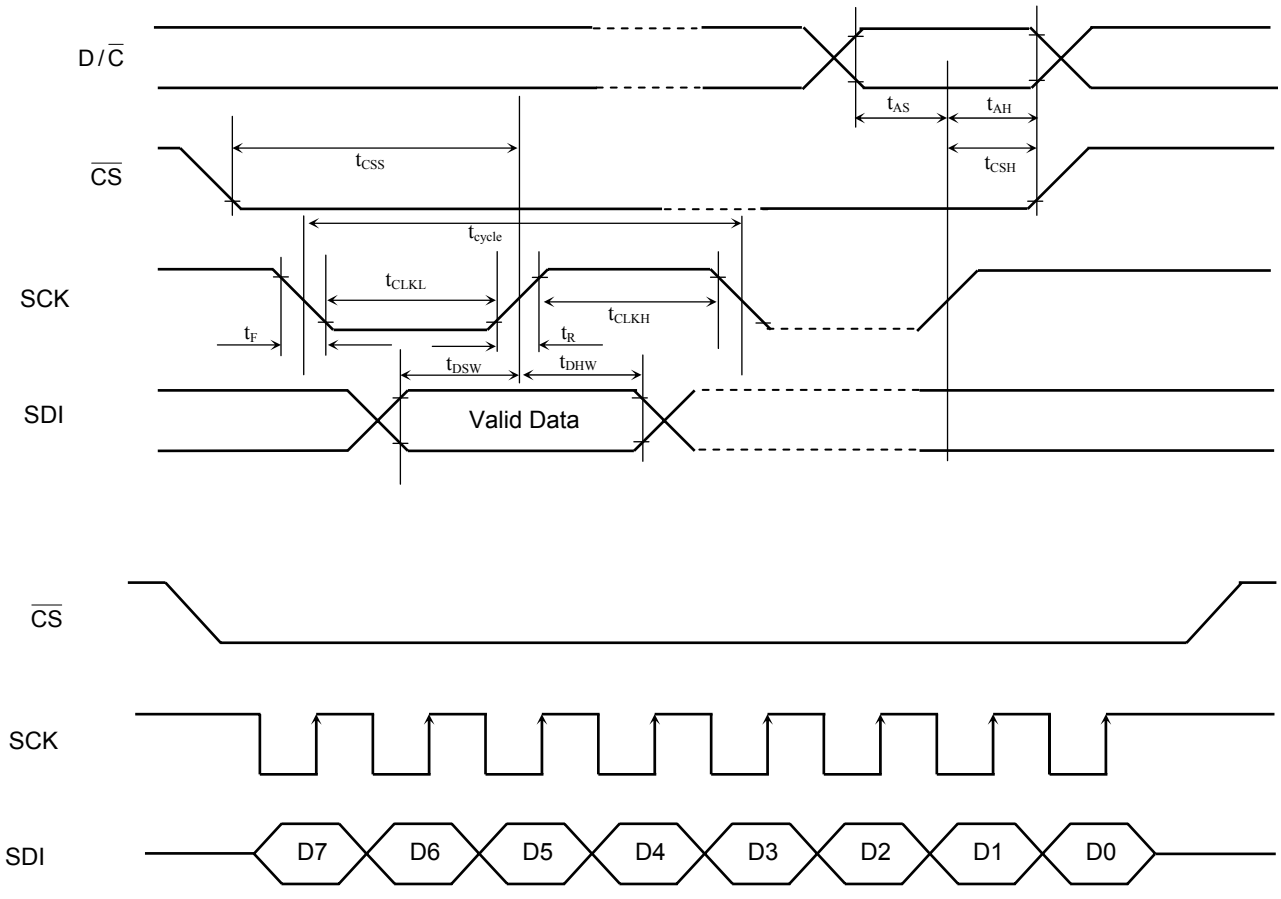


Figure 13-3 4 wire Serial Timing Characteristics

14. GDDRAM Address

	RL=1	S0	S1	S2	S3	S4	S5	S6	S7	S8	…	S714	S715	S716	S717	S718	S719	
	RL=0	S719	S718	S717	S716	S715	S714	S713	S712	S711	…	S5	S4	S3	S2	S1	S0	
	BGR=0	R	G	B	R	G	B	R	G	B	…	R	G	B	R	G	B	Vertical address
	BGR=1	B	G	R	B	G	R	B	G	R	…	B	G	R	B	G	R	
TB=1	TB=0																	
G0	G319	0000H,0000H			0000H, 0001H			0000H, 0010H			…	0000H, 00EEH			0000H, 00EFH			0
G1	G318	0001H,0000H			0001H, 0001H			0001H, 0010H			…	0001H, 00EEH			0001H, 00EFH			1
G2	G317	0010H,0000H			0010H, 0001H			0010H, 0010H			…	0010H, 00EEH			0010H, 00EFH			2
G3	G316	0011H,0000H			0011H, 0001H			0011H, 0010H			…	0011H, 00EEH			0011H, 00EFH			3
G4	G315	0100H,0000H			0100H, 0001H			0100H, 0010H			…	0100H, 00EEH			0100H, 00EFH			4
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
G316	G3	013CH, 0000H			013CH, 0001H			013CH, 0010H			…	013CH, 00EEH			013CH, 00EFH			316
G317	G2	013DH, 0000H			013DH, 0001H			013DH, 0010H			…	013DH, 00EEH			013DH, 00EFH			317
G318	G1	013EH, 0000H			013EH, 0001H			013EH, 0010H			…	013EH, 00EEH			013EH, 00EFH			318
G319	G0	013FH, 0000H			013FH, 0001H			013FH, 0010H			…	013FH, 00EEH			013FH, 00EFH			319

Horizontal address	0	1	2	…	238	239

Remark : The address is in 00xxH,0yyyH format, where yyy is the vertical address and xx is the horizontal address

15. INTERFACE MAPPING

15.1 Interface Setting

Table 15-1 Interface setting and data bus setting

PS3	PS2	PS1	PS0	Interface Mode	Data bus
0	0	0	0	16-bit, 8080 parallel, 65K color	D[15:0]
0	0	0	1	16-bit, 8080 parallel, 262K color (TypeA)	D[15:0]
0	0	1	0	18-bit, 8080 parallel, 262K color	D[17:0]
0	0	1	1	8-bit, 8080 parallel, 262K color	D[7:0]
0	1	0	0	16-bit, 8080 parallel, 262K color	D[15:0]
0	1	0	1	18-bit, 8080 parallel, 262K color	D[17:0]
1	0	0	0	16-bit, 6800 parallel, 65K color	D[15:0]
1	0	0	1	16-bit, 6800 parallel, 262K color(TypeA)	D[15:0]
1	0	1	0	18-bit, 6800 parallel, 262K color	D[17:0]
1	0	1	1	8-bit, 6800 parallel, 262K color	D[7:0]
1	1	0	0	16-bit, 6800 parallel, 262K color	D[15:0]
1	1	0	1	18-bit, 6800 parallel, 262K color	D[17:0]

15.1.1 6800-series System Bus Interface

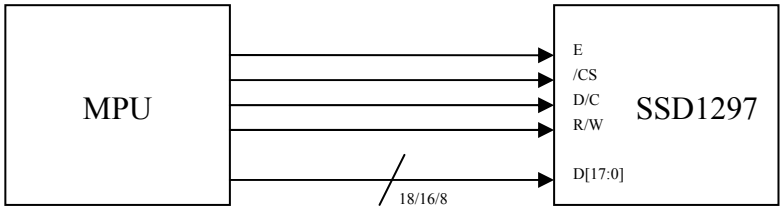


Table 15-2 The Function of 6800-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	R/W	E	D/C	/CS	Operation
1	0	0	0	16-bit 6800 parallel interface	D[15:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
1	0	0	1			0	↴	0	0	Write 8-bit command
1	1	0	0			0	↴	1	0	Write 16-bit display data
1	0	1	0	18-bit 6800 parallel interface	D[17:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
1	1	0	1			0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 18-bit display data
1	0	1	1	8-bits 6800 parallel interface	D[7:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 8-bit display data

* A dummy read is required before the first actual display data read

15.1.2 8080-series System Bus Interface

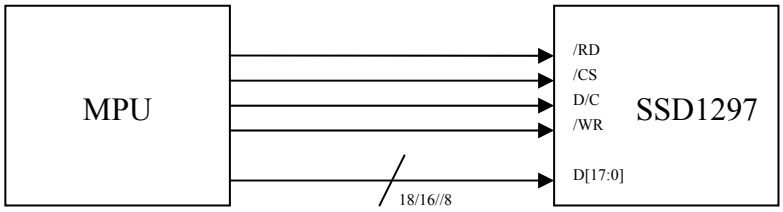


Table 15-3 The Function of 8080-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	/WR	/RD	D/C	/CS	Operation
0	0	0	0	16-bit 8080 parallel interface	D[15:0]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
0	0	0	1			0	1	0	0	Write 8-bit command
0	1	0	0			0	1	1	0	Write 16-bit display data
0	0	1	0	18-bit 8080 parallel interface	D[17:0]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
0	1	0	1			0	1	0	0	Write 8-bit command
						0	1	1	0	Write 18-bit display data
0	0	1	1	8-bit 8080 parallel interface	D[7:0]	0	1	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 8-bit display data

* A dummy read is required before the first actual display data read

15.2Mapping for Writing an Instruction

		Hardware pins																	
Interface	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits		X	X	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
16 bits		X	X	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
8 bits	1st	X	X	X	X	X	X	X	X	X	X	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
	2nd	X	X	X	X	X	X	X	X	X	X	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

X - Don't care bits

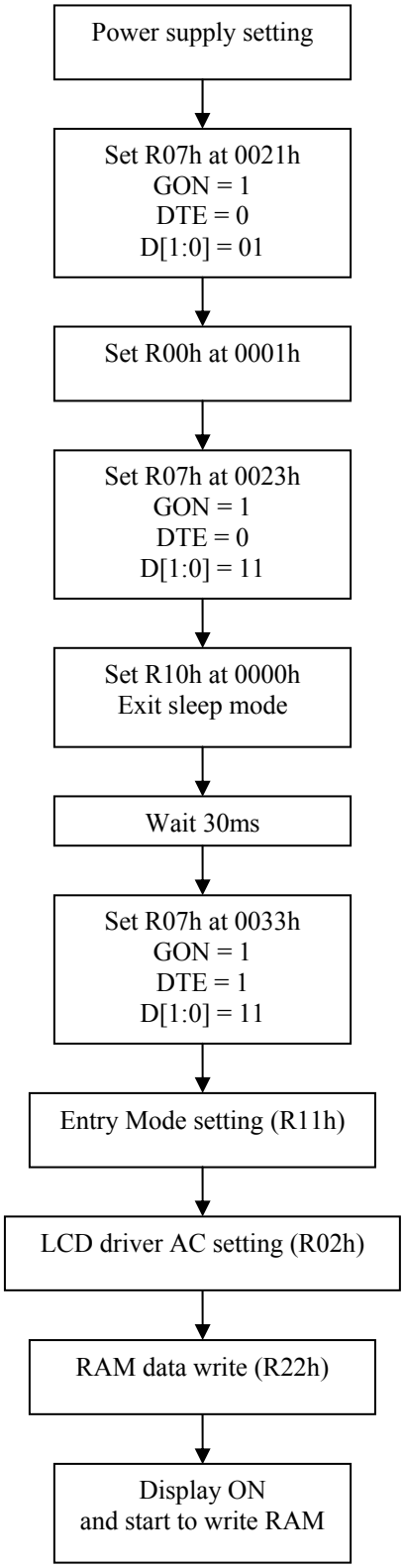
15.3Mapping for Writing Pixel Data

				DB pins (D[17:0])																			
Mode	**Interface**	**Color Mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**SCL**	**SDI/O**
Parallel	18 bits	262K	N/A	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0		
	16 bits	262K Type A	1st	X	X	R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X		
			2nd	X	X	B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X		
			3rd	X	X	G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X		
		262K Type B	1st	X	X	R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X		
			2nd	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0	X	X		
		262K Type C	1st	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2		
			2nd	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B1	B0		
		65K	N/A	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0		
	8 bits	262K	1st	X	X	X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	X	X		
			2nd	X	X	X	X	X	X	X	X	X	X	G5	G4	G3	G2	G1	G0	X	X		
			3rd	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0	X	X		
Serial	3-wire	Any	N/A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	√	√
	4-wire	Any	N/A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	√	√
Generic	18 bits	262K	N/A	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	√	√
		65K	N/A	R4	R3	R2	R1	R0	X	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	X	√	√

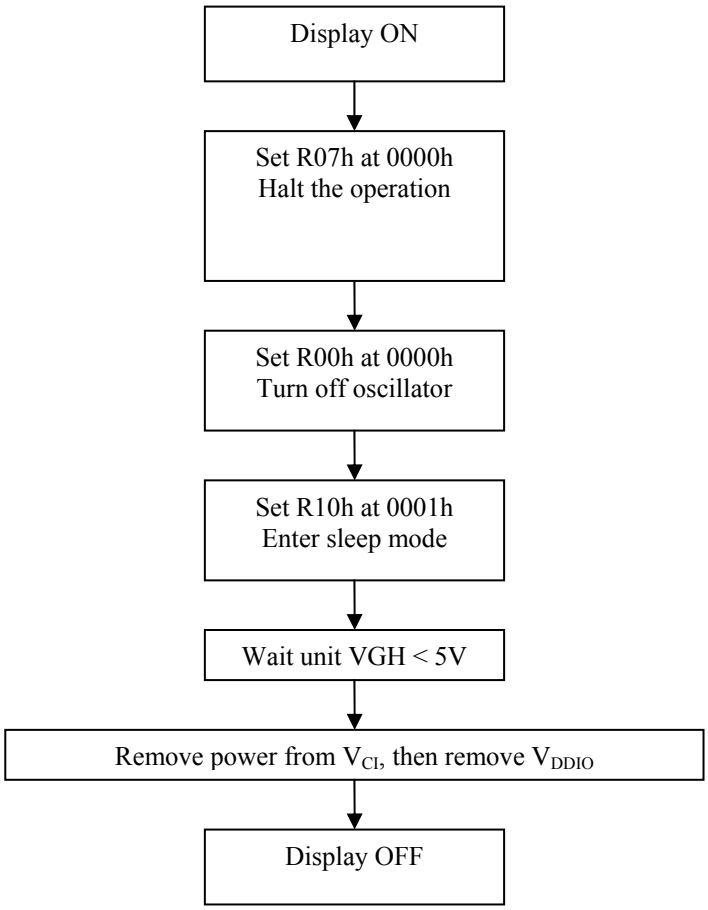
Legend: X - don't care

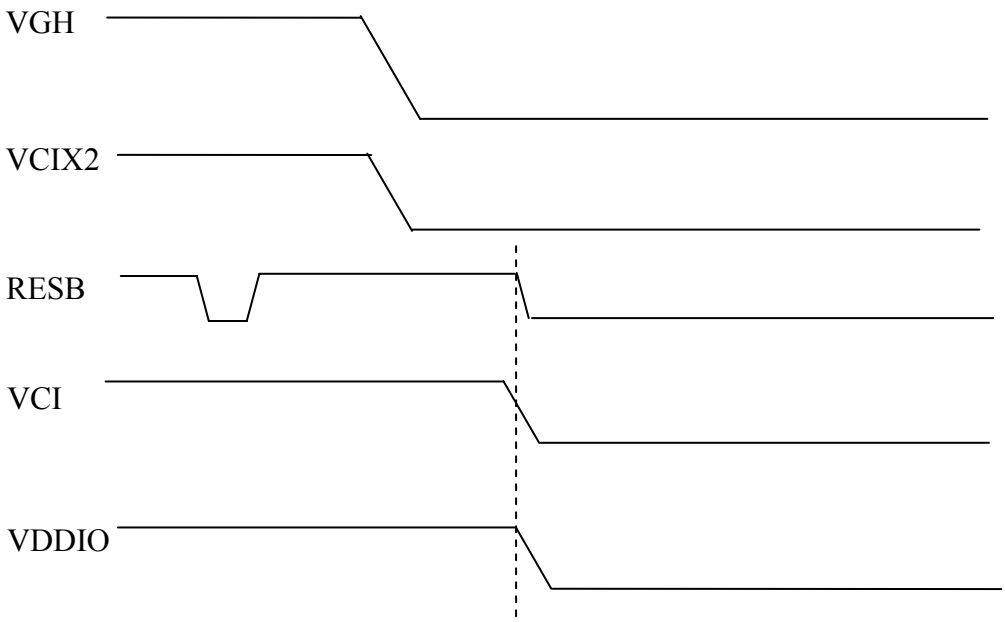
16. DISPLAY SETTING SEQUENCE

16.1Display ON Sequence



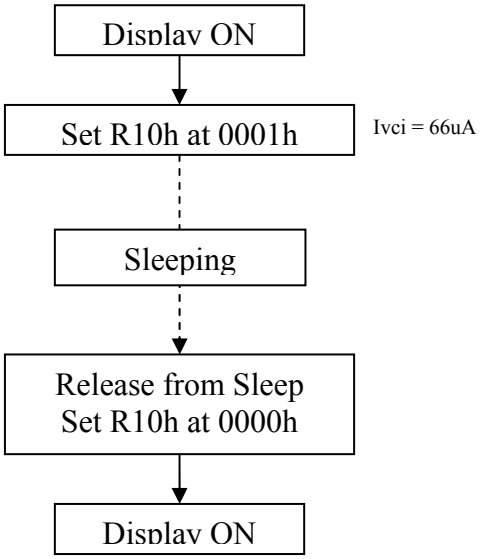
16.2Display OFF Sequence



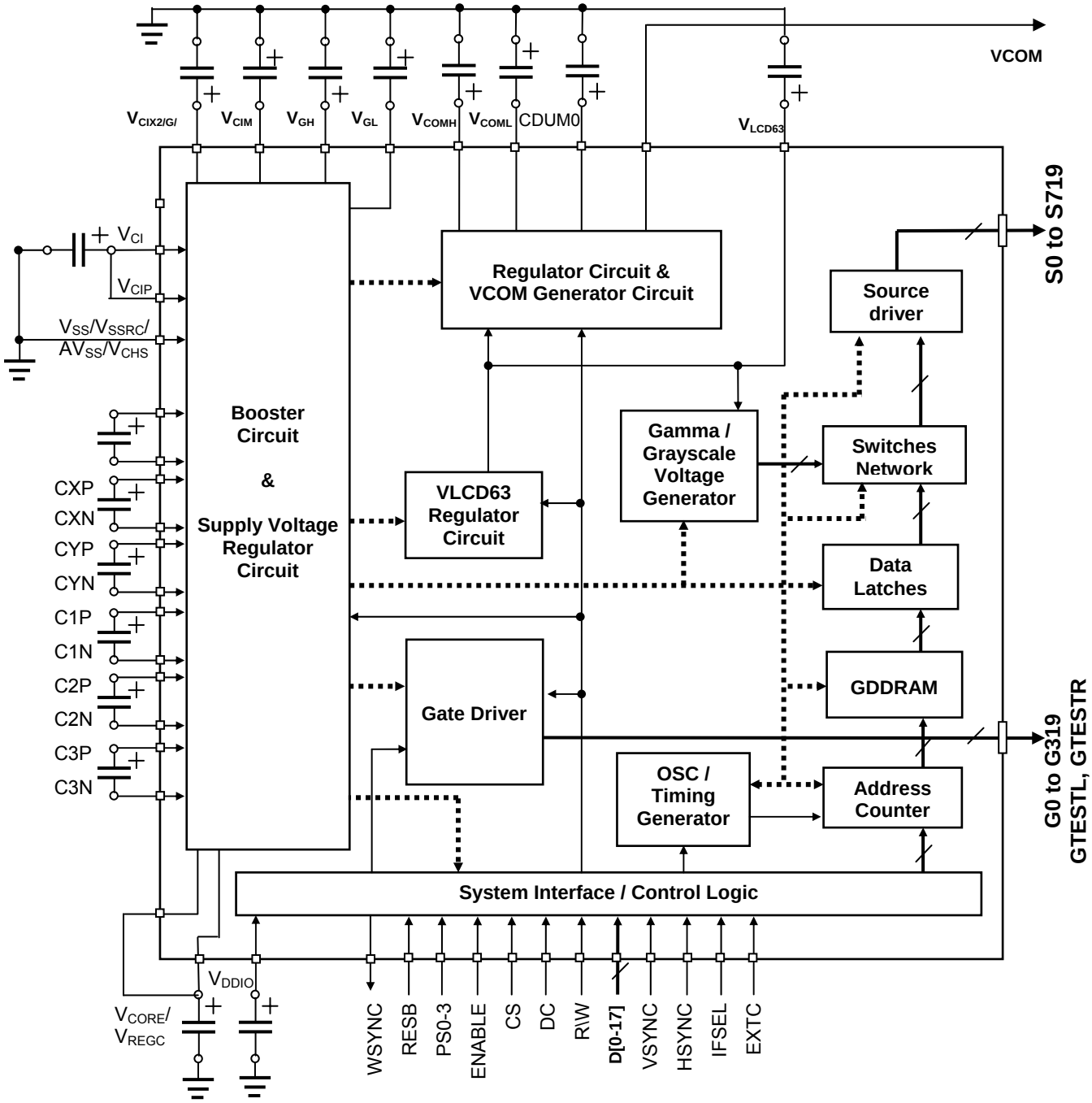


Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the MTP programming voltage should be turned off and capacitors at VGH and VCIX2 discharged before VCI/VDDIO are turned off.

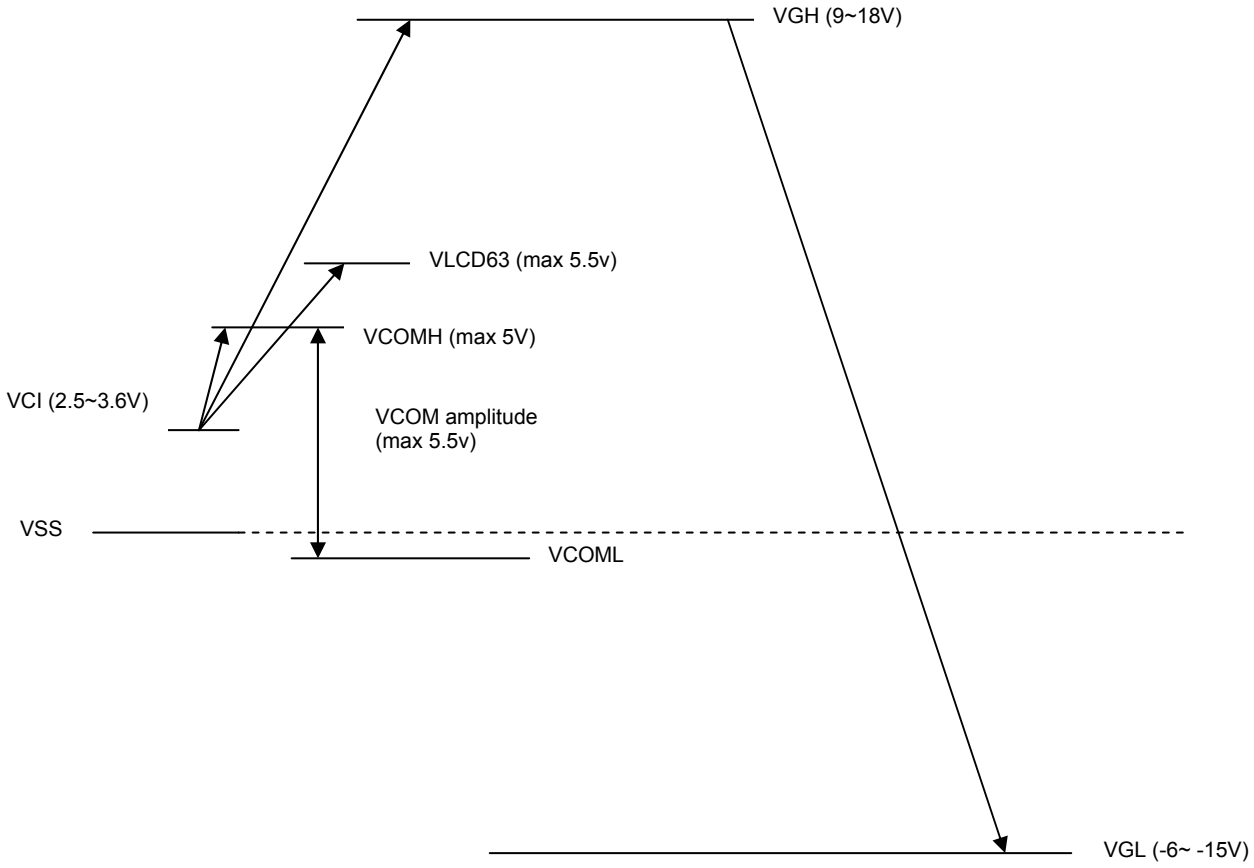
16.3Sleep Mode Display Sequence



17. POWER SUPPLY BLOCK DIAGRAM



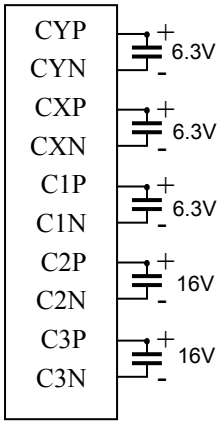
18. SSD1297OUTPUT VOLTAGE RELATIONSHIP



Note: VGH-VGL<30V_{p-p}

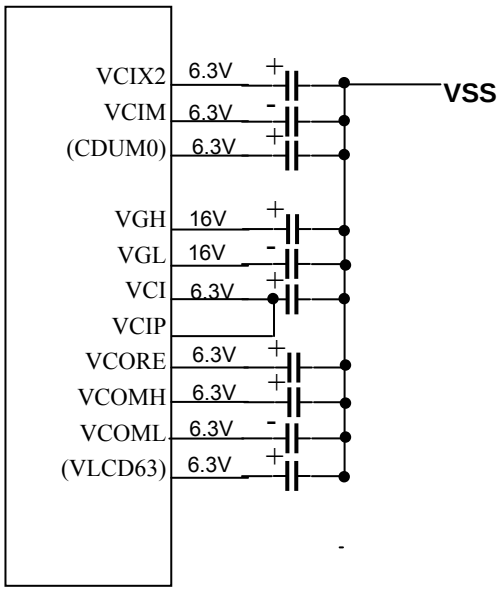
19. APPLICATION CIRCUIT

Figure 19-1 Booster Capacitors



All capacitors
0.1 ~ 0.22uF (0.22uF for better stability)

Figure 19-2 Filtering and Charge Sharing Capacitors



Mandatory requirement on external components for SSD1297 is 10 capacitors.
VCIX2, VCIM, VGH, VGL, VCI, VCORE, VCOMH, VCOML
C1P/C1N, C2P/C2N, C3P/C3N, CYP/CYN, CXP/CXN

Remark:
Capacitor for VCIX2 = 2.2uF
VCI should be separated with VCIP at ITO layout to provide noise free path.
VSS should be separated with VCHS, AVSS and VSSRC at ITO layout to provide noise free path.
All other capacitors 1.0uF ~ 2.2uF (2.2uF is preferred for better display quality and power consumption.)

(Optional capacitors)
VLCD63, capacitors are for stability
Capacitors on CDUM0 are for power saving.

Figure 19-3 Panel Connection Example

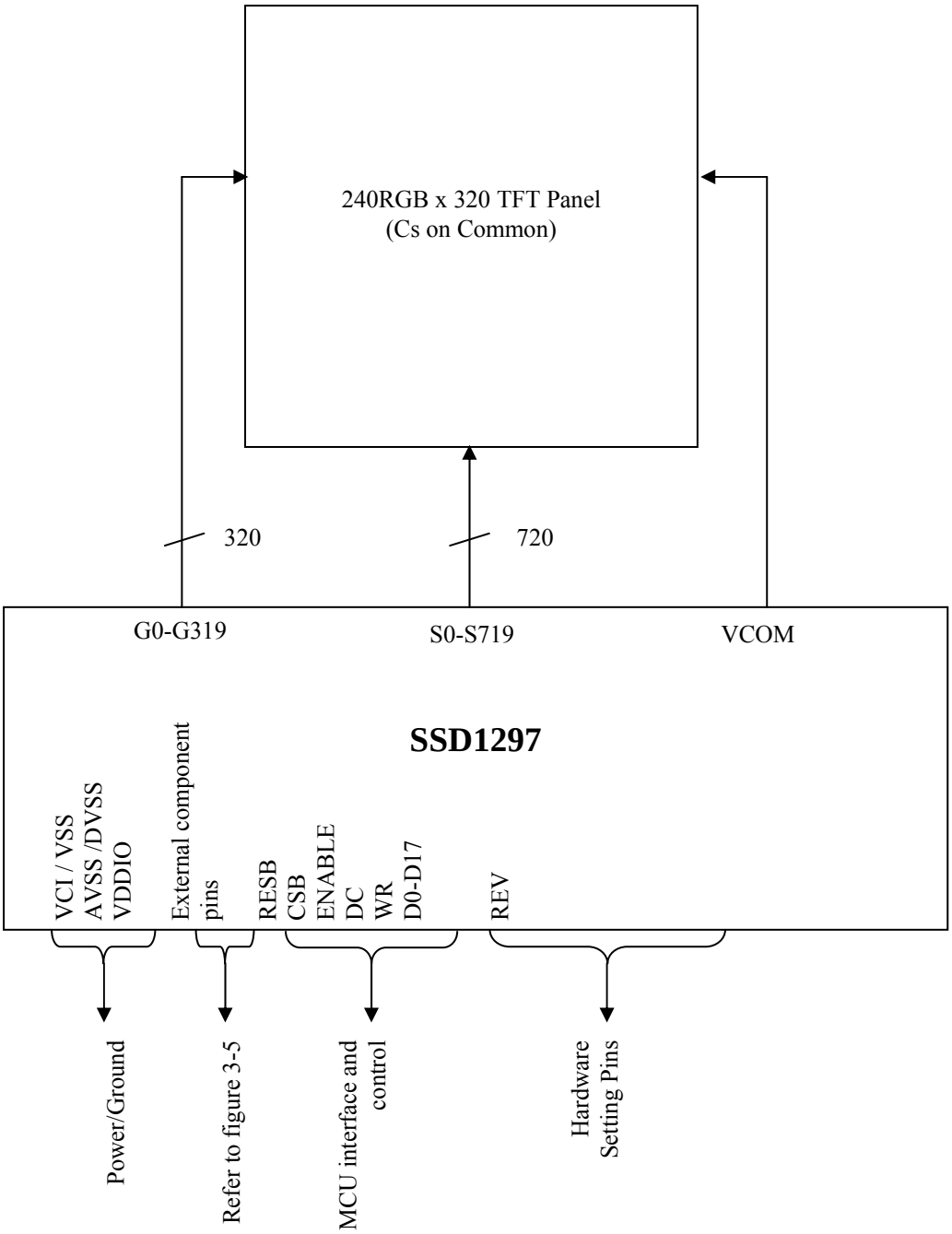
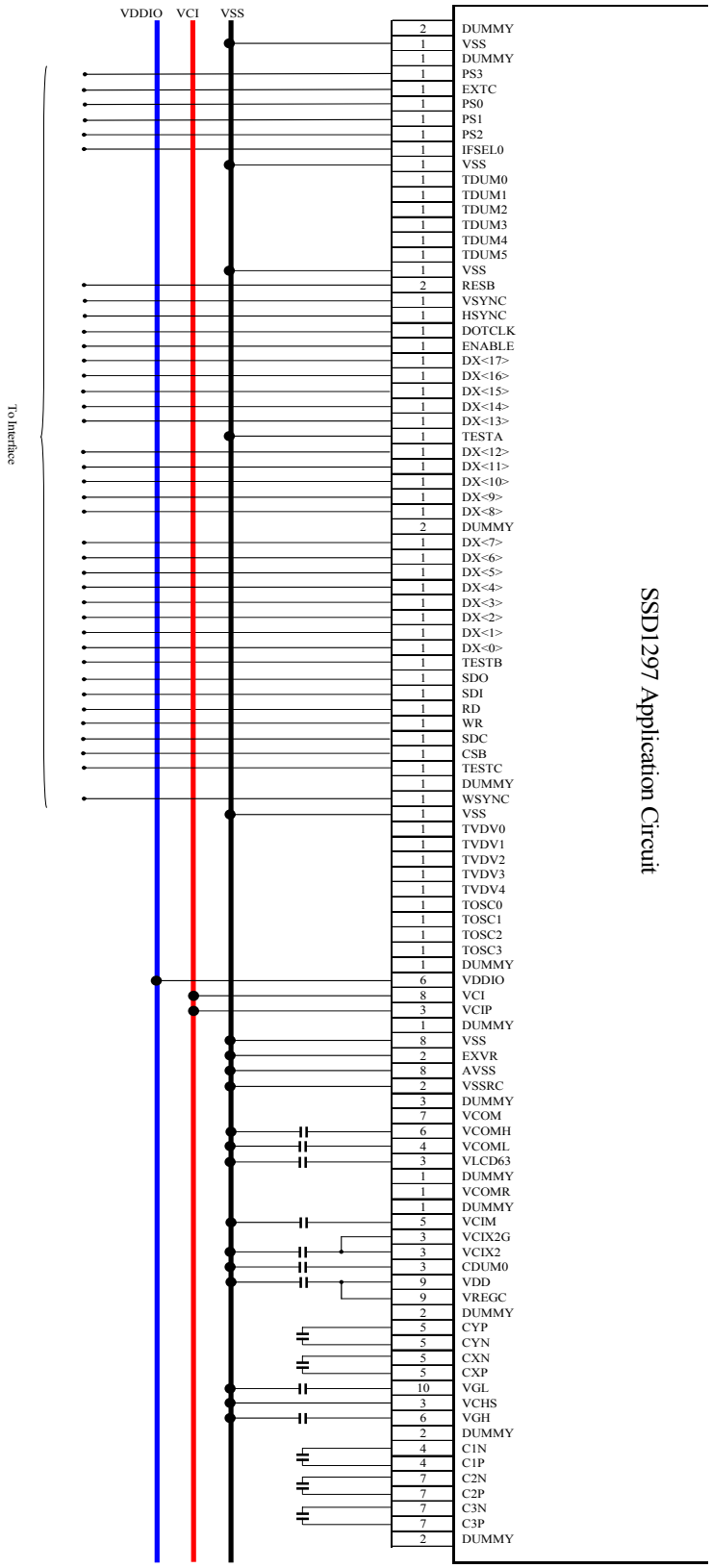
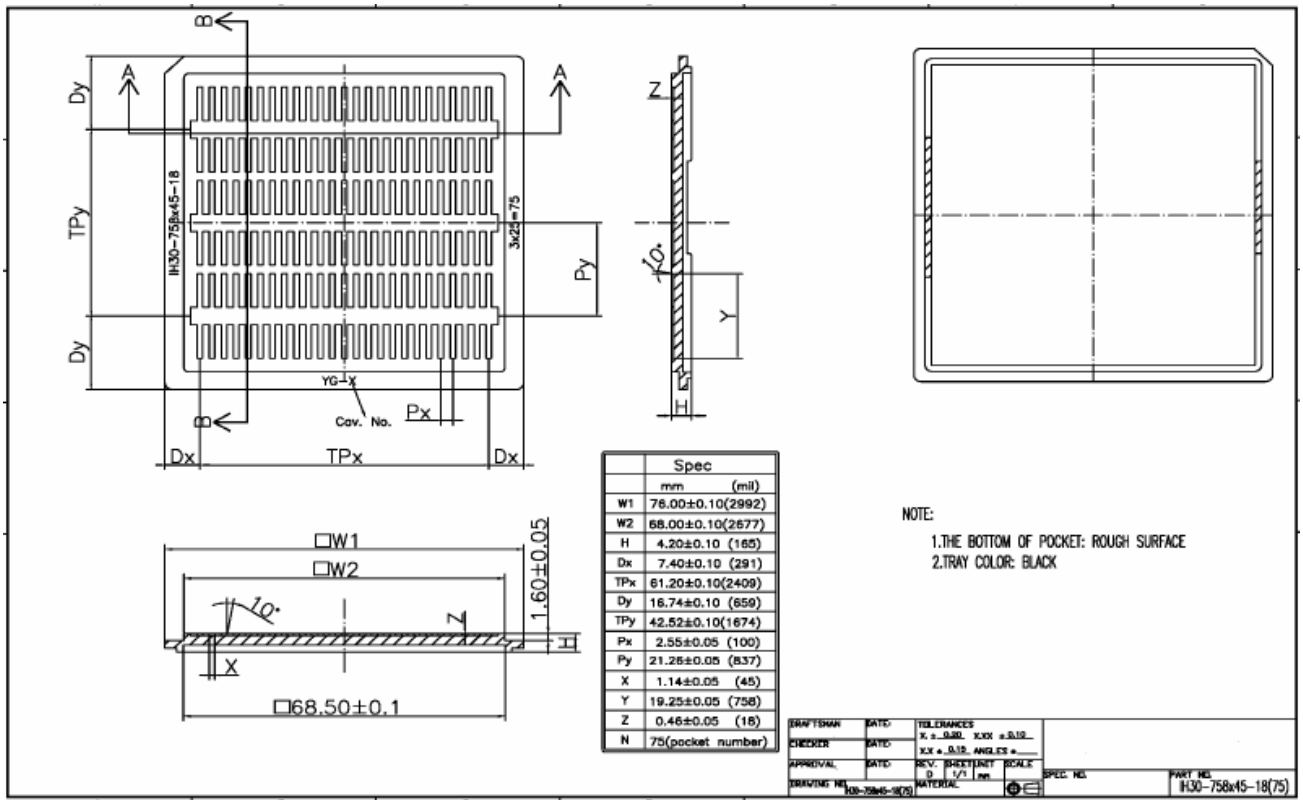


Figure 19-4 ITO and FPC connection example



20. PACKAGE INFORMATION

20.1 DIE TRAY DIMENSIONS



	Spec mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
H	4.20±0.10	(165)
Dx	7.40±0.10	(291)
TPx	61.20±0.10	(2409)
Dy	16.74±0.10	(659)
TPy	42.52±0.10	(1674)
Px	2.55±0.05	(100)
Py	21.26±0.05	(837)
X	1.14±0.05	(45)
Y	19.25±0.05	(758)
Z	0.46±0.05	(18)
N	75(pocket number)	

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol Hazardous Substances test report is available upon requested.

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