İstanbul
Bilgi Üniversitesi

CMPE321 - Computer Architecture

Lecture 7
DRAM Types

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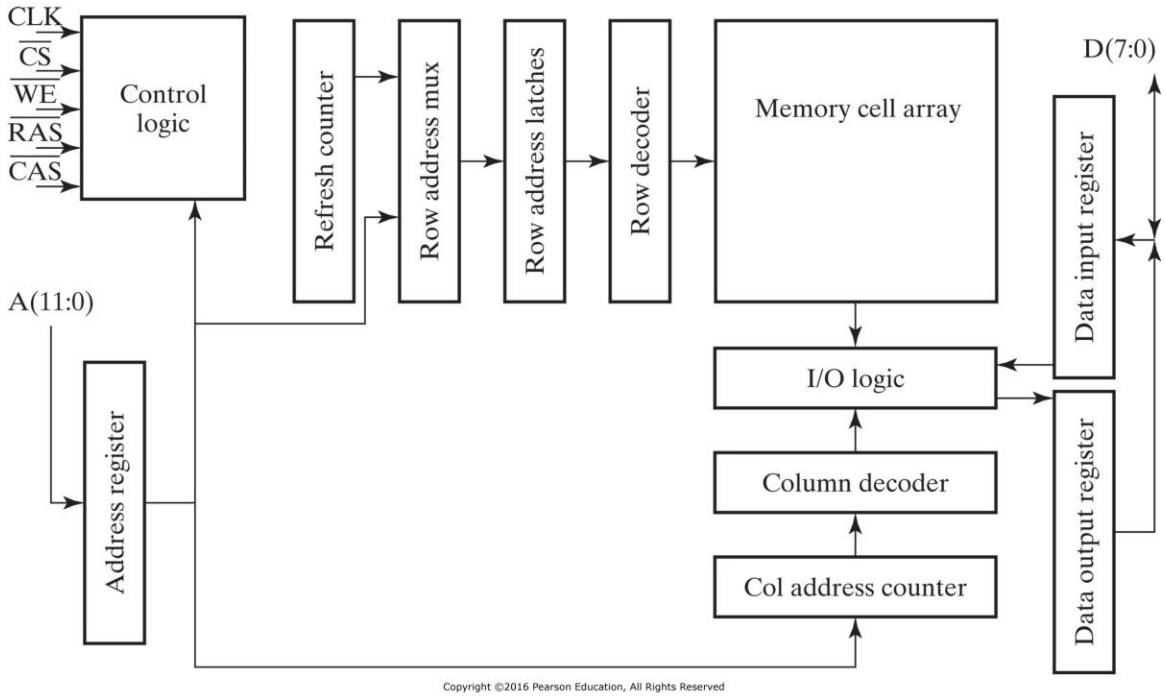
Synchronous DRAM (SDRAM)

- The use of clocked transfers differentiates SDRAM from conventional DRAM.
- A block diagram of a 16-megabyte SDRAM IC appears in Figure.
- The inputs and outputs differ little from those for the DRAM block diagram with the exception of the presence of the clock for synchronous operation.
- Internally, there are a number of differences. Since the SDRAM appears synchronous from the outside, there are synchronous registers on the address inputs and the data inputs and outputs.
- In addition, a column address counter has been added, which is key to the operation of the SDRAM.
- While the control logic may appear to be similar, the control in this case is much more complex, since the SDRAM has a mode control word that can be loaded from the address bus.
- Considering a 16 MB memory, the memory array contains 134,217,728 bits and is almost square, with 8192 rows and 16,384 columns.
  - There are 13 row address bits.
  - Since there are 8 bits per byte, the number of column addresses is 16,384 divided by 8, which equals 2048.
  - This requires 11 column address bits. Note that 13 plus 11 equals 24, giving the correct number of bits to address 16 MB.

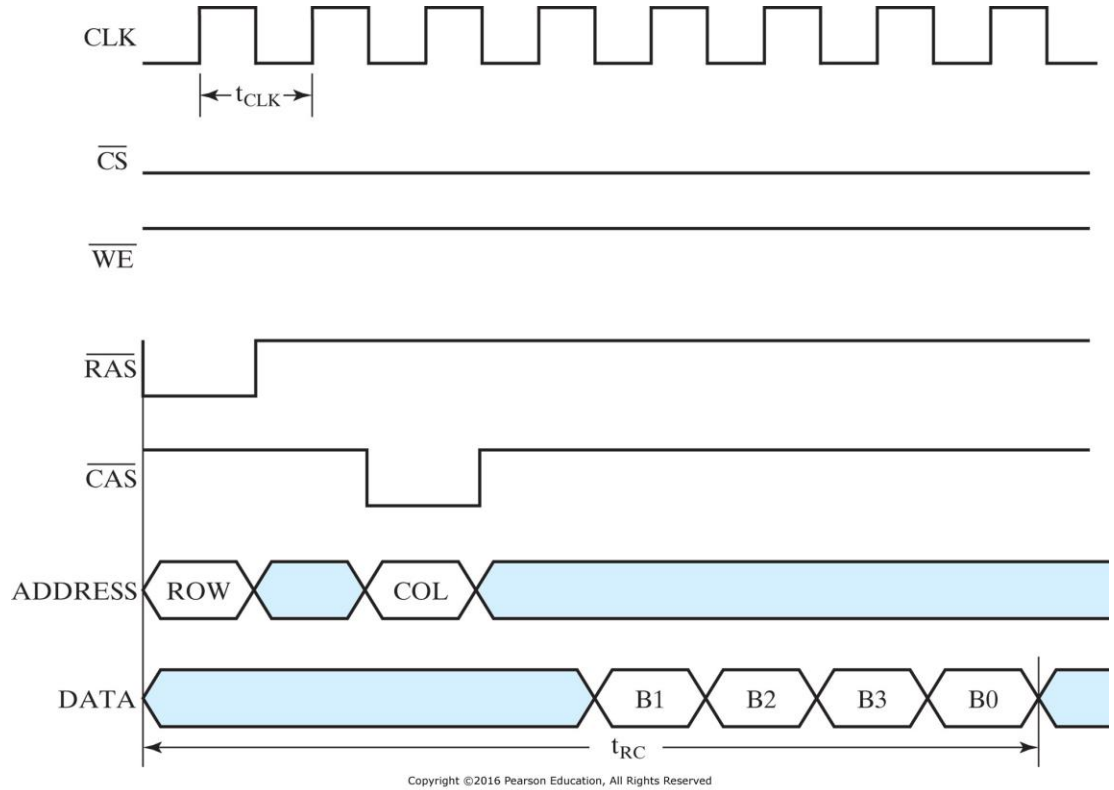


Synchronous DRAM (SDRAM)

- As with the regular DRAM, the SDRAM applies the row address first, followed by the column address.
- The timing, however, is somewhat different, and some new terminology is used. Before performing an actual read operation from a specified column address, the entire row of 2048 bytes specified by the applied row address is read out internally and stored in the I/O logic.
- Internally, this step takes a few clock cycles.
- Next, the actual read step is performed with the column address applied.
- After an additional delay of a few clock cycles, the data bytes begin appearing on the output, one per clock period.
- The number of bytes that appear, the burst length, has been set by loading a mode control word into the control logic from the address input.

Synchronous DRAM (SDRAM)

- The timing of a **burst read cycle** with **burst length** equal to four is shown in Figure.
- The read begins with the application of the row address and the **row address strobe (RAS)**, which causes the row address to be captured in the address register and the reading of the row to be initiated.
- During the next two clock periods, the reading of the row is taking place.
- During the third clock period, the column address and the column address strobe are applied, with the column address captured in the address register and the reading of the first data byte initiated.
- The data byte is then available to be read from the SDRAM at the positive clock edge occurring two cycles later.
- The second, third, and fourth bytes are available for reading on subsequent clock edges.
- In this Figure note that the bytes are presented in the order 1, 2, 3, 0.
  - **This is because, in the column address identifying the byte immediately needed by the CPU, the last two bits are 01.**
  - The subsequent bytes appear in the order of these two bits counted up modulo (burst length) by the column address counter, giving addresses ending in 01, 10, 11, and 00, with all other address bits fixed.



Synchronous DRAM (SDRAM)

- To compare the byte rate for reading bytes from SDRAM to that of the basic DRAM let's assume that the **read cycle time *t*RC** for the basic DRAM is **60 ns** and that the **clock period *t*CLK** for the SDRAM is **7.5 ns**.
- The byte rate for the basic DRAM is one byte per 60 ns, or **16.67 MB/sec**.
- For the SDRAM, using the timing from previous Figure, it requires 8.0 clock cycles, or 60 ns, to read four bytes, giving a byte rate of **66.67 MB/sec**.
- If the burst is eight instead of four bytes, a read cycle time of 90 ns is required, giving a byte rate of **88.89 MB/sec**.
- Finally, if the burst is the entire 2048-byte row of the SDRAM, the read cycle time becomes 60 + (2048 − 4) × 7.5 = 15,390 ns, giving a byte rate of **133.07 MB**, which approaches the limit of one byte per 7.5 ns clock period.

Double-Data-Rate SDRAM (DDR SDRAM)

- The second DRAM type, double-data-rate SDRAM (DDR SDRAM) overcomes the preceding limit without decreasing the clock period.
- Instead, it provides **two bytes of data per clock period** by **using both the positive and negative clock edges**.
- In timing diagram Figure from SDRAM, four bytes were read, one at each positive clock edge.
- By using both clock edges, eight bytes can be transferred in the same **read cycle time *t*RC**.
- For a 7.5 ns clock period, the byte rate limit doubles in the example to **266.14 MB/sec**.
- Additional basic techniques can be applied to further increase the byte rate:
  - For example, instead of having single byte data, an SDRAM IC can have the **data I/O length of four bytes** (32 bits).
  - This gives a byte rate limit of **1.065 GB/sec** with a 7.5 ns clock period. Eight bytes gives a byte rate limit of **2.130 GB/sec**.

Double-Data-Rate SDRAM (DDR SDRAM)

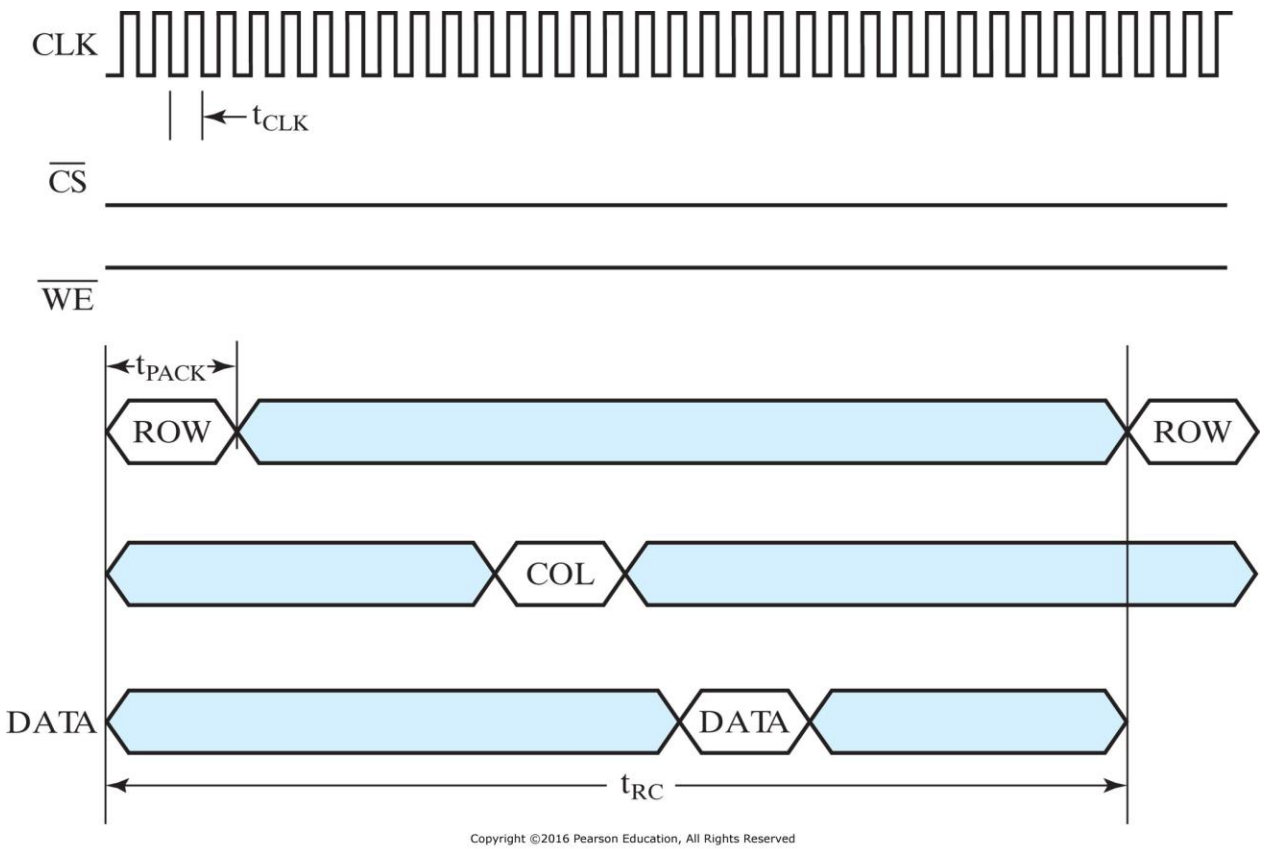
- The byte rates achieved in the examples are upper limits.
- If the actual accesses needed are to different rows of the RAM, the delay from the application of the RAS pulse to read out the first byte of data is significant and leads to performance well below the limit.
- This can be partially offset by breaking up the memory into multiple banks, where each bank performs the row read independently.
- Provided that the row and bank addresses are available early enough, row reads can be performed on one or more banks while data is still being transferred from the currently active row.
- When the column reads from the currently active row are complete, data can potentially be available immediately from other banks, permitting an uninterrupted flow of data from the memory.
- This permits the actual read rate to approach the limit more closely.
- Nevertheless, due to the fact that multiple row accesses to the same bank may occur in sequence, the maximum rate is not reached.

RAMBUS DRAM (RDRAM)

- The final DRAM type to be discussed is RAMBUS DRAM (RDRAM).
- RDRAM ICs are designed to be integrated into a memory system that uses a packet-based bus for the interaction between the RDRAM ICs and the memory bus to the processor.
- The primary components of the bus are a 3-bit path for the row address, a 5-bit path for the column address, and a 16-bit or 18-bit path for data.
- The bus is synchronous and performs transfers on both clock edges, the same property possessed by the DDR SDRAM.
- Information on the three paths mentioned above is transferred in packets that are four clock cycles long, which means that there are eight transfers/packet.
- The number of bits per packet for each of the paths is 24 bits for the row address packet, 40 bits for the column address packet, and 128 bits or 144 bits for the data packet.
- The larger data packet includes 16 parity bits for implementing an error-correcting code.
- The RDRAM IC employs the concept of multiple memory banks mentioned earlier to provide capability for concurrent memory accesses with different row addresses.
- RDRAM uses the usual row-activate technique in which the addressed row data of the memory is read.
- From this row data, the column address is used to select byte pairs in the order in which they are to be transmitted in the packet.

RAMBUS DRAM (RDRAM)

- A typical timing picture for an RDRAM read access is shown in the Figure.
- Due to the sophisticated electronic design of the RAMBUS system, we can consider a clock period of 1.875 ns.
- Thus, the time for transmission of a packet is *t*PACK= 4 × 1.875 = 7.5 ns.
- The cycle time for accessing a single data packet of 8 byte pairs or 16 bytes is 32 clock cycles or 60 ns, as shown in Figure.
- The corresponding byte rate is **266.67 MB/sec**.
- If four of the byte packets are accessed from the same row, the rate increases to **1.067 GB/sec**.
- By reading an entire RDRAM row of 2048 bytes, the cycle time increases to 60 + (2048 - 64) × 1.875/4 = **990 ns** or a byte rate limit of 2048/(990 × 10–9) = **2.069 MB/sec**, approaching the ideal limit of **4/1.875 ns** or **2.133 GB/sec**.



Arrays of Dynamic RAM ICs

- Many of the same design principles used for SRAM arrays also apply to DRAM arrays.
- There are, however, a number of different requirements for the control and addressing of DRAM arrays.
- These requirements are typically handled by a *DRAM controller*, which performs the following functions:
    1. controlling separation of the address into a row address and a column address and providing these addresses at the required times,
    2. providing the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals at the required times for read, write, and refresh operations,
    3. performing refresh operations at the necessary intervals, and
    4. providing status signals to the rest of the system (e.g., indicating whether the memory is busy performing refresh).
- The DRAM controller is a complex synchronous sequential circuit with the external CPU clock providing synchronization of its operation.

Chapter Summary

- Memory is of two types: **random-access memory (RAM)** and **read-only memory (ROM)**.
- For both types, we **apply an address** to **read from or write into a data word**.
- Read and write operations have specific steps and associated timing parameters, including **access time** and **write cycle time**.
- Memory can be **static** or **dynamic** and **volatile** or **nonvolatile**.
- Internally, a RAM chip consists of an array of RAM cells, decoders, write circuits, read circuits, and output circuits.
- A combination of a write circuit, read circuit, and the associated RAM cells can be logically modeled as a **RAM bit slice**.
- RAM bit slices, in turn, can be combined to form two-dimensional **RAM cell arrays**, which, with decoders and output circuits added, form the basis for a **RAM chip**.
- Output circuits use **three-state buffers** in order to facilitate connecting together an array of RAM chips without significant additional logic.
- Due to the need for **refresh**, additional circuitry is required within DRAMs, as well as in arrays of DRAM chips.
- In a quest for faster memory access, a number of new DRAM types have been developed.
- The most recent forms of these high-speed DRAMs employ a **synchronous interface** that uses a clock to control memory accesses.