Technical Reference Manual for the Pixel Array Control Monitor and Network (Pac-Man) Card

February 21, 2020

1 Signal Mapping

Logical	Trenz	Package Pin
SCL	MIO10	
SDA	MIO11	
LED	MIO12	
LED	MIO13	
LED	B35_L20_P	G19
LED	M35_L20_N	F19
TILE1_CLK_1	B33_L13_P	W17
TILE1_CUR_SEL_1	B33_L13_N	W18
TILE1_RESET_1	B33_L4_P	W20
TILE1_TRIG_1	B33_L4_N	W21
TILE1_EN	B33_L12_P	Y18
TILE1_MOSI_0	B33_L7_P	AA22
TILE1_MOSI_1	B33_L8_P	AA21
TILE1_MOSI_2	B33_L11_P	Y19
TILE1_MOSI_3	B33_L17_P	AA17
TILE1_MISO_0	B33_L7_N	AB22
TILE1_MISO_1	B33_L8_N	AB21
TILE1_MISO_2	B33_L11_N	AA19
TILE1_MISO_3	B33_L17_N	AB17

	FPGA	Front Panel	(Connection)	Example Use
1	PANEL_1	PANEL_1	Lemo?	External Trigger
2	PANEL_2	PANEL_2	Lemo?	External Clock
3	PANEL_3	PANEL_3	Lemo?	External Sync
4	PANEL_4	PANEL_4	Lemo?	-
5	LED_1	LED_1	LED	Power
6	LED_2	LED_2	LED	Zynq Power
7	LED_3	LED_3	LED	Tile Analog Power
8	LED_4	LED_4	LED	Tile Digital Power
9	LED_5	LED_5	LED	UART Status
10	LED_6	LED_6	LED	FIFO full detected
11	LED_7	LED_7	LED	-
12	LED_8	LED_8	LED	-
13	BUTTON_1	BUTTON_1	Button	Sync
14	BUTTON_2	BUTTON_2	Button	Soft Reset
15	BUTTON_3	BUTTON_3	Button	Hard Reset
16	BUTTON_4	BUTTON_4	Button	-