SISTEMA DIGITALAK DISEINATZEKO OINARRIAK

2. PRAKTIKA

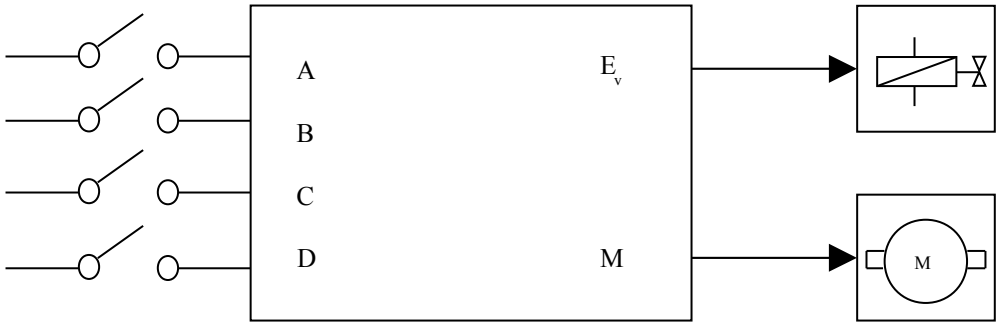
ZIRKUITU KONBINAZIONALAK

Honako funtzio hauek betetzen dituzten zirkuituak muntatu:

1. $Z = A \cdot B$ AND ateak (7408) erabiliz.
2. $Z = A \cdot B$ NOR ateak (7402) erabiliz.
3. $Z = A \oplus B$ XOR ateak (7486) erabiliz.

Motor eta elektro-balbula bat kontrolatzeko zirkuitua diseinatu.Sarrerako seinale moduan 3 mikro-etengailu eta hurbiltasun-detektagailu bat daukagu. Detektagailu hauek, eragiten direnean, ixten dute kontaktu bat. Zirkuitua espezifikazio hauek beteko ditu:

- A edo B aktibatzen badira, elektro-balbula baino ez da aktibatzen (motorra geldirik).
- A eta B aldiberean aktibatzen badira, motorra baino ez da aktibatuko (electro-balbula desaktibaturik)..
- Detektagailu guztiak aktibatzen badira aldiberean, motorra eta elektro-balbula aktibatuko dira.



Ebazpena:

$$E_v = A \oplus B + B \cdot C \cdot D$$
$$M = A \cdot B$$

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

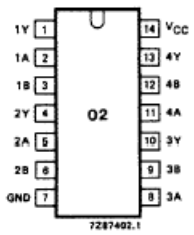


Fig.1 Pin configuration.

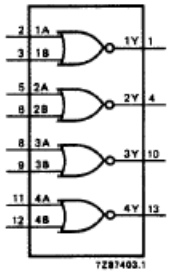


Fig.2 Logic symbol.

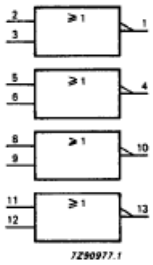


Fig.3 IEC logic symbol.

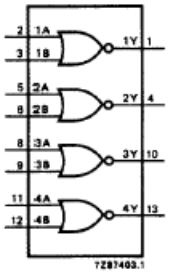


Fig.4 Functional diagram.

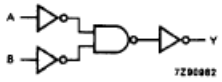


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

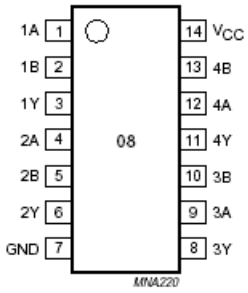
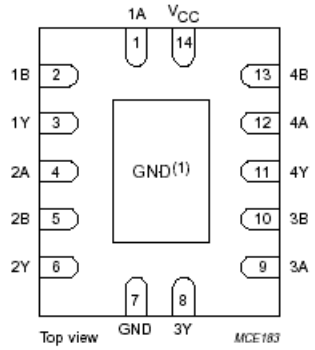


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

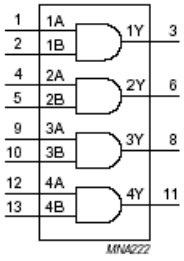


Fig.3 Logic symbol.

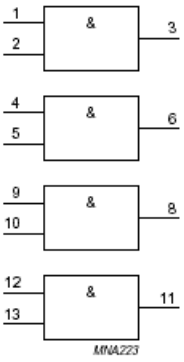


Fig.4 IEC logic symbol.

FUNCTION TABLE

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

PINNING

PIN	SYMBOL	DESCRIPTION
1, 4, 9 and 12	1A to 4A	data inputs
2, 5, 10 and 13	1B to 4B	data inputs
3, 6, 8 and 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	DC supply voltage

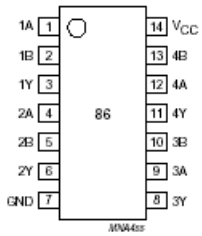


Fig.1 Pin configuration.

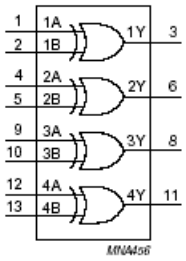


Fig.2 Logic symbol.

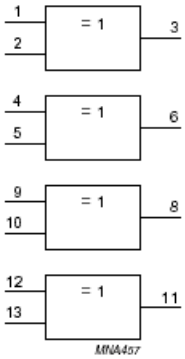


Fig.3 IEC logic symbol.

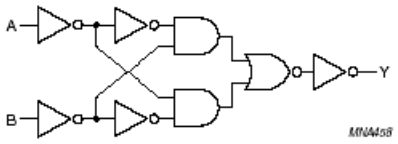


Fig.4 Logic diagram (one gate).

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall times except for Schmitt trigger inputs	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	$V_I < -0.5$ V; note 1	–	–20	mA
I_{OK}	DC output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	DC output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}	DC V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO package: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP package: above 60 °C the value of P_D derates linearly with 5.5 mW/K.