Build a Smarter World

EG91-QuecOpen Hardware Design

LTE Module Series

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Contents

About the Document **2**
Contents **3**
Table Index **5**
Figure Index **7**

1 Introduction **9**
1.1. Safety Information 10

2 Product Concept **11**
2.1. General Description 11
2.2. Key Features 12
2.3. Functional Diagram 15
2.4. Evaluation Board 16

3 Application Interfaces **17**
3.1. General Description 17
3.2. Pin Assignment 18
3.3. Pin Description 19
3.4. Operating Modes 27
3.5. Power Saving 27
3.5.1. Sleep Mode 27
3.5.1.1. Main UART Application 27
3.5.1.2. USB Application with USB Remote Wakeup Function 28
3.5.1.3. USB Application with USB Suspend/Resume and RI Function 29
3.5.1.4. USB Application without USB Suspend Function 30
3.5.2. Airplane Mode 30
3.6. Power Supply 31
3.6.1. Power Supply Pins 31
3.6.2. Decrease Voltage Drop 32
3.6.3. Reference Design for Power Supply 33
3.6.4. Monitor the Power Supply 33
3.7. Turn on and off Scenarios 34
3.7.1. Turn on Module Using the PWRKEY 34
3.7.2. Turn off Module 36
3.7.2.1. Turn off Module Using the PWRKEY Pin 36
3.7.2.2. Turn off Module Using AT Command 36
3.8. Reset the Module 37
3.9. (U)SIM Interfaces 38
3.10. USB Interface 42
3.11. UART Interfaces 43
3.12. PCM and I2C Interfaces 46
3.13. SPI Interface 49
3.14. Network Status Indication 49

3.15. STATUS 50
3.16. Behaviors of RI 51
3.17. USB_BOOT Interface 52
3.18. GPIOs 53

4 GNSS Receiver 54
4.1. General Description 54
4.2. GNSS Performance 54
4.3. Layout Guidelines 55

5 Antenna Interfaces 56
5.1. Main/Rx-diversity Antenna Interfaces 56
5.1.1. Pin Definition 56
5.1.2. Operating Frequency 56
5.1.3. Reference Design of RF Antenna Interface 57
5.1.4. Reference Design of RF Layout 58
5.2. GNSS Antenna Interface 60
5.3. Antenna Installation 61
5.3.1. Antenna Requirement 61
5.3.2. Recommended RF Connector for Antenna Installation 62

6 Electrical, Reliability and Radio Characteristics 64
6.1. Absolute Maximum Ratings 64
6.2. Power Supply Ratings 64
6.3. Operation and Storage Temperatures 65
6.4. Current Consumption 66
6.5. RF Output Power 69
6.6. RF Receiving Sensitivity 70
6.7. Electrostatic Discharge 71
6.8. Thermal Consideration 72

7 Mechanical Dimensions 74
7.1. Mechanical Dimensions of the Module 74
7.2. Recommended Footprint 76
7.3. Design Effect Drawings of the Module 77

8 Storage, Manufacturing and Packaging 78
8.1. Storage 78
8.2. Manufacturing and Soldering 79
8.3. Packaging 80

9 Appendix A References 81
10 Appendix B GPRS Coding Schemes 85
11 Appendix C GPRS Multi-slot Classes 86
12 Appendix D EDGE Modulation and Coding Schemes 88

Table Index

TABLE 1: FREQUENCY BANDS OF EG91-QUECOPEN MODULE 12
TABLE 2: KEY FEATURES OF EG91-QUECOPEN MODULE 12
TABLE 3: IO PARAMETERS DEFINITION 19
TABLE 4: PIN DESCRIPTION 19
TABLE 5: ALTERNATE FUNCTIONS OF MULTIPLEXING PINS 25
TABLE 6: OVERVIEW OF OPERATING MODES 27
TABLE 7: VBAT AND GND PINS 31
TABLE 8: PIN DEFINITION OF PWRKEY 34
TABLE 9: PIN DEFINITION OF RESET_N 37
TABLE 10: PIN DEFINITION OF (U)SIM INTERFACES 38
TABLE 11: PIN DEFINITION OF USB INTERFACE 42
TABLE 12: PIN DEFINITION OF MAIN UART INTERFACE 44
TABLE 13: PIN DEFINITION OF DEBUG UART INTERFACE 44
TABLE 14: PIN DEFINITION OF APPLICATION UART INTERFACE (MULTIPLEXED WITH SPI) 44
TABLE 15: LOGIC LEVELS OF DIGITAL I/O 45
TABLE 16: PIN DEFINITION OF PCM AND I2C INTERFACES 48
TABLE 17: PIN DEFINITION OF SPI INTERFACE 49
TABLE 18: PIN DEFINITION OF NETWORK STATUS INDICATOR 50
TABLE 19: WORKING STATE OF THE NETWORK STATUS INDICATOR 50
TABLE 20: PIN DEFINITION OF STATUS 51
TABLE 21: DEFAULT BEHAVIORS OF RI 52
TABLE 22: PIN DEFINITION OF USB_BOOT INTERFACE 52
TABLE 23: ALTERNATE GPIO FUNCTION OF THE MULTI-FUNCTION PINS 53
TABLE 24: GNSS PERFORMANCE 54
TABLE 25: PIN DEFINITION OF RF ANTENNA 56
TABLE 26: MODULE OPERATING FREQUENCIES 56
TABLE 27: PIN DEFINITION OF GNSS ANTENNA INTERFACE 60
TABLE 28: GNSS FREQUENCY 60
TABLE 29: ANTENNA REQUIREMENTS 61
TABLE 30: ABSOLUTE MAXIMUM RATINGS 64
TABLE 31: POWER SUPPLY RATINGS 64
TABLE 32: OPERATION AND STORAGE TEMPERATURES 65
TABLE 33: EG91-E-QUECOPEN CURRENT CONSUMPTION 66
TABLE 34: EG91-NA-QUECOPEN CURRENT CONSUMPTION 68
TABLE 35: GNSS CURRENT CONSUMPTION OF EG91-NA-QUECOPEN 69
TABLE 36: RF OUTPUT POWER 69
TABLE 37: EG91-E-QUECOPEN CONDUCTED RF RECEIVING SENSITIVITY 70
TABLE 38: EG91-NA-QUECOPEN CONDUCTED RF RECEIVING SENSITIVITY 71
TABLE 39: ELECTROSTATIC DISCHARGE CHARACTERISTICS 71
TABLE 40: RELATED DOCUMENTS 81
TABLE 41: TERMS AND ABBREVIATIONS 81
TABLE 42: DESCRIPTION OF DIFFERENT CODING SCHEMES 85

TABLE 43: GPRS MULTI-SLOT CLASSES 86
TABLE 44: EDGE MODULATION AND CODING SCHEMES..... 88

Figure Index

FIGURE 1: FUNCTIONAL DIAGRAM 15
FIGURE 2: PIN ASSIGNMENT (TOP VIEW) 18
FIGURE 3: SLEEP MODE APPLICATION VIA UART 28
FIGURE 4: SLEEP MODE APPLICATION WITH USB REMOTE WAKEUP 29
FIGURE 5: SLEEP MODE APPLICATION WITH RI 29
FIGURE 6: SLEEP MODE APPLICATION WITHOUT SUSPEND FUNCTION 30
FIGURE 7: POWER SUPPLY LIMITS DURING BURST TRANSMISSION 32
FIGURE 8: STAR STRUCTURE OF THE POWER SUPPLY 32
FIGURE 9: REFERENCE CIRCUIT OF POWER SUPPLY 33
FIGURE 10: TURN ON THE MODULE USING DRIVING CIRCUIT 34
FIGURE 11: TURN ON THE MODULE USING BUTTON 35
FIGURE 12: TIMING OF TURNING ON MODULE 35
FIGURE 13: TIMING OF TURNING OFF MODULE 36
FIGURE 14: REFERENCE CIRCUIT OF RESET_N BY USING DRIVING CIRCUIT 37
FIGURE 15: REFERENCE CIRCUIT OF RESET_N BY USING BUTTON 37
FIGURE 16: TIMING OF RESETTING MODULE 38
FIGURE 17: REFERENCE CIRCUIT OF (U)SIM1 INTERFACE WITH AN 8-PIN (U)SIM CARD CONNECTOR 39
FIGURE 18: REFERENCE CIRCUIT OF (U)SIM1 INTERFACE WITH A 6-PIN (U)SIM CARD CONNECTOR 40
FIGURE 19: REFERENCE CIRCUIT OF (U)SIM2 INTERFACE WITH AN 8-PIN (U)SIM CARD CONNECTOR 40
FIGURE 20: REFERENCE CIRCUIT OF (U)SIM2 INTERFACE WITH A 6-PIN (U)SIM CARD CONNECTOR 41
FIGURE 21: REFERENCE CIRCUIT OF USB INTERFACE 42
FIGURE 22: REFERENCE CIRCUIT WITH TRANSLATOR CHIP 45
FIGURE 23: REFERENCE CIRCUIT WITH TRANSISTOR CIRCUIT 46
FIGURE 24: PRIMARY MODE TIMING 47
FIGURE 25: AUXILIARY MODE TIMING 47
FIGURE 26: REFERENCE CIRCUIT OF PCM APPLICATION WITH AUDIO CODEC 48
FIGURE 27: REFERENCE CIRCUIT OF SPI INTERFACE WITH PERIPHERALS 49
FIGURE 28: REFERENCE CIRCUIT OF THE NETWORK STATUS INDICATOR 50
FIGURE 29: REFERENCE CIRCUIT OF STATUS 51
FIGURE 30: REFERENCE CIRCUIT OF USB_BOOT INTERFACE 52
FIGURE 31: REFERENCE CIRCUIT OF RF ANTENNA INTERFACE 57
FIGURE 32: MICROSTRIP LINE DESIGN ON A 2-LAYER PCB 58
FIGURE 33: COPLANAR WAVEGUIDE LINE DESIGN ON A 2-LAYER PCB 58
FIGURE 34: COPLANAR WAVEGUIDE LINE DESIGN ON A 4-LAYER PCB (LAYER 3 AS REFERENCE GROUND) 59
FIGURE 35: COPLANAR WAVEGUIDE LINE DESIGN ON A 4-LAYER PCB (LAYER 4 AS REFERENCE GROUND) 59
FIGURE 36:REFERENCE CIRCUIT OF GNSS ANTENNA 60
FIGURE 37: DIMENSIONS OF THE U.FL-R-SMT CONNECTOR (UNIT: MM) 62

FIGURE 38: MECHANICALS OF U.FL-LP CONNECTORS 62
FIGURE 39: SPACE FACTOR OF MATED CONNECTOR (UNIT: MM) 63
FIGURE 40: REFERENCED HEATSINK DESIGN (HEATSINK AT THE TOP OF THE MODULE) 72
FIGURE 41: REFERENCED HEATSINK DESIGN (HEATSINK AT THE BOTTOM OF CUSTOMERS' PCB) . 73
FIGURE 42: MODULE TOP AND SIDE DIMENSIONS 74
FIGURE 43: MODULE BOTTOM DIMENSIONS (TOP VIEW) 75
FIGURE 44: RECOMMENDED FOOTPRINT (TOP VIEW) 76
FIGURE 45: TOP VIEW OF THE MODULE 77
FIGURE 46: BOTTOM VIEW OF THE MODULE 77
FIGURE 47: REFLOW SOLDERING THERMAL PROFILE 79
FIGURE 48: TAPE DIMENSIONS 80
FIGURE 49: REEL DIMENSIONS 80

1 Introduction

This document defines the EG91-QuecOpen module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EG91-QuecOpen module. Associated with application note and user guide, customers can use EG91-QuecOpen module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG91-QuecOpen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

QuecOpen® is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of QuecOpen® solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With QuecOpen® solution, development flow for wireless application and hardware design will be simplified. Main features of QuecOpen® solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware wirelessly
- Improves products' cost-performance ratio, and enhances products' competitiveness

EG91-QuecOpen module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.2GHz. Customers can use EG91-QuecOpen modules as the basis for development of QuecOpen® applications.

EG91-QuecOpen module is an embedded 4G wireless communication module with receive diversity. It supports LTE-FDD/WCDMA/GSM wireless communication, and provides data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It can also provide voice functionality [1)] to meet customers' specific application demands.

Wit a compact profile of 29.0mm × 25.0mm × 2.25mm, EG91-QuecOpen can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

It is an SMD type module which can be embedded into applications through its 106 LGA pads.

EG91-QuecOpen is integrated with internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

The following table shows the frequency bands of EG91-QuecOpen module.

Table 1: Frequency Bands of EG91-QuecOpen Module

Module	LTE Bands (with Rx-diversity)	WCDMA (with Rx-diversity)	GSM	GNSS [2)]
EG91-E-QuecOpen	FDD: B1/B3/B7/B8/B20/B28A	B1/B8	900/1800MHz	Not supported
EG91-NA-QuecOpen	FDD: B2/B4/B5/B12/B13	B2/B4/B5	Not supported	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

1. [1)] EG91-QuecOpen contains **Telematics** version and **Data-only** version. **Telematics** version supports voice and data functions, while **Data-only** version only supports data function.
2. [2)] GNSS function is optional.
3. "*" means under development.

2.2. Key Features

The following table describes the detailed features of EG91-QuecOpen module.

Table 2: Key Features of EG91-QuecOpen Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands
LTE Features	Support up to non-CA Cat 1 FDD Support 1.4MHz~20MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max 10Mbps (DL)/5Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42Mbps (DL)

	HSUPA: Max 5.76Mbps (UL) WCDMA: Max 384Kbps (DL)/384Kbps (UL)
GSM Features	**R99:** CSD: 9.6kbps **GPRS:** Support GPRS multi-slot class 33 Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL)/Max 85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL)/Max 236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/CMUX*/HTTPS*/ SMTP*/MMS*/FTPS*/SMTPS*/SSL*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interfaces	Support 1.8V and 3.0V (U)SIM cards
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB* Support USB serial drivers for Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.0/7.x/8.x

UART Interface	**Main UART:** Used for AT command communication only Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output 115200bps baud rate Application UART multiplexed from SPI interface Used for communication and data transmission with peripherals Baud rate reach up to 921600bps, 115200bps by default
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NETLIGHT pin for network activity status
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversity antenna (ANT_DIV) interface and GNSS antenna interface (ANT_GNSS) [1)]
Physical Characteristics	Size: (29.0±0.15)mm × (25.0±0.15)mm × (2.25±0.2)mm Package: LGA Weight: approx. 3.8g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] GNSS antenna interface is only supported on EG91-NA-QuecOpen.
2. [2)] Within operating temperature range, the module is 3GPP compliant.
3. [3)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.
4. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EG91-QuecOpen and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

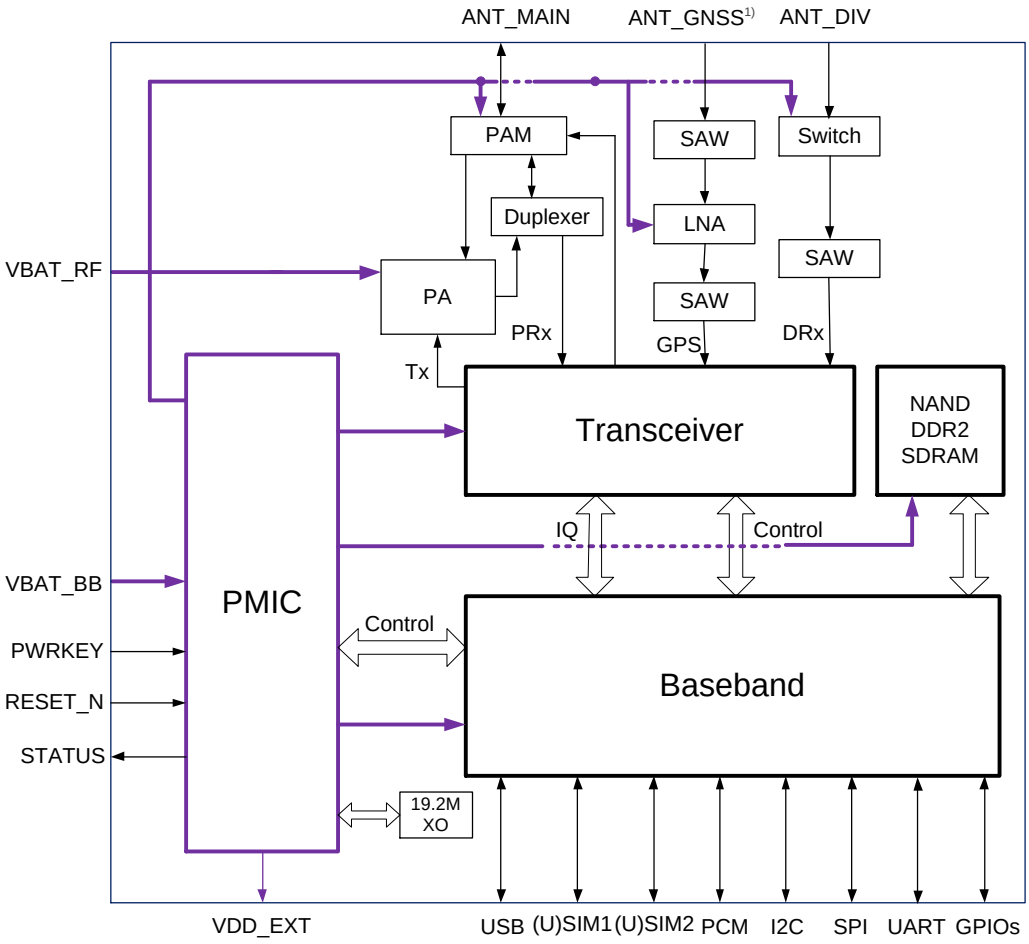


Figure 1: Functional Diagram

NOTE

1) GNSS antenna interface is only supported on EG91-NA-QuecOpen.

2.4. Evaluation Board

In order to help customers develop applications conveniently with EG91-QuecOpen, Quectel supplies an evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EG91-QuecOpen is equipped with 62-pin 1.1mm pitch SMT pads plus 44-pin ground/reserved pads that can be connected to customers' cellular application platforms. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI interface
- Status indication
- USB_BOOT interface
- GPIOs

3.2. Pin Assignment

The following figure shows the pin assignment of EG91-QuecOpen module.

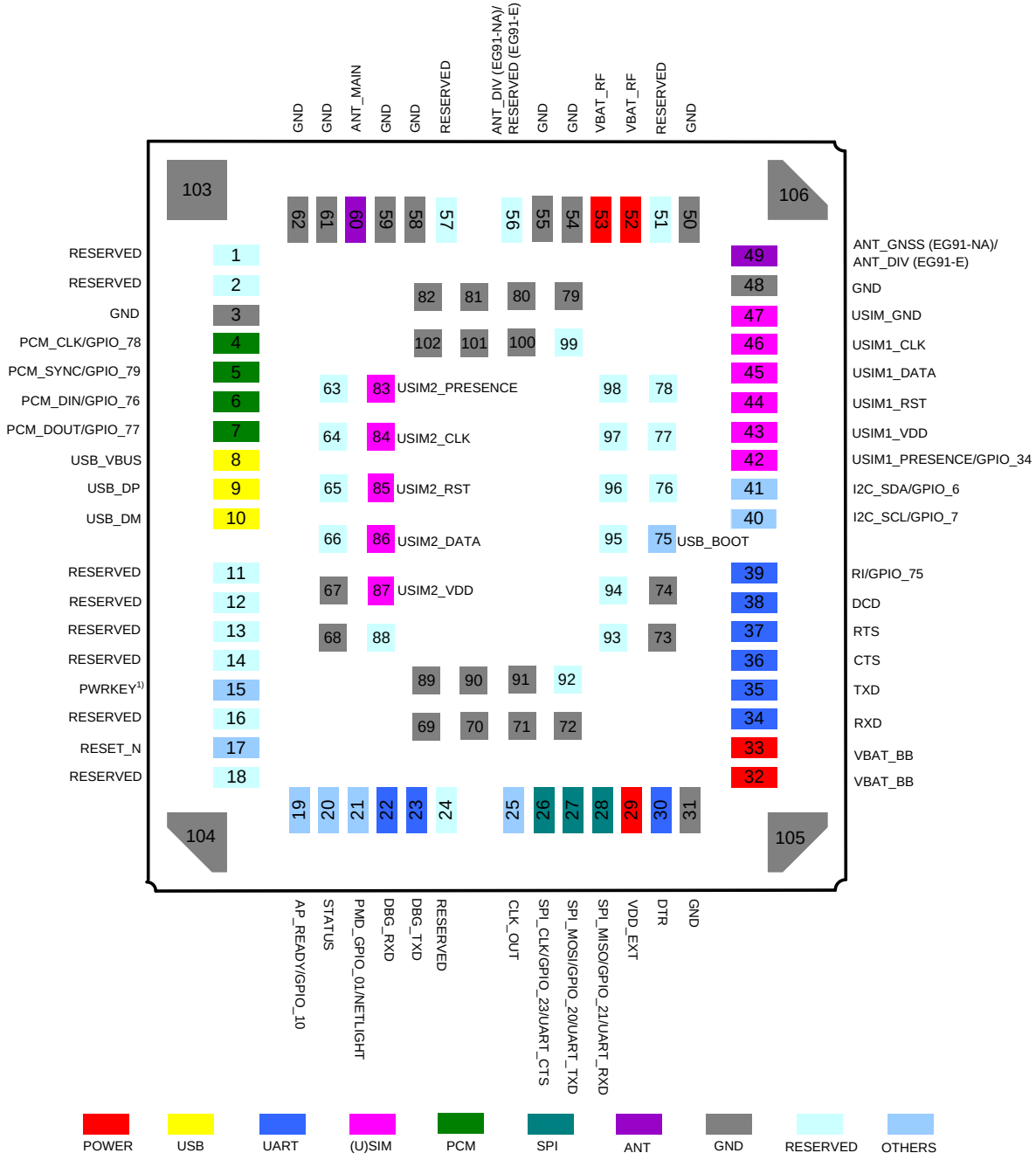


Figure 2: Pin Assignment (Top View)

NOTES

1. [1] PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pads should be connected to ground in the design.
4. Please note that the definition of pin 49 and 56 are different between EG91-E-QuecOpen and EG91-NA-QuecOpen.

3.3. Pin Description

The following tables show the pin definition and description of EG91-QuecOpen.

Table 3: IO Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.

VBAT_RF	52, 53	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a transmitting burst.
VDD_EXT	29	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~106		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	$V_O$in=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.
NETLIGHT	21	DO	Indicate the module's network activity status	$V_O$in=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	PI	USB detection	Vnorm=5.0V	
USB_DP	9	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.

USB_DM	10	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	47		Specified ground for (U)SIM card		
USIM1_VDD	43	PO	Power supply for (U)SIM card	For 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V For 3.0V (U)SIM: Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM2_VDD	87				
USIM1_DATA	45	IO	Data signal of (U)SIM card	For 1.8V (U)SIM: V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V $V_O$in=1.35V For 3.0V (U)SIM: V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V $V_O$in=2.55V	
USIM2_DATA	86				
USIM1_CLK	46	DO	Clock signal of (U)SIM card	For 1.8V (U)SIM: V_{OL}max=0.45V $V_O$in=1.35V For 3.0V (U)SIM: V_{OL}max=0.45V $V_O$in=2.55V	
USIM2_CLK	84				
USIM1_RST	44	DO	Reset signal of (U)SIM card	For 1.8V (U)SIM: V_{OL}max=0.45V $V_O$in=1.35V For 3.0V (U)SIM: V_{OL}max=0.45V $V_O$in=2.55V	
USIM2_RST	85				
USIM1_ PRESENCE	42	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V	1.8V power domain. If unused, keep it

USIM2_ PRESENCE	83			V_{IH}min=1.2V V_{IH}max=2.0V	open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	39	DO	Ring indicator	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
DCD	38	DO	Data carrier detection	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
CTS	36	DO	Clear to send	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
RTS	37	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control.	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit data	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
RXD	34	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	23	DO	Transmit data	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	22	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	6	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_DOUT	7	DO	PCM data output	V_{OL}max=0.45V V_{O}in=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	5	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{O}in=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	4	IO	PCM clock	V_{OL}max=0.45V V_{O}in=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock. Used for external codec.		An external pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data. Used for external codec.		An external pull-up resistor is required. 1.8V only. If unused, keep it open.
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SPI_CLK	26	DO	Clock signal of SPI interface	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
SPI_MOSI	27	DO	Master output slave input of SPI interface	V_{OL}max=0.45V $V_O$in=1.35V	1.8V power domain. If unused, keep it open.
SPI_MISO	28	DI	Master input slave output of SPI interface	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	49 (EG91-QuecOpen-NA)	AI	GNSS antenna pad		50Ω impedance. If unused, keep it open. Pin 49 is defined as ANT_DIV on EG91-QuecOpen-E.
ANT_DIV	49 (EG91-QuecOpen-E)	AI	Receive diversity antenna pad		50Ω impedance. If unused, keep it open.
	56 (EG91-QuecOpen-NA)	AI	Receive diversity antenna pad		50Ω impedance. If unused, keep it open. Pin 56 is reserved on EG91-QuecOpen-E.
ANT_MAIN	60	IO	Main antenna pad		50Ω impedance
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CLK_OUT	25	DI	Clock output		Provide a digital clock output for an external audio codec. If unused, keep this pin open.
AP_READY	19	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

USB_BOOT	75	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	1, 2, 11~14, 16, 18, 24, 51 57, 63~66, 76~78, 88, 92~99		Reserved		Keep these pins unconnected.

For EG91-QuecOpen module, some pins have multi-functions that can be used as GPIO or UART besides its' default function. The following table show the alternate functions of these multiplexing pins in EG91-QuecOpen module.

Table 5: Alternate Functions of Multiplexing Pins

Pin Name	Pin No.	Model 1 (Default)	Model 2	Model 3	Reset [1]	Wake-up Interrupt [2]	Comment
PCM_CLK	4	PCM_CLK	GPIO_78	--	B-PD,L	NO	BOOT_ CONFIG_8
PCM_SYNC	5	PCM_SYNC	GPIO_79	--	B-PD,L	YES	BOOT_ CONFIG_7
PCM_DIN	6	PCM_DIN	GPIO_76	--	B-PD,L	YES	
PCM_DOUT	7	PCM_DOUT	GPIO_77	--	B-PD,L	NO	
AP_READY	19	AP_READY	GPIO_10	--	B-PD,L	NO	
STATUS	20	STATUS	--	--	B-PD,L	--	
NETLIGHT	21	PMD[3] (GPIO_01)	NETLIGHT	--	B-PD,L	NO	
DBG_RXD	22	DBG_RXD	--	--	B-PD,L	--	
DBG_TXD	23	DBG_TXD	--	--	B-PD,L	--	
SPI_CLK	26	SPI_CLK	GPIO_23[4]	UART_CTS_BLSP6	B-PU,H	NO	BOOT_ CONFIG_4
SPI_MOSI	27	SPI_MOSI	GPIO_20	UART_TX	B-PD,L	YES	

				D_BLSP6			
SPI_MISO	28	SPI_MISO	GPIO_21	UART_RX D_BLSP6	B-PD,L	YES	
DTR	30	DTR	--	--	B-PD,L	--	Used as AT command Communication only.
RXD	34	RXD	--	--	B-PD,L	--	
TXD	35	TXD	--	--	B-PD,L	--	
CTS	36	CTS	--	--	B-PD,L	--	
RTS	37	RTS	--	--	B-PD,L	--	
DCD	38	DCD	--	--	B-PD,L	--	
RI	39	RI	GPIO_75	--	B-PD,L	YES	
I2C_SCL	40	I2C_SCL	GPIO_7	UART_CTS_BLSP2	B-PD,L	NO	
I2C_SDA	41	I2C_SDA	GPIO_6	UART_RTS_BLSP2	B-PD,L	NO	
USIM1_PRESENCE	42	USIM1_PRESENCE	GPIO_34	--	B-PD,L	YES	
USIM1_RST	44	USIM1_RST	--	--	BH-PD,L	--	Dedicated pin. It can not be reassigned as GPIO.
USIM1_DATA	45	USIM1_DATA	--	--	BH-PD,L	--	
USIM1_CLK	46	USIM1_CLK	--	--	BH-PD,L	--	
USIM2_PRESENCE	83	USIM2_PRESENCE	--	--	B-PD,L	--	Dedicated pin. It can not be reassigned as GPIO.
USIM2_CLK	84	USIM2_CLK	--	--	BH-PD,L	--	
USIM2_RST	85	USIM2_RST	--	--	BH-PD,L	--	
USIM2_DATA	86	USIM2_DATA	--	--	BH-PD,L	--	

NOTES

1. The pin function in Model 2 and Model 3 takes effect only after software configuration.
2. [1)] Please refer to ***Table 2*** for more details about the symbol description.
3. [2)]All the GPIO that located on baseband of Qualcomm chipset support interrupt function. But not all interrupts can wake up the sleeping module. The wake-up interrupt function is disabled by default.
4. [3)]means the GPIO that located on PMD of Qualcomm chipset.
5. [4)]means the GPIO_XX that located on baseband of Qualcomm chipset.

6. All BOOT_CONFIG pins are prohibited to be pulled up before the module is powered on.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EG91-QuecOpen is able to reduce its current consumption to a minimum value during the sleep mode. The following sections describe the power saving procedures of EG91-QuecOpen module.

3.5.1.1. Main UART Application

If the host communicates with the module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

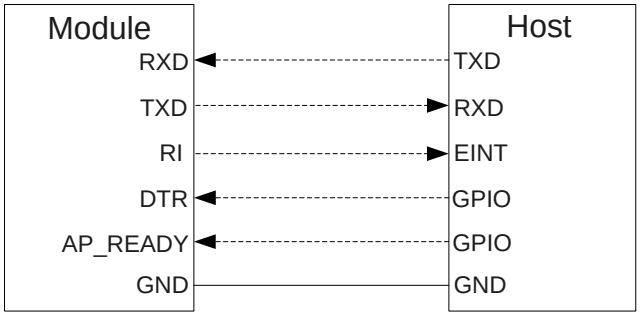


Figure 3: Sleep Mode Application via UART

Driving the host DTR to low level will wake up the module.

- When EG91-QuecOpen has a URC to report, RI signal will wake up the host. Refer to ***Chapter 3.16*** for details about RI behavior.
- AP_READY will detect the sleep state of host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"*** command for details.

NOTES

1. The MAIN UART is used as AT command communitcation only.
2. "*" means under development.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

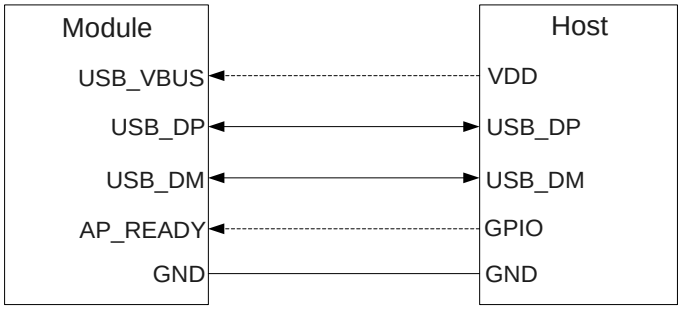


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG91-QuecOpen through USB will wake up the module.
- When EG91-QuecOpen has a URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

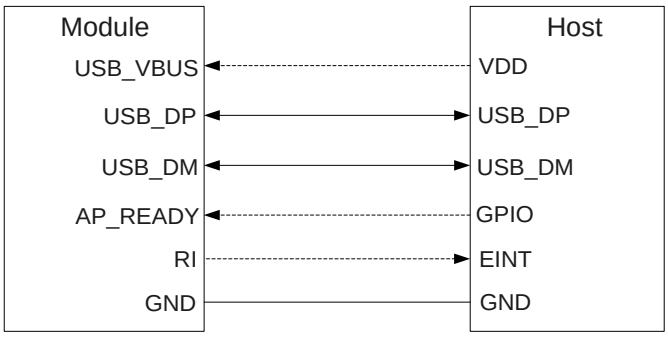


Figure 5: Sleep Mode Application with RI

- Sending data to EG91-QuecOpen through USB will wake up the module.
- When EG91-QuecOpen has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

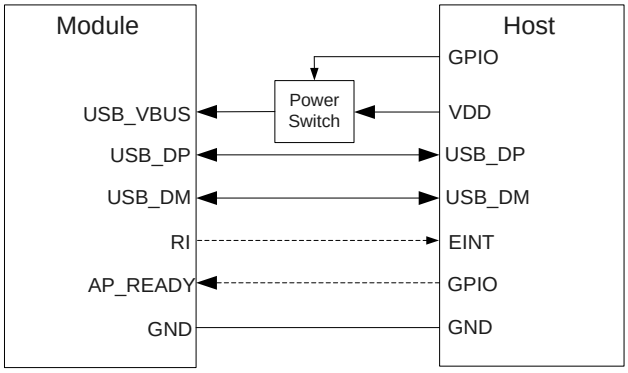


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Please refer to ***document [1]*** for more details about EG91-QuecOpen power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUN command provides the choice of functionality levels as shown below:

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command and this command is under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG91-QuecOpen provides four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module's RF part.	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for module's baseband part.	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~106	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

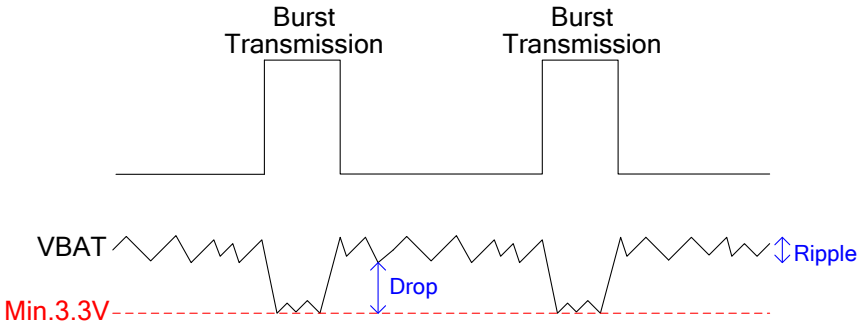


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested that a zener diode whose dissipation power is more than 0.5W should be used. The following figure shows the star structure of the power supply.

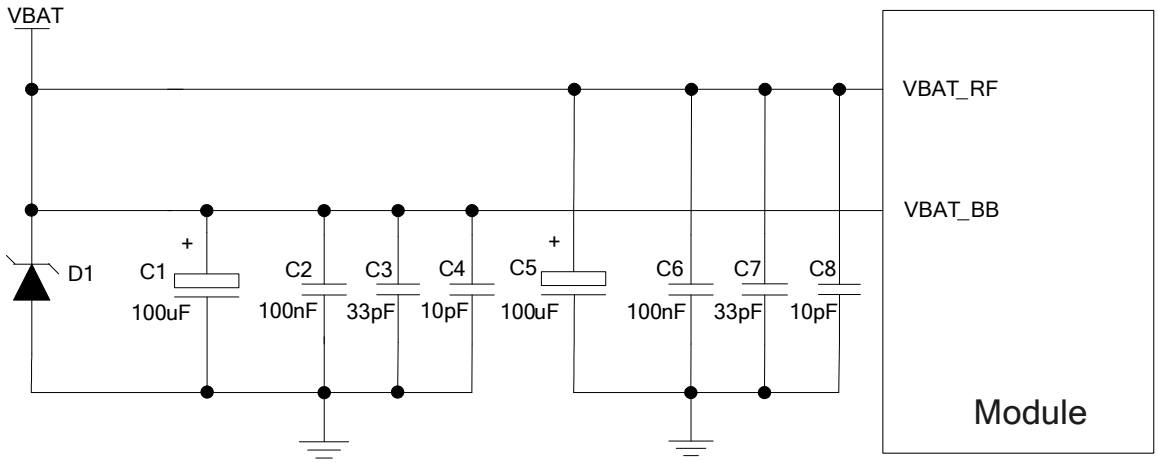


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3A.

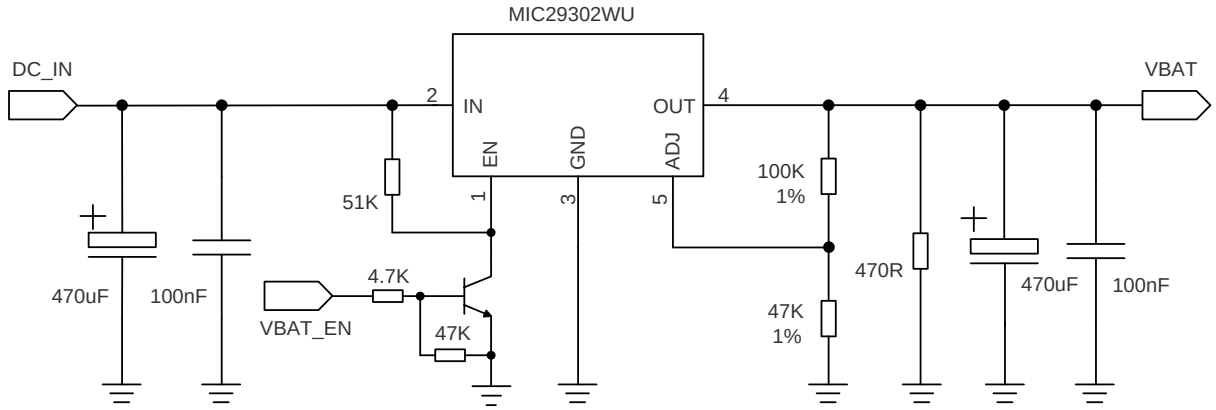


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EG91-QuecOpen is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputting a high level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

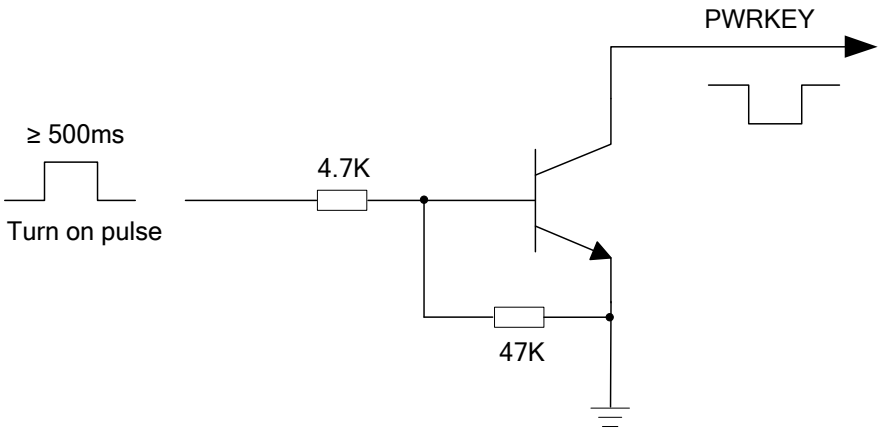


Figure 10: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

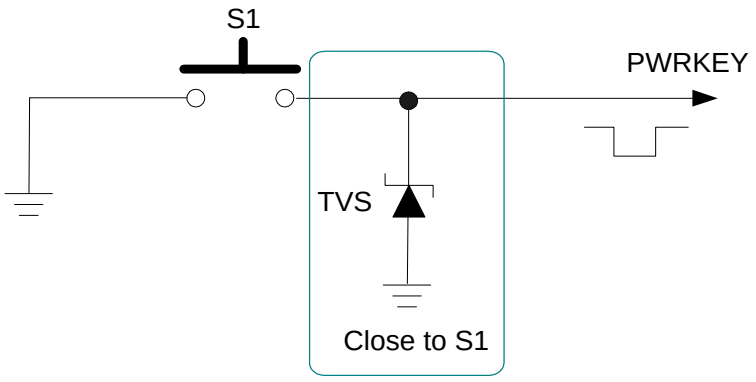


Figure 11: Turn on the Module Using Button

The turn on scenario is illustrated in the following figure.

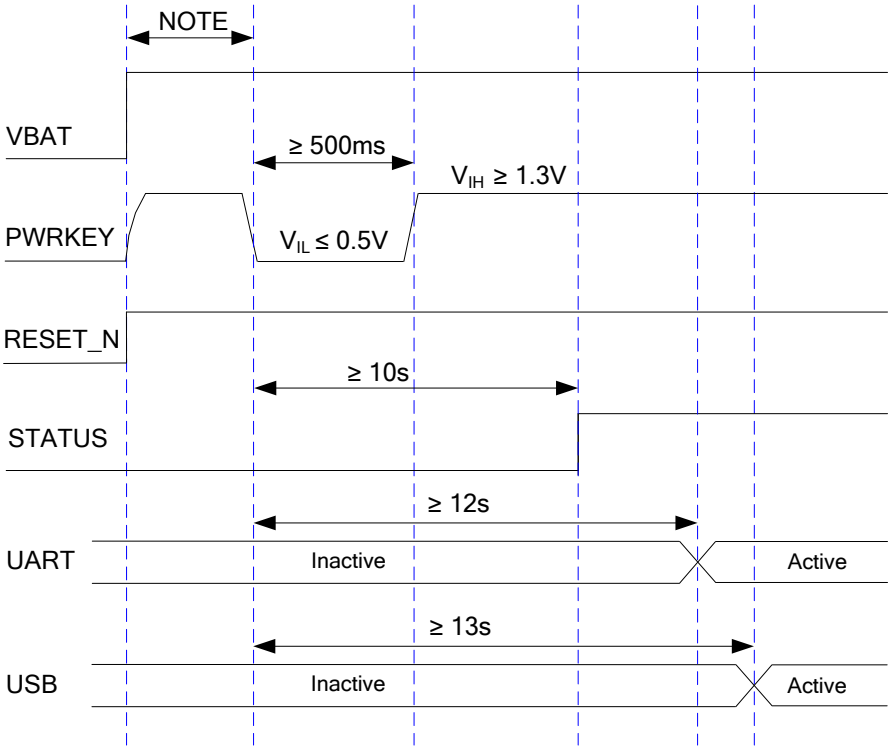


Figure 12: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.7.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

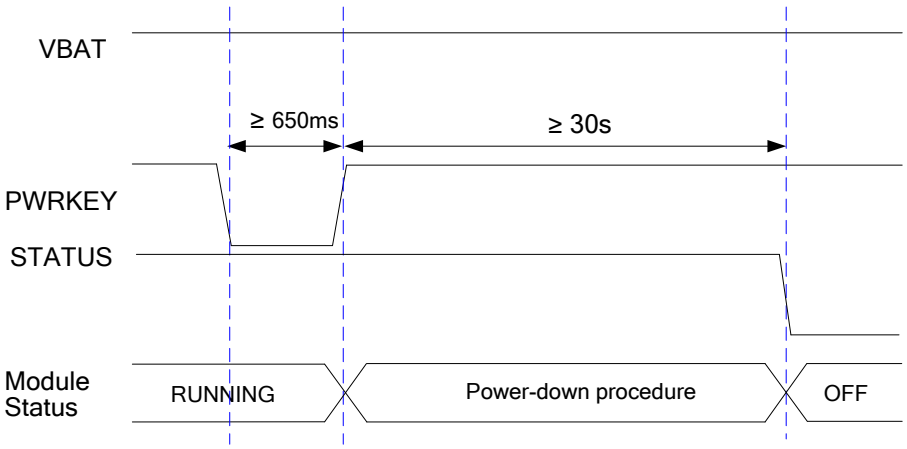


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about the **AT+QPOWD** command.

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.

3.8. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for 150ms~460ms.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

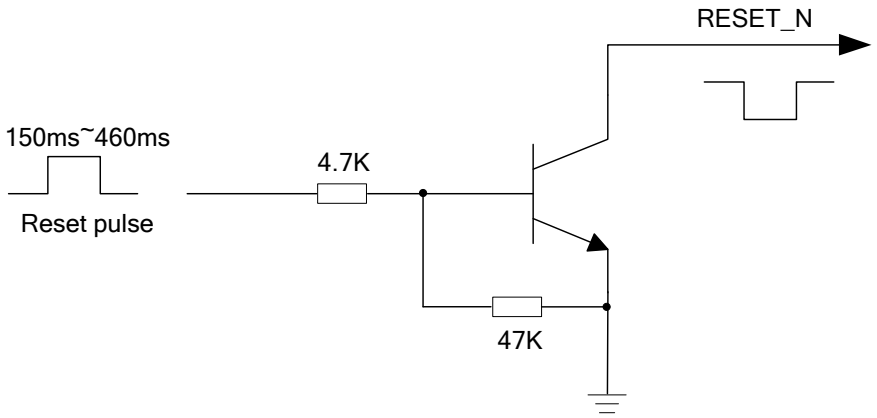


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

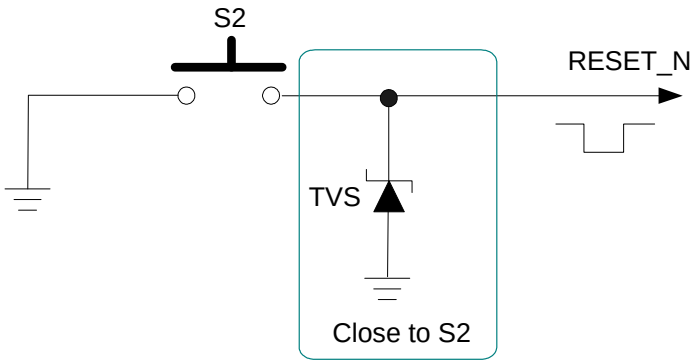


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

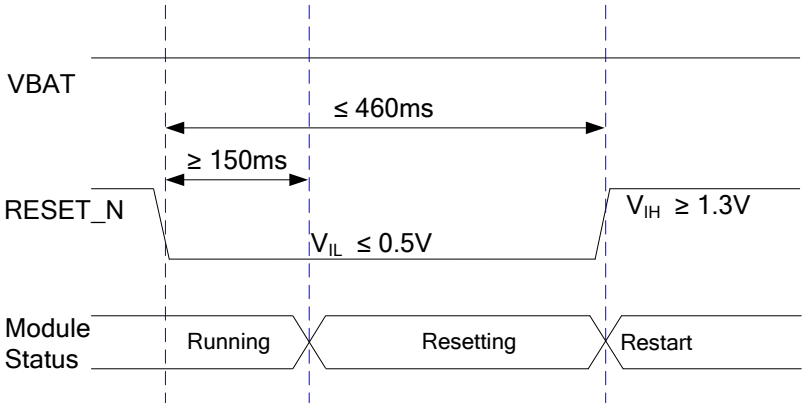


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interfaces

EG91-QuecOpen provides two (U)SIM interfaces, and only one (U)SIM card can work at a time. The (U)SIM 1 and (U)SIM 2 cards can be switched by **AT+QDSIM** command. For more details, please refer to ***document [2]***.

The (U)SIM interfaces circuitry meet ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	Power supply for (U)SIM1 card	Either 1.8V or 3.0V is supported by the module automatically.
USIM1_DATA	45	IO	Data signal of (U)SIM1 card	
USIM1_CLK	46	DO	Clock signal of (U)SIM1 card	

USIM1_RST	44	DO	Reset signal of (U)SIM1 card	
USIM1_ PRESENCE	42	DI	(U)SIM1 card insertion detection	
USIM_GND	47		Specified ground for (U)SIM card	
USIM2_VDD	87	PO	Power supply for (U)SIM2 card	Either 1.8V or 3.0V is supported by the module automatically.
USIM2_DATA	86	IO	Data signal of (U)SIM2 card	
USIM2_CLK	84	DO	Clock signal of (U)SIM2 card	
USIM2_RST	85	DO	Reset signal of (U)SIM2 card	
USIM2_ PRESENCE	83	DI	(U)SIM2 card insertion detection	

EG91-QuecOpen supports (U)SIM card hot-plug via USIM1_PRESENCE or USIM2_PRESENCE pin. The function supports low level and high level detections, and it is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command for details.

The following figure shows a reference design for (U)SIM1 interface with an 8-pin (U)SIM card connector.

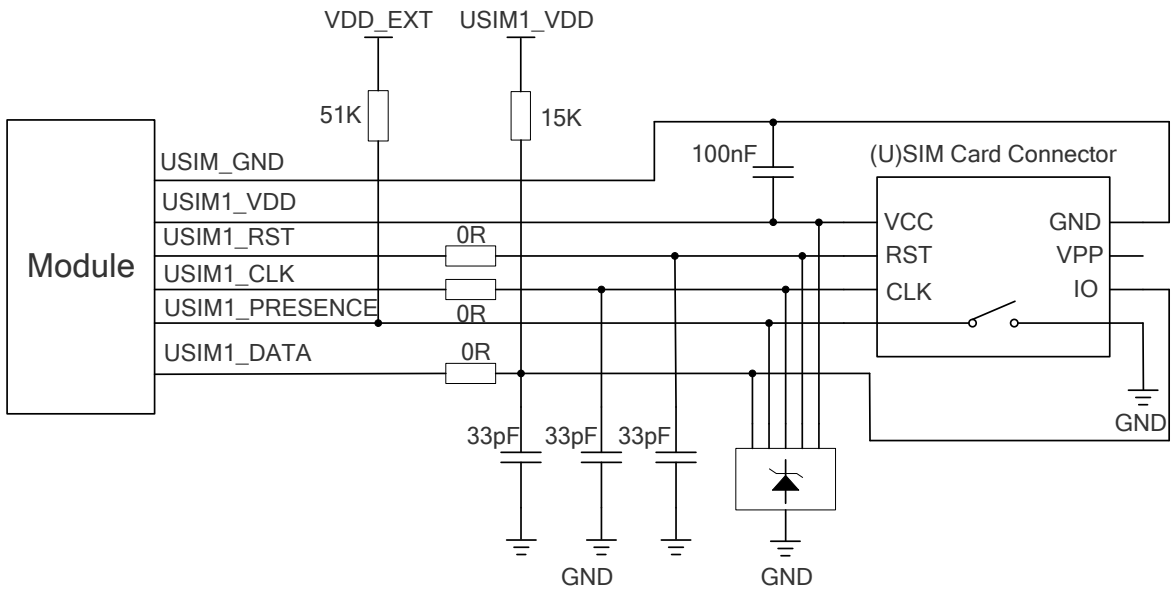


Figure 17: Reference Circuit of (U)SIM1 Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM1 card detection function is not needed, please keep USIM1_PRESENCE unconnected. A reference circuit of (U)SIM1 interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

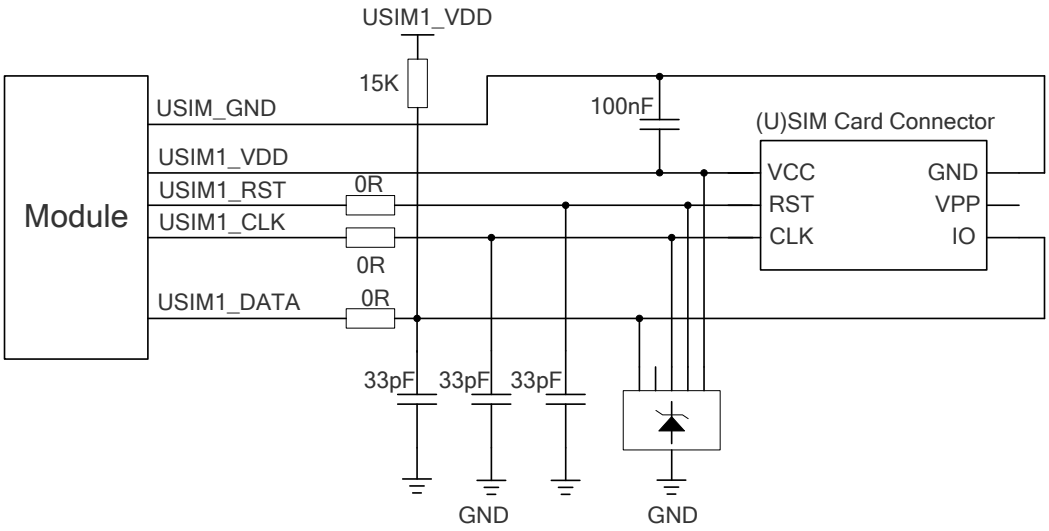


Figure 18: Reference Circuit of (U)SIM1 Interface with a 6-Pin (U)SIM Card Connector

The following figure shows a reference design of (U)SIM2 interface with an 8-pin (U)SIM card connector.

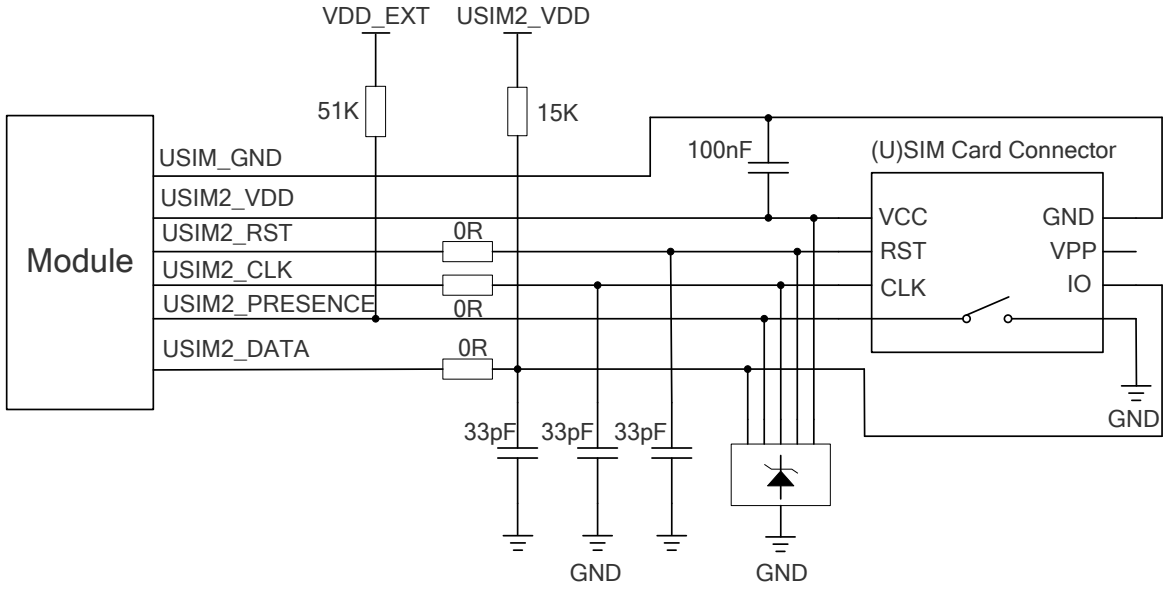


Figure 19: Reference Circuit of (U)SIM2 Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM2 card detection function is not needed, please keep USIM2_PRESENCE unconnected. A reference circuit of (U)SIM2 interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

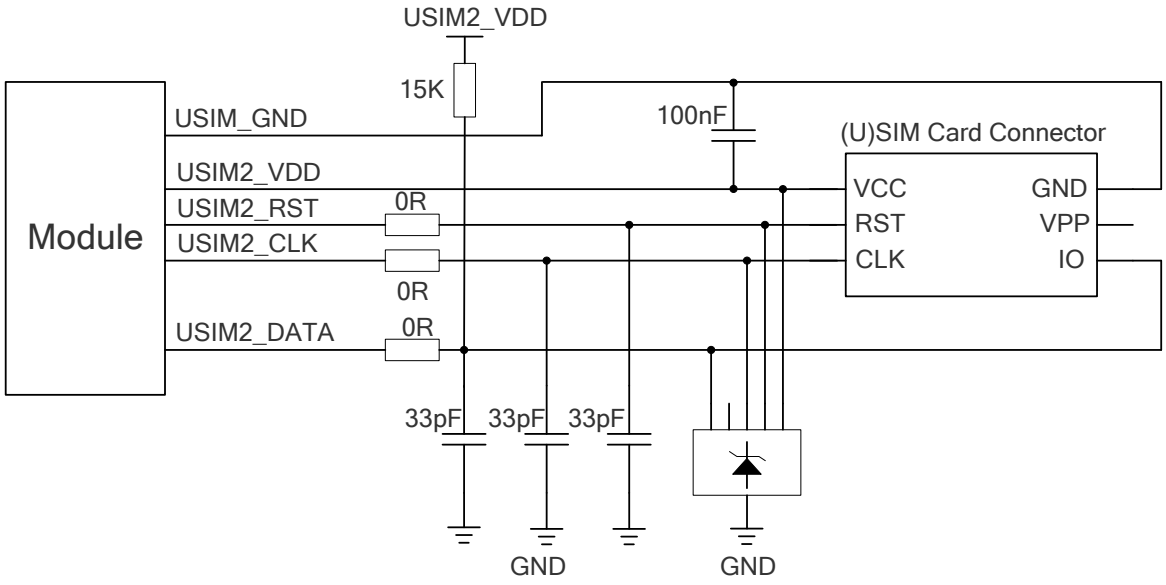


Figure 20: Reference Circuit of (U)SIM2 Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM cards in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not exceed 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. The 33pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG91-QuecOpen contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90Ω.
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90Ω.
USB_VBUS	8	PI	USB detection	Typically 5.0V
GND	3		Ground	

More details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' design. The following figure shows a reference circuit of USB interface.

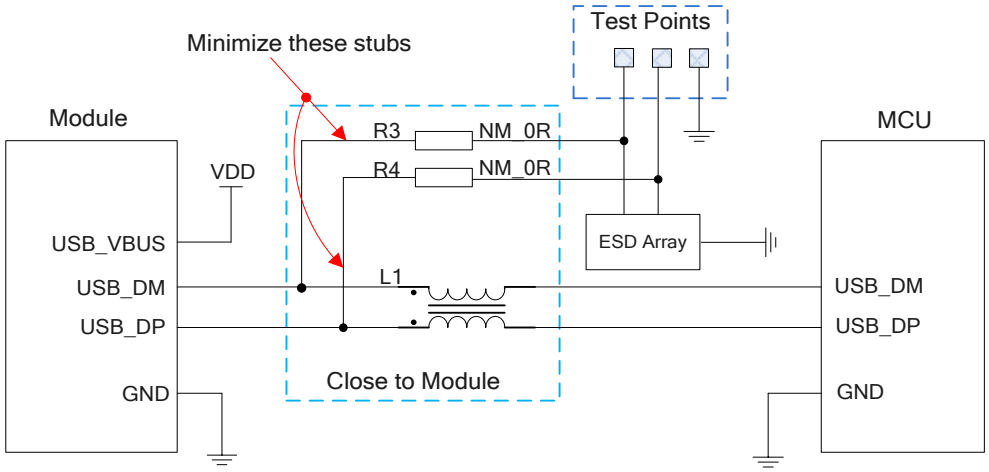


Figure 21: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be

added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection component on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EG91-QuecOpen module can only be used as a slave device.
2. "*" means under development.

3.11. UART Interfaces

The EG91-QucOpen module provides three UART interfaces: main UART interface, debug UART interface and application UART which is multiplexing from SPI interface(Pin26~28).

The application UART means that this uart interface can be contrloed by custormer application sortware and is used for communication and data transmission with peripherals while the main UART is used for AT command communication only.

The following shows their features.

- The main UART interface supports 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 3000000bps baud rates, and the default is 115200bps. The interface can only be used for AT command communication.
- The debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.
- The UART that multiplexed with SPI interface(Pin26~28) supports 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 3000000bps baud rates, and the default is 115200bps. The interface can be used for communication and data transmission with peripherals.

The following tables show the pin definition of the three UART interfaces.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indicator	1.8V power domain
DCD	38	DO	Data carrier detection	
CTS	36	DO	Clear to send	
RTS	37	DI	Request to send	
DTR	30	DI	Sleep mode control	
TXD	35	DO	Transmit data	
RXD	34	DI	Receive data	

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Transmit data	1.8V power domain
DBG_RXD	22	DI	Receive data	1.8V power domain

Table 14: Pin Definition of Application UART Interface (Multiplexed with SPI)

Pin Name	Pin No.	I/O	Description		
			function 1 (Default)	function 2	function 3
SPI_CLK	26	DO	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6
SPI_MOSI	27	DO	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6
SPI_MISO	28	DI	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6

NOTE

Due to three line of SPI interface, the application UART that multiplexed from SPI is also three line.

The logic levels are described in the following table.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

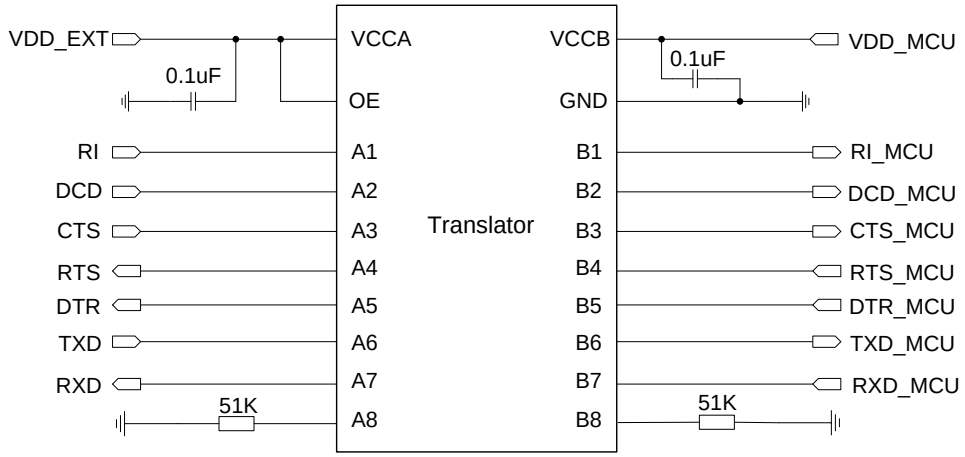


Figure 22: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the circuit design of solid line section, in terms of both module input and output circuit design. Please pay attention to the direction of connection.

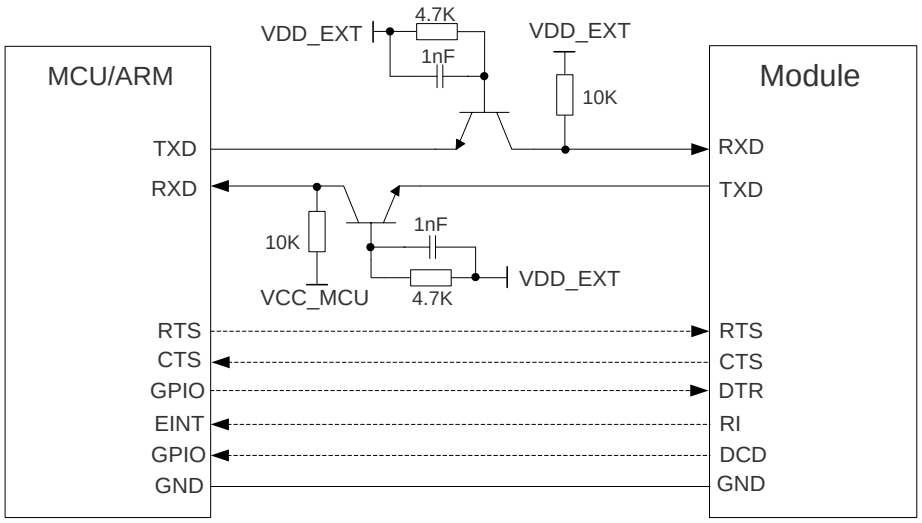


Figure 23: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.12. PCM and I2C Interfaces

EG91-QuecOpen provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

EG91-QuecOpen supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8KHz PCM_SYNC and 2048KHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8KHz PCM_SYNC and 256KHz PCM_CLK.

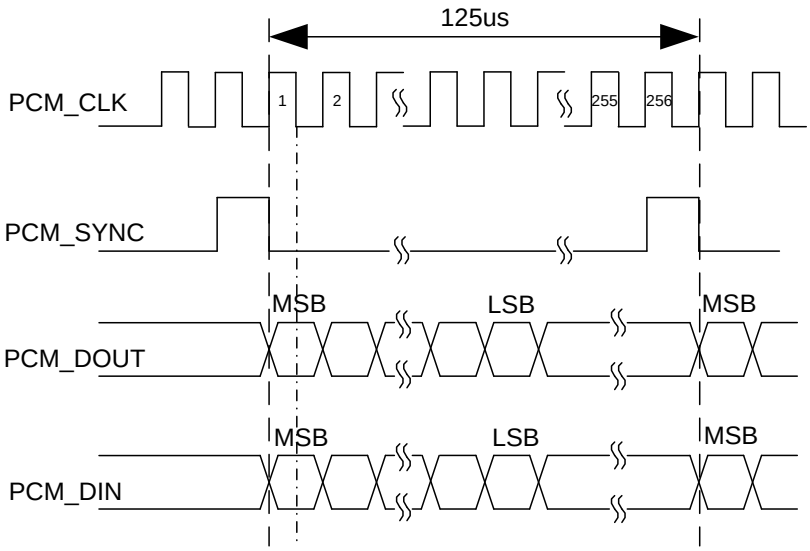


Figure 24: Primary Mode Timing

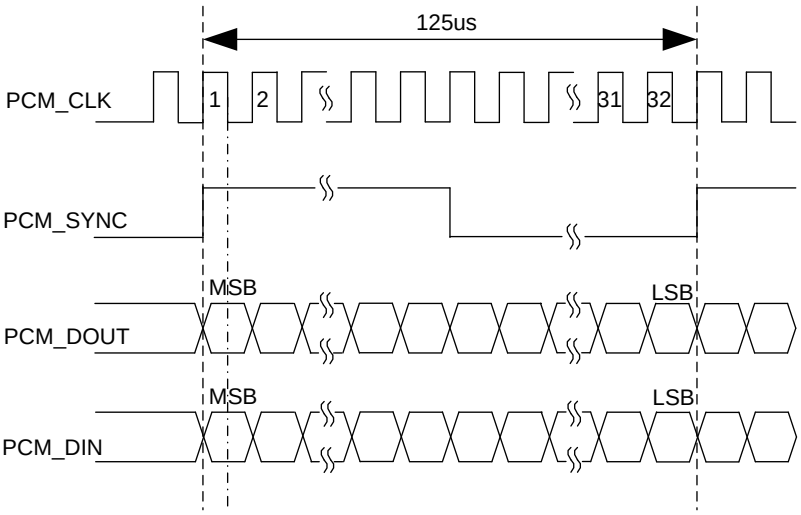


Figure 25: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 16: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8V power domain
PCM_DOUT	7	DO	PCM data output	1.8V power domain
PCM_SYNC	5	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK	4	IO	PCM data bit clock	1.8V power domain
I2C_SCL	40	OD	I2C serial clock	Require an external pull-up to 1.8V
I2C_SDA	41	OD	I2C serial data	Require an external pull-up to 1.8V

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048KHz PCM_CLK and 8KHz PCM_SYNC. Please refer to ***document [2]*** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM interface with external codec IC.

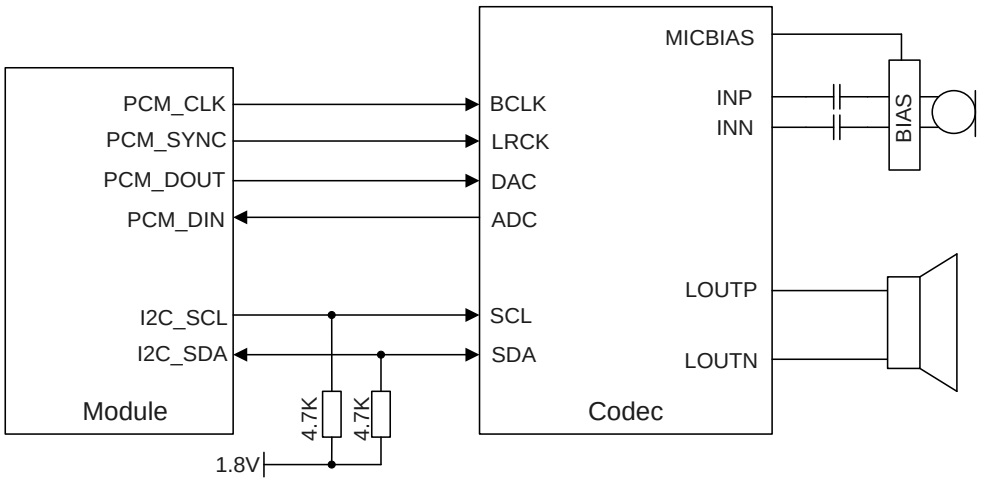


Figure 26: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG91-QuecOpen works as a master device pertaining to I2C interface.

3.13. SPI Interface

SPI interface of EG91-QuecOpen acts as the master only. It provides a duplex, synchronous and serial communication link with the peripheral devices. It is dedicated to one-to-one connection, without chip select. Its operation voltage is 1.8V with clock rates up to 50MHz.

The following table shows the pin definition of SPI interface.

Table 17: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	Clock signal of SPI interface	1.8V power domain
SPI_MOSI	27	DO	Master output slave input of SPI interface	1.8V power domain
SPI_MISO	28	DI	Master input slave output of SPI interface	1.8V power domain

The following figure shows a reference design of SPI interface with peripherals.

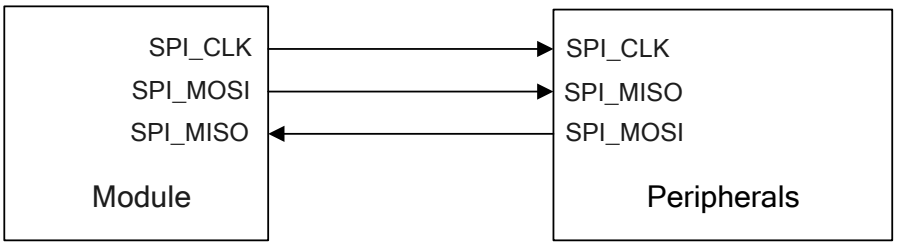


Figure 27: Reference Circuit of SPI Interface with Peripherals

3.14. Network Status Indication

The module provides one network indication pin: NETLIGHT. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

Table 18: Pin Definition of Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8V power domain

Table 19: Working State of the Network Status Indicator

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

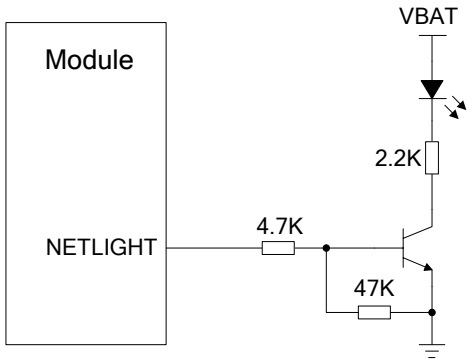


Figure 28: Reference Circuit of the Network Status Indicator

3.15. STATUS

The STATUS pin is set as the module's operation status indicator. It will output high level when the module is powered on. The following table describes the pin definition of STATUS.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8V power domain

A reference circuit is shown as below.

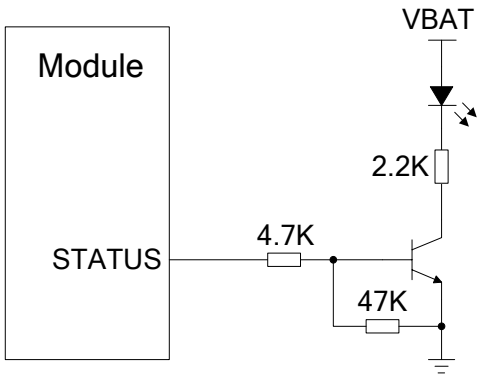


Figure 29: Reference Circuit of STATUS

3.16. Behaviors of RI

AT+QCFG="risignaltype","physical" command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behaviors of the RI are shown as below.

Table 21: Default Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120ms low pulse when a new URC returns

The default RI behaviors can be changed by **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [2]*** for details.

3.17. USB_BOOT Interface

EG91-QuecOpen provides a USB_BOOT pin. Developers can pull up the USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into forced download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 22: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to boot from USB port	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

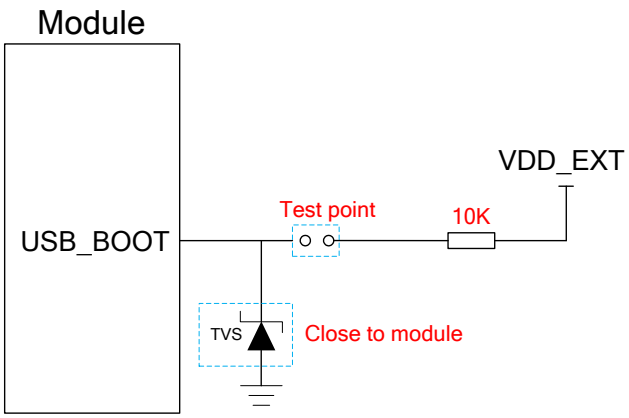


Figure 30: Reference Circuit of USB_BOOT Interface

3.18. GPIOs

EG91-QuecOpen module provides some multi-function pins that can be configured as GPIOs when their default function are not been used. The following table show the alternate GPIO function of this pins in EG91-QuecOpen module.

Table 23: Alternate GPIO Function of the Multi-function Pins

Pin Name	Pin No.	Default Function	GPIOs	Comment
PCM_CLK	4	PCM_CLK	GPIO_78	BOOT_CONFIG_8
PCM_SYNC	5	PCM_SYNC	GPIO_79	BOOT_CONFIG_7
PCM_DIN	6	PCM_DIN	GPIO_76	
PCM_DOUT	7	PCM_DOUT	GPIO_77	
AP_READY	19	AP_READY	GPIO_10	
NETLIGHT	21	PMD[1)] (GPIO_01)	NETLIGHT	
SPI_CLK	26	SPI_CLK	GPIO_23	BOOT_CONFIG_4
SPI_MOSI	27	SPI_MOSI	GPIO_20	
SPI_MISO	28	SPI_MISO	GPIO_21	
RI	39	RI	GPIO_75	
I2C_SCL	40	I2C_SCL	GPIO_7	
I2C_SDA	41	I2C_SDA	GPIO_6	
USIM1_PRESENCE	42	USIM1_PRESENCE	GPIO_34	

NOTES

1. The power domian of this pins are 1.8V, pay attention to the logic level when design with peripheral.
2. [1)]means the GPIO that located on PMD of Qualcomm chipset.
3. All BOOT_CONFIG pins are prohibited to be pulled up before the module is powered on.

4 GNSS Receiver

4.1. General Description

EG91-QuecOpen includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EG91-QuecOpen supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EG91-QuecOpen GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EG91-QuecOpen.

Table 24: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	34.7	s
		XTRA enabled	2.42	s
	Warm start @open sky	Autonomous	29.34	s
		XTRA enabled	2.29	s

	Hot start @open sky	Autonomous	2.19	s
		XTRA enabled	1.73	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to ***Chapter 5*** for GNSS reference design and antenna installation information.

5 Antenna Interfaces

EG91-QuecOpen antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface which is only supported on EG91-NA-QuecOpen. The impedance of the antenna port is 50Ω.

5.1. Main/Rx-diversity Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 25: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna pad	50Ω impedance
ANT_DIV (EG91-E-QuecOpen)	49	AI	Receive diversity antenna pad	50Ω impedance
ANT_DIV (EG91-NA-QuecOpen)	56	AI	Receive diversity antenna pad	50Ω impedance

5.1.2. Operating Frequency

Table 26: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1850~1910	1930~1990	MHz

WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE FDD B4	1710~1755	2110~2155	MHz
LTE FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE FDD B12	699~716	729~746	MHz
LTE FDD B13	777~787	746~756	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B28A	703~733	758~788	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

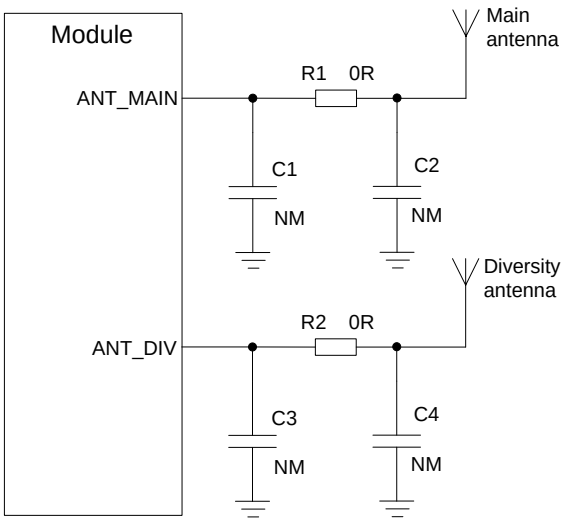


Figure 31: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity.
3. Place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

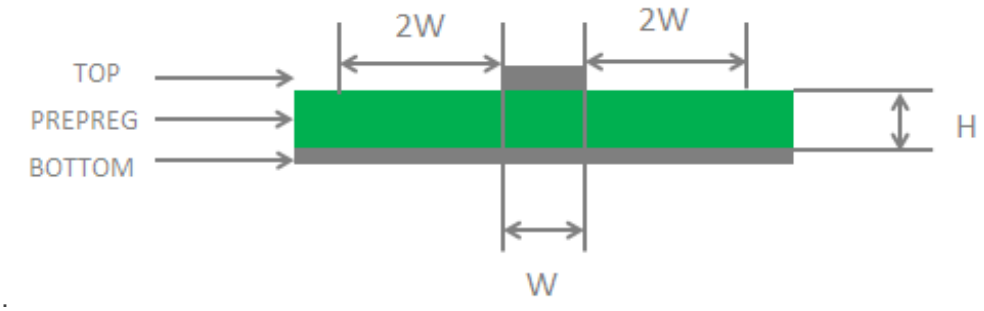


Figure 32: Microstrip Line Design on a 2-layer PCB

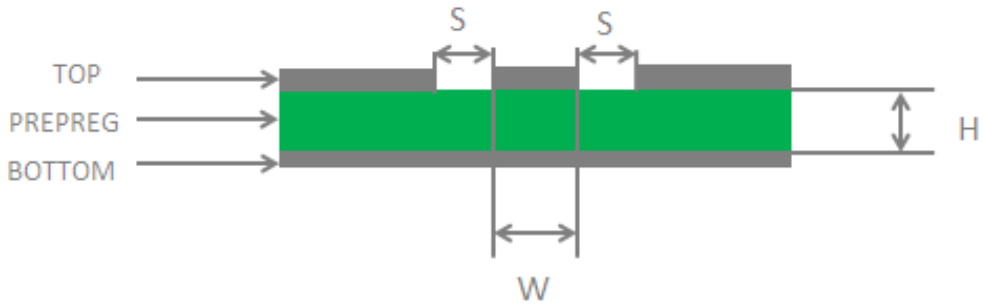


Figure 33: Coplanar Waveguide Line Design on a 2-layer PCB

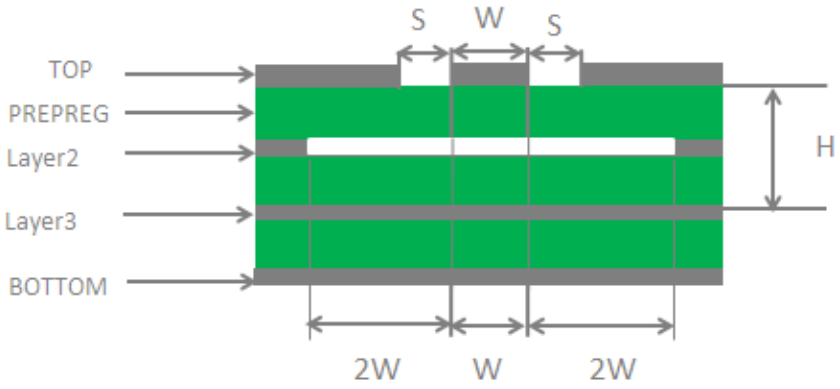


Figure 34: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

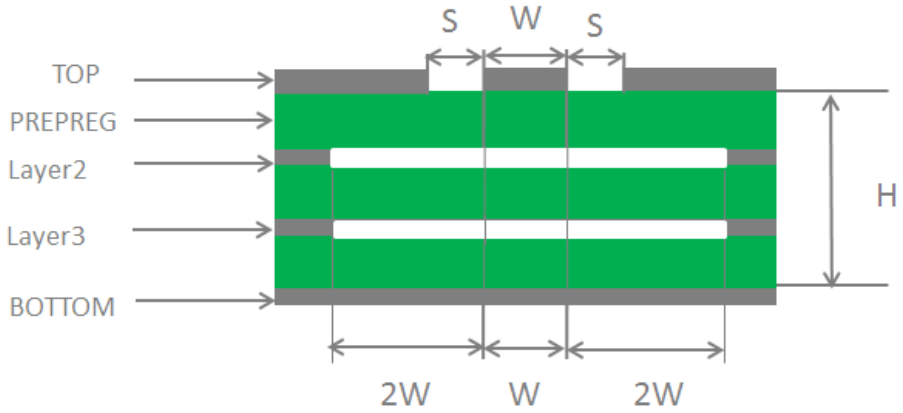


Figure 35: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [4]***.

5.2. GNSS Antenna Interface

The GNSS antenna interface is only supported on EG91-NA-QuecOpen. The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 27: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS (EG91-NA-QuecOpen)	49	AI	GNSS antenna	50Ω impedance

Table 28: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
Galileo	1575.42±2.046	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

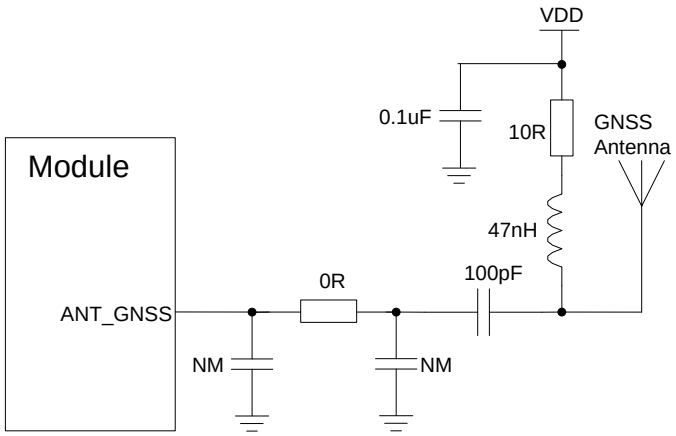


Figure 36:Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 29: Antenna Requirements

Type	Requirements
GNSS[1)]	Frequency range: 1559MHz ~ 1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17dB
GSM/WCDMA/LTE	VSWR: ≤ 2 Efficiency : > 30% Max Input Power: 50 W Input Impedance: 50Ω Cable insertion loss: < 1dB (EGSM900,WCDMA B5/B8, LTE B5/B8/B12/B13/B20/B28A) Cable Insertion Loss: < 1.5dB (DCS1800, WCDMA B1/B2/B4, LTE B1/B2/B3/B4) Cable insertion loss: < 2dB (LTE B7)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

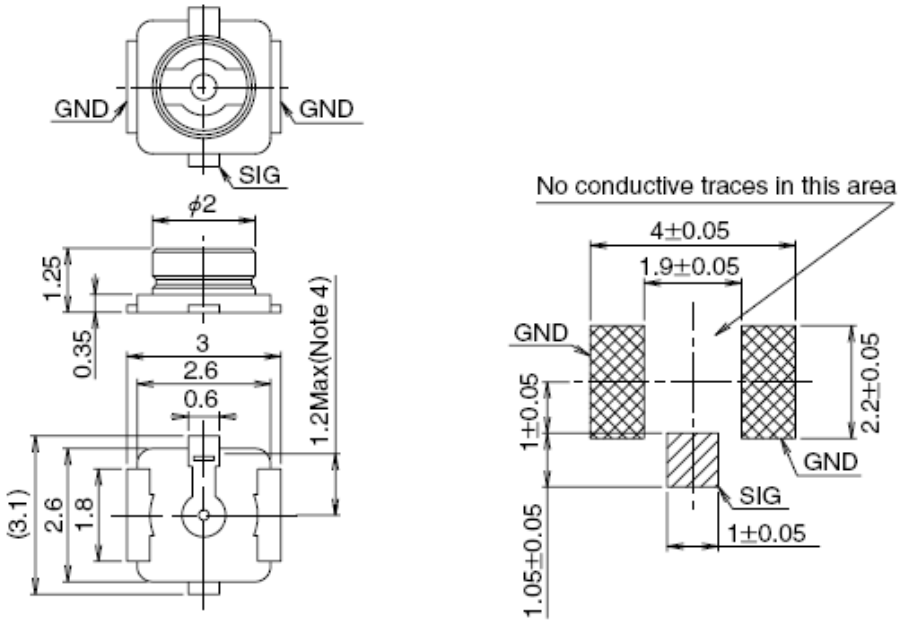


Figure 37: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

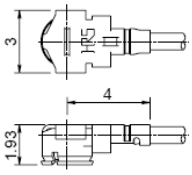
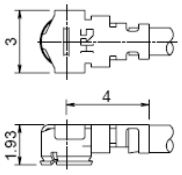
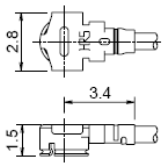
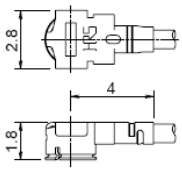
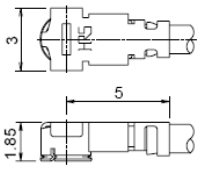
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

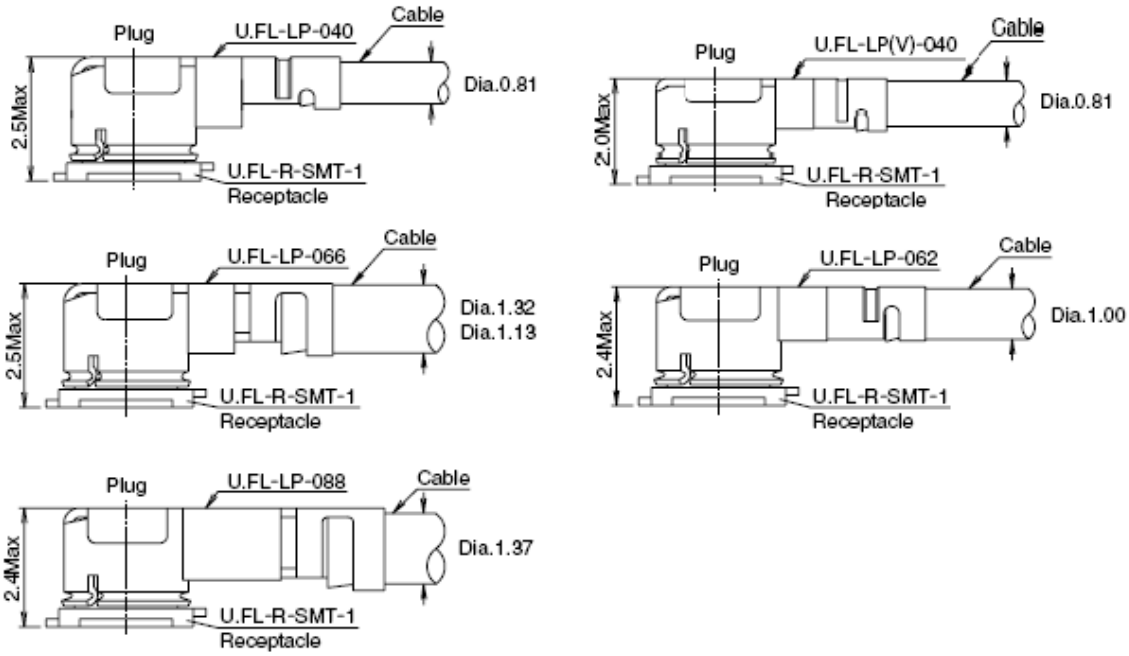


Figure 39: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 31: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 32: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1]	-35	+25	+75	ºC
Extended Temperature Range [2]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The values of current consumption are shown below.

Table 33: EG91-E-QuecOpen Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
		GSM DRX=2 (USB disconnected)	2.0	mA
		GSM DRX=5 (USB suspend)	1.9	mA
		GSM DRX=9 (USB disconnected)	1.3	mA
		WCDMA PF=64 (USB disconnected)	1.7	mA
		WCDMA PF=64 (USB suspend)	2.1	mA
		WCDMA PF=512 (USB disconnected)	1.1	mA
		LTE-FDD PF=64 (USB disconnected)	2.1	mA
		LTE-FDD PF=64 (USB suspend)	2.6	mA
		LTE-FDD PF=256 (USB disconnected)	1.4	mA
	Idle state	GSM DRX=5 (USB disconnected)	19.0	mA
		GSM DRX=5 (USB connected)	29.0	mA
		WCDMA PF=64 (USB disconnected)	19.0	mA
		WCDMA PF=64 (USB connected)	29.0	mA
		LTE-FDD PF=64 (USB disconnected)	19.0	mA
		LTE-FDD PF=64 (USB connected)	29.0	mA
	GPRS data transfer	EGSM900 4DL/1UL @32.67dBm	260	mA
		EGSM900 3DL/2UL @32.59dBm	463	mA
		EGSM900 2DL/3UL @30.74dBm	552	mA

		EGSM900 1DL/4UL @29.26dBm	619	mA
		DCS1800 4DL/1UL @29.2dBm	165	mA
		DCS1800 3DL/2UL @29.13dBm	267	mA
		DCS1800 2DL/3UL @29.01dBm	406	mA
		DCS1800 1DL/4UL @28.86dBm	467	mA
	EDGE data transfer	EGSM900 4DL/1UL PCL=8 @27.1dBm	163	mA
		EGSM900 3DL/2UL PCL=8 @27.16dBm	274	mA
		EGSM900 2DL/3UL PCL=8 @26.91dBm	383	mA
		EGSM900 1DL/4UL PCL=8 @26.12dBm	463	mA
		DCS1800 4DL/1UL PCL=2 @25.54dBm	136	mA
		DCS1800 3DL/2UL PCL=2 @25.68dBm	220	mA
		DCS1800 2DL/3UL PCL=2 @25.61dBm	306	mA
		DCS1800 1DL/4UL PCL=2 @25.41dBm	396	mA
	WCDMA data transfer	WCDMA B1 HSDPA CH10700 @22.29dBm	507	mA
		WCDMA B1 HSUPA CH10700 @21.79dBm	516	mA
		WCDMA B8 HSDPA CH3012 @22.47dBm	489	mA
		WCDMA B8 HSUPA CH3012 @21.98dBm	482	mA
	LTE data transfer	LTE-FDD B1 CH18300 @22.98dBm	685	mA
		LTE-FDD B3 CH19575 @23.23dBm	698	mA
		LTE-FDD B7 CH21100 @23.46dBm	723	mA
		LTE-FDD B8 CH21625 @23.35dBm	655	mA
		LTE-FDD B20 CH24300 @23.41dBm	723	mA
		LTE-FDD B28A CH27360 @23.16dBm	660	mA
	GSM voice call	EGSM900 PCL=5 @32.5dBm	258	mA
		DCS1800 PCL=0 @29.23dBm	159	mA

	WCDMA voice call	WCDMA B1 CH10700 @23.06dBm	555	mA
		WCDMA B8 CH3012 @23.45dBm	535	mA

Table 34: EG91-NA-QuecOpen Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	TBD	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
		WCDMA PF=64 (USB disconnected)	TBD	mA
		WCDMA PF=64 (USB suspend)	TBD	mA
		WCDMA PF=512 (USB disconnected)	TBD	mA
		LTE-FDD PF=64 (USB disconnected)	TBD	mA
		LTE-FDD PF=64 (USB suspend)	TBD	mA
		LTE-FDD PF=256 (USB disconnected)	TBD	mA
	Idle state	WCDMA PF=64 (USB disconnected)	TBD	mA
		WCDMA PF=64 (USB connected)	TBD	mA
		LTE-FDD PF=64 (USB disconnected)	TBD	mA
		LTE-FDD PF=64 (USB connected)	TBD	mA
	WCDMA data transfer	WCDMA B2 HSDPA @ TBD dBm	TBD	mA
		WCDMA B2 HSUPA @ TBD dBm	TBD	mA
		WCDMA B4 HSDPA @ TBD dBm	TBD	mA
		WCDMA B4 HSUPA @ TBD dBm	TBD	mA
		WCDMA B5 HSDPA @ TBD dBm	TBD	mA
		WCDMA B5 HSUPA @ TBD dBm	TBD	mA
	LTE data transfer	LTE-FDD B2 @ TBD dBm	TBD	mA
		LTE-FDD B4 @ TBD dBm	TBD	mA

		LTE-FDD B5 @ TBD dBm	TBD	mA
		LTE-FDD B12 @ TBD dBm	TBD	mA
		LTE-FDD B13 @ TBD dBm	TBD	mA
	WCDMA voice call	WCDMA B2 @ TBD dBm	TBD	mA
		WCDMA B4 @ TBD dBm	TBD	mA
		WCDMA B5 @ TBD dBm	TBD	mA

Table 35: GNSS Current Consumption of EG91-NA-QuecOpen

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	TBD	mA
		Lost state @Passive Antenna	TBD	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	TBD	mA
		Open Sky @Passive Antenna	TBD	mA
		Open Sky @Active Antenna	TBD	mA

6.5. RF Output Power

The following table shows the RF output power of EG91-QuecOpen module.

Table 36: RF Output Power

Frequency	Max.	Min.
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
EGSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800 (8-PSK)	26dBm±3dB	0dBm±5dB

WCDMA B1/B2/B4/B5/B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1/B2/B3/B4/B5/B7/ B8/B12/B13/B20/B28A	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of EG91-QuecOpen module.

Table 37: EG91-E-QuecOpen Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-108.6dBm	NA	NA	-102dBm
DCS1800	-109.4 dBm	NA	NA	-102dbm
WCDMA B1	-109.5dBm	-110dBm	-112.5dBm	-106.7dBm
WCDMA B8	-109.5dBm	-110dBm	-112.5dBm	-103.7dBm
LTE-FDD B1 (10M)	-97.5dBm	-98.3dBm	-101.4dBm	-96.3dBm
LTE-FDD B3 (10M)	-98.3dBm	-98.5dBm	-101.5dBm	-93.3dBm
LTE-FDD B7 (10M)	-96.3dBm	-98.4dBm	-101.3dBm	-94.3dBm
LTE-FDD B8 (10M)	-97.1dBm	-99.1dBm	-101.2dBm	-93.3dBm
LTE-FDD B20 (10M)	-97dBm	-99dBm	-101.3dBm	-93.3dBm
LTE-FDD B28A (10M)	-98.3dBm	-99dBm	-101.4dBm	-94.8dBm

Table 38: EG91-NA-QuecOpen Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	TBD	TBD	TBD	-104.7dBm
WCDMA B4	TBD	TBD	TBD	-106.7dBm
WCDMA B5	TBD	TBD	TBD	-104.7dBm
LTE-FDD B2 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B4 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B5 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B12 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B13 (10M)	TBD	TBD	TBD	-93.3dBm

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 39: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
All Antenna Interfaces	±4	±8	KV
Other Interfaces	±0.5	±1	KV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.
- The size of the heatsink should be larger than that of the module's shielding cover to avoid the deformation of the shielding cover.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

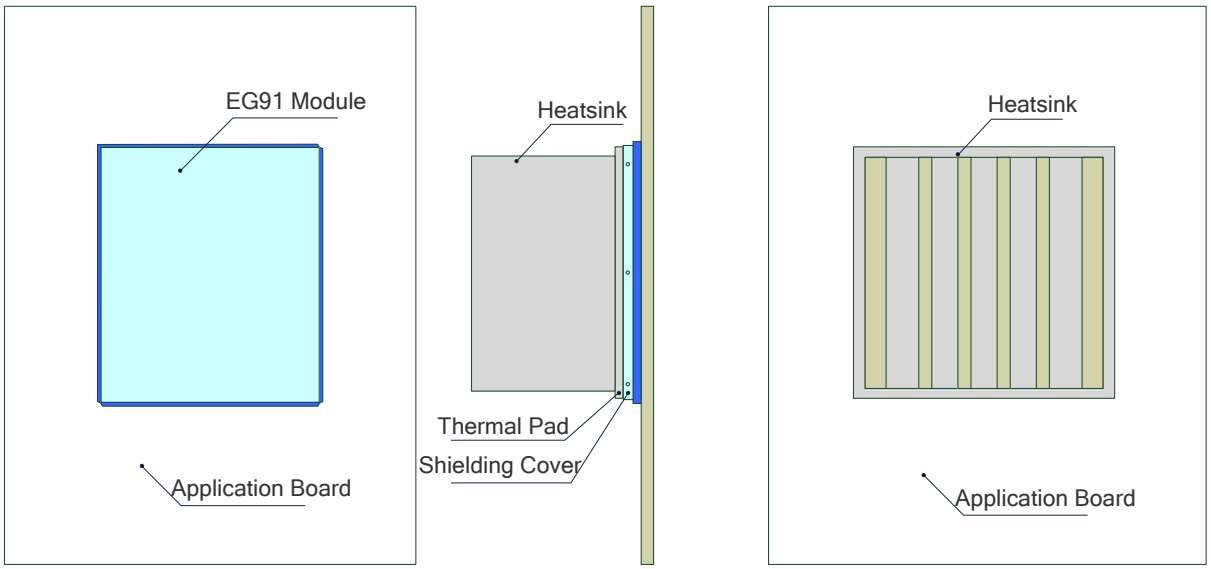


Figure 40: Referenced Heatsink Design (Heatsink at the Top of the Module)

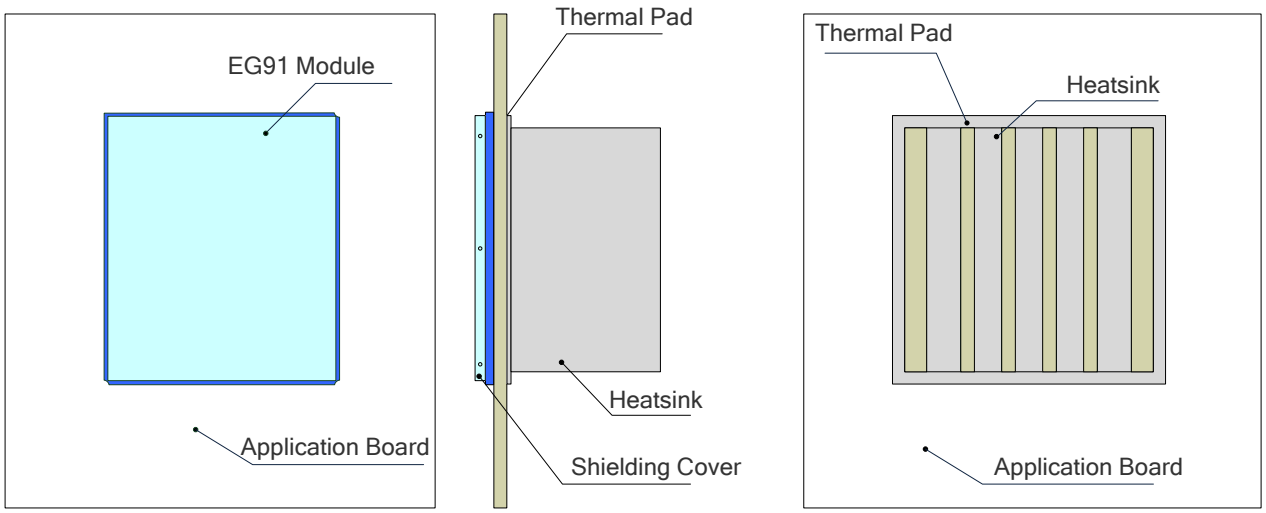


Figure 41: Referenced Heatsink Design (Heatsink at the Bottom of Customers' PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

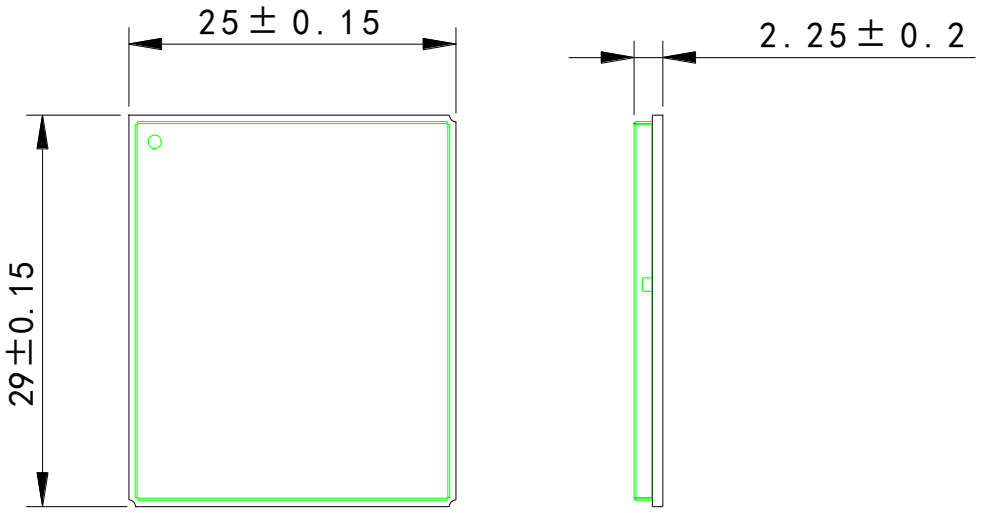


Figure 42: Module Top and Side Dimensions

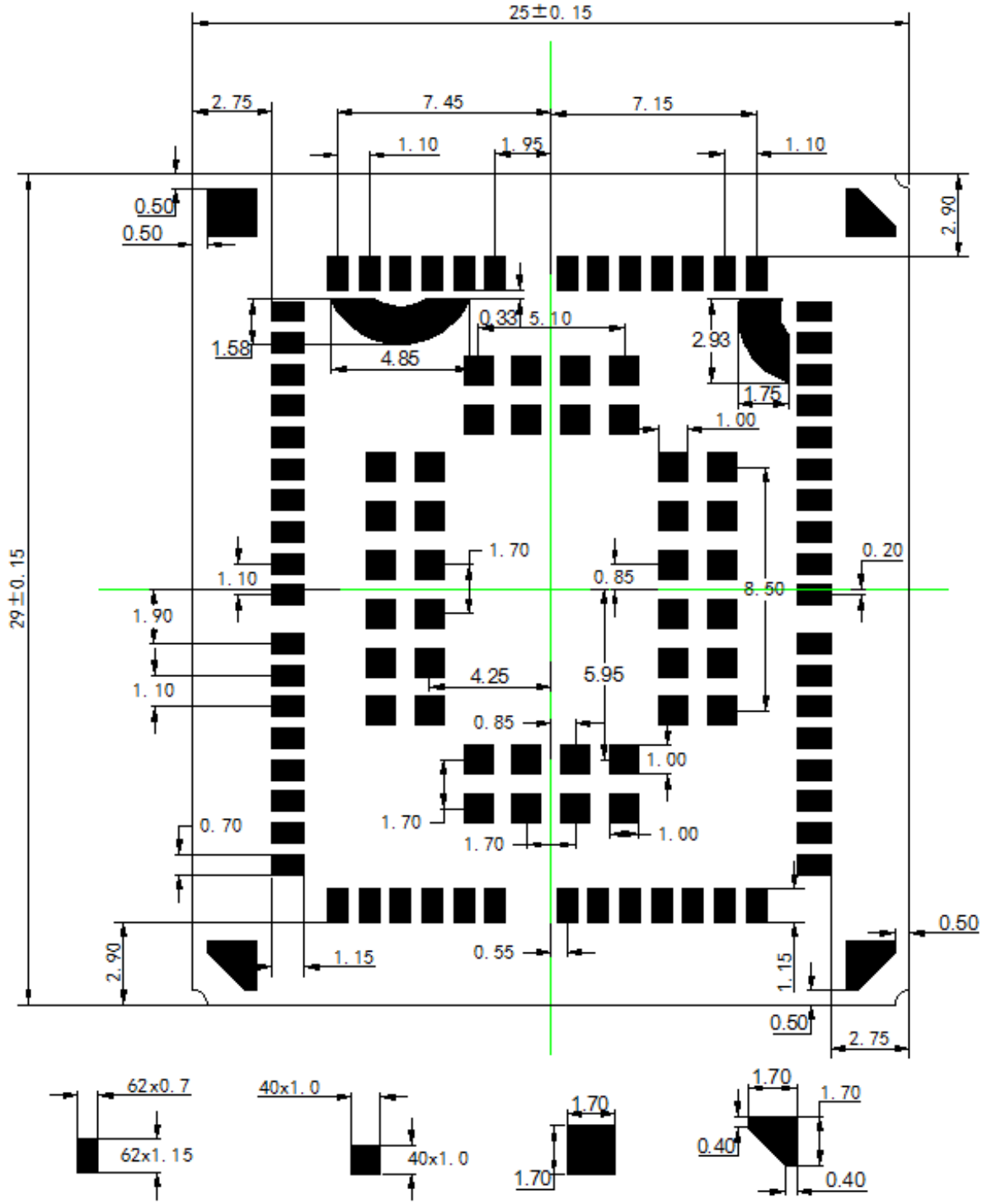


Figure 43: Module Bottom Dimensions (Top View)

7.2. Recommended Footprint

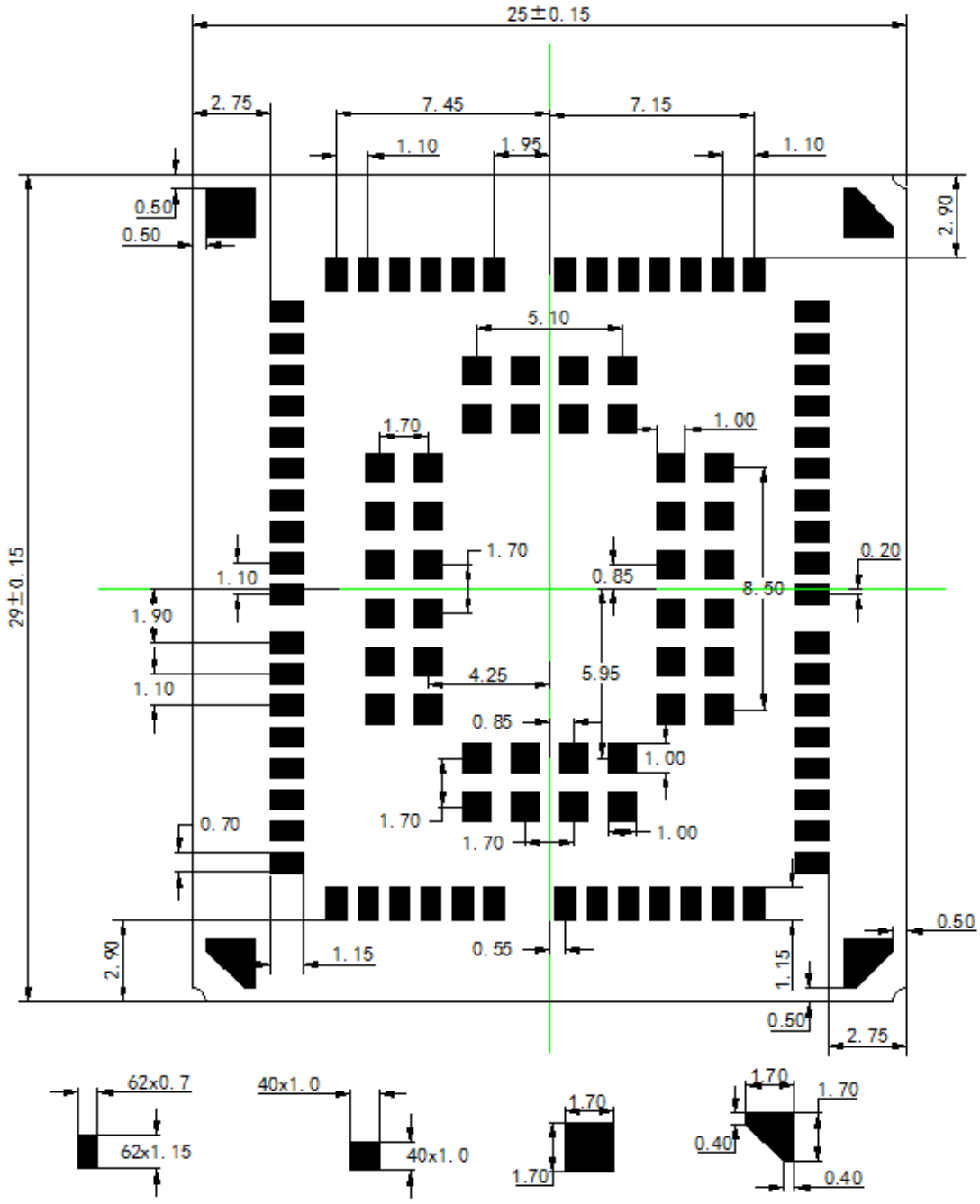


Figure 44: Recommended Footprint (Top View)

NOTE

For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

7.3. Design Effect Drawings of the Module

Figure 45: Top View of the Module

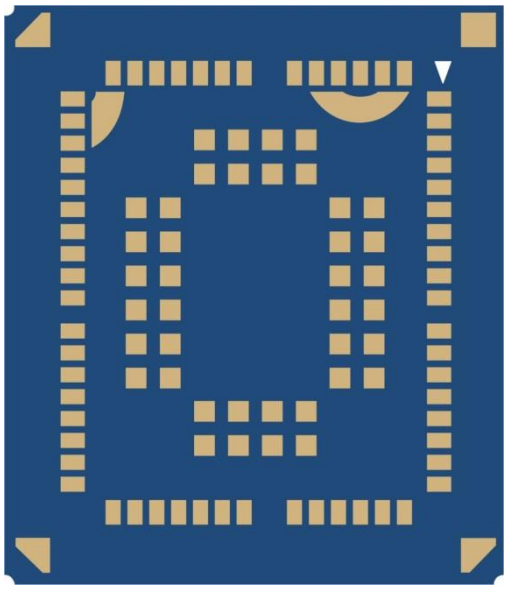


Figure 46: Bottom View of the Module

NOTE

These are design effect drawings of EG91-QuecOpen module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EG91-QuecOpen is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

- Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
- Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.

- When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
- Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm. For more details, please refer to ***document [3]***.

It is suggested that the peak reflow temperature is 235ºC~245ºC (for SnAg3.0Cu0.5 alloy). The absolute maximum reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

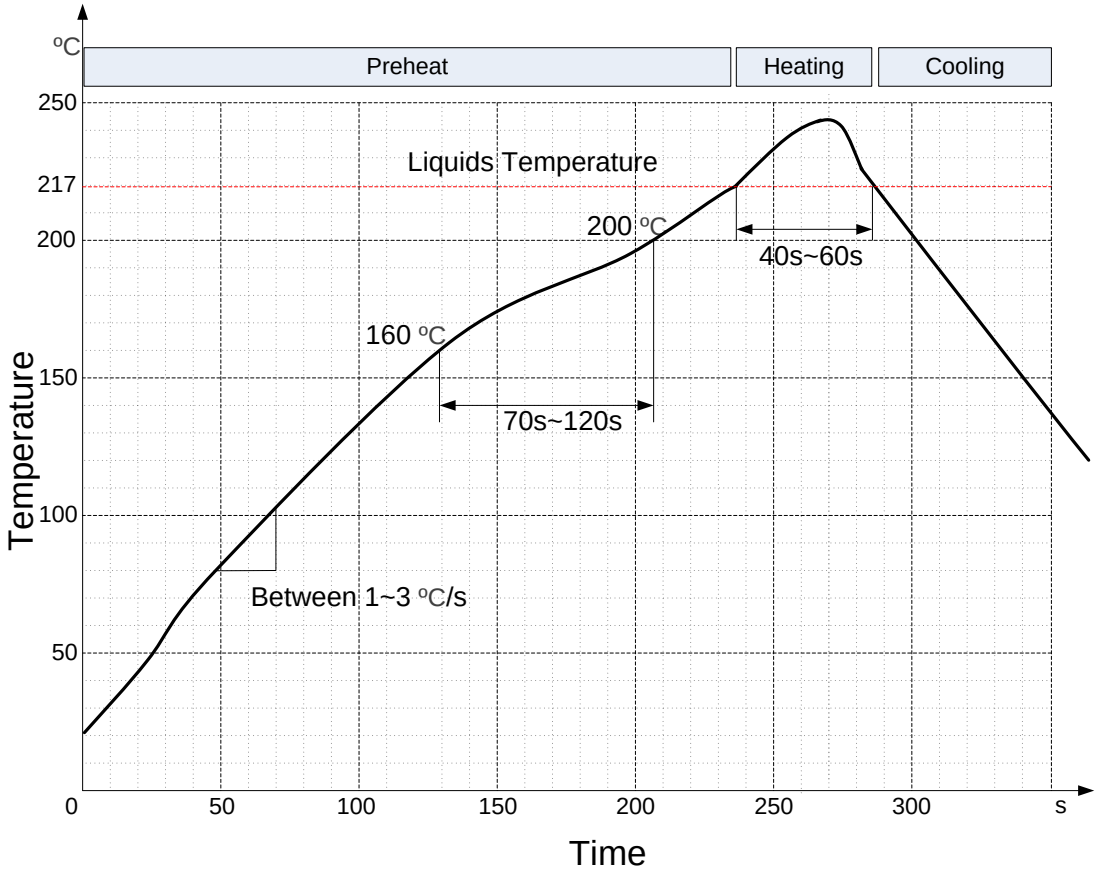


Figure 47: Reflow Soldering Thermal Profile

8.3. Packaging

EG91-QuecOpen is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330mm in diameter and each reel contains 250pcs modules. The following figures show the packaging details, measured in mm.

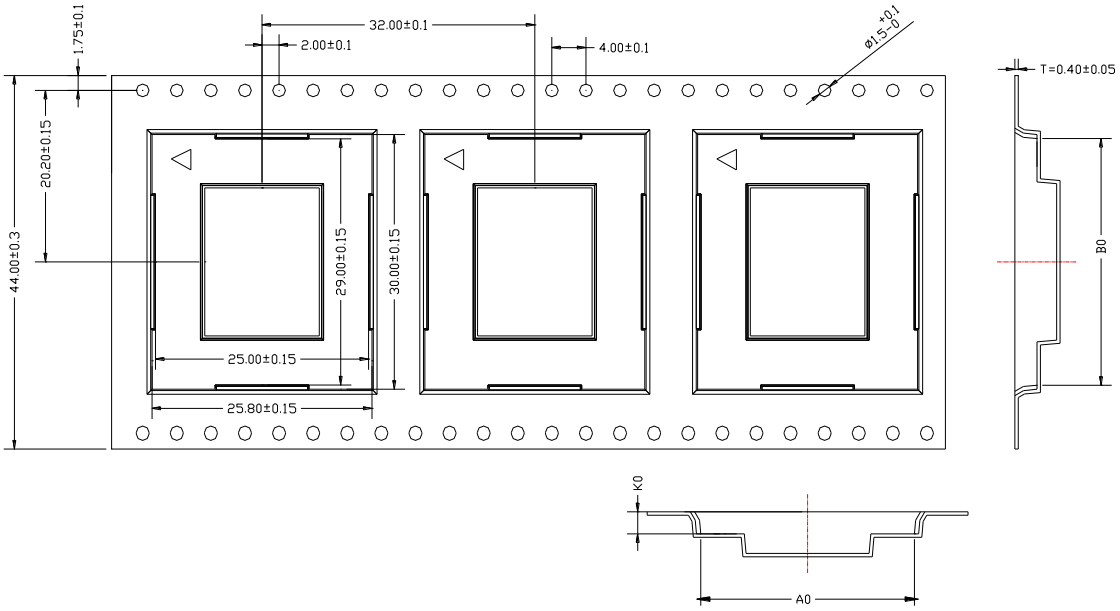


Figure 48: Tape Dimensions

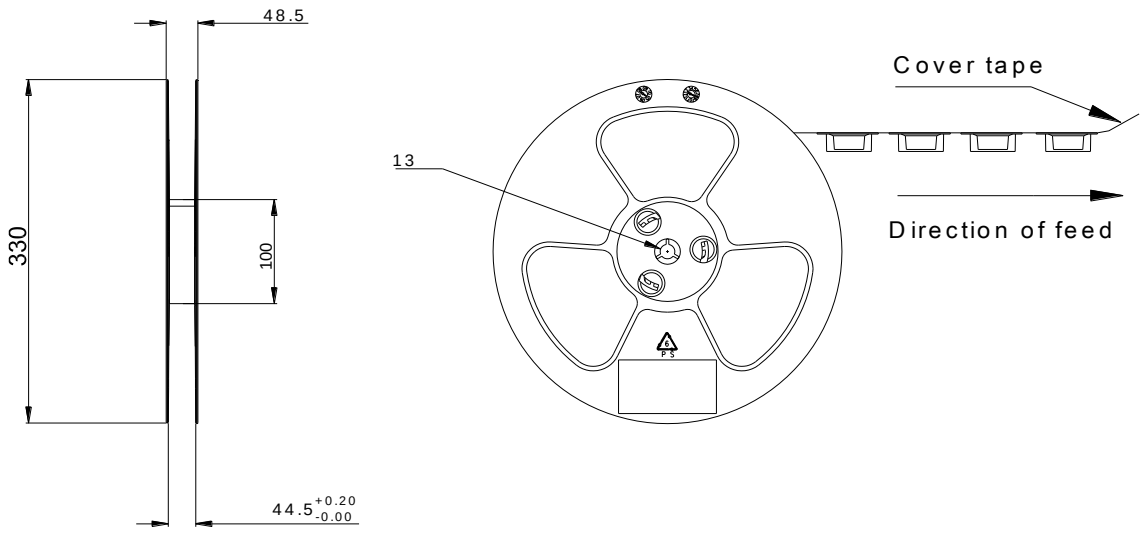


Figure 49: Reel Dimensions

9 Appendix A References

Table 40: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x&EM05_Power_Management_Application_Note	Power Management Application Note for EC25, EC21, EC20 R2.0, EC20 R2.1, EG95, EG91 and EM05
[2]	Quectel_EG9x_AT_Commands_Manual	AT Commands Manual for EG95 and EG91
[3]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note

Table 41: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission

EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PMD	Power Management Device
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{O}ax	Maximum Output High Level Voltage Value
V_{O}in	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

WCDMA	Wideband Code Division Multiple Access

10 Appendix B GPRS Coding Schemes

Table 42: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 43: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 44: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps