EC2x&AG35-Quecopen NAU8810 Codec Debugging Guidelines

LTE Standard/Automotive Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2018-02-22	Thirty XU	Initial

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1 Introduction

This document mainly introduces the debugging methods of gain registers in ADC/DAC paths of NAU8810 referring to the datasheet of NAU8810 Codec, which applies for users to debug the volume of NAU8810 Codec.

2 Audio Paths Introduction

NAU8810 hardware block diagram that the software defaults to apply is illustrated by the arrows below.

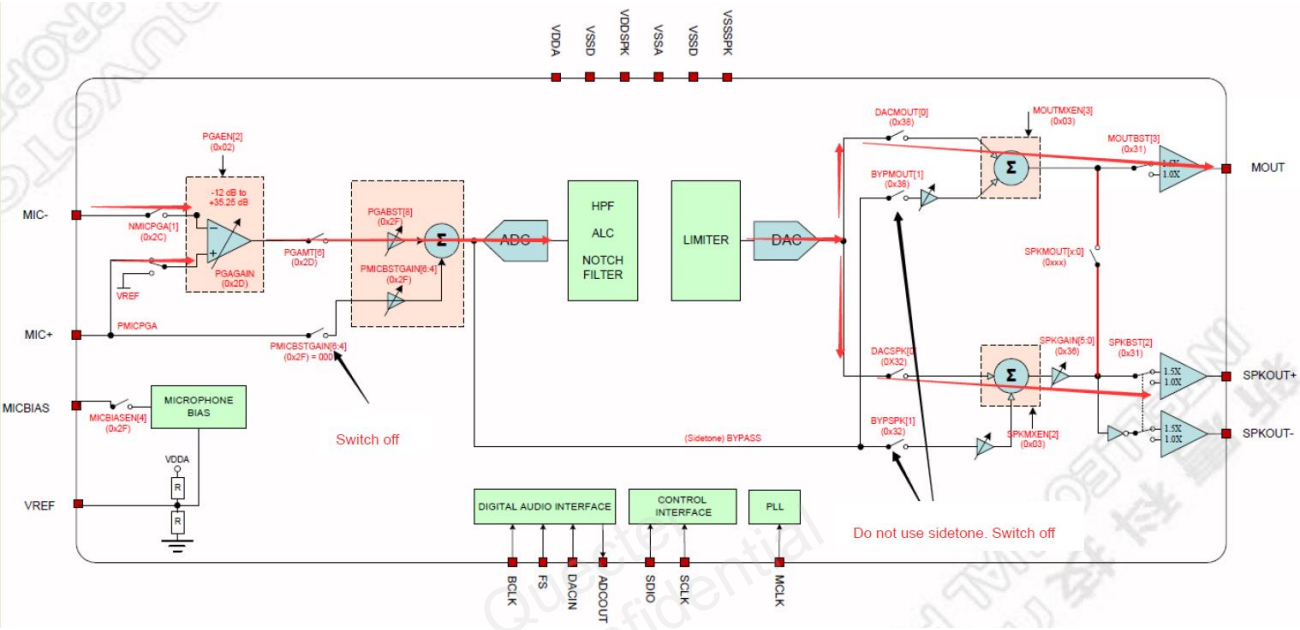

Figure 1: NAU8810 Overall Block Diagram

2.1. NAU8810 Uplink Block Diagram

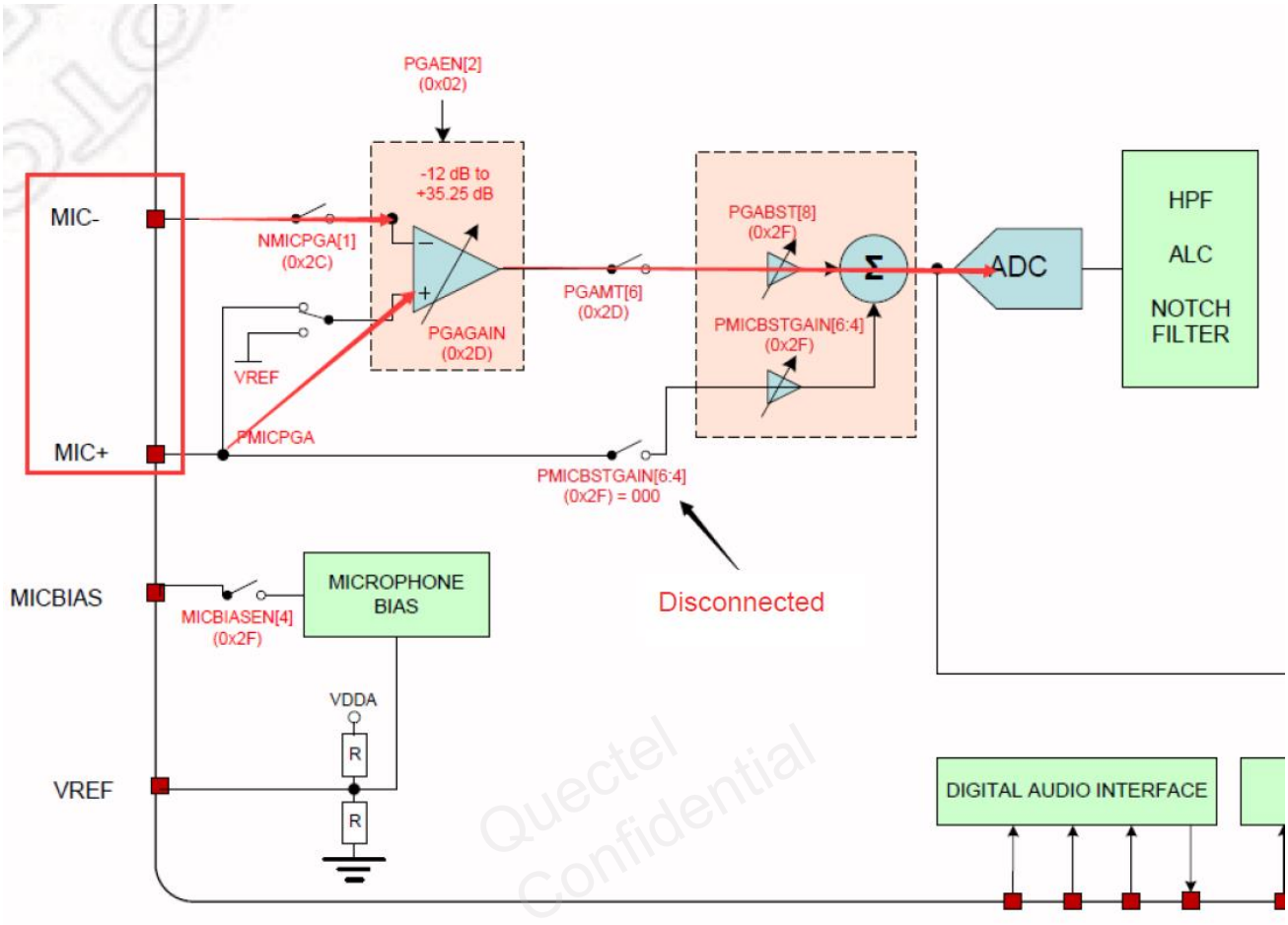

Figure 2: NAU8810 Uplink Block Diagram

NAU8810 defaults that uplink MIC goes through differential signals and merges at PGA into one path and then goes into ADC via ADC Boost. During the process, registers of 0x2D/0x2F can adjust the analog gain.

If the signal inputs from single-ended MIC, where it moves from MIC+ to ADC via ADC Boost directly, the switch from MIC- to PGA should be disconnected and the switch from PGA to MIC+ should be connected to reference electric level voltage VREF. Users can select the path via registers 0x2C/0x2F and adjust the analog gain via register 0x2F.

2.2. NAU8810 Downlink Block Diagram

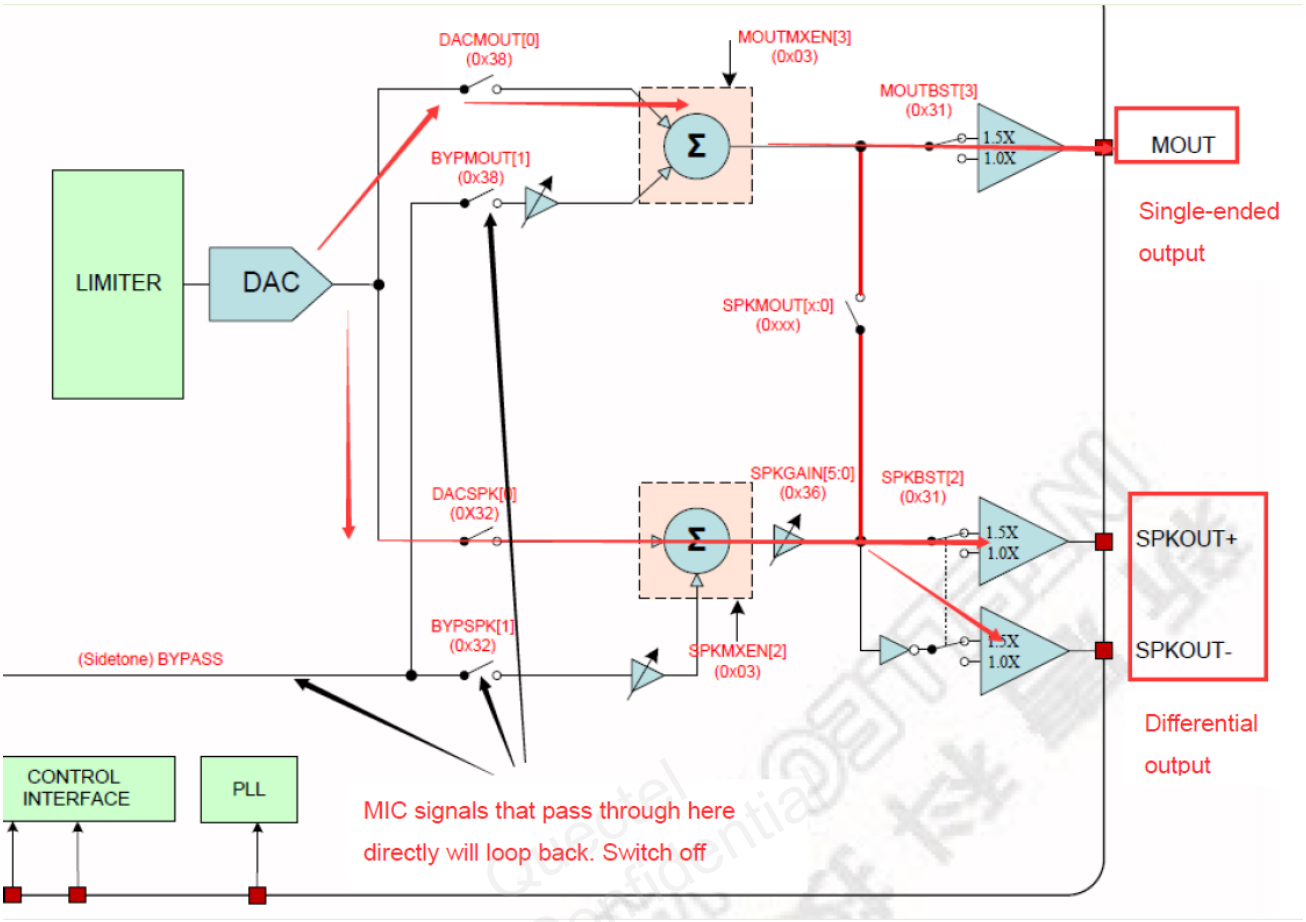

Figure 3: NAU8810 Downlink Block Diagram

There is only mono DAC in downlink block, which is divided into two paths to output–MOUT single-ended output and SPKOUT+/- differential output.

3 Introduction of Uplink and Downlink Register Configuration

3.1. AT Command Format for NAU8810 Codec Reading and Writing Registers

Read register values

```
AT+QIIC=1,0x1A,0x58,2
```

In the command, the meaning of the four parameters are as follows:

1	means to read
0x1A	stands for NAU8810 Codec
0x58	register address (Actual address is 0x2C, details show below.)
2	indicates the register length read is a 16-bit value.

Write register values

```
AT+QIIC=0,0x1A,0x58,1,0x03
```

In the command, the meaning of the five parameters are as follows:

0	means to write
0x1A	stands for NAU8810 Codec
0x58	register address
1	means that the register length written is 8 bits.
0x03	indicates the value written to the register

The register's physical length of NAU8810 is 8 bits while the register values are 9 bits, so in actual use, the highest bit (D8) of the values is placed in the lowest bit (D0) of the address register and at the same time, all the addresses in the address register shift one bit to the left. When writing a register command, users only need to write one byte, and read two bytes when reading. For example, if the user writes 0x03, then he should read 0x003.

See the diagram as below:

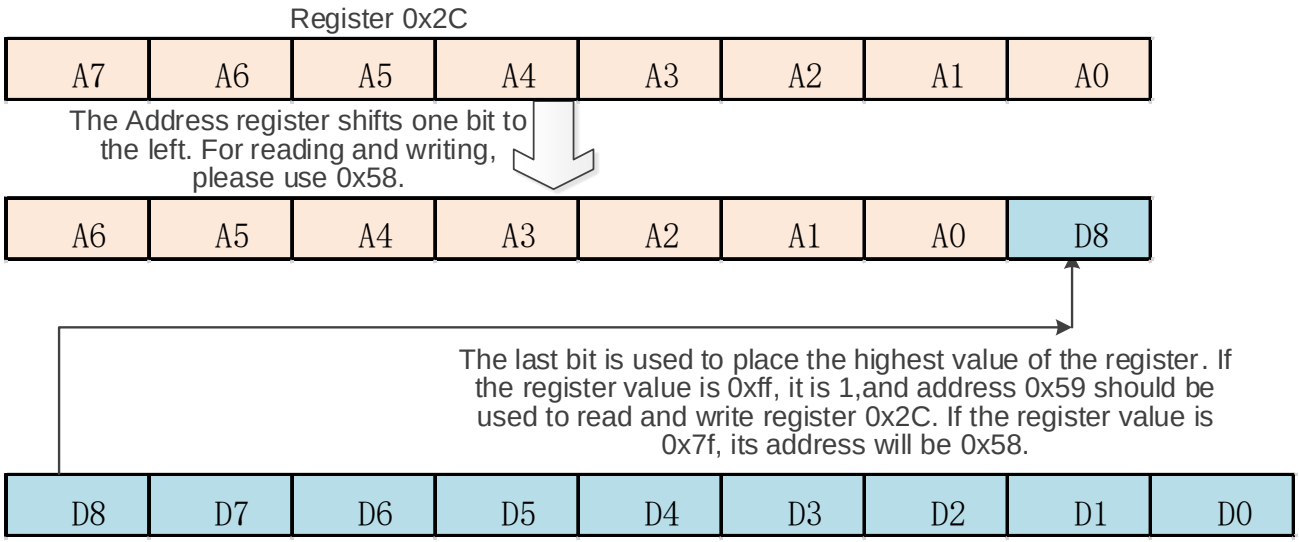

Figure 4: Command Rules of Reading and Writing NAU8810 Registers

3.2. MIC Gain Debugging

3.2.1. Input Signal Control Register 0x2C

Table 1: Input Signal Control Register (Addr 0x2C)

BIT	DESCRIPTION (Default 0x003)
D7-D8	Control the output voltage of MICBIASV (Affected by register 0x3A D4 at the same time) **MICBIASM[4] = 0 Address (0x3A)** 00:VDDA*0.9 01:VDDA*0.65 10:VDDA*0.75 11:VDDA*0.5 **MICBIASM[4] = 1 Address (0x3A)** 00:VDDA*0.85 01:VDDA*0.6 10:VDDA*0.7 11:VDDA*0.5
D2-D6	Reserved 00000
D1	NMICPGA control switch, controls the on/off from MIC- to PGA 0: MICN not connected to input PGA. 1: MICN to input PGA Negative terminal.
D0	PMICPGA control switch controls to select the paths from MIC+ to PGA 0: Input PGA Positive terminal to VREF

1: Input PGA Positive terminal to MICP through variable resistor

Register name: Input Signal Control Register
Register function: Control MIC path selection of and MIC Bias output voltage
Register address: 0x2C
Recommended value: 0x003
Command to read register: **AT+QIIC=1,0x1A,0x58,2**
Command to write register: **AT+QIIC=0,0x1A,0x58,1,0x03**
Register description: The register can control to select the paths from MIC to PGA. It is configured from differential MIC-/+ signals to PGA by default. If single-ended MIC (only MIC+) is applied, users need to reconfigure registers 0x2C and 0x2F.

3.2.2. PGA Gain Control Register

Table 2: PGA Gain Control Register (Addr 0x2D)

BIT	DESCRIPTION (Default 0x010)
D8	Reserved 0
D7	PGA Zero Cross Enable 0: Update gain when gain register changes 1: Update gain on 1st zero cross after gain register write
D6	Mute Control for PGA 0: PGA not mute. 1: PGA Mute.
D0-D5	Programmable Gain Amplifier Gain (PGA Gain Range -12dB to +35.25dB @0.75 increment) 000000: -12dB 000001: -11.25dB 000010:-10.50dB … 010000:0dB … 111110:34.5dB 111111:35.25dB

Register name: PGA Gain Control Register
Register function: Control gain of uplink differential signals passing through PGA
Register address: 0x2D
Recommended value: 0x014 (3dB)→The actual uplink volume of NAU8810 is a bit small. Users can turn it up to 15dB.
Command to read register: **AT+QIIC=1,0x1A,0x5A,2**
Command to write register: **AT+QIIC=0,0x1A,0x5A,1,0x14**
Gain description: The gain range of the register is -12~35.25dB and the gain can be adjusted according to

actual needs. When ALC function is turned on (D8 of 0x20 register is set to 1), the gain size of input PGA will be controlled automatically by ALC, and the PGA gain set by 0x2D does not take effect.

3.2.3. ADC Boost Control Register

Table 3: ADC Boost Control Register (Addr 0x2F)

BIT	DESCRIPTION (Default 0x100)
D8	PGABST Gain 0: PGA output has +0dB gain through input Boost stage 1: PGA output has +20dB gain through input Boost stage
D7	Reserved 0
D4-D6	PMICBSTGAIN, control the switch on/off and gain size from MIC+ to ADC (PMICBSTGAIN Gain Range -12dB to 6dB @3dB increment) 000: Path Disconnect 001: -12dB 010:-9dB … 101:0dB 110:3dB 111:6dB
D0-D3	Reserved 0000

Register name: ADC Boost Control Register
Register function: Control the switch from uplink MIC+ signal to ADC Boost and the gain of the differential signals passing through ADC Boost
Register address: 0x2F
Recommended value: 0x000 (0dB)
Command to read register: **AT+QIIC=1,0x1A,0x5E (0x5F),2**
Command to write register: **AT+QIIC=0,0x1A,0x5E(0x5F),1,0x00**
Register description: When using the differential MIC signals, one of the gain of 0dB/20dB can be controlled by D8 of 0x2F register after the signal passing PGA. However, the gain stepping is too much, please use it cautiously. When D8 is set to 1, the register address changes from 0x5E to 0x5F in **AT+QIIC** command because D8 is placed in the lowest bit of the address. When using single-ended MIC, users can control the on/off and the gain by D4-D6 of 0x2F if they need the signal pass directly from MIC+ to ADC Boost. When differential MIC signals are applied, D4-D6 should be disconnected. When single-end MIC+ is used, 20Db gain of D8 does not take effect.

3.2.4. Digital ADC Gain Control Register

Table 4: ADC Gain Control Register (Addr 0x0F)

BIT	DESCRIPTION (Default 0x0FF)
D8	Reserved 0
D0-D7	ADC Gain, control the gain size of uplink digital (ADC Gain Range -127dB to 0dB in 0.5dB increments) 00000000: Unused 00000001: -127dB 00000010:-126.5dB … 11111110:-0.5dB 11111111:0dB

Register name: Digital ADC Gain Control Register
Register function: Control uplink ADC digital gain
Register address: 0x0F
Recommended value: 0x0FF (0dB)
Command to read register: **AT+QIIC=1,0x1A,0x1E,2**
Command to write register: **AT+QIIC=0,0x1A,0x1E,1,0xff**
Register description: Default to configure based on 0dB.

3.3. Debugging Downlink Gain

3.3.1. Digital DAC Gain Control Register

Table 5: DAC Gain Control Register (Addr 0x0B)

BIT	DESCRIPTION (Default 0x0FF)
D8	Reserved 0
D0-D7	DAC Gain, control downlink digital gain size (DAC Gain Range -127dB to 0dB in 0.5dB increments 00000000: Digital Mute 00000001: -127dB 00000010: -126.5dB … 11111110: -0.5dB 11111111: 0dB

Register name: Digital DAC Gain Control Register
Register function: Control downlink DAC digital gain
Register address: 0x0B
Recommended value: 0x0FF(0dB)

Command to read register: **AT+QIIC=1,0x1A,0x16,2**
Command to write register: **AT+QIIC=0,0x1A,0x16,1,0xff**
Register description: Select the gain size according to actual needs. When the configuration is 0x000, please make the downlink mute.

3.3.2. Digital DAC Limiter Register

Table 6: DAC Limiter Register (Addr 0x19)

BIT	DESCRIPTION (Default 0x000)
D7-D8	Reserved 0
D4-D6	DAC Limiter Programmable signal threshold level, determines level at which the limiter starts to operate. (The limiter will take effect when the highest bit of 0x18 register DACLIMEN=0, or else the limiter volume boost will take effect.) 000: -1dB 001: -2dB 010: -3dB 011: -4dB 100: -5dB 101 to 111: -6dB
D0-D3	DAC Limiter volume Boost, can be used as a stand-alone volume Boost when DACLIMEN=0. (Limiter volume Boost Range is 0dB to 12dB in 1dB increments) 0000: 0dB 0001: 1dB 0010: 2dB … 1011: 11dB 1100: 12dB 1101 to 1111: Reserved

Register name: Digital DAC Limiter Register
Register function: Control downlink DAC limiter functions
Register address: 0x19
Recommended value: 0x000
Command to read register: **AT+QIIC=1,0x1A,0x32,2**
Command to write register: AT+QIIC=0,0x1A,0x32,1,0x00
Register description: To increase the downlink volume without using the limiter, users can add up to the gain of 12dB to downlink DAC via limiter volume boost. Before this, please confirm that the highest bit of 0x18 register is 0. Checking method: Execute **AT+QIIC=1,0x1A,0x31,2**, then read 0x18 register bit. Default value: 0x0032, D8 is 0.

3.3.3. Speaker Gain Control Register

Table 7: Speaker Gain Control Register (Addr 0x36)

BIT	DESCRIPTION (Default 0x039)
D8	Reserved 0
D7	SPKZC (Speaker Gain Control Zero Cross) 0: Change Gain on Zero Cross ONLY 1: Change Gain Immediately
D6	Mute Control for SPK 0: Speaker Enable 1: Speaker Mute.
D0-D5	Speaker Gain (SPK Gain Range -57dB to +6dB @1dB increment) 000000: -57dB 000001: -56dB 000010:-55dB … 111001:0dB … 111110:5dB 111111:6dB

Register name: Speaker Gain Control Register
Register function: Control the analog gain of downlink differential signal analog gain
Register address: 0x36
Recommended value: 0x039 (0dB)
Command to read register: **AT+QIIC=1,0x1A,0x6C,2**
Command to write register: **AT+QIIC=0,0x1A,0x6C,1,0x39**
Gain description: The register gain range is -57~6dB and it can be adjusted according to actual needs. When D6 is configured to 1, the downlink differential output is muted.

3.3.4. Output Register

Table 8: Output Register (Addr 0x31)

BIT	DESCRIPTION (Default 0x002)
D4-D8	Reserved 00000
D3	MOUTBST (MONO Output Boost Stage) 0: (1.0 x VREF) Gain Boost 1: (1.5 x VREF) Gain Boost
D2	SPKBST (Speaker Output Boost Stage) 0: (1.0 x VREF) Gain Boost

	1: (1.5 x VREF) Gain Boost
D1	TSEN (Thermal Shutdown) 0:Disabled 1:Enabled
D0	AOUTIMP (Analog Output Resistance) 0: ~1KΩ 1: ~30KΩ

Register name: Output Register
Register function: Control the output gain of downlink differential/single-ended signals
Register address: 0x31
Recommended value: 0x002
Command to read register: **AT+QIIC=1,0x1A,0x62,2**
Command to write register: AT+QIIC=0,0x1A,0x62,1,0x02
Gain description: The register can select the boost gain of downlink output. To make NAU8810 output maximum power, VDDSPK needs to be powered as shown below. In this mode, the output can directly push the speaker of 8Ω, 1W to phonate.

VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)						
Full scale output [7]		SPKBST = 0 VDDSPK = VDDA		VDDA / 3.3		V_{RMS}
		SPKBST = 1 VDDSPK = 1.5*VDDA		(VDDA / 3.3) * 1.5		

Figure 5: Recommended Values of NAU8810 SPKBOOST Power Supply

4 Appendix

This document mainly introduces registers controlled by NAU8810 gain. If the blocks need to be checked, please confirm the registers of power management are well configured and the path used for power supply is enabled. The software that supports NAU 8810 modules has enabled these registers by default.

All the registers are shown as follows. The functions of the registers are classified and can be found here.

Register Address		Register Names	Register Bits									Default
DEC	HEX		D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	Software Reset	RESET (SOFTWARE)									000
			POWER MANAGEMENT									
1	01	Power Management 1	DCBUFEN	0	0	PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		000
2	02	Power Management 2	0	0	0	0	BSTEN	0	PGAEN	0	ADCEN	000
3	03	Power Management 3	0	MOUTEN	NSPKEN	PSPKEN	0	MOUTMXEN	SPKMXEN	0	DACEN	000
			AUDIO CONTROL									
4	04	Audio Interface	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	050
5	05	Companding	0	0	0	0	DACCM[1:0]		ADCCM[1:0]		ADDAP	000
6	06	Clock Control 1	CLKM	MCLKSEL[2:0]			BCLKSEL[2:0]			0	CLKIOEN	140
7	07	Clock Control 2	0	0	0	0	0	SMPLR[2:0]			SCLKEN	000
10	0A	DAC CTRL	0	0	DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	000
11	0B	DAC Volume	0	DACGAIN								0FF
14	0E	ADC CTRL	HPFEN	HPFAM	HPF[2:0]			ADCOS	0	0	ADCPL	100
15	0F	ADC Volume	0	ADCGAIN								0FF

			EQUALISER					
18	0x12	EQ1-Low Cutoff	EQM	0	EQ1CF[1:0]	EQ1GC[4:0]		12C
19	0x13	EQ2-Peak 1	EQ2BW	0	EQ2CF[1:0]	EQ2GC[4:0]		02C
20	0x14	EQ3-Peak 2	EQ3BW	0	EQ3CF[1:0]	EQ3GC[4:0]		02C
21	0x15	EQ4-Peak3	EQ4BW	0	EQ4CF[1:0]	EQ4GC[4:0]		02C
22	0x16	EQ5-High Cutoff	0	0	EQ5CF[1:0]	EQ5GC[4:0]		02C
			DIGITAL TO ANALOG (DAC) LIMITER					
24	18	DAC Limiter 1	DACLIMEN	DACLIMDCY[3:0]		DACLIMATK[3:0]		032
25	19	DAC Limiter 2	0	0	DACLIMTHL[2:0]	DACLIMBST[3:0]		000
			NOTCH FILTER					
27	1B	Notch Filter High	NFCU	NFCEN	NFCA0[13:7]			000
28	1C	Notch Filter Low	NFCU	0	NFCA0[6:0]			000
29	1D	Notch Filter High	NFCU	0	NFCA1[13:7]			000
30	1E	Notch Filter Low	NFCU	0	NFCA1[6:0]			000
			ALC CONTROL					
32	20	ALC CTRL 1	ALCEN	0	0	ALCMXGAIN[2:0]	ALCMNGAIN[2:0]	038
33	21	ALC CTRL 2	ALCZC	ALCHT[3:0]		ALCSL[3:0]		00B
34	22	ALC CTRL 3	ALCM	ALCDCY[3:0]		ALCATK[3:0]		032
35	23	Noise Gate	0	0	0	0	0 ALCNEN	ALCNTH[2:0] 000

			PLL CONTROL					
36	24	PLL N CTRL	0	0	0	0	PLLMCLK	PLLN[3:0] 008
37	25	PLL K 1	0	0	0	PLLK[23:18]		00C
38	26	PLL K 2	PLLK[17:9]					093

Register Address		Register Names	Register Bits									Default
DEC	HEX		D8	D7	D6	D5	D4	D3	D2	D1	D0	
39	27	PLL K 3	PLLK[8:0]									0E9
			INPUT, OUTPUT & MIXER CONTROL									
40	28	Attenuation CTRL	0	0	0	0	0	0	MOUTATT	SPKATT	0	000
44	2C	Input CTRL	MICBIASV		0	0	0	0	0	NMICPGA	PMICPGA	003
45	2D	PGA Gain	0	PGAZC	PGAMT	PGAGAIN[5:0]						010
47	2F	ADC Boost	PGABST	0	PMICBSTGAIN			0	0	0	0	100
49	31	Output CTRL	0	0	0	0	0	MOUTBST	SPKBST	TSEN	AOUTIMP	002
50	32	Mixer CTRL	0	0	0	0	0	0	0	BYPSPK	DACSPK	001
54	36	SPKOUT Volume	0	SPKZC	SPKMT	SPKGAIN[5:0]						039
56	38	MONO Mixer Control	0	0	MOUTMT	0	0	0	0	BYPMOUT	DACMOUT	001
			LOW POWER CONTROL									
58	3A	Power Management 4	LPIPBST	LPADC	LPSPKD	LPDAC	MICBIASM	TRIMREG		IBADJ		000
			PCM TIME SLOT & ADCOUT IMPEDANCE OPTION CONTROL									
59	3B	Time Slot	TSLOT[8:0]									000
60	3C	ADCOUT Drive	PCMTSEN	TRI	PCM8BIT	PUDOEN	PUDPE	PUDPS	LOUTR	PCMB	TSLOT[9:8]	020

			REGISTER ID									
62	3E	Silicon Revision	0	1	1	1	0	1	1	1	1	0EF
63	3F	2-Wire ID	0	0	0	0	1	1	0	1	0	01A
64	40	Additional ID	0	1	1	0	0	1	0	1	0	0CA
65	41	Reserved	1	0	0	1	0	0	1	0	0	124
69	45	High Voltage CTRL	0	0	0	0	MOUTMT	0	HVOPU	0	HVOP	001
70	46	ALC Enhancements 1	ALCTBLSEL	ALCPKSEL	ALCNGSEL	ALCGAINL (ONLY)						000
71	47	ALC Enhancements 2	PKLIMEN	0	0	1	1	1	0	0	1	039
73	49	Additional IF CTRL	0	FSERRVAL[1:0]		FSERFLSH	FSERRENA	NFDLY	DACINMT	PLLLOCKP	DACOS256	000
75	4B	Power/Tie-off CTRL	0	LPSPKA	0	0	0	0	MANVREFH	MANVREFM	MANVREFL	000
76	4C	AGC P2P Detector	P2PDET (ONLY)									000
77	4D	AGC Peak Detector	PDET (ONLY)									000
78	4E	Control and Status	0	0	AMTCTRL	HVDET	NSGATE	AMUTE	DMUTE	0	FTDEC	000
79	4F	Output tie-off CTRL	MANOUTEN	SBUFH	SBUFL	SNSPK	SPSPK	SMOUT	0	0	0	000