EC2x&EG06&AG35-Quecopen

NAU8810 Codec Debugging Guidelines

LTE Standard/LTE-A Standard/Automotive Module Series

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Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
7th Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

History

Revision	Date	Author	Description
1.0	2018-02-22	Thirty XU	Initial
1.1	2018-05-25	Thirty XU	Added Chapter 4 to briefly introduce Codec gain debugging

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1 Introduction

This document mainly introduces the debugging methods of gain registers in ADC/DAC paths of NAU8810, which applies for users to debug the volume of NAU8810 Codec.

Currently Quectel modules that support NAU8810 Codec are:

- EC2x (EC25, EC21, EC20 R2.1, EC20 R2.0)
- EG06
- AG35

Before debugging, users should confirm the input and output paths used by the device, such as the interfaces used by MIC_IN and SPK_OUT; and then get a clear idea of uplink and downlink paths of the registers by checking internal Codec block diagram.

Execute command **AT+QIIC** to read the values of Codec register to make sure that the switches in the block are all connected and the others are disconnected. Make sure the power management registers applied by the modules in the block are all powered on. After that, check the original gain size in the block and adjust the gain size of corresponding registers according to actual needs.

2 Audio Paths Introduction

NAU8810 hardware block diagram that the software defaults to apply is illustrated as below: MIC differential input, single-ended and differential output.

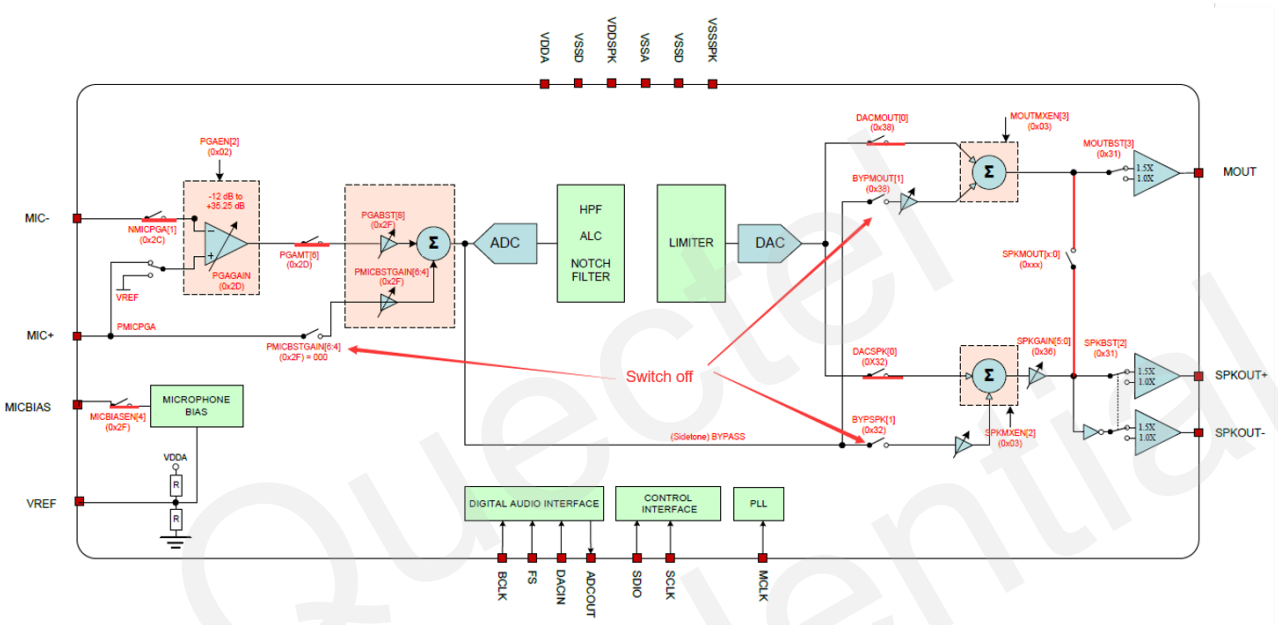

Figure 1: NAU8810 General Block Diagram

Users can reconfigure the input and output according to different product design demands. For example, selecting single-ended MIC input or using only one of single-ended/differential outputs can turn off the power supply from the other output to save power.

2.1. NAU8810 Uplink Block Diagram

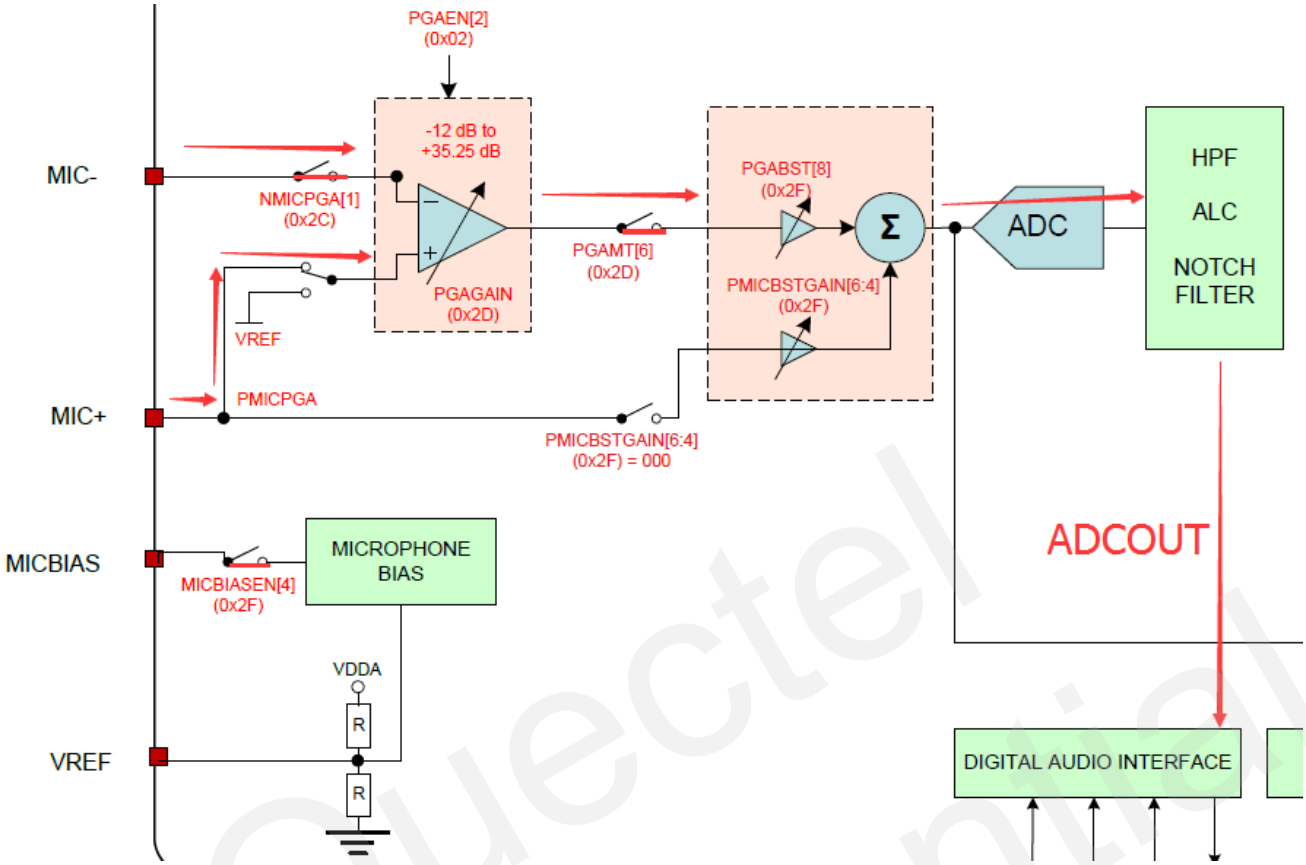

Figure 2: NAU8810 Uplink Block Diagram

NAU8810 defaults that uplink MIC goes through differential signals and merges at PGA into one path and then goes into ADC via ADC Boost. It will convert into digital signals and transmit to Quectel modules via the PCM interface. During the process, registers of 0x2D/0x2F can adjust the analog gain.

If the signal inputs from single-ended MIC, where it moves from MIC+ to ADC via ADC Boost directly, the switch from MIC- to PGA should be disconnected and the switch from PGA to MIC+ should be connected to reference electric level voltage VREF. Users can select the path via registers 0x2C/0x2F and adjust the analog gain via register 0x2F.

2.2. NAU8810 Downlink Block Diagram

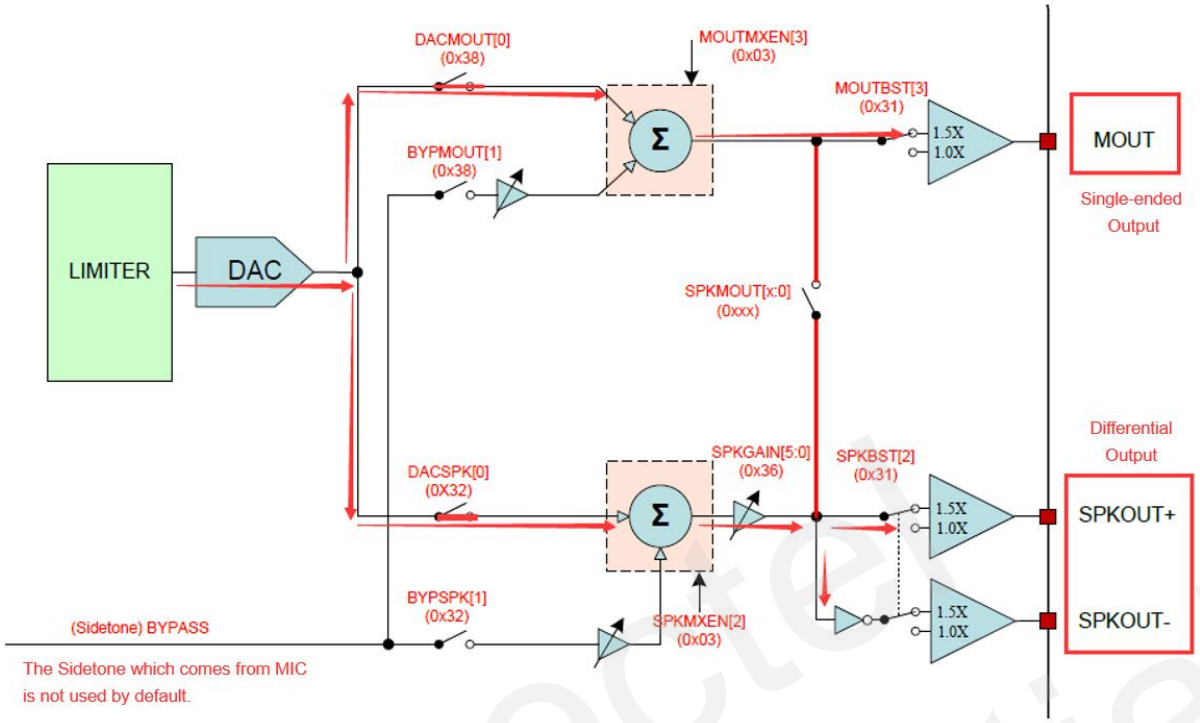

Figure 3: NAU8810 Downlink Block Diagram

There is only mono DAC in downlink block. Quectel modules output digital audio signals to NAU8810 via the PCM interfaces and divide into two paths of analog output after passing through DAC–MOUT single-ended output and SPKOUT+/- differential output.

3 Introduction of Uplink and Downlink Register Configuration

3.1. AT Command Format for NAU8810 Codec Reading and Writing Registers

Read register values:

```
AT+QIIC=1,0x1A,0x58,2
```

In the command, the meaning of the four parameters are as follows:

1	means to read
0x1A	stands for NAU8810 Codec
0x58	register address (Actual address is 0x2C, details show below.)
2	indicates the register length read is a 16-bit value.

Write register values:

```
AT+QIIC=0,0x1A,0x58,1,0x03
```

In the command, the meaning of the five parameters are as follows:

0	means to write
0x1A	stands for NAU8810 Codec
0x58	register address
1	means that the register length written is 8 bits.
0x03	indicates the value written to the register

The register's physical length of NAU8810 is 8 bits while the register values are 9 bits, so in actual use, the highest bit (D8) of the values is placed in the lowest bit (D0) of the address register and at the same time, all the addresses in the address register shift one bit to the left. When writing a register command, users only need to write one byte, and read two bytes when reading. For example, if the user writes 0x03, then he should read 0x003.

See the diagram as below:

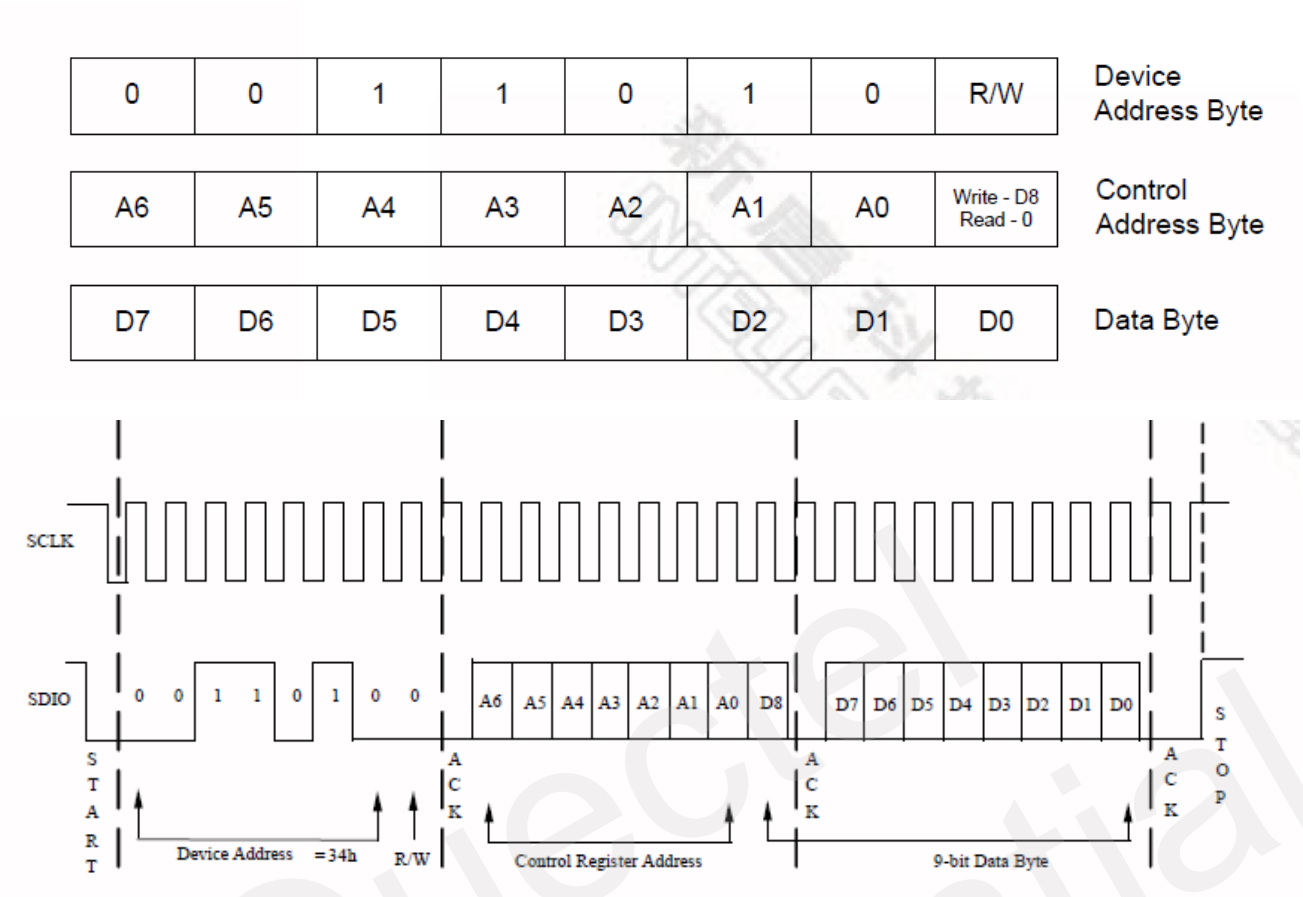

Figure 4: Command Rules of Reading and Writing NAU8810 Registers

3.2. MIC Gain Debugging

3.2.1. Input Signal Control Register (0x2C)

Table 1: Introduction of Input Signal Control Register

REGISTER	DESCRIPTION
Register name	Input Signal Control Register
Register function	Control MIC path selection and MIC Bias output voltage
Register address	0x2C
Recommended value	0x003
Command to read register	**AT+QIIC=1,0x1A,0x58,2**

Command to write register	**AT+QIIC=0,0x1A,0x58,1,0x03**
Register description	The register can control to select the paths from MIC to PGA. It is configured from differential MIC-/+ signals to PGA by default. If single-ended MIC (only MIC+) is applied, users need to reconfigure registers 0x2C and 0x2F.

Table 2: Configuration of Input Signal Control Register

BIT	DESCRIPTION (Default 0x003)
D7-D8	Control the output voltage of MICBIASV (Affected by register 0x3A D4 at the same time) MICBIASM[4] = 0 Address (0x3A) 00:VDDA*0.9 01:VDDA*0.65 10:VDDA*0.75 11:VDDA*0.5 MICBIASM[4] = 1 Address (0x3A) 00:VDDA*0.85 01:VDDA*0.6 10:VDDA*0.7 11:VDDA*0.5
D2-D6	Reserved 00000
D1	NMICPGA control switch, controls the on/off from MIC- to PGA 0: MICN not connected to input PGA. 1: MICN to input PGA Negative terminal.
D0	PMICPGA control switch controls to select the paths from MIC+ to PGA 0: Input PGA Positive terminal to VREF 1: Input PGA Positive terminal to MICP through variable resistor

3.2.2. PGA Gain Control Register (0x2D)

Table 3: Introduction of PGA Gain Control Register

REGISTER	DESCRIPTION
Register name	PGA Gain Control Register
Register function	Control the gain of uplink differential signals passing through PGA
Register address	0x2D
Recommended value	0x014 (3dB) The actual uplink volume of NAU8810 is a bit small. Users can turn it up to about

	15dB.
Command to read register	**AT+QIIC=1,0x1A,0x5A,2**
Command to write register	**AT+QIIC=0,0x1A,0x5A,1,0x14**
Register description	The gain range of the register is -12~35.25dB and the gain can be adjusted according to actual needs. When ALC function is turned on (Set D8 of 0x20 register to 1), the gain size of input PGA will be controlled automatically by ALC, and the PGA gain set by 0x2D does not take effect.

Table 4: Configuration of PGA Gain Control Register

BIT	DESCRIPTION (Default 0x010)
D8	Reserved 0
D7	PGA Zero Cross Enable 0: Update gain when gain register changes 1: Update gain on 1st zero cross after gain register write
D6	Mute Control for PGA 0: PGA not mute. 1: PGA Mute.
D0-D5	Programmable Gain Amplifier Gain (PGA Gain Range -12dB to +35.25dB in 0.75 increments) 000000: -12dB 000001: -11.25dB 000010:-10.50dB … 010000:0dB … 111110:34.5dB 111111:35.25dB

3.2.3. ADC Boost Control Register (0x2F)

Table 5: Introduction of ADC Boost Control Register

REGISTER	DESCRIPTION
Register name	ADC Boost Control Register
Register function	Control the switch from uplink MIC+ signal to ADC Boost and the gain of the differential signals passing through ADC Boost

Register address	0x2F
Recommended value	0x000 (0dB)
Command to read register	**AT+QIIC=1,0x1A,0x5E(0x5F),2**
Command to write register	**AT+QIIC=0,0x1A,0x5E(0x5F),1,0x00**
Register description	When differential MIC signals are applied, one of the gain of 0dB/20dB can be controlled by D8 of 0x2F register after the signal passing PGA. However, the gain stepping is too much, please use it cautiously. When D8 is set to 1, the register address changes from 0x5E to 0x5F in **AT+QIIC** command because D8 is placed in the lowest bit of the address. When using single-ended MIC, users can control the on/off and the gain by D4-D6 of 0x2F if they need the signals pass directly from MIC+ to ADC Boost. When differential MIC signals are applied, D4-D6 should be disconnected. When single-end MIC+ is applied, 20Db gain of D8 does not take effect.

Table 6: Configuration of ADC Boost Control Register

BIT	DESCRIPTION (Default 0x100)
D8	PGABST Gain 0: PGA output has +0dB gain through input Boost stage 1: PGA output has +20dB gain through input Boost stage
D7	Reserved 0
D4-D6	PMICBSTGAIN, control the switch on/off and gain size from MIC+ to ADC (PMICBSTGAIN Gain Range -12dB to 6dB in 3dB increments) 000: Path Disconnect 001: -12dB 010:-9dB … 101:0dB 110:3dB 111:6dB
D0-D3	Reserved 0000

3.2.4. ADC Gain Control Register (0x0F)

Table 7: Introduction of ADC Gain Control Register

REGISTER	DESCRIPTION
Register name	ADC Gain Control Register
Register function	Control uplink ADC digital gain
Register address	0x0F
Recommended value	0x0FF（0dB）
Command to read register	**AT+QIIC=1,0x1A,0x1E,2**
Command to write register	**AT+QIIC=0,0x1A,0x1E,1,0xff**
Register description	Default to configure based on 0dB.

Table 8: Configuration of ADC Gain Control Register

Bit	DESCRIPTION (Default 0x0FF)
D8	Reserved 0
D0-D7	ADC Gain, control the gain size of uplink digital (ADC Gain Range -127dB to 0dB in 0.5dB increments) 00000000: Unused 00000001: -127dB 00000010: -126.5dB … 11111110: -0.5dB 11111111: 0dB

3.3. Debugging Downlink Gain

3.3.1. DAC Gain Control Register (0x0B)

Table 9: Introduction of DAC Gain Control Register

REGISTER	DESCRIPTION
Register name	DAC Gain Control Register

Register function	Control downlink DAC digital gain
Register address	0x0B
Recommended value	0x0FF (0dB)
Command to read register	**AT+QIIC=1,0x1A,0x16,2**
Command to write register	**AT+QIIC=0,0x1A,0x16,1,0xff**
Register description	Select the gain size according to actual needs. When the configuration is 0x000, please make the downlink mute.

Table 10: Configuration of DAC Gain Control Register

BIT	DESCRIPTION (Default 0x0FF)
D8	Reserved 0
D0-D7	DAC Gain, control downlink digital gain size (DAC Gain Range -127dB to 0dB in 0.5dB increments) 00000000: Digital Mute 00000001: -127dB 00000010: -126.5dB … 11111110: -0.5dB 11111111: 0dB

3.3.2. DAC Limiter Register (0x19)

Table 11: Introduction of DAC Limiter Register

REGISTER	DESCRIPTION
Register name	DAC Limiter Register
Register function	Control downlink DAC limiter functions
Register address	0x19
Recommended value	0x000
Command to read register	**AT+QIIC=1,0x1A,0x32,2**

Command to write register	**AT+QIIC=0,0x1A,0x32,1,0x00**
Register description	To increase the downlink volume without using the limiter, users can add up to the gain of 12dB to downlink DAC via limiter volume boost. Before this, please first confirm that the highest bit of 0x18 register is 0. Checking method: Execute **AT+QIIC=1,0x1A,0x31,2**, then read 0x18 register bit. Default value: 0x0032, D8 is 0.

Table 12: Configuration of DAC Limiter Register

BIT	DESCRIPTION (Default 0x000)
D7-D8	Reserved 0
D4-D6	DAC Limiter Programmable signal threshold level, determines level at which the limiter starts to operate. (The limiter will take effect when the highest bit of 0x18 register DACLIMEN=0, or else the limiter volume boost will take effect.) 000: -1dB 001: -2dB 010: -3dB 011: -4dB 100: -5dB 101 to 111: -6dB
D0-D3	DAC Limiter volume Boost, can be used as a stand-alone volume Boost when DACLIMEN=0. (Limiter volume Boost Range is 0dB to 12dB in 1dB increments) 0000: 0dB 0001: 1dB 0010: 2dB … 1011: 11dB 1100: 12dB 1101 to 1111: Reserved

3.3.3. Speaker Gain Control Register

Table 13: Introduction of Speaker Gain Control Register

REGISTER	DESCRIPTION
Register name	Speaker Gain Control Register
Register function	Control the analog gain of the downlink differential signal

Register address	0x36
Recommended value	0x039（0dB）
Command to read register	**AT+QIIC=1,0x1A,0x6C,2**
Command to write register	**AT+QIIC=0,0x1A,0x6C,1,0x39**
Register description	The register gain range is -57~6dB and the gain size can be adjusted according to actual needs. When D6 is configured to 1, the downlink differential output is muted.

Table 14: Configuration of Speaker Gain Control Register

BIT	DESCRIPTION (Default 0x039)
D8	Reserved 0
D7	SPKZC (Speaker Gain Control Zero Cross) 0: Change Gain on Zero Cross ONLY 1: Change Gain Immediately
D6	Mute Control for SPK 0: Speaker Enable 1: Speaker Mute.
D0-D5	Speaker Gain (SPK Gain Range -57dB to +6dB in 1dB increments) 000000: -57dB 000001: -56dB 000010:-55dB … 111001:0dB … 111110:5dB 111111:6dB

3.3.4. Output Register (0x31)

Table 15: Introduction of Output Register

REGISTER	DESCRIPTION
Register name	Output Register
Register function	Control the output gain of downlink differential/single-ended signals

Register address	0x31
Recommended value	0x002
Command to read register	**AT+QIIC=1,0x1A,0x62,2**
Command to write register	**AT+QIIC=0,0x1A,0x62,1,0x02**
Register description	The register can select the boost gain of downlink output. To make NAU8810 output maximum power, VDDSPK needs to be powered as shown below. In this mode, the output can directly push the speaker of 8 Ω, 1W to phonate.

VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)						
Full scale output [7]		SPKBST = 0 VDDSPK = VDDA		VDDA / 3.3		V_{RMS}
		SPKBST = 1 VDDSPK = 1.5*VDDA		(VDDA / 3.3) * 1.5		

Figure 5: Recommended Values of NAU8810 SPKBOOST Power Supply

Table 16: Configuration of Output Register

BIT	DESCRIPTION (Default 0x002)
D4-D8	Reserved 00000
D3	MOUTBST (MONO Output Boost Stage) 0: (1.0 x VREF) Gain Boost 1: (1.5 x VREF) Gain Boost
D2	SPKBST (Speaker Output Boost Stage) 0: (1.0 x VREF) Gain Boost 1: (1.5 x VREF) Gain Boost
D1	TSEN (Thermal Shutdown) 0:Disabled 1:Enabled
D0	AOUTIMP (Analog Output Resistance) 0: ~1KΩ 1: ~30KΩ

4 Codec Gain Debugging Guide

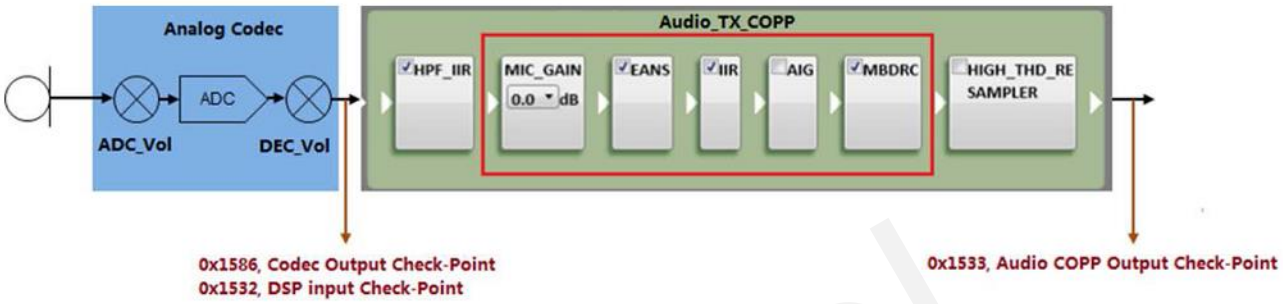

Figure 6: Codec and Module DSP Topological Diagram

Take the above diagram as an example. When debugging Codec gain, users should make sure that signals arriving at ADC and signals that PCM interfaces output are not too saturated to result in signal clipping. Excessive signal clipping will lead to sound distortion and may introduce noise.

Figure 7: Signal Clipping Caused by Excessive Gain

If using analog microphones, users can add the gain to ADC_Volume, but the gain of DEC_Vol should not be too high. If a digital microphone is used, both ADC_Volume and DEC_Vol use 0dB gain.

4.1. ADC_Volume

ADC_Volume controls the input signal volume VADC of analog to digital converter (ADC). Excessive input signals of ADC will lead to signal clipping. NAU8810 Codec ADC coverts at 0dBFS/V. If the amplitude of

VADC is greater than 1V (or 0dBV), the signal will be clipped.

The sensitivity of the Microphone (Smic) and the intensity of the acoustic signals near the microphone (Paoc) will also influence the amplitude of the microphone input signals. Ignoring the influence of the acoustic structure such as the microphone sound transmission holes on the signal amplitude, it can be approximated that:

VADC = Paoc * Smic *ADCvol

Change it to dB:

VADC(dBV) = Paoc(dBSPL)-94 + Smic(dBV/Pa) + ADCvol(dB)

The stronger the acoustic signals around the microphone, the easier it is to generate recording clipping problems, such as speaking loudly close to the microphone, or recording a live concert. To avoid clipping problems, please lower ADCvol.

Acoustic overload point (AOP) is considered as the maximum intensity of the acoustic signal that the microphone can effectively pick up. According to AOP of the microphone and the formula above and to avoid clipping (VADC<=0dBV) within the effective working range of the microphone, the maximum value that ADC_Volume can take is:

ADCvol(dB) = 0 - Paop(dBSPL) + 94 - Smic(dBV/Pa)

The sensitivity and AOP of the microphone are usually available from the microphone specification. Take certain analog microphone as an example, if its sensitivity is -38dBV/Pa, its AOP is 124dBSPL, so it can be calculated from the above formula that:

ADCvol(dB)= 0 -124 + 94 - (-38) = 8(dB)

If ADC_Volume is set too low (such as 0dB), signal clipping will not occur, but the amplitude of recording signal will be low. Digital gain can be used to increase signal amplitude, however, the resolution of the signal will be low and the recording quality will not be too good.

ADC_Volume can use the values that are calculated based on microphone AOP and sensitivity for recording debugging. When calculating ADCvol, users can take into account the effect of acoustic structures such as sensitivity bias, AOP bias and microphone sound transmission holes on the calculation results in order to get a safer and more reasonable result.

After setting ADC_Volume, users can take a recording test (Here set DEC_Volume to 0dB). Play a signal with a sound intensity of about to reach AOP near the microphone, then check the signal of Codec PCM_OUT to confirm if there is clipping.

No ADC is required in the Codec path if a digital microphone is used. Users can take a recording test (Here set DEC_Volume to 0dB) and play a signal with a sound intensity of about to reach AOP near the microphone, then check the signal of Codec PCM_OUT to confirm if there is clipping.

- If clipping occurs, users should try to debug the gain inside the microphone because it may be too high.
- If the signal is very low, for example, and the maximum signal amplitude is less than -15dB, it

indicates that the gain inside the microphone may be too low. Users can adjust the gain appropriately so that the signal output of AOP is between [-12dBFS, -3dBFS].

5 Appendix A--Registers List

This document mainly introduces registers controlled by NAU8810 gain. If the block needs to be checked, please confirm the registers of power management are well configured and the path used for power supply is enabled. The software that supports NAU8810 modules has enabled these registers by default.

All the registers are shown as follows. The functions of the registers are classified and can be found here.

Register Address		Register Name	Register Bits									Default
DEC	HEX		D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	Software Reset	RESET (SOFTWARE)									0x000
Power Management												
1	1	Power Management 1	DCBUFEN	0	0	PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		0x000
2	2	Power Management 2	0	0	0	0	BSTEN	0	PGAEN	0	ADCEN	0x000
3	3	Power Management 3	0	MOUTEN	NSPKEN	PSPKEN	0	MOUTMXEN	SPKMXEN	0	DACEN	0x000
Audio Ctrl												
4	4	Audio Interface	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	0x050
5	5	Companding	0	0	0	0	DACCM[1:0]		ADCCM[1:0]		ADDAP	0x000
6	6	Clock Control 1	CLKM	MCLKSEL[2:0]			BCLKSEL[2:0]			0	CLKIOEN	0x140
7	7	Clock Control 2	0	0	0	0	0	SMPLR[2:0]			SCLKEN	0x000
10	A	DAC CTRL	0	0	DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	0x000

11	B	DAC Volume	0	DACGAIN						0x0FF
14	E	ADC CTRL	HPFEN	HPFAM	HPF[2:0]		ADCOS	0	0	ADCPL	0x100
15	F	ADC Volume	0	ADCGAIN						0x0FF
EQUALISER										
18	12	EQ1-Low Cutoff	EQM	0	EQ1CF[1:0]		EQ1GC[4:0]			0x12C
19	13	EQ2-Peak 1	EQ2BW	0	EQ2CF[1:0]		EQ2GC[4:0]			0x02C
20	14	EQ3-Peak 2	EQ3BW	0	EQ3CF[1:0]		EQ3GC[4:0]			0x02C
21	15	EQ4-Peak 3	EQ4BW	0	EQ4CF[1:0]		EQ4GC[4:0]			0x02C
22	16	EQ5-High Cutoff	0	0	EQ5CF[1:0]		EQ5GC[4:0]			0x02C
DIGITAL TO ANALOG (DAC) LIMITER										
24	18	DAC Limiter 1	DACLIMEN	DACLIMDCY[3:0]			DACLIMATK[3:0]			0x032
25	19	DAC Limiter 2	0	0	DACLIMTHL[2:0]		DACLIMBST[3:0]			0x000
NOTCH FILTER										
27	1B	Notch Filter High	NFCU	NFCEN	NFCA0[13:7]					0x000
28	1C	Notch Filter Low	NFCU	0	NFCA0[6:0]					0x000
29	1D	Notch Filter High	NFCU	0	NFCA1[13:7]					0x000
30	1E	Notch Filter Low	NFCU	0	NFCA1[6:0]					0x000
ALC CONTROL										
32	20	ALC CTRL 1	ALCEN	0	0	ALCMXGAIN[2:0]		ALCMNGAIN[2:0]		0x038
33	21	ALC CTRL 2	ALCZC	ALCHT[3:0]			ALCSL[3:0]			0x00B
34	22	ALC CTRL 3	ALCM	ALCDCY[3:0]			ALCATK[3:0]			0x032

35	23	Noise Gate	0	0	0	0	0	ALCN EN	ALCNTH[2:0]			0x0 00
PLL CONTROL												
36	24	PLL N CTRL	0	0	0	0	PLLM CLK	PLLN[3:0]				0x0 08
37	25	PLL K 1	0	0	0	PLLK[23:18]						0x0 0C
38	26	PLL K 2	PLLK[17:9]									0x0 93
39	27	PLL K 3	PLLK[8:0]									0x0 E9
INPUT, OUTPUT & MIXER CONTROL												
40	28	Attenuation CTRL	0	0	0	0	0	0	MOU TATT	SPKA TT	0	0x0 00
44	2C	Input CTRL	MICBIASV		0	0	0	0	0	NMIC PGA	PMIC PGA	0x0 03
45	2D	PGA Gain	0	PGA ZC	PGA MT	PGAGAIN[5:0]						0x0 10
47	2F	ADC Boost	PGAB ST	0	PMICBSTGAIN			0	0	0	0	0x1 00
49	31	Output CTRL	0	0	0	0	0	MOU TBST	SPKB ST	TSEN	AOU TIMP	0x0 02
50	32	Mixer CTRL	0	0	0	0	0	0	0	BYPS PK	DAC SPK	0x0 01
54	36	SPKOUT Volume	0	SPK ZC	SPK MT	SPKGAIN[5:0]						0x0 39
56	38	MONO Mixer Control	0	0	MOU TMT	0	0	0	0	BYP MOU T	DAC MOU T	0x0 01
LOW POWER CONTROL												
58	3A	Power Management 4	LPIP BST	LPA DC	LPSP KD	LPD AC	MICB IASM	TRIMREG		IBADJ		0x0 00
PCM TIME SLOT & ADCOUT IMPEDANCE OPTION CONTROL												
59	3B	Time Slot	TSLOT[8:0]									0x0 00
60	3C	ADCOUT Drive	PCM TSEN	TRI	PCM 8BIT	PUD OEN	PUD PE	PUDP S	LOUT R	PCM B	TSLO T[9:8]	0x0 20

ID REGISTER												
62	3E	Silicon Revision	0	1	1	1	0	1	1	1	1	0x0EF
63	3F	2-Wire ID	0	0	0	0	1	1	0	1	0	0x01A
64	40	Additional ID	0	1	1	0	0	1	0	1	0	0x0CA
65	41	Reserved	1	0	0	1	0	0	1	0	0	0x124
69	45	High Voltage CTRL	0	0	0	0	MOUTMT	0	HVOPU	0	HVOP	0x001
70	46	ALC Enhancements 1	ALCTBLSEL	ALCPKSEL	ALCNGSEL	ALCGAINL (ONLY)						0x000
71	47	ALC Enhancements 2	PKLIMEN	0	0	1	1	1	0	0	1	0x039
73	49	Additional IF CTRL	0	FSERRVAL[1:0]		FSERFLSH	FSERRENA	NFDLY	DACINMT	PLLLOCKP	DACOS256	0x000
75	4B	Power/Tie-off CTRL	0	LPSPKA	0	0	0	0	MANVREFH	MANVREFM	MANVREFL	0x000
76	4C	AGC P2P Detector	P2PDET (ONLY)									0x000
77	4D	AGC Peak Detector	PDET (ONLY)									0x000
78	4E	Control and Status	0	0	AMTCTRL	HVDET	NSGATE	AMUTE	DMUTE	0	FTDEC	0x000
79	4F	Output tie-off CTRL	MANOUTEN	SBUFH	SBUFL	SNSPK	SPSPK	SMOUT	0	0	0	0x000