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EC2x Series QuecOpen Module Booting User Guide

LTE Standard Module Series

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About the Document

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1 Introduction

Quectel LTE Standard EC2x series modules support QuecOpen® solution. This document mainly introduces the booting types and how to query these types of EC2x series QuecOpen® modules.

The applicable modules of this document are as follows:

- EC21 series QuecOpen
- EC25 series QuecOpen
- EC20 R2.1 series QuecOpen

2 Introduction to PMIC and SMPL Function

This chapter mainly introduces the module PMIC pin information and SMPL function related to module booting.

2.1. PMIC Introduction

The PMIC structure of the EC2x series QuecOpen modules is shown in the figure below, and the PMIC pins related to the module booting are described as follows:

- CBL_PWR_N: works as the power switch and is internally pulled up by default.
- RESIN_N: works as reset switch and is internally pulled up by default.
- PON_TRIG: can power on the module and is active high. It is connected to the ground by default and is not used to power on the module.
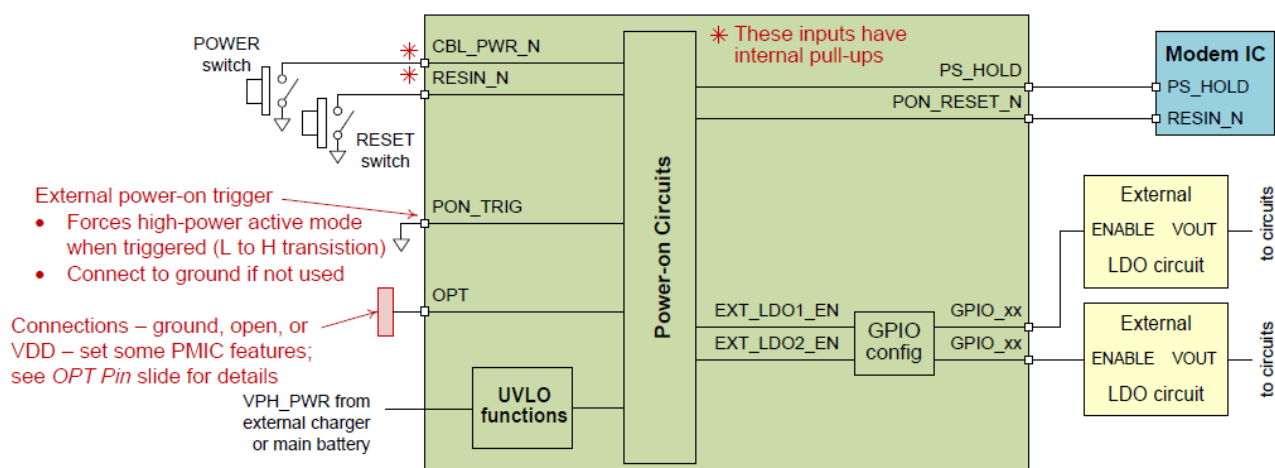- VPH_PWR: is from VBAT pin. It can supply power to PMIC through UVLO and SMPL circuit.

Figure 1: Module PMIC Structure Diagram

2.2. SMPL Function Introduction

When enabled by software, there is immediate and automatic recovery from a momentary PMIC power loss. If VDD drops out of range (for example, a UVLO event is detected) and it returns in range within 0.5 s, the SMPL (a power ON trigger), automatically turns on the PMIC.

Some operational details:

● UVLO event clears PON_RST_N; PMIC is powered down.
● If VDD returns to its valid range before timeout, a power-on sequence is initiated without software intervention, and an interrupt is sent to the modem IC indicating:

    1) Power was momentarily lost
    2) RTC is corrupted due to insufficient voltage
    3) Current PMIC actions are not a normal power sequence.

● If SMPL times out without VDD returning to its valid range, then the handset must undergo the normal power-on sequence whenever the next initializing event occurs.
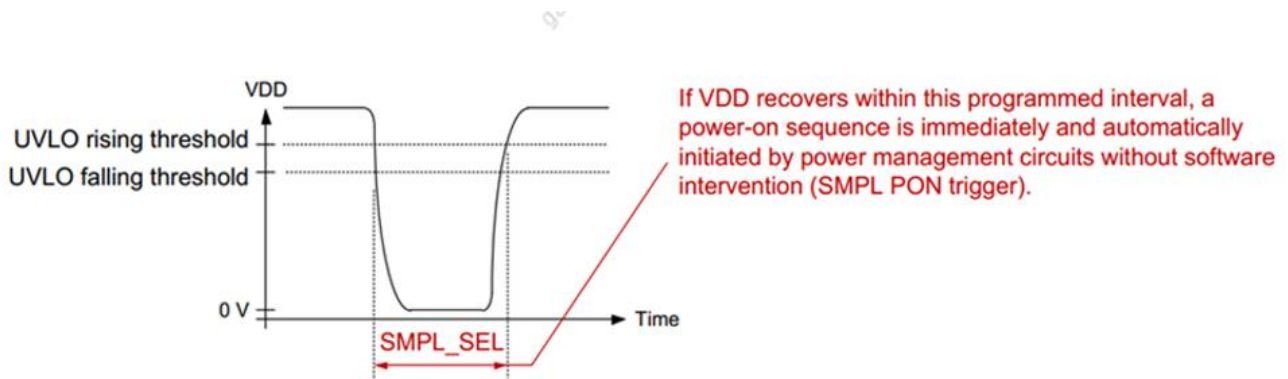

Figure 2: SMPL

3 Module Power-on

3.1. Types of Module Power-on

Currently, the booting types of EC2x QuecOpen module are as follows:

1. Powerkey: inputs internal pull-up by default; it is level triggered, active low.
2. Reset: inputs internal pull-up by default; it is level triggered, active high.
3. Reboot: Restart the software. It is much safer method to power on the module by rebooting the module.
4. RTC Alarm: After the register of the internal RTC alarm is enabled, the module will be powered on at a specified time.
5. SMPL: If VBAT voltage can drop to about 1.4 V through momentary PMIC power loss, and restore the voltage within 0.5 s (SMPL is enabled by default and SMPL default valid detection time is 0.5 s), SMPL will trigger the module to power on automatically.

3.2. Check Module Power-on Method

3.2.1. Check through Kernel Log

Execute command **dmesg |grep qpn** to view the Kernel log. The returned log prints the power-on reason.

1. If the module is powered on through pressing the powerkey, the log will print the following information:

```
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~# dmesg  |grep qpnp
[    0.292104] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.292830] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.305635] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from CBL (external power supply) and 'cold' boot
[    0.305664] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0: Unknown power-off reason
[    0.305906] input: qpnp_pon as /devices/virtual/input/input0
[    0.426906] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.179203] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:00:03 UTC (3)
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~#
```

2. If the module is reset, the log prints the following information:

```
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~# dmesg  |grep qpnp
[    0.292092] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.292818] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.305436] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from Hard Reset and 'cold' boot
[    0.305466] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-off reason: Triggered from RESIN_N (Reset line/Volume Down Key)
[    0.305708] input: qpnp_pon as /devices/virtual/input/input0
[    0.426843] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.179273] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:11:04 UTC (664)
root@mdm9607-perf:~#
root@mdm9607-perf:~#
```

3. If the module is rebooted, the log prints the following information:

```
root@mdm9607-perf:~#
root@mdm9607-perf:~#
root@mdm9607-perf:~# dmesg  |grep qpnp
[    0.292098] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.292823] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.305632] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from Hard Reset and 'cold' boot
[    0.305662] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-off reason: Triggered from PS_HOLD (PS_HOLD/MSM controlled shutdown)
[    0.305909] input: qpnp_pon as /devices/virtual/input/input0
[    0.426877] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.179221] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:12:55 UTC (775)
```

4. If the module automatically powers on after a sudden power-down, the log prints the following information:

```
root@mdm9607-perf:~#
root@mdm9607-perf:~# dmesg  |grep qpnp
[    0.292096] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.292816] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.305457] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from SMPL (sudden momentary power loss) and 'cold' boot
[    0.305487] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-off reason: Triggered from UVLO (Under Voltage Lock Out)
[    0.305730] input: qpnp_pon as /devices/virtual/input/input0
[    0.426843] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.178799] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:02:16 UTC (136)
root@mdm9607-perf:~#
```

NOTE

If the power-on reason cannot be viewed in the log, Please confirm if the power-on related logs are cleared because too many irrelevant logs are printed.

3.2.2. Check through Command in User Layer

Execute command **cat /proc/sys/kernel/boot_reason** in user layer to query the power-on type. Different return values indicate different power-on type:

● 1 indicates the module is reset or rebooted.
● 2 indicates the module is powered on by SMPL.
● 3 indicates the module is powered on by RTC alarm at the specified time.
● 7 indicates the module is powered on by pressing the powerkey

As shown in the figure below, the command returns 7 to indicate that the module is powered on by pressing the powerkey.

```
root@mdm9607-perf:/proc/sys/kernel# cat boot_reason
7
root@mdm9607-perf:/proc/sys/kernel# 
```

3.2.3. Check through Reading PMIC Information in User Layer

The PON_PON_REASON1 register is read-only, and is used to store the power-on types. The slave whose address is 0x808 is used to check the power-on reason.

```
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0# echo 0x808 > address
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0# cat data
00800 -- -- -- -- -- -- -- 01
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0#
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0# []
```

The meaning of each bit of 0x808 represents:

Table 1: Bit Information

Bit	Name	Description
7	KPDPWR_N	Read Only Triggered from new KPDPWR press 1: TRIGGER_RECEIVED
6	CBLPWR_N	Read Only Triggered from CBL_PER1_N 1: TRIGGER_RECEIVED
5	PON1	Read Only Triggered from PON1 1: TRIGGER_RECEIVED
4	USB_CHG	Read Only Triggered from USB charger 1: TRIGGER_RECEIVED
3	DC_CHG	Read Only Triggered from DC charger 1: TRIGGER_RECEIVED
2	RTC	Read Only Triggered from RTC 1: TRIGGER_RECEIVED
1	SMPL	Read Only Triggered from SMPL 1: TRIGGER_RECEIVED
0	HARD_RESET	Read Only Triggered from a Hard Reset event (check POFF reason for the trigger) 1: TRIGGER_RECEIVED

4 Appendix A References

Table 2: Terms and Abbreviations

Abbreviation	Description
IC	Integrated Circuit
PMIC	Power Management IC
RTC	Real-Time Clock
SMPL	Sudden Momentary Power Loss
USB	Universal Serial Bus