AG35-QuecOpen

GPIO Assignment

LTE Module Series

Rev. AG35-QuecOpen_GPIO_Assignment_V1.3

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Status: Preliminary

Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
7th Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

History

Revision	Date	Author	Description
1.0	2018-04-28	Eden LIU	Initial
1.1	2018-06-26	Eden LIU	Updated the note for pin 159 and pin 160.
1.2	2018-09-07	Eden LIU	1) Updated the function for pin 9, 160, 170 and pin 171. 2) Updated the remark for pins multiplexing.
1.3	2018-09-14	Eden LIU	1) Updated the voltage domain information of USB interface. 2) Updated the description information for interrupt.

IMPORTANT NOTES:

"B-PD": Bidirectional digital with CMOS input

"BH-PD": Bidirectional digital with CMOS input and high voltage tolerant

"PD": Contain an internal pulldown device

"PU": Contain an internal pullup device

"L": Low level, "H": High level

By default, module PINs have the primary function.

The interrupt can be a normal interrupt or a sleep wake-up interrupt, please see field "Interrupt".

THE ITEMS WITH DARK GREY BACKGROUND COLOR ARE NOT SUPPORTED IN THIS STAGE.

"BOOT_CONFIG_xx & FORCE_USB_BOOT": means this pin **MUST** be kept the "Reset" status when powering up module, or the module cannot probably boot.

Pins Multiplexing for AG35 QuecOpen

Pin No.	Pin Name	Default Function Interface	Pin Multiplexing				Power Domain	Reset	GPIO Status in Booting	Interrupt	Remark
			Primary Function	Alternate Function 1	Alternate Function 2	Alternate Function3					
1	RESET_N	Reset	RESET_N	--	--	--	1.8V		--	--	
2	PWRKEY	Power Key	PWRKEY	--	--	--	1.8V		--	--	
170	NET_STATUS		PMU_GPIO_01	NET_STATUS	--	--	1.8V		Low level in GPIO Mode	✗	If use this PIN for GPIO purpose, it can only be OUTPUT mode.
171	STATUS		STATUS		--	--	1.8V		Low level in GPIO Mode	--	
176	SHDN_N	Shut down	SHDN_N	--	--	--	1.8V	B-PD,H	--	--	
4	VDD_MDIO	SGMII	VDD_MDIO	--	--	--	1.8V/2.85V		--	--	Dedicated pin(VDD for MDIO)
6	EPHY_RST_N		EPHY_RST_N	--	--	--	1.8V/2.85V	BH-PD,L	--	--	
7	SGMII_CLK		SGMII_CLK	--	--	--	1.8V/2.85V	BH-PD,L	--	--	
8	SGMII_DATA		SGMII_DATA	--	--	--	1.8V/2.85V	BH-PD,L	--	--	
9	EPHY_INT_N		EPHY_INT_N	--	--	--	1.8V	B-PD,L	--	--	
11	SGMII_RX_M		SGMII_RX_M	--	--	--	Analog signal	L	--	--	Dedicated pin
12	SGMII_RX_P		SGMII_RX_P	--	--	--	Analog signal	L	--	--	Dedicated pin
14	SGMII_TX_P		SGMII_TX_P	--	--	--	Analog signal	L	--	--	Dedicated pin
15	SGMII_TX_M		SGMII_TX_M	--	--	--	Analog signal	L	--	--	Dedicated pin
18	SDC1_CMD	WLAN & BT	SDC1_CMD	GPIO_17	UART_RXD_BLSP4	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
19	SDC1_CLK		SDC1_CLK	GPIO_16	UART_TXD_BLSP4	--	1.8V	B-NP,L	Low level in GPIO Mode	✓	
20	SDC1_DATA0		SDC1_DATA0	GPIO_15	UART_CTS_BLSP1	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
21	SDC1_DATA1		SDC1_DATA1	GPIO_14	UART_RTS_BLSP1	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
22	SDC1_DATA2		SDC1_DATA2	GPIO_13	UART_RXD_BLSP1	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
23	SDC1_DATA3		SDC1_DATA3	GPIO_12	UART_TXD_BLSP1	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
149	WLAN_EN		WLAN_EN	GPIO_54	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	BOOT_CONFIG_6
160	WLAN_WAKE		WLAN_WAKE	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	Dedicated pin
169	WLAN_SLP_CLK		WLAN_SLP_CLK	PMU_GPIO_06	--	--	1.8V		Low level in GPIO Mode	✗	If use this PIN for GPIO purpose, it can only be OUTPUT mode.
5	PM_ENABLE_WIFI		PM_ENABLE_WIFI	PMU_GPIO_03	--	--	1.8V	L	Low level in GPIO Mode	✗	If use this PIN for GPIO purpose, it can only be OUTPUT mode.
3	BT_EN		BT_EN	PMU_GPIO_02	--	--	1.8V	L	Low level in GPIO Mode	✗	If use this PIN for GPIO purpose, it can only be OUTPUT mode.

46	VDD_SDIO	SD /EMMC	VDD_SDIO	--	--	--	LOW SD Voltage:1.8V HIGH SD Voltage:2.85V	L	--	--	Power,Dedicated pin
47	SDC2_DATA2		SDC2_DATA2	--	--	--		B-PD,L	--	--	SDIO signal level can be selected according to the one supported by SD card. 1.8V power domain for eMMC. Please refer to SD 3.0 protocol for more details.
48	SDC2_DATA3		SDC2_DATA3	--	--	--		B-PD,L	--	--	
49	SDC2_DATA0		SDC2_DATA0	--	--	--		B-PD,L	--	--	
50	SDC2_DATA1		SDC2_DATA1	--	--	--		B-PD,L	--	--	
51	SDC2_CMD		SDC2_CMD	--	--	--		B-PD,L	--	--	
53	SDC2_CLK		SDC2_CLK	--	--	--		B-PD,L	--	--	
52	SDC2_INT_DET		SDC2_INT_DET	GPIO_26	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	FOR EMMC_RST
145	COEX_UART_TXD	WLAN/BT Coexistence Control	COEX_UART_TXD	--	--	--	1.8V	B-PD,L	--	✗	BOOT_CONFIG_3
146	COEX_UART_RXD		COEX_UART_RXD	--	--	--	1.8V	B-PD,L	--	✓	Dedicated pin. Besides, this pin is also FORCE_USB_BOOT, which means module can enter download mode when pulling up the pin during booting.
56	UART1_CTS	UART1	UART_CTS_BLSP3	GPIO_3	SPI_CLK_BLSP3	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
57	UART1_RTS		UART_RTS_BLSP3	GPIO_2	SPI_CS_N_BLSP3	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
58	UART1_RXD		UART_RXD_BLSP3	GPIO_1	SPI_MISO_BLSP3	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
60	UART1_TXD		UART_TXD_BLSP3	GPIO_0	SPI_MOSI_BLSP3	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
163	UART2_TXD	UART2	UART_TXD_BLSP5	GPIO_8	SPI_MOSI_BLSP5	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	When use BT data function,It is using GPIO_8~GPIO_11 as BT uart.
164	UART2_CTS		UART_CTS_BLSP5	GPIO_11	SPI_CLK_BLSP5	--	1.8V	B-PD,L	High level in GPIO Mode	✓	
165	UART2_RXD		UART_RXD_BLSP5	GPIO_9	SPI_MISO_BLSP5	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
166	UART2_RTS		UART_RTS_BLSP5	GPIO_10	SPI_CS_N_BLSP5	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
71	DBG_TXD	DEBUG UART	DBG_TXD	--	--	--	1.8V	B-PD,L	--	--	Dedicated pin
72	DBG_RXD		DBG_RXD	--	--	--	1.8V	B-PD,L	--	--	Dedicated pin
77	SPI_MOSI	SPI	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6	PCM_1_SYNC	1.8V	B-PD,L	Low level in GPIO Mode	✓	When use BT audio function,It is using GPIO_20~GPIO_23 as BT PCM.
78	SPI_MISO		SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6	PCM_1_DIN	1.8V	B-PD,L	Low level in GPIO Mode	✓	
79	SPI_CS_N		SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6	PCM_1_DOUT	1.8V	B-PD,L	Low level in GPIO Mode	✓	
80	SPI_CLK		SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6	PCM_1_CLK	1.8V	B-PU,H	High level in GPIO Mode	✗	BOOT_CONFIG_4
65	PCM_SYNC	PCM	PCM_SYNC	GPIO_79	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	BOOT_CONFIG_7
66	PCM_IN		PCM_IN	GPIO_76	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	
67	PCM_CLK		PCM_CLK	GPIO_78	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	BOOT_CONFIG_8
68	PCM_OUT		PCM_OUT	GPIO_77	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
152	MCLK		MCLK	--	--	--	1.8V	B-PD,L	--	--	
42	I2C1_SDA	I2C1 (Host Only)	I2C_SDA_BLSP4	GPIO_18	--	--	1.8V	B-PD,L	High level in GPIO Mode	✗	FOR Communicate to codec default
43	I2C1_SCL		I2C_SCL_BLSP4	GPIO_19	--	--	1.8V	B-PD,L	High level in GPIO Mode	✗	FOR Communicate to codec default

73	I2C2_SDA	I2C2 (Host Only)	I2C_SDA_BLSP2	GPIO_6	--	--	1.8V	B-PD,L	high pulse in GPIO Mode	✗	Recommended as input pin when used as GPIO
74	I2C2_SCL		I2C_SCL_BLSP2	GPIO_7	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	
25	USIM_PRESENCE	USIM	USIM_PRESENCE	GPIO_34	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	If use this PIN for GPIO purpose, the SIM hot swap is not available any more.
26	USIM_VDD		USIM_VDD	--	--	--	1.8V / 2.85V		--	--	Dedicated pin
27	USIM_CLK		USIM_CLK	--	--	--	1.8V / 2.85V	BH-PD,L	--	--	Dedicated pin
28	USIM_RST		USIM_RST	--	--	--	1.8V / 2.85V	BH-PD,L	--	--	Dedicated pin
29	USIM_DATA		USIM_DATA	--	--	--	1.8V / 2.85V	BH-PD,L	--	--	Dedicated pin
32	USB_VBUS	USB	USB_VBUS	--	--	--	5V		--	--	Dedicated pin
33	USB_DM		USB_DM	--	--	--			--	--	Dedicated pin
34	USB_DP		USB_DP	--	--	--			--	--	Dedicated pin
59	GPIO1	GPIO	GPIO_38	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	BOOT_CONFIG_12
61	GPIO2		GPIO_75	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	In Quectel LPM feature, it is regarded as wakeup_in
62	GPIO3		GPIO_74	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	In Quectel BT feature, it is regarded as BT WAKEUP HOST
144	GPIO4		GPIO_25	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	BOOT_CONFIG_2
147	GPIO5		GPIO_24	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	BOOT_CONFIG_1 In Quectel LPM feature, it is regarded as wakeup_out
150	GPIO6		GPIO_42	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✓	In Quectel BT feature, it is regarded as HOST WAKEUP BT. (When the pin is used as GPIO, it is recommended to be used as OUTPUT. If it is intended to be used as INPUT, the GPIO should config as no-pull mode (pull-up or pull-down), and an external pull circuit should be added.)
159	GPIO7		GPIO_58	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	BOOT_CONFIG_11 When the pin is used as GPIO, it is recommended to be used as OUTPUT. If it is intended to be used as INPUT, the GPIO should config as no-pull mode (pull-up or pull-down), and an external pull circuit should be added.
143	GPIO8		GPIO_41	--	--	--	1.8V	B-PD,L	Low level in GPIO Mode	✗	When the pin is used as GPIO, it is recommended to be used as OUTPUT. If it is intended to be used as INPUT, the GPIO should config as no-pull mode (pull-up or pull-down), and an external pull circuit should be added.
173	ADC0	ADC	ADC0	--	--	--	Analog signal		--	--	PMU(MPP_04)
175	ADC1		ADC1	--	--	--	Analog signal		--	--	PMU(MPP_06)
172	ADC2		ADC2	--	--	--	Analog signal		--	--	PMU(PA_THERM2)
132	SPK2_P	Audio	SPK2_P	--	--	--	Analog signal		--	--	The built-in codec uses the same signals as the module's PCM interface (pins 65~68) for external digital audio design. Therefore, when the built-in codec is utilized, the PCM interface cannot be used for other purposes
133	SPK2_N		SPK2_N	--	--	--	Analog signal		--	--	
134	SPK1_P		SPK1_P	--	--	--	Analog signal		--	--	
135	SPK1_N		SPK1_N	--	--	--	Analog signal		--	--	
136	MICBIAS		MICBIAS	--	--	--	MICBIAS		--	--	
137	MIC2_N		MIC2_N	--	--	--	Analog signal		--	--	
138	MIC2_P		MIC2_P	--	--	--	Analog signal		--	--	
139	MIC1_N		MIC1_N	--	--	--	Analog signal		--	--	
140	MIC1_P		MIC1_P	--	--	--	Analog signal		--	--	
141	AGND		AGND	--	--	--	Analog GND		--	--	