EC2x&AG35-Quecopen

PCM Interface Configuration

LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2018-04-11	Grady QUAN	Initial
1.1	2018-08-28	Grady QUAN	Added AG35 pin

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1 Introduction

This document mainly introduces how to configure PCM interface especially how to configure the pins and the interfaces from the perspective of users development to use PCM interface.

2 Hardware Design

2.1. Pins Assignment

2.1.1. The Primary PCM

Table 1: Multiplexing the Primary PCM Pins

Pin Name	Pin Number	Primary Function	Multiplexing Function 1	Multiplexing Function 2	Multiplexing Function 3	Multiplexing Function 4
SPI_CS_N	37(EC2x)/ 79(AG35)	SPI_CS_N _BLSP6	PCM_IN	I2S_IN	GPIO22	UART_RTS_BLSP6
SPI_MOSI	38(EC2x)/ 77(AG35)	SPI_MOSI _BLSP6	PCM_OUT	I2S_OUT	GPIO20	UART_TXD_BLSP6
SPI_MISO	39(EC2x)/ 78(AG35)	SPI_MISO _BLSP6	PCM_SYNC	I2S_WS	GPIO21	UART_RXD_BLSP6
SPI_CLK	40(EC2x)/ 80(AG35)	SPI_CLK_ BLSP6	PCM_CLK	I2S_CLK	GPIO23	UART_CTS_BLSP6

The primary PCM is used as SPI function by default, so it needs to configure the pins of the primary PCM to PCM function.

2.1.2. The Second PCM

Table 2: Multiplexing the Second PCM Pins

Pin Name	Pin Number	Primary Function	Multiplexing Function 1	Multiplexing Function 2
PCM_IN	24(EC2x)/ 66(AG35)	PCM_IN	I2S_IN	GPIO76
PCM_OUT	25(EC2x)/ 68(AG35)	PCM_OUT	I2S_OUT	GPIO77
PCM_SYNC	26(EC2x)/ 65(AG35)	PCM_SYNC	I2S_WS	GPIO79
PCM_CLK	27(EC2x)/ 67(AG35)	PCM_CLK	I2S_CLK	GPIO78

The second PCM is used as SPI function by default.

2.2. Recommended Circuit Design

The following figure is the reference design of PCM interface with an external Codec chip:

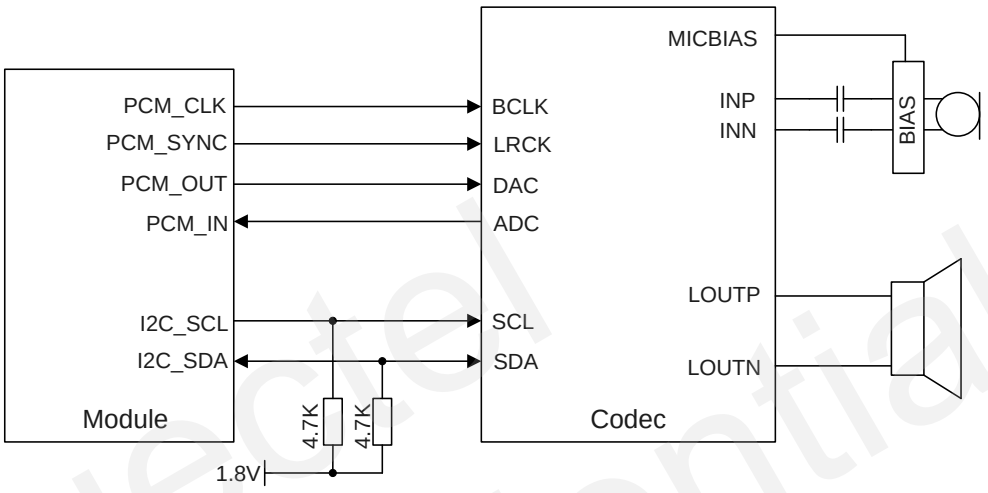

Figure 1：PCM Circuit Reference Design

It is suggested to reserve RC (R=22Ω, C=22pF) circuit on PCM signal lines, especially PCM_CLK.

3 PCM Timing Analysis

3.1. Timings of Auxiliary and Primary Modes

The timings of PCM auxiliary and primary modes are shown respectively in the following figures. Data is triggered on the falling edge of PCM_SYNC in primary mode (Figure 2) while triggered on the rising edge in auxiliary mode (Figure 3).

Figure 2: Timing of Primary Mode

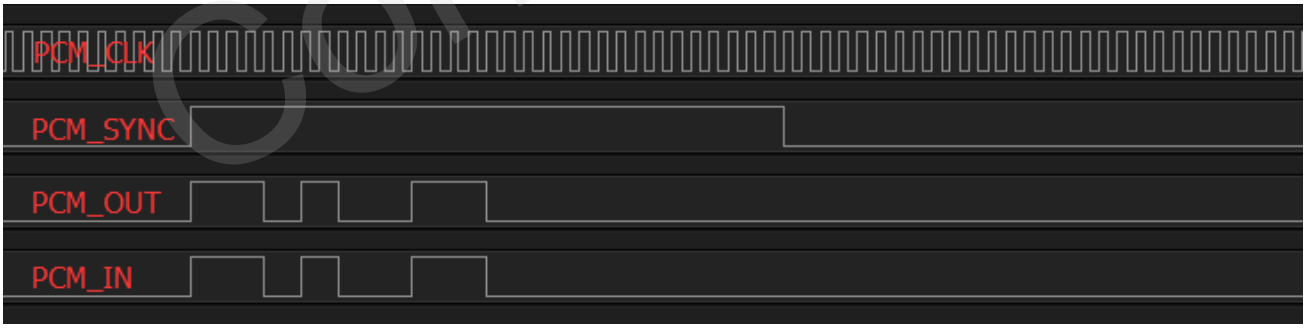

Figure 3: Timing of Auxiliary Mode

3.2. Different Timings of Time Slot

Each time slot of PCM occupies 16 bits of data. Figure 4 shows the timing of PCM data in time slot 1 and Figure 5 shows the timing of PCM data in time slot 2. Time slot 2 shifts 16 bits backward compared with

time slot 2.

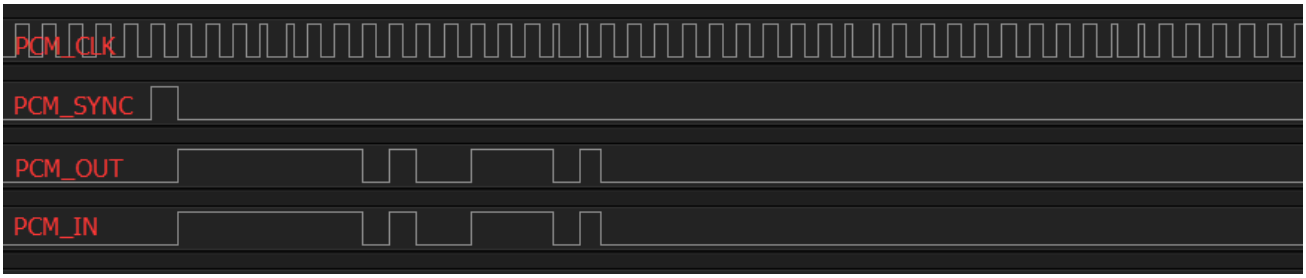

Figure 4: Timing of Data in time slot 1

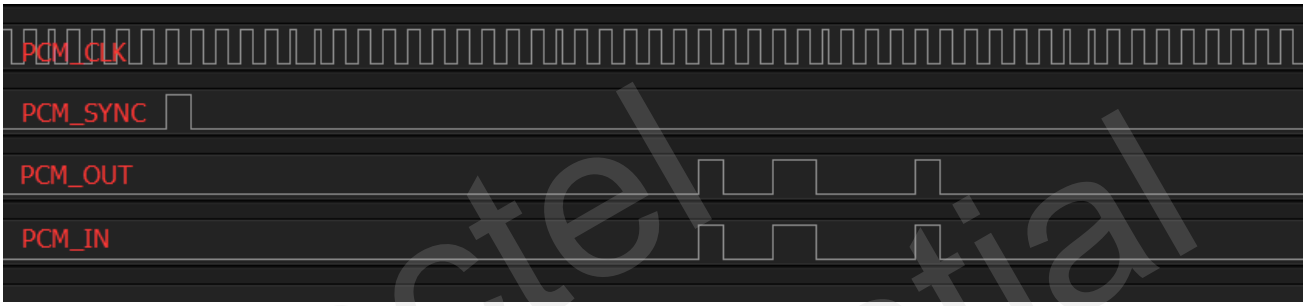

Figure 5: Timing of Data in time slot 2

3.3. Different Timings of Sample Rates

PCM supports 8kHz and 16kHz sample rates. Figure 6 shows the timing of 8kHz sample rate and that the interval between two sync signals is 0.125ms. Figure 7 shows the timing of 16kHz sample rate and that the interval between two sync signals is 62.5 μs.

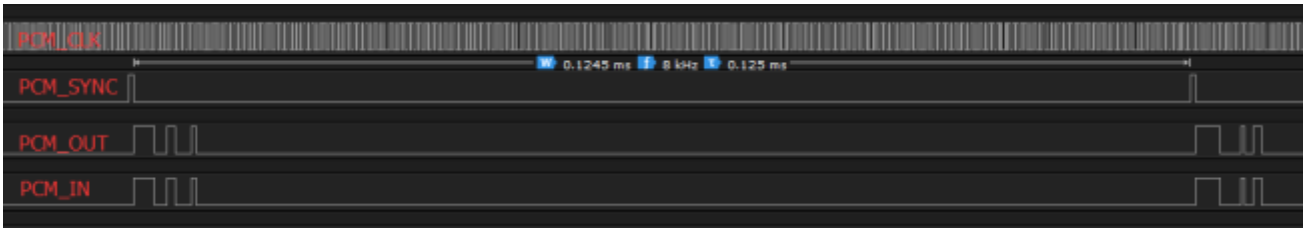

Figure 6: Timing of 8kHz Sample Rate

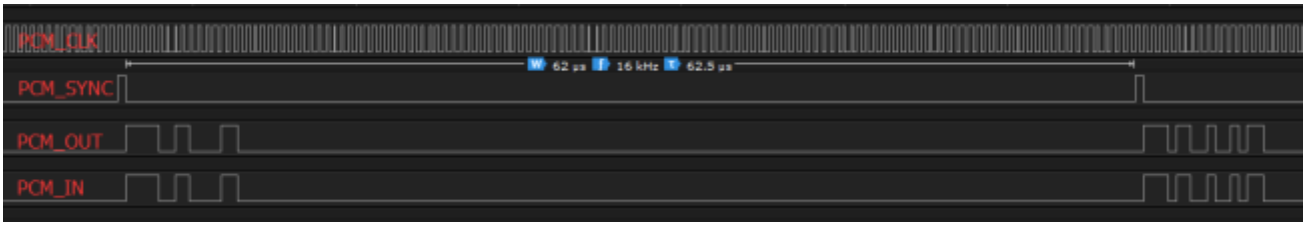

Figure 7: Timing of 16kHz Sample Rate

4 PCM Pin Configurations

4.1. mdm9607-mtp.dtsi

4.1.1. The Primary PCM

The primary PCM pins correspond to gpio20, gpio21, gpio22, and gpio23. In the codes released on the platform, the primary PCM pins are used as SPI6, so SPI6 in mdm9607-mtp.dtsi needs to be disabled. Please modify the codes as follows:

```
    &spi_6 {
-           status = "ok";
+           status = "disabled";
    };
```

4.1.2. The Second PCM

The second PCM pins correspond to gpio76, gpio77, gpio78 and gpio79. In the codes released on the platform, the pins have been used as PCM function, so it is not necessary to modify the codes.

4.2. mdm9607-pinctrl.dtsi

The description of some parameters of this file can be referred to qcom,mdm9607-pinctrl.txt in path: apps_proc/kernel/Documentation/devicetree/bindings/pinctrl.

4.2.1. The Primary PCM

Modify the primary PCM pins to gpio20, gpio21, gpio22 and gpio23. Please see the modification as below:

```
    pmx_pri_auxpcm {
            pri_auxpcm_ws_active: pri_auxpcm_ws_active {
            mux {
-               pins = "gpio79";
-               function = "sec_mi2s";
```

```
+                   pins = "gpio20";
+                   function = "pri_mi2s_ws_a";
                };
                config {
-                   pins = "gpio79";
+                   pins = "gpio20";
                    drive-strength = <8>;     /* 8 MA */
                    bias-disable;              /* No PULL */
                    output-high;
                };
            };
```

```
            pri_auxpcm_sck_active: pri_auxpcm_sck_active {
                mux {
-                   pins = " gpio78";
-                   function = "sec_mi2s";
+                   pins = "gpio23";
+                   function = "pri_mi2s_sck_a";
                };
                config {
-                   pins = "gpio78";
+                   pins = "gpio23";
                    drive-strength = <8>;     /* 8 MA */
                    bias-disable;              /* No PULL */
                    output-high;
                };
            };
```

```
            pri_auxpcm_dout_active: pri_auxpcm_dout_active {
                mux {
-                   pins = " gpio77";
-                   function = "sec_mi2s";
+                   pins = "gpio22";
+                   function = "pri_mi2s_data1_a";
                };
                config {
-                   pins = "gpio77";
+                   pins = "gpio22";
                    drive-strength = <8>;     /* 8 MA */
                    bias-disable;              /* No PULL */
                    output-high;
                };
            };
            pri_auxpcm_ws_sleep: pri_auxpcm_ws_sleep {
```

```
                mux {
-                       pins = "gpio79";
-                       function = "sec_mi2s";
+                       pins = "gpio20";
+                       function = "pri_mi2s_ws_a";
                };
                config {
-                       pins = "gpio79";
+                       pins = "gpio20";
                        drive-strength = <2>;     /* 2 MA */
                        bias-pull-down;               /* PULL DOWN */
                };
        };
```

```
        pri_auxpcm_sck_sleep: pri_auxpcm_sck_sleep {
                mux {
-                       pins = " gpio78";
-                       function = "sec_mi2s";
+                       pins = "gpio23";
+                       function = "pri_mi2s_sck_a";
```

```
                };
                config {
-                       pins = "gpio78";
+                       pins = "gpio23";
                        drive-strength = <2>;     /* 2 MA */
                        bias-pull-down;               /* PULL DOWN */
                };
        };
```

```
        pri_auxpcm_dout_sleep: pri_auxpcm_dout_sleep {
                mux {
-                       pins = " gpio77";
-                       function = "sec_mi2s";
+                       pins = "gpio22";
+                       function = "pri_mi2s_data1_a";
                };
```

```
                config {
-                       pins = "gpio77";
+                       pins = "gpio22";
                        drive-strength = <2>;     /* 2 MA */
                        bias-pull-down;               /* PULL DOWN */
                };
```

```
        };
    };
```

```
    pmx_pri_auxpcm_din {
        pri_auxpcm_din_active: pri_auxpcm_din_active {
            mux {
-                   pins = " gpio76";
-                   function = "sec_mi2s";
+                   pins = "gpio21";
+                   function = "pri_mi2s_data0_a";
            };
            config {
-                   pins = "gpio76";
+                   pins = "gpio21";
                    drive-strength = <8>;     /* 8 MA */
                    bias-disable;             /* No PULL */
            };
        };
```

```
        pri_auxpcm_din_sleep: pri_auxpcm_din_sleep {
            mux {
-                   pins = " gpio76";
-                   function = "sec_mi2s";
+                   pins = "gpio21";
+                   function = "pri_mi2s_data0_a";
            };
            config {
-                   pins = "gpio76";
+                   pins = "gpio21";
                    drive-strength = <2>;     /* 2 MA */
                    bias-pull-down;               /* PULL DOWN */
            };
        };
    };
```

Here drive-strength stands for the drive strength of I/O pins, and bias-disable, bias-pull-down stand for I/O pin status and output-high means to output high level voltage.

4.2.2. The Second PCM

The second PCM pins whose codes have been released on the platform do not need to be modified.

4.3. mdm9607.dtsi

The description of some parameters of this file can be referred to qcom-audio-dev.txt in path: apps_proc/kernel/Documentation/devicetree/bindings/sound.

4.3.1. The Primary PCM

Open pinctrl corresponded to the primary PCM and modify the codes as follows:

```
    dai_pri_auxpcm: qcom,msm-pri-auxpcm {
        ……
        qcom,msm-auxpcm-interface = "primary";
-       /*pinctrl-names = "default", "idle";
+       pinctrl-names = "default", "idle";
        pinctrl-0 = <&pri_auxpcm_ws_active
                &pri_auxpcm_sck_active
                &pri_auxpcm_dout_active
                &pri_auxpcm_din_active>;
        pinctrl-1 = <&pri_auxpcm_ws_sleep
                &pri_auxpcm_sck_sleep
                &pri_auxpcm_dout_sleep
                &sec_auxpcm_din_sleep>;
-       */
    };
```

4.3.2. The Second PCM

The pinctrl corresponded to the second PCM is open by default.

4.4. PCM Pin Mode Verification

After modifying the device tree files, users can execute the command cat /sys/kernel/debug/gpio to verify whether the pins are in PCM mode.

```
~ # cat /sys/kernel/debug/gpio
GPIOs 0-79, platform/1000000.pinctrl, 1000000.pinctrl:
 gpio0   : out 1 2mA no pull
 gpio1   : out 1 2mA no pull
 gpio2   : out 1 2mA no pull
 gpio3   : out 1 2mA no pull
 gpio4   : out 2 2mA pull down
 gpio5   : in  2 2mA pull down
 gpio6   : in  0 2mA pull down
 gpio7   : in  0 2mA pull down
 gpio8   : in  0 2mA pull down
 gpio9   : in  0 2mA pull down
 gpio10  : in  0 2mA pull down
 gpio11  : in  0 2mA pull up
 gpio12  : in  0 2mA pull down
 gpio13  : in  0 2mA pull down
 gpio14  : in  0 2mA pull down
 gpio15  : in  0 2mA pull down
 gpio16  : in  0 2mA no pull
 gpio17  : in  0 2mA pull down
 gpio18  : in  0 2mA pull down
 gpio19  : in  0 2mA pull down
 gpio20  : out 3 8mA no pull
 gpio21  : in  3 8mA no pull
 gpio22  : out 3 8mA no pull
 gpio23  : out 3 8mA no pull
```

Figure 8: Pin Status 1

```
gpio54  : in  0 2mA pull down
gpio55  : out 0 2mA no pull
gpio56  : in  0 2mA no pull
gpio57  : out 0 2mA no pull
gpio58  : in  0 2mA pull down
gpio59  : in  0 2mA pull down
gpio60  : in  0 2mA pull down
gpio61  : in  0 2mA pull down
gpio62  : in  0 2mA pull down
gpio63  : in  0 2mA pull down
gpio64  : in  0 2mA pull down
gpio65  : in  0 2mA pull down
gpio66  : in  0 2mA pull down
gpio67  : in  0 2mA pull down
gpio68  : in  0 2mA pull down
gpio69  : in  0 2mA pull down
gpio70  : in  0 2mA pull down
gpio71  : in  0 2mA pull down
gpio72  : in  0 2mA pull down
gpio73  : in  0 2mA pull down
gpio74  : in  0 2mA pull down
gpio75  : out 0 2mA no pull
gpio76  : in  2 8mA no pull
gpio77  : out 2 8mA no pull
gpio78  : out 2 8mA no pull
gpio79  : out 1 8mA no pull
```

Figure 9: Pin Status 2

5 PCM Interface Configuration

5.1. mdm9607.dtsi

There are many parameters to be configured for PCM interfaces, but the methods to configure the two PCM interfaces are similar. Take the primary PCM as an example to introduce how to configure every parameter. For the second PCM, please also refer to this method.

5.1.1. Master and Slave Modes

The PCM interface defaults to be in master mode. If it is necessary to modify it into slave mode, please do as follows:

Code 1:

```
    sound{
            compatible = "qcom,mdm9607-audio-tomtom";
            ……
-           qcom,auxpcm-interface-mode = "pri_pcm_master", "sec_pcm_master";
+           qcom,auxpcm-interface-mode = "pri_pcm_slave", " sec_pcm_master ";
            asoc-platform = <&pcm0>, <&pcm1>, <&voip>, <&voice>,
            ……
    }
```

The first parameter stands for the primary PCM mode while the second one stands for the second PCM mode.

Code 2:

```
    dai_pri_auxpcm: qcom,msm-pri-auxpcm {
            compatible = "qcom,msm-auxpcm-dev";
            qcom,msm-cpudai-auxpcm-mode = <0>, <0>;
-           qcom,msm-cpudai-auxpcm-sync = <1>, <1>;
+           qcom,msm-cpudai-auxpcm-sync = <0>, <0>;
            qcom,msm-cpudai-auxpcm-frame = <5>, <5>;
            ……
```

“1” stands for master mode and “2” stands for slave mode. The first value is configured at 8kHz sample rate while the second one is configured at 16kHz sample rate.

5.1.2. Frame Format

PCM interface defaults to primary mode format. If it is necessary to modify it to auxiliary mode format, please do as follows:

```
    dai_pri_auxpcm: qcom,msm-pri-auxpcm {
                compatible = "qcom,msm-auxpcm-dev";
-               qcom,msm-cpudai-auxpcm-mode = <0>, <0>;
+               qcom,msm-cpudai-auxpcm-mode = <1>, <1>;
                qcom,msm-cpudai-auxpcm-sync = <1>, <1>;
                qcom,msm-cpudai-auxpcm-frame = <5>, <5>;
                ……
    }
```

“1” stands for auxiliary mode while “0” stands for primary mode. The first value is configured at 8kHz sample rate while the second one is configured at 16kHz sample rate.

5.1.3. Clock

The default clock for PCM interface at 8kHz sample rate is 2M and the default clock at 16kHz sample rate is 4M. If it is necessary to modify the clock such as modifying it to 1M at 8kHz sample rate or modifying it to 2M at 16kHz sample rate, please do as follows:

```
    dai_pri_auxpcm: qcom,msm-pri-auxpcm {
                compatible = "qcom,msm-auxpcm-dev";
                qcom,msm-cpudai-auxpcm-mode = <0>, <0>;
                qcom,msm-cpudai-auxpcm-sync = <1>, <1>;
-               qcom,msm-cpudai-auxpcm-frame = <5>, <5>;
+               qcom,msm-cpudai-auxpcm-frame = <4>, <4>;
                qcom,msm-cpudai-auxpcm-quant = <2>, <2>;
                qcom,msm-cpudai-auxpcm-num-slots = <1>, <1>;
                qcom,msm-cpudai-auxpcm-slot-mapping = <1>, <1>;
                qcom,msm-cpudai-auxpcm-data = <0>, <0>;
-               qcom,msm-cpudai-auxpcm-pcm-clk-rate = <2048000>, <4096000>;
+               qcom,msm-cpudai-auxpcm-pcm-clk-rate = <1024000>, <2048000>;
                ……
    }
```

qcom,msm-cpudai-auxpcm-pcm-clk-rate that stands for PCM clock supports 256kHz, 512kHz, 1024kHz, 2048kHz and 4096kHz, in which 4096kHz only supports 16kHz sample rate. The first value is configured at 8kHz sample rate while the second one configured at 16kHz sampling rate.

qcom,msm-cpudai-auxpcm-frame shows the bits quantity per frame. The first value is configured at 8kHz sample rate while the second one configured at 16kHz sample rate. The values corresponding to the numbers 0~5 are as follows

5 - 256BPF
4 - 128BPF
3 - 64BPF
2 - 32BPF
1 - 16BPF
0 - 8BPF

For example if the clock supports 1024k with 8kHz sample rate, then it is 128 bits per frame and the corresponding number is 4.

5.1.4. Time Slot

PCM interfaces use the first time slot by default. If another time slot is needed, please modify it as follows:

```
    dai_pri_auxpcm: qcom,msm-pri-auxpcm {
            compatible = "qcom,msm-auxpcm-dev";
            qcom,msm-cpudai-auxpcm-mode = <0>, <0>;
            ……
-           qcom,msm-cpudai-auxpcm-slot-mapping = <1>, <1>;
+           qcom,msm-cpudai-auxpcm-slot-mapping = <2>, <2>;
            ……
    }
```

“1” stands for the first time slot while “2” stands for the second one. PCM has 16 time slots in total. The first value is configured at 8kHz sample rate while the second one configured at 16kHz sample rate.

5.2. mdm9607.c

5.2.1. Sample Rate

The sample rates of primary and second PCM interfaces are initialized by static global variable mdm_auxpcm_rate. Users can obtain and set up PCM sample rates by the two functions: mdm_auxpcm_rate_get, mdm_auxpcm_rate_put. The static global variable is initialized to 8kHz sample rate by default. If it is necessary to modify it to 16kHz sample rate, do as follows:

```
-   static int mdm_auxpcm_rate = SAMPLE_RATE_8KHZ;
+   static int mdm_auxpcm_rate = SAMPLE_RATE_16KHZ;
```