EC2x&AG35-Quecopen

Device Tree Configuration Instruction

LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2017-12-20	Gale GAO	Initial
1.1	2018-09-28	Larry ZHANG	Added PCM related properties and enabling device nodes

Contents

1 Device Tree Related Files

QuecOpen is developed based on Qualcomm platform. 9x07 platform device tree source file is located in ql-ol-kernel/arch/arm/boot/dts/qcom/ and 9x28 platform device tree source file is located in ql-ol-kernel/msm-3.18/arch/arm/boot/dts/qcom/. The DTB that 9x07 platform and 9x28 platform used is mdm9607-mtp.dtb.

This file is mainly compiled by the following files:

```
arch/arm/boot/dts/qcom/mdm9607-mtp.dts          # dts source file, root of DTB
arch/arm/boot/dts/qcom/mdm9607-pinctrl.dtsi     # pin function define
arch/arm/boot/dts/qcom/mdm9607.dtsi             # platform feature define
arch/arm/boot/dts/qcom/mdm9607-mtp.dtsi         # list of interface features
```

To configure the Device Tree of the project, please only modify three files: mdm9607-pinctrl.dtsi, mdm9607.dtsi and mdm9607-mtp.dtsi.

2 Corresponding Functions of Peripheral Interface

2.1. 9x07 Platform

For all the I/O interface types and the quantities opened in OpenLinux, please refer to **EC2x_OpenLinux_GPIO_Assignment_Speadsheet**. The correspondence of I/O interfaces in the Device Tree nodes is as follows:

Table 1: Correspondence of I/O Interfaces in the Device Tree Nodes

PIN Num	Interface	Primary Function	GPIO	Address	Device Node	Remarks
37	SPI 6 Interface	SPI6_CS	GPIO_22	Spi6 spi@78ba000	/dev/spi	Enabled by default; Multiplexed with UART6
38		SPI6_MOSI	GPIO_20			
39		SPI6_MISO	GPIO_21			
40		SPI6_CLK	GPIO_23			
41	I2C-2 interface, host only	I2C2_SCL	GPIO_7	I2c2 i2c@78b6000	/dev/i2c-2	Enabled by default; Used to communicate with codec
42		I2C2_SDA	GPIO_6			
12	UART-5 interface (DEBUG UART interface)	UART5_TX	GPIO_8	blsp1_uart5: serial@78b3000	/dev/ttyHSL0	Enabled by default; Debug the serial port, do not modify
11		UART5_RX	GPIO_9			
63	UART-2 interface	UART2_TX	GPIO_4	blsp1_uart2: serial@78b0000	/dev/ttyHSL1	Enabled by default;
66		UART2_RX	GPIO_5			
38	UART-6	UART6_TX	GPIO_20	blsp1_uart6:	/dev/ttyHSL2	Disabled by

	interface			serial@78b4000		default; Multiplexed with SPI, need to modify to enable Device Tree
39		UART6_RX	GPIO_21			
67	UART-3 interface (MAIN UART-interface)	UART3_TXD	GPIO_0	blsp1_uart3: serial@78b1000	/dev/ttyHS0	Enabled by default
68		UART3_RXD	GPIO_1			
65		UART3_RTS	GPIO_2			
64		UART3_CTS	GPIO_3			

2.2. 9x28 Platform

For all the I/O interface types and the quantities opened in OpenLinux, please refer to **EC2x_QuecOpen_GPIO_Assignment_Speadsheet**. The correspondence of I/O interfaces in the Device Tree nodes is as follows:

Table 2: Correspondence of I/O Interfaces in the Device Tree Nodes

PIN Num	Interface	Primary Function	GPIO	Address	Device Node	Remarks
79	SPI 6 Interface	SPI6_CS	GPIO_22	Spi6 spi@78ba000	/dev/spi	Enabled by default; Multiplexed with UART6
77		SPI6_MOSI	GPIO_20			
78		SPI6_MISO	GPIO_21			
80		SPI6_CLK	GPIO_23			
74	I2C-2 interface, host only	I2C2_SCL	GPIO_7	I2c2 i2c@78b6000	/dev/i2c-2	Enabled by default;
73		I2C2_SDA	GPIO_6			
43	I2C-4 interface, host only	I2C4_CLK	GPIO_19	I2c4 i2c@78b8000	/dev/i2c-4	Enabled by default; Used to communicate with codec
42		I2C4_SDA	GPIO_18			
163	UART-5	UART5_TX	GPIO_8	blsp1_uart5:	/dev/ttyHSL1	Disabled by

165	interface	UART5_RX	GPIO_9	serial@78b3000		default
71	UART-2 interface (DEBUG UART interface)	UART2_TX	GPIO_4	blsp1_uart2: serial@78b0000	/dev/ttyHSL0	Enabled by default; Debug the serial port, do not modify
72		UART2_RX	GPIO_5			
77	UART-6 interface	UART6_TX	GPIO_20	blsp1_uart6: serial@78b4000	/dev/ttyHSL2	Disabled by defaul; Multiplexed with SPI, need to modify to enable Device Tree
78		UART6_RX	GPIO_21			
60	UART-3 interface (MAIN UART-interface)	UART3_TXD	GPIO_0	blsp1_uart3: serial@78b1000	/dev/ttyHS0	Enabled by default
58		UART3_RXD	GPIO_1			
57		UART3_RTS	GPIO_2			
56		UART3_CTS	GPIO_3			

3 Modifying Device Tree Related Files

3.1. UART Related Properties and Enabled Device Nodes

Take UART6 as an example, it is disabled by default.

NOTE

This group of pins have been enabled as SPI.

3.1.1. Function Configurations when the pins are in active and sleep status

File path: arch/arm/boot/dts/qcom/mdm9607-pinctrl.dtsi

The node definition of UART6 pin is shown in the figure below. Node blsp1_uart_active defines the pin configuration of UART6 interface in working status. Configure function to “blsp_uart6” mode. blsp1_uart_sleep is the pin configuration of UART6 interface when the system suspends. Configure function to “GPIO” mode.

```
/* UART6: add gpio20,21 uart6 by gale */
blsp1_uart6_active: blsp1_uart6_active {
        mux {
                pins = "gpio20", "gpio21";
                function = "blsp_uart6";
        };

        config {
                pins = "gpio20", "gpio21";
                drive-strength = <2>;
                bias-pull-down;
        };
};

blsp1_uart6_sleep: blsp1_uart6_sleep {
        mux {
                pins = "gpio20", "gpio21";
                function = "gpio";
        };
        config {
                pins = "gpio20", "gpio21";
                drive-strength = <2>;
                bias-pull-down;
        };
};
```

Function configured when the system is active

Function configured when the system suspends

3.1.2. Configuring Other Properties

File path: arch/arm/boot/dts/qcom/mdm9607.dtsi

Configure other properties, such as corresponding driver, register address, interrupts, clocks etc..

```
/* UART6: add gpio20,21 uart6 by gale */
blsp1_uart6: serial@78b4000 { /* BLSP1 UART6 */
        compatible = "qcom,msm-lsuart-v14";
        reg = <0x78b4000 0x200>;
        interrupts = <0 122 0>;
        clocks = <&clock_gcc clk_gcc_blsp1_uart6_apps_clk>,
              <&clock_gcc clk_gcc_blsp1_ahb_clk>;
        clock-names = "core_clk", "iface_clk";
        status = "disabled";
};
```

Configure other properties and corresponding driver here

3.1.3. UART Master Switch

File path: arch/arm/boot/dts/qcom/mdm9607-mtp.dtsi

Use the function configured by mdm9607-pinctl.dtsi, and enable serial port function; status="disabled" means to disable serial port function.

NOTE

If gpio20, gpio21 multiplex to UART, SPI, GPIO, it can only enable one of them. Please set the corresponding status of UART, SPI to disabled if gpio20,gpio21 are used as normal GPIO.

```
/* UART6: enable gpio20, 21 uart6 by gale */
&blsp1_uart6 {
        status = "disabled";
        pinctrl-names = "default";
        pinctrl-0 = <&blsp1_uart6_active>;
};
```

Here select the function configured in mdm9607-pinctl.dtsi. Disable UART by default.

3.2. I2C Related Properties and Enabled Device Nodes

9x07 platform I2C2, used to communicate with codec
9x28 platform I2C4, used to communicate with codec

Here's an example of I2C4 modification.

3.2.1. Function Configurations When the Pins Are in Active and Sleep Status

File path: arch/arm/boot/dts/qcom/mdm9607-pinctrl.dtsi

The node definition of I2C4 pin is shown in the figure below. Node i2c_4_active defines the pin configuration of I2C4 interface in working status. Configure function to “blsp_i2c4” mode. i2c_4_sleep is the pin configuration of I2C4 interface when the system suspends. Configure function to “GPIO” mode.

3.2.2. Configuring Other Properties

File path: arch/arm/boot/dts/qcom/mdm9607.dtsi

Configure other properties, such as function in mdm9607-pinctl.dtsi, corresponding driver, register address, interrupts, clocks etc.

```
i2c_4: i2c@78b8000 { /* BLSP1 QUP4 */
        compatible = "qcom,i2c-msm-v2";
        #address-cells = <1>;
        #size-cells = <0>;
        reg-names = "qup_phys_addr";
        reg = <0x78b8000 0x600>;
        interrupt-names = "qup_irq";
        interrupts = <0 98 0>;
        qcom,clk-freq-out = <400000>;
        qcom,clk-freq-in  = <19200000>;
        clock-names = "iface_clk", "core_clk";
        clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,
                 <&clock_gcc clk_gcc_blsp1_qup4_i2c_apps_clk>;

        pinctrl-names = "i2c_active", "i2c_sleep";
        pinctrl-0 = <&i2c_4_active>;
        pinctrl-1 = <&i2c_4_sleep>;
        qcom,noise-rjct-scl = <0>;
        qcom,noise-rjct-sda = <0>;
        qcom,master-id = <86>;
        dmas = <&dma_blsp1 18 64 0x20000020 0x20>,
               <&dma_blsp1 19 32 0x20000020 0x20>;
        dma-names = "tx", "rx";
        status = "disabled";

        //2016-02-23, add by jun.wu
        alc5616_codec@1b{
                compatible = "quec,quec-alc5616-i2c";
                reg = <0x1b>;
        };

        //2016-02-23, add by jun.wu
        nau8814_codec@1a{
                compatible = "quec,quec-nau8814-i2c";
                reg = <0x1a>;
        };
```

Here are other properties of I2C. Select function defined in mdm9607-pinctl.dtsi

3.2.3. I2C Master Switch

File path: arch/arm/boot/dts/qcom/mdm9607-mtp.dtsi

Configure serial port to enabled status. Here status="ok" means to enable I2C function. Please modify the status to disabled and turn off the multiplexed function of pin if I2C is used as normal GPIO.

```
&i2c_4 {
        status = "ok";
};
```

i2c_4 master switch; Enabled by default

3.3. SPI Related Properties and Enabled Device Nodes

Enable SPI by default and insmod kmod. Application programming please refer to **QuecOpen_Peripheral_API_Guidelines_V1.0**.

3.3.1. Function Configurations When the Pins Are in Active and Sleep Status

Modify file: arch/arm/boot/dts/qcom/mdm9607-pinctrl.dtsi

The node definition of SPI6 is shown in the figure below. Node spi6_default defines the pin configuration of SPI6 interface in working status. Configure function to “blsp_spi6” mode. spi_sleep is the pin configuration of SPI6 interface when the system suspends. Configure function to “gpio” mode and configure the status of CS pins.

```
spi6 {
        spi6_default: spi6_default {
                /* active state */
                mux {
                        /* MOSI, MISO CLK */
                        pins = "gpio20","gpio21","gpio23";
                        function = "blsp_spi6";
                };

                config {
                        pins = "gpio20","gpio21","gpio23";
                        drive-strength = <12>; /* 12 MA */
                        bias-disable = <0>; /* No PULL */
                };
        };

        spi6_sleep: spi6_sleep {
                /* suspended state */
                mux {
                        /* MOSI, MISO, CLK */
                        pins = "gpio20","gpio21","gpio23";
                        function = "gpio";
                };

                config {
                        pins = "gpio20","gpio21","gpio23";
                        drive-strength = <2>; /* 2 MA */
                        bias-pull-down; /* PULL Down */
                };
        };
        spi6_cs0_active: cs0_active {
                /* CS */
                mux {
                        pins = "gpio22";
                        function = "blsp_spi6";
                };

                config {
                        pins = "gpio22";
                        drive-strength = <2>;
                        bias-disable = <0>;
                };
```

Function and drive strength configured when the system is active. Pull up and down.

Function and drive strength configured when the system suspends. Pull up and down.

CS pin configuration

3.3.2. Configuring Other Properties

File path: arch/arm/boot/dts/qcom/mdm9607.dtsi

Configure other properties, such as function in mdm9607-pinctl.dtsi, corresponding driver, register address, interrupts, clocks etc.

```
        /*BLSP QUP6*/
    spi_6: spi@78ba000 {
            compatible = "qcom,spi-qup-v2";
            #address-cells = <1>;
            #size-cells = <0>;
            reg-names = "spi_physical", "spi_bam_physical";
            reg = <0x78ba000 0x600>,
                  <0x7884000 0x2b000>;
            interrupt-names = "spi_irq", "spi_bam_irq";
            interrupts = <0 100 0>, <0 238 0>;
            spi-max-frequency = <19200000>;
            pinctrl-names = "spi_default", "spi_sleep";
            pinctrl-0 = <&spi6_default &spi6_cs0_active>;
            pinctrl-1 = <&spi6_sleep &spi6_cs0_sleep>;
            clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,
                     <&clock_gcc clk_gcc_blsp1_qup6_spi_apps_clk>;
            clock-names = "iface_clk", "core_clk";
            qcom,infinite-mode = <0>;
            qcom,use-bam;
            qcom,use-pinctrl;
            qcom,ver-reg-exists;
            qcom,bam-consumer-pipe-index = <22>;
            qcom,bam-producer-pipe-index = <23>;
            qcom,master-id = <86>;
            status = "disabled";
    };
     /*end cullen.wang*/
```

Here are other configurations of SPI.
Select function in mdm9607-pinctl.dtsi

3.3.3. SPI6 Master Switch

File path: arch/arm/boot/dts/qcom/mdm9607-mtp.dtsi

Configure SPI to enabled status. Here status="ok" means to enable SPI function. Please turn off all multiplexed pin functions if SPI6 is used as normal GPIO.

```
//add by cullen
&spi_6 {
        status = "ok";
};
```

SPI master switch; Enabled by default

3.4. PCM Related Properties and Enabled Device Nodes

Enable PCM by default, used to communicate with codec

Please refer to **Quectel_EC2X&AG35-QuecOpen_PCM Interface Configurations _V1.1_Preliminary.docx**.

3.4.1. Function Configurations When the Pins Are in Active and Sleep Status

Modify file: arch/arm/boot/dts/qcom/mdm9607-pinctrl.dtsi

The node definition of PCM is shown in the figure below. Node sec_auxpcm_xx_active defines the pin configuration of PCM interface in working status. Configure function to "sec_mi2s" mode.

sec_auxpcm_xx_sleep is the pin configuration of PCM interface when the system suspends. Configure function to “GPIO” mode. Configure function to “sec_mi2s” mode.

```
pmx_sec_auxpcm {
		sec_auxpcm_ws_active: sec_auxpcm_ws_active {
		mux {
			pins = "gpio79";
			function = "sec_mi2s";
		};
		config {
			pins = "gpio79";
			drive-strength = <8>;   /* 8 MA */
			bias-disable;           /* No PULL */
			output-high;
		};
	};

	sec_auxpcm_sck_active: sec_auxpcm_sck_active {
		mux {
			pins = "gpio78";
			function = "sec_mi2s";
		};

		config {
			pins = "gpio78";
			drive-strength = <8>;   /* 8 MA */
			bias-disable;           /* No PULL */
			output-high;
		};
	};

	sec_auxpcm_dout_active: sec_auxpcm_dout_active {
		mux {
			pins = "gpio77";
			function = "sec_mi2s";
		};
		config {
			pins = "gpio77";
			drive-strength = <8>;   /* 8 MA */
			bias-disable;           /* No PULL */
			output-high;
		};
	};

	sec_auxpcm_ws_sleep: sec_auxpcm_ws_sleep {
		mux {
			pins = "gpio79";
			function = "sec_mi2s";
		};
		config {
			pins = "gpio79";
			drive-strength = <2>;   /* 2 MA */
			bias-pull-down;         /* PULL DOWN */
		};
	};

	sec_auxpcm_sck_sleep: sec_auxpcm_sck_sleep {
		mux {
			pins = "gpio78";
			function = "sec_mi2s";
		};
		config {
			pins = "gpio78";
			drive-strength = <2>;   /* 2 MA */
			bias-pull-down;         /* PULL DOWN */
		};
	};
```

```
            sec_auxpcm_dout_sleep: sec_auxpcm_dout_sleep {
                    mux {
                            pins = "gpio77";
                            function = "sec_mi2s";
                    };

                    config {
                            pins = "gpio77";
                            drive-strength = <2>;   /* 2 MA */
                            bias-pull-down;         /* PULL DOWN */
                    };
            };
    };

    pmx_sec_auxpcm_din {
                    sec_auxpcm_din_active: sec_auxpcm_din_active {
                    mux {
                            pins = "gpio76";
                            function = "sec_mi2s";
                    };
                    config {
                            pins = "gpio76";
                            drive-strength = <8>;   /* 8 MA */
                            bias-disable;           /* No PULL */
                    };
            };

            sec_auxpcm_din_sleep: sec_auxpcm_din_sleep {
                    mux {
                            pins = "gpio76";
                            function = "sec_mi2s";
                    };
                    config {
                            pins = "gpio76";
                            drive-strength = <2>;   /* 2 MA */
                            bias-pull-down;         /* PULL DOWN */
                    };
            };
    };
```

3.4.2. Configuring Other Properties

File path: arch/arm/boot/dts/qcom/mdm9607.dtsi

Configure other properties, such as function in mdm9607-pinctl.dts, corresponding driver, clocks etc.

```
    dai_sec_auxpcm: qcom,msm-sec-auxpcm {
            compatible = "qcom,msm-auxpcm-dev";
            qcom,msm-cpudai-auxpcm-mode = <0>, <0>;
            qcom,msm-cpudai-auxpcm-sync = <1>, <1>;
            qcom,msm-cpudai-auxpcm-frame = <5>, <5>;
            qcom,msm-cpudai-auxpcm-quant = <2>, <2>;
            qcom,msm-cpudai-auxpcm-num-slots = <1>, <1>;
            qcom,msm-cpudai-auxpcm-slot-mapping = <1>, <1>;
            qcom,msm-cpudai-auxpcm-data = <0>, <0>;
            qcom,msm-cpudai-auxpcm-pcm-clk-rate = <2048000>, <40960000>;
            qcom,msm-auxpcm-interface = "secondary";
            pinctrl-names = "default", "idle";
                    pinctrl-0 = <&sec_auxpcm_ws_active
                                 &sec_auxpcm_sck_active
                                 &sec_auxpcm_dout_active
                                 &sec_auxpcm_din_active>;
                    pinctrl-1 = <&sec_auxpcm_ws_sleep
                                 &sec_auxpcm_sck_sleep
                                 &sec_auxpcm_dout_sleep
                                 &sec_auxpcm_din_sleep>;
    };
```

3.4.3. PCM Master Driver

PCM function is open by default. Currently there's no status switch.
If users need to use the pins corresponding to PCM function as normal GPIO, please modify it as follows:

```
diff --git a/mdm9607.dtsi b/mdm9607.dtsi
index 0995a2a..cc7903c 100755
--- a/mdm9607.dtsi
+++ b/mdm9607.dtsi
@@ -1169,7 +1169,7 @@
                qcom,msm-cpudai-auxpcm-pcm-clk-rate = <2048000>, <40960000>;
                qcom,msm-auxpcm-interface = "secondary";
                pinctrl-names = "default", "idle";
-               pinctrl-0 = <&sec_auxpcm_ws_active
+               /*      pinctrl-0 = <&sec_auxpcm_ws_active
                                        &sec_auxpcm_sck_active
                                        &sec_auxpcm_dout_active
                                        &sec_auxpcm_din_active>;
@@ -1177,6 +1177,7 @@
                                        &sec_auxpcm_sck_sleep
                                        &sec_auxpcm_dout_sleep
                                        &sec_auxpcm_din_sleep>;
+               */
        };
```

Because the pin is multiplexing, it is necessary to confirm if it is enabled in other nodes. Please pay attention to the following code modification. Confirm if GPIO of pinctrl-0 set in mdm9607-pinctrl.dtsi is gpio76/77/78/79. If so, please modify it as follows:

```
index 6418b04..8a561b3 100755
--- a/mdm9607.dtsi
+++ b/mdm9607.dtsi
@@ -1218,7 +1218,7 @@
                qcom,msm-cpudai-auxpcm-data = <0>, <0>;
                qcom,msm-cpudai-auxpcm-pcm-clk-rate = <2048000>, <4096000>;     //for pcm 16k, clock rate nede 4096000
                qcom,msm-auxpcm-interface = "primary";
-               /*pinctrl-names = "default", "idle";
+               /* pinctrl-names = "default", "idle";
                        pinctrl-0 = <&pri_auxpcm_ws_active
                                        &pri_auxpcm_sck_active
                                        &pri_auxpcm_dout_active
@@ -1227,7 +1227,7 @@
                                        &pri_auxpcm_sck_sleep
                                        &pri_auxpcm_dout_sleep
                                        &sec_auxpcm_din_sleep>;
-               */
+               */
        };
```

4 Regenerating boot.img

4.1. Compiling Kernel

```
ql-ol-sdk$ make kernel
```

mdm9607-perf-boot.img will be generated in target directory

4.2. Downloading Firmware

Replace boot.img in the original firmware with boot.img in ql-ol-sdk/target/ directory

Download with the tool Quectel_Customer_FW_Download_Tool_V4.30 or fastboot.