AG35-Quecopen

Reference Design

LTE Module Series

Rev. AG35-Quecopen_Reference_Design_Rev.A

Date: 2018-06-05

Status: Released

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About the Document

History

Revision	Date	Author	Description
A	2018-06-05	Canice CHEN	Initial

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel AG35-Quecopen module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Module Interface

Notes:

1. ADC pin cannot be directly connected to the power supply and must not exceed the voltage range.
2. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
3. Keep all RESERVED and unused pins unconnected, and ensure all GND pins are connected to the ground network.
4. PCM_***_BT network is used for communication with AF20 module. CODEC_PCM_*** network is used for communication with codec.
5. Pins 59, 65, 67, 80, 144, 145, 146, 147, 149 and 159 must be at low level before the module starts up successfully.
6. The module supports both Analog Audio and Digital Audio via PCM interface (pin 65 ~pin 68), but the two functions cannot be used synchronously.

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CHECKED BY Yeoman CHEN	SIZE A2	VER A
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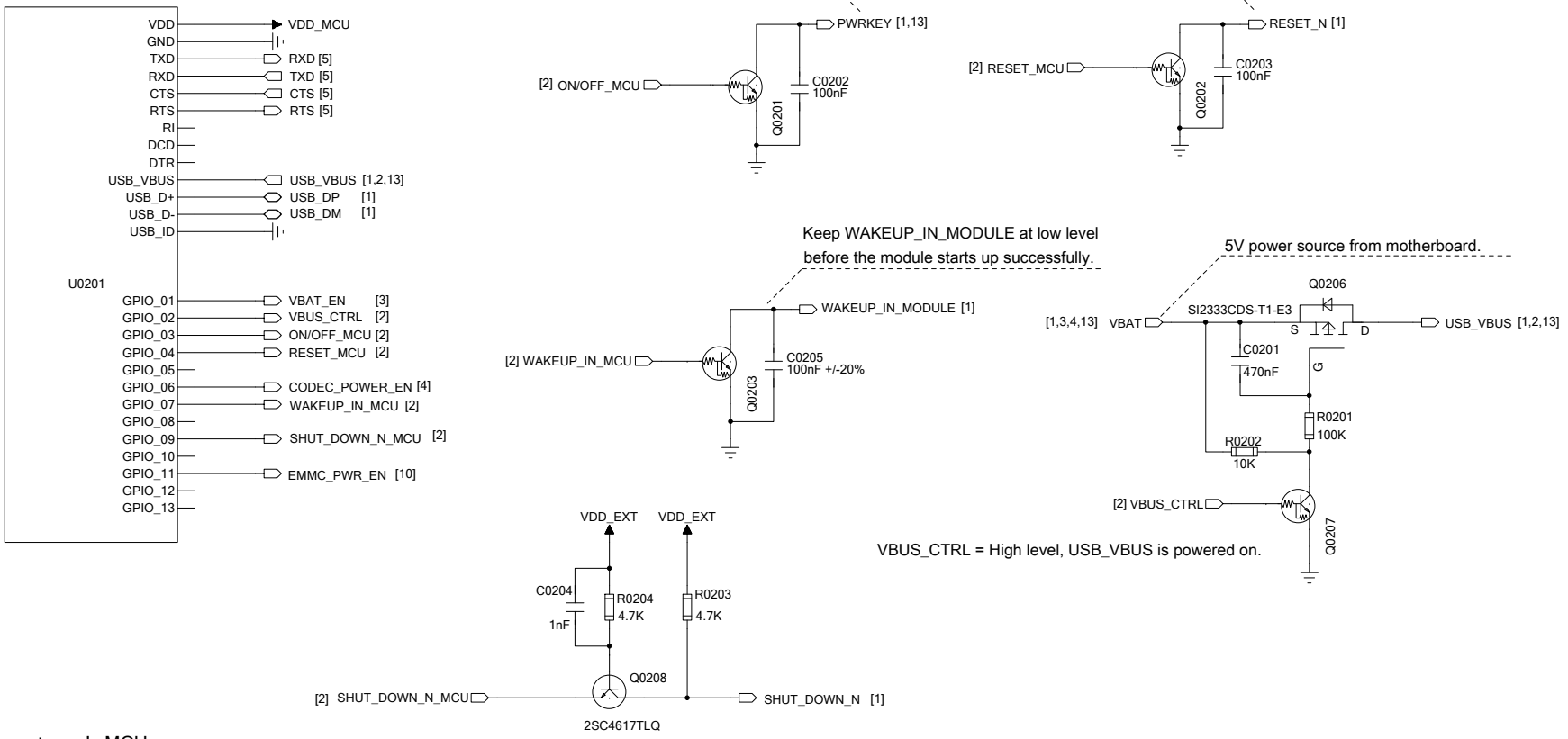
MCU Interface



Notes:

1. U0201 represents customer's MCU.
2. AG35-Quecopen can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and AG35-Quecopen should be powered by a 5V power system for USB detection, and VBUS_CTRL is used to turn on/off VBUS power supply. When VBUS_CTRL is at high level, USB_VBUS will be powered on.
3. Transistor circuits (Q0201~Q0203, Q0208) are used for level translation.

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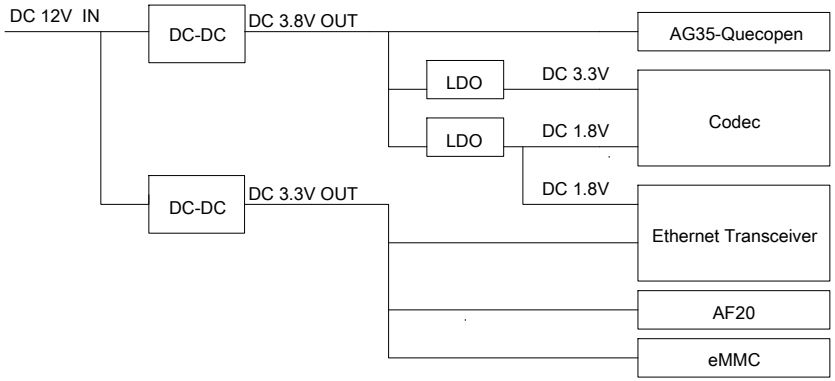
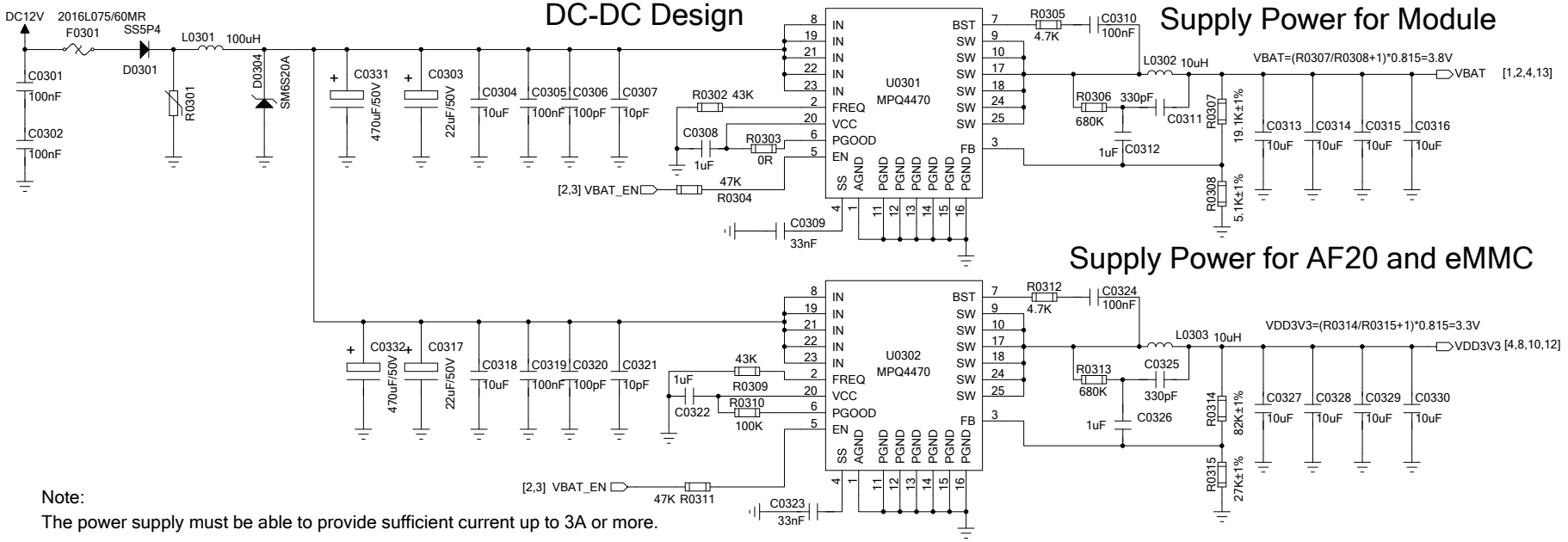
Power Supply Design (Part 1)

Block Diagram for DC-DC Application

A DC-DC converter is used to convert a high input voltage into 3.8V and 3.3V outputs, and then the LDOs will generate 3.3V and 1.8V typical voltages.



DC-DC Design



Supply Power for Module

Supply Power for AF20 and eMMC

Note:
The power supply must be able to provide sufficient current up to 3A or more.

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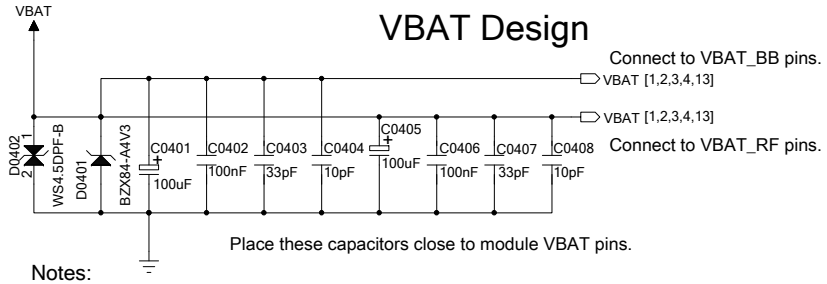
Power Supply Design (Part 2)

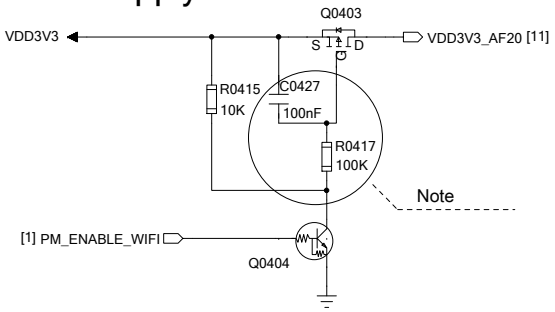
VBAT Design



Notes:

1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.

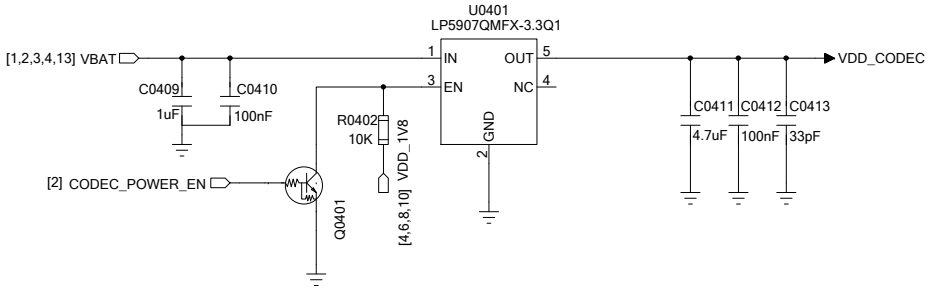
Supply Power for AF20

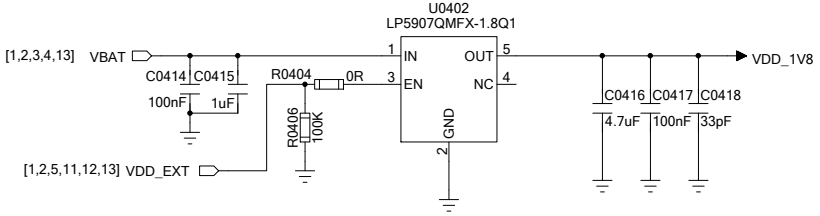


Note:

The RC circuit, which is assembled with R0417 and C0427, is used to delay the start-up of MOSFET switch circuit.

Supply Power for PCM Codec





Note:

CODEC_POWER_EN must be at low level in order to ensure normal output voltage of VDD_CODEC.
If VDD_CODEC power supply needs to be switched off, please keep CODEC_POWER_EN at high level.

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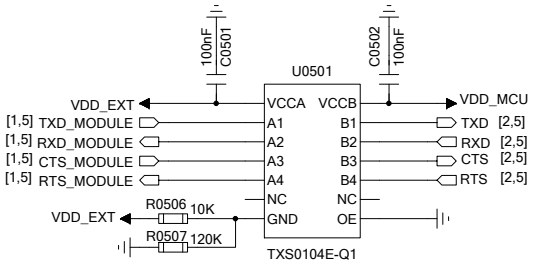
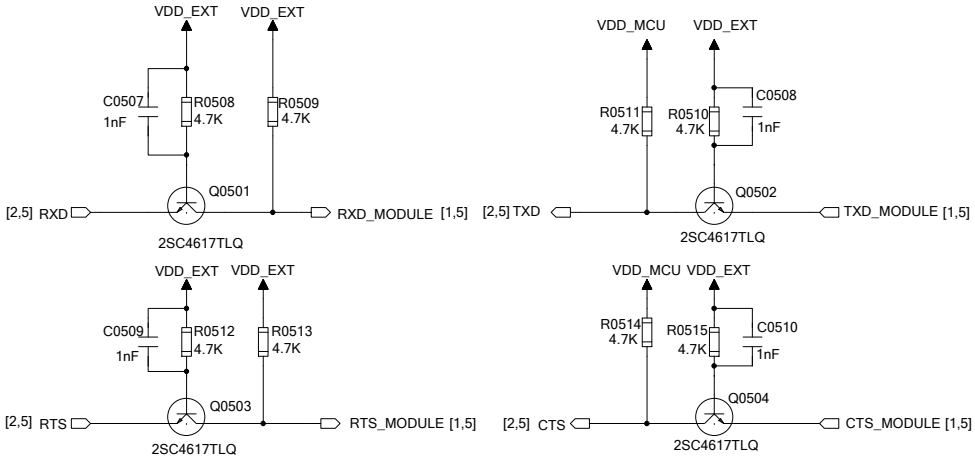
UART and (U)SIM Design

UART Level Translation - IC Solution (Recommended)



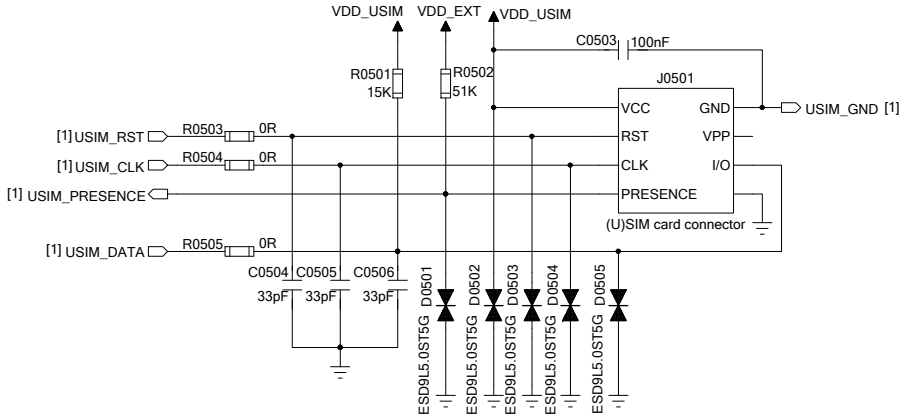
UART Level Translation - Transistor Solution



Notes:

1. It is recommended to use the voltage level translation IC solution.
   The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. The supply voltage range of VCCA should not exceed that of VCCB. For more information about TXS0104E-Q1, please refer to the datasheet from TI.
3. If high baud rate is needed, it is highly recommended to install four 1nF capacitors (C0507/C0508 /C0509/C0510) on transistor circiuts.

(U)SIM Interface



Notes:

1. The decouple capacitor of VDD_USIM should be less than 1uF and must be near to (U)SIM card connector.
2. AG35-Quecopen module provides an input pin (USIM_PRESENCE) to detect whether the (U)SIM card exists or not. It supports both low level and high level detections.
   For more details, please refer to *Quectel_AG35-Quecopen_Hardware_Design*.
3. R0503~R0505 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
4. It is recommended to take electrostatic discharge (ESD) protection measures near the (U)SIM card connector. The TVS diode with junction capacitance less than 10 pF must be placed as close as possible to the (U)SIM card connector.
5. R0501 can improve anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.

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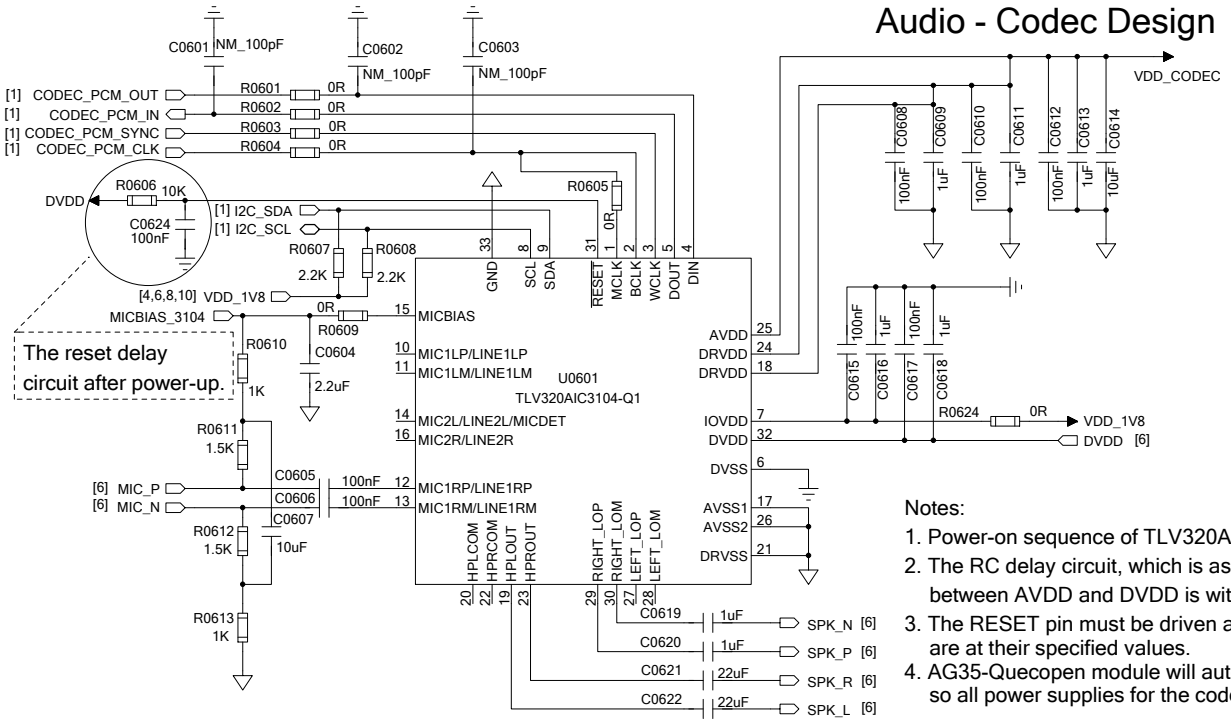
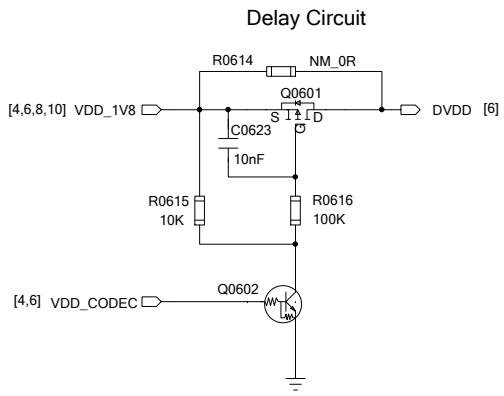
Audio Design (PCM Interface)

Audio - Codec Design



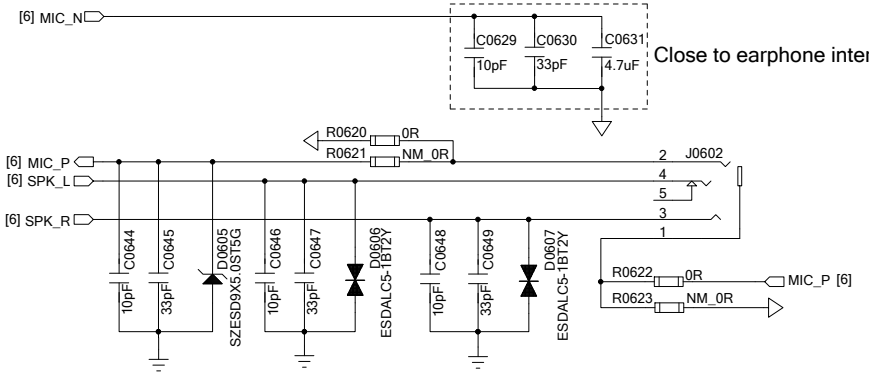
Delay Circuit

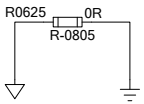


Notes:

1. Power-on sequence of TLV320AIC3104-Q1: IOVDD → AVDD/DRVDD → DVDD → Software Initialization
2. The RC delay circuit, which is assembled with C0623 and R0616, is used to ensure that the power-on time difference between AVDD and DVDD is within 5ms. For more details, please refer to TLV320AIC3104-Q1 datasheet.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104-Q1 are at their specified values.
4. AG35-Quecopen module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be turned on before that.

Audio - Earphone Application



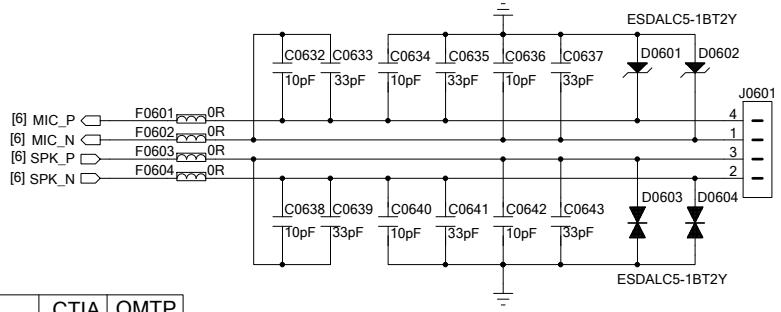


	CTIA	OMTP
R0621/R0623	NM	M
R0620/R0622	M	NM

Notes:

1. The analog output only drives earphone and handset. For larger power loads such as speakers, the design for an audio power amplifier should be added.
2. The maximum capacitive loading for speaker is 330 pF and the maximum capacitive loading for microphone is 250 pF.

Audio - Handset Application



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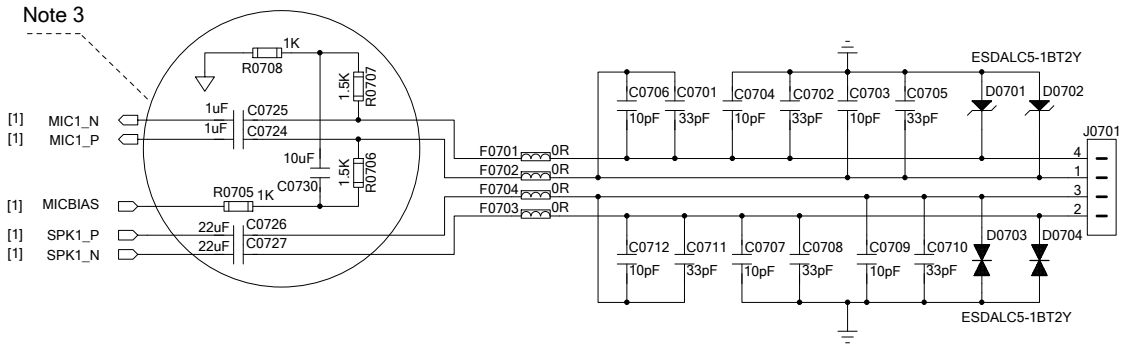
Audio Design (Analog Interface)

Audio - Handset Application



Notes:

1. The analog output only drives handset. For larger power loads such as speakers, the design for an audio power amplifier should be added.
2. The maximum capacitive loading for speaker is 330 pF and the maximum capacitive loading for microphone is 250 pF.
3. The analog output and input interface circuits should close to AG35-Quecopen.

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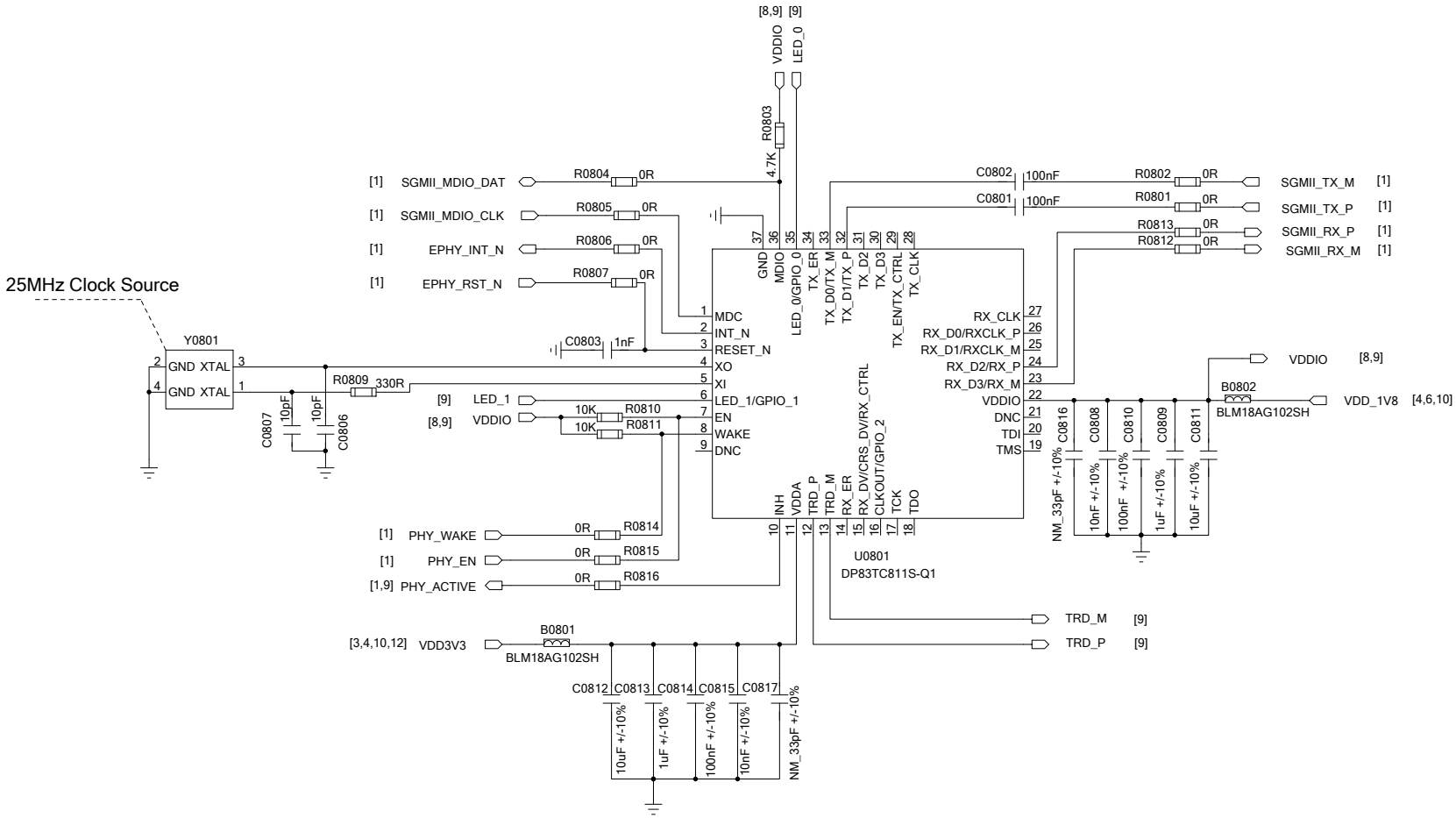
Ethernet Transceiver Design (Part 1)



Note:
SGMII interface for DP83TC811S-Q1 Ethernet transceiver function is still under development.

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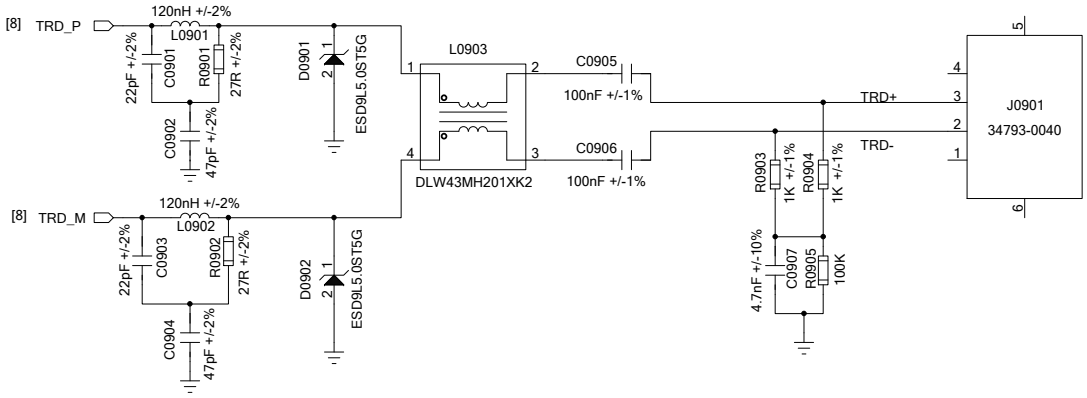
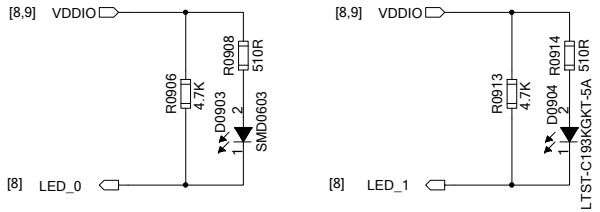
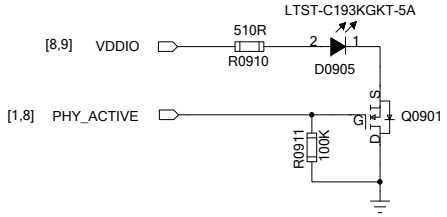
Ethernet Transceiver Design (Part 2)



Link Rate Indication LEDs



Operation Status Indication LED



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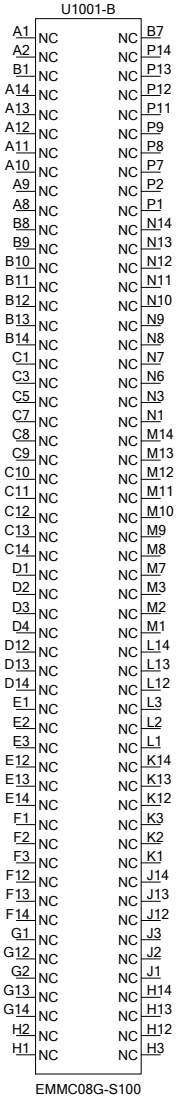
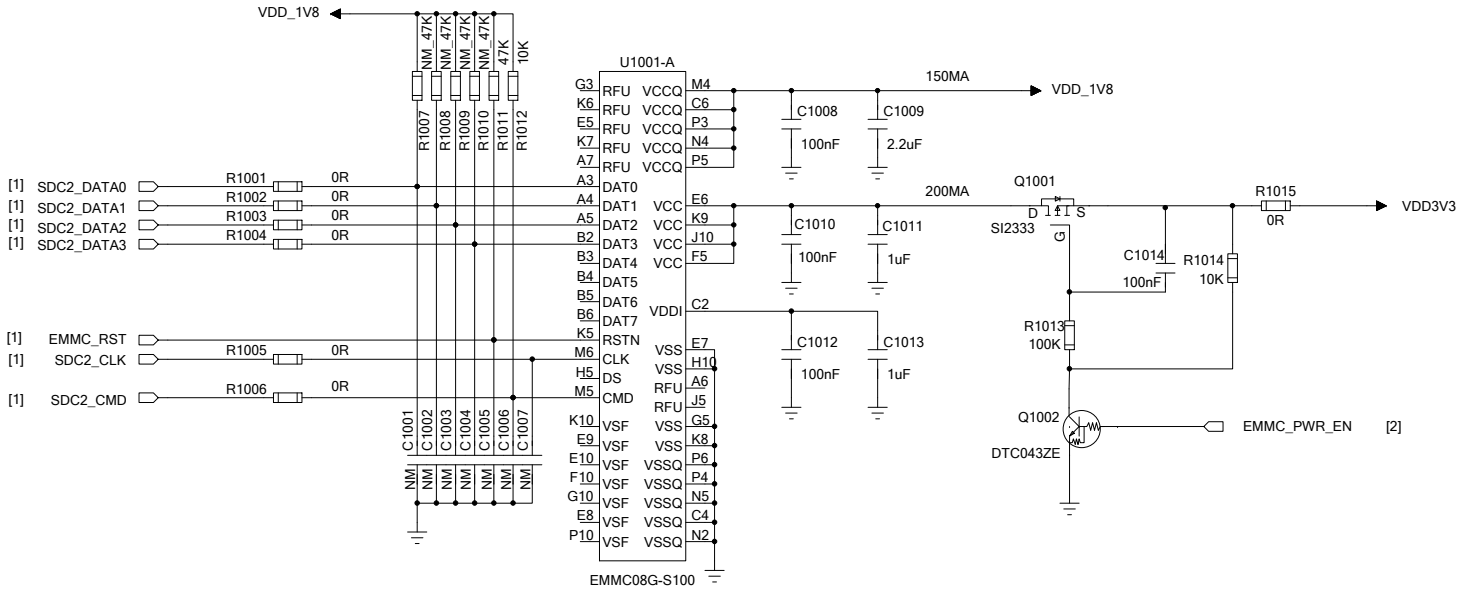
eMMC Design





Notes:

1. AG35-Quecopen supports the following eMMC models: eMMC08G-S100, SDINBDG4-8G-I and MTFC4GMDEA-4M IT.
2. Typical value of power filter capacitors:

Model	C1008	C1009	C1010	C1011	C1012	C1013
eMMC08G-S100	100nF	2.2uF	100nF	1uF	100nF	1uF
SDINBDG4-8G-I	100nF	4.7uF	100nF	4.7uF	100nF	1uF
MTFC4GMDEA-4M IT	100nF	2.2uF	100nF	2.2uF	100nF	1uF

3. For more details, please refer to the datasheet of eMMC devices.
4. SDIO2 interface of AG35-Quecopen supports both SD card and eMMC, but the two functions cannot be used synchronously. Customers can select SD card or eMMC according to application demands.

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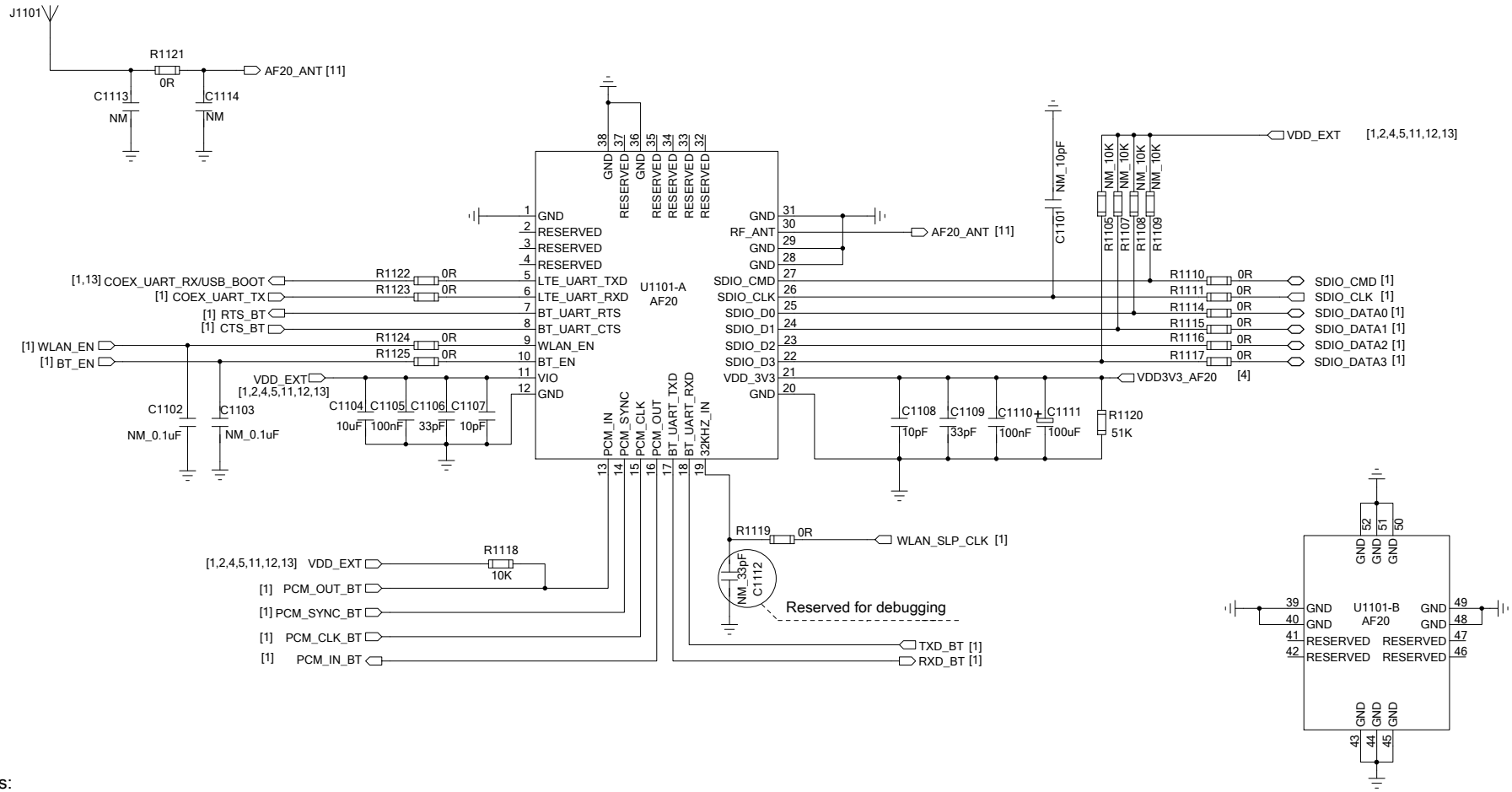
AF20 Design

AF20 Antenna Circuit



Notes:

1. Keep all RESERVED and unused pins unconnected.
2. The impedance of the SDIO data signal traces must be controlled as 50Ω when routing.
3. SDIO data lines should be shielded by ground; SDIO_CMD and SDIO_CLK signal lines should be shielded by ground seperately.
4. It is recommended to use PI type AF20 antenna circuit, thus ensuring covenicent subsequent debugging.
5. The impedance of RF signal trace must be controlled as 50Ω when routing.

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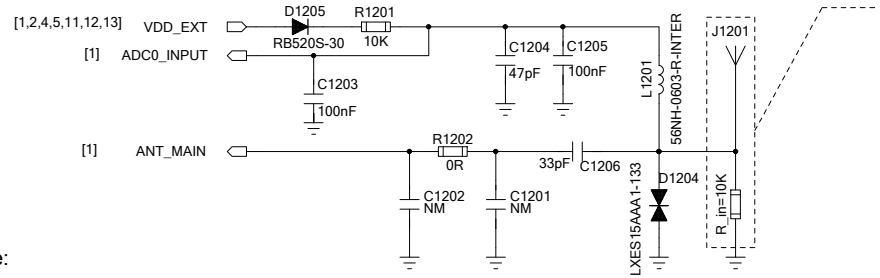
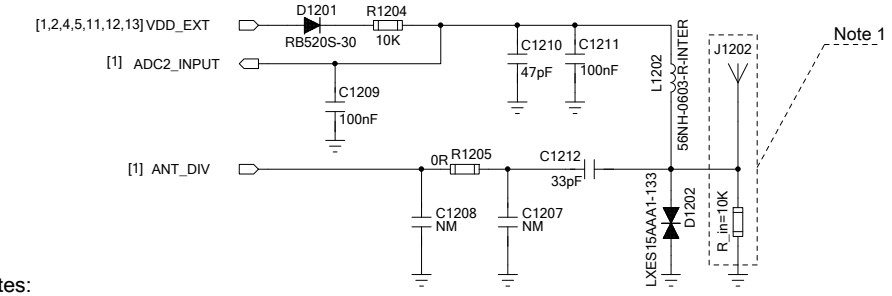
Antenna Interface and Antenna Detection Circuit Designs

Main Antenna Intreface and Detection Circuit (Normal)



Note:
In order to achieve successful antenna status detection, the main antenna is recommended to integrate an 8~13K resistor (R_in) to GND. And the typical value for the resistor is 10K.

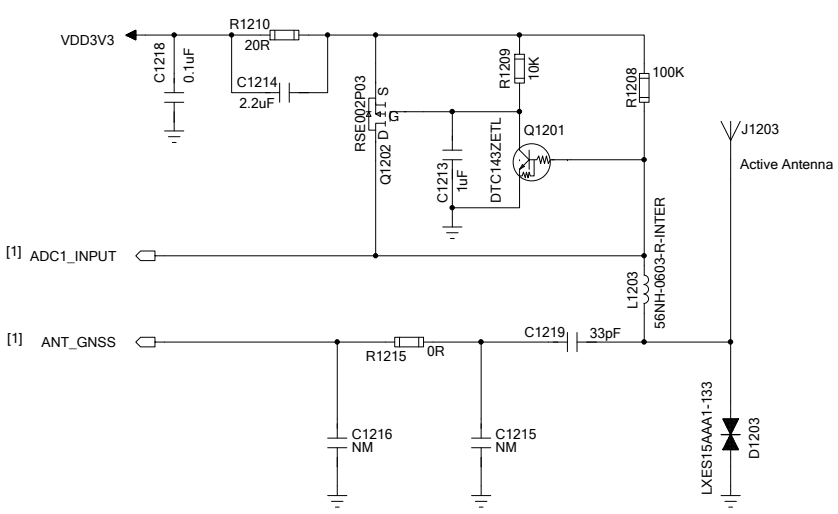
Rx-diversity Antenna Interface and Detection Circuit (Normal)



Notes:
1. In order to achieve successful antenna status detection, the Rx-diversity antenna is recommended to integrate an 8~13K resistor (R_in) to GND. And the typical value for the resistor is 10K.
2. The Rx-diversity reception function is ON by default. If Rx-diversity antenna is not used, there is a need to use AT command to turn off Rx-diversity reception.

Main / Rx-diversity Antenna Status Indication					
Antenna Status	Open	R_in=8K	R_in=10K	R_in=13K	Short to GND
ADC Value	1.7V	0.7V	0.8V	0.9V	0V
Status Indication	Open	Normal	Normal	Normal	Short to GND

GNSS Antenna Interface and Detection Circuit (Normal)



GNSS Antenna Status Indication			
Antenna Status	Open	Normal	Short to GND
ADC Value	VDD_3V3	VDD_3V3-R1210*I_GNSS	0V

Notes:
1. A low power active antenna is recommended to be selected. If passive antenna is used, then R1210 and L1203 are not needed.
2. An external LDO can be selected to supply power for active antenna.
3. VDD_3V3 is the power supply for active antenna, and I_GNSS is the working current of active antenna.
4. The active antenna power supply shall not exceed VBAT voltage of the module. And ADC0 or ADC1 shall be selected for ADC value detection.

Notes:
1. It is recommended to use PI type Main/Rx-diversity antenna circuit, thus ensuring covenicent subsequent debugging.
2. The impedance of the RF signal traces must be controlled as 50Ω when routing.
3. ADC value can be read by AT+QADC=<port> or API ql_adc_show. For more details, please refer to *Quectel_AG35_AT_Commands_Manual* or *Quectel_AG35-Quecopen_Developer_Guide.*
4. Three kinds of antenna status are designed to be detected: Normal, Short to GND and Open.
5. The antenna connection status is judged by the ADC feedback value.

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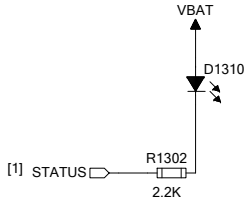
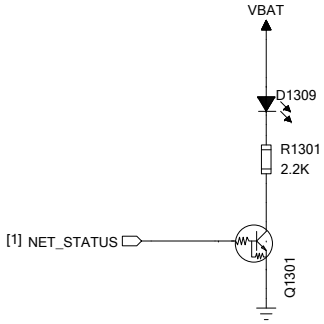
Indicators and Test Points

Indicators

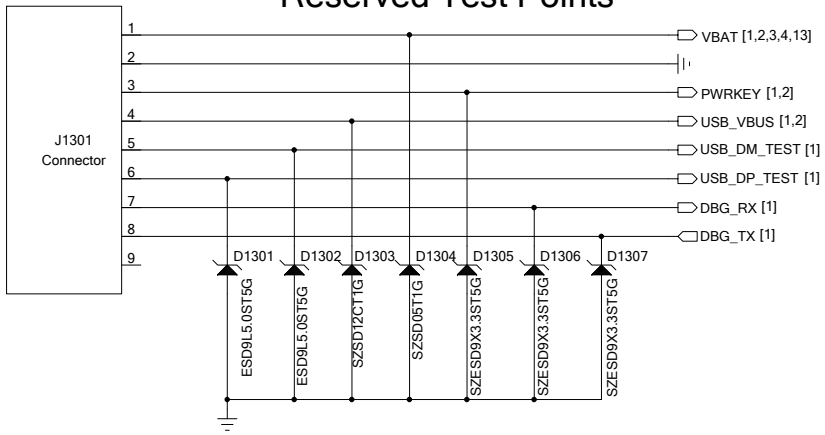




Notes:

1. The STATUS is an open drain output pin, and its drive current is less than 0.9mA.
2. For more details about STATUS and NET_STATUS, please refer to *Quectel_AG35-Quecopen_Hardware_Design*.
3. If the current consumption is required as low as possible when the device is in sleep, replace the power supply of indicators with a controllable one. Turn off the power when the module enters into sleep mode.

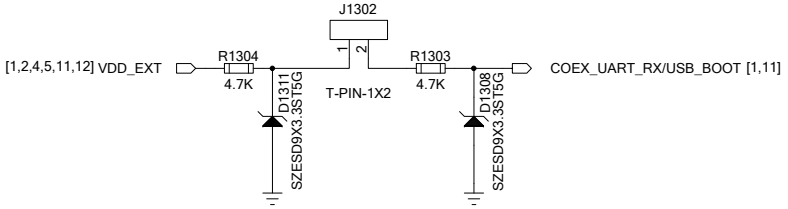
Reserved Test Points



Notes:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.
   Junction capacitance of ESD protection devices on USB data lines might influence the signal, please pay attention to it. Typically, the capacitance should be less than 1pF.
4. The debug interface supports 1.8V power domain.
   A level translator should be used if the power domain of customers' application is 3.3V.

USB_BOOT for Download



Note:
COEX_UART_RX/USB_BOOT is kept open by default and the module will be forced into download mode quickly when COEX_UART_RX/USB_BOOT is at high level.

Quectel Wireless Solutions		
DRAWN BY Canice CHEN	PROJECT AG35-Quecopen	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER A
	SHEET 13 OF 13	DATE 2018/6/5