EC2x Series QuecOpen Module Startup Reason Identification

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2020-05-22	Javen SHEN	Creation of the document
1.0	2021-01-05	Javen SHEN	First official release

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1 Introduction

Quectel EC2x series supports QuecOpen® solution. QuecOpen® is an open-source embedded development platform based on the Linux system, which is intended to simplify the design and development of IoT applications. For more information on QuecOpen®, see ***document [1]***.

This document describes the startup methods supported by EC2x series in QuecOpen® solution and the software methods available to identify the startup (power on, reset, etc.) reasons. It also introduces basic hardware designs relating to the module's startup, including the hardware design block diagram and the SMPL mechanism of PMIC.

1.1. Applicable Modules

Table 1: Applicable Modules

Module Series	Module
EC2x series	EC25 series
	EC21 series
	EC20 R2.1

2 Hardware Design Block Diagram

2.1. Block Diagram of the Module

The following is the hardware design block diagram of EC2x series in QuecOpen solution.

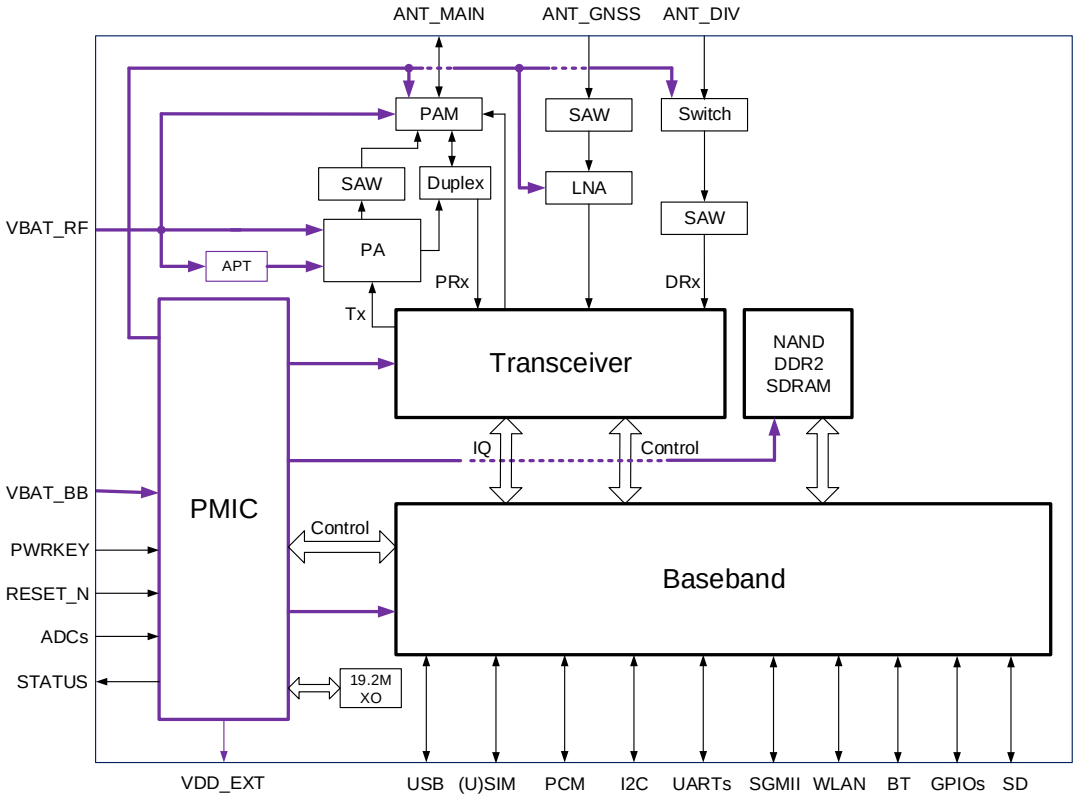


Figure 1: Block Diagram of EC2x Series QuecOpen® Module

In the block diagram above, the PWRKEY, RESET_N and SHDN_N pins are correlated with power-on/off of the module, and these pins are routed out from the PMIC. See ***Table 1*** for details.

2.2. Block Diagram of the PMIC

The figure below is the hardware design block diagram of PMIC. It only illustrates the parts that correlates with the power-on/off of the module.

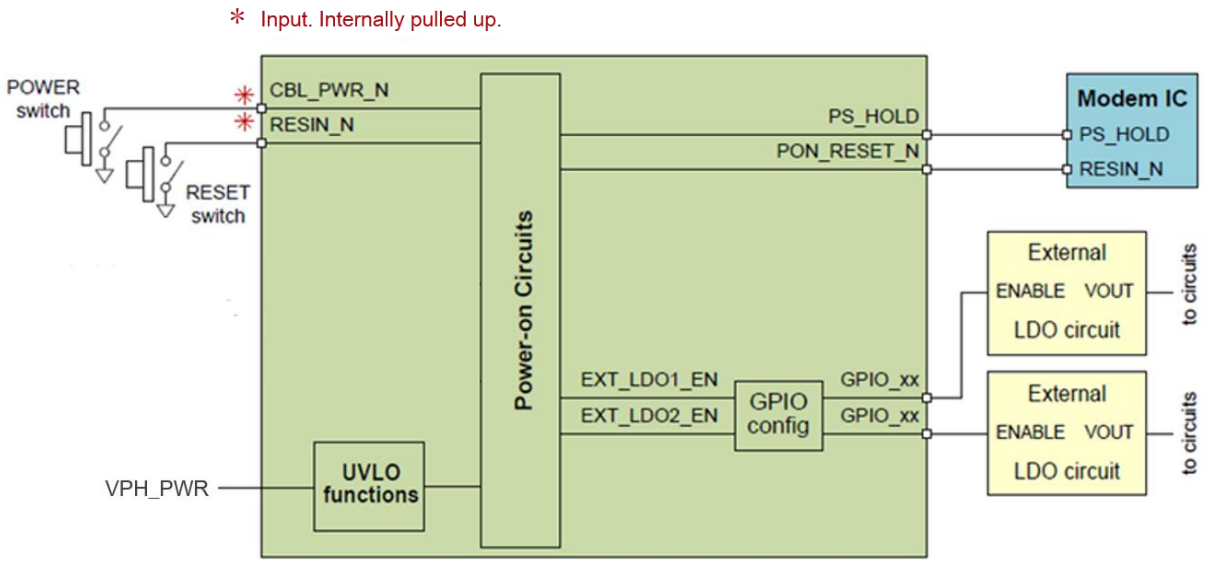


Figure 2: Block Diagram of PMIC (Partial)

NOTE

VPH_PWR is powered by VBAT_BB of the module, and connects to the PMIC's VDD pin inside the module. Through the built-in UVLO/SMPL circuits, VPH_PWR supplies power to the PMIC.

Table 2: Power-on/off Correlated Module Pins and Corresponding PMIC Pins

Power-on/off Correlated Module Pins			Corresponding PMIC Pins	
Pin Name	**I/O**	**Pin Description**	**Pin Name**	**Pin Description**
PWRKEY	DI	Power on/off the module	CBL_PWR_N	For power supply control. Internally pulled up by default. Low active.
RESET_N	DI	Reset the module	RESIN_N	For reset control. Internally pulled up by default. Low active.
SHDN_N	DI	Emergency shutdown of the module	PS_HOLD	Power supply hold-up signal. HIGH: the power supply is normal (the module is powered on.

	LOW: the power supply is disconnected (the module powers off).

3 Module Startup Methods

This chapter introduces the common methods to start up the module.

3.1. Methods to Start up the Module

Table 3: Common Methods to Start up the Module

SN.	Startup Method	Description	Remark
1	Hardware power-on	Drive PWRKEY low for at least 500 ms to power on the module.	
2	Hardware reset	Drive RESET_N low for 150–460 ms to reset the module.	
3	Software reboot	Run a software command such as **reboot** or an API function such as *QL_Powerdown(1)* to stop software processes and realize safe restart of the module.	
4	RTC timer startup	After the register of the internal RTC timer is enabled, the module starts up automatically when the timer expires.	For details about how to enable the RTC registers, see the example in the SDK path below: *ql-ol-sdk/ql-ol-extsdk/example/posix_timer/example_timer.c*.
5	SMPL mechanism	When the module's VBAT_BB drops down to a specified level (approx. 1.4 V), and then returns to the normal range within 0.5 s, the SMPL mechanism triggers the module to restart automatically.	See ***Chapter 3.2*** for details.

3.2. SMPL Mechanism

SMPL is a hardware mechanism of the module's PMIC, and is enabled by default.

The PMIC SMPL feature initiates a power-on sequence if the monitored VBAT_BB (PMIC's VDD) drops out of range (for example when a UVLO event is detected) and then returns in-range within 0.5 s. SMPL achieves immediate and automatic recovery from momentary power loss.

Operation details:

- A UVLO event drives low the PMIC's PON_RST_N, which resets PMIC and makes the module power off.
- If the VBAT_BB (PMIC's VDD) returns in-range within 0.5 s, the module starts up automatically without any additional software operation.
- If the VBAT_BB (PMIC's VDD) cannot return in-range within 0.5 s, the module powers off. In such a case, it has to be powered on with PWRKEY.

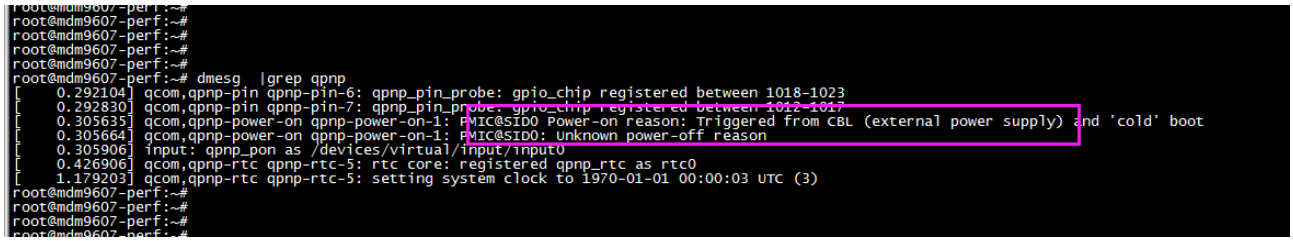
4 Identify Module Startup Reasons

This chapter introduces how to identify the startup reasons of EC2x series in QuecOpen solution.

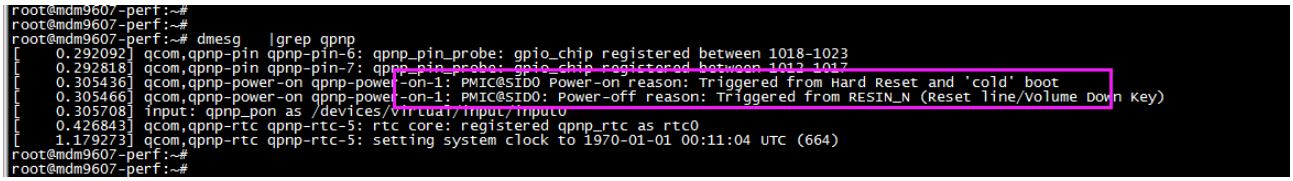
4.1. Through Kernel Logs

The “Power-on reason” in Kernel logs indicates the startup reason of the module. Run the command **dmesg |grep qpn** to view the Kernel logs.

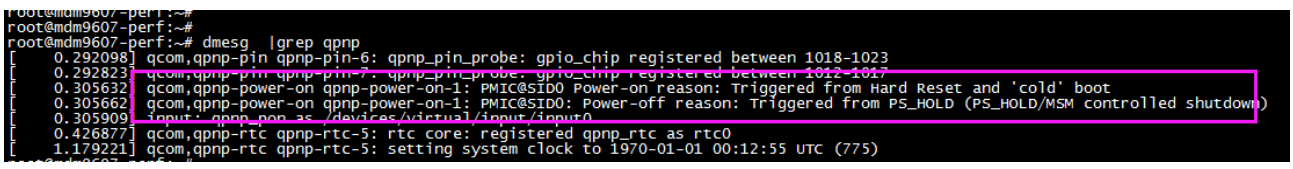
1. The “Power-on reason” shown as below indicates that the module is powered on through the PWRKEY pin.



2. The “Power-on reason” shown as below indicates that the module starts up because of RESET_N operation.



3. The “Power-on reason” shown as below indicates that the module starts up because of software restart operation.



4. The “Power-on reason” shown as below indicates that the module starts up because of RTC timer setting.

```
root@mdm9607-perf:~# dmesg | grep qpnp
[    0.302087] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.302820] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.315817] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from RTC (RTC alarm expiry) and 'cold' boot
[    0.315847] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0: Power-off reason: Triggered from PS_HOLD (PS_HOLD/MSM controlled shutdown)
[    0.316051] input: qpnp_pon as /devices/virtual/input/input0
[    0.438329] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.391699] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:20:54 UTC (1254)
root@mdm9607-perf:~#
```

5. The “Power-on reason” shown as below indicates that the module starts up based on SMPL mechanism.

```
root@mdm9607-perf:~#
root@mdm9607-perf:~# dmesg  |grep qpnp
[    0.292096] qcom,qpnp-pin qpnp-pin-6: qpnp_pin_probe: gpio_chip registered between 1018-1023
[    0.302816] qcom,qpnp-pin qpnp-pin-7: qpnp_pin_probe: gpio_chip registered between 1012-1017
[    0.305457] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0 Power-on reason: Triggered from SMPL (sudden momentary power loss) and 'cold' boot
[    0.305487] qcom,qpnp-power-on qpnp-power-on-1: PMIC@SID0: Power-off reason: Triggered from UVLO (Under Voltage Lock Out)
[    0.305736] input: qpnp_pon as /devices/virtual/input/input0
[    0.426843] qcom,qpnp-rtc qpnp-rtc-5: rtc core: registered qpnp_rtc as rtc0
[    1.178799] qcom,qpnp-rtc qpnp-rtc-5: setting system clock to 1970-01-01 00:02:16 UTC (136)
root@mdm9607-perf:~#
```

NOTES

1. If you cannot find the “Power-on reason” in the Kernel log, check and confirm whether the valid dmesg logs have been cleared because of too many irrelevant logs are printed.
2. The “Power-off reason” in the Kernel log indicates the latest power-off reason of the module.

4.2. Through a Command in User Layer

Run the command **cat /proc/sys/kernel/boot_reason** in user layer to query the startup reason. Different return values indicate different startup reasons:

Return Value:

1	The module is reset (hardware reset) or restarted with a command or an API (software reboot).
2	The module restarts based on the SMPL mechanism.
3	The module powers on according to the RTC timer setting.
7	The module is powered on through using the PWRKEY pin.

In the example below, the command returns 7 which indicates the module is powered on through using the PWRKEY pin.

```
root@mdm9607-perf:/proc/sys/kernel# cat boot_reason
7
root@mdm9607-perf:/proc/sys/kernel#
```

4.3. Through Reading PMIC Information in User Layer

The PON_PON_REASON1 register of PMIC is read-only, and is used to store the module's startup reasons (that is, PMIC's startup reasons). The slave address is 0x808, and you can read the register information to identify the startup reasons.

```
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0# echo 0x808 > address
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0# cat data
00800 -- -- -- -- -- -- -- 01
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0#
root@mdm9607-perf:/sys/kernel/debug/spmi/spmi-0#
```

The meaning of each bit of 0x808 represents:

Table 4: Bit Information

Bit	Name	Description
7	KPDPWR_N	Read only. Trigger the module to start up through KPDPWR. (Not supported.) 1: TRIGGER_RECEIVED
6	CBLPWR_N	Read only. Trigger the module to start up through PMIC's CBL_PWR_N (or the module's PWRKEY pin). 1: TRIGGER_RECEIVED
5	PON1	Read only. Trigger the module to start up through PON1. (Not supported.) 1: TRIGGER_RECEIVED
4	USB_CHG	Read only. Trigger the module to start up through USB charger. (Not supported.) 1: TRIGGER_RECEIVED
3	DC_CHG	Read only. Trigger the module to start up through DC charger. (Not supported.) 1: TRIGGER_RECEIVED
2	RTC	Read only. Trigger the module to start up through RTC timer. 1: TRIGGER_RECEIVED
1	SMPL	Read only. Trigger the module to start up through SMPL mechanism. 1: TRIGGER_RECEIVED
0	HARD_RESET	Read only. Trigger the module to start up through a hardware reset event (check power-on reason).

1: TRIGGER_RECEIVED

NOTE

If you cannot identify the module's startup reasons through any of the methods listed in Chapter, contact Quectel Technical Support (support@quectel.com) to get supports.

5 Appendix A References

Table 5: Related Document

SN	Document Name	Description
[1]	Quectel_EC2x_Series_QuecOpen_Quick_Start_Guide	Quick start guide for QuecOpen solution of EC25 series, EC21 series and EC20 R2.1 modules

Table 6: Terms and Abbreviations

Abbreviation	Description
API	Application Programming Interface
DC	Direct Current
IC	Integrated Circuit
IoT	Internet of Things
PMIC	Power Management IC
RTC	Real-Time Clock
SDK	Software Development Kit
SMPL	Sudden Momentary Power Loss
USB	Universal Serial Bus
UVLO	Under-Voltage Lockout