AG35-CEN-Quecopen Hardware Design

LTE Standard Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2018-03-19	Eden LIU/ Dominic GONG/ Jun WU	Initial
2.0	2019-04-30	Canice CHEN/ Dominic GONG	Numerous changes have been made to this document, so it is recommended to read it in its entirety.
2.1	2019-05-20	Eden LIU	Corrected some pin names in the pin assignment figure (Figure 2).

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1 Introduction

This document defines the AG35-CEN-Quecopen module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application note and user guide, customers can use AG35-CEN-Quecopen module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating AG35-CEN-Quecopen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals, clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

Quecopen® is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of Quecopen® solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With Quecopen® solution, development flow for wireless application and hardware design will be simplified. Main features of Quecopen® solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware wirelessly
- Improves products' cost-performance ratio, and enhances products' competitiveness

AG35-CEN-Quecopen module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.3GHz. Customers can use AG35-CEN-Quecopen modules as the basis for development of Quecopen® applications.

AG35-CEN-Quecopen is a series of LTE-FDD/LTE-TDD/WCDMA/TD-SCDMA/EVDO/CDMA/GSM wireless communication module with receive diversity, and provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, TD-SCDMA, EVDO, CDMA, EDGE and GPRS networks. It also provides GNSS and voice functionalities to meet customers' specific application demands.

With a compact profile of 33.0mm × 37.5mm × 3.0mm, AG35-CEN-Quecopen can meet almost all requirements for industrial application. It is an SMD type module which can be embedded into applications through its 299-pin LGA pads.

The following table shows the frequency bands and GNSS function of the module.

Table 1: Frequency Bands and GNSS Function of AG35-CEN-Quecopen Module

Network Type	AG35-CEN-Quecopen
LTE-FDD (with Rx-diversity)	B1/B3/B5/B8
LTE-TDD (with Rx-diversity)	B34/B38/B39/B40/B41
WCDMA (with Rx-diversity)	B1/B8
TD-SCDMA	B34/B39
EVDO/CDMA	BC0
GSM	900/1800MHz
GNSS	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

2.2. Key Features

The following table describes the detailed features of AG35-CEN-Quecopen module.

Table 2: Key Features of AG35-CEN-Quecopen Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+2/-1dB) for EVDO/CDMA BC0 Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 4 LTE FDD and TDD Support 1.4 to 20MHz RF bandwidth Support Multiuser MIMO in DL direction ● FDD: Max 150Mbps (DL)/50Mbps (UL) ● TDD: Max 130Mbps (DL)/30Mbps (UL)

UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA Support QPSK, 16-QAM and 64-QAM modulation ● DC-HSDPA: Max 42Mbps (DL) ● HSUPA: Max 5.76Mbps (UL) ● WCDMA: Max 384Kbps (DL)/384Kbps (UL)
TD-SCDMA Features	Support CCSA Release 3 TD-SCDMA ● Max 4.2Mbps (DL)/2.2Mbps (UL)
CDMA2000 Features	Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A ● EVDO: Max 3.1Mbps (DL)/1.8Mbps (UL) ● 1X Advanced: Max 307.2Kbps (DL)/307.2Kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL)/85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL)/236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS/SMTP/MMS/FTPS/SMTPS/SSL protocols Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
SMS	Text and PDU modes Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support two digital audio interfaces: PCM interface (one of them multiplexed from SPI interface) GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization

USB Interface	Compliant with USB 2.0 specification (slave mode by default, support USB HOST) and the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging and firmware upgrade **USB Driver:** Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.x/7.x/8.x/9.x
HSIC Interface*	High-speed inter-chip USB electrical specification.
UART Interfaces	**UART1:** Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **UART2:** Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **UART3 (Multiplexed from SPI):** Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **UART4 (Multiplexed from SDIO1):** Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **UART5 (Multiplexed from SDIO1):** Max baud rate reach up to 115200bps **Debug UART:** Used for Linux console and log output, 115200bps baud rate
SDIO Interfaces	**SDIO1:** Compliant with SD 3.0 protocol Used for WLAN function **SDIO2:** Compliant with SD 3.0 protocol Support eMMC and SD card
SPI Interfaces	Support three SPI interfaces SPI2 and SPI3 multiplexed from UART1 and UART2, respectively Support master mode only Maximum clock frequency rate: 50MHz for SPI1/SPI3, 38MHz for SPI2
I2C Interfaces	**I2C1:** Compliant with I2C specification version 5.0 Multi-master is not supported Used for codec configuration by default **I2C2:** Compliant with I2C specification version 5.0 Multi-master is not supported
SGMII Interface	Support half/full duplex for 10/100/1000Mbps
Wireless Connectivity	**WLAN：**

Interfaces	● Compliance with IEEE 802.11 Standard ● Correspond with the SDIO 3.0 specification
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C-Lite of Qualcomm Protocol: NMEA 0183 Data update rate: 1Hz by default and maximally up to 10Hz
AT Commands	3GPP TS 27.007/3GPP TS 27.005 AT commands and Quectel enhanced AT commands
Network Indication	NET_STATUS is used to indicate network connectivity status
Antenna Interfaces	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (33.0±0.15)mm × (37.5±0.15)mm × (3.0±0.2)mm Weight: approx. 8.1g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of AG35-CEN-Quecopen and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash

- Radio frequency
- Peripheral interfaces

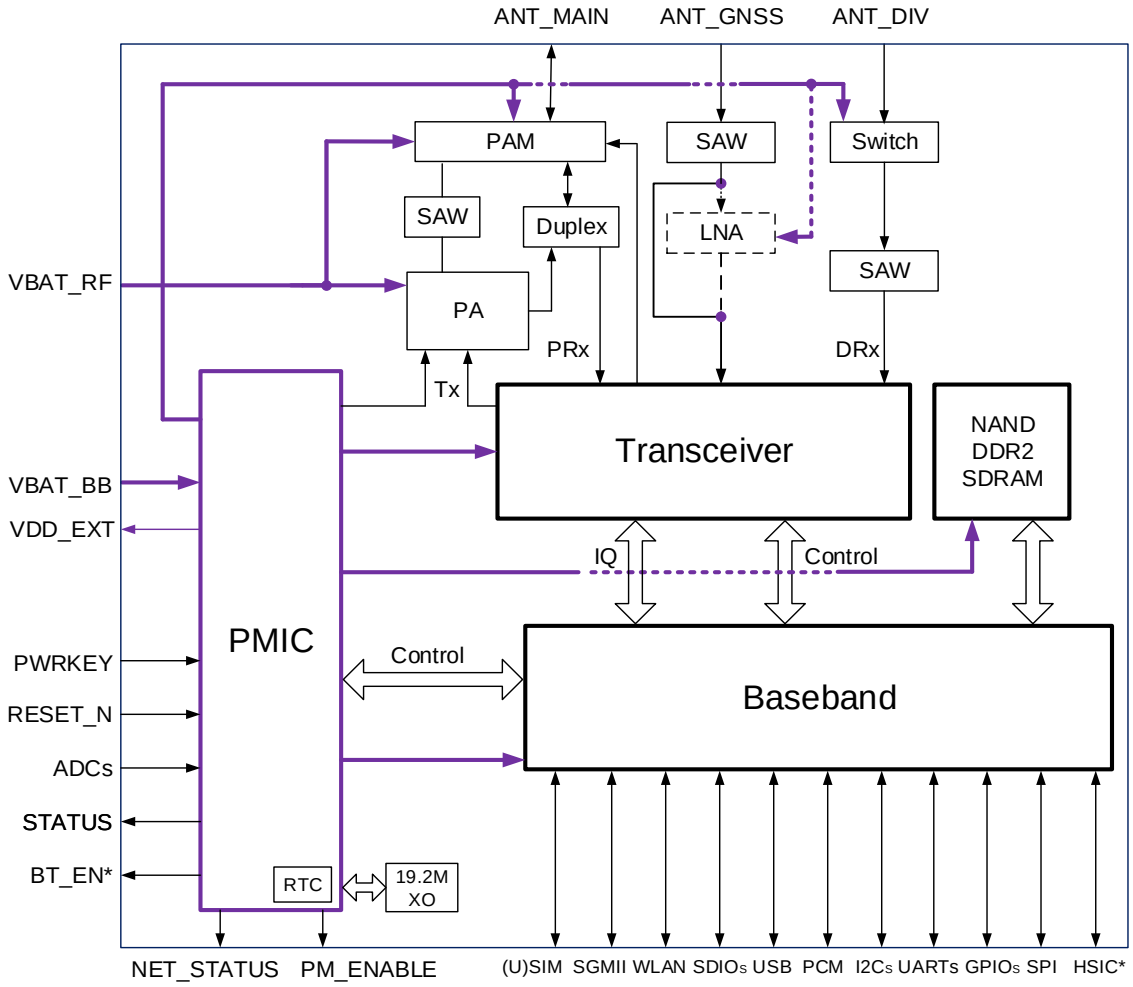


Figure 1: Functional Diagram

NOTE

"*" means under development.

2.4. Evaluation Board

In order to help customers develop applications conveniently with AG35-CEN-Quecopen module, Quectel supplies the evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

AG35-CEN-Quecopen is equipped with 299-pin LGA pads that can be connected to cellular application platform. Sub-interfaces included in these pads are described in detail in the following sub-chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SDIO interfaces
- SPI interfaces
- SGMII interface
- Wireless connectivity interfaces
- ADC interfaces
- Status indication interfaces
- USB_BOOT interface
- HSIC interface*

NOTE

"*" means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of AG35-CEN-Quecopen module.

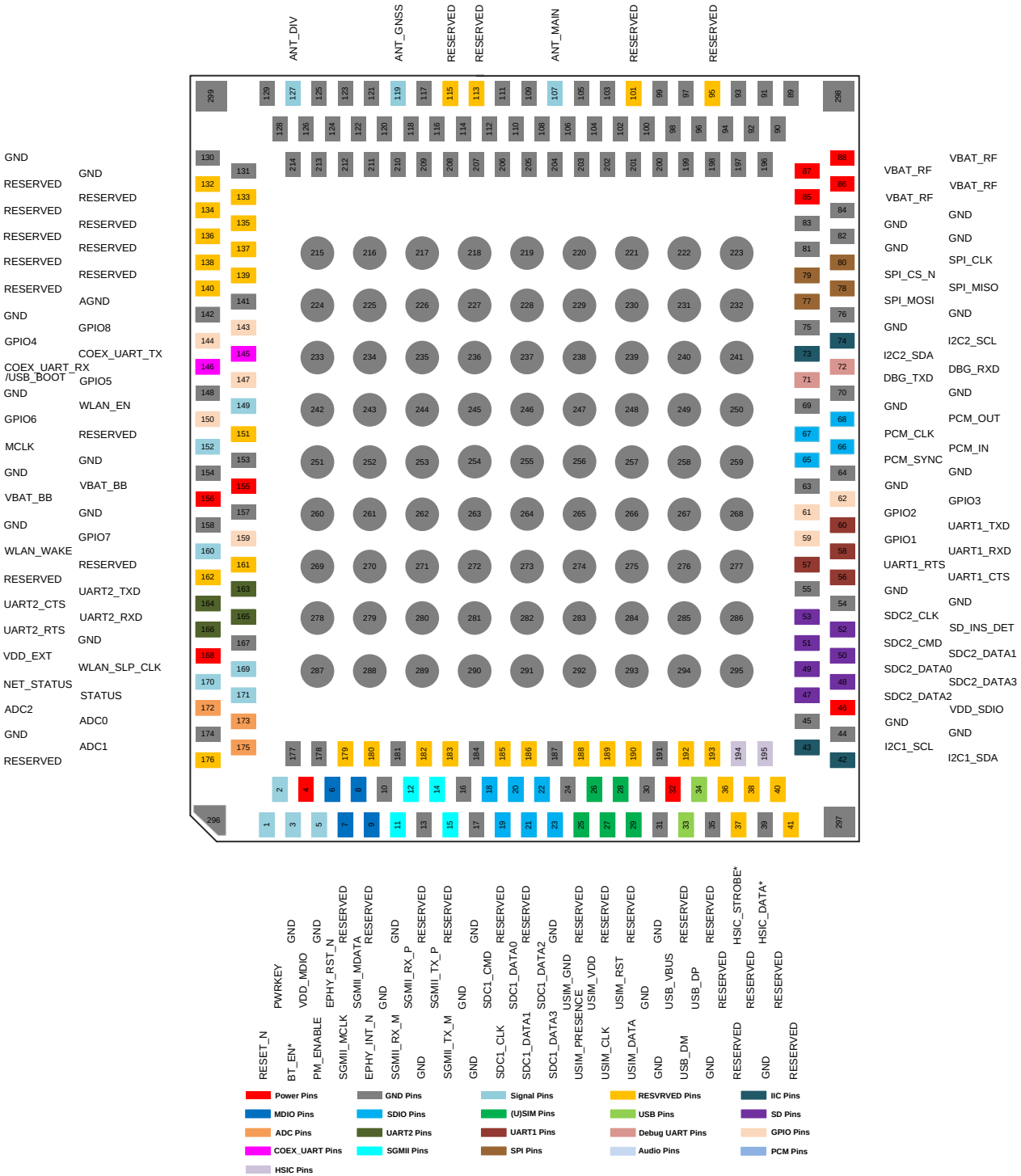


Figure 2: Pin Assignment (Top View)

NOTES

1. Pins 59, 65, 67, 144~147, 149 and 159 cannot be pulled up before power-up. Pin 80 cannot be pulled down before power-up.
2. PWRKEY (pin 2) output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. GND pins 215~299 should be connected to ground in the design.
4. Keep all RESERVED pins and unused pins unconnected.
5. "*" means under development.

3.3. Pin Description

The following tables show the pin definition of AG35-CEN-Quecopen module, as well as the alternate functions of multiplexing pins.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
BH	High-voltage tolerant bidirectional digital with CMOS input
DI	Digital input
DO	Digital output
H	High level
IO	Bidirectional
L	Low level
OC	Open collector
OD	Open drain
PD	Pull-down
PI	Power input
PO	Power output

PU	Pull-up
NP	No pull-up/down

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155, 156	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	85, 86, 87, 88	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a transmitting burst.
VDD_EXT	168	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
GND	10, 13, 16, 17, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89~94, 96~100, 102~106, 108~112, 114, 116~118, 120~126, 128~131, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191,		Ground.		

	196~299				
AGND	141		Analog ground		If unused, keep it open.
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	2	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	1	DI	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pulled up to 1.8V internally. Active low.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	24		Specified ground for (U)SIM card		
USIM_ PRESENCE	25	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USIM_VDD	26	PO	Power supply for (U)SIM card	**For 1.8V (U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V (U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3V is supported by the module automatically.
USIM_CLK	27	DO	Clock signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	28	DO	Reset signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:**	

				V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_DATA	29	IO	Data signal of (U)SIM card	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	PI	USB connection detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	Maximum current: 1mA
USB_DM	33	IO	USB differential data bus (-)		Compliant with USB 2.0 standard specification. Require differential impedance of 90Ω.
USB_DP	34	IO	USB differential data bus (+)		
HSIC Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HSIC_ STROBE*	194	IO	High speed inter chip interface - strobe	V_{IL}max=0.40V V_{IH}min=0.80V V_{OL}max=0.30V V_{OH}min=0.90V	1.2V power domain. If unused, keep them open.
HSIC_ DATA*	195	IO	High speed inter chip interface - data		
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	171	OD	Indicate the module's operating status	The drive current should be less than 0.15mA.	Require external pull-up. If unused, keep it open.
NET_ STATUS	170	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
UART1 Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
UART1_CTS	56	DO	DTE clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
UART1_RTS	57	DI	DTE request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
UART1_RXD	58	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
UART1_TXD	60	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
UART2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_TXD	163	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
UART2_CTS	164	DO	DTE clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
UART2_RXD	165	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
UART2_RTS	166	DI	DTE request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	71	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	72	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V	1.8V power domain. If unused, keep it open.

				V_{IH}max=2.0V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	175	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC2	172	AI	General purpose analog to digital converter interface	Voltage range: 0.1V to 1.7V	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	65	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_IN	66	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_CLK	67	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MCLK	152	DO	Main clock	V_{OL}max=0.45V V_{OH}min=1.35V	Output 12.288MHz. If unused, keep it open.
I2C1 Interface (for Codec Configuration by Default)					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C1_SDA	42	IO	I2C serial data	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C1_SCL	43	DO	I2C serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C2_SDA [1)]	73	IO	I2C serial data	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C2_SCL	74	DO	I2C serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	External pull-up resistor is required. 1.8V only. If unused, keep it open.
SDIO2 Interface (for eMMC & SD Card)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_SDIO	46	PO	**SD card application**: SDIO pull-up power source. **eMMC application**: Keep it open when used for eMMC.	$I_O$max=50mA	1.8V/2.85V configurable power output. Cannot be used as power supply for SD card. If unused, keep it open.
SDC2_DATA2	47	IO	SDIO data signal (bit 2)	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V	SDIO signal level can be selected according to the one supported by SD card. 1.8V power domain for eMMC. Please refer to SD
SDC2_DATA3	48	IO	SDIO data signal (bit 3)		
SDC2_DATA0	49	IO	SDIO data signal (bit 0)		
SDC2_DATA1	50	IO	SDIO data signal (bit 1)		

SDC2_CMD	51	IO	SDIO command signal	**For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	3.0 protocol for more details. If unused, keep it open.
SD_INS_DET	52	DI/DO	**DI:** Insertion detection for SD card **DO:** Reset eMMC	V_{IL}min=-0.3V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open. Currently eMMC resetting is not supported.
SDC2_CLK	53	DO	SDIO clock signal	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V	SDIO signal level can be selected according to the one supported by SD card. 1.8V power domain for eMMC. Please refer to SD 3.0 protocol for more details. If unused, keep it open.

SPI Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_MOSI	77	DO	SPI master out slave in	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MISO	78	DI	SPI master in slave out	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SPI_CS_N	79	DO	SPI chip select	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_CLK	80	DO	SPI serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.

MDIO Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment

VDD_MDIO	4	PO	SGMII_MDATA pull-up power source		1.8V/2.85V configurable output power supply. If unused, keep it open.
EPHY_RST_N	6	DO	Ethernet PHY reset	**1.8V:** V_{OL}max=0.45V V_{OH}min=1.35V **2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MCLK	7	DO	SGMII MDIO (Management Data Input/Output) clock	**1.8V:** V_{OL}max=0.45V V_{OH}min=1.35V **2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MDATA	8	IO	SGMII MDIO (Management Data Input/Output) data	**1.8V:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.85V:** V_{IL}max=0.71V V_{IH}min=1.78V V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. Should be externally pulled up to VDD_MDIO. If unused, keep it open.
EPHY_INT_N	9	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SGMII_RX_M	11	AI	SGMII receiving (-)		If unused, keep it open.
SGMII_RX_P	12	AI	SGMII receiving (+)		If unused, keep it open.
SGMII_TX_P	14	AO	SGMII transmission (+)		If unused, keep it open.
SGMII_TX_M	15	AO	SGMII transmission (-)		If unused, keep it open.

WLAN Interface (SDIO1 and WLAN Control Interfaces)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	169	DO	WLAN sleep clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PM_ENABLE	5	DO	External power enable control for WLAN	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. If unused, keep it open.
SDC1_CMD	18	IO	WLAN SDIO command signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SDC1_CLK	19	DO	WLAN SDIO clock signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SDC1_DATA0	20	IO	WLAN SDIO data bus (bit 0)	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA1	21	IO	WLAN SDIO data bus (bit 1)		
SDC1_DATA2	22	IO	WLAN SDIO data bus (bit 2)		
SDC1_DATA3	23	IO	WLAN SDIO data bus (bit 3)		
WLAN_WAKE	160	DI	Wake up module via WLAN	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active low. If unused, keep it open.
WLAN_EN	149	DO	WLAN function enable control via Wi-Fi module	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. If unused, keep it open.
COEX_UART_RX/USB_BOOT	146 [2]	DI	LTE/WLAN & BT coexistence signal./ Force the module to enter into emergency download mode.	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
COEX_UART_TX	145 [2]	DO	LTE/WLAN & BT coexistence signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RF Interface					

Pin Name	Pin No.	I/O	Description	Characteristics	Comment
ANT_MAIN	107	IO	Main antenna interface		50Ω impedance.
ANT_GNSS	119	AI	GNSS antenna interface		50Ω impedance. If unused, keep it open.
ANT_DIV	127	AI	Diversity antenna interface		50Ω impedance. If unused, keep it open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	59 [2]	IO	General purpose input/output interface	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
GPIO2	61	IO			
GPIO3	62	IO			
GPIO4	144 [2]	IO			
GPIO5	147 [2]	IO			
GPIO6	150	IO			
GPIO7	159 [2]	IO			
GPIO8	143 [3]	IO			
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_EN*	3	DO	Bluetooth enable control	V_{OL}max=0.45V V_{OH}min=1.35V	The function is still under development.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	36~38, 40, 41, 95, 101, 113, 115, 132~140, 151, 161, 162, 176, 179, 180,		Reserved		Keep these pins open.

	182, 183, 185, 186, 188~190, 192, 193

NOTES

1. [1] Pin 73 (I2C2_SDA) has high-voltage level pulse during power-up of the module, and it is recommended to configure it as input when it is used as GPIO.
2. [2] Pins 59, 144~147 and 159 must be at low level before the module powers up successfully.
3. [3] It is recommended to configure pin 143 (GPIO8) as input, and in such case, it should be pulled up/down externally and configured as NP (No pull-up/down) internally.
4. Pin 80 cannot be pulled down before power-up.
5. Keep all RESERVED pins and unused pins unconnected.
6. "*" means under development.

The following table lists the multiplexing pins and their respective alternate functions of AG35-CEN-Quecopen.

Table 5: Alternate Functions of Multiplexing Pins

Pin Name	Pin No.	Model 1 (Default)	Model 2	Model 3	Model 4	Reset [1)]	Status in Booting	Interrupt [2)]	Remark
GPIO1	59	GPIO_38	--	--		B-PD,L	Low level	YES	BOOT_CONFIG_12
GPIO2	61	GPIO_75	--	--		B-PD,L	Low level	YES	
GPIO3	62	GPIO_74	--	--		B-PD,L	Low level	YES	
GPIO4	144	GPIO_25	--	--		B-PD,L	Low level	YES	BOOT_CONFIG_2
GPIO5	147	GPIO_24	--	--		B-PD,L	Low level	NO	BOOT_CONFIG_1
GPIO6	150	GPIO_42				B-PD,L	Low level	YES	Recommended to be “output”. Please refer to NOTE 2 for details.
GPIO7	159	GPIO_58				B-PD,L	Low level	NO	BOOT_CONFIG_11. Recommended to be “output”. Please refer to NOTE 2 for details.
GPIO8	143	GPIO_41		--		B-PD,L	Low level	NO	Recommended to be “output”. Please refer to NOTE 2 for details.
BT_EN* [3)]	3	BT_EN*	PMU_ GPIO_02	--		B-PD,L	Low level	NO	Must be “output” when used as GPIO.

PM_ENABLE [3]	5	PM_ENABLE	PMU_ GPIO_03	--		B-PD,L	Low level	NO	Must be “output” when used as GPIO.
SDC1_CMD	18	SDC1_CMD	GPIO_17	UART_RXD _BLSP4		B-PD,L	Low level	YES	
SDC1_CLK	19	SDC1_CLK	GPIO_16	UART_TXD _BLSP4		B-NP,L	Low level	YES	
SDC1_DATA0	20	SDC1_DATA0	GPIO_15	UART_CTS _BLSP1	SPI_CLK_ BLSP1	B-PD,L	Low level	NO	
SDC1_DATA1	21	SDC1_DATA1	GPIO_14	UART_RTS _BLSP1	SPI_CS_N _BLSP1	B-PD,L	Low level	NO	
SDC1_DATA2	22	SDC1_DATA2	GPIO_13	UART_RXD _BLSP1	SPI_MISO _BLSP1	B-PD,L	Low level	YES	
SDC1_DATA3	23	SDC1_DATA3	GPIO_12	UART_TXD _BLSP1	SPI_MOSI _BLSP1	B-PD,L	Low level	YES	
USIM_ PRESENCE	25	USIM_ PRESENCE	GPIO_34	--		B-PD,L	Low level	YES	
I2C1_SDA	42	I2C_SDA_ BLSP4	GPIO_18	--		B-PD,L	High level	NO	
I2C1_SCL	43	I2C_SCL_ BLSP4	GPIO_19	--		B-PD,L	High level	NO	
SDC2_INS_ DET	52	SDC2_INS_ DET	GPIO_26	--		B-PD,L	Low level	YES	
UART1_CTS	56	UART_CTS_ BLSP3	GPIO_3	SPI_CLK_B LSP3		B-PD,L	Low level	YES	
UART1_RTS	57	UART_RTS_ BLSP3	GPIO_2	SPI_CS_N_ BLSP3		B-PD,L	Low level	NO	

UART1_RXD	58	UART_RXD_BLSP3	GPIO_1	SPI_MISO_BLSP3		B-PD,L	Low level	YES	
UART1_TXD	60	UART_TXD_BLSP3	GPIO_0	SPI_MOSI_BLSP3		B-PD,L	Low level	NO	
PCM_SYNC	65	PCM_SYNC	GPIO_79	--		B-PD,L	Low level	YES	BOOT_CONFIG_7
PCM_IN	66	PCM_IN	GPIO_76	--		B-PD,L	Low level	YES	
PCM_CLK	67	PCM_CLK	GPIO_78	--		B-PD,L	Low level	NO	BOOT_CONFIG_8
PCM_OUT	68	PCM_OUT	GPIO_77	--		B-PD,L	Low level	NO	
I2C2_SDA	73	I2C_SDA_BLSP2	GPIO_6	--		B-PD,L	High pulse	NO	Recommended to be “input”. Please refer to NOTE 3 for details.
I2C2_SCL	74	I2C_SCL_BLSP2	GPIO_7	--		B-PD,L	Low level	NO	
SPI_MOSI	77	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6	PCM_1A_SYNC	B-PD,L	Low level	YES	
SPI_MISO	78	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6	PCM_1A_IN	B-PD,L	Low level	YES	
SPI_CS_N	79	SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6	PCM_1A_OUT	B-PD,L	Low level	YES	
SPI_CLK	80	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6	PCM_1A_CLK	B-PU,H	High level	NO	BOOT_CONFIG_4
WLAN_EN	149	WLAN_EN	GPIO_54	--		B-PD,L	Low level	NO	BOOT_CONFIG_6
UART2_TXD	163	UART_TXD_BLSP5	GPIO_8	SPI_MOSI_BLSP5		B-PD,L	Low level	YES	

UART2_CTS	164	UART_CTS_BLSP5	GPIO_11	SPI_CLK_BLSP5	B-PU,L	High level	YES	
UART2_RXD	165	UART_RXD_BLSP5	GPIO_9	SPI_MISO_BLSP5	B-PD,L	Low level	YES	
UART2_RTS	166	UART_RTS_BLSP5	GPIO_10	SPI_CS_N_BLSP5	B-PD,L	Low level	NO	
WLAN_SLP_CLK [3)]	169	WLAN_SLP_CLK	PMU_GPIO_06	--	B-PD,L	Low level	NO	Must be “output” when used as GPIO.
NET_STATUS [3)]	170	PMU_GPIO_01	NET_STATUS	--	B-PD,L	Low level	NO	Must be “output” when used as GPIO.

NOTES

1. Pins 59, 65, 67, 144~147, 149 and 159 cannot be pulled up before power-up. Pin 80 cannot be pulled down before power-up.
2. Pins 150, 159, 143 are recommended to be configured as output when multiplexed as GPIOs; when used as input, these pins should be pulled-up/down externally and configured as NP (No pull-up/down) internally.
3. The pin functions in Model 2/3/4 take effect only after software configuration.
4. [1)] Please refer to ***Table 3*** for more details about the symbol description.
5. [2)] “YES” means “interrupt function is supported”. “NO” means “interrupt function is not supported”.
6. [3)] When pins 3, 5, 169 and 170 are used as GPIOs, they can only be used as “output”.
7. All BOOT_CONFIG and FORCE_USB_BOOT pins are prohibited to be pulled up before the module is powered on.
8. “*” means under development.

The following table lists the pull-up and pull-down resistance values of AG35-CEN-Quecopen GPIOs.

Table 6: Pull-up/Pull-down Resistance of GPIOs

Symbol	Description	Pin No.	Min	Typ	Max	Unit
R_{PU}	Pull-up resistance	18~23, 25, 42, 43, 52, 56~62, 65~68, 73, 74, 77~80, 144, 147, 149, 163~166	55	100	390	kΩ
		143, 150, 159	5	7	50	kΩ
R_{PD}	Pull-down resistance	18~23, 25, 42, 43, 52, 56~ 62, 65~68, 73, 74, 77~80, 144, 147, 149, 163~166	55	100	390	kΩ
		143, 150, 159	5	7	50	kΩ

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command can set the module into airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

AG35-CEN-Quecopen is able to reduce its current consumption to a minimum value during the sleep mode. This chapter mainly introduces some ways to enter into or exit from sleep mode. The diagram below illustrates the current consumption of AG35-CEN-Quecopen during sleep mode.

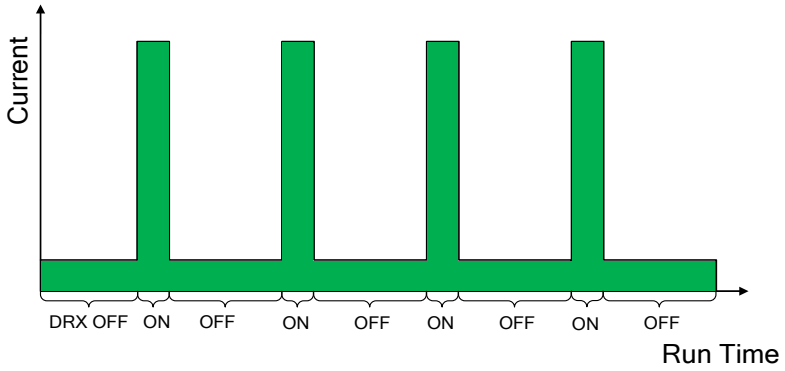


Figure 3: Sleep Mode Current Consumption Diagram

NOTE

DRX cycle index values are broadcasted by the wireless network.

3.5.1.1. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions must be met to let the module enter into the sleep mode.

- Use sleep & wakeup API to enable the sleep mode.
- Ensure the level of pins that configured as interrupt in ***Table 5*** are under non-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

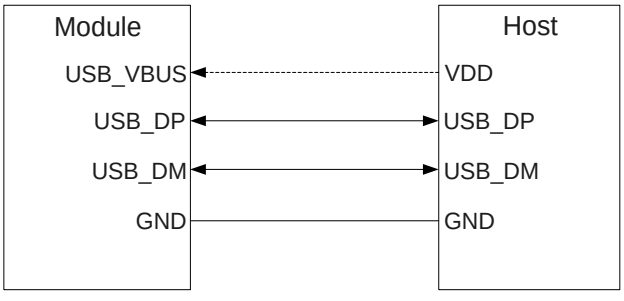


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to AG35-CEN-Quecopen through USB will wake up the module.
- When AG35-CEN-Quecopen has URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.2. USB Application without USB Remote Wakeup Function

If the host supports USB suspend/resume, but does not support remote wake-up function, it needs to be woken up via the module's GPIO.

There are three preconditions to let the module enter into the sleep mode.

- Use sleep & wakeup API to enable the sleep mode.
- Ensure the level of pins that configured as interrupt in ***Table 5*** are under non-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

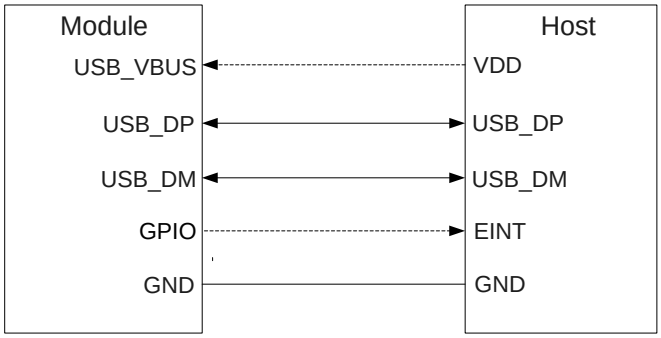


Figure 5: Sleep Mode Application without USB Remote Wakeup

- Sending data to AG35-CEN-Quecopen through USB will wake up the module.
- When AG35-CEN-Quecopen has URC to report, the module's GPIO signal can be used to wake up the host.

3.5.1.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to let the module enter into sleep mode.

- Use sleep & wakeup API to enable the sleep mode.
- Ensure the level of pins that configured as interrupt in ***Table 5*** are under non-wakeup status.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

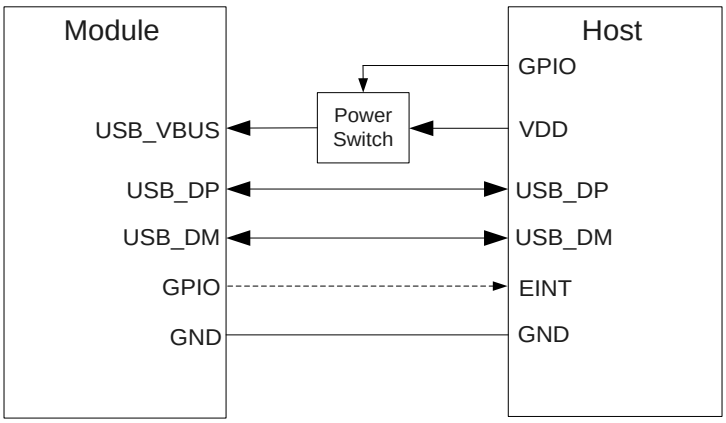


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Refer to ***document [2]*** for more details about the module's power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. The mode can be set via **AT+CFUN=<fun>** command. The parameter **<fun>** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

AG35-CEN-Quecopen provides six VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 8: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86, 87, 88	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	10, 13, 16, 17, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89~94, 96~100, 102~106, 108~112, 114, 116~118, 120~126, 128~131, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196~299	Ground		0		V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

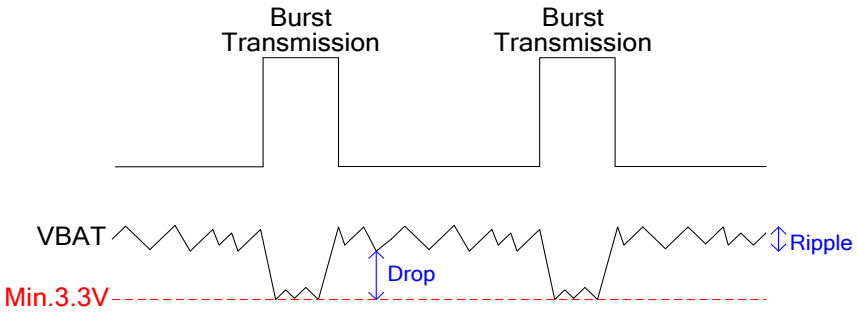


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a power TVS (e.g. WS4.5DPF-B, Vrwm=4.5V, Ppp=450W) and a zener diode with dissipation power more than 0.5W, and place it as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

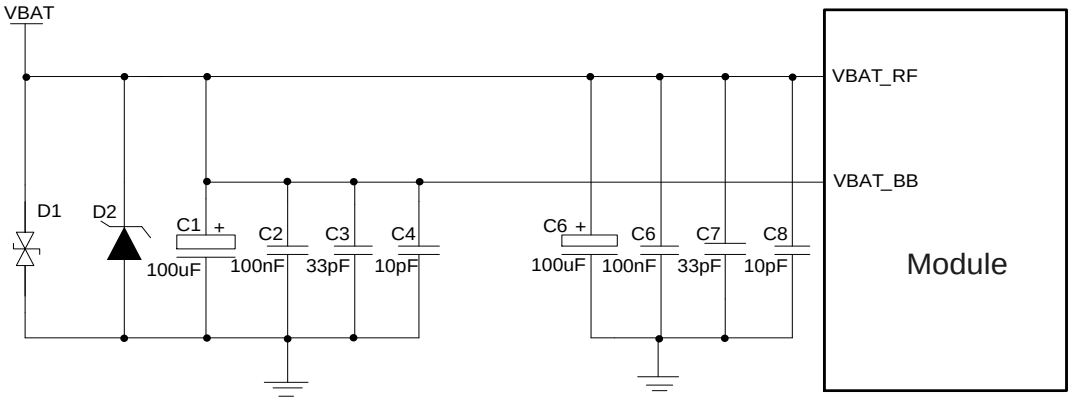


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply for AG35-CEN-Quecopen should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is recommended to use

an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

It is recommended use DC-DC converters with wide output voltage range (such as TPS54560-Q1 from *Texas Instruments*) for 12V/24V power systems. The following figure shows a reference design for +12V/24V input power system.

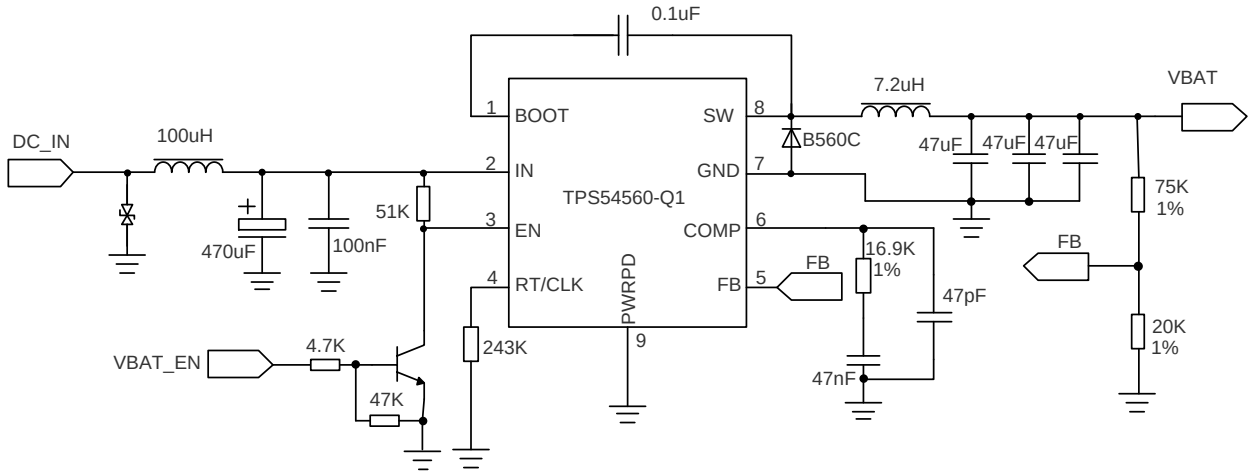


Figure 9: Reference Circuit of 12V/24V Power Supply

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. Please refer to ***document [3]*** for more details.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 9: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	2	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When AG35-CEN-Quecopen is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

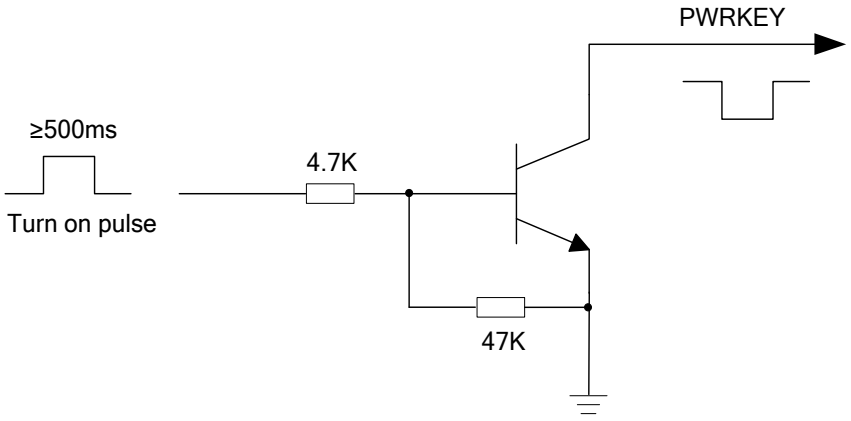


Figure 10: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

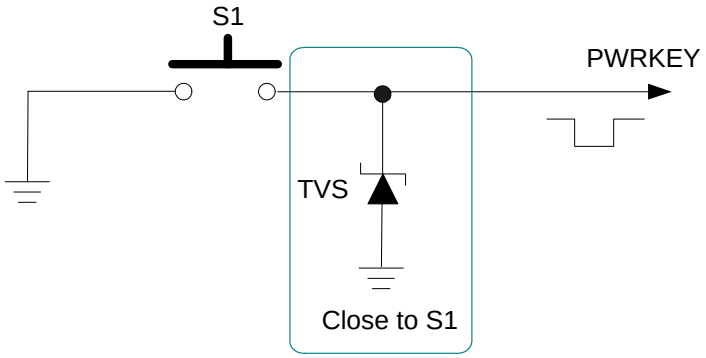


Figure 11: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

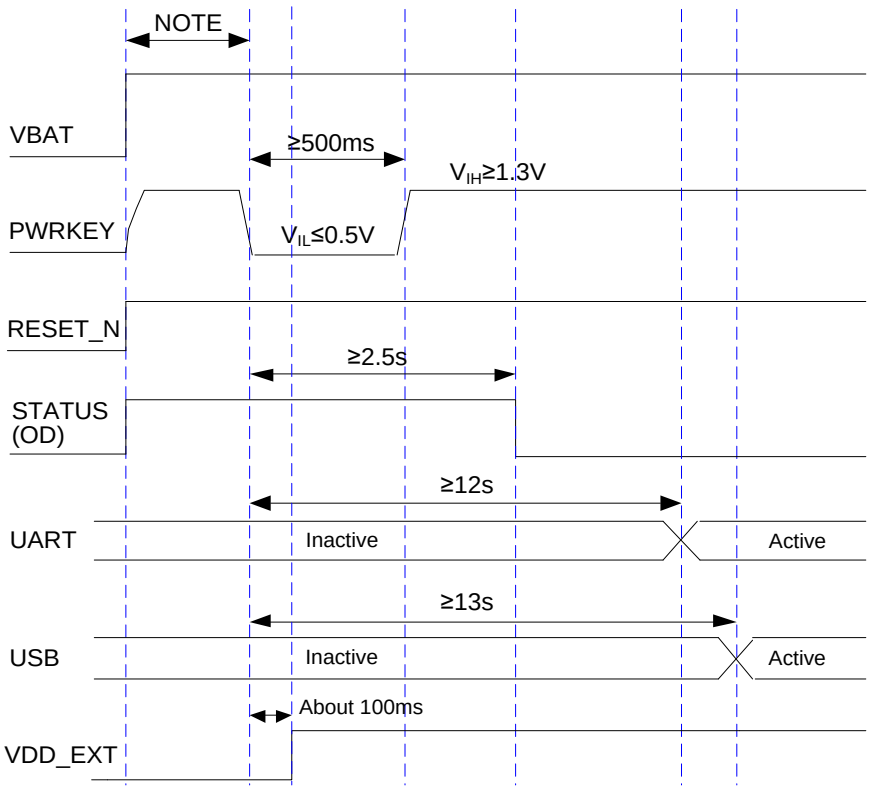


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.
2. It is recommended to use an external OD/OC circuit to control the PWRKEY pin.

3.7.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using AT command or API interface.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after PWRKEY is released. The power-down scenario is illustrated in the following figure.

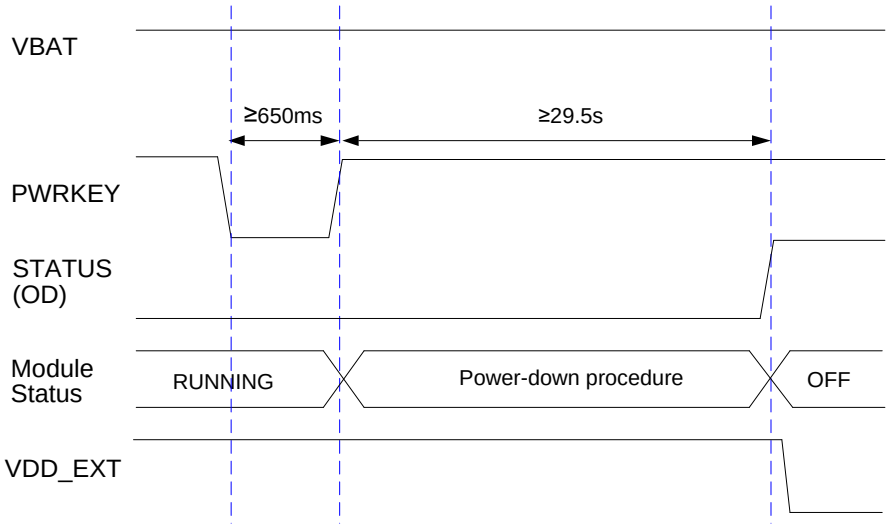


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command or API Interface

It is also a safe way to use **AT+QPOWD** command or API interface to turn off the module, which is similar to turning off the module via PWRKEY pin.

NOTES

1. In order to avoid damaging the internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command or API interface, the power supply can be cut off.
2. When turn off module with AT command or API, please keep PWRKEY at high level after the execution of power off command. If keep PWRKEY at low level voltage, the module will be turned on again.

3.7.3. Reset the Module

RESET_N can be used to reset the module. The module can be reset by driving the RESET_N to a low level voltage for 150~460ms. As the RESET_N pin is sensitive to interference, the routing trace on the interface board of the module is recommended to be as short as possible and totally ground shielded.

Table 10: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	1	Reset the module	V_{IH}max=2.1V	Pull-up to 1.8V internally.

	V_{IH}min=1.3V V_{IL}max=0.5V	Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

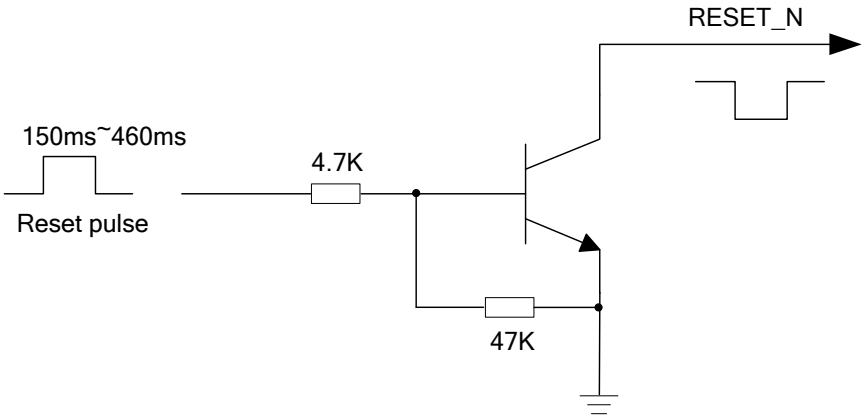


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

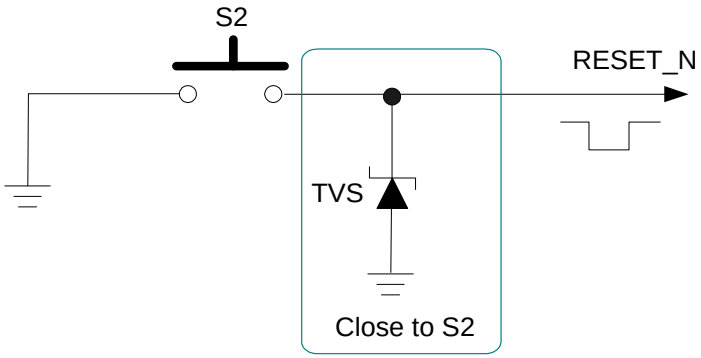


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

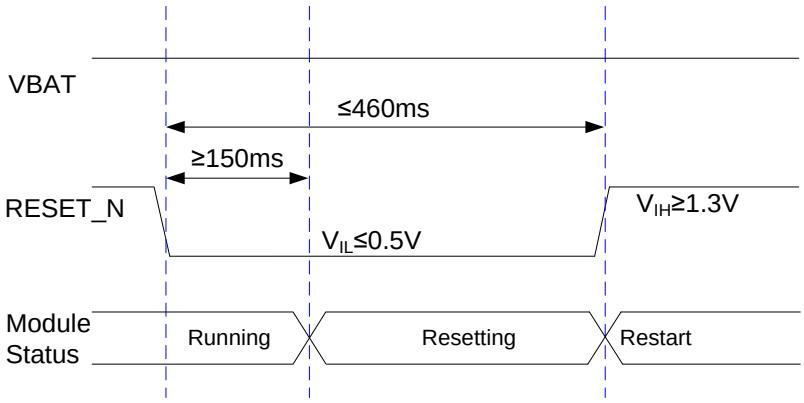


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by AT command, API interface and PWRKEY pin all failed.
2. Please assure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 11: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	26	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	29	IO	Data signal of (U)SIM card	
USIM_CLK	27	DO	Clock signal of (U)SIM card	
USIM_RST	28	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	25	DI	(U)SIM card insertion detection	
USIM_GND	24		Specified ground for (U)SIM card	

AG35-CEN-Quecopen supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [3]*** about **AT+QSIMDET** command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

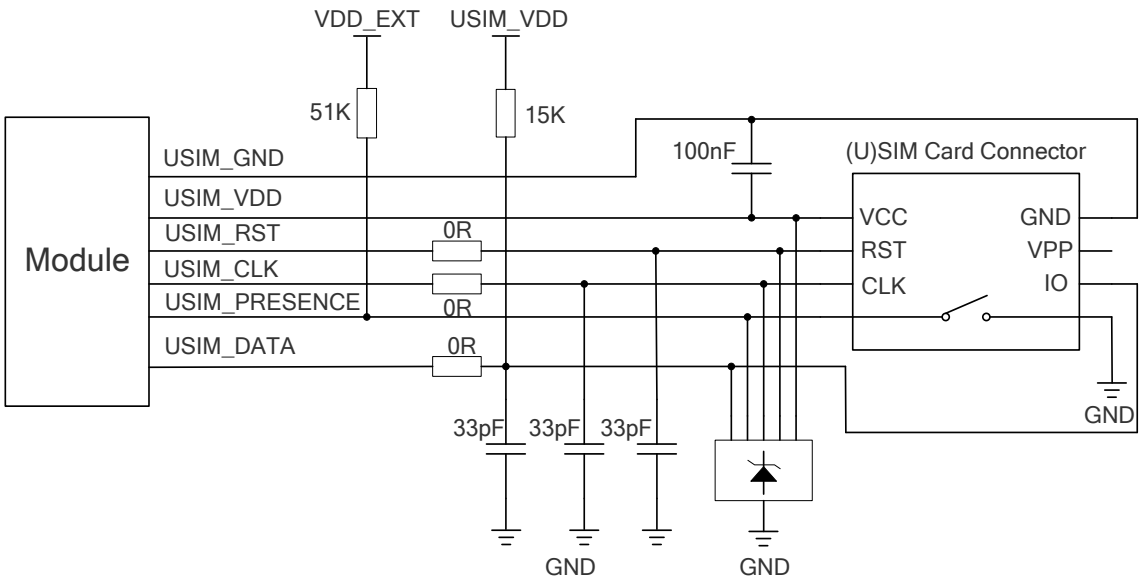


Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, then USIM_PRESENCE can be used for other functions. Please refer to ***Table 5*** for more details. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

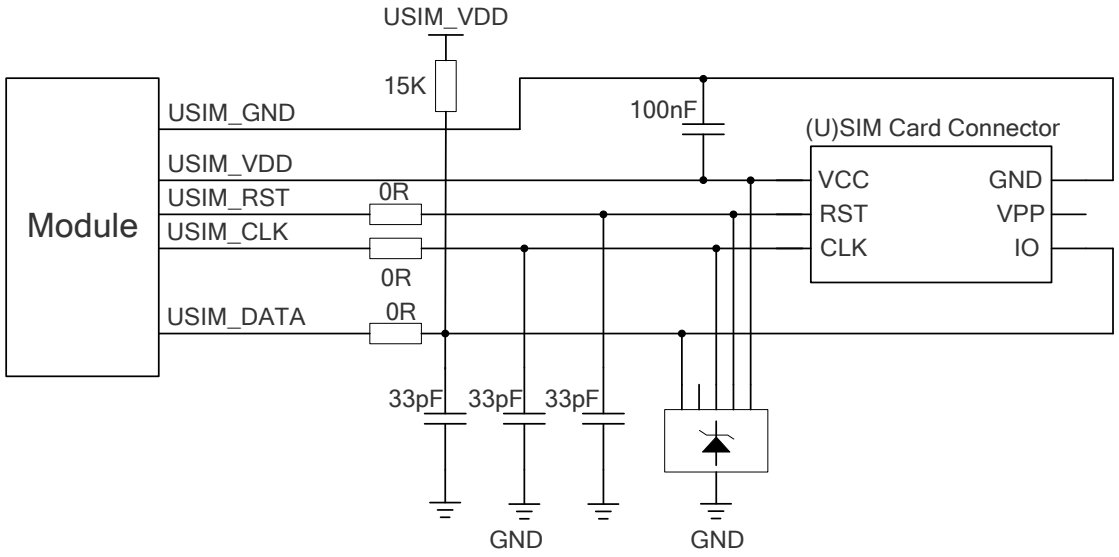


Figure 18: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10pF. The 0Ω resistors should be added in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 33pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

NOTE

The load capacitance of (U)SIM interface will affect rise and fall time of the data exchange.

3.9. USB Interface

AG35-CEN-Quecopen contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	PI	Power supply for USB USB connection detection	Typical 5.0V Maximum current: 1mA
USB_DM	33	IO	USB differential data bus (-)	Require differential impedance of 90Ω
USB_DP	34	IO	USB differential data bus (+)	
GND	30		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in application design. The following figure shows a reference circuit of USB interface.

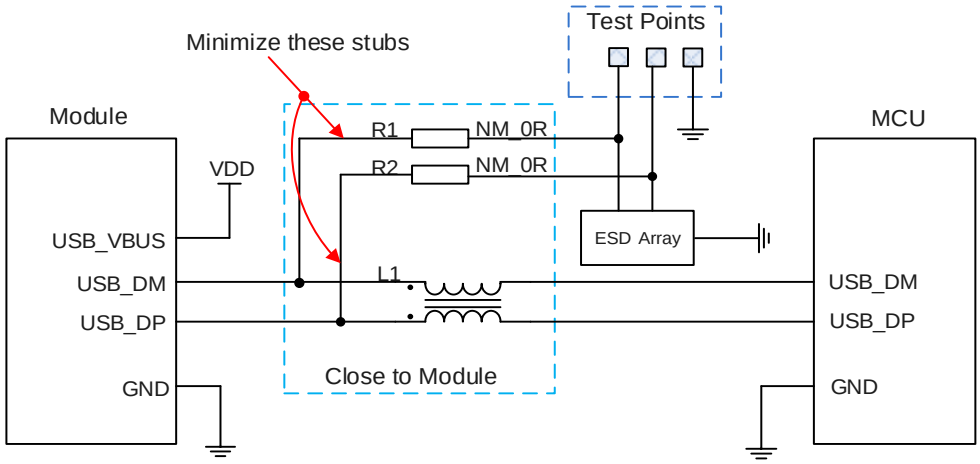


Figure 19: Reference Circuit of USB Application

In order to ensure signal integrity of USB data lines, components R1, R2 and L1 (Common Mode Chock) must be placed close to the module, and also these not mounted resistors which are used for debugging should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components as close to the USB connector as possible.

NOTE

AG35-CEN supports USB host mode, and the USB interface worked in slave mode by default.

3.10. UART Interfaces

The module provides six UART interfaces: UART1 ~ UART5 and debug UART. The following are the features of these UART interfaces.

- UART1 ~ UART4 have the same functions. They support 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bps baud rates, and the default is 115200bps. They all support RTS and CTS hardware flow control, and are used for data transmission with peripherals.
- UART3 is multiplexed from SPI. UART4 and UART5 are multiplexed from SDIO1.
- UART5 does not support hardware flow control, and the maximum baud rate is 115200bps.
- The debug UART interface supports 115200bps baud rate, and is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 13: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Function		UART1 Pin Description
			Alternate Function 1 (Default)	Alternate Function 2	
UART1_CTS	56	DO	UART_CTS_BLSP3	GPIO_3	DTE clear to send
UART1_RTS	57	DI	UART_RTS_BLSP3	GPIO_2	DTE request to send
UART1_RXD	58	DI	UART_RXD_BLSP3	GPIO_1	Receive data
UART1_TXD	60	DO	UART_TXD_BLSP3	GPIO_0	Transmit data

Table 14: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Function		
			Alternate Function 1 (Default)	Alternate Function 2	Alternate Function 3
UART2_TXD	163	DO	UART_TXD_BLSP5	GPIO_8	SPI_MOSI_BLSP5
UART2_CTS	164	DO	UART_CTS_BLSP5	GPIO_11	SPI_CLK_BLSP5
UART2_RXD	165	DI	UART_RXD_BLSP5	GPIO_9	SPI_MISO_BLSP5
UART2_RTS	166	DI	UART_RTS_BLSP5	GPIO_10	SPI_CS_N_BLSP5

Table 15: Pin Definition of UART3 Interface (Multiplexed from SPI)

Pin Name	Pin No.	I/O	Function			
			Alternate Function 1 (Default)	Alternate Function 2	Alternate Function 3	Alternate Function 4
SPI_MOSI	77	DO	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6	PCM_1_SYNC
SPI_MISO	78	DI	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6	PCM_1_DIN
SPI_CS_N	79	DO	SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6	PCM_1_DOUT
SPI_CLK	80	DO	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6	PCM_1_CLK

Table 16: Pin Definition of UART4 Interface (Multiplexed from SDIO1)

Pin Name	Pin No.	I/O	Function		
			Alternate Function 1 (Default)	Alternate Function 2	Alternate Function 3
SDC1_DATA0	20	IO	SDC1_DATA0	GPIO_15	UART_CTS_BLSP1
SDC1_DATA1	21	IO	SDC1_DATA1	GPIO_14	UART_RTS_BLSP1
SDC1_DATA2	22	IO	SDC1_DATA2	GPIO_13	UART_RXD_BLSP1
SDC1_DATA3	23	IO	SDC1_DATA3	GPIO_12	UART_TXD_BLSP1

Table 17: Pin Definition of UART5 Interface (Multiplexed from SDIO1)

Pin Name	Pin No.	I/O	Function		
			Alternate Function 1 (Default)	Alternate Function 2	Alternate Function 3
SDC1_CMD	18	IO	SDC1_CMD	GPIO_17	UART_RXD_BLSP4
SDC1_CLK	19	DO	SDC1_CLK	GPIO_16	UART_TXD_BLSP4

Table 18: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	71	DO	Transmit data	1.8V power domain
DBG_RXD	72	DI	Receive data	1.8V power domain

NOTEs

1. The non-default alternate functions mentioned in the above tables take effect only after software configuration. Please refer to ***Table 5*** for details.
2. When UART3 (multiplexed from SPI interface) uses a voltage-level translator chip to communicate with MCU, it is recommended to select translator chips without pull-ups internally.

The logic levels of the UART interfaces are described in the table below.

Table 19: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interfaces. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0104EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

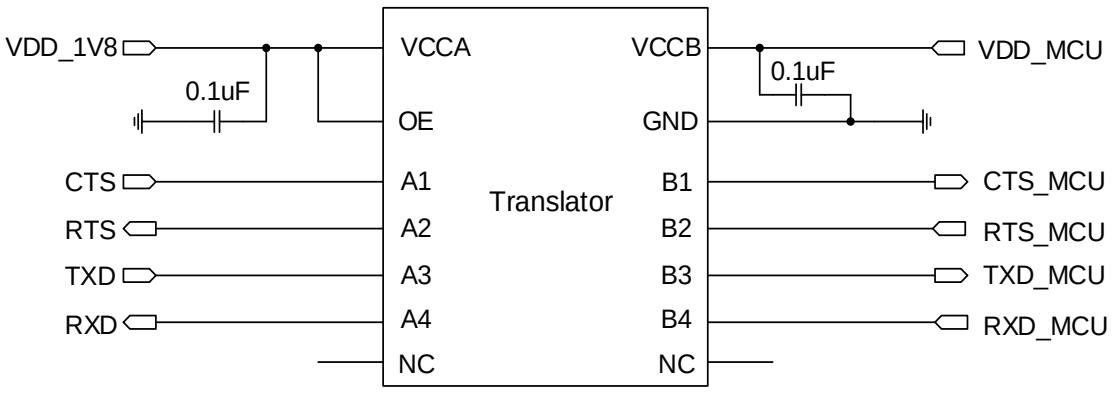


Figure 20: Reference Circuit with Translator Chip

NOTE

When the customers select TXS series level translator provided by *Texas Instruments*, attention should be paid to whether the pin connected with level translator is BOOT_CONFIG pin. If the BOOT_CONFIG pin have to connect with level translator, it is recommended to control the OE pin of the level translator by MCU, make the OE pin at low level before the module turn on by default, when the module starts up successfully, make the OE pin at high level.

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

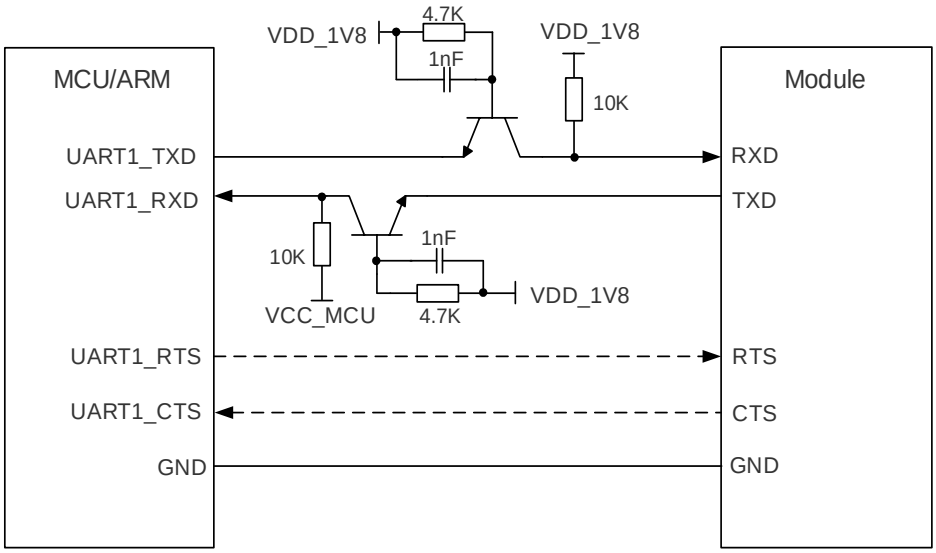


Figure 21: Reference Circuit with Transistor Circuit

NOTES

1. The above is a reference circuit of UART1 interface, which is similar to that of other UART interfaces.
2. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
3. If customers' design need to use flow control function, the CTS and RTS also need to use level translator.
4. When the module enters into sleep mode, it is recommended to switch off the power supply for VDD_1V8 so as to reduce power consumption.

3.11. PCM and I2C Interfaces

AG35-CEN-Quecopen provides one Pulse Code Modulation (PCM) digital interface for audio design. The interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

AG35-CEN-Quecopen supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8kHz PCM_SYNC and 256kHz PCM_CLK.

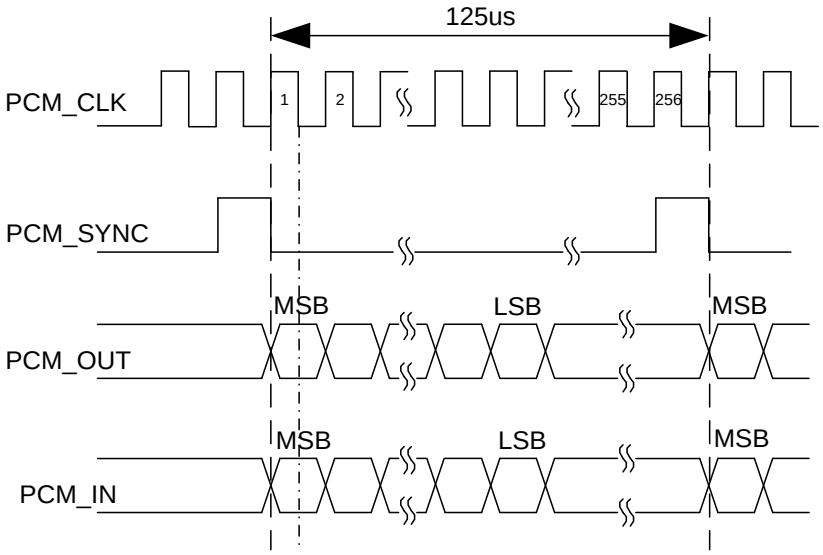


Figure 22: Primary Mode Timing

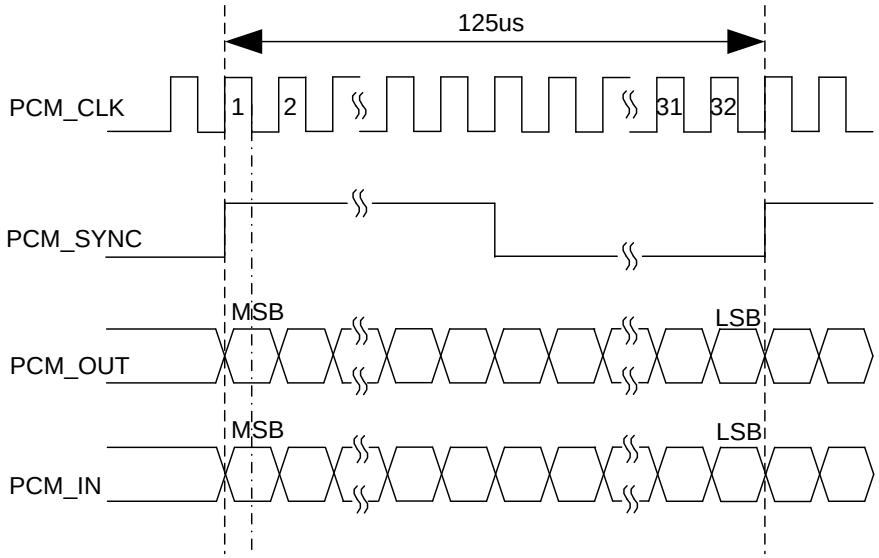


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 20: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	65	IO	PCM data frame sync signal	1.8V power domain. In host mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_IN	66	DI	PCM data input	1.8V power domain. If unused, keep it open.
PCM_CLK	67	IO	PCM data bit clock	1.8V power domain. In host mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	1.8V power domain. If unused, keep it open.
MCLK	152	DO	Main clock	Output 12.288MHz.

Table 21: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	42	IO	I2C1 serial data	Used for external codec configuration by default. Require external pull-up to 1.8V. If unused, keep it open.
I2C1_SCL	43	DO	I2C1 serial clock	
I2C2_SDA	73	IO	I2C2 serial data	Require external pull-up to 1.8V. If unused, keep it open.
I2C2_SCL	74	DO	I2C2 serial clock	

NOTES

1. For more details about non-default alternate functions for the pins mentioned in the above two tables, please refer to Table 5.
2. By default, I2C1 is used for codec configuration while I2C2 is not available with any codec configuration driver.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048kHz PCM_CLK and 8kHz PCM_SYNC. Please refer to ***document [3]*** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM interface with an external codec IC.

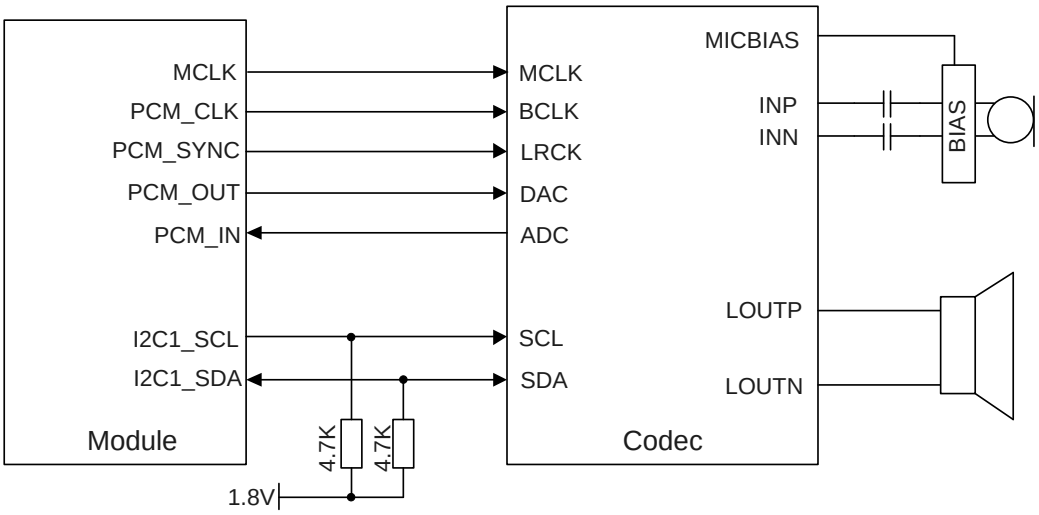


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. AG35-CEN-Quecopen works as a master device pertaining to I2C interface.
3. The analog GND designed for external audio function should be connected to the main GND via the 0Ω resistor.

3.12. SDIO Interfaces

AG35-CEN-Quecopen provides the following two SDIO interfaces which support SD 3.0 protocol:

3.12.1. SDIO1 Interface

SDIO1 interface is used for WLAN function. More details are provided in ***Chapter 3.15***.

3.12.2. SDIO2 Interface

SDIO2 interface supports 1.8V/2.85V SD card and 1.8V eMMC (embedded MultiMediaCard).

The following tables show the pin definition of SDIO2 interface.

Table 22: Pin Definition of SDIO2 Interface

Pin Name	Pin No.	I/O	Description	Comment
VDD_SDIO	46	PO	**SD card application:** SDIO pull-up power source **eMMC application:** Keep it open	1.8V/2.85V configurable output. SDIO pull-up power source for SD card.
SDC2_DATA2	47	IO	SDIO data signal (bit 2)	SDIO signal level can be selected according to the one supported by SD card. 1.8V power domain for eMMC. Please refer to SD 3.0 protocol for more details.
SDC2_DATA3	48	IO	SDIO data signal (bit 3)	
SDC2_DATA0	49	IO	SDIO data signal (bit 0)	
SDC2_DATA1	50	IO	SDIO data signal (bit 1)	
SDC2_CMD	51	IO	SDIO commend single	

SDC2_CLK	53	DO	SDIO bus clock
SD_INS_DET[1)]	52	DI/DO	**DI:** Insertion detection for SD card. **DO:** Reset eMMC [1)]

NOTE

1) SD_INS_DET for eMMC resetting is currently not supported.

3.12.2.1. Reference Design for SD Card Application

The following figure shows a reference design of SDIO2 interface for SD card application.

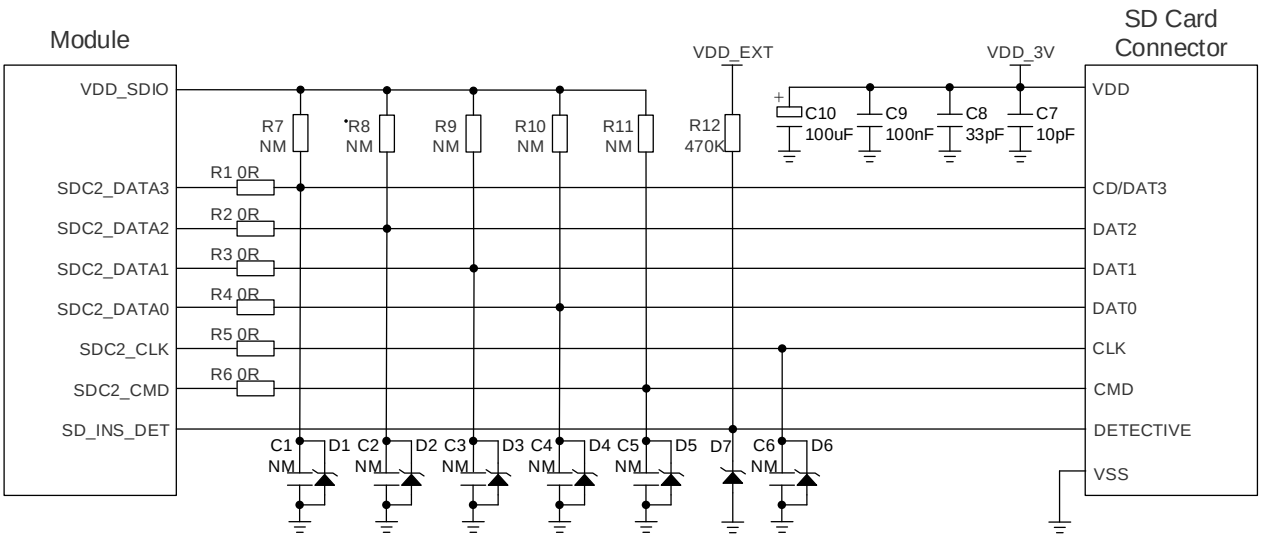


Figure 25: Reference Circuit Design for SD Card Application

In order to enhance the reliability and availability of customers' application, please follow the principles below in the SD card circuit design:

- The voltage range of SD card power supply VDD_3V is 2.7~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, it is recommended to reserve 100kΩ resistors R7~R11 for pulling up SDIOs to VDD_SDIO. The resistors are not mounted by default, and the recommended resistor value is among 10~100kΩ.
- In order to improve signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default.

All resistors and bypass capacitors should be placed close to the module.

- In order to offer good ESD protection, it is recommended to add TVS with capacitance value less than 2pF on SD card pins, and place it close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 0.8mm and the total routing length less than 50mm. The total trace length inside the module is 23mm, so the exterior total trace length should be less than 27mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 40pF.

3.12.2.2. Reference Design for eMMC Application

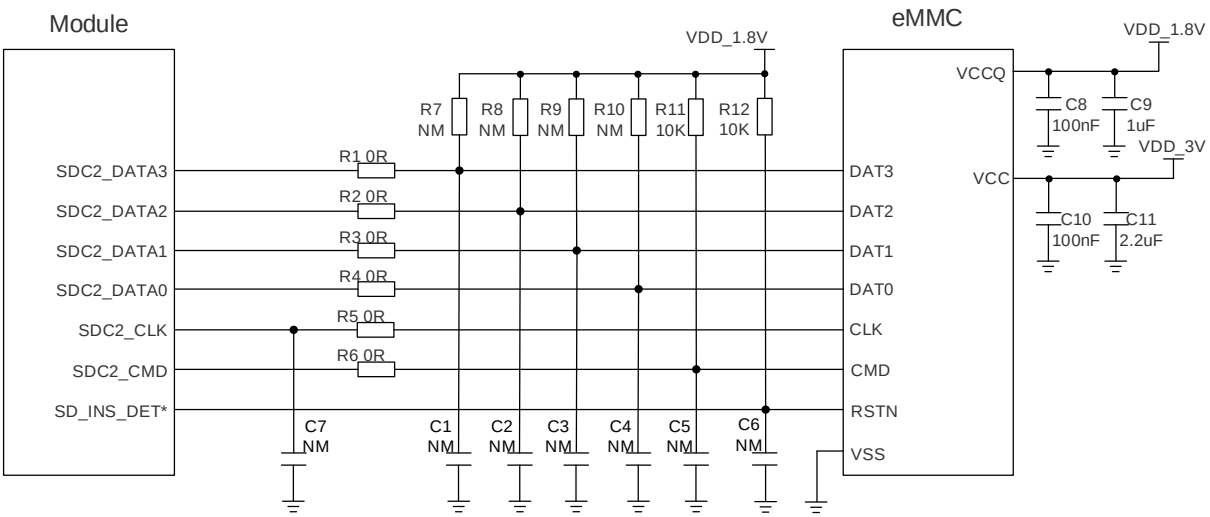


Figure 26: Reference Circuit Design for eMMC Application

Please follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve 100kΩ resistors R7~R10 for pulling up SDIOs to VDD_1.8V. The resistors are not mounted by default, and the recommended resistor value is among 10~100kΩ.
- In order to improve signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and eMMC. The bypass capacitors C1~C7 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 0.8mm and the total routing length less than 50mm. The total trace length inside the module is 23mm, so the exterior total trace length should be less than 27mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 40pF.

3.13. SPI Interfaces

AG35-CEN-Quecopen provides three SPI interfaces (SPI2 and SPI3 multiplexed from UARTs) which support only master mode. The maximum clock frequency of SPI1 and SPI3 is 50MHz, and the maximum clock frequency of SPI2 is 38MHz.

The following tables show the pin definition.

Table 23: Pin Definition of SPI1 Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_MOSI	77	DO	SPI master out slave in	1.8V power domain. If unused, keep it open.
SPI_MISO	78	DI	SPI master in slave out	1.8V power domain. If unused, keep it open.
SPI_CS_N	79	DO	SPI chip select	1.8V power domain. If unused, keep it open.
SPI_CLK	80	DO	SPI serial clock	1.8V power domain. If unused, keep it open.

Table 24: Pin Definition of SPI2 Interface (Multiplexed from UART1)

Pin Name	Pin No.	I/O	Function		
			Alternate function 1 (Default)	Alternate function 2	Alternate function 3
UART1_CTS	56	DO	UART_CTS_BLSP3	GPIO_3	SPI_CLK_BLSP3
UART1_RTS	57	DI	UART_RTS_BLSP3	GPIO_2	SPI_CS_N_BLSP3
UART1_RXD	58	DI	UART_RXD_BLSP3	GPIO_1	SPI_MISO_BLSP3
UART1_TXD	60	DO	UART_TXD_BLSP3	GPIO_0	SPI_MOSI_BLSP3

Table 25: Pin Definition of SPI3 Interface (Multiplexed from UART2)

Pin Name	Pin No.	I/O	Function		
			Alternate function 1 (Default)	Alternate function 2	Alternate function 3
UART2_TXD	163	DO	UART_TXD_BLSP5	GPIO_8	SPI_MOSI_BLSP5
UART2_CTS	164	DO	UART_CTS_BLSP5	GPIO_11	SPI_CLK_BLSP5
UART2_RXD	165	DI	UART_RXD_BLSP5	GPIO_9	SPI_MISO_BLSP5
UART2_RTS	166	DI	UART_RTS_BLSP5	GPIO_10	SPI_CS_N_BLSP5

NOTE

For more details about non-default alternate functions for the pins mentioned in the above table, please refer to ***Table 5***.

The following figure shows the timing relationship of SPI interfaces. The related parameters of SPI timing are shown in the table below.

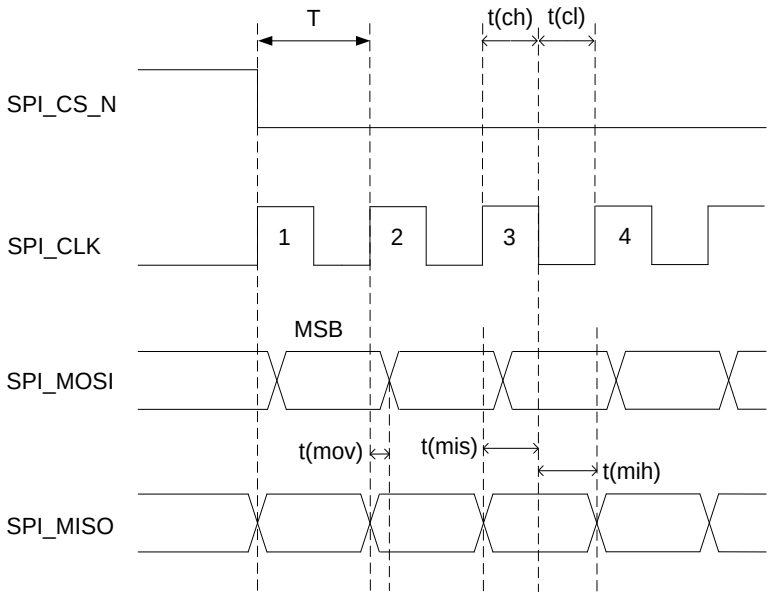


Figure 27: SPI Timing

Table 26: Parameters of SPI Interface Timing

Parameter	Description	Min	Typical	Max	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	9.0	-	-	ns
t(cl)	SPI clock low-level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8V SPI interfaces. A level translator should be used between the module and the host if customer's application is equipped with a 3.3V processor or device interface.

3.14. SGMII Interface

AG35-CEN-Quecopen includes an integrated ethernet MAC with an SGMII interface and two management interfaces. Key features of the SGMII interface are shown below:

- IEEE802.3 compliant
- Half/full duplex for 10/100/1000Mbps
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY, such as DP83TC811S-Q1, or to an external switch
- Management interfaces support 1.8V/2.85V power domains

The following table shows the pin definition of SGMII interface.

Table 27: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
MDIO Interface				
EPHY_RST_N	6	DO	Ethernet PHY reset	1.8V/2.85V power domain

EPHY_INT_N	9	DI	Ethernet PHY interrupt	1.8V power domain
SGMII_MDATA	8	IO	SGMII MDIO (Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	7	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
VDD_MDIO	4	PO	SGMII MDIO pull-up power source	1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	15	AO	SGMII transmission (-)	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	14	AO	SGMII transmission (+)	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	12	AI	SGMII receiving (+)	
SGMII_RX_M	11	AI	SGMII receiving (-)	

The following figure shows the simplified block diagram for Ethernet application.

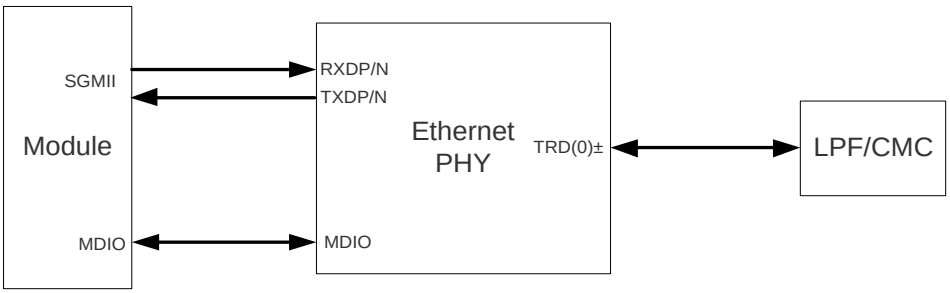


Figure 28: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY application for AG35-CEN-Quecopen module. For more details, please refer to ***document [6]***.

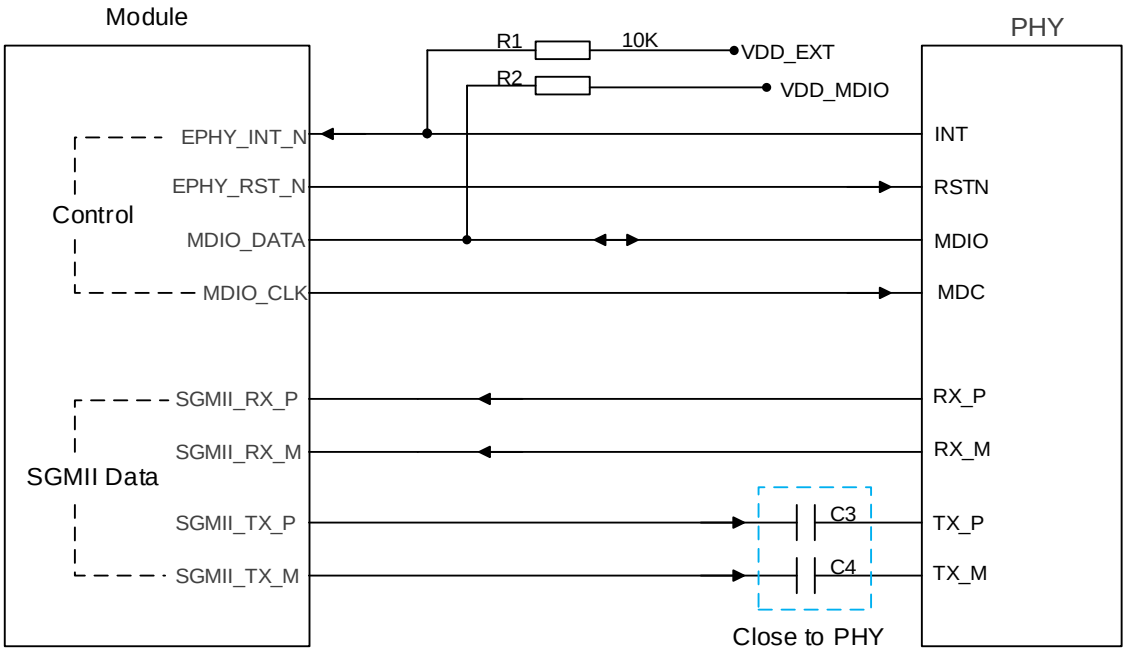


Figure 29: Reference Circuit of SGMII Interface with PHY Application

In order to enhance the reliability and availability of customers' application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- Keep the maximum trace length less than 25.4mm and keep skew on the differential pairs less than 0.5mm.
- The differential impedance of SGMII data trace is 100Ω±10%. It is important to route the data and control signals with total grounding.
- To minimize crosstalk, it is recommended to maintain the intra-lane spacing of control signals and intra-pair spacing of data signals both as three times of the trace width.
- The resistor R2 should be placed near the PHY, and its value varies according to the selection of PHY.

3.15. Wireless Connectivity Interfaces

AG35-CEN-Quecopen provides a low-power SDIO 3.0 interface (SDIO1 interface) for WLAN function.

The following table shows the pin definition of wireless connectivity interfaces.

Table 28: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
Power Part				
PM_ENABLE	5	DO	External power enable control for WLAN	1.8V power domain
WLAN Part				
SDC1_CMD	18	IO	WLAN SDIO command signal	1.8V power domain
SDC1_CLK	19	DO	WLAN SDIO clock signal	1.8V power domain
SDC1_DATA0	20	IO	WLAN SDIO data bus (bit 0)	1.8V power domain
SDC1_DATA1	21	IO	WLAN SDIO data bus (bit 1)	1.8V power domain
SDC1_DATA2	22	IO	WLAN SDIO data bus (bit 2)	1.8V power domain
SDC1_DATA3	23	IO	WLAN SDIO data bus (bit 3)	1.8V power domain
WLAN_EN	149	DO	WLAN function enable control via Wi-Fi module	1.8V power domain
WLAN_WAKE [1)]	160	DI	Wake up module via WLAN	1.8V power domain
WLAN_SLP_CLK	169	DO	WLAN sleep clock	1.8V power domain
Coexistence Part				
COEX_UART_TX	145	DO	LTE/WLAN&BT coexistence signal	1.8V power domain Must be at low level before the module powers up successfully.
COEX_UART_RX /USB_BOOT	146	DI	LTE/WLAN&BT coexistence signal	1.8V power domain Must be at low level before the module powers up successfully.

NOTES

1. When WLAN function is used, the coexistence part mentioned in the above table must be used simultaneously. The coexistence part cannot be used as common serial port (UART).
2. [1)] The internal pull-up/down resistor pin 160 (WLAN_WAKE) ranges from 5kΩ ~ 50kΩ (Typical: 7kΩ).

The following figure shows a reference design for the connection between wireless connectivity interfaces with Quectel FC20 module.

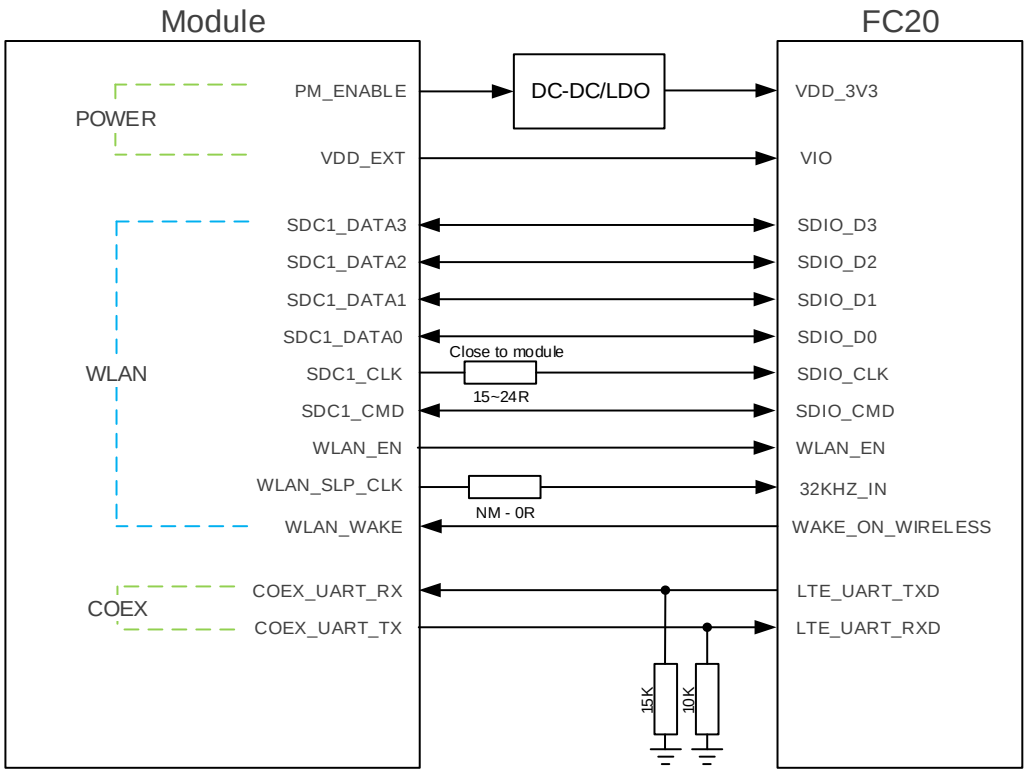


Figure 30: Reference Circuit for Connection with FC20 Module

NOTES

1. FC20 module can only be used as a slave device.
2. For more information about wireless connectivity interfaces application, please refer to ***document [6]***.

3.15.1. WLAN Interface

AG35-CEN-QuecOpen provides SDIO1 interface which supports Single data rate (SDR) mode (up to 50MHz).

As SDIO signals are high-speed signals, in order to ensure the SDIO1 interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.

- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total length of SDIO signal traces inside AG35-CEN-Quecopen module is 12mm and that inside FC20 is 10mm, so the exterior total trace length should be less than 28mm.
- Keep termination resistors within 15~24Ω on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5mm.
- Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.

3.16. ADC Interfaces

The module provides three analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read via **AT+QADC=<port>** command, through setting **<port>** into 0, 1 or 2. For more details about the AT command, please refer to ***document [3]***.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2

In order to improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 29: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC2	172	General purpose analog to digital converter interface
ADC1	175	General purpose analog to digital converter interface
ADC0	173	General purpose analog to digital converter interface

The following table describes the characteristic of ADC interfaces.

Table 30: Characteristic of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC2 Voltage Range	0.1		1.7	V
ADC1 Voltage Range	0.3		VBAT_BB	V

ADC0 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits
ADC Sample Rate		2.4		MHz

NOTES

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.17. Network Status Indication

AG35-CEN-Quecopen provides one network indication pin: NET_STATUS. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NET_STATUS in different network status.

Table 31: Pin Definition of the Network Status Indicator (NET_STATUS)

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	170	DO	Indicate the module's network activity status.	1.8V power domain

Table 32: Working State of the Network Status Indicator (NET_STATUS)

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

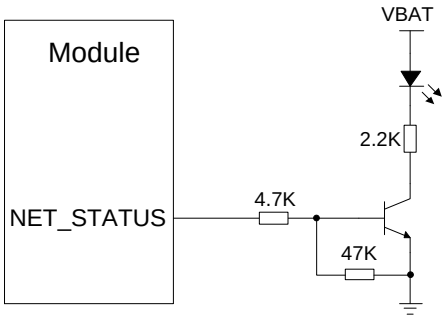


Figure 31: Reference Circuit of the Network Status Indicator

3.18. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pulled up resistor, or as LED indication circuit as shown below. When the module is turned on normally, the STATUS will present a low level state. Otherwise, the STATUS will present high-impedance state.

Table 33: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	OD	Indicate the module's operation status	Require external pull-up, If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to specific application demands.

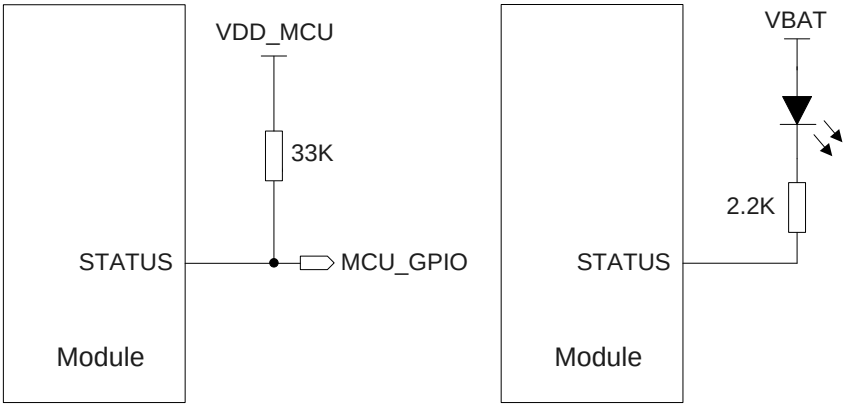


Figure 32: Reference Circuits of STATUS

NOTE

1. In sleep state, STATUS will still output a low voltage to drive the LED, causing an extra current consumption on VBAT. So it is recommended to replace VBAT with an external controllable power supply, and use it to switch off the power source during sleep state so as to reduce power consumption.
2. It is not recommended to use voltage-level translator for the circuit design of pin 171 (STATUS).

3.19. USB_BOOT Interface

AG35-CEN-Quecopen supports USB BOOT function. Developers can pull up the pin to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 34: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_ UART_RX/ USB_BOOT	146	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

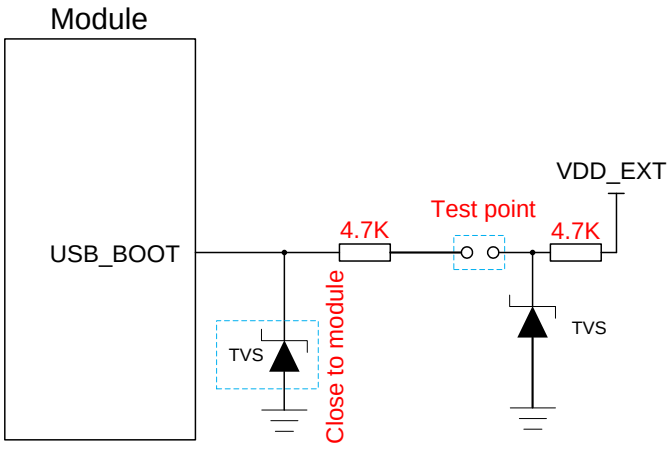


Figure 33: Reference Circuit of USB_BOOT Interface

3.20. RTC

AG35-CEN-Quecopen has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not be maintained. If RTC needs to be maintained, then VBAT_BB must be powered all the time.

3.21. HSIC Interface*

AG35-CEN-Quecopen provides a HSIC interface for EAVB. HSIC is a 2-signal source synchronous serial interface which uses 240MHz DDR signaling to provide High-Speed 480Mbps USB transfers which are 100% host driver compatible with traditional USB cable-connected topologies. The HSIC interface supports the following features:

- High-Speed 480Mbps data rate only
- No power consumed unless a transfer in progress
- Signals driven at 1.2V standard LVCMOS levels.

The following table shows the pin definition of HSIC interface.

Table 35: Pin Definition of HSIC Interface

Pin Name	Pin No.	I/O	Description	Comment
HSIC_STROBE*	194	IO	High speed inter chip interface - strobe	1.2V power domain. If unused, keep them open.
HSIC_DATA*	195	IO	High speed inter chip interface - data	

The following table shows the layout guidelines of HSIC interface.

Table 36: Design guidelines for HSIC

Designs		Guidelines
General	Data rate	480Mbps
	Impedance	45Ω ~ 55Ω
Length matching	Intra-pair match	< 2.5mm (15ps)

	Maximum trace length	8cm
Spacing	HSIC to all other signals	> 3 × line width
	HSIC_DATA to HSIC_STROBE	> 3 × line width

NOTES

1. "*" means under development.
2. More details will be provided in a future release of this document.

4 GNSS Receiver

4.1. General Description

AG35-CEN-Quecopen includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

AG35-CEN-Quecopen supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, GNSS engine of the module is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [5]***.

4.2. GNSS Performance

The following table shows GNSS performance of AG35-CEN-Quecopen.

Table 37: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start	Autonomous	2.5	s

	@open sky	XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and eMMC should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Control the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

AG35-CEN-Quecopen include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The antenna ports have an impedance of 50Ω.

5.1. Main/Rx-diversity Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces are shown below.

Table 38: Pin Definition of the RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	107	IO	Main antenna interface	50Ω impedance
ANT_DIV	127	AI	Receive diversity antenna interface	50Ω impedance If unused, keep it open.

5.1.2. Operating Frequency

Table 39: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B8	880~915	925~960	MHz
EVDO/CDMA BC0	824~849	869~894	MHz
TD-SCDMA B34	2010~2025	2010~2025	MHz

TD-SCDMA B39	1880~1920	1880~1920	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of main and Rx-diversity antenna interfaces is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2 and R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default.

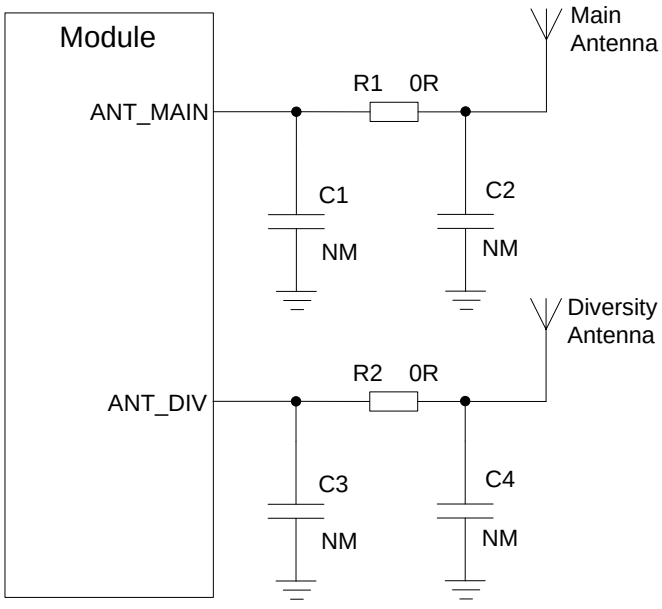


Figure 34: Reference Circuit of RF Antenna Interfaces

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity. Please refer to ***document [2]*** for details.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

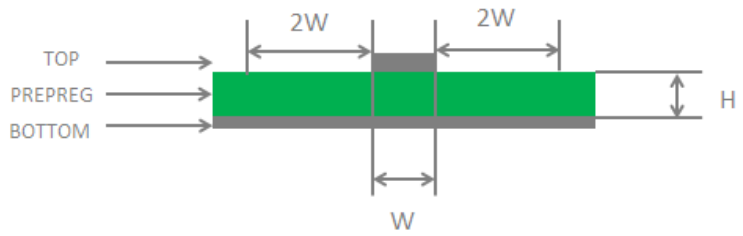


Figure 35: Microstrip Design on a 2-layer PCB

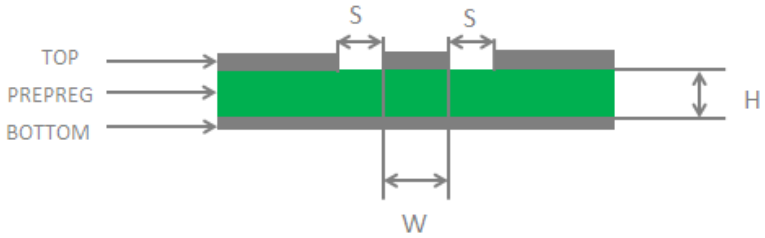


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

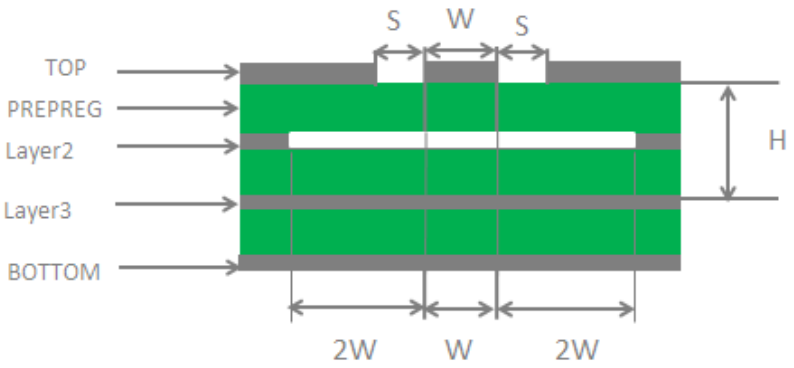


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

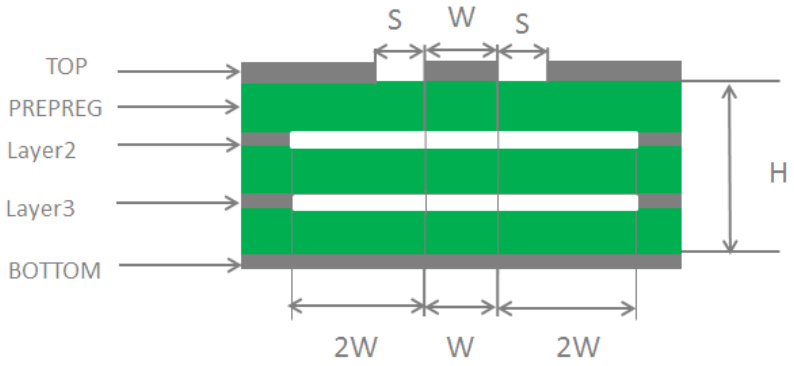


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2*W).

For more details about RF layout, please refer to ***document [5]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 40: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50Ω impedance

Table 41: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

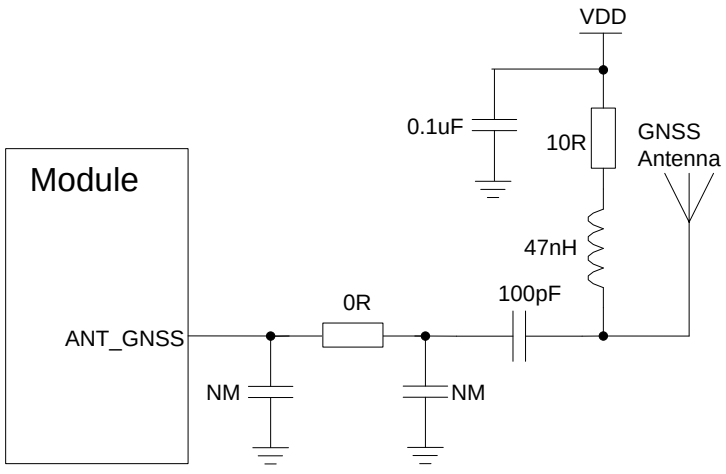


Figure 39: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 42: Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17dB
GSM/EVDO/CDMA/UMTS/ TD-SCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30% Max input power: 50W Input impedance: 50Ω Cable insertion loss: < 1dB (EGSM900, WCDMA B8, LTE-FDD B5/B8, EVDO/CDMA BC0) Cable insertion loss: < 1.5dB (DCS1800, WCDMA B1, LTE-FDD B1/B3, LTE-TDD B34/B39, TD-SCDMA B34/B39) Cable insertion loss: < 2dB (LTE-TDD B38/B40/B41)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *HIROSE*.

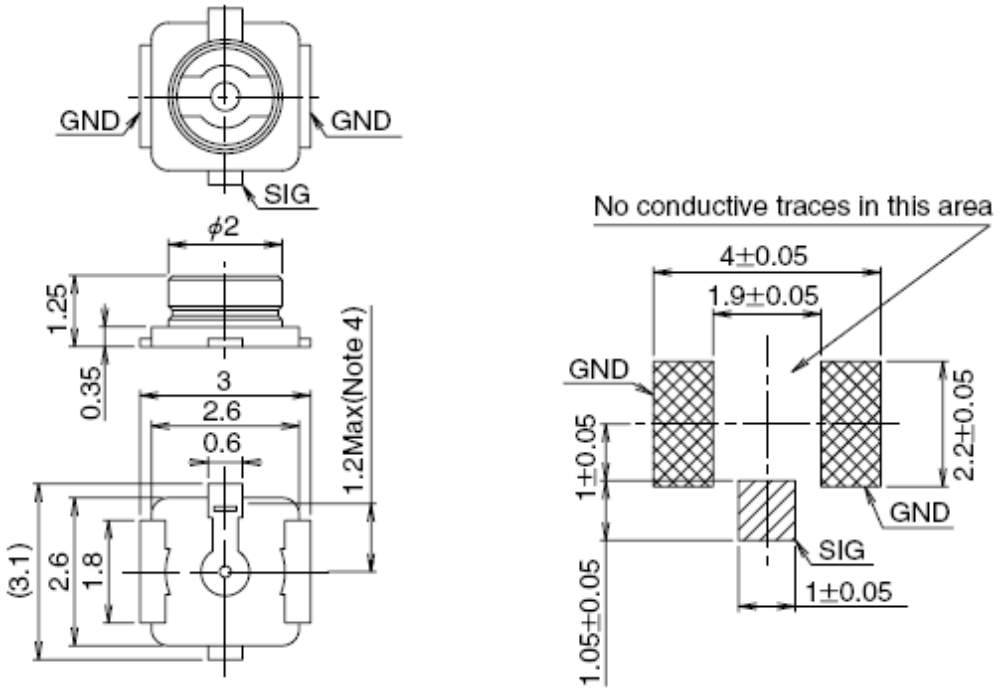


Figure 40: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connector listed in the following figure can be used to match the U.FL-R-SMT.

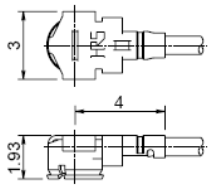
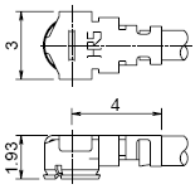
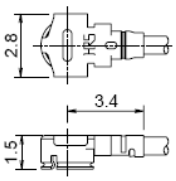
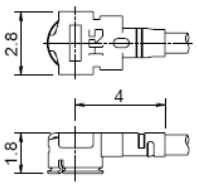
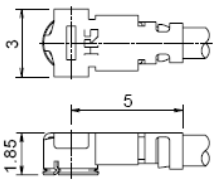
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 41: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

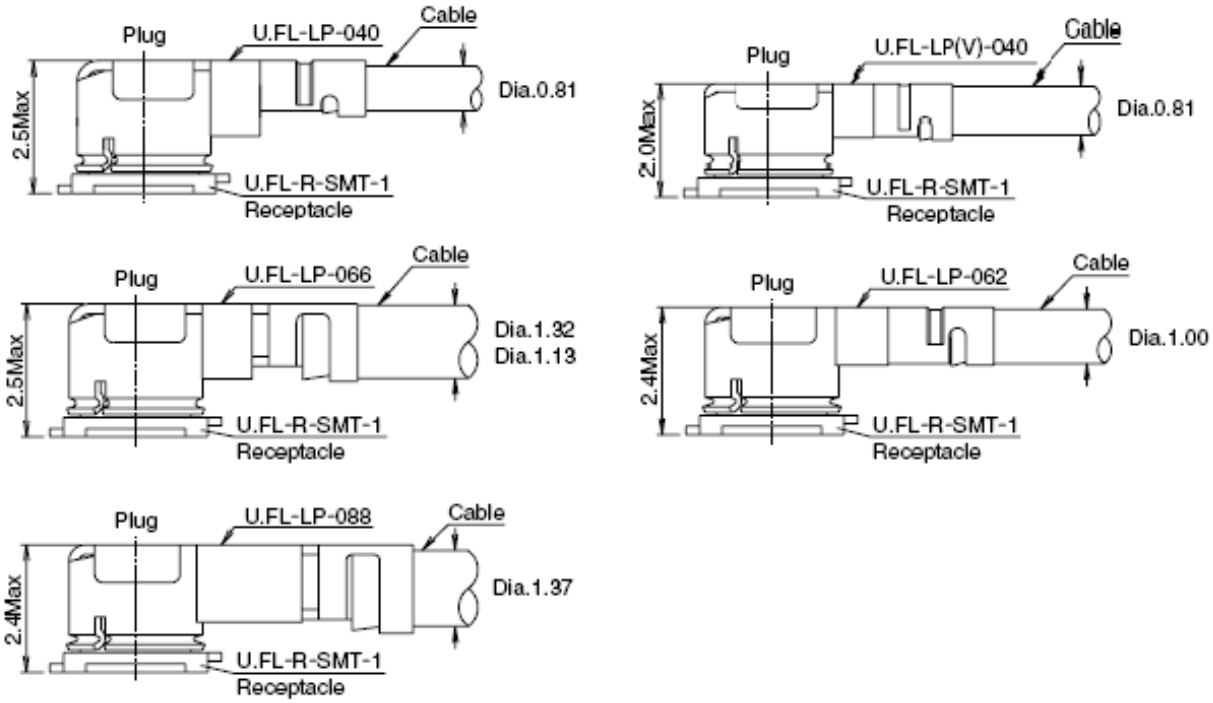


Figure 42: Space Factor of Mated Connector (Unit: mm)

For more details, please visit https://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 43: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0.3	VBAT_BB	V
Voltage at ADC1	0.3	VBAT_BB	V
Voltage at ADC2	0.1	1.7	V

6.2. Power Supply Ratings

Table 44: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

Table 45: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

Table 46: Current Consumption of AG35-CEN-Quecopen Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.2	mA
		GSM DRX=2 (USB disconnected)	2.2	mA
		GSM DRX=5 (USB disconnected)	1.7	mA
		GSM DRX=9 (USB disconnected)	1.6	mA
		WCDMA PF=64 (USB disconnected)	2.1	mA
		WCDMA PF=128 (USB disconnected)	1.6	mA
		WCDMA PF=512 (USB disconnected)	1.4	mA
		LTE-FDD PF=64 (USB disconnected)	2.2	mA
		LTE-FDD PF=128 (USB disconnected)	1.9	mA
		LTE-FDD PF=256 (USB disconnected)	1.5	mA
		LTE-TDD PF=64 (USB disconnected)	2.5	mA
		LTE-TDD PF=128 (USB disconnected)	1.9	mA
		LTE-TDD PF=256 (USB disconnected)	1.7	mA
	Idle state	GSM DRX=5 (USB connected)	29	mA
		GSM DRX=5 (USB disconnected)	19	mA
		WCDMA PF=64 (USB connected)	28	mA
		WCDMA PF=64 (USB disconnected)	18.4	mA
		LTE-FDD PF=64 (USB connected)	28.5	mA
		LTE-FDD PF=64 (USB disconnected)	18.9	mA
		LTE-TDD PF=64 (USB connected)	28.5	mA
		LTE-TDD PF=64 (USB disconnected)	18.3	mA

	GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @32.67dBm	240.55	mA
		EGSM900 3DL/2UL @32.55dBm	408.24	mA
		EGSM900 2DL/3UL @30.65dBm	484.39	mA
		EGSM900 1DL/4UL @29.43dBm	561.25	mA
		DCS1800 4DL/1UL @29.75dBm	167.89	mA
		DCS1800 3DL/2UL @29.66dBm	269.48	mA
		DCS1800 2DL/3UL @29.53dBm	368.02	mA
		DCS1800 1DL/4UL @29.38dBm	468.22	mA
	EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @27.42dBm	165.47	mA
		EGSM900 3DL/2UL @27.26dBm	263.20	mA
		EGSM900 2DL/3UL @27.14dBm	356.80	mA
		EGSM900 1DL/4UL @26.96dBm	452.79	mA
		DCS1800 4DL/1UL @27.00dBm	148.27	mA
		DCS1800 3DL/2UL @26.88dBm	230.03	mA
		DCS1800 2DL/3UL @26.73dBm	309.87	mA
		DCS1800 1DL/4UL @26.63dBm	393.00	mA
	EVDO/CDMA data transfer (GNSS OFF)	BC0 (Max Power) @24.69dBm	544.63	mA
	TD-SCDMA data transfer (GNSS OFF)	B34 (Max Power) @23.08dBm	129.64	mA
		B39 (Max Power) @23.17dBm	131.14	mA
	WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA (max power) @21.92dBm	528.43	mA
		WCDMA B8 HSDPA (max power) @22.72dBm	524.75	mA
		WCDMA B1 HSUPA (max power) @21.25dBm	501.26	mA
		WCDMA B8 HSUPA (max power) @21.64dBm	486.28	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.15dBm	691.68	mA
		LTE-FDD B3 @23.01dBm	748.72	mA

		LTE-FDD B5 @23.16dBm	633.65	mA
		LTE-FDD B8 @22.35dBm	552.74	mA
		LTE-TDD B34 @23.62dBm	342.68	mA
		LTE-TDD B38 @23.6dBm	470.22	mA
		LTE-TDD B39 @23.55dBm	345.04	mA
		LTE-TDD B40 @23.71dBm	488.58	mA
		LTE-TDD B41 @23.53dBm	484.02	mA
	GSM voice call	EGSM900, PCL=5 @32.79dBm	240.47	mA
		EGSM900, PCL=12 @19.62dBm	107.25	mA
		EGSM900, PCL=19 @5.72dBm	76.08	mA
		DCS1800, PCL=0 @29.89dBm	163.25	mA
		DCS1800, PCL=7 @16.98dBm	118.82	mA
		DCS1800, PCL=15 @0.68dBm	98.78	mA
	EVDO/CDMA voice call	BC0 @24.35dBm	628.35	mA
		BC0 @-59.72dBm	118.36	mA
	WCDMA voice call	WCDMA B1 @22.97dBm	637.43	mA
		WCDMA B8 @23.02dBm	542.73	mA

Table 47: GNSS Current Consumption of AG35-CEN-Quecopen Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold Start @Passive Antenna	50.5	mA
		Hot Start @Passive Antenna	49.7	mA
		Lost State @Passive Antenna	49.8	mA
	Tracking (**AT+CFUN=0**)	Open Sky @Passive Antenna	28.8	mA

6.5. RF Output Power

The following table shows the RF output power of AG35-CEN-Quecopen module.

Table 48: RF Output Power

Frequency	Max.	Min.
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0	24dBm+2/-1dB	<-49dBm
TD-SCDMA B34	24dBm+1/-3dB	<-49dBm
TD-SCDMA B39	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-TDD B34	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 2.5dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

Table 49: AG35-CEN-Quecopen RF Receiving Sensitivity

	Receive Sensitivity (Typ.)			
Frequency	**Primary**	**Diversity**	**SIMO**	**3GPP (SIMO)**
EGSM900	-109dBm	/	/	-102dBm
DCS1800	-109dBm	/	/	-102dBm
WCDMA B1	-109.6dBm	-110dBm	-112dBm	-106.7dBm
WCDMA B8	-109.8dBm	-110dBm	-112dBm	-103.7dBm
EVDO/CDMA BC0	-109dBm	/	/	-104dBm
TD-SCDMA B34	-109.1dBm	/	/	-108dBm
TD-SCDMA B39	-109.5dBm	/	/	-108dBm
LTE-FDD B1 (10M)	-98dBm	-99dBm	-102dBm	-96.3dBm
LTE-FDD B3 (10M)	-98.6dBm	-99dBm	-102dBm	-93.3dBm
LTE-FDD B5 (10M)	-98.5dBm	-100dBm	-102.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-98.5dBm	-100dBm	-102.1dBm	-93.3dBm
LTE-TDD B34 (10M)	-98.1dBm	-99dBm	-101.7dBm	-96.3dBm
LTE-TDD B38 (10M)	-98.5dBm	-98dBm	-101dBm	-94.3dBm
LTE-TDD B39 (10M)	-98.4dBm	-99dBm	-102dBm	-96.3dBm
LTE-TDD B40 (10M)	-98.3dBm	-99dBm	-101.5dBm	-96.3dBm
LTE-TDD B41 (10M)	-97.6dBm	-98dBm	-100.5dBm	-94.3dBm

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and

packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 50: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation. Through-holes will create better heat dissipation performance.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

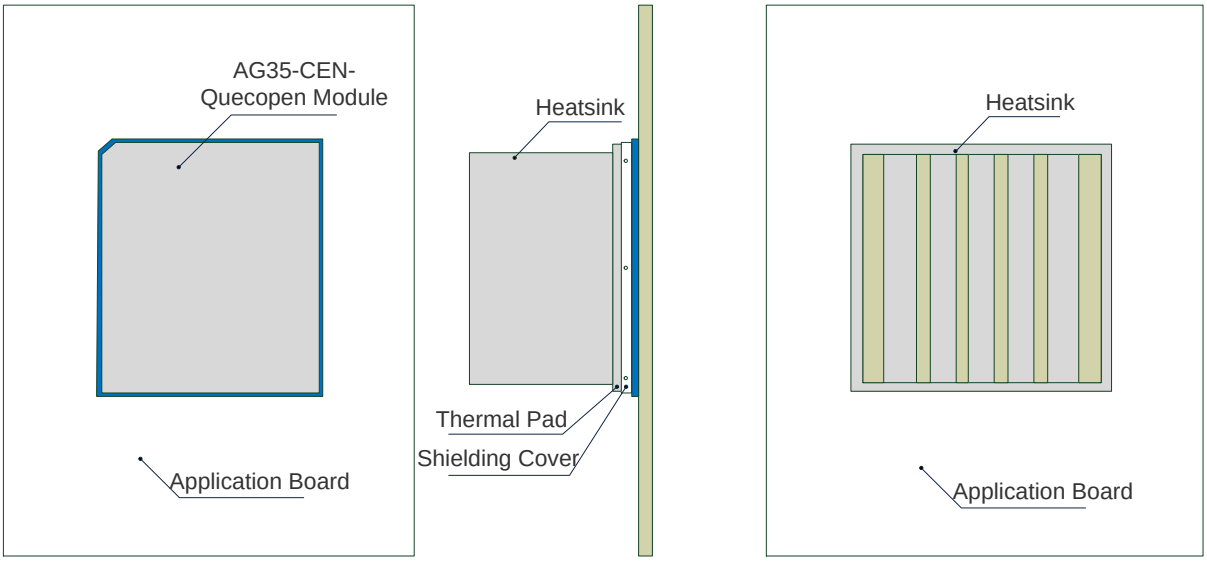


Figure 43: Referenced Heatsink Design (Heatsink at the Top of the Module)

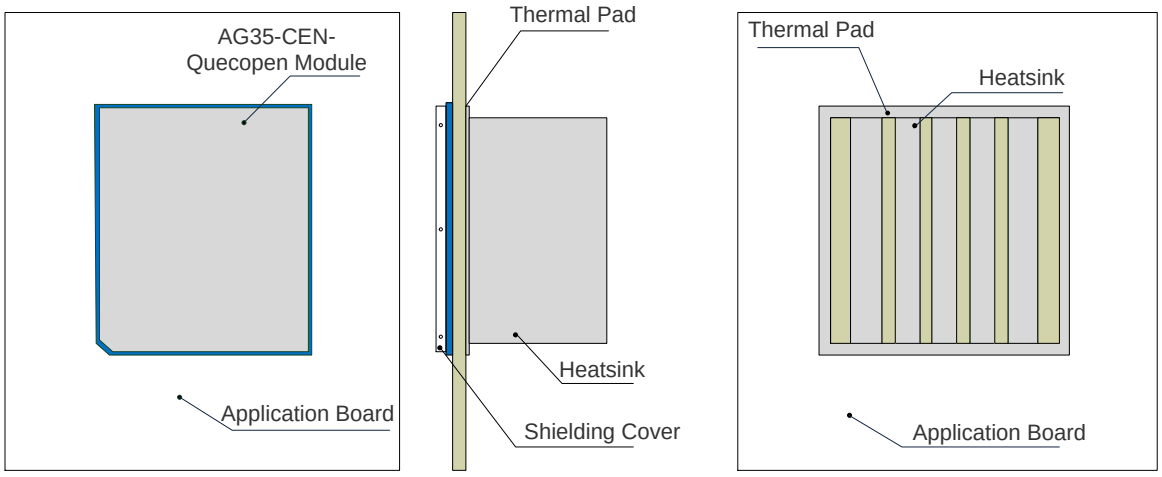


Figure 44: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTES

1. The module offers the better performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.
2. For more information about thermal consideration, please refer to ***document [8]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

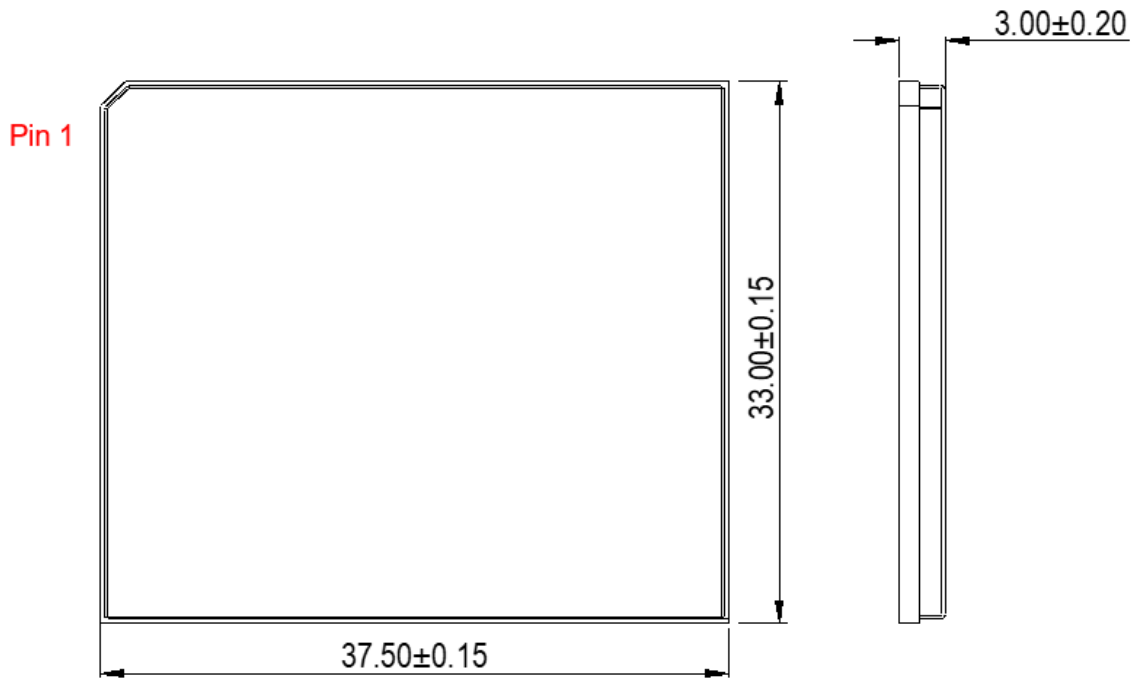


Figure 45: Module Top and Side Dimensions

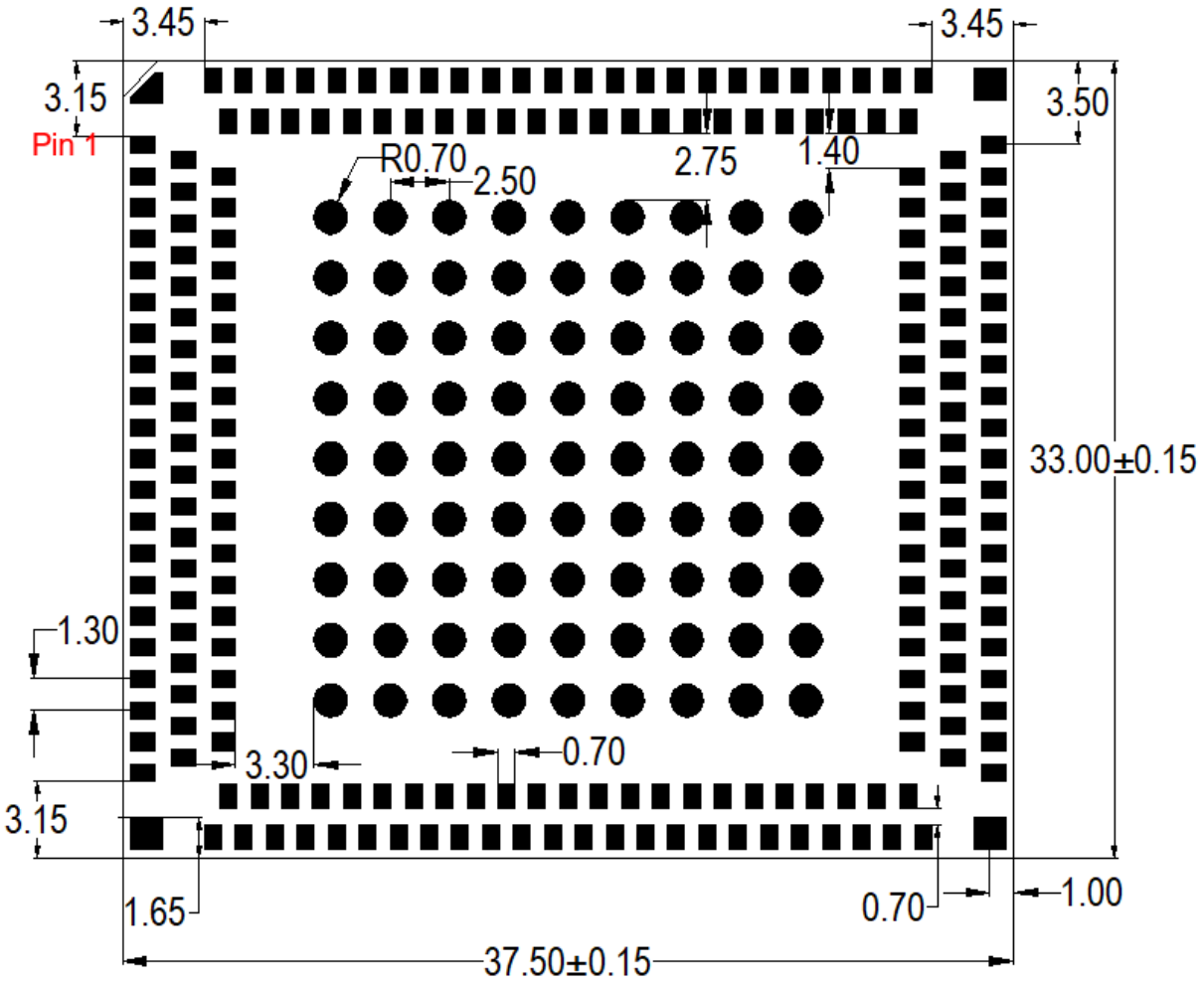


Figure 46: Module Bottom Dimensions (Top View)

7.2. Recommended Footprint

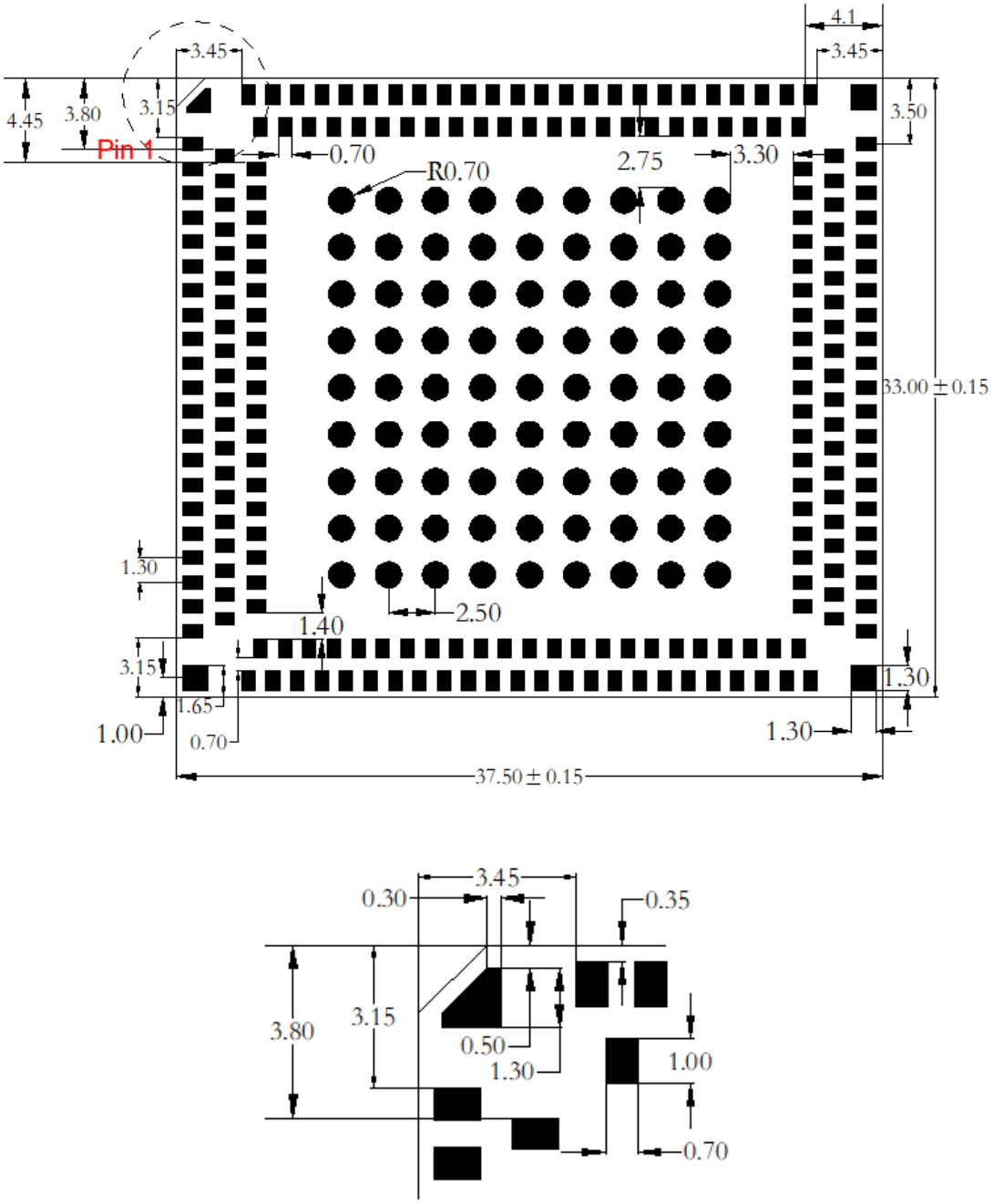


Figure 47: Recommended Footprint (Top View)

NOTE

For convenient maintenance of the module, please keep about 3mm between the module and other components on the host PCB.

7.3. Design Effect Drawings of the Module

Figure 48: Top View of the Module

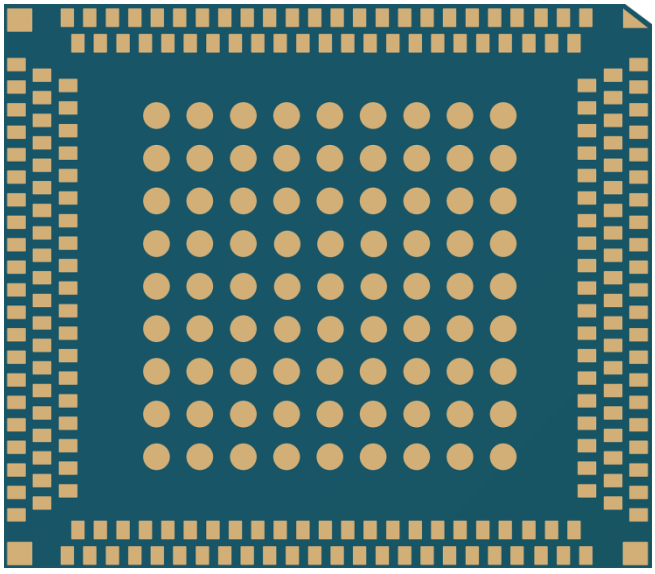


Figure 49: Bottom View of the Module

NOTE

These are renderings of AG35-CEN-Quecopen module. For authentic appearance, please refer to the module that you receive from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

AG35-CEN-Quecopen is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstance below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic container cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13mm~0.15mm. For more details, please refer to ***document [7]***.

It is suggested that the peak reflow temperature is 238~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

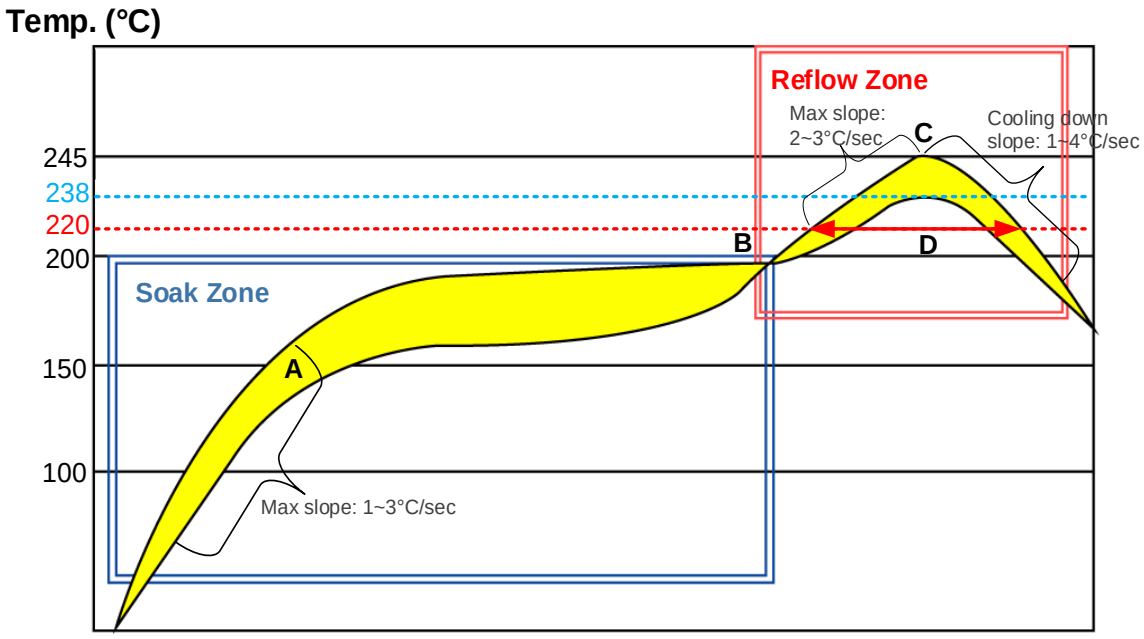


Figure 50: Recommended Reflow Soldering Thermal Profile

Table 51: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

AG35-CEN-Quecopen is packaged in tape and reel carriers. One reel is 10.56 meters long and contains 220 modules. The figures below show the packaging details, measured in mm.

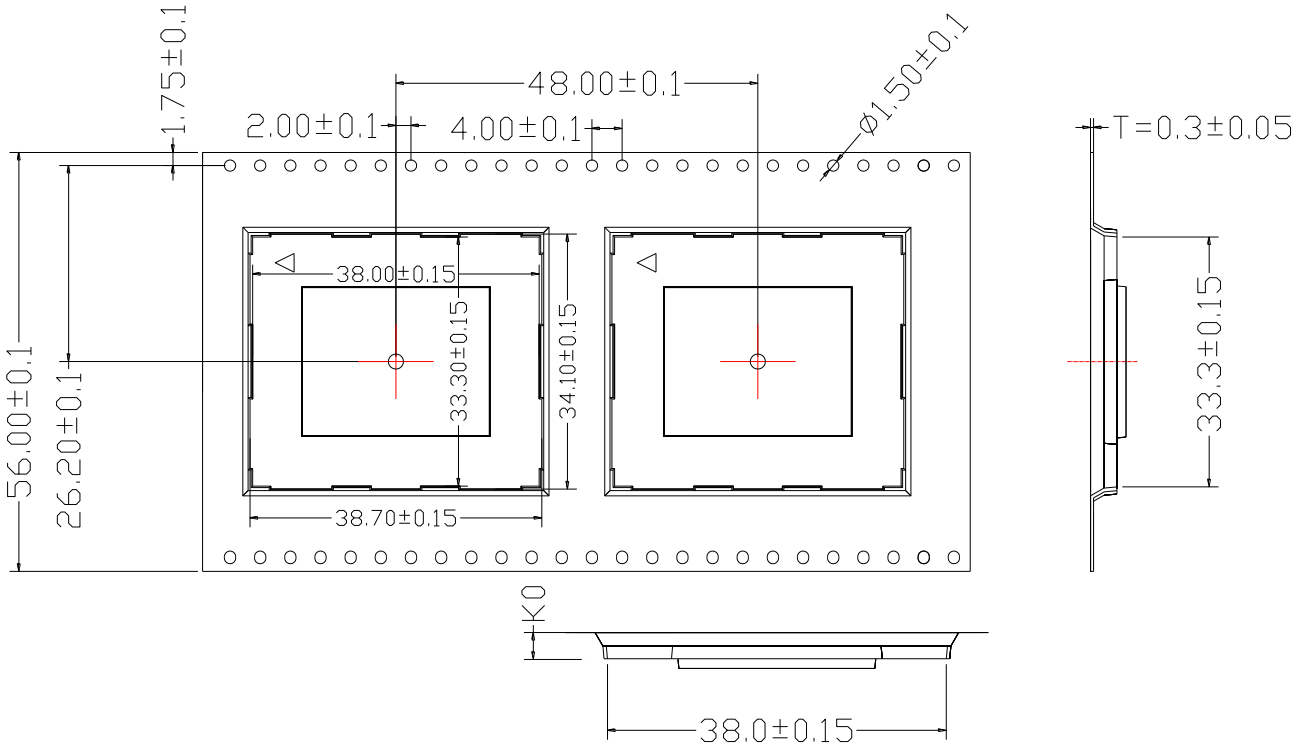


Figure 51: Tape Specifications

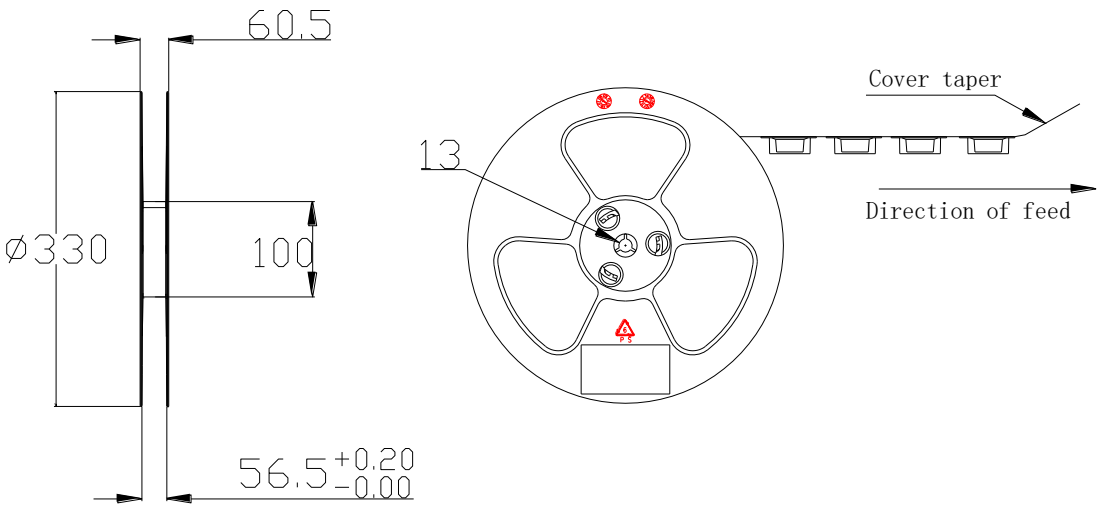


Figure 52: Reel Specifications

9 Appendix A References

Table 52: Related Documents

SN	Document Name	Remark
[1]	Quectel_LTE_OPEN_EVB_User_Guide	EVB User Guide for LTE Quecopen Modules
[2]	Quectel_AG35_Power_Management_Application_Note	AG35 Power Management Application Note
[3]	Quectel_AG35_AT_Commands_Manual	AG35 AT Commands Manual
[4]	Quectel_AG35_GNSS_AT_Commands_Manual	AG35 GNSS AT Commands Manual
[5]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[6]	Quectel_AG35-Quecopen_Developer_Guide	AG35-Quecopen Developer Guide
[7]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[8]	Quectel_AG35-Quecopen_Reference_Design	Quectel_AG35-Quecopen_Reference_Design

Table 53: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
API	Application Program Interface
bps	Bits Per Second
BT	Bluetooth
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data

CTS	Clear to Send
DDR	Double Data Rate
DRX	Discontinuous Reception
DCE	Data Communications Equipment (typically the module)
DTE	Data Terminal Equipment (typically the computer, external controller)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)
ESD	Electrostatic Discharge
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
ME	Mobile Equipment
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel

PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame
Ppp	Peak Pulse Power
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square (value)
Rx	Receive
SMS	Short Message Service
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value

$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
V_{RWM}	Reserve Stand-Off Voltage
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
VSWR	Voltage Standing Wave Ratio

10 Appendix B GPRS Coding Schemes

Table 54: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 55: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 56: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps