Build a Smarter World

EC25-Quecopen

Hardware Design

LTE Module Series

Rev. EC25-Quecopen_Hardware_Design_V1.2

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About the Document

History

Revision	Date	Author	Description
1.0	2017-02-23	Lorry XU	Initial
1.1	2019-01-08	Woody WU/ Frank WANG	1. Added variant EC25-E-Quecopen and EC25-A-Quecopen of EC25-Quecopen and related contents 2. Deleted related contents of GSM800 and PCS1900 3. Updated key features of the module (Table 2) 4. Updated functional diagram (Figure 1) 5. Updated pin description (Table 4) 6. Added multiplexing pin functions of the module (Table 5) 7. Updated pull-up/pull-down resistance of GPIOs (Table 6) 8. Deleted main UART sleep application 9. Updated PWRKEY pull-down time as 500ms (Chapter 3.7.1 and Figure 9) 10. Updated the description of (U)SIM interface (Chapter 3.8) 11. Updated the description of USB interface (Chapter 3.9) 12. Updated the description of UART interface (Chapter 3.10) 13. Updated description of PCM and I2C interfaces (Chapter 3.11) 14. Updated the description of SD card interface (Chapter 3.12) 15. Added SGMII interface (Chapter

			3.15) and related contents 16. Updated pin definition of NET_STATUS (Chapter 3.17) 17. Added USB_BOOT timing sequence (Chapter 3.19) 18. Added current consumption of EC25-E/EC25-A-Quecopen (Chapter 6.4) 19. Added description of thermal consideration (Chapter 6.8) 20. Updated module operating frequencies (Table 34) 21. Updated GNSS frequency (Table 36) 22. Updated antenna requirements (Table 37) 23. Updated RF output power (Table 44) Updated reference circuit of GNSS antenna (Figure 38) 24. Added RF receiving sensitivity of EC25-E/EC25-A-Quecopen (Chapter 6.6)
1.2	2019-01-09	Woody WU/ Frank WANG	1. Modified NOTES in Chapter 3.7.1 and 3.19 2. Deleted NOTES in Chapter 3.12 and 3.13

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1 Introduction

This document defines EC25-Quecopen module and describes its air interfaces and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC25-Quecopen module. To facilitate its application in different fields, relevant reference design is also provided for customers' reference. Associated with application note and user guide, customers can use EC25-Quecopen module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC25-Quecopen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

Quecopen® is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of Quecopen® solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With Quecopen® solution, development flow for wireless application and hardware design will be simplified. Main features of Quecopen® solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware wirelessly
- Improves products' cost-performance ratio, and enhances products' competitiveness

EC25-Quecopen module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.2GHz. Customers can use EC25-Quecopen module as the basis for development of Quecopen® applications.

EC25-Quecopen is a series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity, and provides data connectivity on LTE-FDD, LTE-TDD, DC-HSPA+, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS [1)] and voice [2)] functionalities for customers' specific application. The following table shows the frequency bands of EC25-Quecopen series module.

Table 1: Frequency Bands of EC25-Quecopen Series Module

Module	LTE Bands	WCDMA Bands	GSM Bands	Rx-diversity	GNSS [1)]
EC25-E	FDD: B1/B3/B5/B7/B8/B20 TDD: B38/B40/B41	B1/B5/B8	900/1800MHz	Y	GPS, GLONASS, BeiDou/ Compass, Galileo,
EC25-A	FDD: B2/B4/B12	B2/B4/B5	N	Y	

	QZSS

NOTES

1. [1] GNSS function is optional.
2. [2] EC25-Quecopen series module includes **Data-only** and **Telematics** versions. **Data-only** version does not support voice function, while **Telematics** version supports it.

With a compact profile of 29.0mm × 32.0mm × 2.4mm, EC25-Quecopen can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC25-Quecopen is an SMD type module which can be embedded into applications through its 144-pin pads, including 80 LCC signal pads and 64 LGA signal pads.

2.2. Key Features

The following table describes the detailed features of EC25-Quecopen module.

Table 2: Key Features of EC25-Quecopen Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 4 FDD and TDD Support 1.4MHz~20MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max 150Mbps (DL), Max 50Mbps (UL) LTE-TDD: Max 130Mbps (DL), Max 30Mbps (UL)
WCDMA Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42Mbps (DL)

	HSUPA: Max 5.76Mbps (UL) WCDMA: Max 384Kbps (DL), Max 384Kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL), Max 85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL), Max 236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/NITZ/CMUX*/HTTPS*/SMTP/MMS*/FTPS*/SMTPS*/SSL*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU modes Point to point MO and MT SMS cell broadcast SMS storage: ME by default
GPIO Interfaces	Support 24 GPIOs that can be used for input and output, and 4 PMU GPIOs that can only be used for output
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (not support OTG); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging, firmware upgrade and voice over USB* Support USB serial drivers for: Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.x/7.x/8.x, etc.
UART Interface	**Main UART:** Used for AT command communication only

	Baud rates reach up to 3000000bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console, log output 115200bps baud rate **UART1 (Multiplexed with SPI):** Used for application UART Baud rates reach up to 3000000bps, 115200bps by default Support RTS and CTS hardware flow control **UART2 (Multiplexed with SDC1_DATA[3:0]):** Used for application UART Baud rates reach up to 3000000bps, 115200bps by default Support RTS and CTS hardware flow control **UART3 (Multiplexed with SDC1_CLK&CMD):** Used for application UART Baud rates reach up to 3000000bps, 115200bps by default
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	Support 10M/100M/1000M Ethernet work mode Support maximum 150Mbps (DL)/50Mbps (UL) for 4G network
ADC Interfaces	Two ADC interfaces
SPI Interface	Support master mode only Maximum clock frequency rate: 50MHz
I2C Interface	Compliant with I2C specification 5.0 Multi-master is not supported
WLAN Interface	Compliant with IEEE 802.11 standard Support SDIO 3.0 protocol
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C-Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NET_STATUS is used to indicate network connectivity status
Antenna Interfaces	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (29.0±0.15)mm × (32.0±0.15)mm × (2.4±0.2)mm Weight: approx. 4.9g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface or DFOTA*

RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC25-Quecopen and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

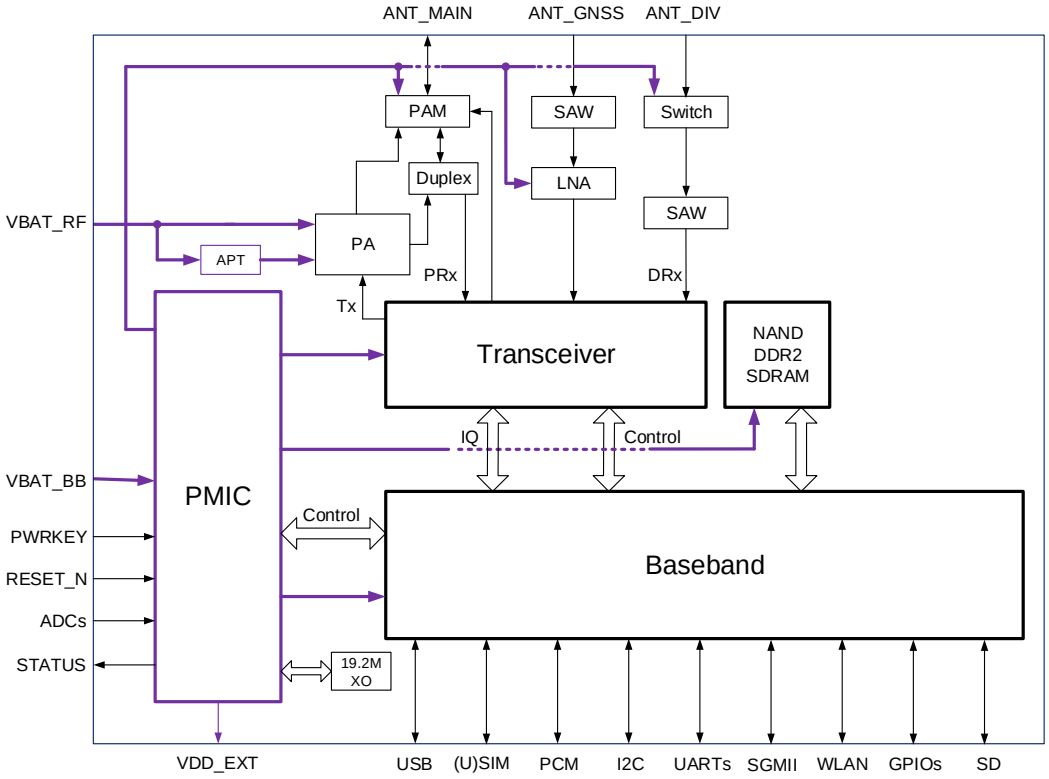


Figure 1: Functional Diagram

2.4. Evaluation Board

Quectel provides a complete set of evaluation tools to facilitate the use and testing of EC25-Quecopen module. The evaluation tool kit includes the evaluation board (EVB), USB data cable, earphone, antenna and other peripherals.

3 Application Interfaces

3.1. General Description

EC25-Quecopen is equipped with 80-pin LCC pads plus 64-pin LGA pads. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- SPI interface
- WLAN interface
- SGMII Interface
- ADC interfaces
- Status indication
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC25-Quecopen module.

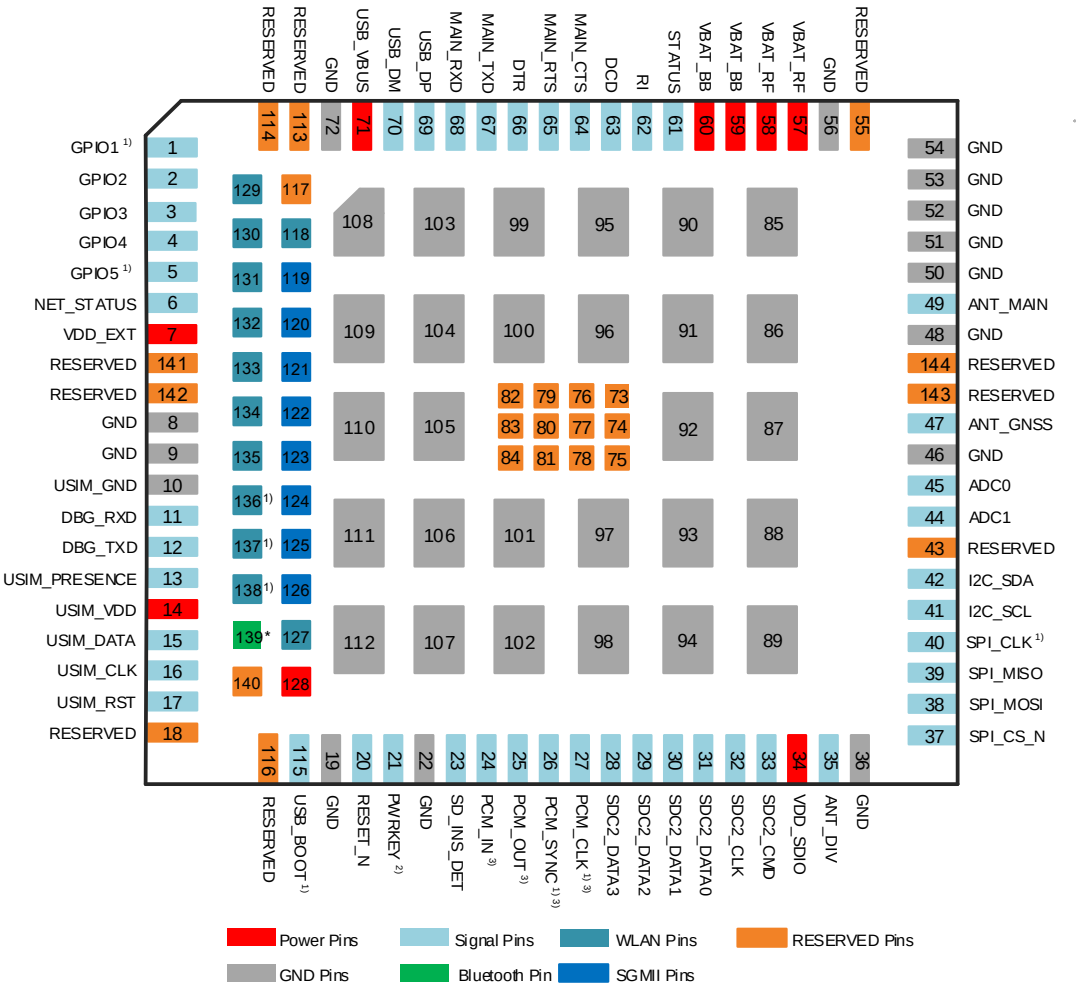


Figure 2: Pin Assignment (Top View)

NOTES

1. 1) means these pins cannot be pulled up to high level, even to VDD_EXT before startup.
2. 2) PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. 3) means these interface functions are only supported on **Telematics** version.
4. Pads 118, 127 and 129~138 are WLAN interface pins.
5. Pads 119~126 and 128 are SGMII interface pins.
6. Keep all RESERVED pins and unused pins unconnected.
7. GND pads 85~112 should be connected to ground in the design, and RESERVED pads 73~84 should not be designed in schematic and PCB decal.

8. "*" means under development.

3.3. Pin Description

The following tables show the pin definition, multiplexing function and GPIO pull-up/down resistance of EC25-Quecopen module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
BH	High-voltage tolerant bidirectional digital with CMOS input
DI	Digital input
DO	Digital output
H	High level
IO	Bidirectional
L	Low level
OD	Open drain
PD	Pull down
PI	Power input
PO	Power output
PU	Pull up

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	20	DI	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pull-up to 1.8V internally. Active low. If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module operating status	The drive current should be less than 0.9mA.	An external pull-up resistor is required. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module network activity	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it

			status		open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	PI	USB power supply, used for USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	Typical: 5.0V If unused, keep it open.
USB_DP	69	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω. If unused, keep it open.
USB_DM	70	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM_VDD	14	PO	Power supply for (U)SIM card	**For 1.8V (U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V (U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	16	DO	Clock signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V	

				For 3.0V (U)SIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	17	DO	Reset signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DCD	63	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready, sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
MAIN_CTS	64	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
MAIN_TXD	67	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V	1.8V power domain. If unused, keep it open.

				V_{IH}max=2.0V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	11	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	44	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.

PCM_CLK	27	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock. Used for external codec.		An external pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data. Used for external codec.		An external pull-up resistor is required. 1.8V only. If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_ DATA3	28	IO	SD card SDIO bus DATA3	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_ DATA2	29	IO	SD card SDIO bus DATA2	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V	

				V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V
SDC2_CLK	32	DO	SD card SDIO bus clock	**1.8V signaling:** V_{OL}max=0.45V

				V_{OH}min=1.4V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V	
SDC2_CMD	33	IO	SD card SDIO bus command	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	
SD_INS_DET	23	DI	SD card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull-up power	$I_O$max=50mA	1.8V/2.85V configurable. Cannot be used for SD card power. If unused, keep it open.
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS_N	37	DO	SPI chip selection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MOSI	38	DO	SPI master out slave in	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MISO	39	DI	SPI master in slave out	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

SPI_CLK	40	DO	SPI serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
PM_ENABLE	127	DO	WLAN power control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. If unused, keep it open.
SDC1_DATA3	129	IO	WLAN SDIO bus DATA3	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA2	130	IO	WLAN SDIO bus DATA2	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA1	131	IO	WLAN SDIO bus DATA1	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA0	132	IO	WLAN SDIO bus DATA0	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_CLK	133	DO	WLAN SDIO bus clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.

SDC1_CMD	134	DO	WLAN SDIO bus command	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
WLAN_WAKE	135	DI	WLAN wake up the host	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active low. If unused, keep it open.
WLAN_EN	136	DO	WLAN enable	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.
COEX_UART_RX	137	DI	LTE/WLAN coexistence signal	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.
COEX_UART_TX	138	DO	LTE/WLAN coexistence signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Cannot be pulled up to high level, even to VDD_EXT before startup. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	Description	**DC Characteristics**	**Comment**
EPHY_RST_N	119	DO	Ethernet PHY reset	**For 1.8V:** V_{OL}max=0.45V V_{OH}min=1.4V **For 2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	**For 1.8V:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **For 2.85V:** V_{IL}max=0.71V V_{IH}min=1.78V V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. Require external pull-up to USIM2_VDD, and the resistor should be 1.5K. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII MDIO clock	**For 1.8V:** V_{OL}max=0.45V V_{OH}min=1.4V **For 2.85V:** V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmission - minus		If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission - plus		If unused, keep it open.
SGMII_RX_P	125	AI	SGMII receiving - plus		If unused, keep it open.
SGMII_RX_M	126	AI	SGMII receiving - minus		If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power source		1.8V/2.85V configurable. If unused, keep it open
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna		50Ω impedance. If unused, keep it open.
ANT_MAIN	49	IO	Main antenna		50Ω impedance
ANT_GNSS	47	AI	GNSS antenna		50Ω impedance. If unused, keep it open.
GPIO Pins					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO1	1	IO	General purpose input/output	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
GPIO2	2	IO	General purpose input/output	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
GPIO3	3	IO	General purpose input/output	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
GPIO4	4	IO	General purpose input/output	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
GPIO5	5	IO	General purpose input/output	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active high. It is recommended to reserve the pin as test point.
BT_EN*	139	DO	BT enabling pin	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.

RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	18, 43, 55, 73~84, 113, 114, 116, 117, 140~144		Reserved		Keep these pins unconnected.

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. "*" means under development.

Table 5: Multiplexing Pin Functions of EC25-Quecopen

Pin Name	Pin No.	Model 1 (Default)	Model 2	Model 3	Reset [1)]	Interrupt [2)]	Comment
GPIO1	1	GPIO_25	--	--	B-PD, L	YES	BOOT_ CONFIG_2
GPIO2	2	GPIO_10	HOST_ WAKE_BT	--	B-PD, L	NO	
GPIO3	3	GPIO_42	BT_WAKE_ HOST	--	B-PD, L	YES	
GPIO4	4	GPIO_11	--	--	B-PU, H	YES	
GPIO5	5	GPIO_24	--	--	B-PD, L	NO	BOOT_ CONFIG_1
USIM_ PRESENCE	13	GPIO_34	USIM_ PRESENCE	--	B-PD, L	YES	
SD_INS_DET	23	SD_INS _DET	GPIO_26	--	B-PD, L	YES	
PCM_IN	24	PCM_IN	GPIO_76	I2S_IN	B-PD, L	YES	
PCM_OUT	25	PCM_ OUT	GPIO_77	I2S_OUT	B-PD, L	NO	
PCM_SYNC	26	PCM_ SYNC	GPIO_79	I2S_WS	B-PD, L	YES	BOOT_ CONFIG_7
PCM_CLK	27	PCM_CLK	GPIO_78	I2S_CLK	B-PD, L	NO	BOOT_ CONFIG_8
SPI_CS_N	37	SPI_CS_ N_ BLSP6	GPIO_22	UART_ RTS_	B-PD, L	YES	

				BLSP6			
SPI_MOSI	38	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6	B-PD, L	YES	
SPI_MISO	39	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6	B-PD, L	YES	
SPI_CLK	40	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6	B-PU, H	NO	BOOT_CONFIG_4
I2C_SCL	41	I2C_SCL_BLSP2	GPIO_07	--	B-PD, L	NO	
I2C_SDA	42	I2C_SDA_BLSP2	GPIO_06	--	B-PD, L	NO	
SDC1_DATA3	129	SDC1_DATA3	GPIO_12	UART_TXD_BLSP1	B-PD, L	YES	
SDC1_DATA2	130	SDC1_DATA2	GPIO_13	UART_RXD_BLSP1	B-PD, L	YES	
SDC1_DATA1	131	SDC1_DATA1	GPIO_14	UART_RTS_BLSP1	B-PD, L	NO	
SDC1_DATA0	132	SDC1_DATA0	GPIO_15	UART_CTS_BLSP1	B-PD, L	NO	
SDC1_CLK	133	SDC1_CLK	GPIO_16	UART_TXD_BLSP4	B-NP, L	YES	
SDC1_CMD	134	SDC1_CMD	GPIO_17	UART_RXD_BLSP4	B-PD, L	YES	
WLAN_EN	136	WLAN_EN	GPIO_38	--	B-PD, L	YES	BOOT_CONFIG_12
NET_STATUS	6	NET_STATUS	PMU_GPIO1018	--	B-PD, L	NO	If this pin is used for GPIO purpose, it can only be OUTPUT mode.

WLAN_ SLP_CLK	118	WLAN_ SLP_CLK	PMU_ GPIO1023	--	B-PD, L	NO	If this pin is used for GPIO purpose, it can only be OUTPUT mode.
PM_ENABLE	127	PM_ ENABLE	PMU_ GPIO1020	--	B-PD, L	NO	If this pin is used for GPIO purpose, it can only be OUTPUT mode.
BT_EN*	139	BT_EN*	PMU_ GPIO1019	--	B-PD, L	NO	If this pin is used for GPIO purpose, it can only be OUTPUT mode.

NOTES

1. The pin function in Model 2 and Model 3 takes effect only after software configuration.
2. [1)] Please refer to ***Table 2*** for more details about the symbol description.
3. [2)] YES means this pin can be used as a normal interrupt source or sleep wake-up interrupt source.
4. All BOOT_CONFIG and FORCE_USB_BOOT pins are prohibited to be pulled up to high level, even if pulled up to VDD_EXT before startup.
5. "*" means under development.

Table 6: Pull-up/Pull-down Resistance of GPIOs

Symbol	Description	Pin No.	Min	Typ	Max	Unit
R_P	Pull-up &pull-down resistance	1~2, 4~5, 13, 23~27, 37~42, 129~134, 136	55	100	390	kohm
		3	5	7	50	kohm

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN** command can set the module enter into airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EC25-Quecopen is able to reduce its current consumption to a minimum value during the sleep mode. The following sub-chapters describe power saving procedures of EC25-Quecopen module.

3.5.1.1. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions must be met to let the module enter into the sleep mode.

- Enable the sleep mode by the sleep and wake-up relevant APIs.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

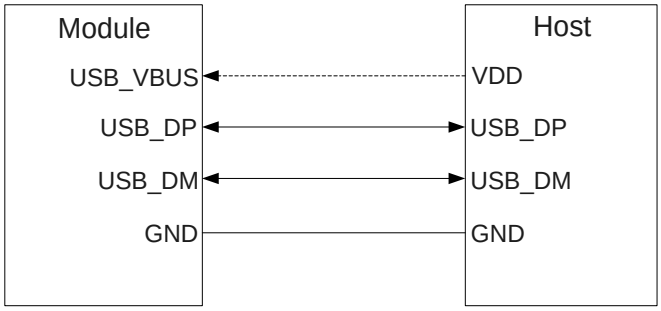


Figure 3: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC25-Quecopen through USB will wake up the module.
- When EC25-Quecopen has URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.2. USB Application without USB Remote Wakeup Function

If the host supports USB suspend/resume, but does not support remote wake-up function, it needs to be woken up via the module's GPIO.

There are three preconditions to let the module enter into the sleep mode.

- Enable the sleep mode by the sleep and wake-up relevant APIs.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

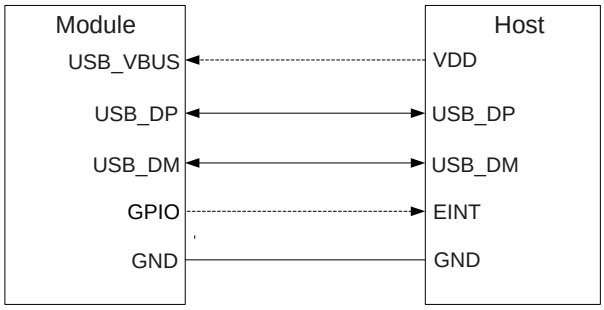


Figure 4: Sleep Mode Application without USB Remote Wakeup

- Sending data to EC25-Quecopen through USB will wake up the module.
- When EC25-Quecopen has URC to report, the module's GPIO signal can be used to wake up the host.

3.5.1.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to let the module enter into sleep mode.

- Enable the sleep mode by the sleep and wake-up relevant APIs.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

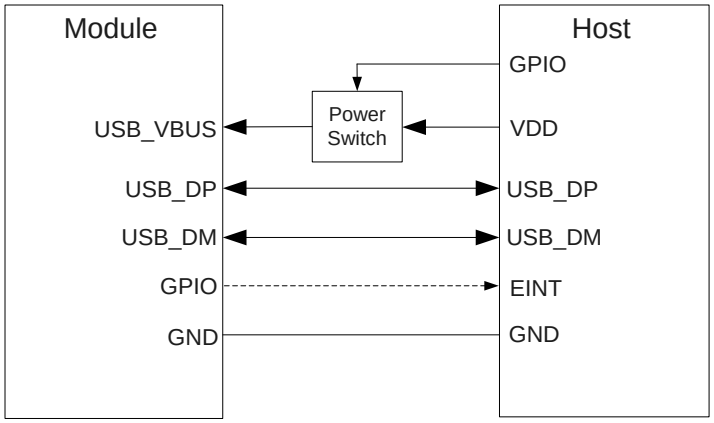


Figure 5: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Refer to ***document [1]*** for more details about the module's power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following way.

AT+CFUN command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EC25-Quecopen provides four VBAT pins dedicated to connect with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module RF part
- Two VBAT_BB pins for module baseband part

The following table shows the details of VBAT pins and ground pins.

Table 8: Pin Definition of VBAT and GND

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

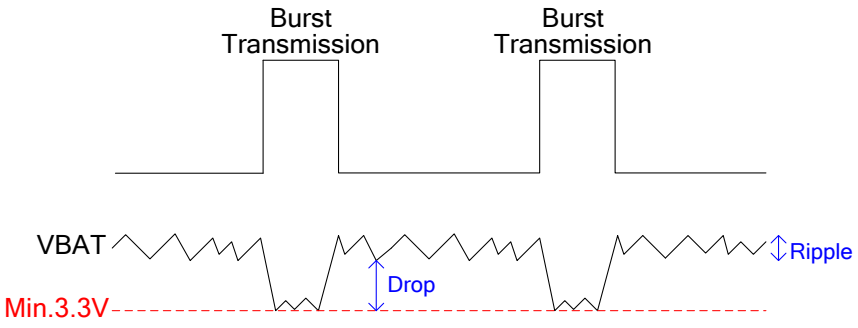


Figure 6: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and ESD, it is suggested that a TVS diode with low reverse stand-off voltage V_{RWM}, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

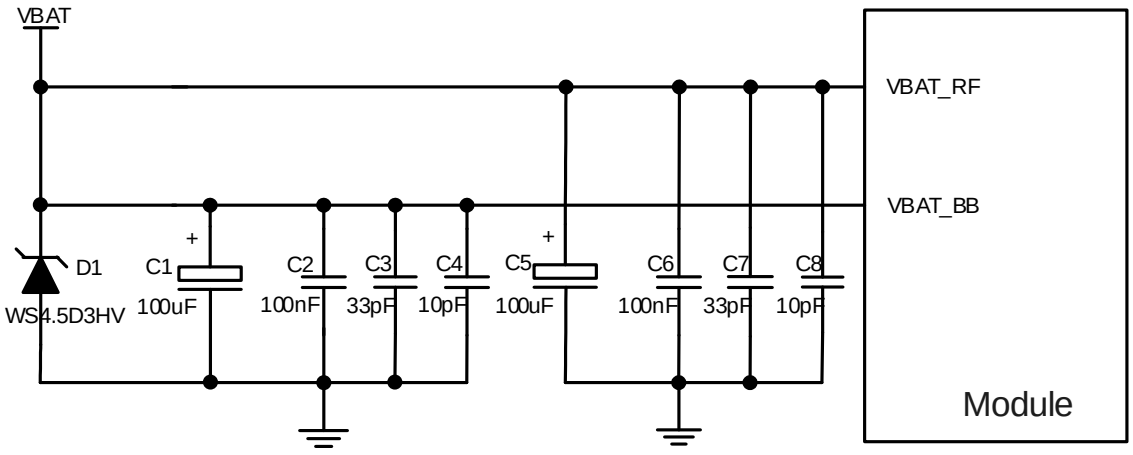


Figure 7: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply

power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3A.

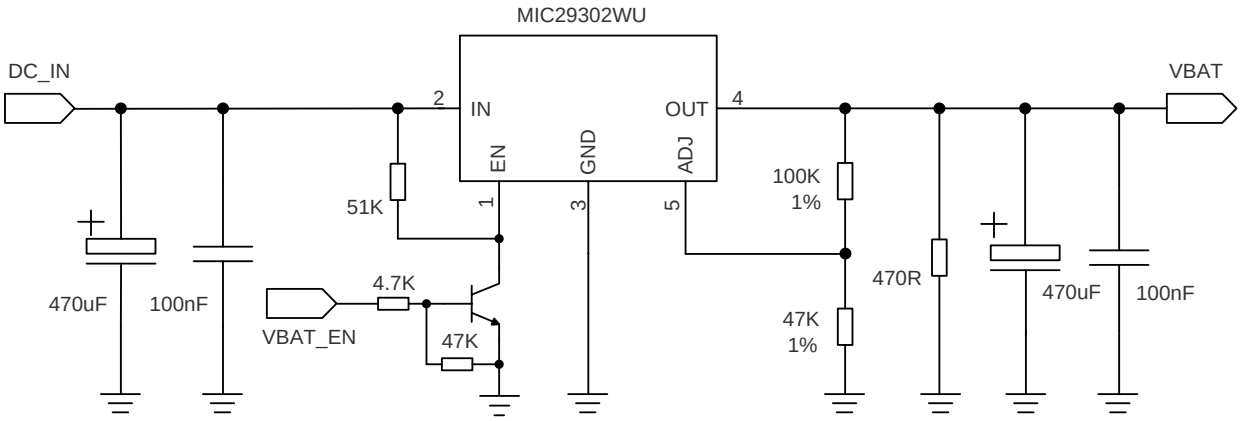


Figure 8: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply

Related software command or API can be used to monitor the VBAT_BB voltage value.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 9: PWRKEY Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EC25-Quecopen is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputs a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

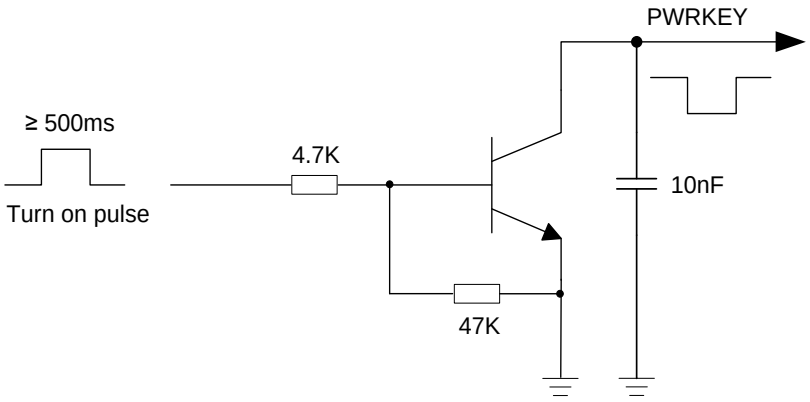


Figure 9: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

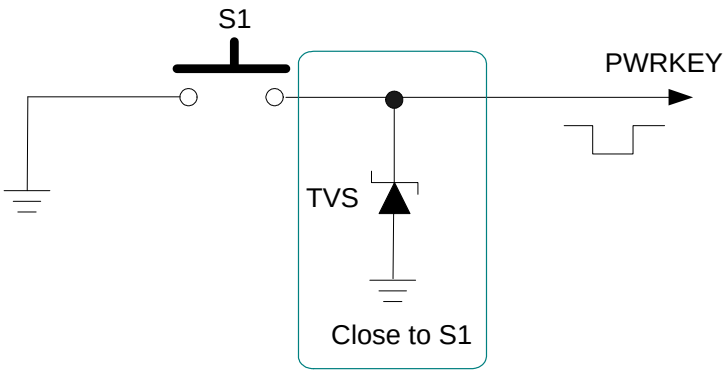


Figure 10: Turn on the Module Using Keystroke

The power-on scenario is illustrated in the following figure.

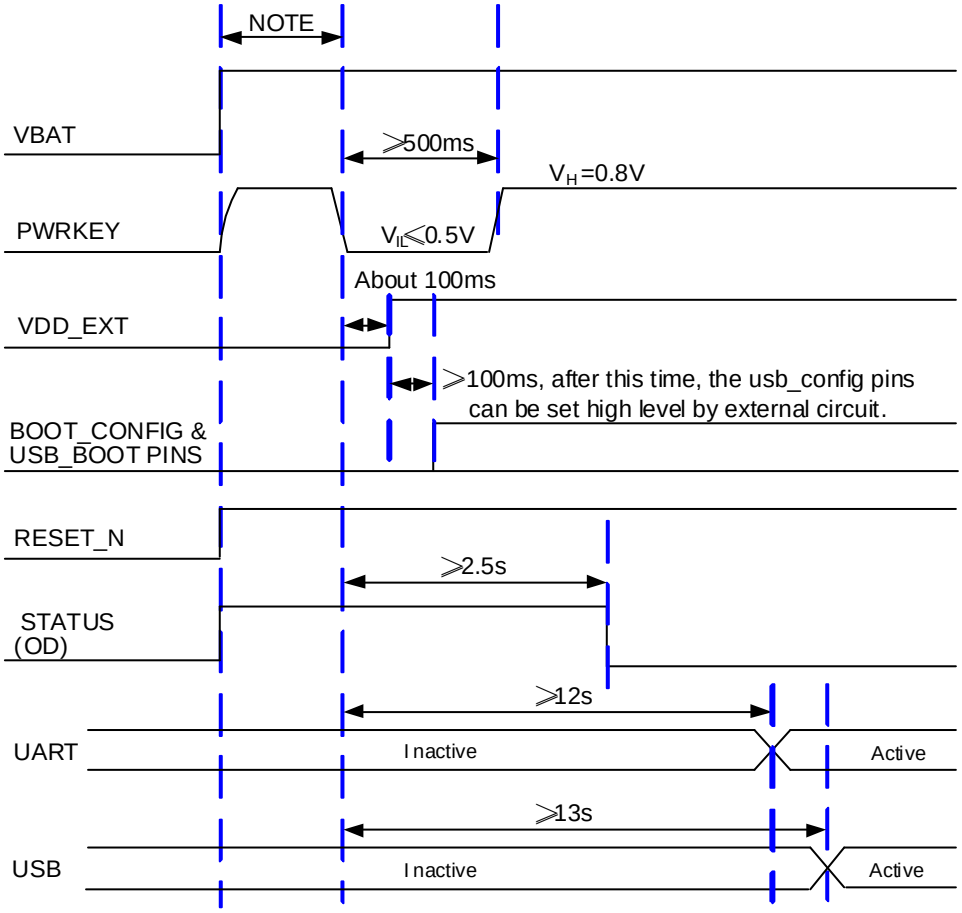


Figure 11: Power-on Scenario

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10K resistor if module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal turn-off procedure: Turn off the module using the PWRKEY pin.
- Normal turn-off procedure: Turn off the module using related software command or API.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-off scenario is illustrated in the following figure.

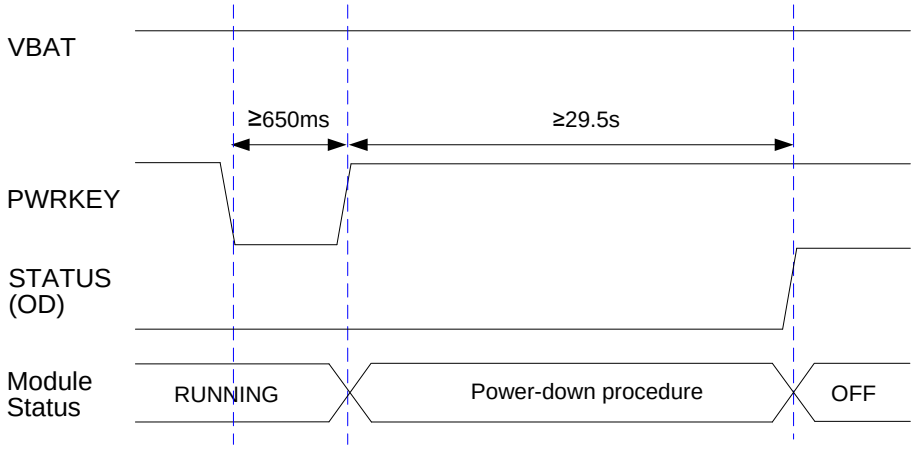


Figure 12: Power-off Scenario

3.7.2.2. Turn off Module Using Related Software Command or API

It is also a safe way to use software command or API interface to turn off the module, which is similar to turning off the module via PWRKEY pin.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY, related software command or API, the power supply can be cut off.
2. When turning off module with related software command or API, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successful turn-off.

3.7.3. Reset The Module

The RESET_N can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for time between 150ms and 460ms.

Table 10: RESET_N Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

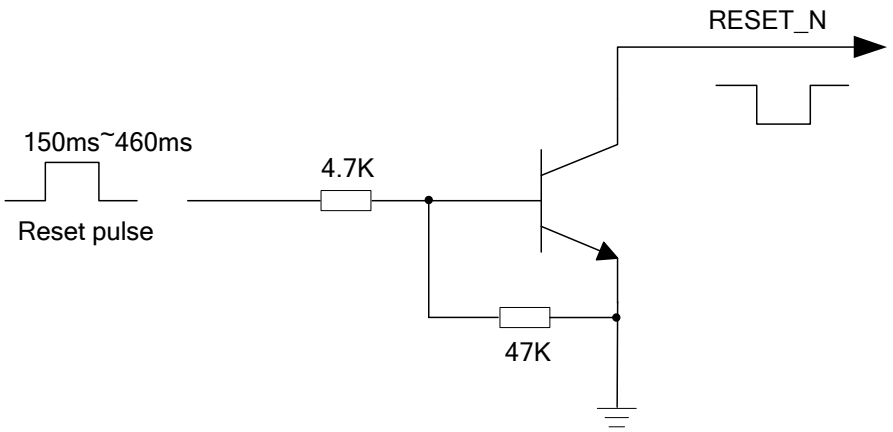


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

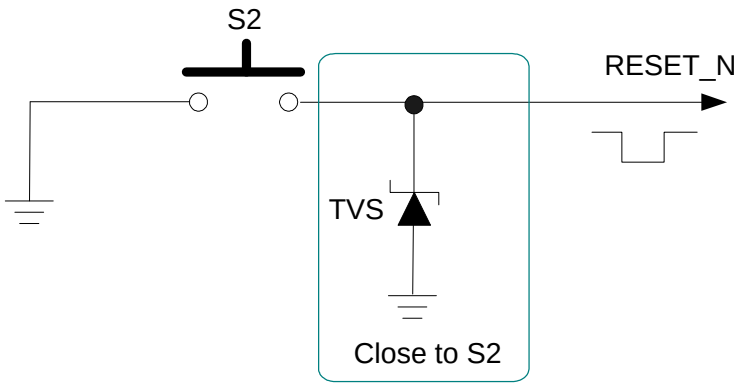


Figure 14: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

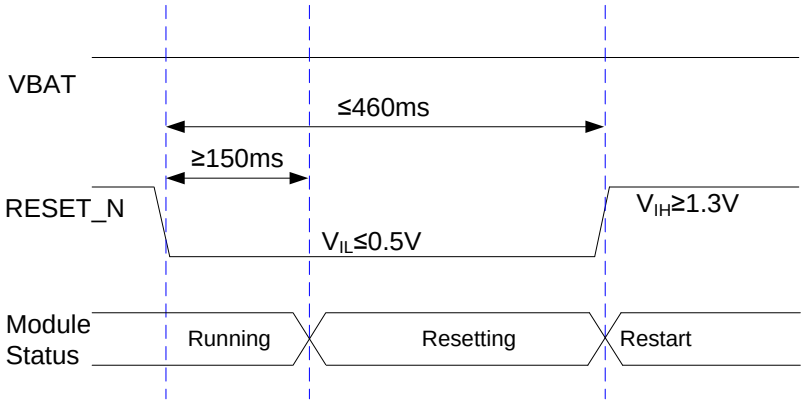


Figure 15: Reset Scenario

NOTES

1. RESET_N is only used when the module fails to be shut down via related software command, API and the PWRKEY pin.
2. Please ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 11: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	
USIM_CLK	16	DO	Clock signal of (U)SIM card	
USIM_RST	17	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	1.8V power domain. If unused, keep it open.
USIM_GND	10		Specified ground for (U)SIM card	

EC25-Quecopen supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command for details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

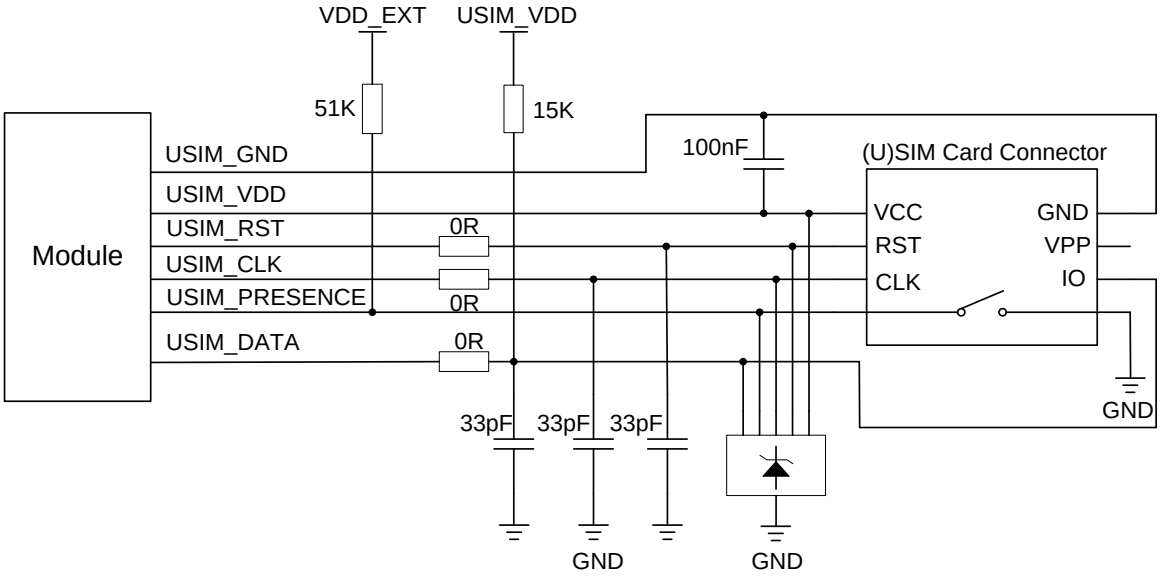


Figure 16: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

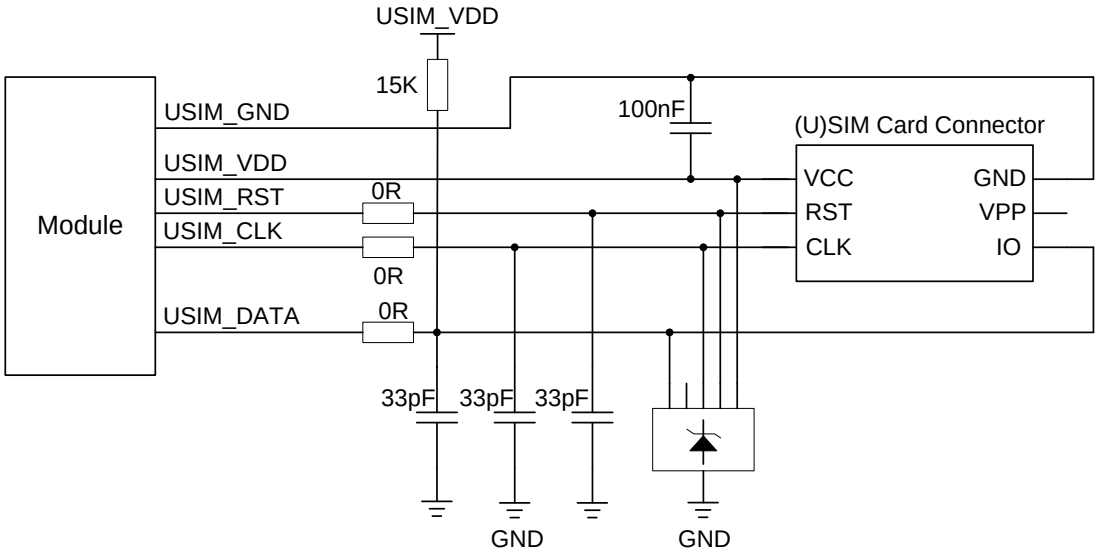


Figure 17: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1uF, and place it as close to (U)SIM card connector as possible. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33pF capacitors are used for filtering interference of GSM900MHz. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

EC25-Quecopen contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for software command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB Signal Part				
USB_DP	69	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	70	IO	USB differential data bus (-)	
USB_VBUS	71	PI	USB connection detection	Typical 5.0V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' design. The following figure shows a reference circuit of USB interface.

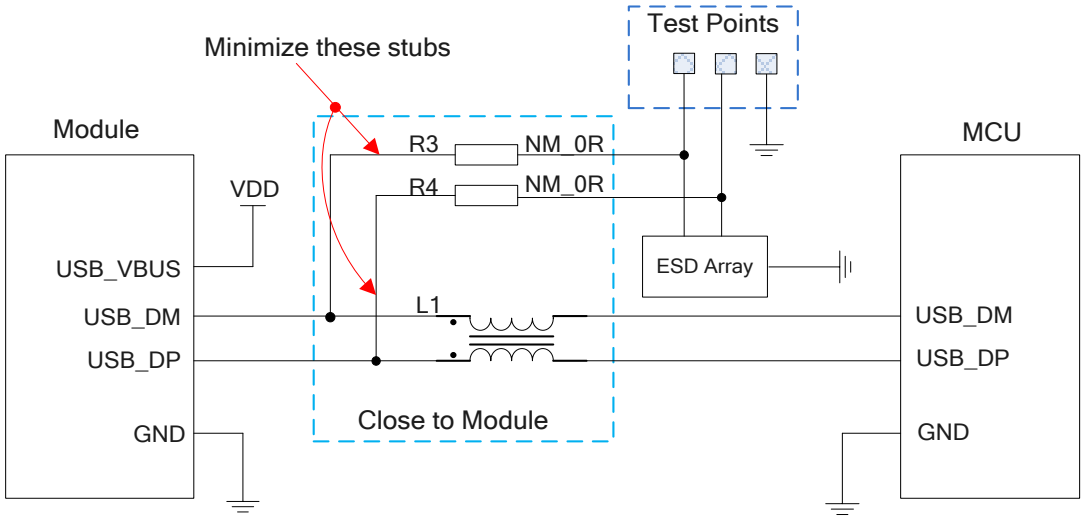


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EC25-Quecopen module's USB interface supports slave and host modes, but does not support OTG mode.
2. "*" means under development.

3.10. UART Interfaces

The module provides five UART interfaces: main UART, debug UART, UART1, UART2 and UART3. UART1, UART2 and UART3 can be used for application UART through API. Main UART, UART1 and UART2 support RTS/CTS, while debug UART and UART3 do not.

The following shows their features.

- The Main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 3000000bps baud rates, and the default is 115200bps. It supports RTS and CTS hardware flow control, and it is used for AT command communication only.
- The Debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.
- The UART1 and UART2 interface support 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 3000000bps baud rates, and the default is 115200bps. They support RTS and CTS hardware flow control, and are used for communication and data transmission with peripherals.
- The UART3 interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 3000000bps baud rates, and the default is 115200bps. It does not support RTS and CTS hardware flow control, and is used for communication and data transmission with peripherals.

The following tables show the pin definition.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Ring indicator	1.8V power domain
DCD	63	DO	Data carrier detection	1.8V power domain
CTS	64	DO	Clear to send	1.8V power domain
MAIN_CTS	64	DO	Clear to send	1.8V power domain

MAIN_RTS	65	DI	Request to send	1.8V power domain
MAIN_TXD	67	DO	Transmit data	1.8V power domain
MAIN_RXD	68	DI	Receive data	1.8V power domain

NOTE

EC25-Quecopen module's main UART is used for AT command communication only, and cannot be used for communication and data transmission with peripherals such as a MCU through API.

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Transmit data	1.8V power domain
DBG_RXD	11	DI	Receive data	1.8V power domain

Table 15: Pin Definition of UART1 Interface (Multiplexed with SPI)

Pin Name	Pin No.	Multiplexing Function 1 (Default)	Multiplexing Function 2	Multiplexing Function 3
SPI_CS_N	37	SPI_CS_N_BLSP6 (DO)	GPIO_22 (IO)	UART_RTS_BLSP6 (DI)
SPI_MOSI	38	SPI_MOSI_BLSP6 (DO)	GPIO_20 (IO)	UART_TXD_BLSP6 (DO)
SPI_MISO	39	SPI_MISO_BLSP6 (DI)	GPIO_21 (IO)	UART_RXD_BLSP6 (DI)
SPI_CLK	40	SPI_CLK_BLSP6 (DO)	GPIO_23 (IO)	UART_CTS_BLSP6 (DO)

Table 16: Pin Definition of UART2 Interface (Multiplexed with SDC1_DATA[3:0])

Pin Name	Pin No.	Multiplexing Function 1 (Default)	Multiplexing Function 2	Multiplexing Function 3
SDC1_DATA3	129	SDC1_DATA3 (IO)	GPIO_12 (IO)	UART_TXD_BLSP1 (DO)
SDC1_DATA2	130	SDC1_DATA2 (IO)	GPIO_13 (IO)	UART_RXD_BLSP1 (DI)

SDC1_DATA1	131	SDC1_DATA1 (IO)	GPIO_14 (IO)	UART_RTS_BLSP1 (DI)
SDC1_DATA0	132	SDC1_DATA0 (IO)	GPIO_15 (IO)	UART_CTS_BLSP1 (DO)

Table 17: Pin Definition of UART3 Interface (Multiplexed with SDC1_CLK&CMD)

Pin Name	Pin No.	Multiplexing Function 1 (Default)	Multiplexing Function 2	Multiplexing Function 3
SDC1_CLK	133	SDC1_CLK (DO)	GPIO_16 (IO)	UART_TXD_BLSP4 (DO)
SDC1_CMD	134	SDC1_CMD (IO)	GPIO_17 (IO)	UART_RXD_BLSP4 (DI)

NOTE

The non-default multiplexing functions mentioned in the above three tables take effect only after software configuration. Please refer to corresponding chapters for details.

The logic levels are described in the following table.

Table 18: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interfaces. A level translator should be used if the application is equipped with a 3.3V UART interface. A level translator TXS0104EPWR provided by Texas Instrument is recommended. The following figure shows a reference design.

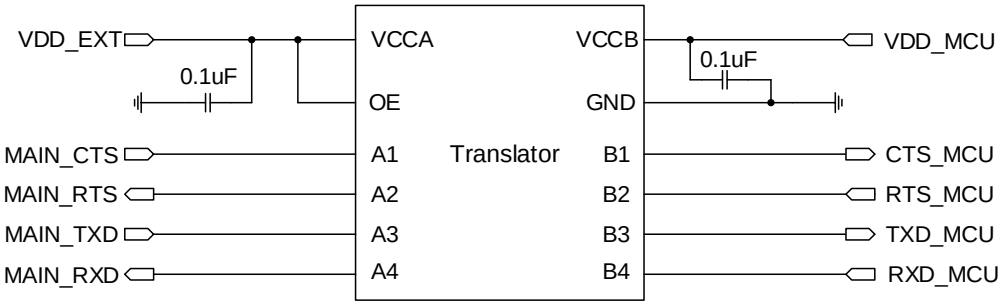


Figure 19: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

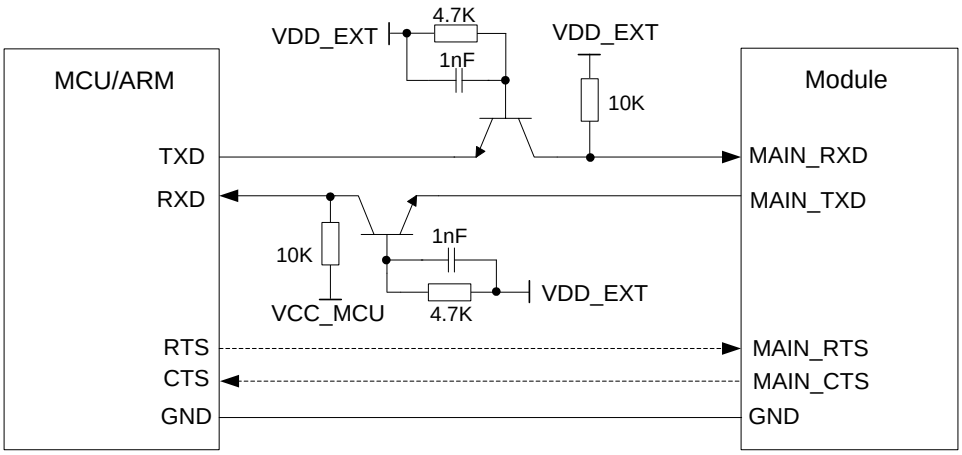


Figure 20: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. PCM and I2C Interfaces

EC25-Quecopen provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256KHz, 512KHz, 1024KHz or 2048KHz PCM_CLK at 8KHz PCM_SYNC, and also supports 4096KHz PCM_CLK at 16KHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256KHz, 512KHz, 1024KHz or 2048KHz PCM_CLK and an 8KHz, 50% duty cycle PCM_SYNC.

EC25-Quecopen supports also 16-bit linear data formats. The following figures show the primary mode's timing relationship with 8KHz PCM_SYNC and 2048KHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8KHz PCM_SYNC and 256KHz PCM_CLK.

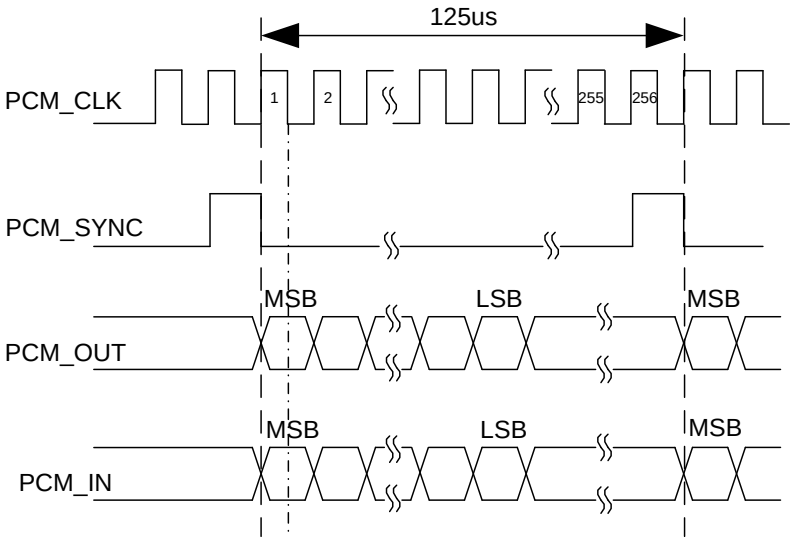


Figure 21: Primary Mode Timing

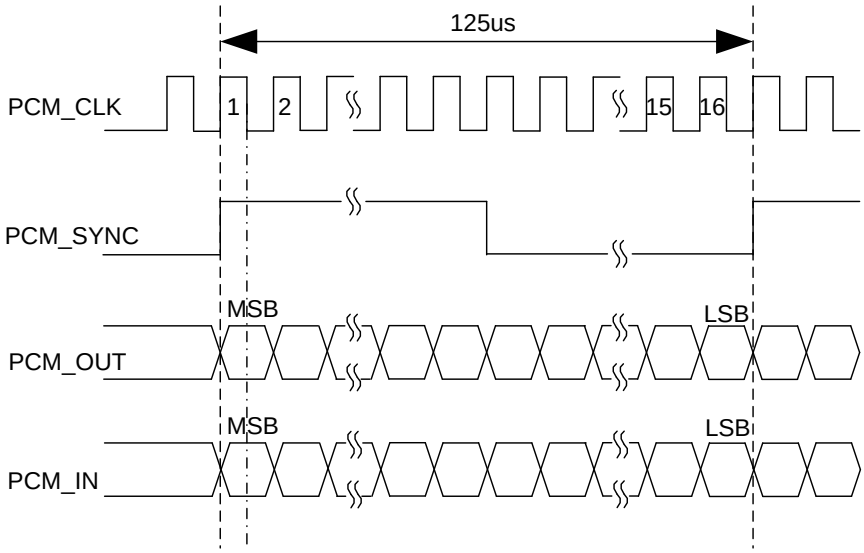


Figure 22: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 19: Pin Definition of PCM

Pin Name	Pin No.	Multiplexing Function 1 (Default)	Multiplexing Function 2	Multiplexing Function 3
PCM_IN	24	PCM_IN (DI)	GPIO_76 (IO)	I2S_IN (DI)
PCM_OUT	25	PCM_OUT (DO)	GPIO_77 (IO)	I2S_OUT (DO)
PCM_SYNC	26	PCM_SYNC (IO)	GPIO_79 (IO)	I2S_WS (DO)
PCM_CLK	27	PCM_CLK (IO)	GPIO_78 (IO)	I2S_CLK (DO)

Table 20: Pin Definition of I2C Interfaces

Pin Name	Pin No.	Multiplexing Function 1 (Default)	Multiplexing Function 2	Multiplexing Function 3
I2C_SCL	41	I2C_SCL_BLSP2 (OD)	GPIO_7 (IO)	--
I2C_SDA	42	I2C_SDA_BLSP2 (OD)	GPIO_6 (IO)	--

NOTE

For more details about non-default multiplexing functions for the pins mentioned in the above two tables, please refer to corresponding chapters.

Clock and mode can be configured by related software command or API, and the default configuration is master mode using short frame synchronization format with 2048KHz PCM_CLK and 8KHz PCM_SYNC.

The following figure shows a reference design of PCM interface with an external codec IC.

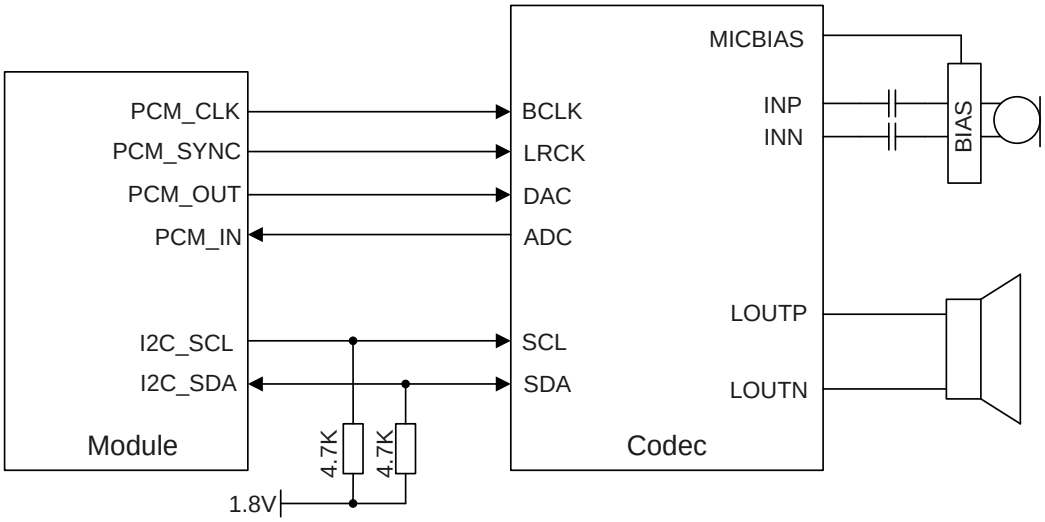


Figure 23: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EC25-Quecopen works as a master device pertaining to I2C interface.

3.12. SD Card Interface

EC25-Quecopen supports SDIO 3.0 interface for SD card.

The following table shows the pin definition of SD card interface.

Table 21: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	IO	SD card SDIO bus DATA3	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA2	29	IO	SD card SDIO bus DATA2	
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	
SDC2_CLK	32	DO	SD card SDIO bus clock	
SDC2_CMD	33	IO	SD card SDIO bus command	
VDD_SDIO	34	PO	SD card SDIO bus pull up power	
SD_INS_DET	23	DI	SD card insertion detect	

The following figure shows a reference design of SD card interface.

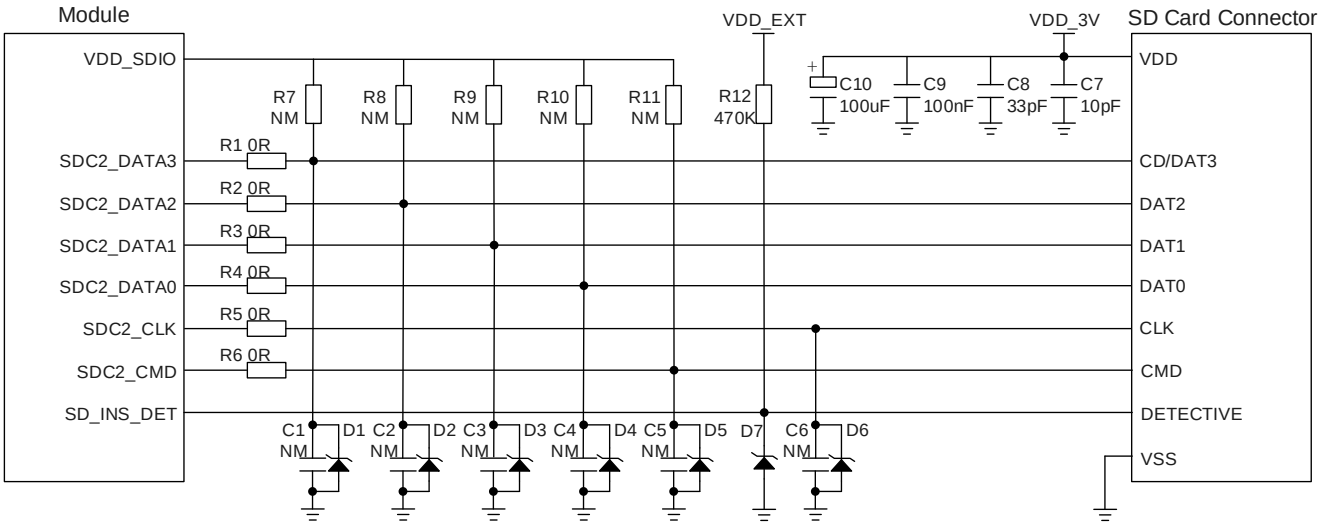


Figure 24: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_INS_DET must be connected.
- The voltage range of SD card power supply VDD_3V is 2.7~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.

- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10KΩ~100KΩ and the recommended value is 100KΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 27mm, so the exterior total trace length should be less than 23mm.

3.13. SPI Interface

EC25-Quecopen provides one SPI interface which supports only master mode with a maximum clock frequency up to 50MHz.

The following table shows the pin definition.

Table 22: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CS_N	37	DO	SPI chip selection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MOSI	38	DO	SPI master out slave in	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MISO	39	DI	SPI master in slave out	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SPI_CLK	40	DO	SPI serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Cannot be pulled up to high level, even to

		VDD_EXT before startup. If unused, keep it open.

The following figure shows the timing relationship of SPI interface. The related parameters of SPI timing is shown in the table below.

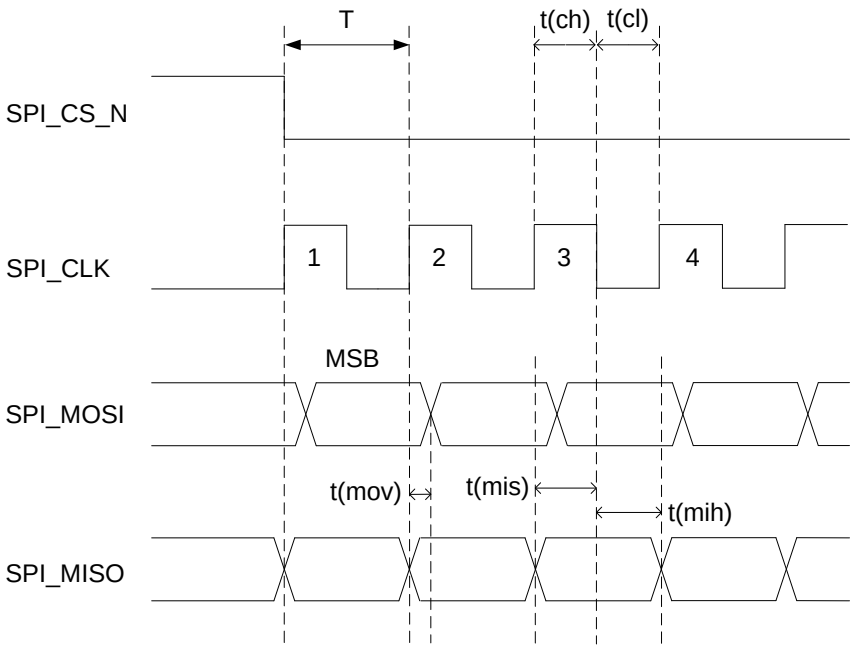


Figure 25: SPI Timing

Table 23: Parameters of SPI Interface Timing

Parameter	Description	Min	Typical	Max	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8V SPI interface. A level translator should be used between the module and the host if customer's application is equipped with a 3.3V processor or device interface.

3.14. WLAN Interface

EC25-Quecopen supports a low-power SDIO 3.0 interface for WLAN.

The following table shows the pin definition of WLAN interface.

Table 24: Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
Power Control Part				
PM_ENABLE	127	DO	WLAN power control.	1.8V power domain Active high.
WLAN Part				
SDC1_DATA3	129	IO	WLAN SDIO bus DATA3	1.8V power domain
SDC1_DATA2	130	IO	WLAN SDIO bus DATA2	1.8V power domain
SDC1_DATA1	131	IO	WLAN SDIO bus DATA1	1.8V power domain
SDC1_DATA0	132	IO	WLAN SDIO bus DATA0	1.8V power domain
SDC1_CLK	133	DO	WLAN SDIO bus clock	1.8V power domain
SDC1_CMD	134	IO	WLAN SDIO bus command	1.8V power domain
WLAN_EN	136	DO	WLAN enable	1.8V power domain Active high. Cannot be pulled up to high level, even to VDD_EXT before startup.
WLAN_SLP_CLK	118	DO	WLAN sleep clock	
WLAN_WAKE	135	DI	WLAN wake up the host	1.8V power domain
Coexistence Part				

COEX_UART_RX	137	DI	LTE/WLAN coexistence signal	1.8V power domain Cannot be pulled up to high level, even to VDD_EXT before startup.
COEX_UART_TX	138	DO	LTE/WLAN coexistence signal	1.8V power domain Cannot be pulled up to high level, even to VDD_EXT before startup.

NOTES

1. For more details about non-default multiplexing functions for the pins mentioned in the above table, please refer to corresponding chapters.
2. When WLAN function is used, the coexistence part mentioned in the above table must be used simultaneously.

The following figure shows a reference design of wireless connectivity interfaces with Quectel FC20 module.

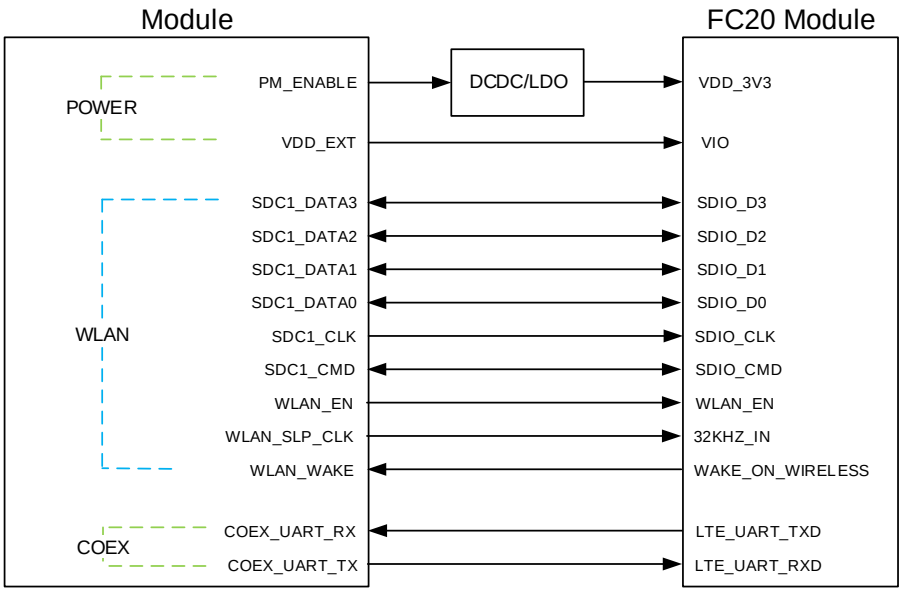


Figure 26: Reference Circuit of Wireless Connectivity Interfaces with FC20 Module

NOTES

1. FC20 module can only be used as a slave device.
2. For more information about WLAN interfaces application, please refer to ***document [5]***.

EC25-Quecopen provides a low power SDIO 3.0 interface and a control interface for WLAN design.

SDIO interface supports the SDR mode (up to 50MHz).

As SDIO signals are very high-speed signals, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm.
- Keep termination resistors within 15Ω~24Ω on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5mm.
- Make sure the adjacent trace spacing is 2 times of the trace width and bus capacitance is less than 15pF.

3.15. SGMII Interface

EC25-Quecopen includes an integrated Ethernet MAC with an SGMII interface and two management interfaces, and key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Support 10M/100M/1000M Ethernet work mode
- Support maximum 150Mbps (DL)/50Mbps (UL) for 4G network
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8V/2.85V

The following table shows the pin definition of SGMII interface.

Table 25: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8V power domain

SGMII_MDATA	121	IO	SGMII MDIO data	1.8V/2.85V power domain
SGMII_MCLK	122	DO	SGMII MDIO clock	1.8V/2.85V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	1.8V/2.85V configurable. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission-minus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII transmission-plus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	125	AI	SGMII receiving-plus	Connect with a 0.1uF capacitor, close to module.
SGMII_RX_M	126	AI	SGMII receiving-minus	Connect with a 0.1uF capacitor, close to module.

The following figure shows the simplified block diagram for Ethernet application.

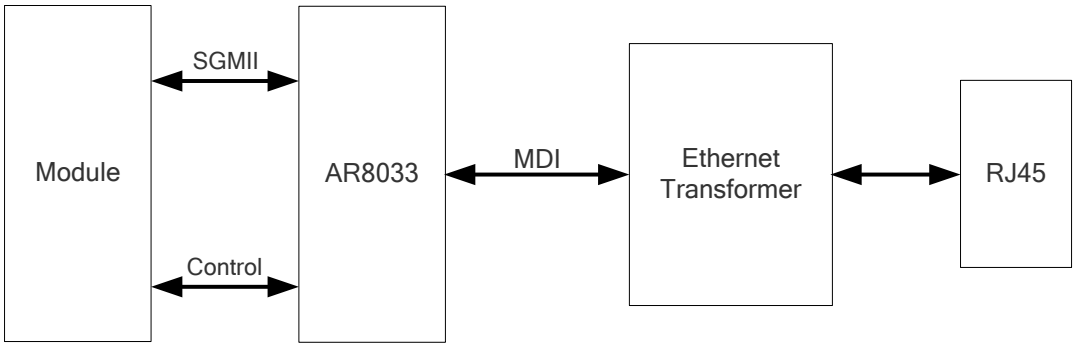


Figure 27: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

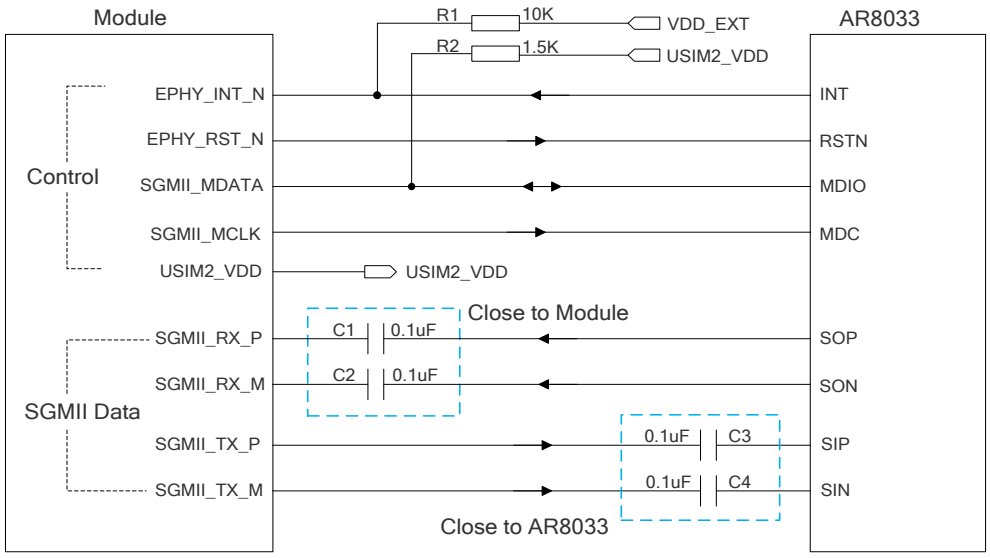


Figure 28: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in customers' applications, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- Keep the maximum trace length less than 10-inch and keep skew on the differential pairs less than 20mil.
- The differential impedance of SGMII data trace is 100Ω±10%, and the reference ground of the area should be complete.
- Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

3.16. ADC Interfaces

The module provides two analog-to-digital converters (ADC) interfaces. Related software command or API can be used to read the voltage value on ADC0 and ADC1 pin.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 26: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	45	General purpose analog to digital converter
ADC1	44	General purpose analog to digital converter

The following table describes the characteristic of the ADC function.

Table 27: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits

NOTES

1. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
2. It is recommended to use resistor divider circuit for ADC application.

3.17. Network Status Indication

The network indication pin can be used to drive network status indication LEDs. EC25-Quecopen provides one network indication pin: NET_STATUS. The following tables describe the pin definition and logic level changes of NET_STATUS in different network status.

Table 28: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	Multiplexing function 1 (Default)	Multiplexing function 2	Multiplexing function 3
NET_STATUS	6	NET_STATUS (DO)	PMU_GPIO1018 (DO)	--

Table 29: Working State of the Network Status Indicator

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

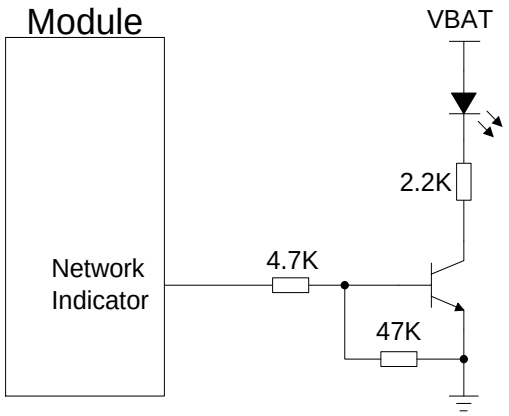


Figure 29: Reference Circuit of the Network Status Indicator

3.18. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pulled up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 30: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to specific application demands.

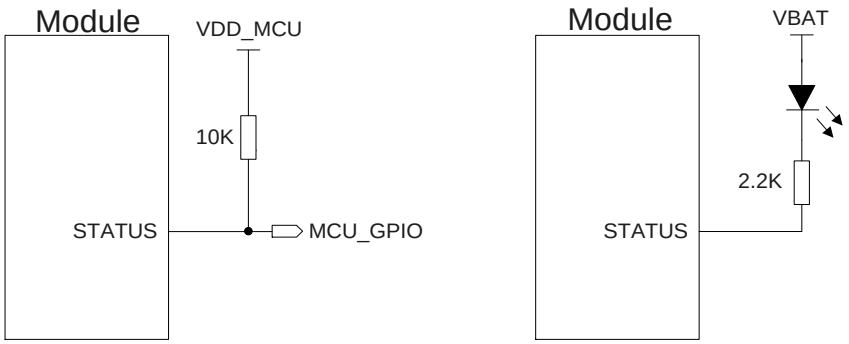


Figure 30: Reference Circuits of STATUS

3.19. USB_BOOT Interface

EC25-Quecopen provides a USB_BOOT pin. Customers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 31: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. It is recommended to reserve this pin as test point.

The following figures show a reference circuit of USB_BOOT interface and timing sequence of entering into emergency download mode.

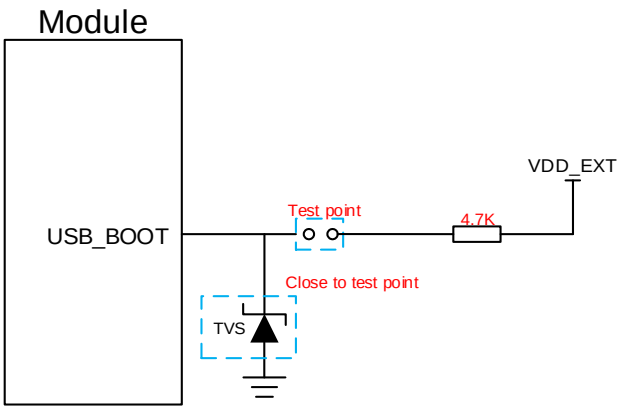


Figure 31: Reference Circuit of USB_BOOT Interface

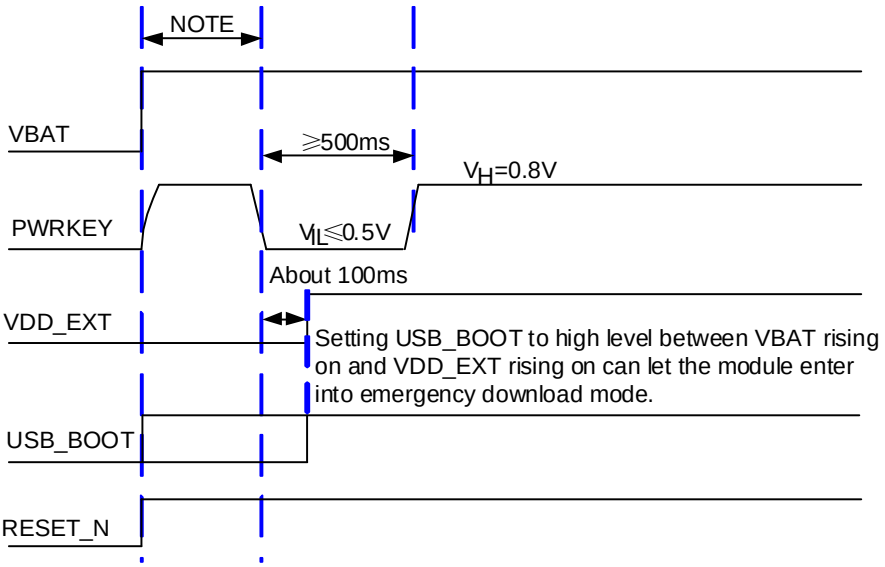


Figure 32: Timing Sequence for Entering into Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin, and the time between them is no less than 30ms.
2. When using MCU to control module to enter into the forced download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8V before powering up the VBAT. Short the test points as shown in ***Figure 31*** can manually force the module to enter into download mode.

4 GNSS Receiver

4.1. General Description

EC25-Quecopen includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EC25-Quecopen supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, GNSS engine of the module is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EC25-Quecopen.

Table 32: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start	Autonomous	2.5	s

	@open sky	XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50Ω characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EC25-Quecopen include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The antenna interfaces have an impedance of 50Ω.

5.1. Main/Rx-diversity Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces are shown below.

Table 33: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna pad	50Ω impedance
ANT_DIV	35	AI	Receive diversity antenna pad	50Ω impedance

5.1.2. Operating Frequency

Table 34: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
B1	1920~1980	2110~2170	MHz
B2	1850~1910	1930~1990	MHz
B3 (1800)	1710~1785	1805~1880	MHz
B4	1710~1755	2110~2155	MHz
B5	824~849	869~894	MHz
B7	2500~2570	2620~2690	MHz

B8 (900)	880~915	925~960	MHz
B12	699~716	729~746	MHz
B20	832~862	791~821	MHz
B38	2570~2620	2570~2620	MHz
B40	2300~2400	2300~2400	MHz
B41	2555~2655	2555~2655	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. It should reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

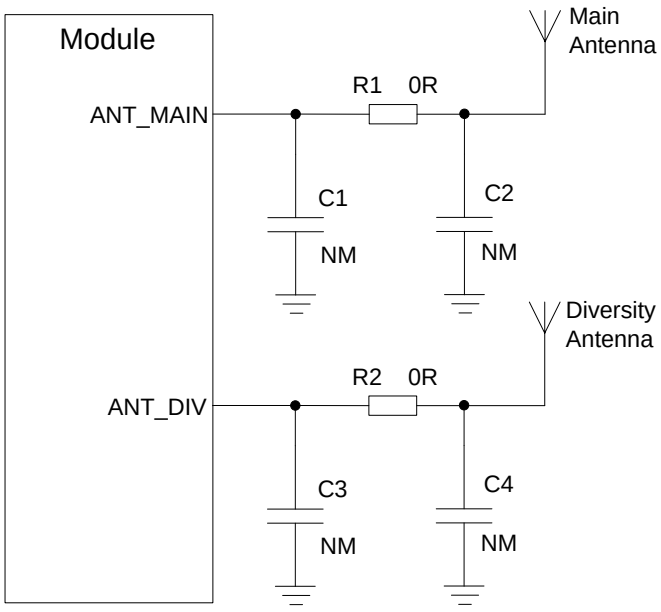


Figure 33: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default.
3. Place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

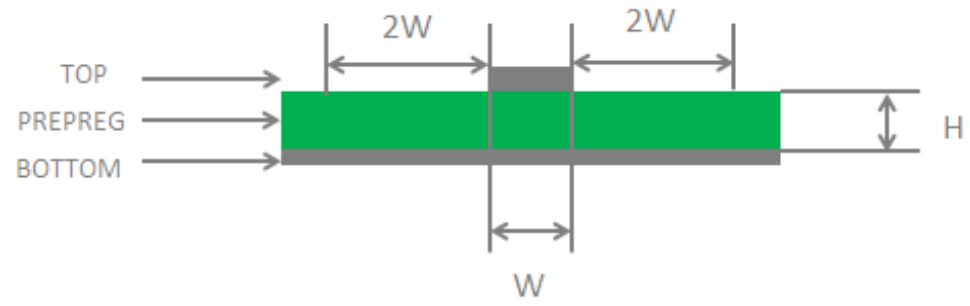


Figure 34: Microstrip Line Design on a 2-layer PCB

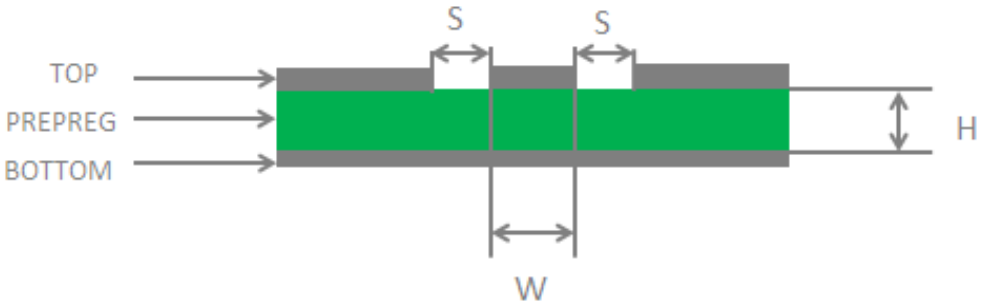


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

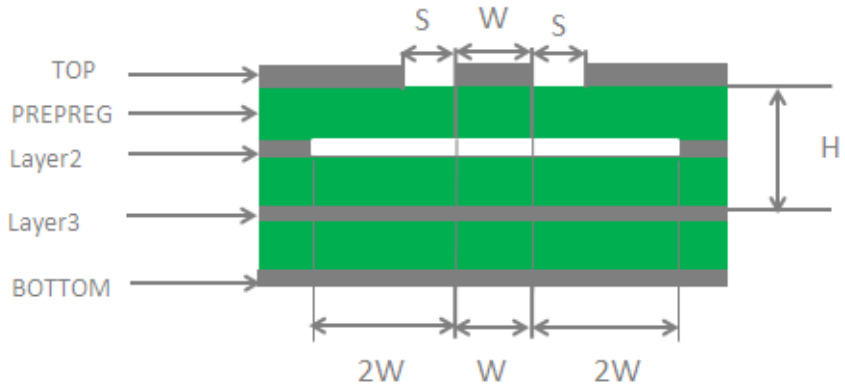


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

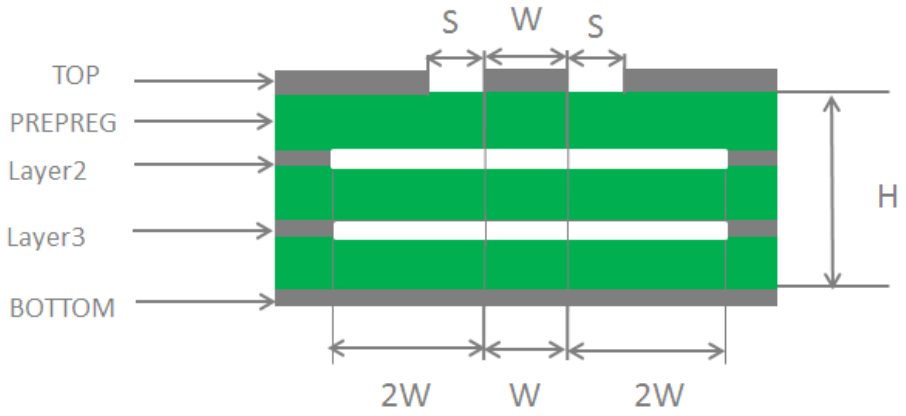


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 35: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50Ω impedance

Table 36: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

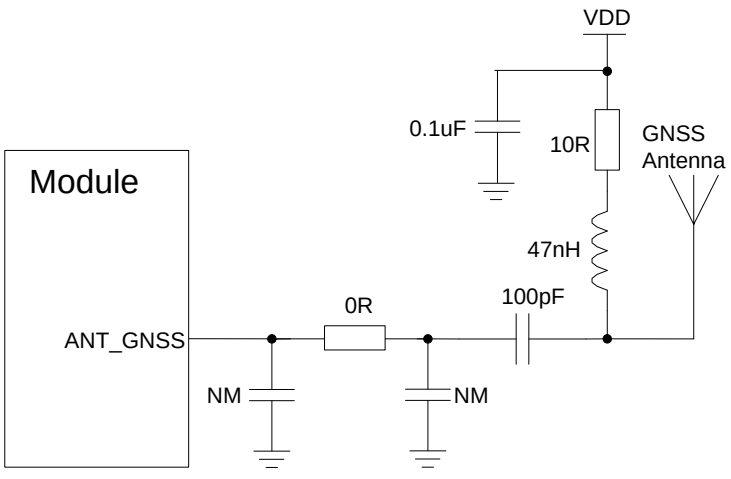


Figure 38: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 37: Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17 dB
GSM/WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50W Input Impedance: 50Ω Cable Insertion Loss: < 1dB (GSM 900, WCDMA B5/B8, LTE-FDD B5/B8/B12/B20) Cable Insertion Loss: < 1.5dB (DCS1800, WCDMA B1/B2/B4, LTE-FDD B1/B2/B3/B4) Cable Insertion loss: < 2dB (LTE-FDD B7, LTE-TDD B38/B40/B41)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use UF.L-R-SMT connector provided by HIROSE.

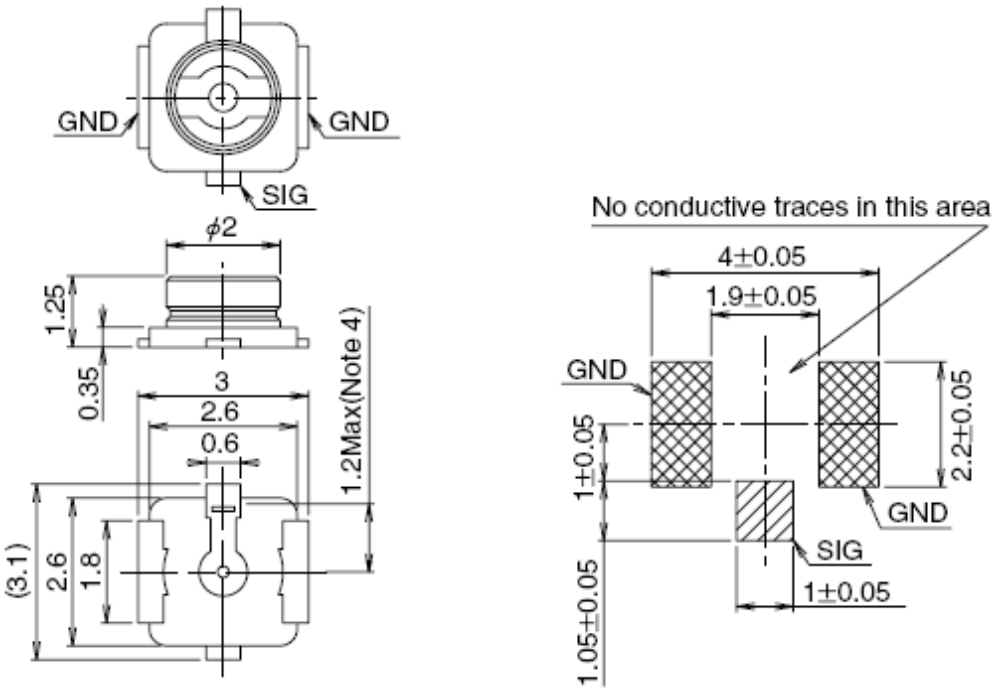


Figure 39: Dimensions of the UF.L-R-SMT Connector (Unit: mm)

U.FL-LP serial connector listed in the following figure can be used to match the UF.L-R-SMT.

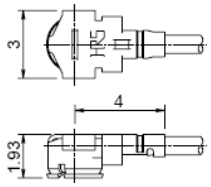
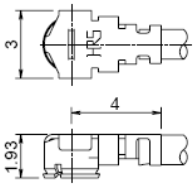
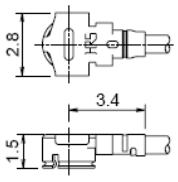
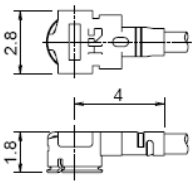
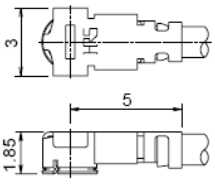
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of UF.L-LP Connectors

The following figure describes the space factor of mated connector.

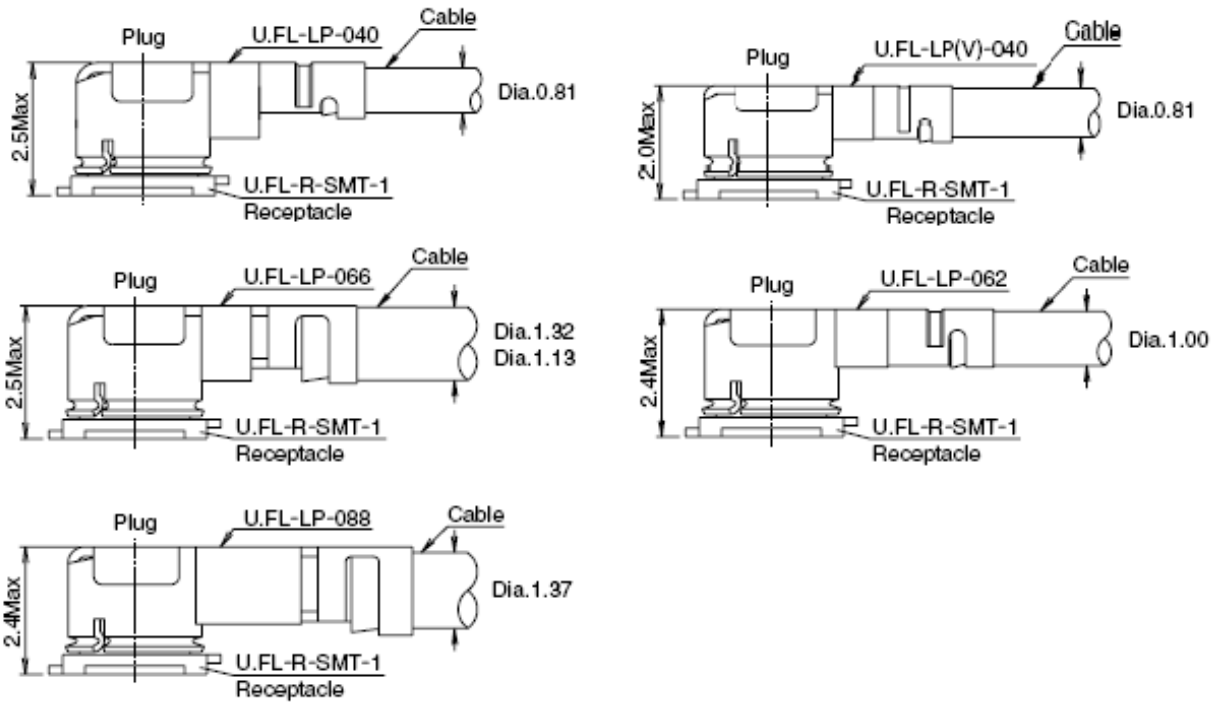


Figure 41: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 38: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 39: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on GSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on GSM900		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 40: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Operation Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operation temperature levels, the module will meet 3GPP specifications

again.

6.4. Current Consumption

The values of current consumption are shown below.

Table 41: EC25-E-Quecopen Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	11	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.16	mA
		GSM DRX=2 (USB disconnected)	2.74	mA
		GSM DRX=9 (USB disconnected)	2.0	mA
		WCDMA PF=64 (USB disconnected)	2.15	mA
		WCDMA PF=128 (USB disconnected)	1.67	mA
		LTE-FDD PF=64 (USB disconnected)	2.60	mA
		LTE-FDD PF=128 (USB disconnected)	1.90	mA
		LTE-TDD PF=64 (USB disconnected)	2.79	mA
		LTE-TDD PF=128 (USB disconnected)	2.00	mA
	Idle state	GSM DRX=5 (USB disconnected)	19.5	mA
		GSM DRX=5 (USB connected)	29.5	mA
		WCDMA PF=64 (USB disconnected)	21.0	mA
		WCDMA PF=64 (USB connected)	31.0	mA
		LTE-FDD PF=64 (USB disconnected)	20.7	mA
		LTE-FDD PF=64 (USB connected)	30.8	mA
		LTE-TDD PF=64 (USB disconnected)	20.8	mA

		LTE-TDD PF=64 (USB connected)	32.0	mA
	GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @33.22dBm	271.0	mA
		EGSM900 3DL/2UL @33.0dBm	464.0	mA
		EGSM900 2DL/3UL @30.86dBm	524.0	mA
		EGSM900 1DL/4UL @29.58dBm	600	mA
		DCS1800 4DL/1UL @29.92dBm	192.0	mA
		DCS1800 3DL/2UL @29.84dBm	311.0	mA
		DCS1800 2DL/3UL @29.67dBm	424.0	mA
		DCS1800 1DL/4UL @29.48dBm	539.0	mA
	EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL PCL=8 @27.40dBm	174.0	mA
		EGSM900 3DL/2UL PCL=8 @27.24dBm	281.0	mA
		EGSM900 2DL/3UL PCL=8 @27.11dBm	379.0	mA
		EGSM900 1DL/4UL PCL=8 @26.99dBm	480.0	mA
		DCS1800 4DL/1UL PCL=2 @25.82dBm	159.0	mA
		DCS1800 3DL/2UL PCL=2 @25.85dBm	251.0	mA
		DCS1800 2DL/3UL PCL=2 @25.68dBm	340.0	mA
		DCS1800 1DL/4UL PCL=2 @25.57dBm	433.0	mA
	WCDMA datatransfer (GNSS OFF)	WCDMA B1 HSDPA @22.47dBm	613.0	mA
		WCDMA B1 HSUPA @22.44dBm	609.0	mA
		WCDMA B5 HSDPA @23.07dBm	671.0	mA
		WCDMA B5 HSUPA @23.07dBm	669.0	mA
		WCDMA B8 HSDPA @22.67dBm	561.0	mA
		WCDMA B8 HSUPA @22.39dBm	557.0	mA
	LTE datatransfer (GNSS OFF)	LTE-FDD B1 @23.27dBm	754.0	mA
		LTE-FDD B3 @23.54dBm	774.0	mA

		LTE-FDD B5 @22.83dBm	762.0	mA
		LTE-FDD B7 @23.37dBm	842.0	mA
		LTE-FDD B8 @23.48dBm	720.0	mA
		LTE-FDD B20 @22.75dBm	714.0	mA
		LTE-TDD B38 @23.05dBm	481.0	mA
		LTE-TDD B40 @23.17dBm	431.8	mA
		LTE-TDD B41 @23.02dBm	480.0	mA
	GSM voice call	EGSM900 PCL=5 @33.08dBm	264.0	mA
		DCS1800 PCL=0 @29.75dBm	190.0	mA
	WCDMA voice call	WCDMA B1 @23.22dBm	680.0	mA
		WCDMA B5 @23.18dBm	677.0	mA
		WCDMA B8 @23.54dBm	618.0	mA

Table 42: EC25-A-Quecopen Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
		WCDMA PF=64 (USB disconnected)	1.8	mA
		WCDMA PF=128 (USB disconnected)	1.5	mA
		LTE-FDD PF=64 (USB disconnected)	2.2	mA
		LTE-FDD PF=128 (USB disconnected)	1.6	mA
	Idle state	WCDMA PF=64 (USB disconnected)	21.0	mA
		WCDMA PF=64 (USB connected)	31.0	mA
		LTE-FDD PF=64 (USB disconnected)	21.0	mA
		LTE-FDD PF=64 (USB connected)	31.0	mA

	WCDMA datatransfer (GNSS OFF)	WCDMA B2 HSDPA @21.9dBm	591.0	mA
		WCDMA B2 HSUPA @21.62dBm	606.0	mA
		WCDMA B4 HSDPA @22.02dBm	524.0	mA
		WCDMA B4 HSUPA @21.67dBm	540.0	mA
		WCDMA B5 HSDPA @22.71dBm	490.0	mA
		WCDMA B5 HSUPA @22.58dBm	520.0	mA
	LTE datatransfer (GNSS OFF)	LTE-FDD B2 @22.93dBm	715.0	mA
		LTE-FDD B4 @22.96dBm	738.0	mA
		LTE-FDD B12 @23.35dBm	663.0	mA
	WCDMA voice call	WCDMA B2 @22.93dBm	646.0	mA
		WCDMA B4 @23dBm	572.0	mA
		WCDMA B5 @23.78dBm	549.0	mA

Table 43: EC25-Quecopen GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	54.0	mA
		Lost state @Passive Antenna	53.9	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	30.5	mA
		Open Sky @Passive Antenna	33.2	mA
		Open Sky @Active Antenna	40.8	mA

6.5. RF Output Power

The following table shows the RF output power of EC25-Quecopen module.

Table 44: RF Output Power

Frequency	Max.	Min.
GSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
GSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800 (8-PSK)	26dBm±3dB	0dBm±5dB
WCDMA bands	24dBm+1/-3dB	<-49dBm
LTE-FDD bands	23dBm±2dB	<-39dBm
LTE-TDD bands	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of EC25-Quecopen series module.

Table 45: EC25-E-Quecopen Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP (SIMO)
EGSM900	-109.0dBm	/	/	-102.0dBm
DCS1800	-109.0dBm	/	/	-102.0dbm
WCDMA B1	-110.5dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm

WCDMA B8	-110.5dBm	/	/	-103.7dBm
LTE-FDD B1 (10M)	-98.0dBm	-98.0dBm	-101.5dBm	-96.3dBm
LTE-FDD B3 (10M)	-96.5dBm	-98.5dBm	-101.5dBm	-93.3dBm
LTE-FDD B5 (10M)	-98.0dBm	-98.5dBm	-101.0dBm	-94.3dBm
LTE-FDD B7 (10M)	-97.0dBm	-94.5dBm	-99.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-97.0dBm	-97.0dBm	-101.0dBm	-93.3dBm
LTE-FDD B20 (10M)	-97.5dBm	-99.0dBm	-102.5dBm	-93.3dBm
LTE-TDD B38 (10M)	-95dBm	-97.0dBm	-98.9dBm	-96.3dBm
LTE-TDD B40 (10M)	-96.3dBm	-98.0dBm	-101.0dBm	-96.3dBm
LTE-TDD B41 (10M)	-94.5dBm	-95.7dBm	-98.5dBm	-94.3dBm

Table 46: EC25-A-Quecopen Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP (SIMO)
WCDMA B2	-110.0dBm	/	/	-104.7dBm
WCDMA B4	-110.0dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm
LTE-FDD B2 (10M)	-98.0dBm	-98.0dBm	-101.0dBm	-94.3dBm
LTE-FDD B4 (10M)	-97.5dBm	-99.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B12 (10M)	-96.5dBm	-98.0dBm	-101.0dBm	-93.3dBm

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 47: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

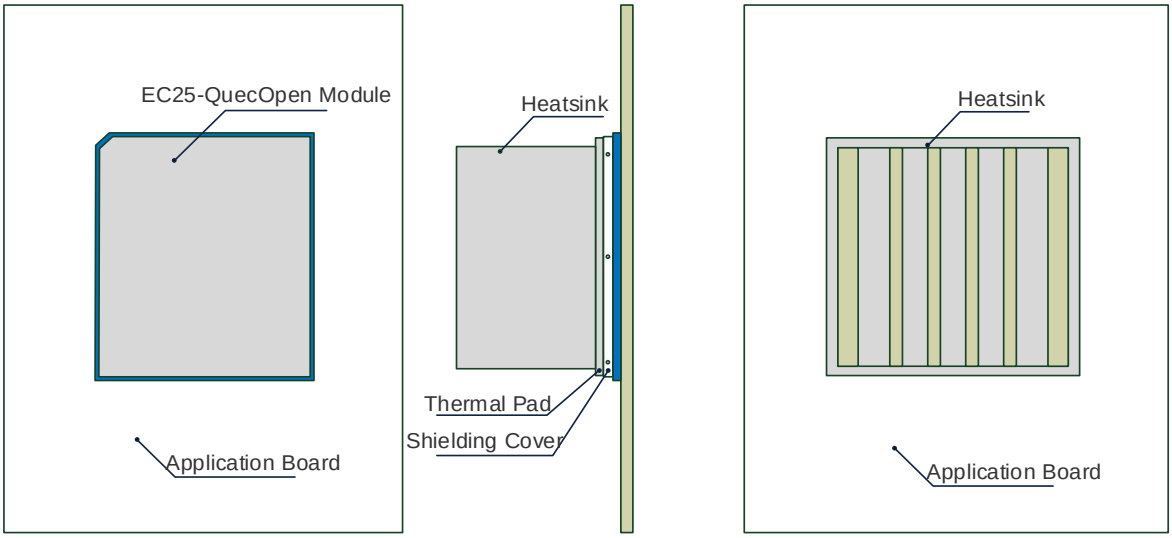


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module

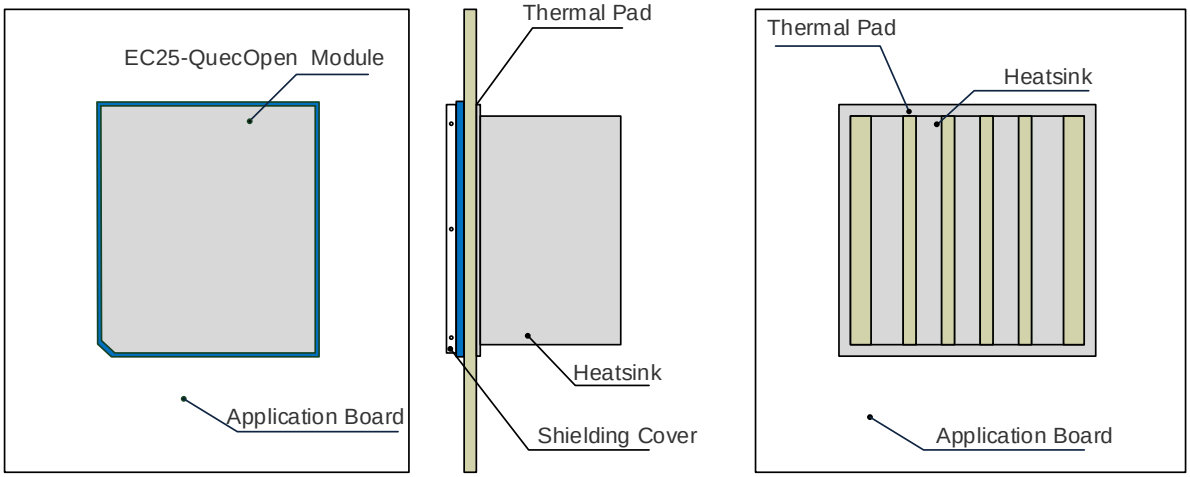


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTES

1. The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute related software command or API and get the maximum BB chip temperature from the returned value.
2. For more detailed guidelines on thermal design, please refer to ***document [7]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

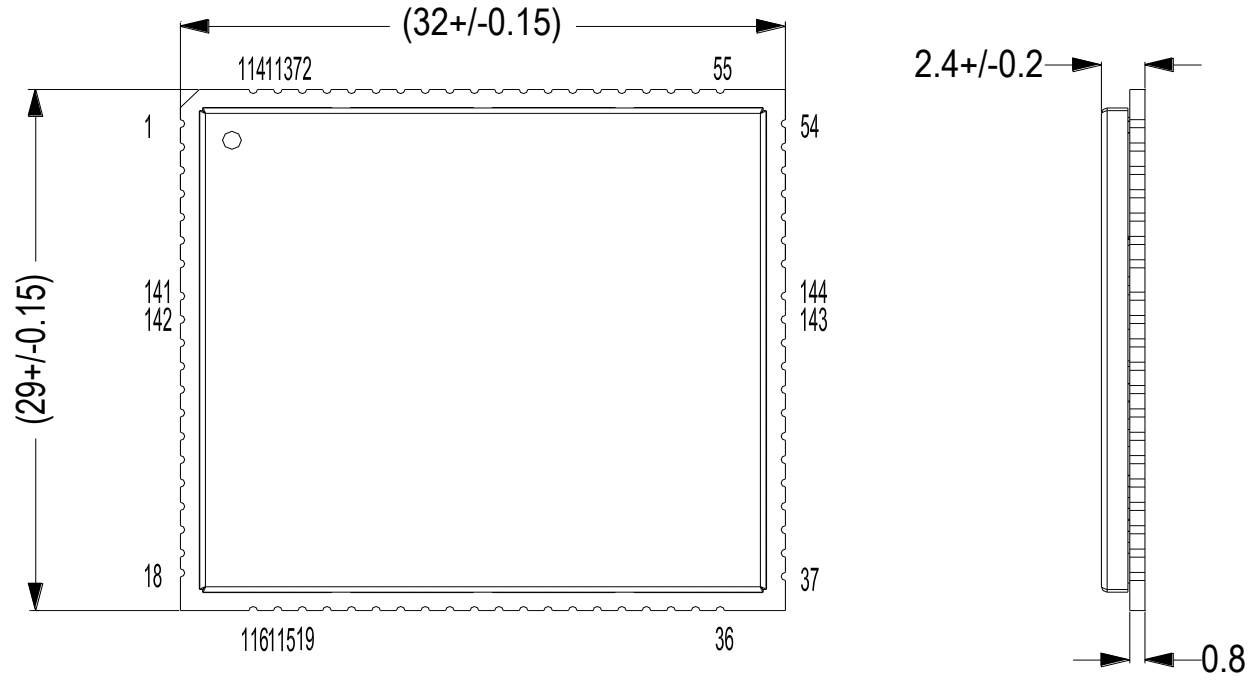


Figure 44: Module Top and Side Dimensions

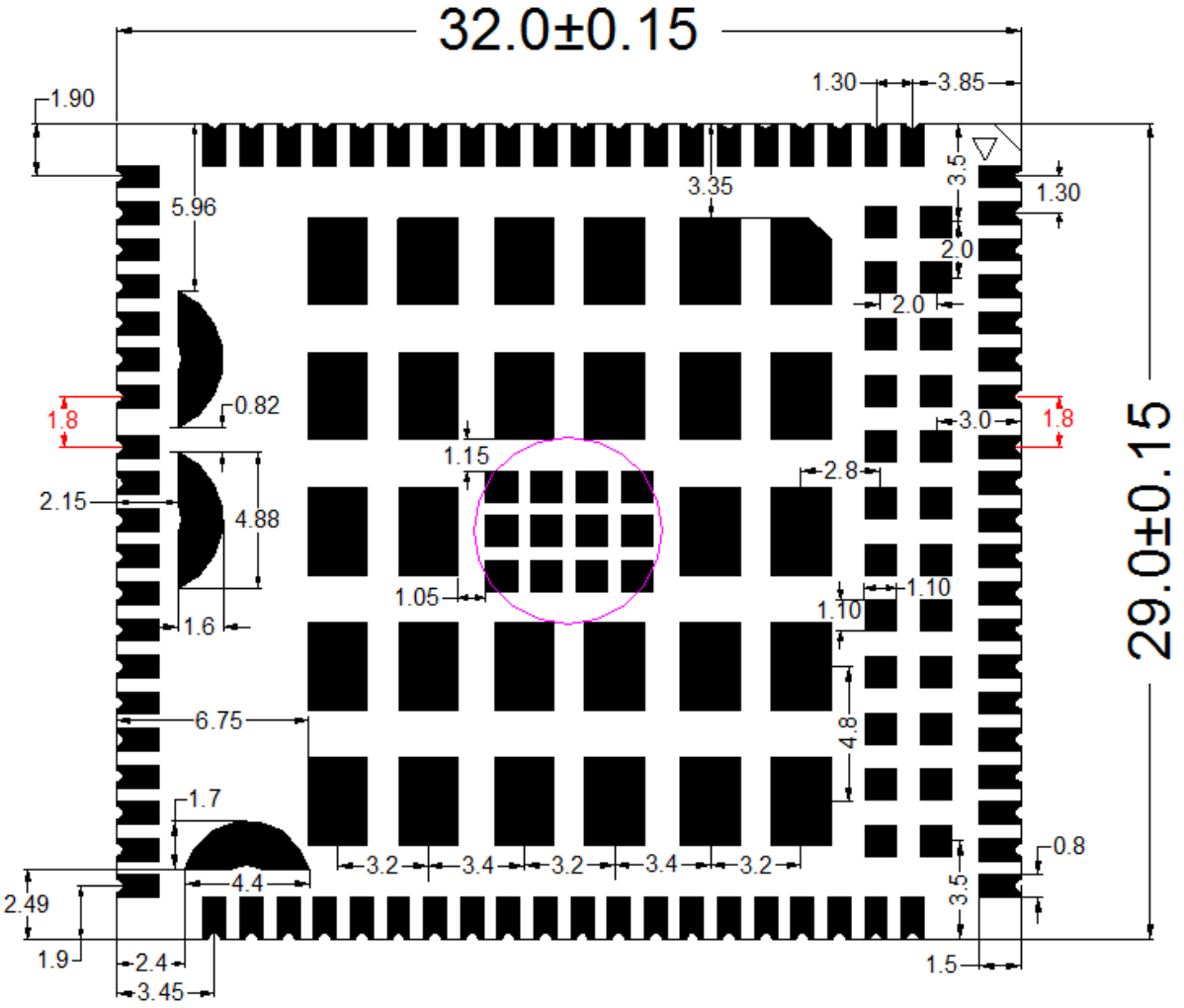


Figure 45: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

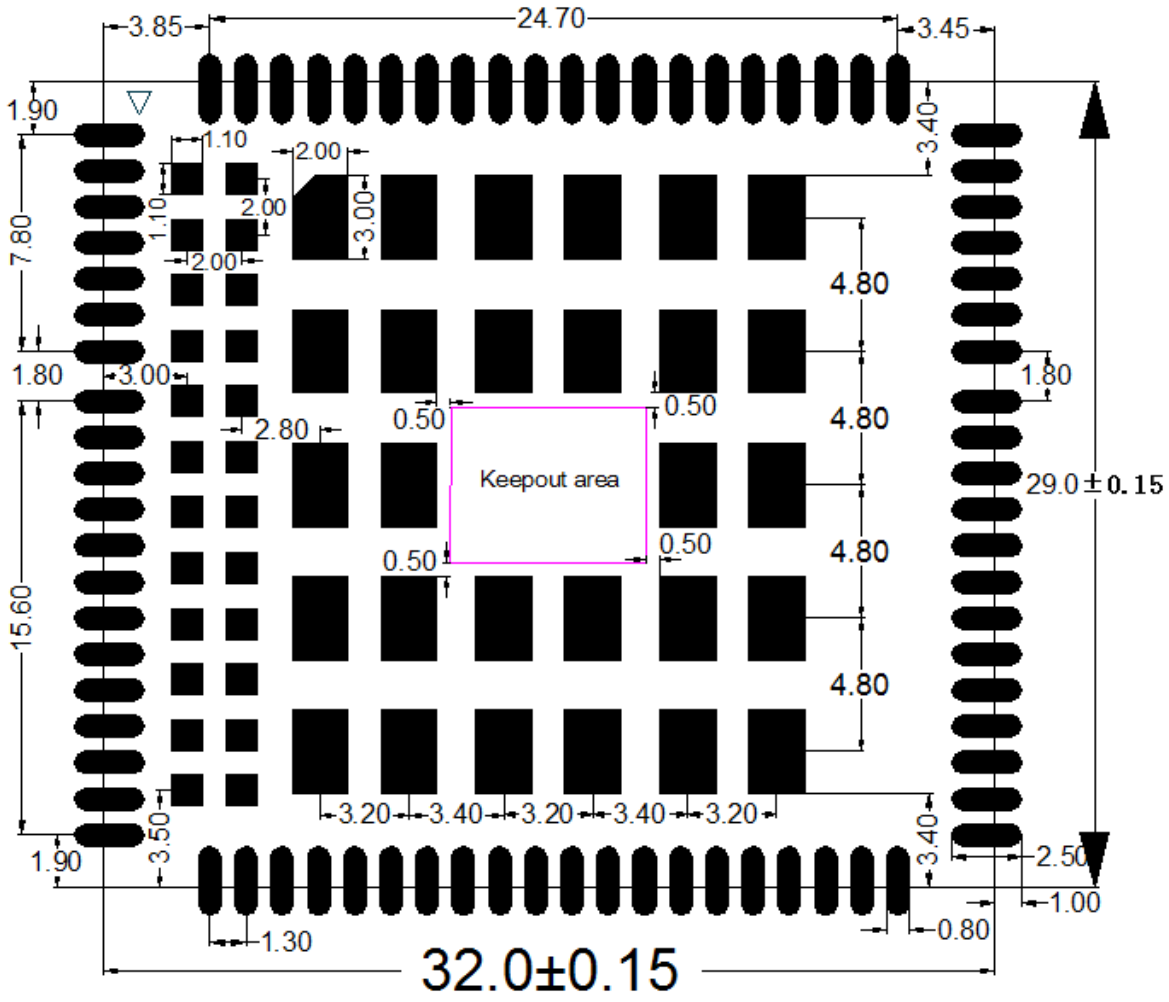


Figure 46: Recommended Footprint (Top View)

NOTES

1. Pads 73~84 should not be designed.
2. For easy maintenance of the module, please keep about 3mm between the module and other components on the host PCB.

7.3. Design Effect Drawings of the Module

Figure 47: Top View of the Module

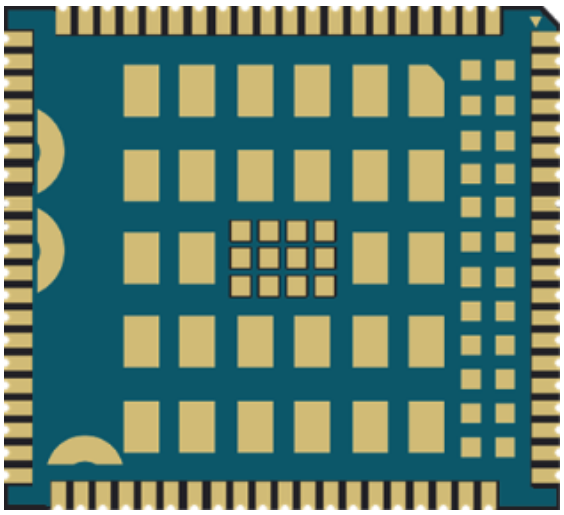


Figure 48: Bottom View of the Module

NOTE

These are design effect drawings of EC25-Quecopen module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EC25-Quecopen is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30º C/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstances below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30º C/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 240ºC ~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

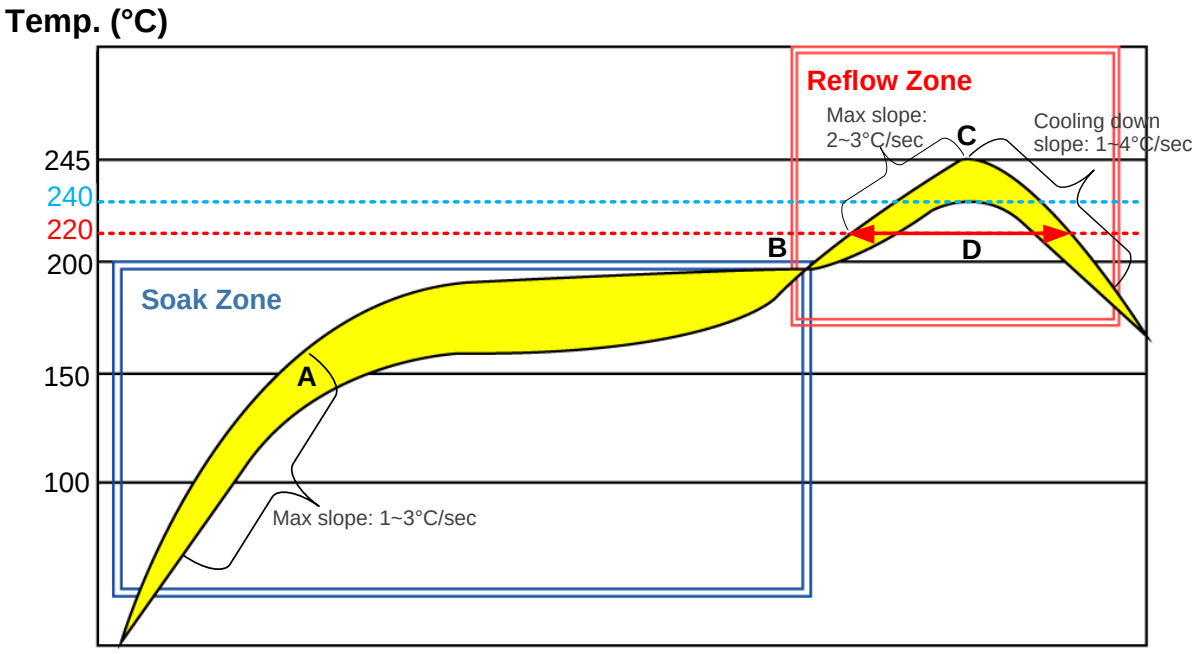


Figure 49: Reflow Soldering Thermal Profile

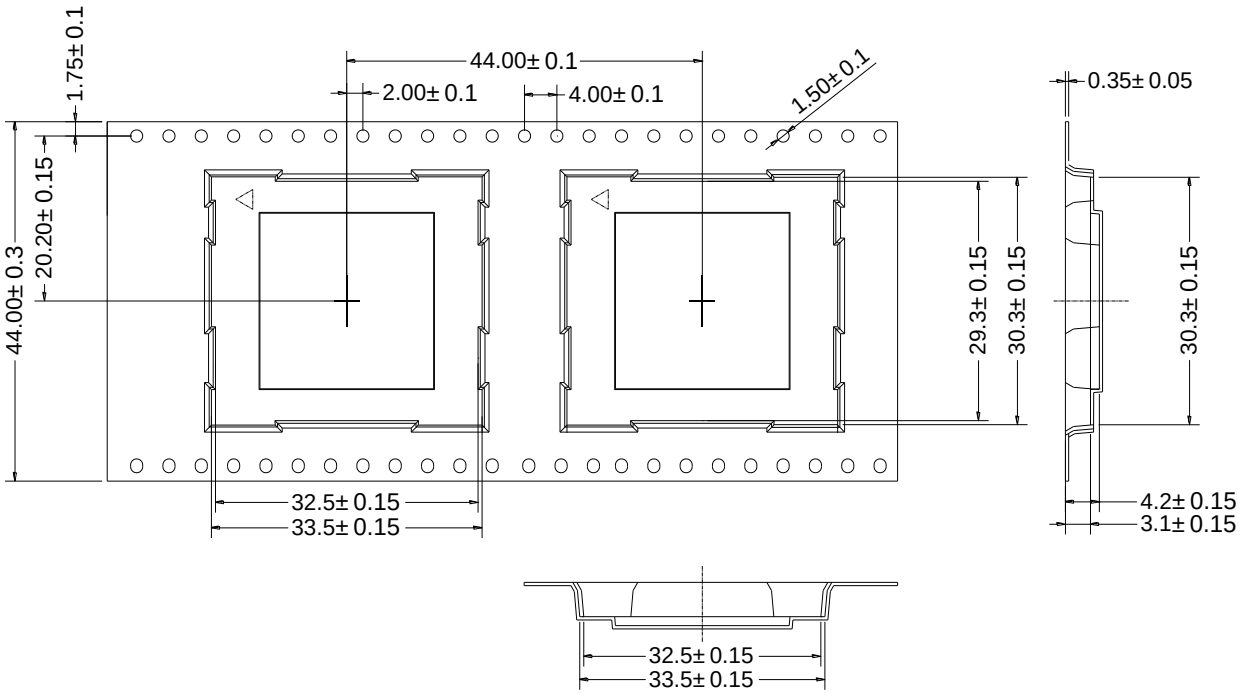
Table 48: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	240°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

EC25-Quecopen is packaged in tape and reel carriers. One reel is 11.88m long and contains 250pcs modules. The reel diameter is 330mm.The figure below shows the package details, measured in mm.



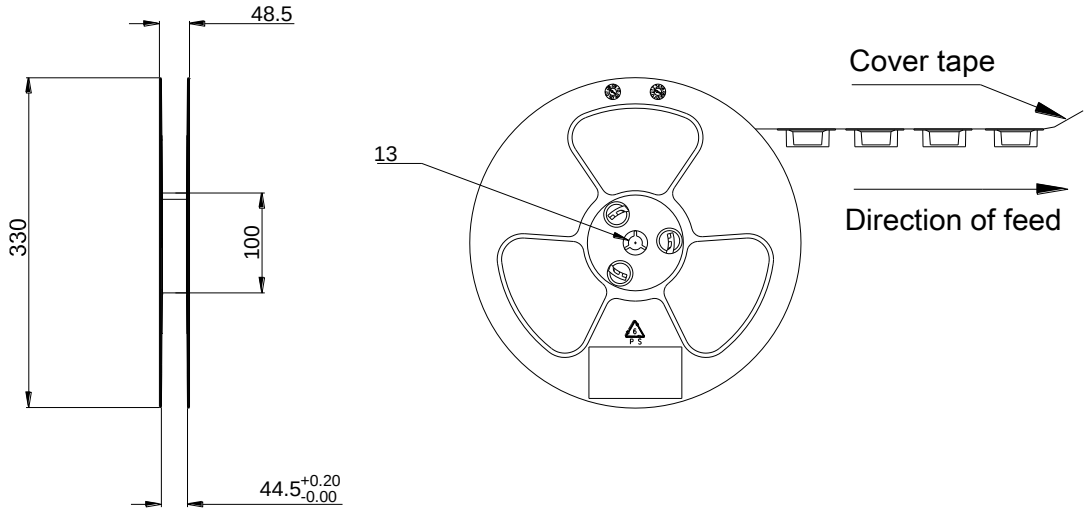


Figure 50: Tape and Reel Specifications

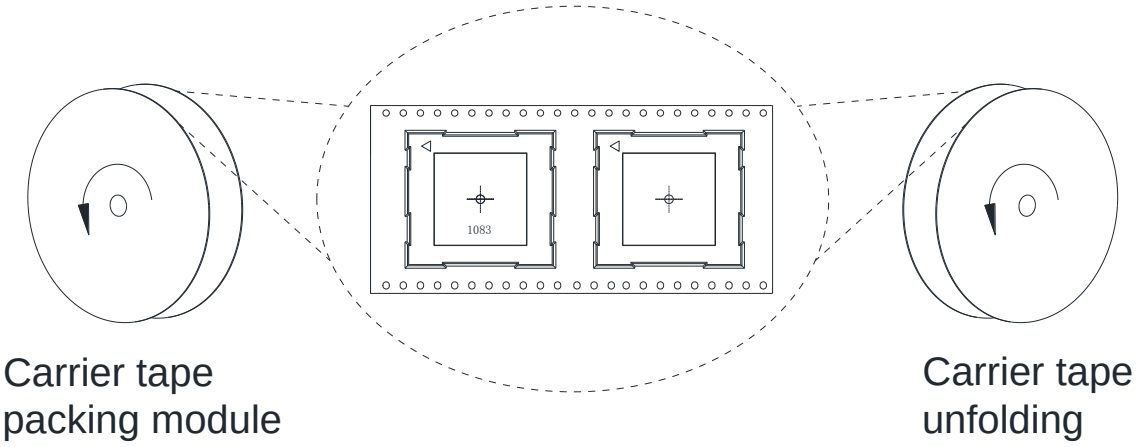


Figure 51: Tape and Reel Directions

9 Appendix A References

Table 49: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x_Power_Management_Application_Note	Power Management Application Note for EC25, EC21, EC20 R2.0, EC20 R2.1, EG91 and EG95 modules
[2]	Quectel_EC25&EC21_AT_Commands_Manual	EC25 and EC21 AT Commands Manual
[3]	Quectel_EC25&EC21_GNSS_AT_Commands_Manual	EC25 and EC21 GNSS AT Commands Manual
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_EC25_Reference_Design	EC25 Reference Design
[6]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[7]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal design guide for LTE modules including EC25, EC21, EC20 R2.0, EC20 R2.1, EG91, EG95, EG25-G, EP06, EG06, EM06 and AG35.

Table 50: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
API	Application Program Interface
bps	Bits Per Second
BT	Bluetooth
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data

CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output

MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value

Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

10 Appendix B GPRS Coding Schemes

Table 51: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 52: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 53: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps