AG35-Quecopen

EAVB Reference Design

Automotive Module Series

Rev. AG35-Quecopen_EAVB_Reference_Design_V1.0

Date: 2019-05-30

Status: Released

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About the Document

History

Revision	Date	Author	Description
1.0	2019-05-30	Eden LIU	Initial

Contents

1 Reference Design

1.1. Introduction

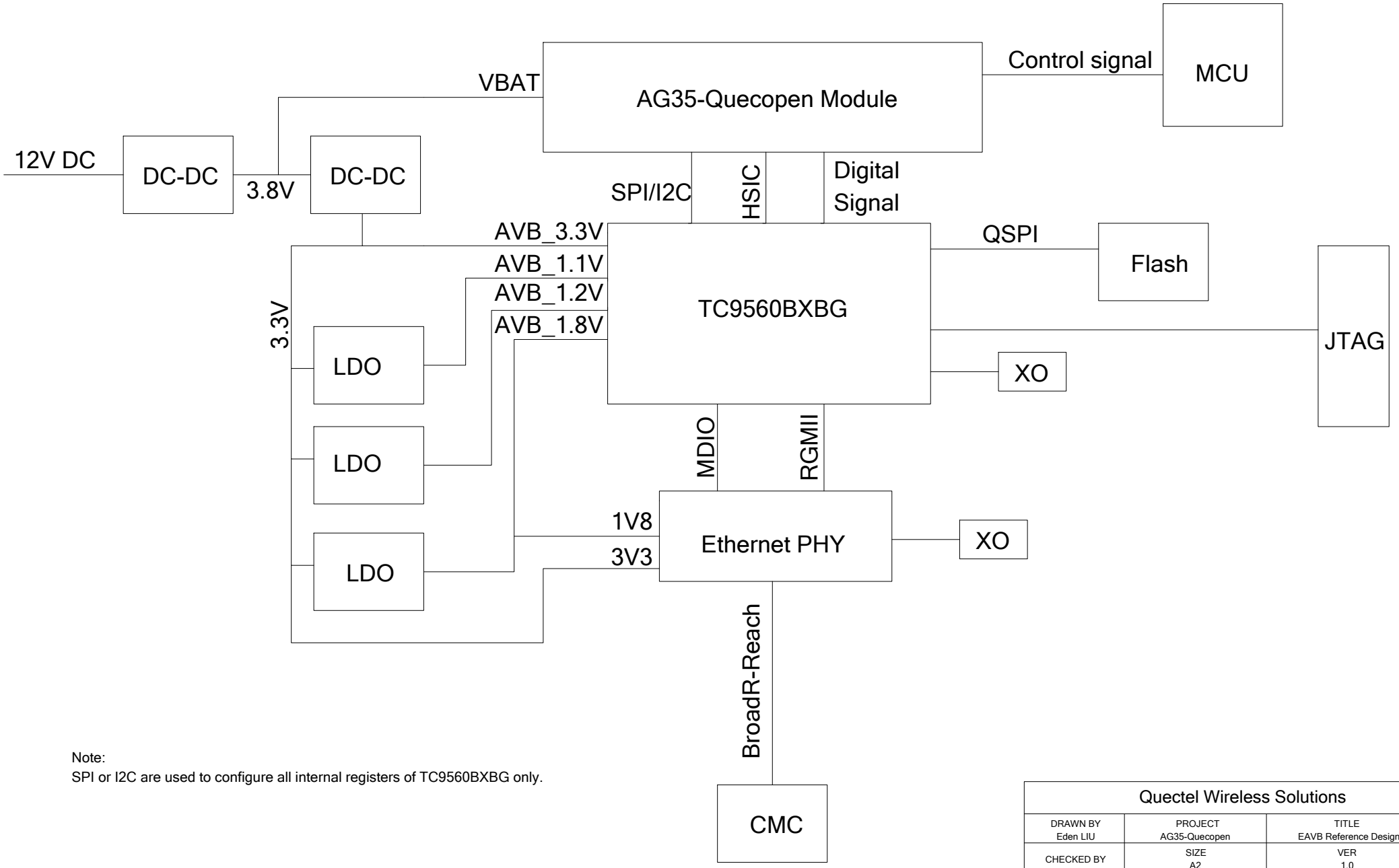
This document provides the EAVB (Ethernet Audio Video Bridging) reference design of Quectel AG35-Quecopen module.

Other necessary designs such as (U)SIM, USB, antenna designs, etc. are not included in this document. For details of other interface designs, please refer to *Quectel_AG35-Quecopen_Reference_Design*.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Function Block



Note:
SPI or I2C are used to configure all internal registers of TC9560BXBG only.

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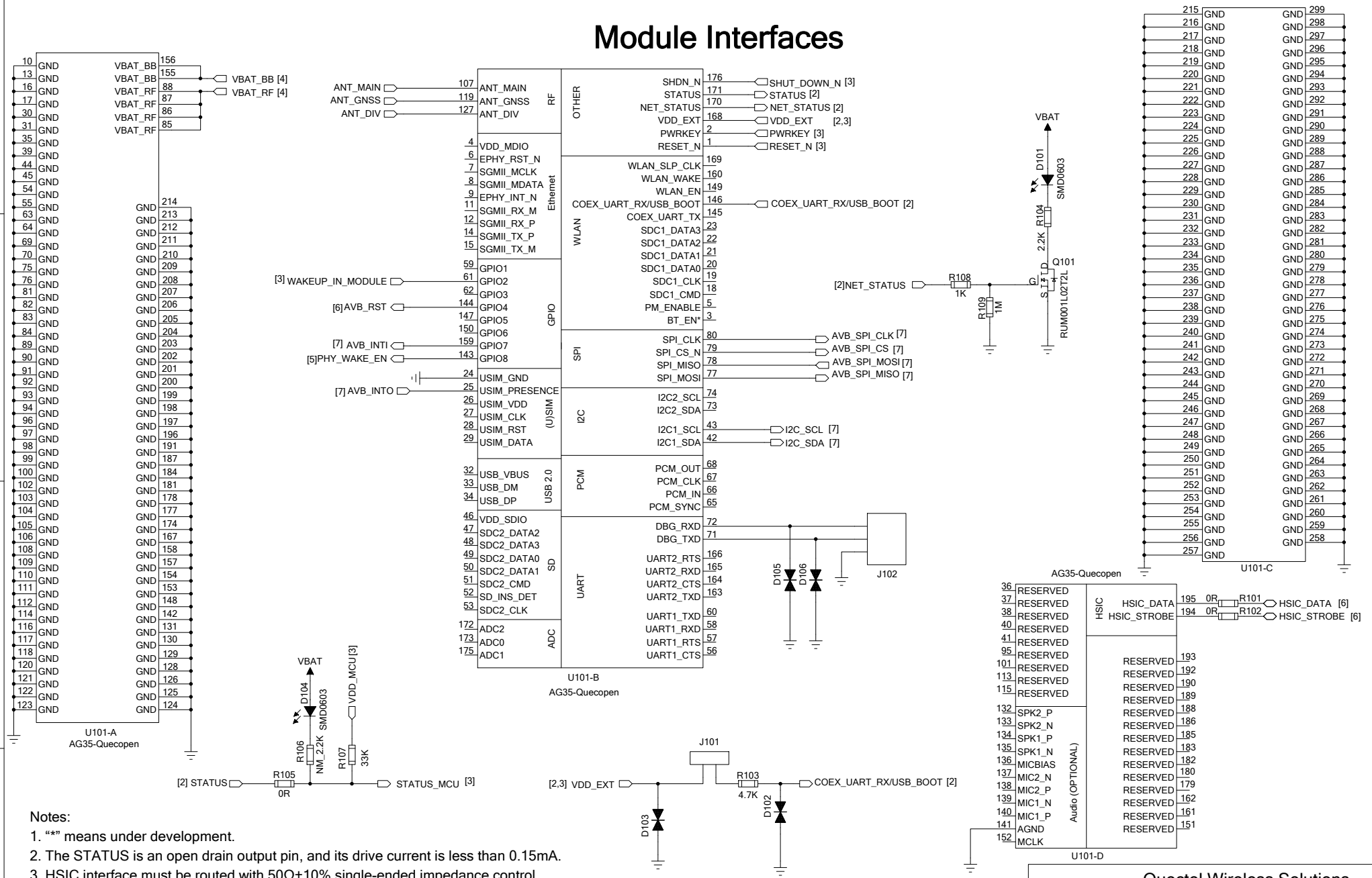
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 1 OF 8	DATE 2019/5/30

Module Interfaces



Notes:

1. "*" means under development.
2. The STATUS is an open drain output pin, and its drive current is less than 0.15mA.
3. HSIC interface must be routed with 50Ω±10% single-ended impedance control.
   The recommended maximum trace length is 8cm, and the intra-pair length match is recommended to be less than 2.5mm.
4. For more details of the module interface designs, please refer to *Quectel_AG35-Quecopen_Hardware_Design* and *Quectel_AG35-Quecopen_Reference_Design*.

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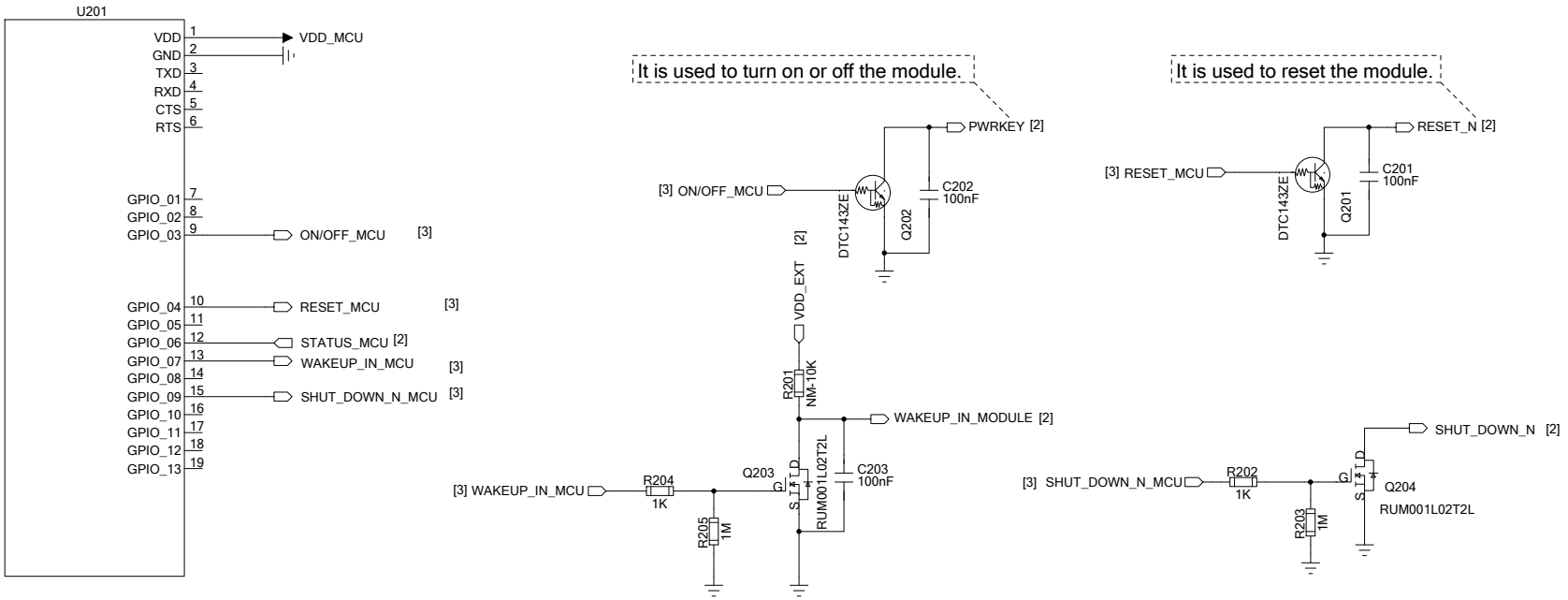
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 2 OF 8	DATE 2019/5/30

MCU Interfaces



Notes:

1. U201 represents customer's MCU.
2. SHUT_DOWN_N_MCU is an emergency option to shut down the module. When it is at high level, the module will be shut down.

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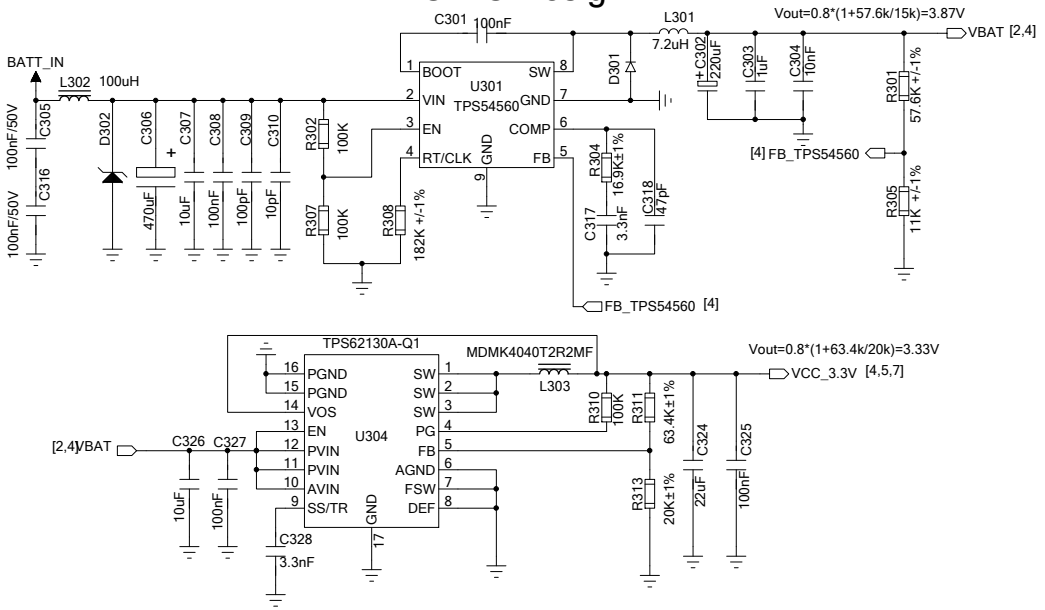
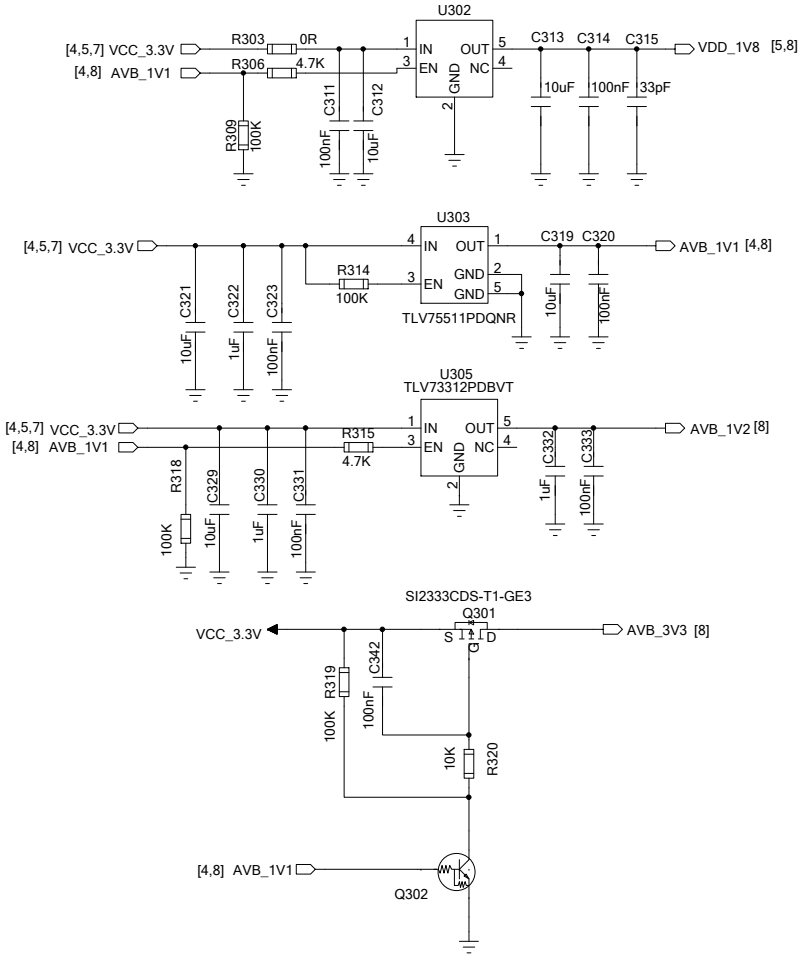
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 3 OF 8	DATE 2019/5/30

Power Supply Design

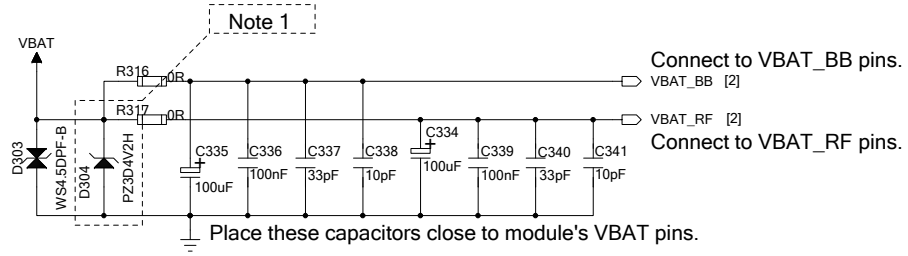
DC-DC Design



Supply Power for EAVB and PHY



VBAT Design



Notes:

1. The zener diode D304 will generate about 3uA leakage current under 3.8V power supply.
2. The power supply must be able to provide sufficient current up to 2A or more.
3. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
4. The recommended operating voltage of VBAT is 3.3V~ 4.3V.

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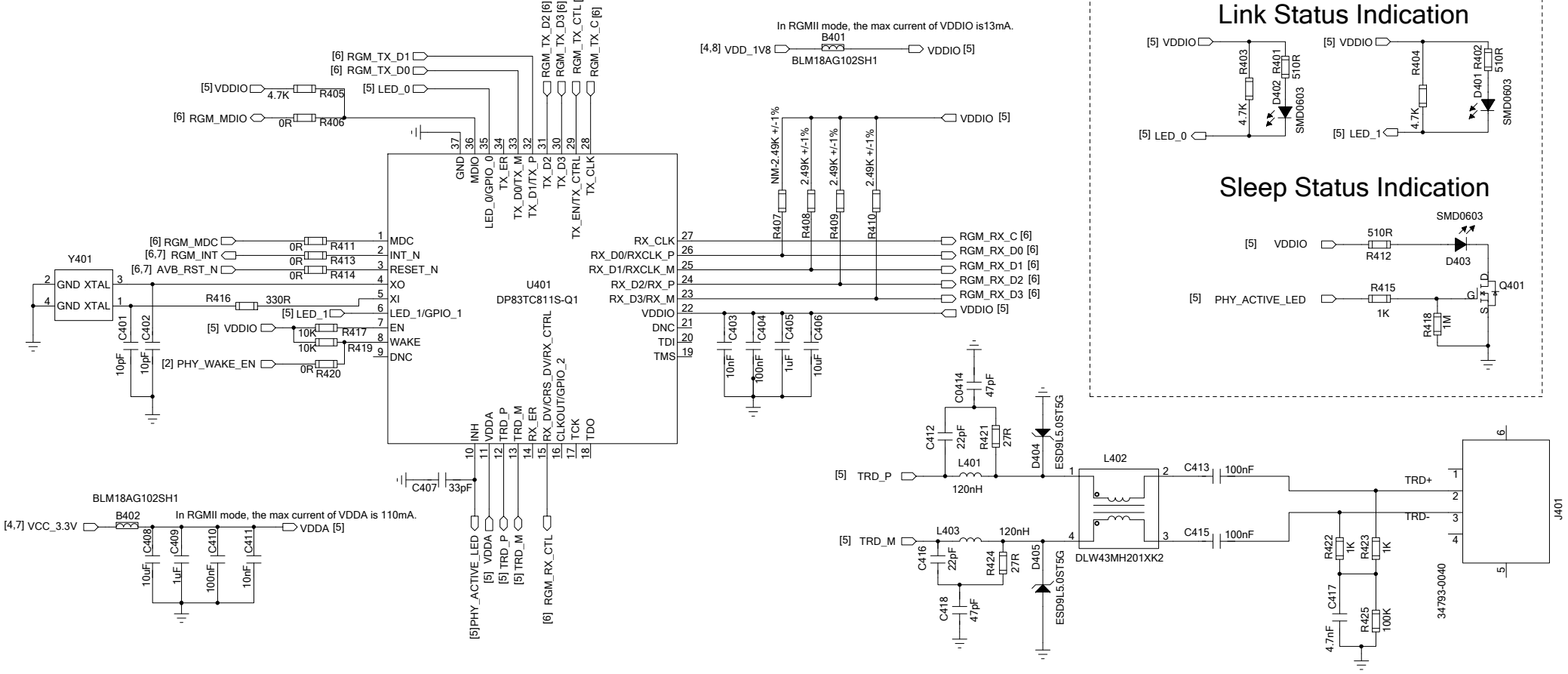
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 4 OF 8	DATE 2019/5/30

PHY (DP83TC811S-Q1) Design



Status Indication LEDs

RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
Note: In band status is valid when RX_CTRL is low	Duplex Status: 0 = Half-Duplex 1 = Full-Duplex	RX_CLK Clock Speed: 00 = 2.5MHz 01 = 25MHz 10 = 125MHz 11 = Reserved	Link Status: 0 = Link not established 1 = Valid link established

Notes:

1. VDDIO and VDDA ramp delay offset of DP83TC811S-Q1: ±50ms.
2. The PHY address is 0x00 by default.
3. This reference design is configured for Physical Medium Attachment Slave Mode.
4. Place the clock source near the XI and XO pins, and it is recommended to keep 50Ω impedance control for the control signals.
5. RX_CTRL/RX_CLK/RX_D0~RX_D3 and TX_CTRL/TX_CLK/TX_D0~TX~D3 must be routed with 50Ω±10% single-ended impedance control.
   The dealy of RX_CLK and TX_CLK is configured through the register of PHY.
   TRD_M and TRD_P must be routed with 100Ω±10% differential impedance control, and keep the reference ground complete and integral.
6. It is recommended to maintain the intra-lane spacing of control signals and intra-pair spacing of data signals both as three times of the trace width.
7. It is important to route the data and control signals with total grounding, and keep them away from sensitive signals.

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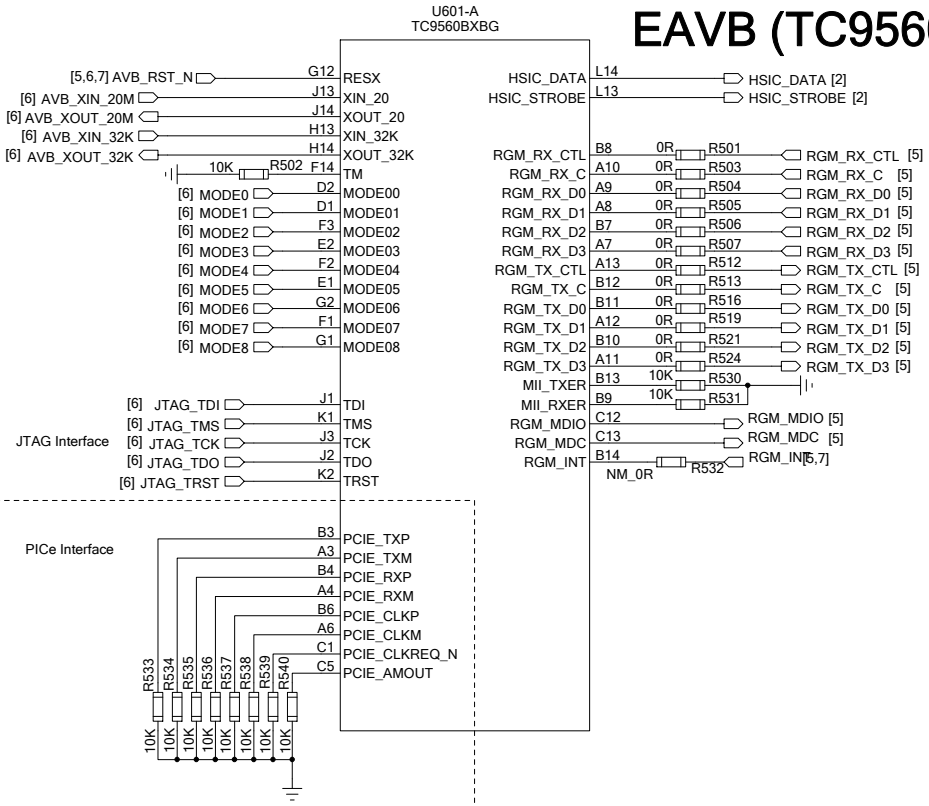
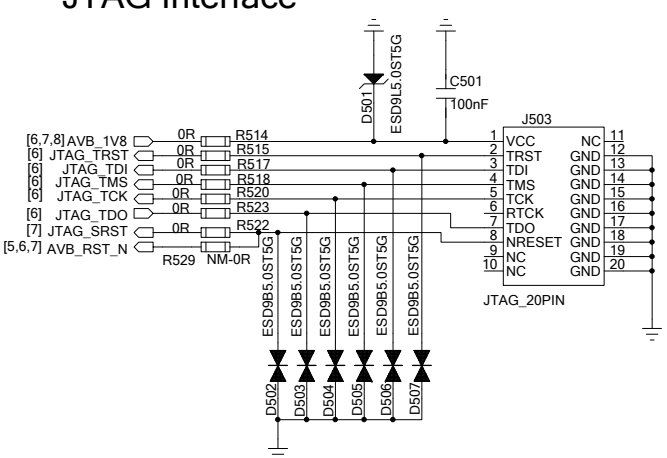
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 5 OF 8	DATE 2019/5/30

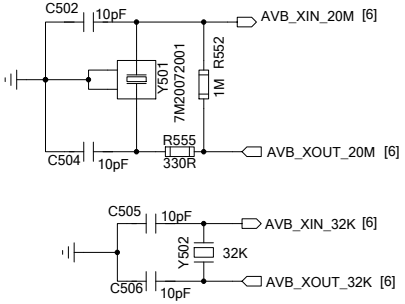
EAVB (TC9560BXBG) Design 1



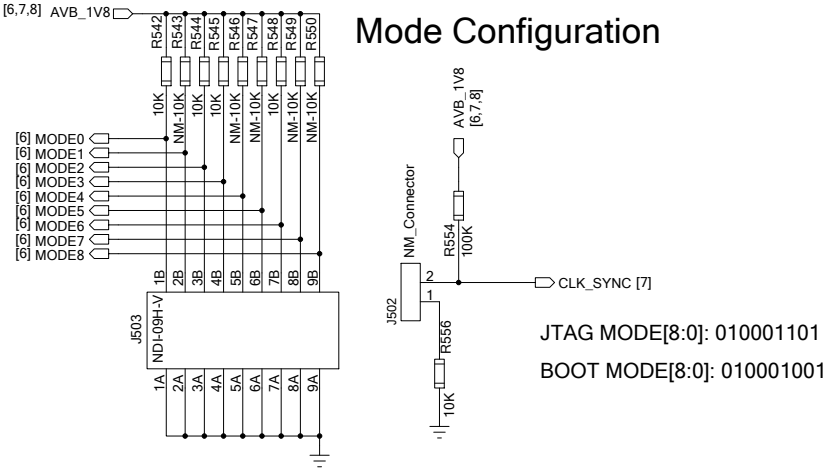
JTAG Interface



Clock



Mode Configuration



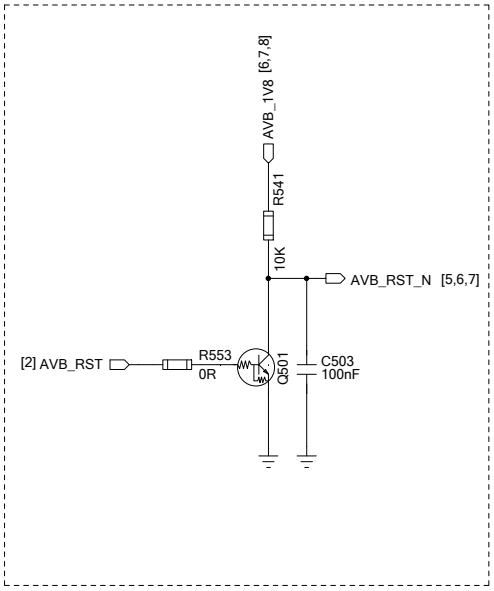
JTAG MODE[8:0]: 010001101

BOOT MODE[8:0]: 010001001

Note:

When CLK_SYNC is pulled down, PCIe interface will be used for firmware downloading.

When CLK_SYNC is pulled up, JTAG interface will be used for firmware downloading.



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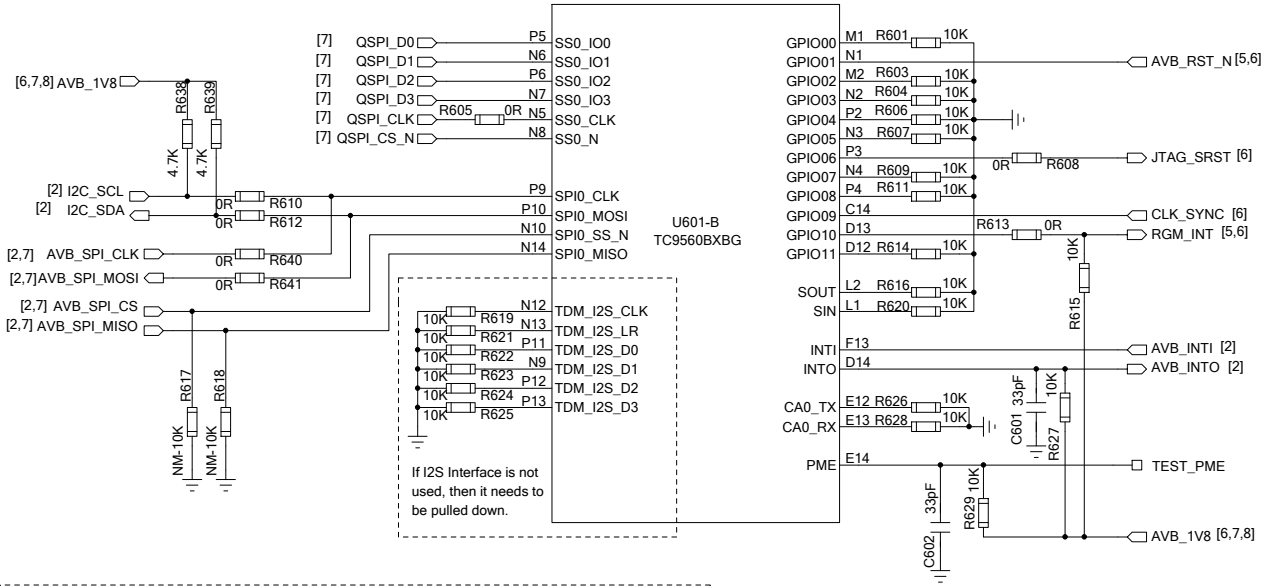
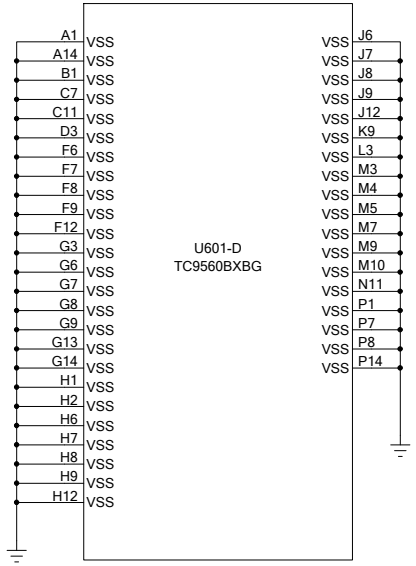
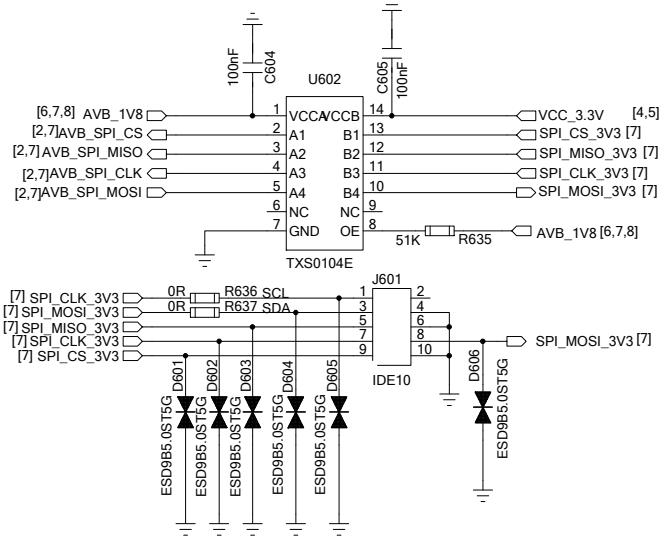
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 6 OF 8	DATE 2019/5/30

EAVB (TC9560BXBG) Design 2

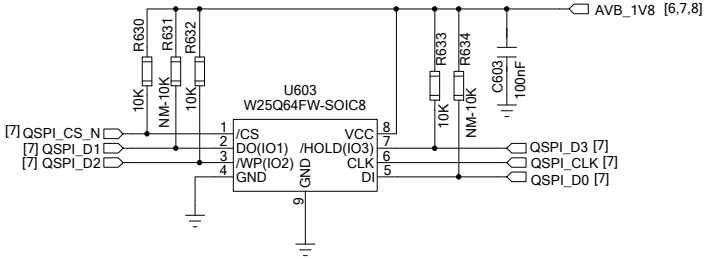




SPI&I2C Download Interfaces



SPI Flash



Note:
TC9560BXBG enters boot mode through the external flash.

SPI/I2C Mode Design

Mode	Mount	Not Mount
I2C	R610/R612/R638/R639 R617/R618	R640/R641
SPI	R640/R641	R610/R612/R638/R639 R617/R618

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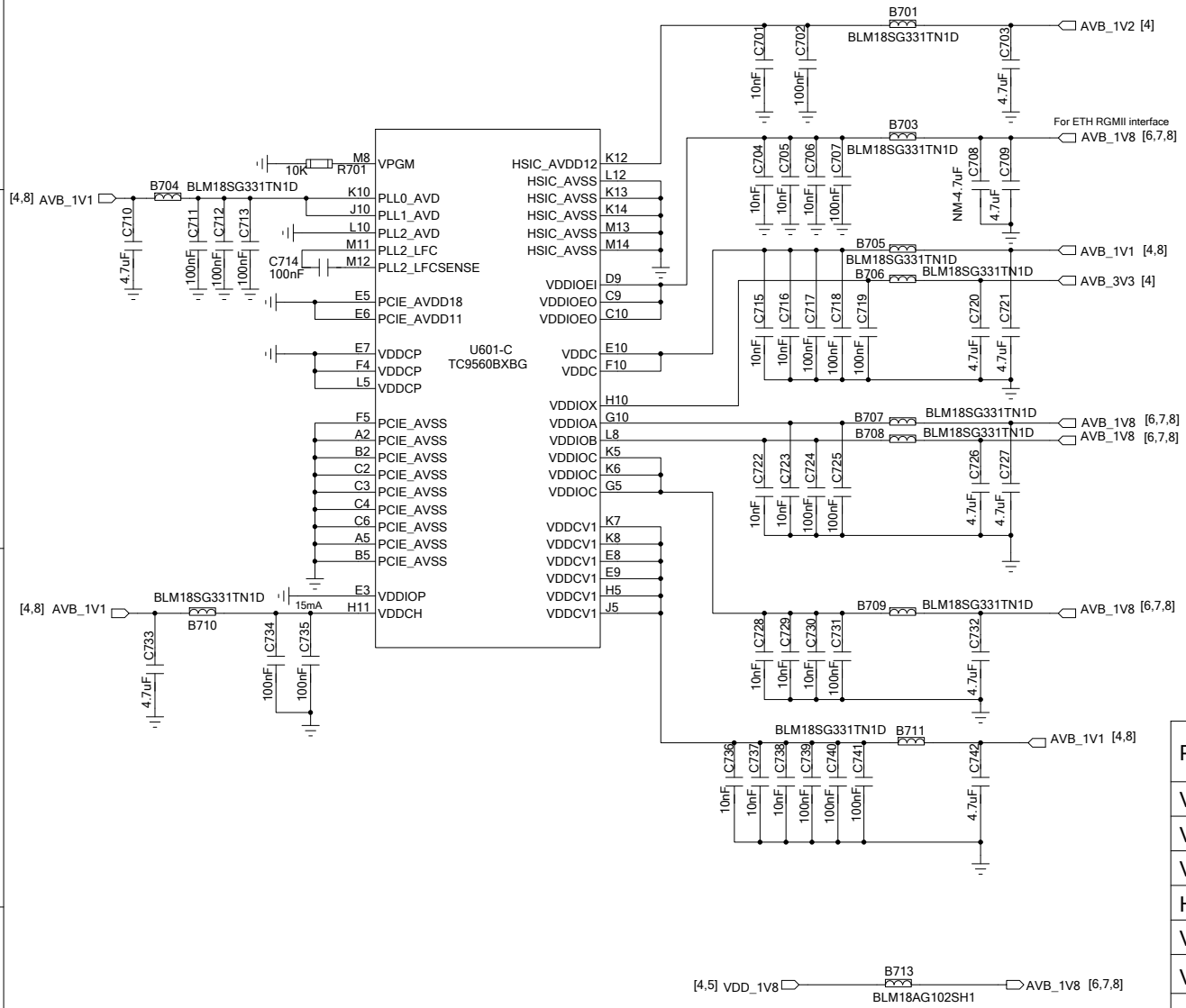
DRAWN BY Eden LIU	PROJECT AG35-Quecopen	TITLE EAVB Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 7 OF 8	DATE 2019/5/30

EAVB (TC9560BXBG) Design 3



Parameter	Condition	Max.	Unit
VDDC	1.0V~1.2V	5	mA
VDDCV1, PLLO_AVD, PLL1_AVD, PLL2_AVD	1.0V~1.2V	130	mA
VDDCH	1.0V~1.2V	15	mA
HSIC_AVDD12	1.1V~1.3V	3	mA
VDDIOEI, VDDIOEO	1.7V~1.9V	30	mA
VDDIOX	3.0V~3.6V	3	mA
VDDIOA, VDDIOB, VDDIOC	1.7V~1.9V	15	mA

Note:
Power-on sequence of TC9560BXBG: power on VDDC/VDDC1/VDDCH first,
then VDDIOX/VDDIOA/VDDIOB/VDDIOC/VDDIOEI/VDDIOEO, and finally pull up RESX.

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CHECKED BY Yeoman CHEN	SIZE A2	VER 1.0
	SHEET 8 OF 8	DATE 2019/5/30