AG35-QuecOpen

Reference Design

Automotive Module Series

Rev. AG35-QuecOpen_Reference_Design_V1.5

Date: 2019-11-26

Status: Released

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About the Document

Revision History

Revision	Date	Author	Description
1.0	2018-06-05	Canice CHEN	Initial
1.1	2018-09-21	Canice CHEN	1. Updated schematic designs relating USB. 2. Updated the power supply block diagram in Sheet 3. 3. Updated the notes for “VBAT Design” section in Sheet 4. 4. Updated the schematic designs and the notes in Sheet 8. 5. Added sensor design in Sheet 13. 6. Changed Q0401/Q0402/Q0602/Q1002/Q1501 from digital transistors to MOS transistors and updated their corresponding circuit designs.
1.2	2018-11-21	Canice CHEN	1. Added C0101 and C0804 in Sheet 1 and Sheet 8, respectively. And both of them are reserved. 2. Updated the design of SHUT_DOWN and the corresponding notes in Sheet 2. 3. Updated the 3.3V/3.8V power supply designs and the block diagram, and additionally added a note in Sheet 3. 4. Updated the design of VDD_CODEC in Sheet 4. 5. Updated the notes for “MDI Low Pass Filter Schematic” section in Sheet 9. 6. Updated the design of STATUS in Sheet 15.
1.3	2019-01-25	Canice CHEN	1. Added a control circuit for the 3.3V DC-DC power supply system in Sheet 3. 2. Updated the note (item 4) and the 3.3V power supply design for eMMC in Sheet 10. 3. Updated R1119 into “NM_0R” (not mounted, 0Ω) in Sheet 11. 4. Updated sensor IC connection interface into I2C1

			interface in Sheet 13. 5. Updated the notes (item 3 and item 4) in Sheet 13.
1.4	2019-05-16	Canice CHEN	1. Enabled HSIC interface (pin 194/195) in Sheet 1. 2. Updated the wakeup pin into pin 61 (GPIO2) in Sheet 1. 3. Updated power supply block diagram for UART in Sheet 3. 4. Added a 1.8V LDO and a control circuit for the UART power supply system in Sheet 4. 5. Updated the UART level translation (IC solution) circuit in Sheet 5. 6. Added pull-down resistors for COEX_UART in Sheet 11. 7. Updated the design for sensor IAM-20680 in Sheet 13. 8. Updated sensor IC connection interface into I2C2 interface in Sheet 13.
1.5	2019-11-26	Canice CHEN	1. Added the timing of PWRKEY and RESET_N in Chapter 1.2. 2. Added the block diagram in Sheet 1. 3. Changed the net name of GPIO8 from PHY_WAKE into PA_EN. 4. Changed the not mounted resistor R0203 into a mounted one in Sheet 4. 5. Updated the “VBAT Design” and the design for “MCU Controlled Power Supply” in Sheet 6. 6. Updated the design for “Audio - Speaker Application” and added the note (item 4) in Sheet 8. 7. Updated the design for “Audio - Speaker Application” and added the note (item 5) in Sheet 9. 8. Updated the sensor power supply design in Sheet 15. 9. Updated the indicators design in Sheet 17.

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1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel AG35-QuecOpen module, including the design of power supply, (U)SIM interface, UART interfaces, and audio interfaces.

1.2. Timing of PWRKEY and RESET_N

During application design, please strictly follow the logic control and timing of PWRKEY and RESET_N.

The power-on scenario is illustrated in the following figure.

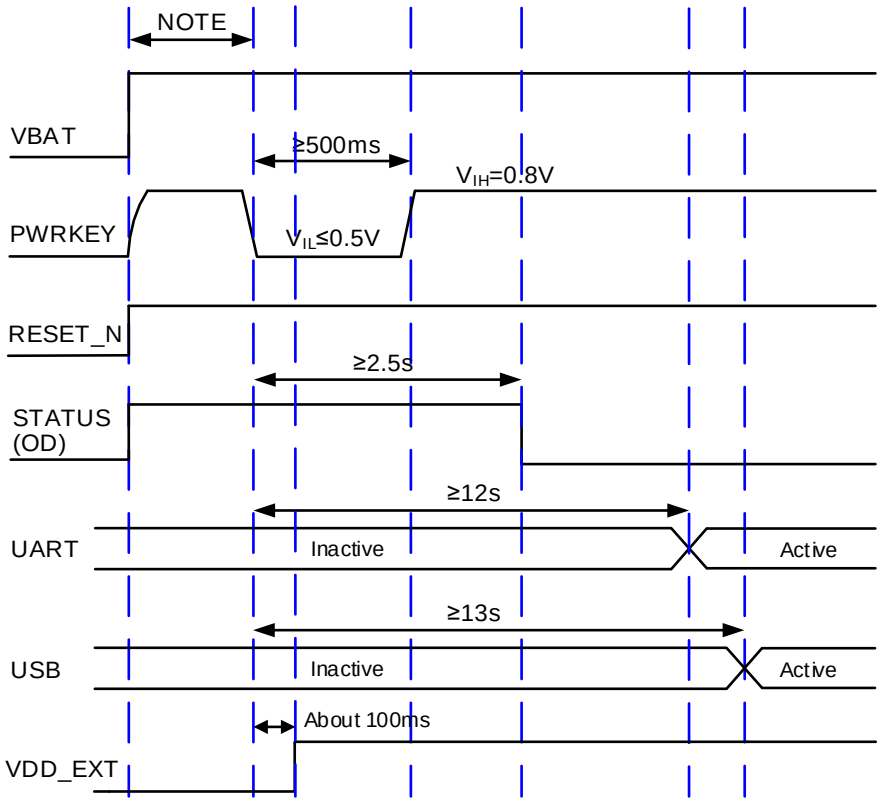


Figure 1: Timing of Turning on Module

Driving PWRKEY low for at least 650ms, the module will execute power-off procedure after the PWRKEY is released. The power-off scenario is illustrated in the following figure.

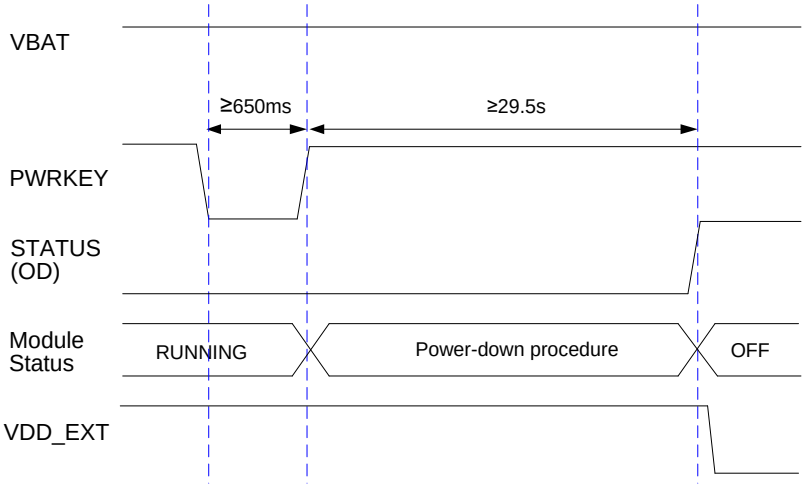


Figure 2: Timing of Turning off Module

The reset scenario is illustrated in the following figure.

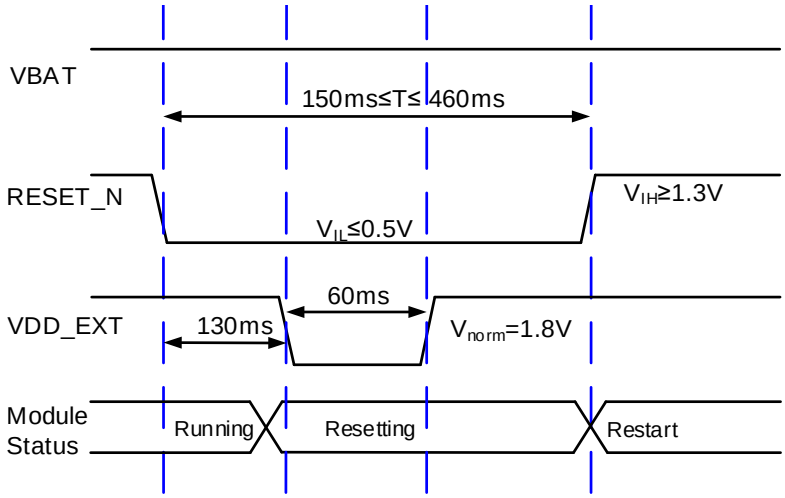


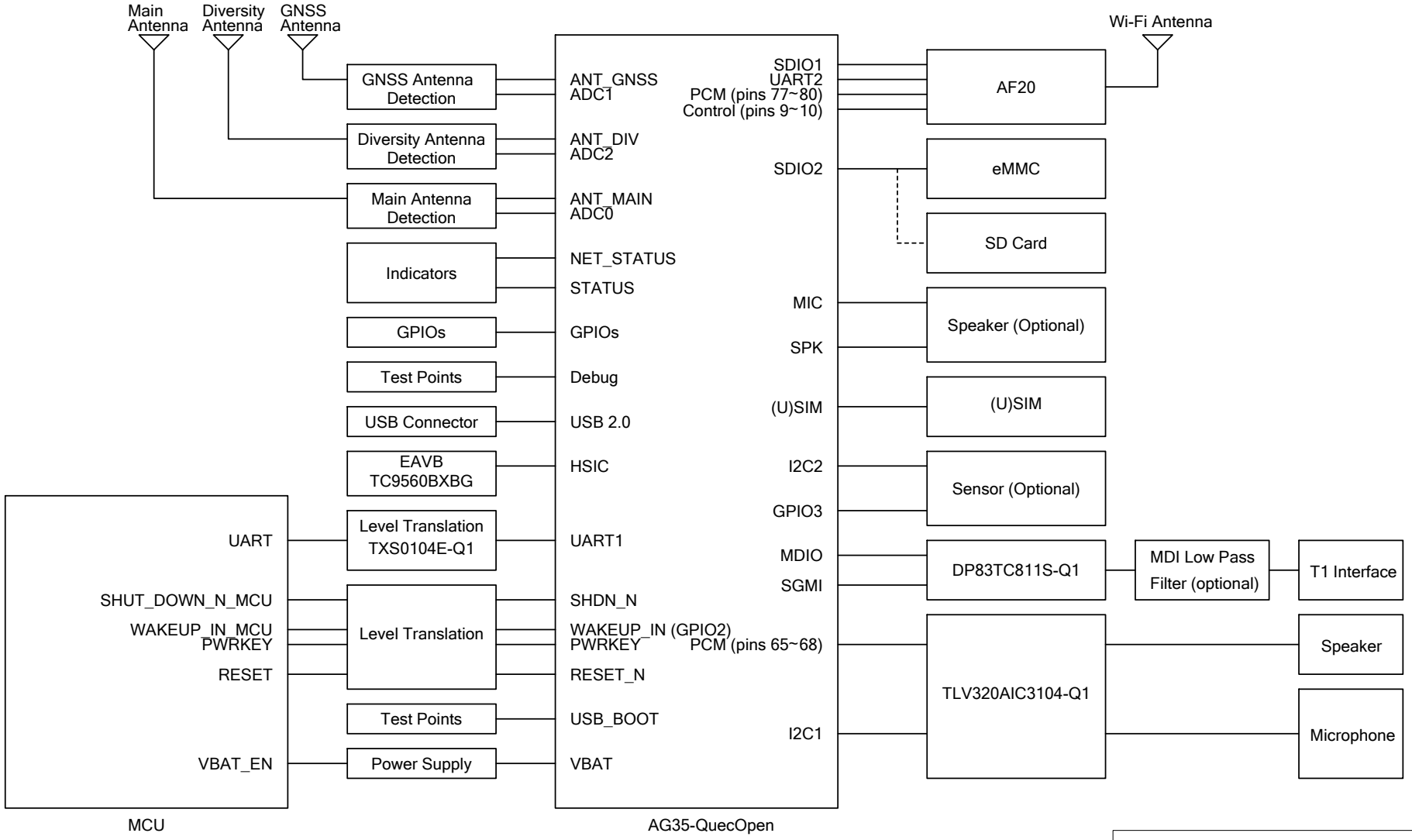
Figure 3: Timing of Resetting Module

For more details about the timing, please refer to *Quectel_AG35-QuecOpen_Hardware_Design*.

1.3. Schematics

The schematics illustrated in the following pages are provided for reference only.

Block Diagram



Notes:

1. Power domain of the MCU is 3.3V.
2. For more information about TC9560BXBG, please refer to *Quectel_AG35-QuecOpen_EAVB_Reference_Design*.

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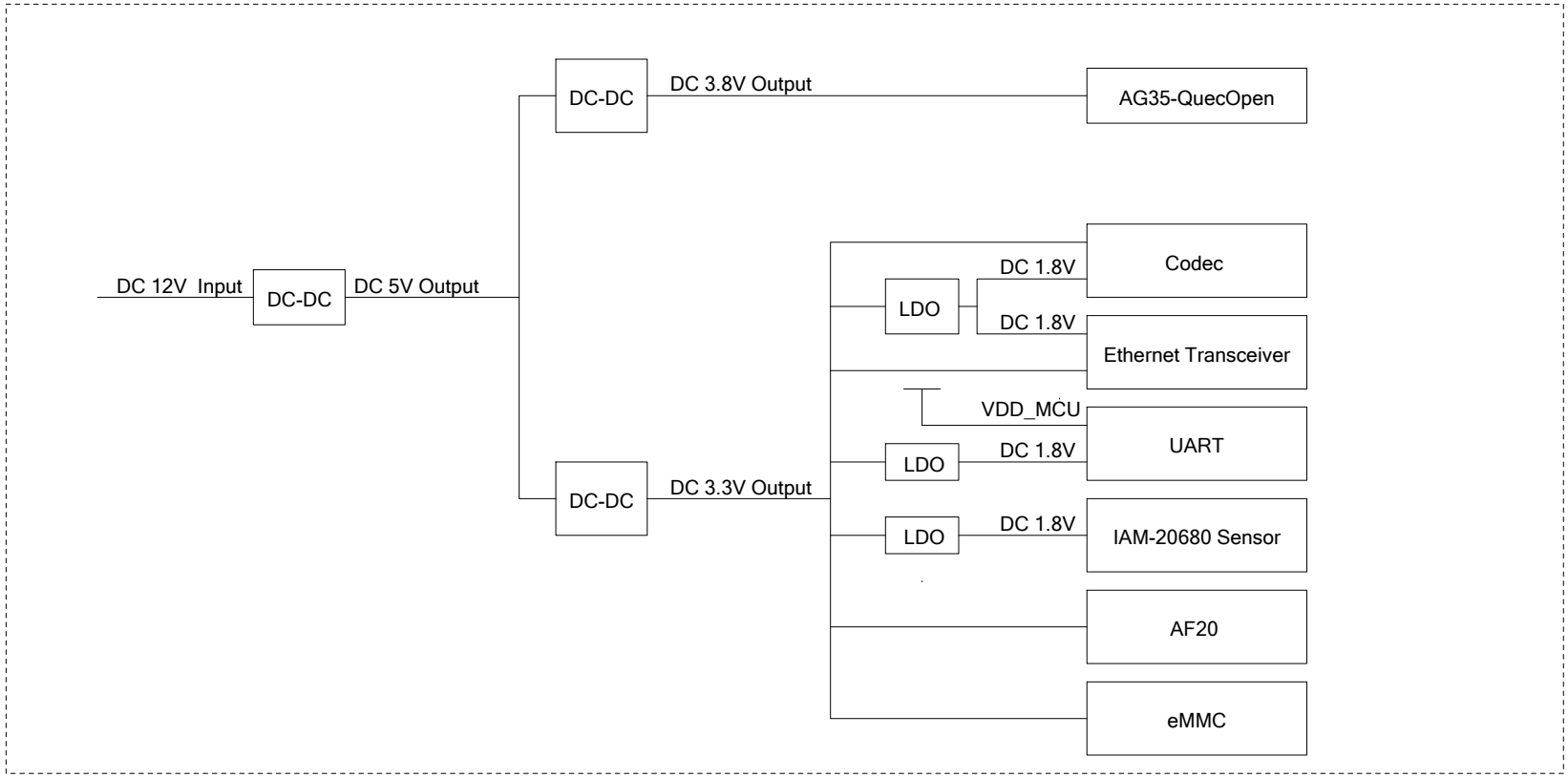
Power Supply Block Diagram

For DC-DC application, a DC-DC converter is used to convert a high input voltage into 5V, 3.8V and 3.3V outputs, and then the LDOs will generate 1.8V typical voltages.



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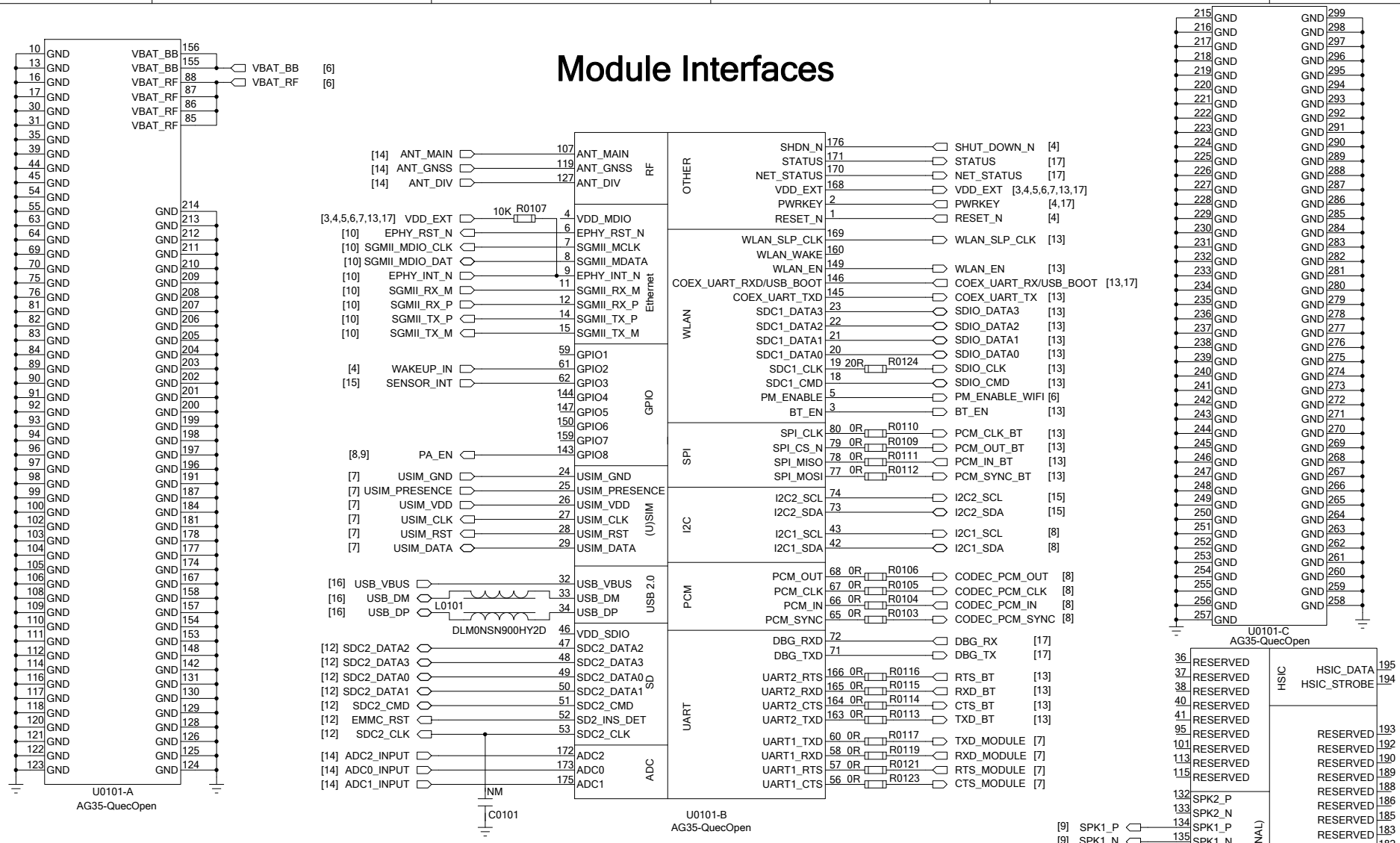
Module Interfaces



Notes:

1. ADC pins cannot be directly connected to the power supply and the test voltage must not exceed their respective voltage range.
2. Keep all RESERVED and unused pins unconnected, and ensure that all GND pins are connected to the ground network.
3. PCM_***_BT network is used for communication with AF20 module by default. CODEC_PCM_*** network is used for communication with external codec.
4. Pins 59, 65, 67, 144, 145, 146, 147, 149 and 159 must be at low level before the module starts up successfully. Pin 80 cannot be pulled down before power-up.
5. The module supports analog audio which is optional, and digital audio through PCM interface (pins 65~68). The two functions cannot be used synchronously.

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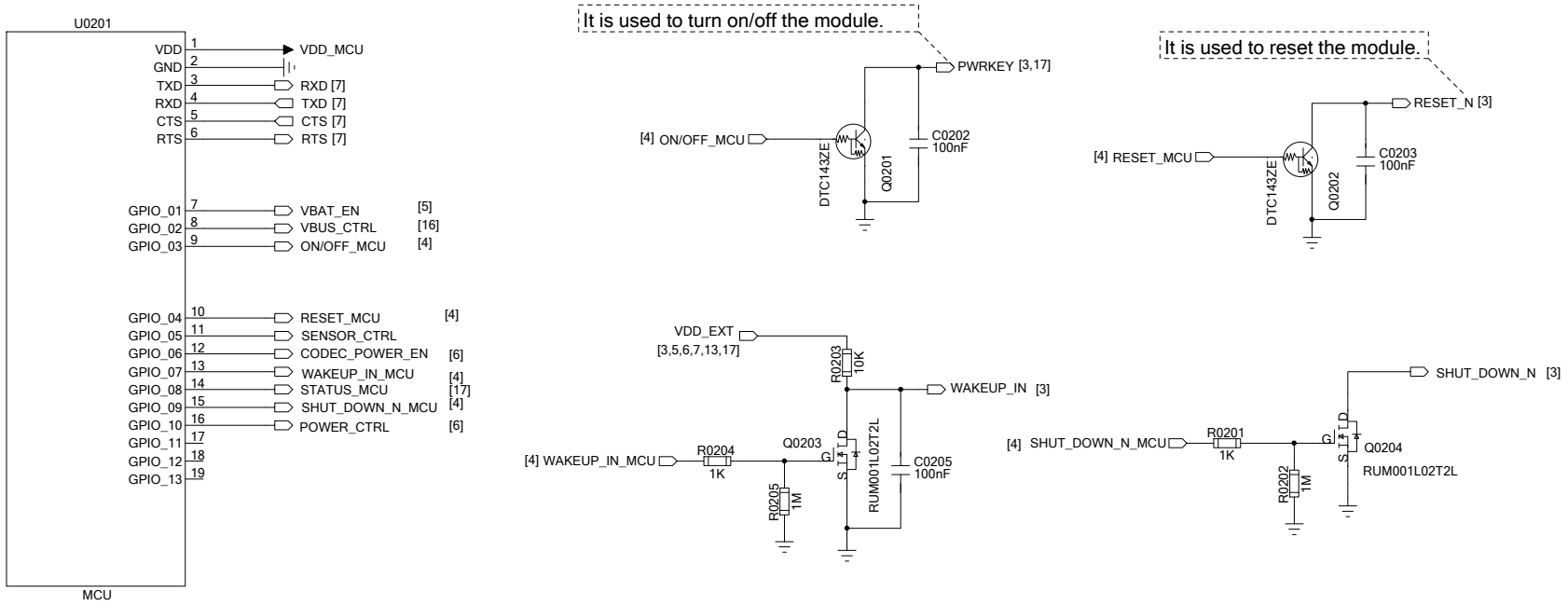
MCU Interfaces



Notes:

1. U0201 represents customer's MCU.
2. Transistor circuits (Q0201~Q0204) are used for level translation.
3. SHUT_DOWN_N_MCU is an emergency option to shut down the module.
   When it is at high level, the module will be forced to shut down.

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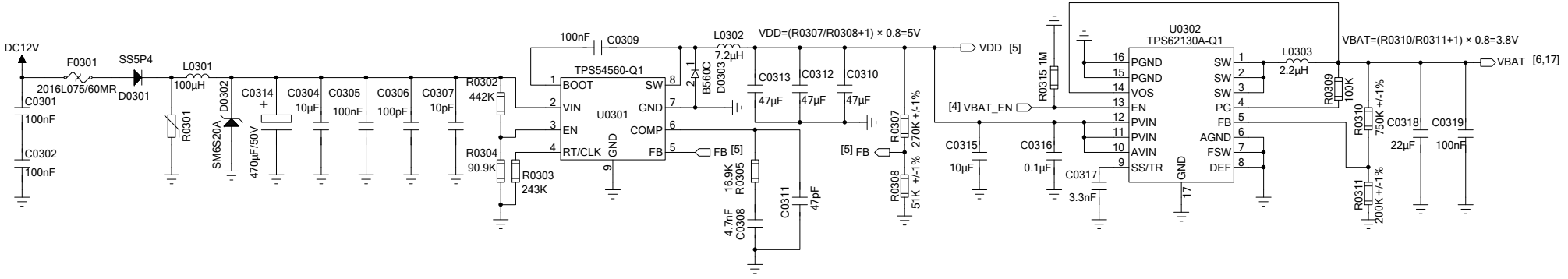
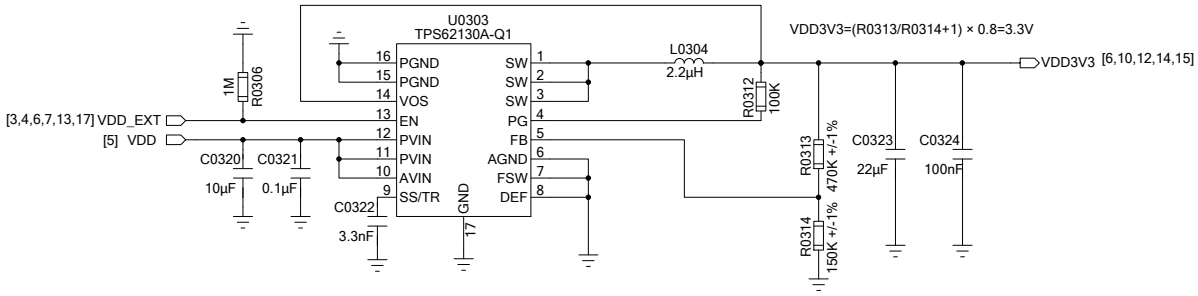
Power Supply Design (Part 1)

DC-DC Design

Module Power Supply



Codec, PHY, Sensor, AF20 and eMMC Power Supply



Notes:

1. The power supply must be able to provide sufficient current up to 3A or more.
2. VBAT_EN is used to control power supply of the module. It is at high level by default.
   When VBAT_EN is at low level, VBAT power supply will be switched off.

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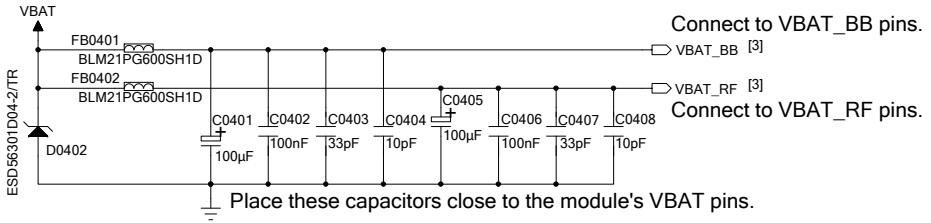
Power Supply Design (Part 2)

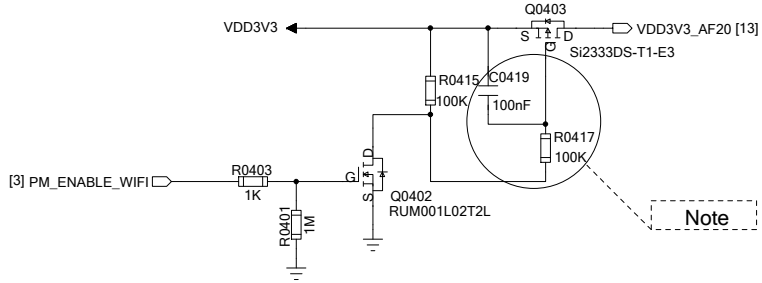
VBAT Design



Notes:

1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.
4. The capacitors C0401~C0408 should be placed close to the module's VBAT pins.

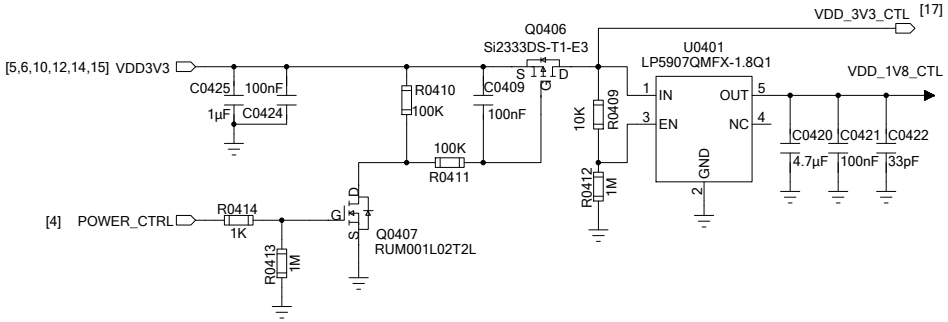
AF20 Power Supply



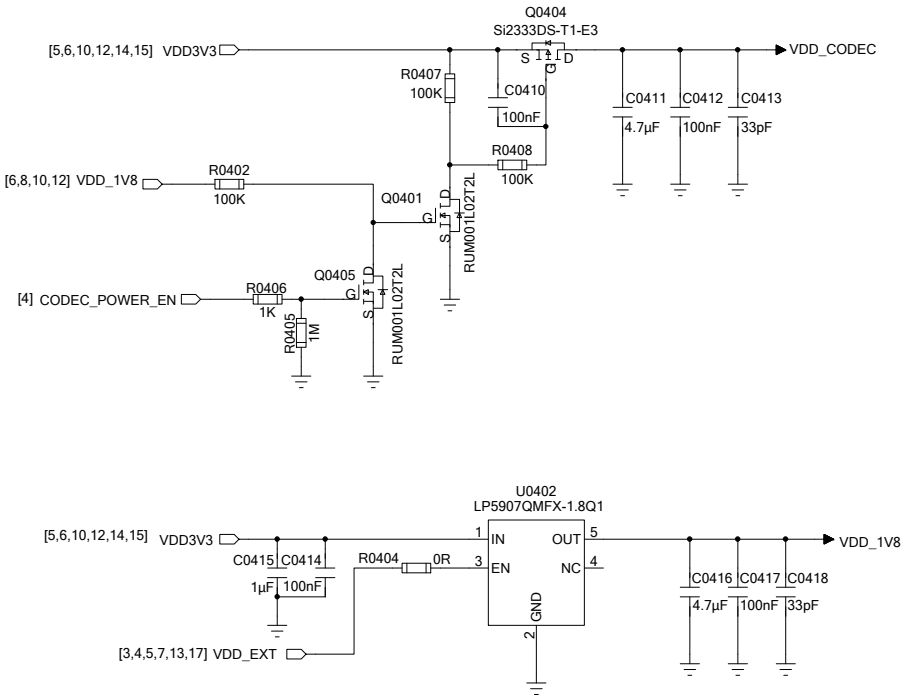
Note:

The RC circuit, which is assembled with R0417 and C0419, is used to delay the start-up of MOSFET switch circuit.

MCU Controlled Power Supply



PCM Codec Power Supply



Note:

CODEC_POWER_EN must be at low level to ensure normal work of PCM codec.
If VDD_CODEC power supply needs to be switched off, please keep CODEC_POWER_EN at high level.

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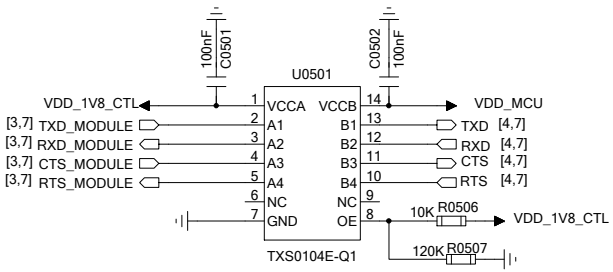
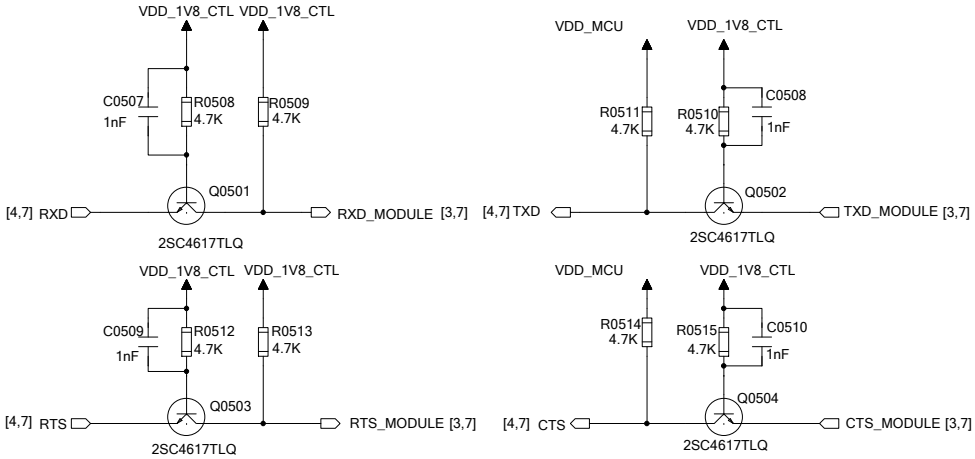
UART and (U)SIM Design

UART Level Translation - IC Solution (Recommended)



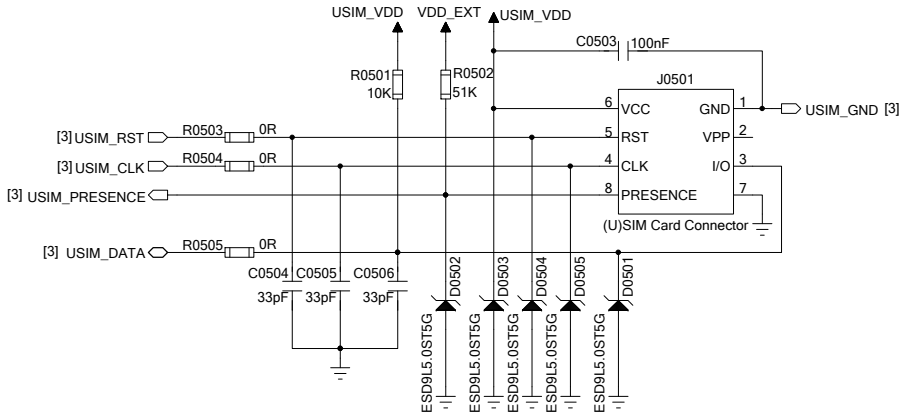
UART Level Translation - Transistor Solution



Notes:

1. It is recommended to use the voltage-level translation IC solution.
   The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. The supply voltage range of VCCA should not exceed that of VCCB. For more information about TXS0104E-Q1, please refer to the datasheet from Texas Instruments.
3. If high baud rate is needed, it is highly recommended to install four 1nF capacitors (C0507/C0508 /C0509/C0510) on transistor circiuts.

(U)SIM Interface



Notes:

1. The decoupling capacitors of USIM_VDD should be less than 1μF and must be placed close to the (U)SIM card connector.
2. AG35-QuecOpen module provides an input pin (USIM_PRESENCE) to detect whether the (U)SIM card exists or not. It supports both low level and high level detections.
   For more details, please refer to *Quectel_AG35-QuecOpen_Hardware_Design*.
3. R0503~R0505 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
4. It is recommended to take electrostatic discharge (ESD) protection measures near the (U)SIM card connector. The TVS diode with a junction capacitance of less than 10pF must be placed as close as possible to the (U)SIM card connector.
5. R0501 can improve anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.

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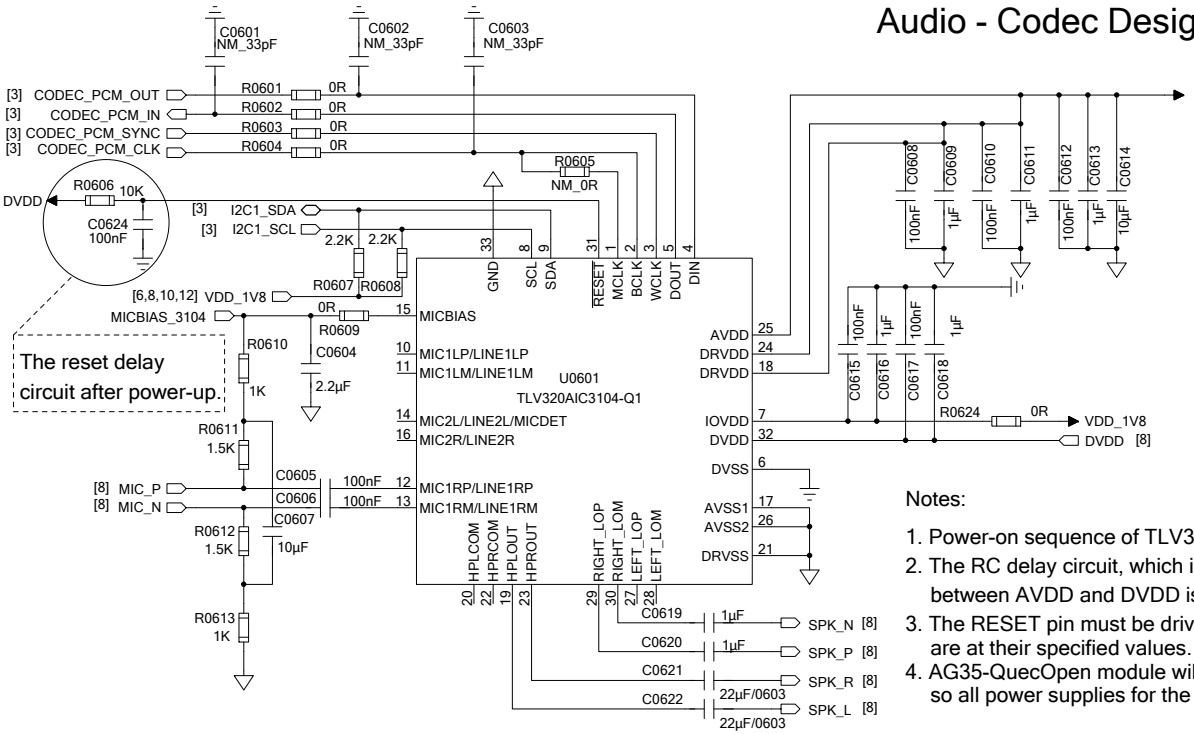
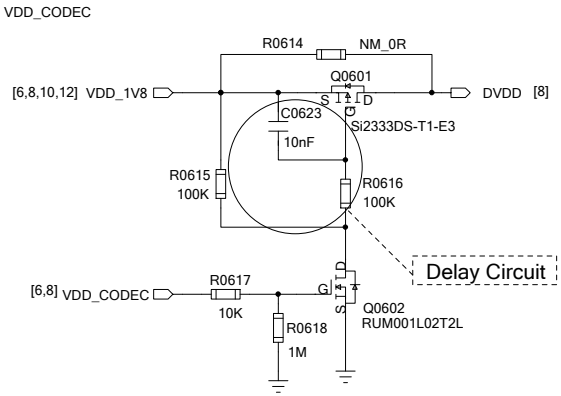
Analog Design (PCM Interface)

Audio - Codec Design

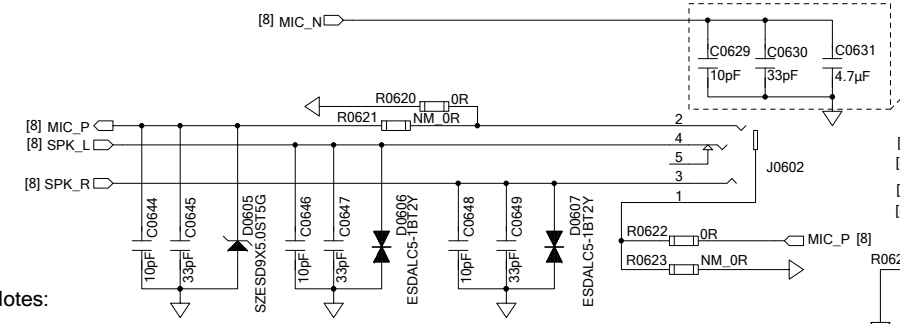




Notes:

1. Power-on sequence of TLV320AIC3104-Q1: IOVDD → AVDD/DRVDD → DVDD → Software Initialization
2. The RC delay circuit, which is assembled with C0623 and R0616, is used to ensure that the power-on time difference between AVDD and DVDD is within 5ms. For more details, please refer to TLV320AIC3104-Q1 datasheet.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104-Q1 are at their specified values.
4. AG35-QuecOpen module will automatically initialize the codec via I2C1 interface after it is turned on successfully, so all power supplies for the codec need to be turned on before that.

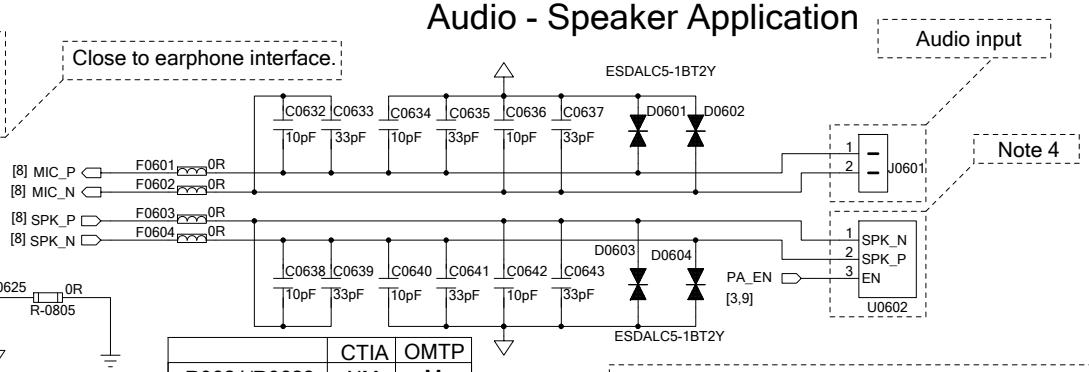
Audio - Earphone Application



Notes:

1. The analog output only drives earphone. For larger power loads such as speakers, the design for an audio power amplifier should be added.
2. The analog GND should be connected to the main GND via the 0Ω resistor (R0625).
3. The maximum capacitive loading for speaker is 330pF and the maximum capacitive loading for microphone is 250pF.
4. U0602 is a simplified speaker output circuit of an external power amplifier. In order to suppress POP, it is recommended to control the external power amplifier through PA_EN, making it turned-on after the module's audio function is established.

Audio - Speaker Application



	CTIA	OMTP
R0621/R0623	NM	M
R0620/R0622	M	NM

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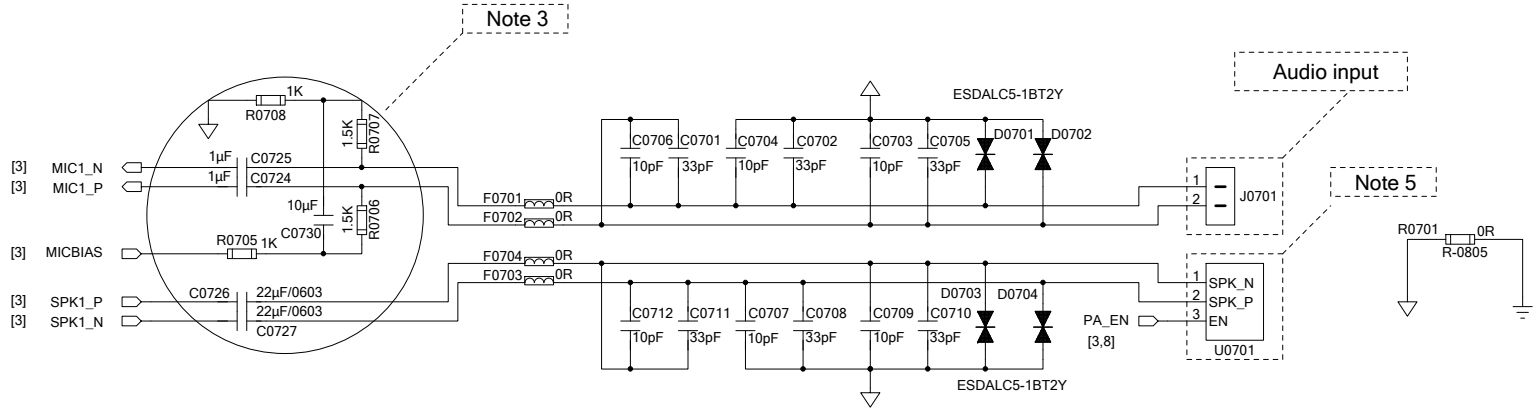
Analog Interface (Optional)

Audio - Speaker Application



Notes:

1. For larger power loads such as speakers, the design for an audio power amplifier should be added.
2. The maximum capacitive loading for speaker is 330pF and the maximum capacitive loading for microphone is 250pF.
3. The analog output and input interface circuits should be close to AG35-QuecOpen.
4. The analog GND should be connected to the main GND via the 0Ω resistor (R0701).
5. U0701 is a simplified speaker output circuit of an external power amplifier. In order to suppress POP, it is recommended to control the external power amplifier through PA_EN, making it turned-on after the module's audio function is established.

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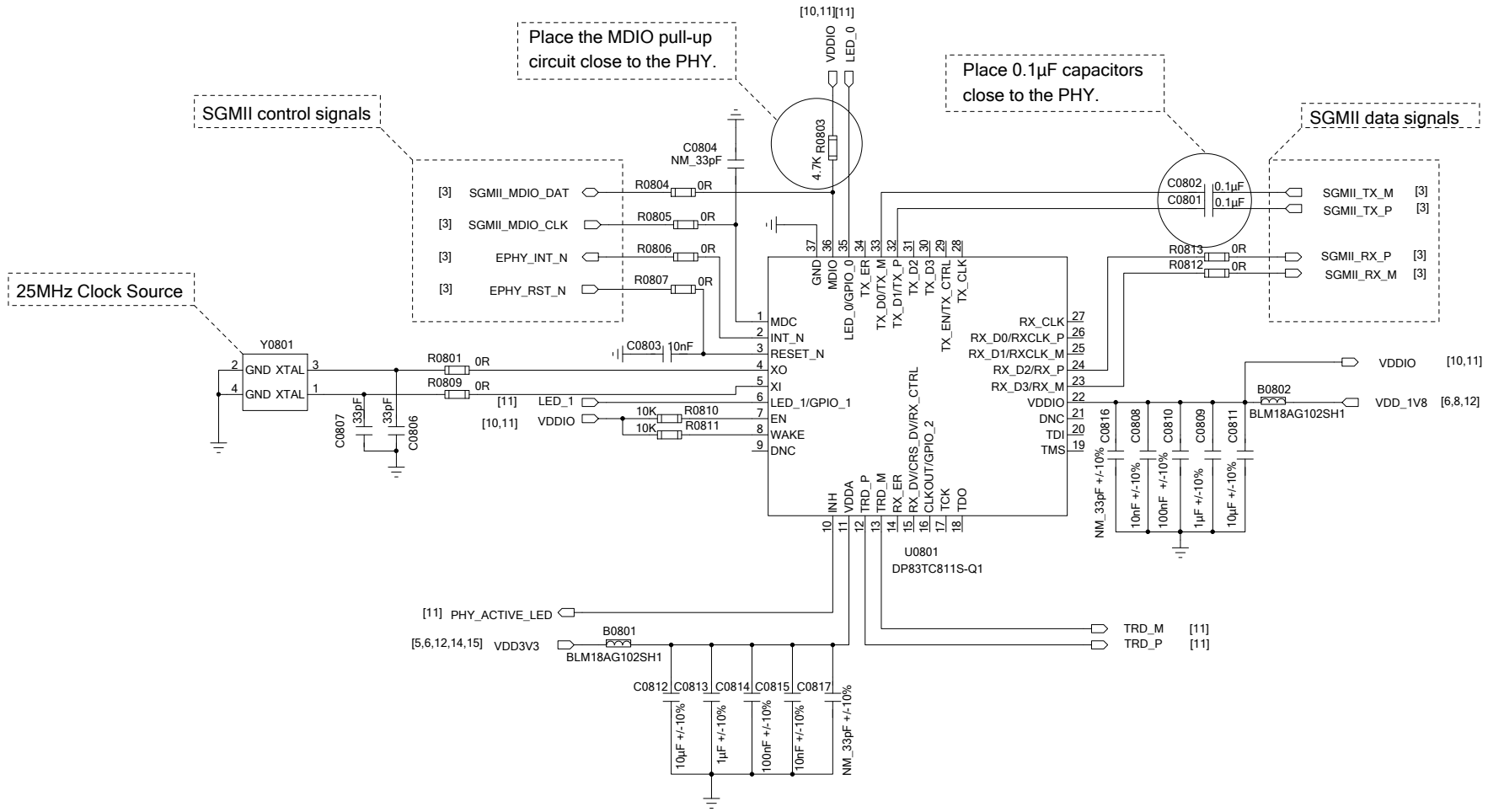
Ethernet Transceiver Design (Part 1)



Notes:

1. The PHY address is 0x00 by default.
2. This reference design is configured for Physical Medium Attachment Slave Mode.
3. Place the clock source near the XI and XO pins, and it is recommended to keep 50Ω impedance control for the control signals.
4. TRD_M and TRD_P, TX_M and TX_P, RX_M and RX_P must be routed with 100Ω±10% differential impedance control, and keep the reference ground complete and integral.
5. Keep the maximum trace length of data signals less than 25mm and keep the intra-pair length matching less than 0.5mm. In order to avoid crosstalk, it is recommended to keep at least three times of the trace width between the control/data signal traces and other signal traces.
6. It is important to route the data and control signals with surrounded ground on the current layer and with ground planes above and below, and keep them away from sensitive signals. The differential pairs are recommended to be routed on inner-layer of PCB.
7. The Ethernet transceiver is recommended to be designed on the same PCB on which the module is mounted, and at least a 4-layer PCB should be used.

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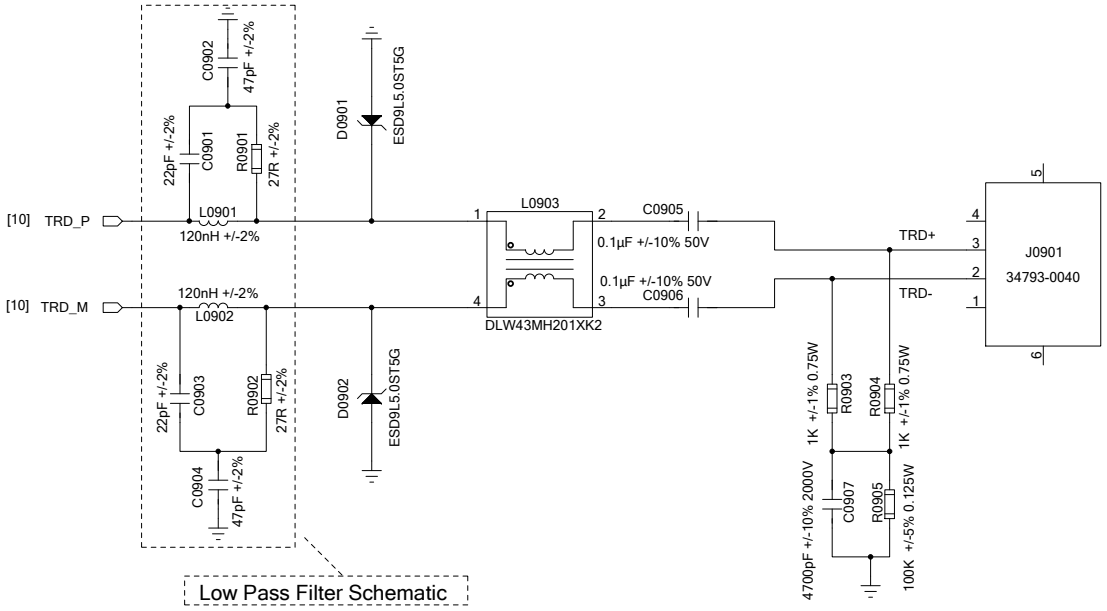
Ethernet Transceiver Design (Part 2)

MDI Low Pass Filter Schematic

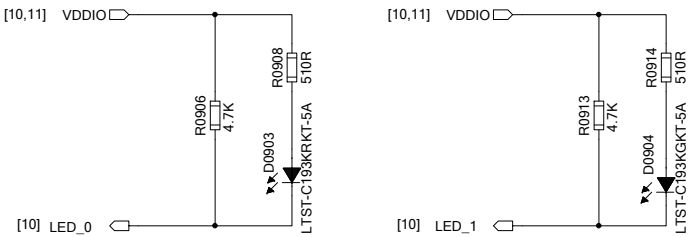


Notes:

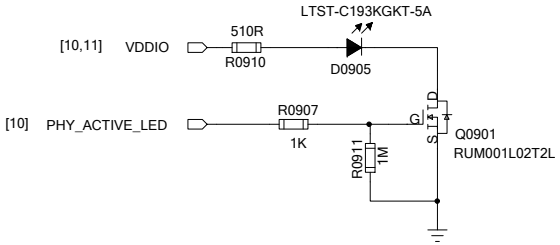
1. Create a top-layer copper pour keepout under the common-mode choke.
2. The low pass filter schematic is already available inside the PHY chip, and the external circuits and ESD circuits are optional.
3. The impedance of MDI TRD_M and TRD_P traces should be controlled as 100Ω while routing.

Indicators

Link Rate Indication LEDs



Operation Status Indication LED



Note:

The operation status indication LED will be turned on when the ethernet transceiver enters sleep or disabled mode.

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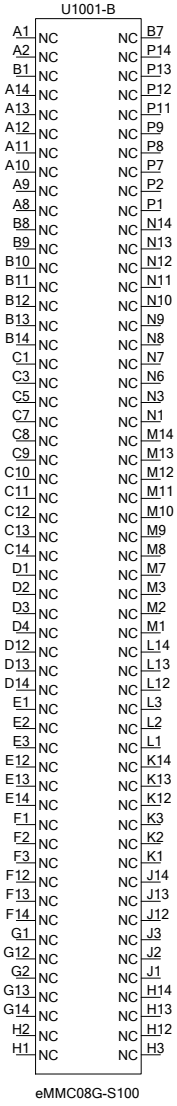
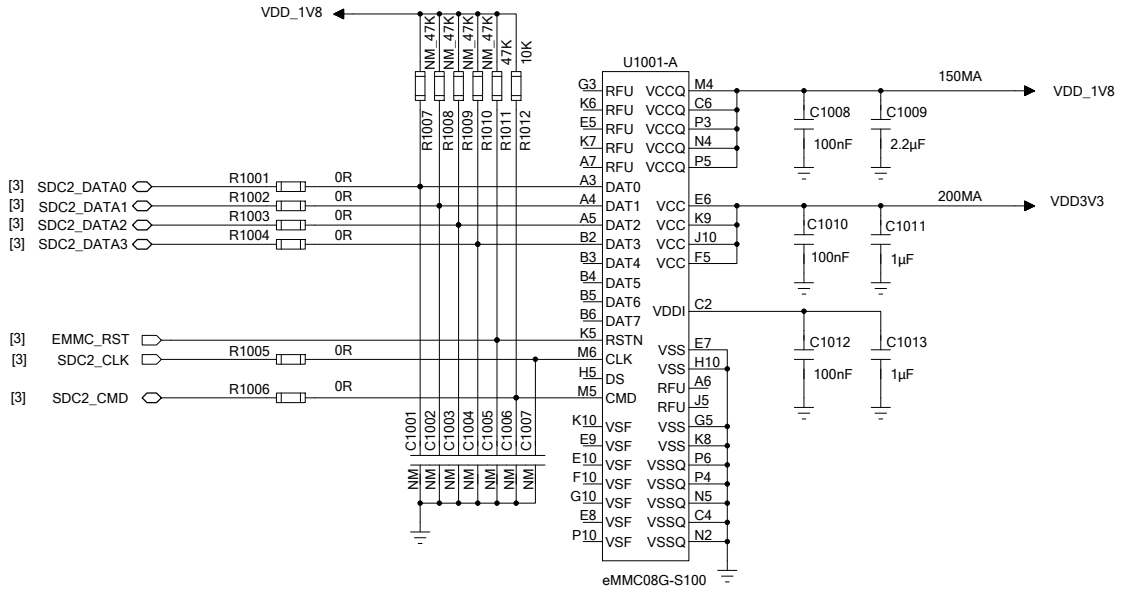
eMMC Design





Notes:

1. AG35-QuecOpen supports the following eMMC models: eMMC08G-S100, SDINBDG4-8G-I and MTFC4GMDEA-4M IT.
2. Typical value of power filter capacitors:

Model	C1008	C1009	C1010	C1011	C1012	C1013
eMMC08G-S100	100nF	2.2μF	100nF	1μF	100nF	1μF
SDINBDG4-8G-I	100nF	4.7μF	100nF	4.7μF	100nF	1μF
MTFC4GMDEA-4M IT	100nF	2.2μF	100nF	2.2μF	100nF	1μF

3. For more details, please refer to the datasheet of eMMC devices.
4. SDIO2 interface of AG35-QuecOpen supports eMMC by default, and also SD card through software configuration. eMMC and SD card cannot be supported synchronously. For more details, please contact Quectel Technical Support team.

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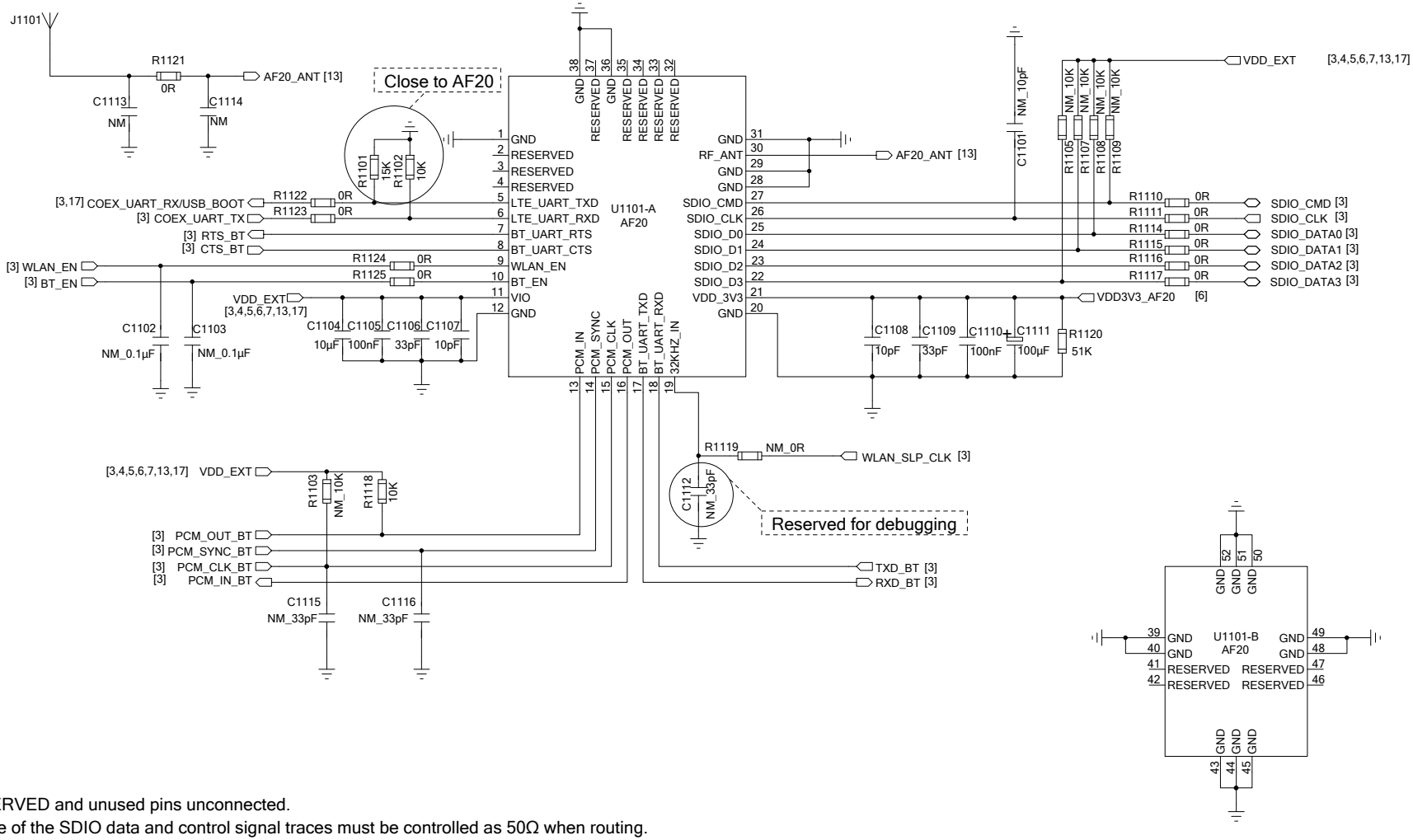
AF20 Design

AF20 Antenna Circuit



Notes:

1. Keep all RESERVED and unused pins unconnected.
2. The impedance of the SDIO data and control signal traces must be controlled as 50Ω when routing.
3. SDIO data lines should be surrounded with ground; SDIO_CMD and SDIO_CLK signal traces should be separately surrounded with gound on the current PCB layer, and with ground planes above and below.
4. It is recommended to use π type AF20 antenna circuit so as to facilitate future debugging.
5. The impedance of RF signal trace must be controlled as 50Ω when routing.

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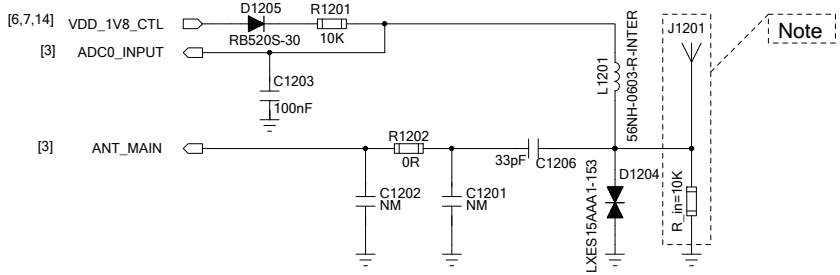
Antenna Interface and Antenna Detection Circuit Designs

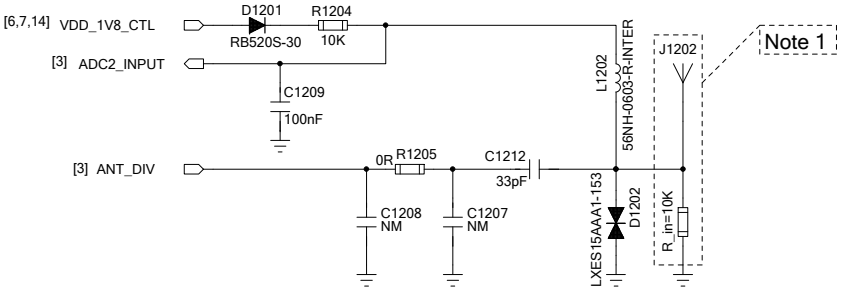
Main Antenna Interface and Detection Circuit (Normal)



Note:

In order to achieve successful antenna status detection, the main antenna is recommended to integrate an 8~13KΩ resistor (R_in) to GND. And the typical value for the resistor is 10KΩ.

Rx-diversity Antenna Interface and Detection Circuit (Normal)

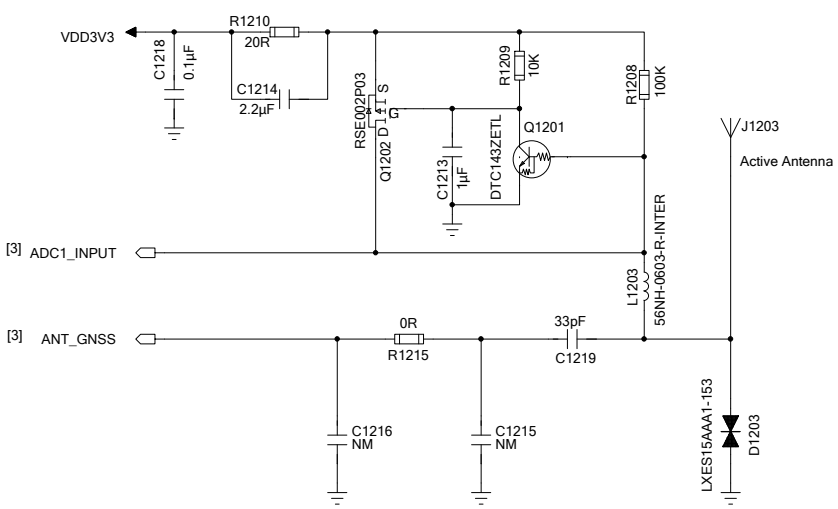


Notes:

1. In order to achieve successful antenna status detection, the Rx-diversity antenna is recommended to integrate an 8~13KΩ resistor (R_in) to GND. And the typical value for the resistor is 10KΩ.
2. The Rx-diversity reception function is ON by default. If Rx-diversity antenna is not used, there is a need to use AT command to turn off Rx-diversity reception.

Main / Rx-diversity Antenna Status Indication					
Antenna Status	Open	R_in=8KΩ	R_in=10KΩ	R_in=13KΩ	Short to GND
ADC Value	1.7V	0.7V	0.8V	0.9V	0V
Status Indication	Open	Normal	Normal	Normal	Short to GND

GNSS Antenna Interface and Detection Circuit (Normal)



GNSS Antenna Status Indication			
Antenna Status	Open	Normal	Short to GND
ADC Value	VDD3V3	VDD3V3-R1210 × I_GNSS	0V

Notes:

1. A low power active antenna is recommended to be selected.
2. An external LDO can be selected to supply power for active antenna.
3. VDD3V3 is the power supply for active antenna, and I_GNSS is the working current of active antenna.
4. The active antenna power supply shall not exceed VBAT voltage of the module. And ADC0 or ADC1 shall be selected for ADC value detection.

Notes:

1. It is recommended to use π type Main/Rx-diversity antenna circuit, so as to facilitate future debugging.
2. The impedance of the RF signal traces must be controlled as 50Ω when routing.
3. ADC value can be read by AT+QADC=<port>. For more details, please refer to *Quectel_AG35_AT_Commands_Manual*.
4. Three kinds of antenna status are designed to be detected: Normal, Short to GND and Open.
5. The antenna connection status is judged by the voltage detected on the ADC pins.

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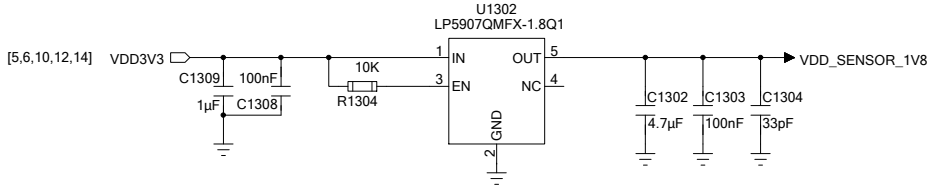
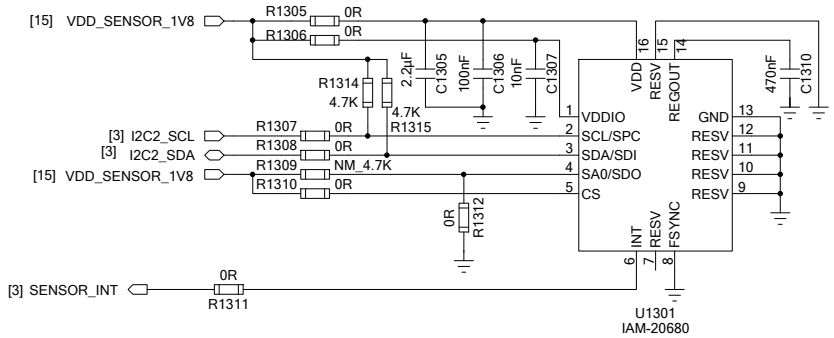
Sensor Design (Optional)

Sensor Power Supply





IAM-20680 I2C Addresses		
Connection	GND (Default)	1V8
SA0	0x68(1101000)	0x69(1101001)

Notes:

1. The device will enter sleep mode upon power-up.
2. If dead reckoning function is used, it is recommended to multiplex the UART1 interface into SPI2 interface for communication with MCU.
3. The module also supports sensor models such as SMI-130 from Bosch and ASM330LHH from STMicroelectronics.

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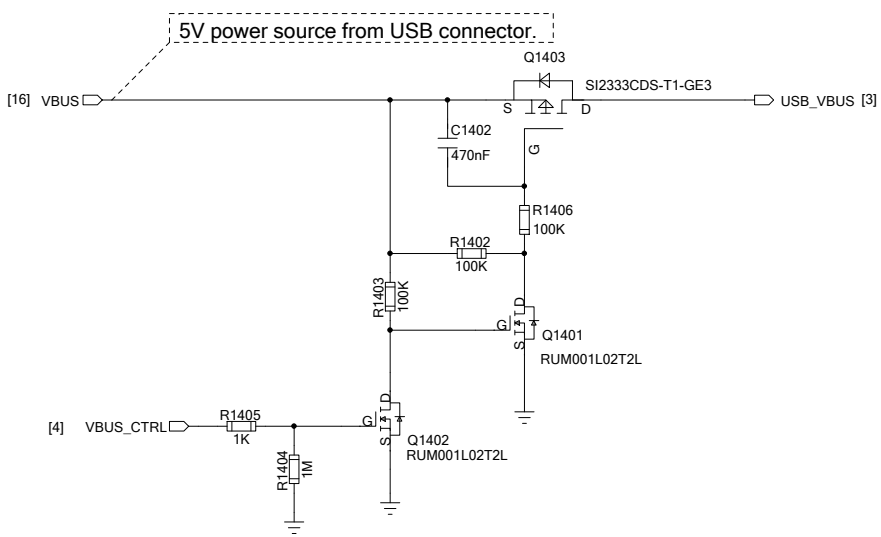
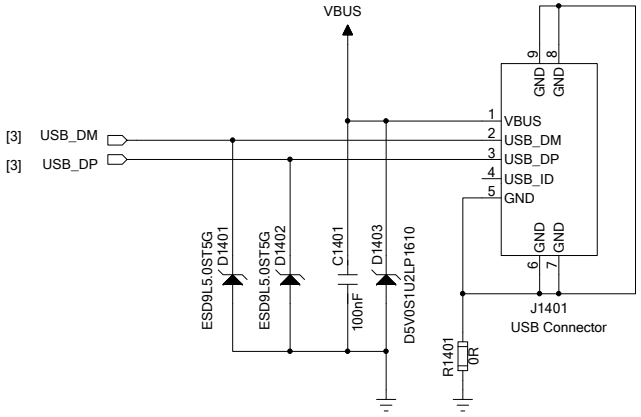
USB Interface





Notes:

1. AG35-QuecOpen can work as a USB device or USB host and supports Full Speed and High Speed modes.
   The USB_VBUS pin of AG35-QuecOpen should be powered by a 5V power system for USB detection.
2. USB interface can be used to debug and upgrade firmware.
3. Please note that the junction capacitance of ESD protection devices on USB data traces
   might influence the signal. Typically, the capacitance should be less than 2pF.
4. USB_VBUS should be controlled by USB host.
   VBUS_CTRL, controlled by MCU, is used to turn on/off USB_VBUS power supply.
   VBUS_CTRL is at low level by default. When it is at high level, USB_VBUS will be switched off.

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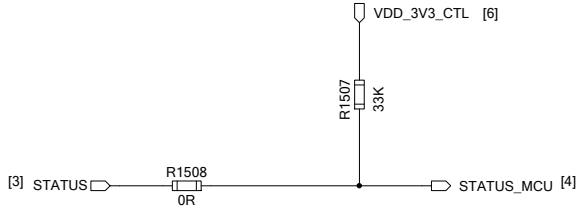
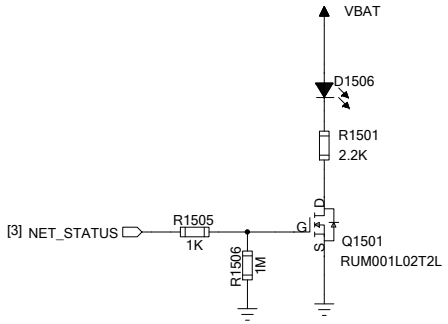
Indicators and Test Points

Indicators

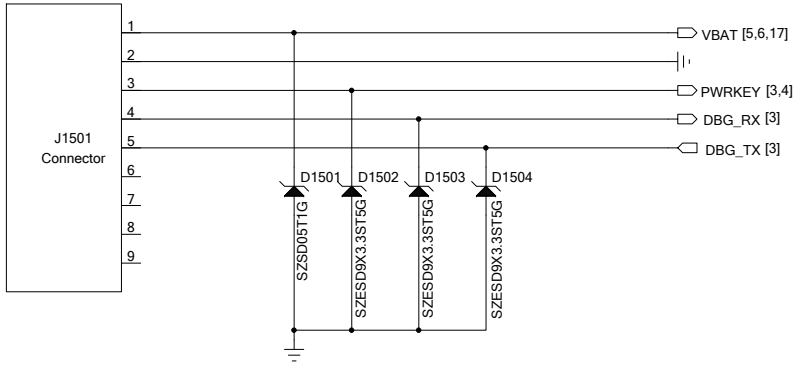




Notes:

1. The STATUS is an open drain output pin, and its drive current is less than 0.15mA.
2. For more details about STATUS and NET_STATUS, please refer to *Quectel_AG35-QuecOpen_Hardware_Design*.
3. If minimized power consumption is required when the device is in sleep mode, it is recommended to replace the power supply of indicators with a controllable one, and switch off the power when the module enters sleep mode.

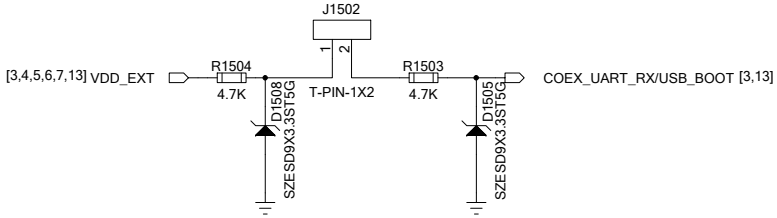
Reserved Test Points



Notes:

1. It is recommended to reserve the test points for debug UART interface so as to facilitate future debugging.
2. The debug interface supports 1.8V power domain. A level translator should be used if the power domain of customers' application is 3.3V.

USB_BOOT for Download



Note:

COEX_UART_RX/USB_BOOT keeps open by default. When it is at high level during module power-up, the module will be forced into download mode directly.

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