

# EC2x-Quecopen Switch Configuration of SPI and UART

# LTE Module Series

Rev. EC2x-Quecopen\_Switch\_Configuration\_of\_SPI-UART

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# **About the Document**

# **History**

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# 1 Introduction

From the perspective of user development, this document introduces how to switch the pin function when SPI and UART pins are multiplexed, which helps customers flexibly configure their peripheral resources for easy and fast development.





# 2 Pin Multiplexing Introduction

The EC2X platform provides a 4-line SPI interface which can also be configured as UART functions. Customers can configure them according to their needs.

# 2.1. SPI-UART Multiplexed Pin

SPI-UART multiplexed pins are shown as follow, also can refer to **Quectel\_EC20 R2.1\_QuecOpen\_GPIO\_Assignment\_Speadsheet**.

Table 1: SPI-UART Multiplexed Pin

	Pin lumber	Mode 1 (As default)	Mode 2	Mode 3	Reset Status	Wakeup Interrupt	Mark
SPI_CS_N	37	SPI_CS_N_ BLSP6	GPIO_22	UART_RTS_BLSP6	B-PD,L	YES	
SPI_MOSI	38	SPI_MOSI_ BLSP6	GPIO_20	UART_TXD_BLSP6	B-PD,L	YES	
SPI_MISO	39	SPI_MISO_ BLSP6	GPIO_21	UART_RXD_BLSP6	B-PD,L	YES	
							BOOT
SPI_CLK	40	SPI_CLK_ BLSP6	GPIO_23	UART_CTS_BLSP6	B-PU,H	NO	CONFI G_4

GPIO20, GPIO21, GPIO22, GPIO23 can be multiplexed by SPI6 and UART6, please note that SPI6 and UART6 are based on the node number in DTS.



# 3 Linux Kernel Configuration

In Linux systems, if users want to use peripherals, must have peripheral drivers. The main peripheral drivers are usually compiled directly into the kernel and when the system starts up, the peripherals would be loaded. The loading process is completed by the driver program.

# 3.1. SPI Driver Configuration

Under SDK directory, execute below command.

\$ make kernel\_menuconfig

```
SPI support
selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes,
for Search. Legend: [*] built-in [ ] excluded <>> module <>> module capable
                            -- SPI support
                           [ ] Bebug support for SPI drivers
                                 *** SPI Master Controller Drivers ***
                                Altera SPI Controller
                                 Utilities for Bitbanging SPI masters
                                 Cadence SPI controller
                                 GPIO-based bitbanging SPI Master
                                 Freescale SPI controller and Aeroflex Gaisler GRLIB SPI controller
                                 OpenCores tiny SPI
                                 Rockchin SPI controller driver
                               Qualcomm SPI controller with QUP interface
                                 NXP SCI815682/6828/683 12C to SPI bridge
Analog Devices AD-FMCOMMS1-EBZ SPI-I2C-bridge driver
                                 Xilinx SPI controller common module
                                 DesignWare SPI controller core support
                                  ** SPI Protocol Masters ***
                                 User mode SPI device driver support
                           <M>
                                 Ouectel spi channel device driver support
                                 Intineon (LEGZAB (for power switching)
```

Make sure the configuration in the red frame is completed. The first part is configured with the SPI bus driver, so that the EC2X platform can drive the SPI bus, the second is the SPI general device driver, the user can send and receive SPI through this driver, and the third is the 6-line SPI driver, which is up to the user to decide whether or not to configure it.

# 3.2. UART Driver Configuration

Under SDK directory, execute below command.

\$ make kernel menuconfig



```
Serial drivers
s submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excluderch. Legend: [*] built-in [ ] excluded <M> module < > module capable
                      < > 8250/16550 and compatible serial support
                          *** Non-8250 serial port support *
                      [ ] Early console using ARM semihosting
                      < > MAX3100 support
                      < > MAX310X support
                      <*> MSM UART High Speed: Serial Driver
                      <>> MSM UART High Speed : Legacy mode Serial Driver
                     [*] MSM High speed serial legacy mode console support
< > SCCNXP serial port support
                      < > SC16IS7xx serial support
                      < > Altera JTAG UART support
                      < > Altera UART support
                      < > SPI protocol driver for Infineon 6x60 modem (EXPERIMENTAL)
                      [*] Enable tty device interface for some SMD ports
                      < > Cadence (Xilinx Zynq) UART support
                      < > ARC UART driver support
                      < > Freescale lpuart serial port support
                      < > ST ASC serial port support
```

Make sure the configuration in the red frame is completed, in which, the second part is the uart driver for the multiplexed pins.



# 4 Switch Configuration of SPI and UART

At this time, there are already UART driver and SPI driver in kernel, please configure them in DTS to determine the use of GPIO20-23.

# 4.1. SPI Configuration

The UART driver in Linux already exists, when the user wants to use GPIO 20~23 as the UART, as long as it is enabled in DTS, Linux can load it normally.

Refer to Figure 1, the corresponding node number of SPI in DTS is 6, in the kernel directory, find file mdm9607-mtp.dtsi in the arch/arm/boot/dts/qcom/ directory, this file is the master switch of the peripheral. Find the SPI node with node number 6 and set status to "ok" to enable SPI, meanwhile, find the UART node with node number 6 and set status to "disabled" to disable UART. At this time, the function of GPIO20-23 is SPI.

```
00049:
00050: &spi 6 (
0005L:
            status =
00052: );
0005B:
       &blsp1 uart3
00054:
            status = "ok";
00055:
00056:
00057:
00058: &blsp1 uart2 (
            status = "ok";
00059:
                            //if need, user can enable by themselves
            pinctrl-names ="sleep", "default";
00060:
            pinctrl-0 = <&blsp1_uart2_sleep>;
00061:
00062:
            pinctrl-1 = <&blsp1 uart2 active>;
00063: );
00064
00065:
        &blsp1_uart6
                      'disabled'
00066:
            status =
00067:
```



# 4.2. UART Configuration

Refer to Figure 1, the corresponding node number of UART in DTS is 6, in the kernel directory, find file mdm9607-mtp.dtsi in the arch/arm/boot/dts/qcom/ directory, this file is the master switch of the peripheral. Find the UART node with node number 6 and set status to "ok" to enable UART, meanwhile, find the SPI node with node number 6 and set status to "disabled" to disable SPI. At this time, the function of GPIO20-23 is UART.

```
00050:
       &spi_b {
            status = "disabled";
00051:
00052:
00053:
00054: &blsp1_uart3 {
00055:
            status = "ok";
00056:
00057:
00058: &blsp1_uart2 (
            status = "ok";
                            //if need, user can enable by themselves
00059:
            pinctrl-names ="sleep", "default";
00060:
            pinctrl-0 = <&blsp1_uart2_sleep>;
00061:
            pinctrl-1 = <&blsp1_uart2_active>;
00062:
00063: );
00064:
00065:
        &blsp1 uart6
                      "ok";
            status =
00066:
00067:
00068:
```

# 4.3. Function Verification

Please refer to **Quectel\_EC2X-QuecOpen\_SPI\_Guidelines** and **Quectel\_EC2X-QuecOpen\_UART\_Guidelines** to verify the corresponding function.