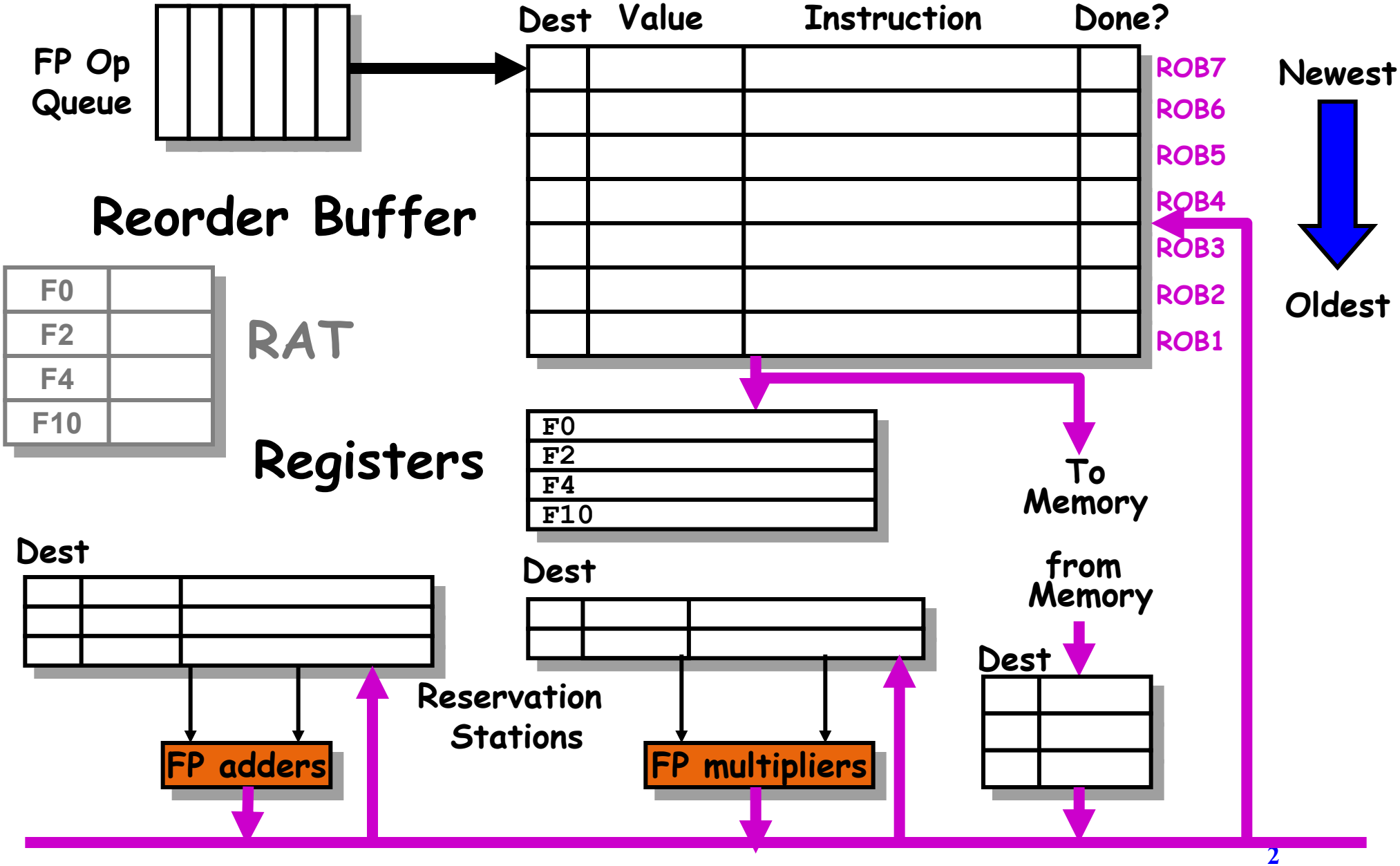
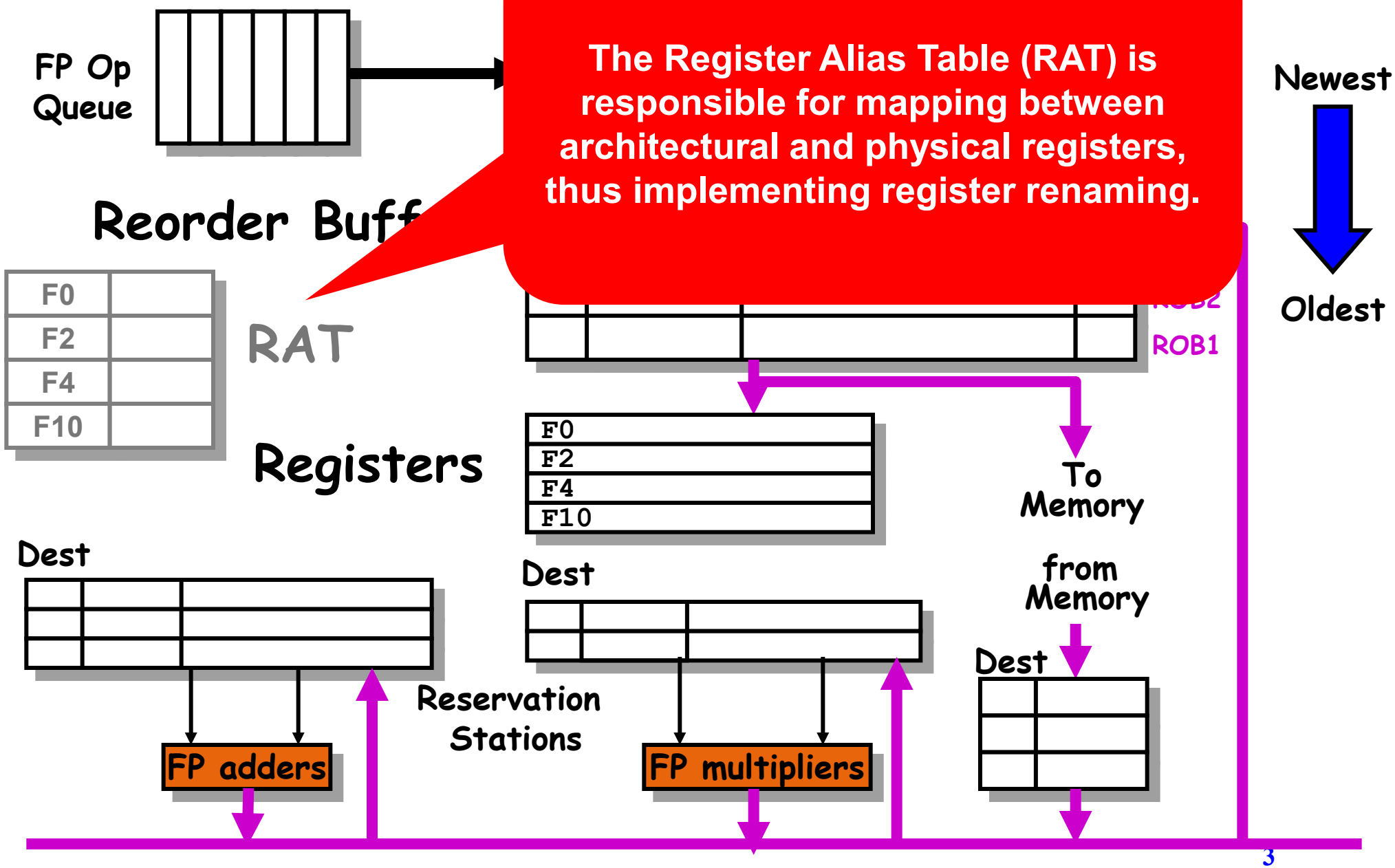
Example of code execution on a processor based on the Tomasulo architecture

Slides modified from Prof. Dave Patterson, Prof. John Kubiatowicz, Prof. Nancy Warter-Perez (Berkeley Un.), and Zvika Guz (Technion)

Tomasulo With Reorder buffer: architecture



Tomasulo With

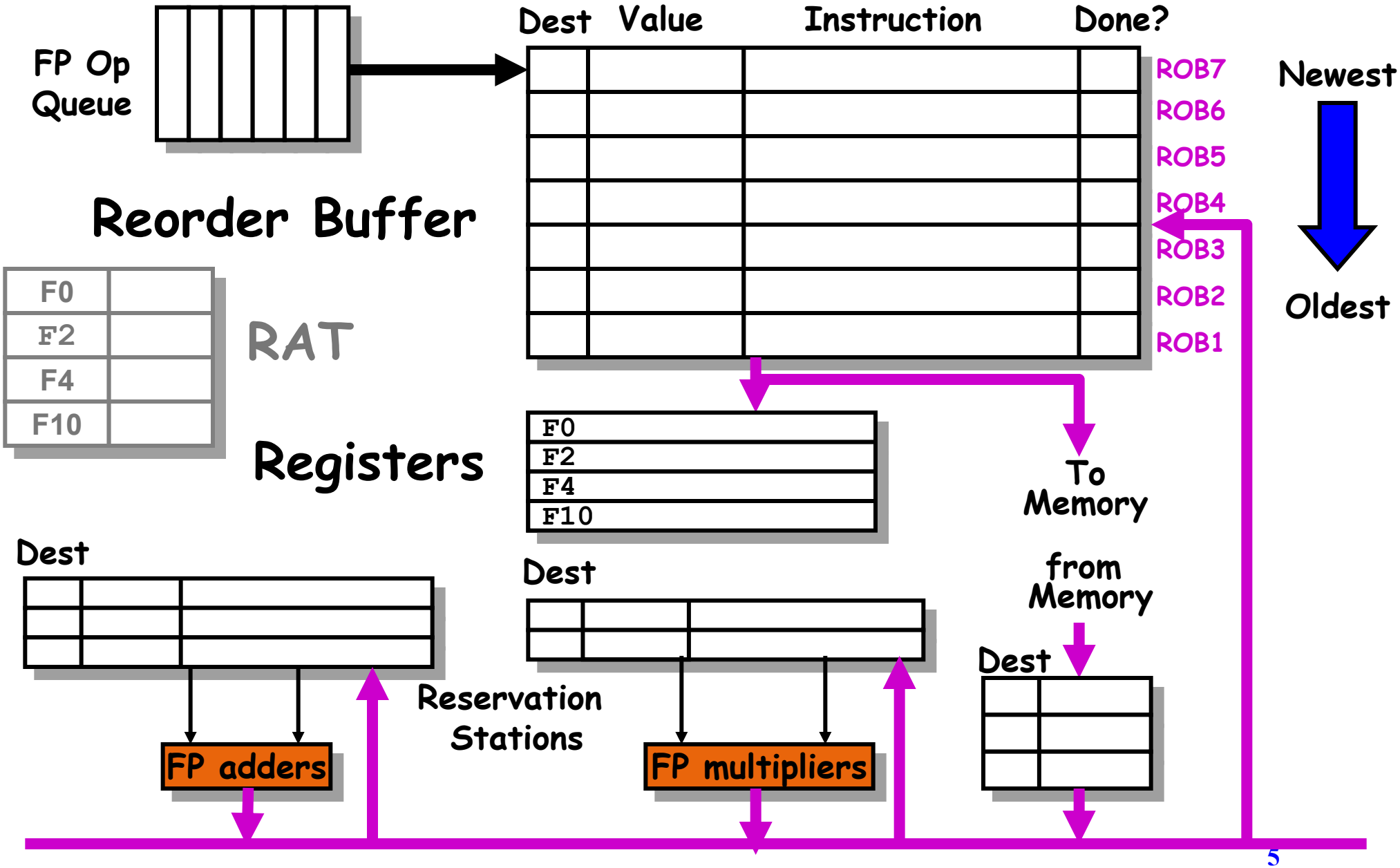


Code example

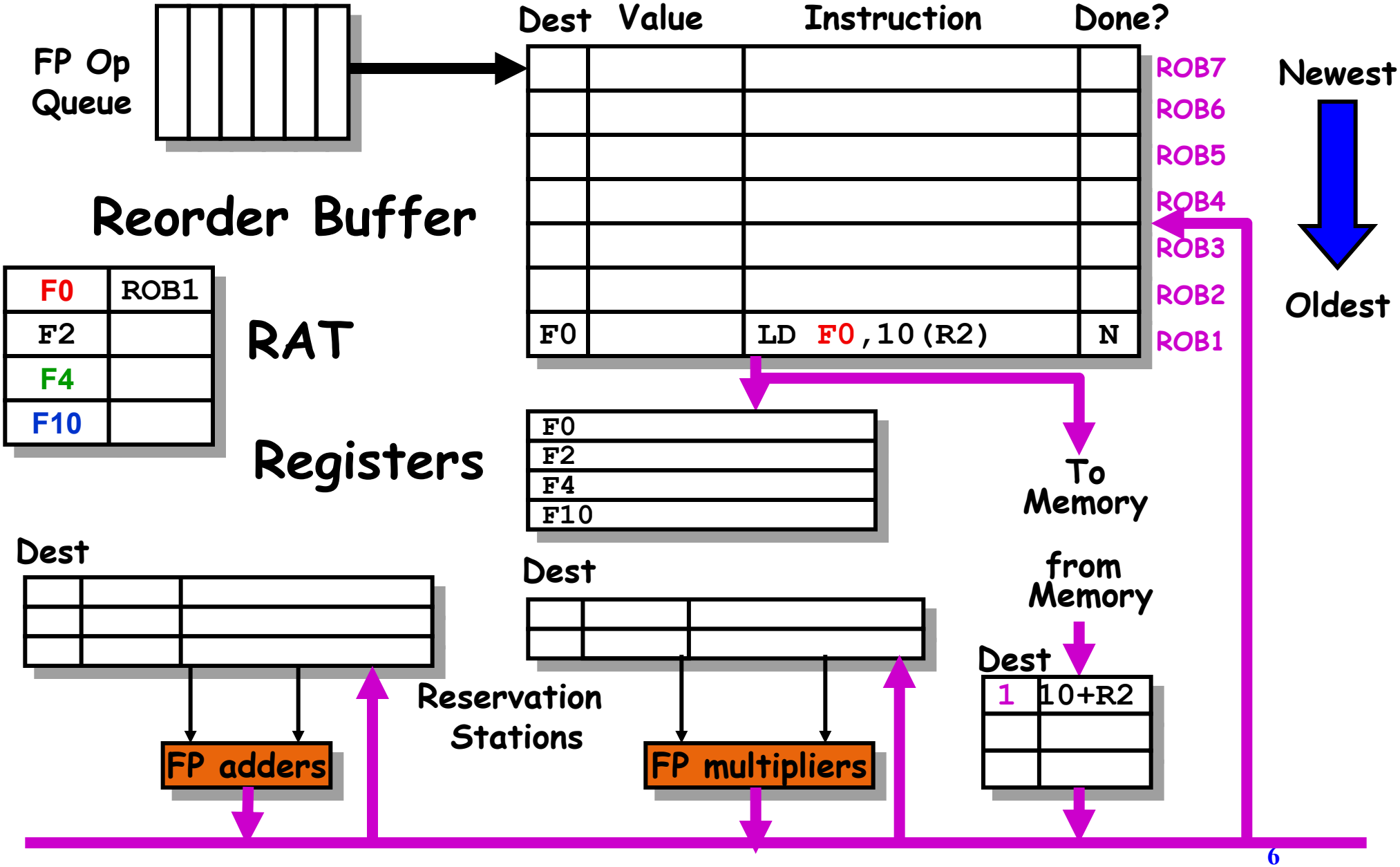
```
1. LD F0, 10(R2)
2. ADDD F10, F4, F0
3. DIVD F2, F10, F6
4. BNE F2, <LAB01>
5. LD F4, 0(R3)
6. ADDD F0, F4, F6
7. ADDD F0, F4, F6


<LAB01>
```

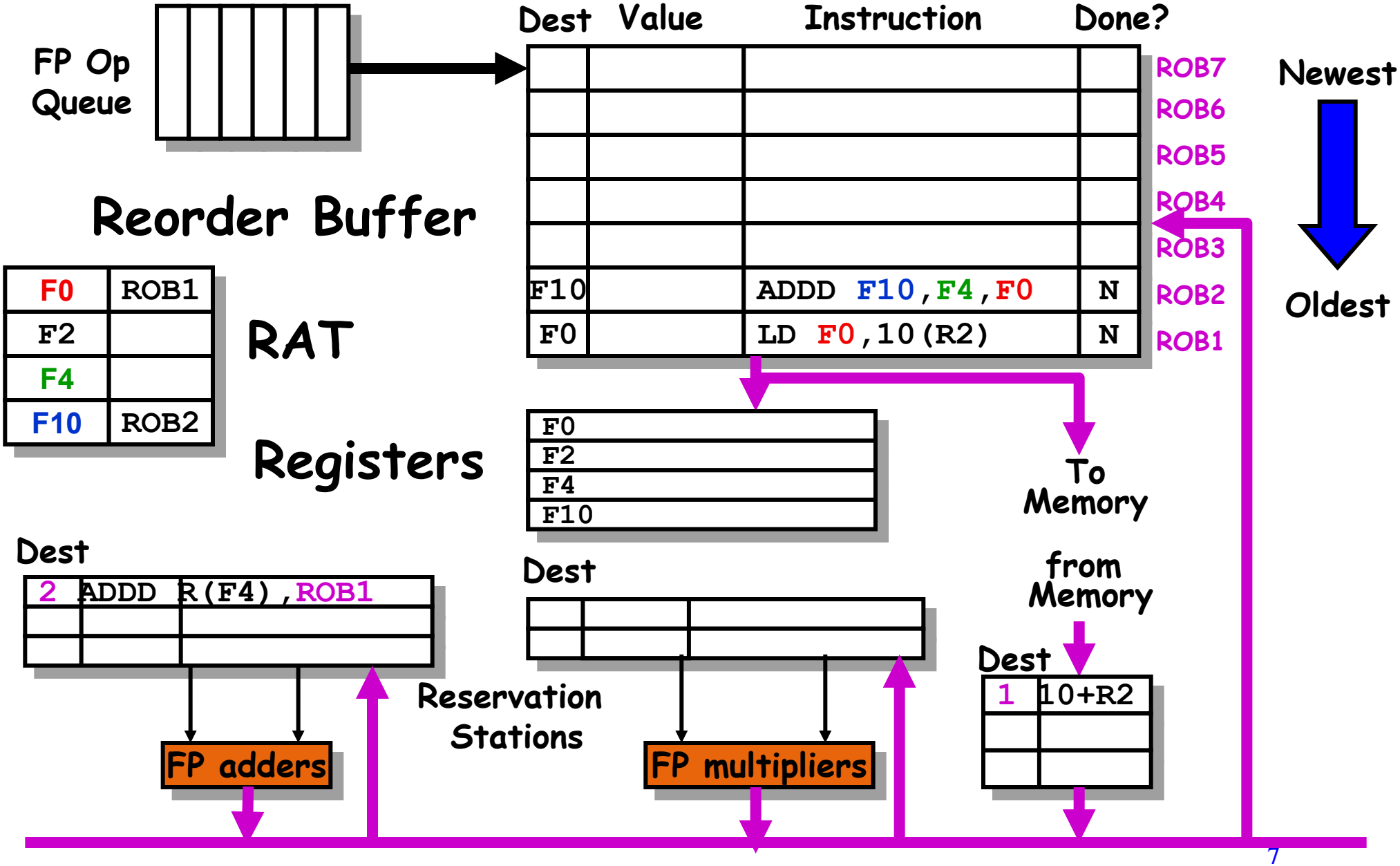
Tomasulo With Reorder buffer



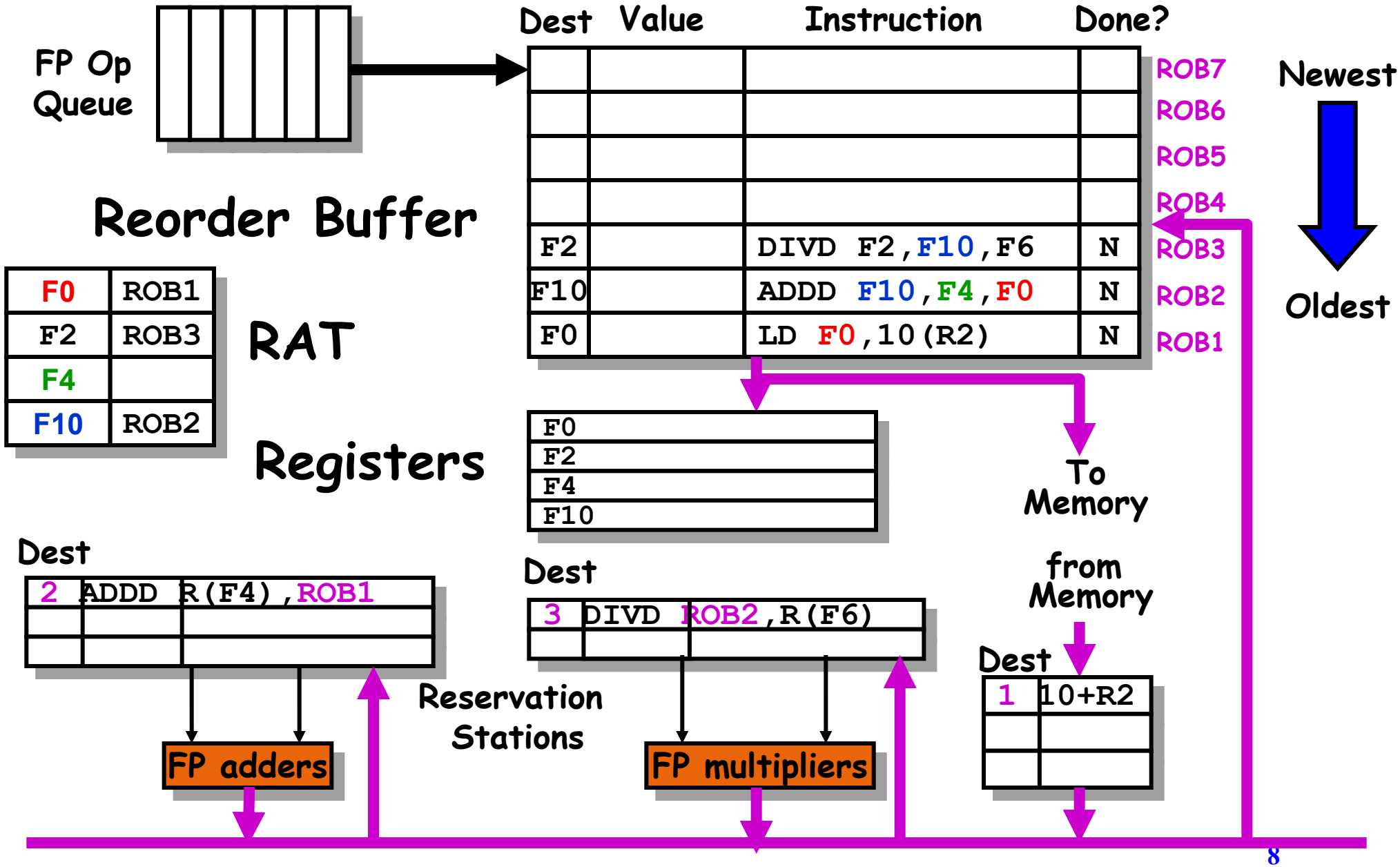
Tomasulo With Reorder buffer: 1



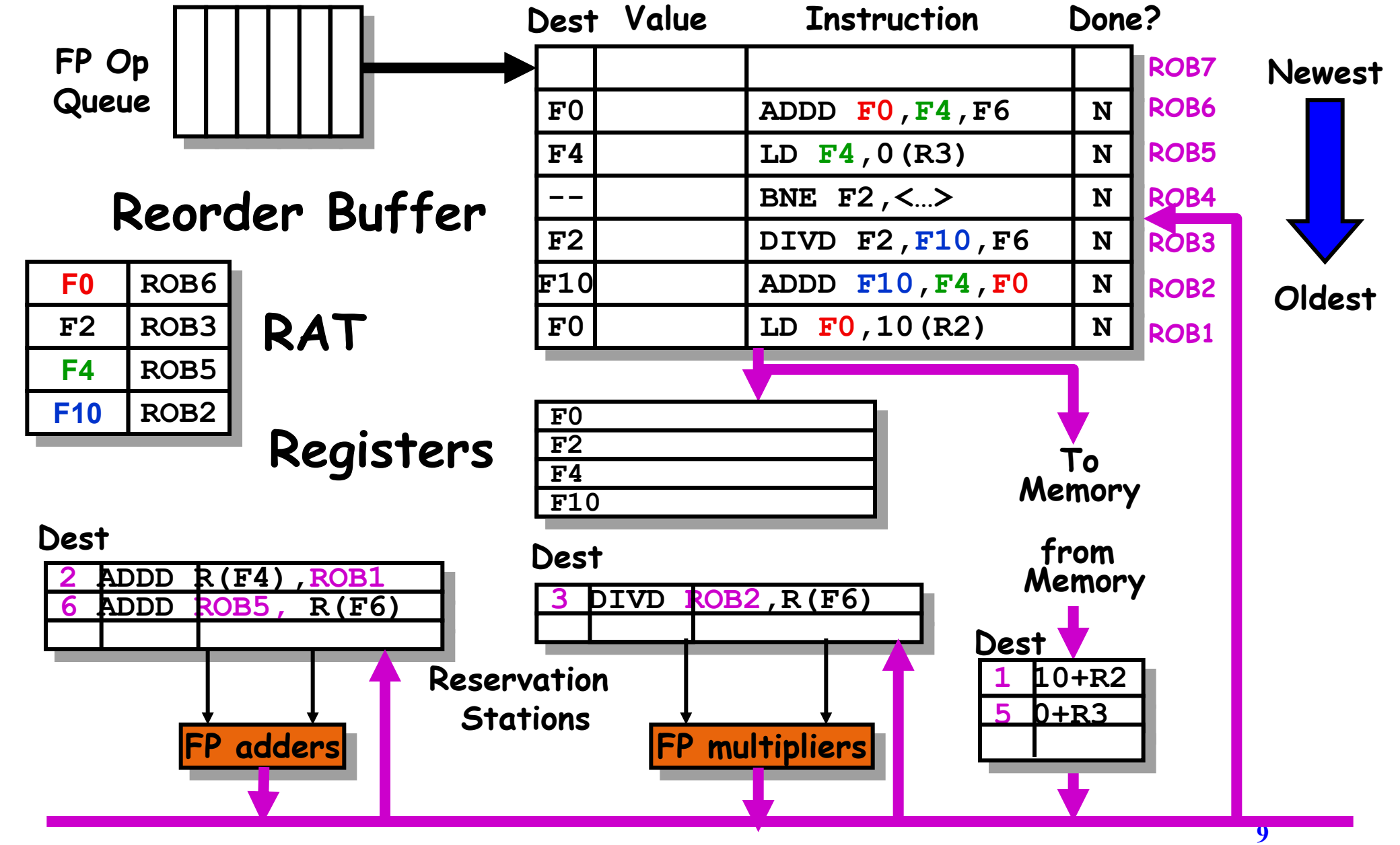
Tomasulo With Reorder buffer: 2



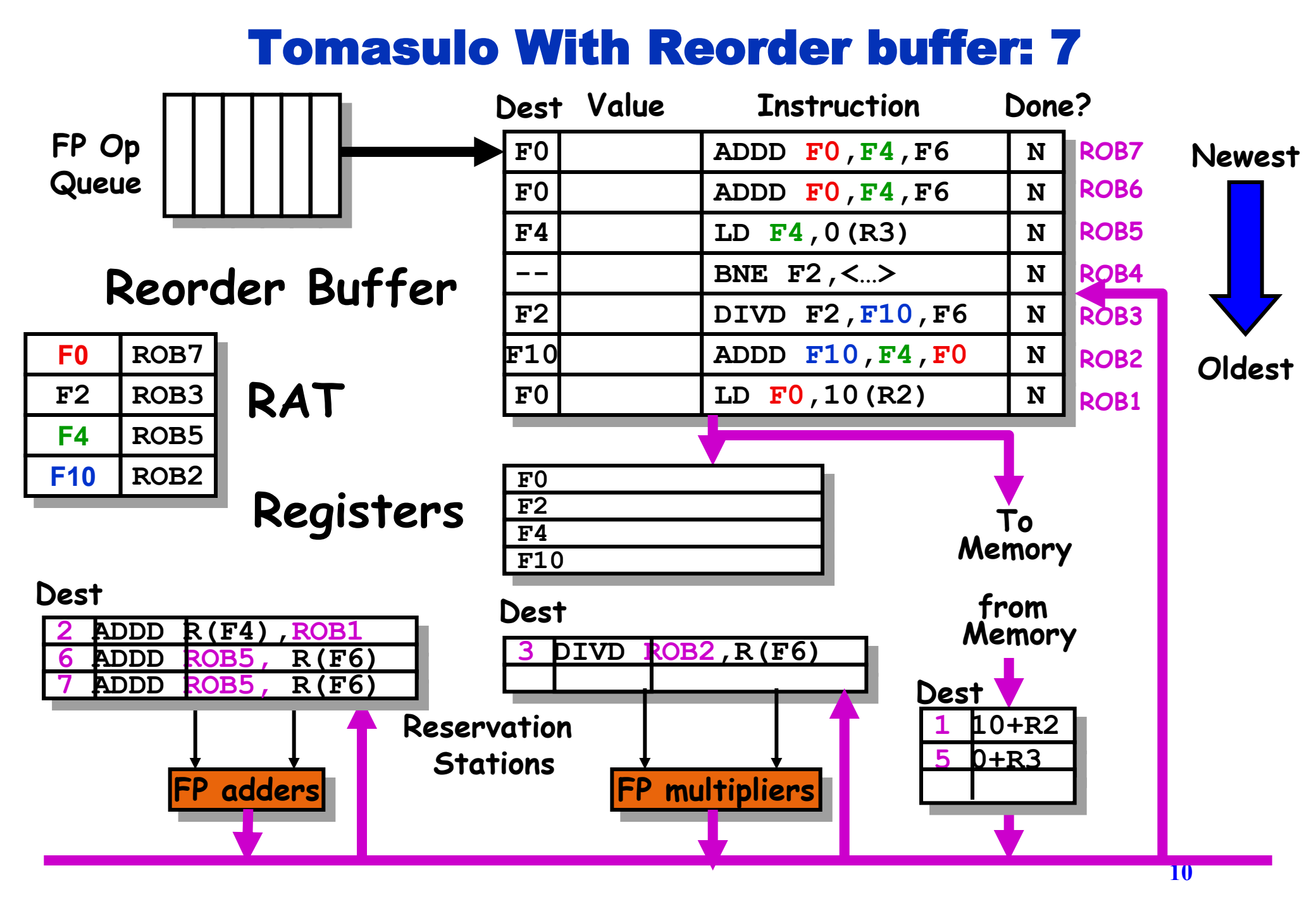
Tomasulo With Reorder buffer: 3



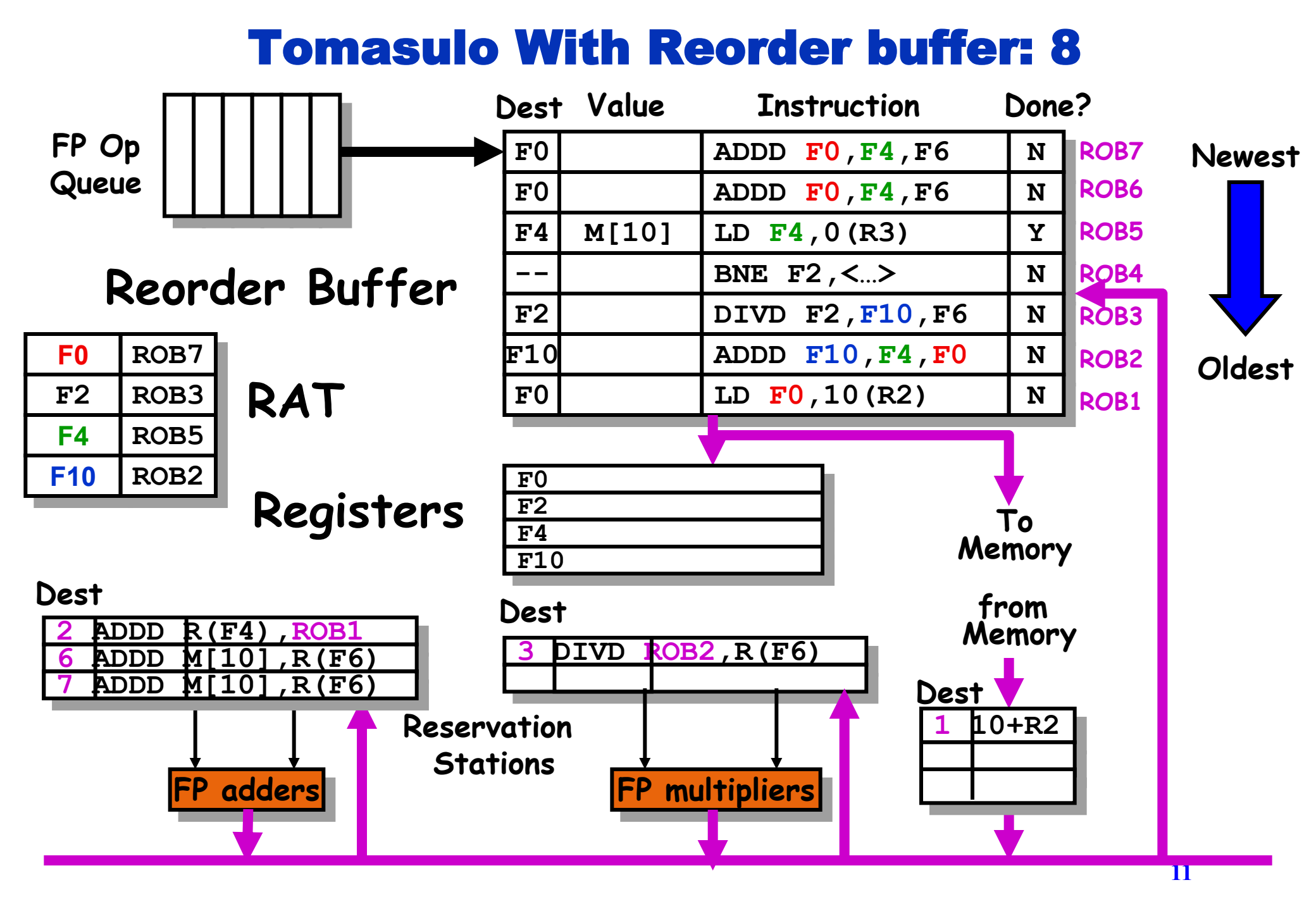
Tomasulo With Reorder buffer: 4, 5, 6



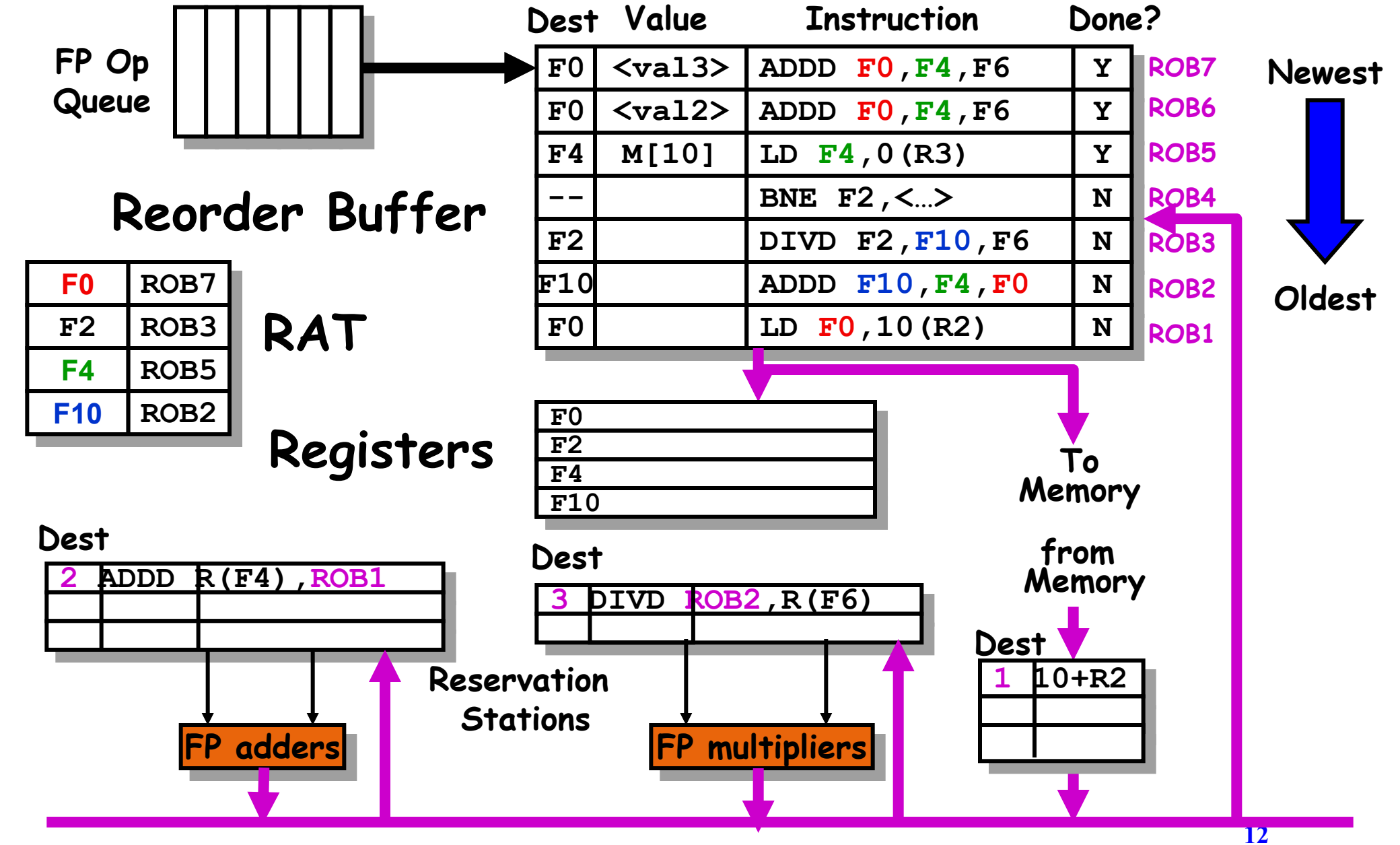
Tomasulo With Reorder buffer: 7



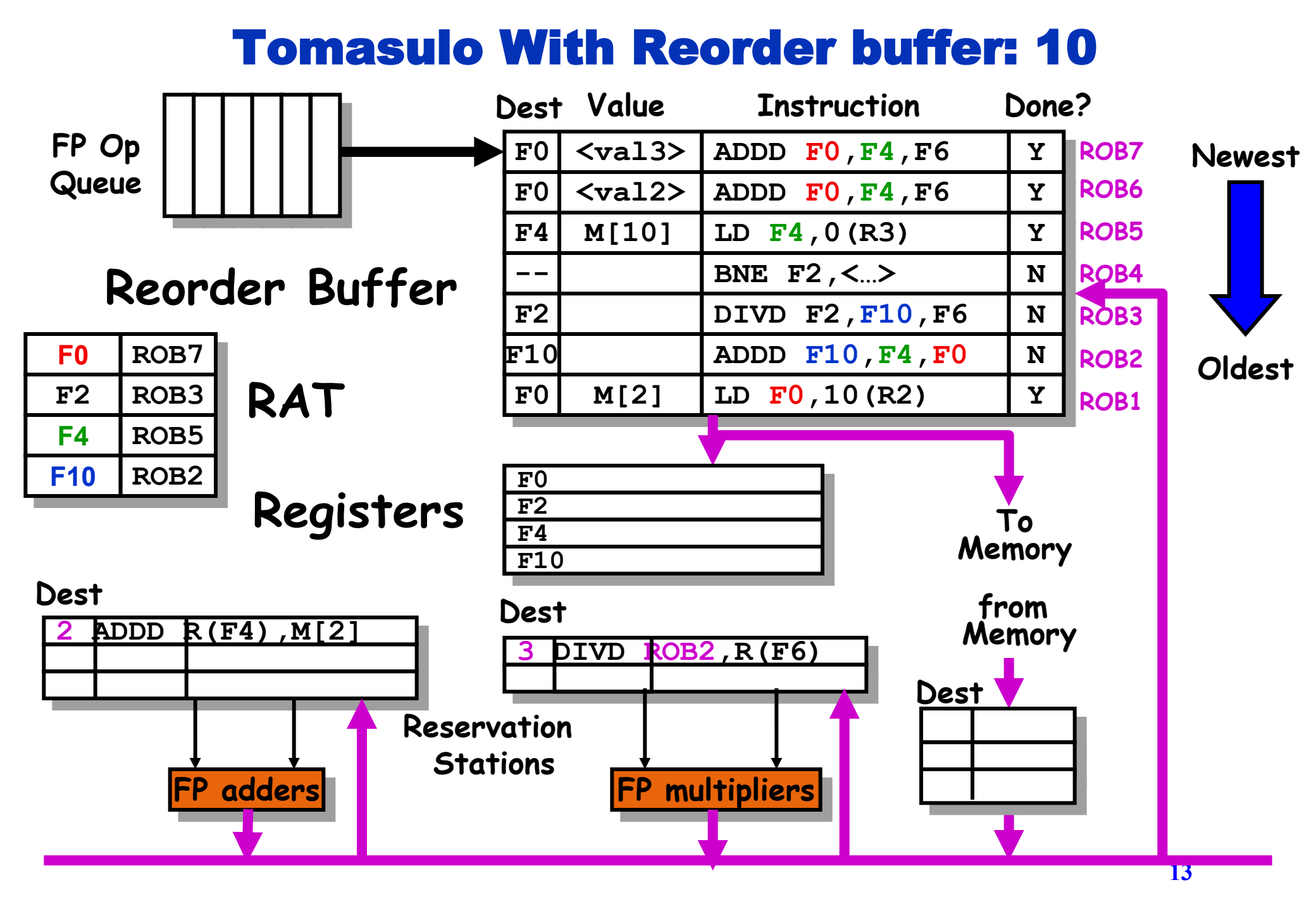
Tomasulo With Reorder buffer: 8



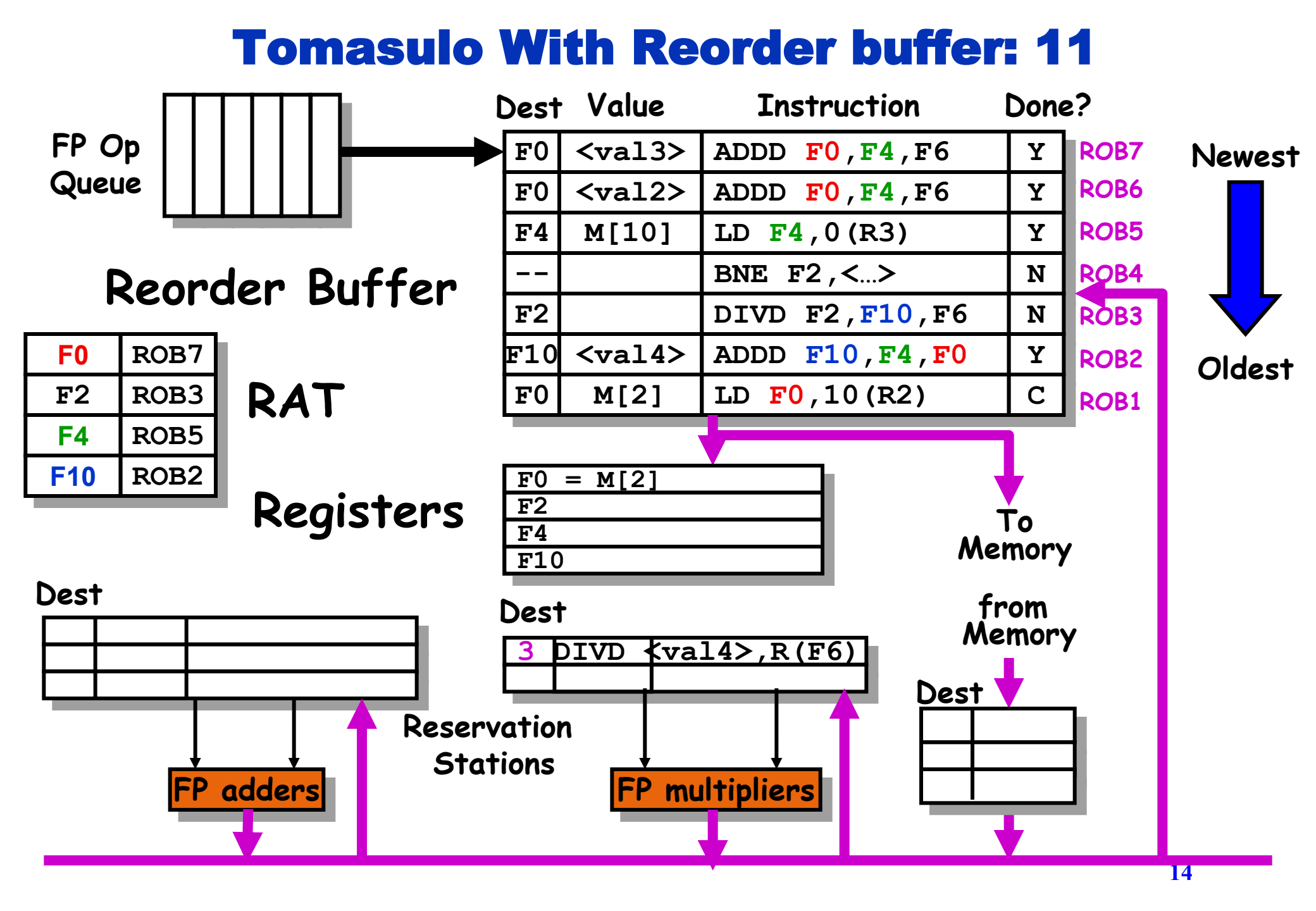
Tomasulo With Reorder buffer: 9



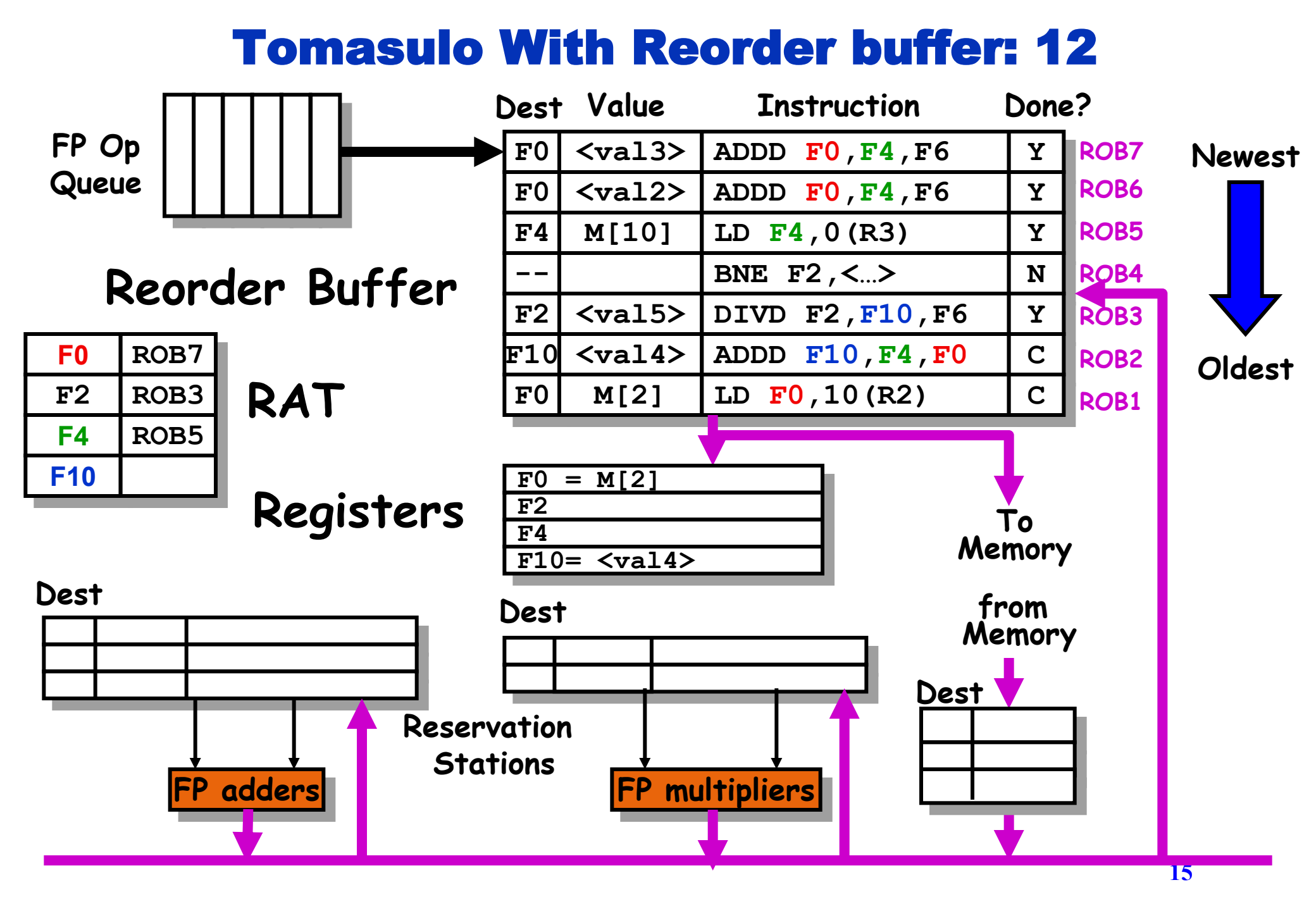
Tomasulo With Reorder buffer: 10



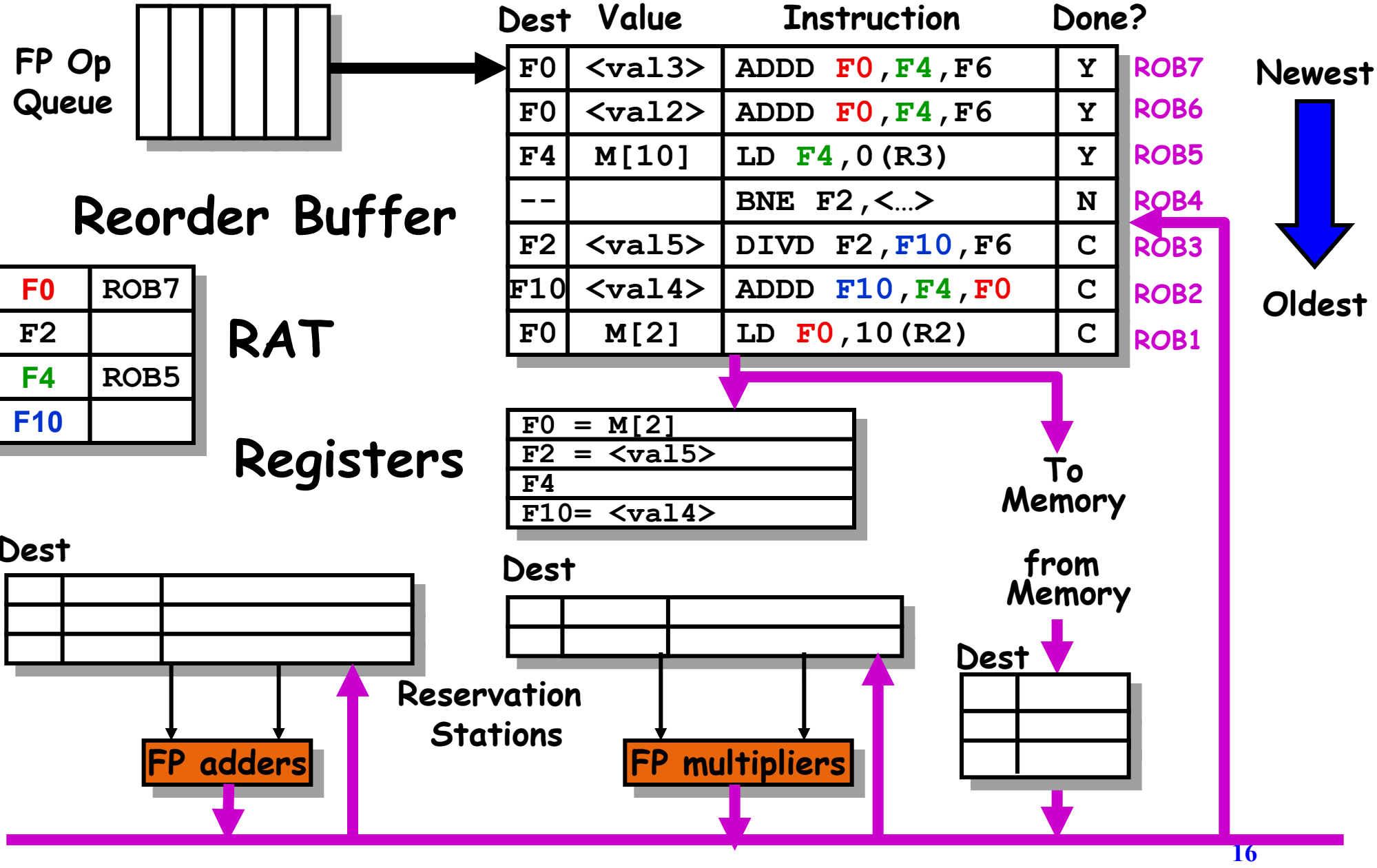
Tomasulo With Reorder buffer: 11



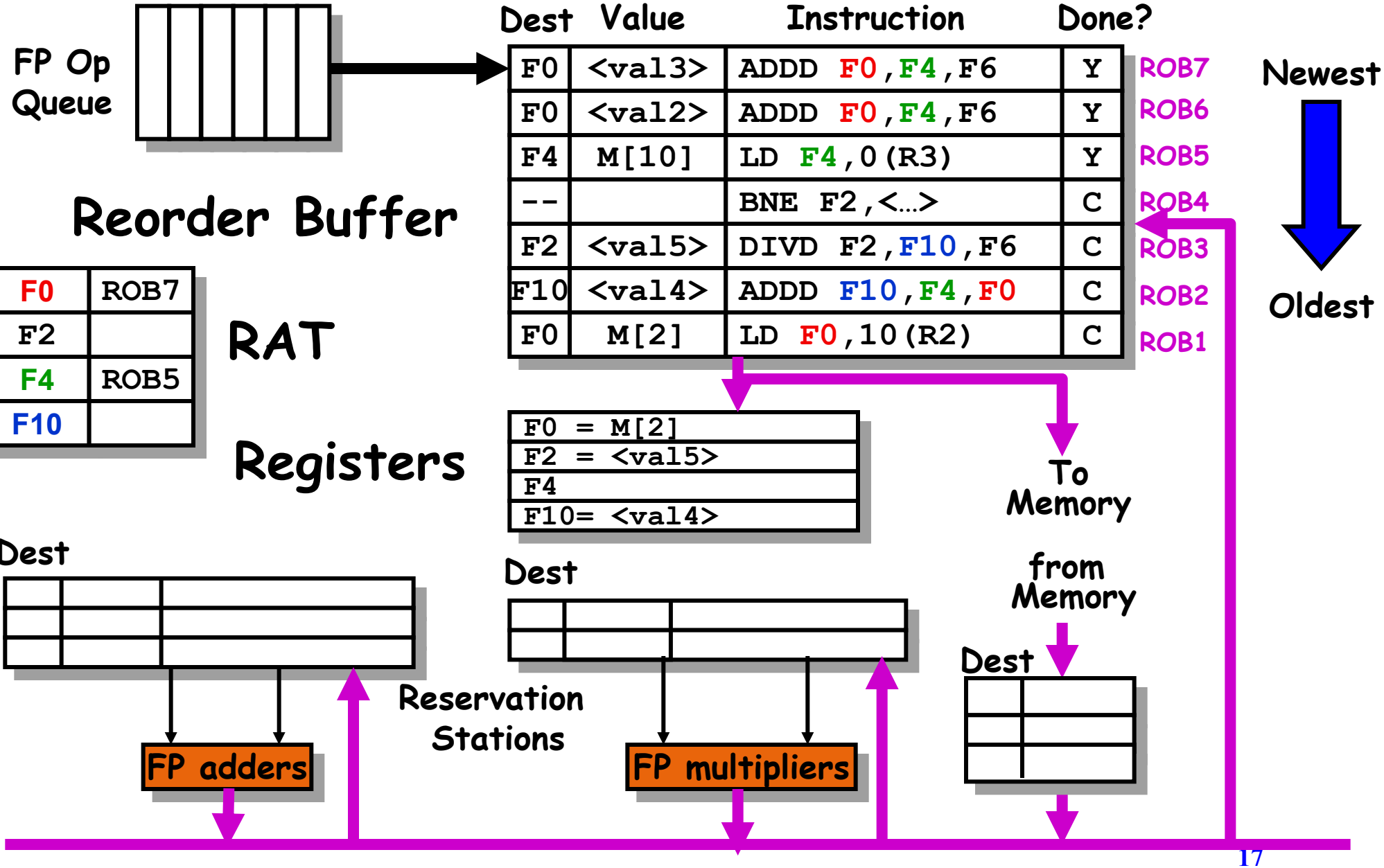
Tomasulo With Reorder buffer: 12



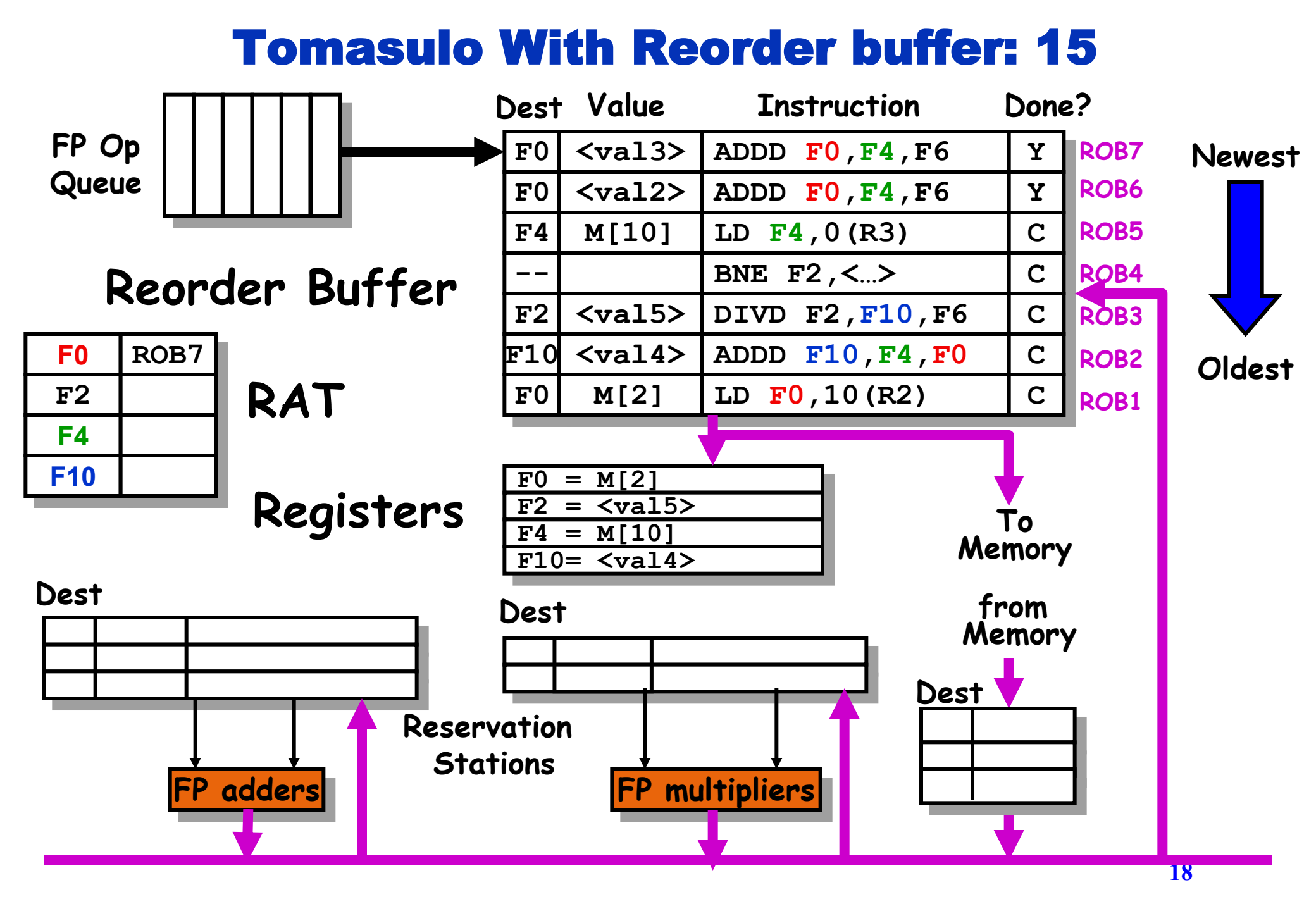
Tomasulo With Reorder buffer: 13



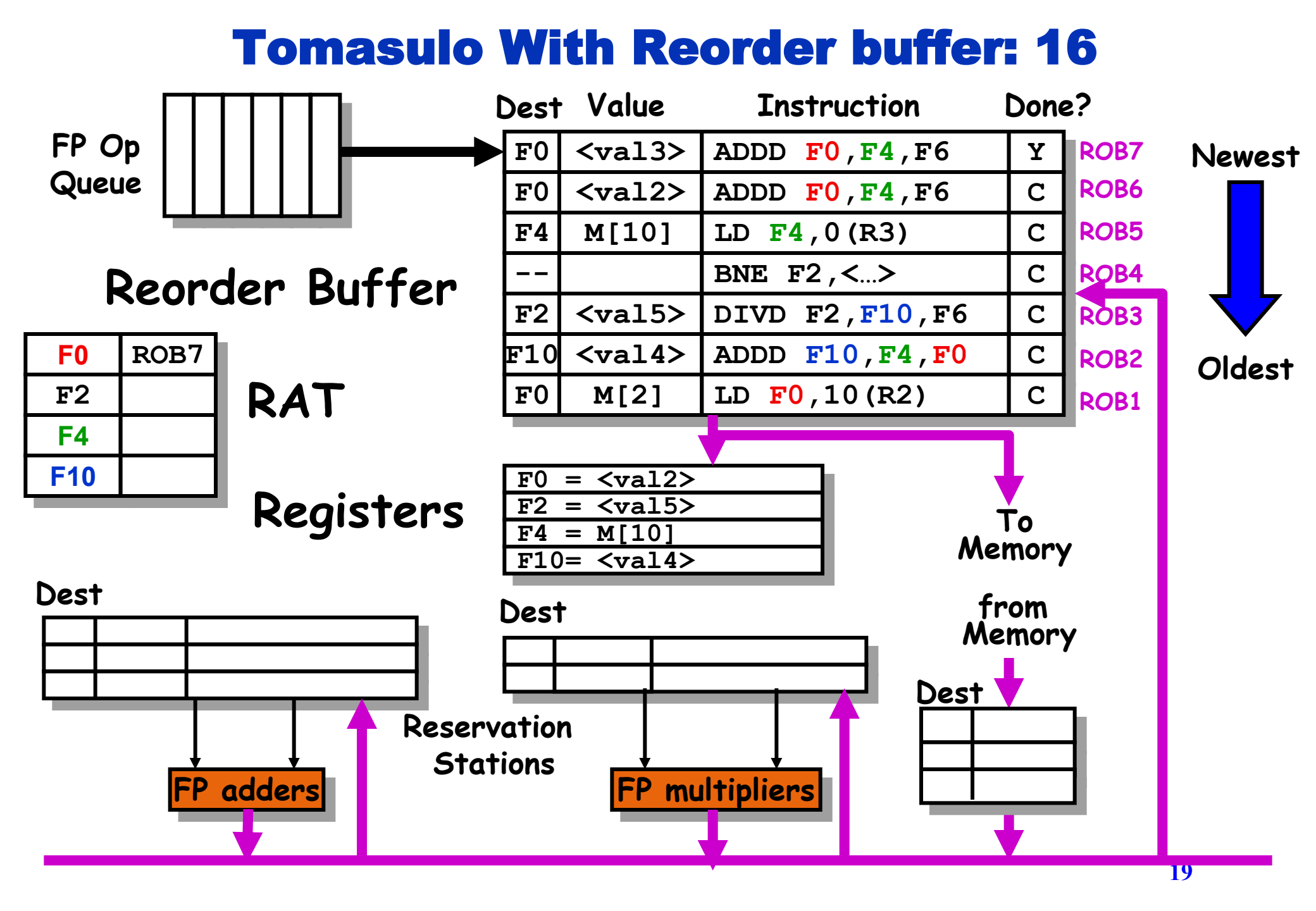
Tomasulo With Reorder buffer: 14



Tomasulo With Reorder buffer: 15



Tomasulo With Reorder buffer: 16



Tomasulo With Reorder buffer: 17