

**Laboratory  
0x04**

Expected delivery of lab\_04.zip must include:

- **program\_1.s**, **program\_1\_a.s**, and **program\_1\_b.s**
- This file, filled with information and possibly compiled in a **PDF** format.

Delivery date:

November 7<sup>th</sup> 2025

This lab will explore some of the concepts seen during the lessons, such as hazards, rescheduling, and loop unrolling. The first thing to do is to configure the GEM5 simulator with the **Initial Configuration** provided below:

```
INTEGER_ALU_LATENCY = 1
INTEGER_MUL_LATENCY = 1
INTEGER_DIV_LATENCY = 1
FLOAT_ALU_LATENCY = 4
FLOAT_MUL_LATENCY = 8
FLOAT_DIV_LATENCY = 20
```

- 1) Write an assembly program (**program\_1.s**) for the RISCV architecture able to compute the output ( $y$ ) of a **neural computation** (see the Fig. below):

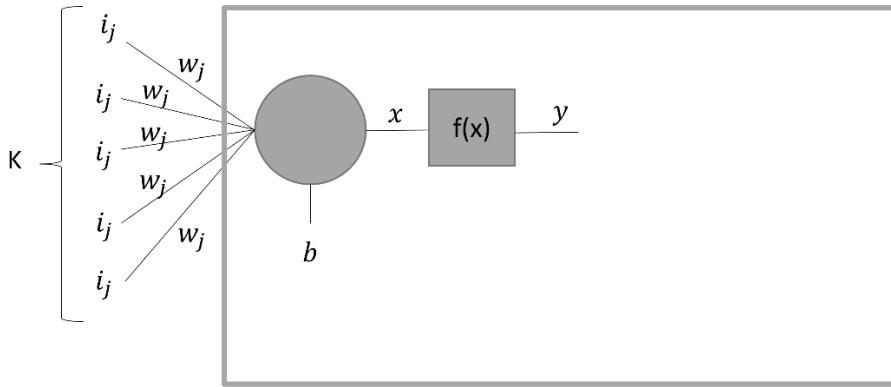
$$x = \sum_{j=0}^{K-1} i_j * w_j + b$$

$$y = f(x)$$

where, to prevent the propagation of NaN (Not a Number), the activation function  $f$  is defined as:

$$f(x) = \begin{cases} 0, & \text{if the exponent part of } x \text{ is equal to } 0x7FF} \\ x, & \text{otherwise} \end{cases}$$

Assume the vectors  $i$  and  $w$  respectively store the inputs entering the neuron and the weights of the connections. They contain  $K=16$  single precision **floating point** elements. Assume that  $b$  is a single precision **floating point** constant and is equal to  $0xab$ , and  $y$  is a single precision **floating point** value stored in memory.  
Compute  $y$ .



Given the *Base Configuration*, run your program and extract the following information.

	Number of clock cycles	Total Instructions	CPI (Clock per Instructions)
program_1.s	342	163	2.098

- a. Optimize the program by re-scheduling instructions to eliminate as many hazards as possible. Manually calculate the number of clock cycles for the new program (**program\_1\_a.s**) to execute and compare the results with those obtained by the simulator.
- b. Unroll the program (**program\_1\_a.s**) two times; If necessary, re-schedule instructions and increase the number of registers used. Manually calculate the number of clock cycles to execute the new program (**program\_1\_b.s**) and compare the results obtained with those obtained by the simulator.

Complete the following table with the obtained results:

Program	program_1.s	program_1_a.s	program_1_b.s
Clock cycles by hand	261	224	166
Clock cycles by simulation	342	237	201

Collect the Cycles Per Instruction (CPI) from the simulator for different programs

	program_1.s	program_1_a.s	program_1_b.s
CPI	2.098	1.419	1.467

Compare the results obtained in 1) and provide some explanation if the results are different.

Eventual explanation: Le discrepanze tra stima a mano e con l'uso del simulatore derivano da hazard strutturali (contenzione in write-back), dipendenze RAW/WAW amplificate da latenze FP, penalità di branch del datapath base e dall'espansione di pseudoistruzioni; nel codice iniziale questi effetti sono marcati, la rischedulazione li attenua, mentre l'unrolling riduce l'overhead di controllo ma intensifica le collisioni su WB e memoria, che il simulatore modella con stall aggiuntivi.

- c. Try different unrolls for the program (**program\_1\_a.s**); If necessary, reschedule instructions and increase the number of registers used. Manually calculate the number of clock cycles to execute the new program (**program\_1\_b.s**) and compare the results obtained with those obtained by the simulator.

Complete the following table with the obtained results:

Program	Number of Loop Unrolling	Code size [bytes]	Clock Cycles [CC]
<b>program_1_a.s</b>	-	188	342
	2	228	201
	4	276	201
	8	372	175
	16	412	149

In order to calculate the code size of your program you can open in `./programs/you_program/your_program.dump` file to retrieve the compiled disassembled code of your executable in which you have the effective addresses from which the code will be executed.

For example (on the right), for *your\_program* you have your disassembled file on 32 bit addresses.

```

1 program1.elf:      file format elf32-littleriscv
2
3
4 Disassembly of section .text:
5
6 00010094 <_start>:
7 10094: 00001097          auipc ra,0x1
8 10098: 06408893          addi  ra,ra,100 # 110f8 <__DATA_BEGIN__>
9 1009c: 0000a487          flw   fs1,0(ra)
10 100a0: 00001097          auipc ra,0x1
11 100a4: 06808893          addi  ra,ra,104 # 11108 <V2>
12 100a8: 0000a487          flw   fs1,0(ra)
13 100ac: 00001097          auipc ra,0x1
14 100b0: 06c08893          addi  ra,ra,108 # 11118 <V3>
15 100b4: 0000a103          lw    sp,0(r)
16 100b8: 00001097          auipc ra,0x1
17 100bc: 07008893          addi  ra,ra,112 # 11128 <T>
18 100c0: 0000a103          lw    sp,0(r)
19 100c4: 00001097          auipc ra,0x1
20 100c8: 03408893          addi  ra,ra,52 # 110f8 <__DATA_BEGIN__>
21 100cc: 00001117          auipc sp,0x1
22 100d0: 03c10113          addi  sp,sp,60 # 11108 <V2>
23 100d4: 0000a087          flw   ft1,0(sp)
24 100d8: 00012107          flw   ft2,0(sp)
25 100dc: 0000a187          flw   ft3,0(ra)
26 100e0: 00012207          flw   ft4,0(sp)
27
28
29 000100e4 <Main>:
30 100e4: 1020f2d3          fmul.s  ft5,ft1,ft2
31 100e8: 1020f2d3          fmul.s  ft5,ft1,ft2
32
33 000100ec <End>:
34 100ec: 00000513          li    a7,93
35 100f0: 05d08893          li    a7,93
36 100f4: 00000073          ecall
37

```