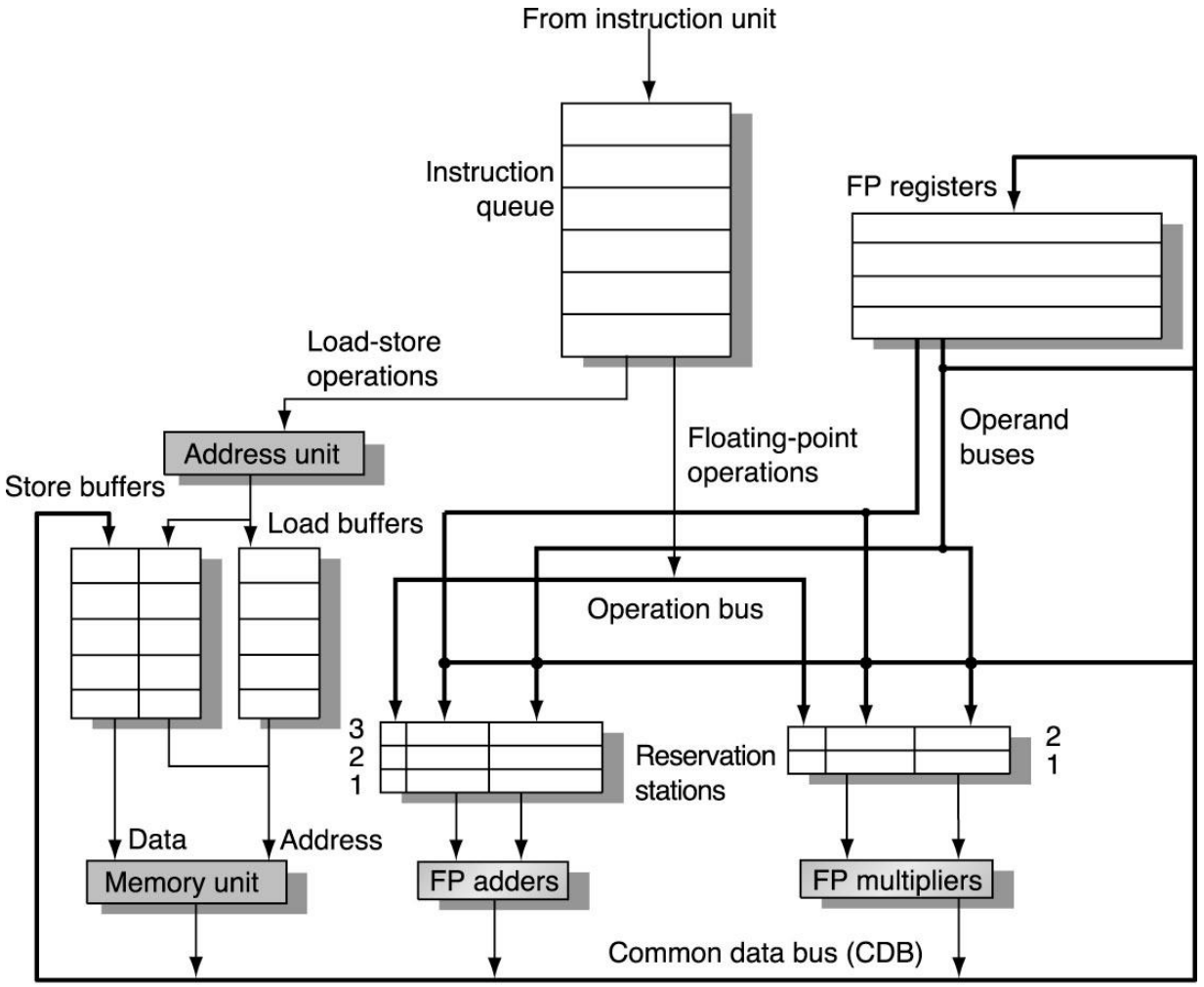
Examples of behavior of the Tomasulo's architecture

Tomasulo Organization



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Reservation Station Components

Op—Operation to perform in the unit (e.g., + or –)

Qj, Qk—Reservation stations producing source registers

Vj, Vk—Value of Source operands

Rj, Rk—Flags indicating when Vj, Vk are ready

Busy—Indicates reservation station and FU is busy

Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

Three Stages of Tomasulo Algorithm

1. **Issue—get instruction from FP Op Queue**

   If reservation station free, the scoreboard issues instr & sends operands (renames registers).

2. **Execution—operate on operands (EX)**

   When both operands ready then execute; if not ready, watch CDB for result

3. **Write result—finish execution (WB)**

   Write on Common Data Bus to all awaiting units; mark reservation station available.

Tomasulo Example Cycle 0

Instruction Status				Issue	Execution Complete	Write Result			Busy	Address		
Instruction		j	k									
LD	**F6**	**34+**	**R2**					Load1	No			
LD	**F2**	**45+**	**R3**					Load2	No			
MULTD	**F0**	**F2**	**F4**					Load3	No			
SUBD	**F8**	**F6**	**F2**									
DIVD	**F10**	**F0**	**F6**									
ADDD	**F6**	**F8**	**F2**									

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	0	Mult1	No									
	0	Mult2	No									

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
0			FU									

Tomasulo Example Cycle 1

Instruction Status					Execution	Write						
Instruction		j	k	Issue	Complete	Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1				Load1	Yes	34+R2		
LD	**F2**	**45+**	**R3**					Load2	No			
MULTD	**F0**	**F2**	**F4**					Load3	No			
SUBD	**F8**	**F6**	**F2**									
DIVD	**F10**	**F0**	**F6**									
ADDD	**F6**	**F8**	**F2**									

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	**No**									
	0	Add2	**No**									
	0	Add3	**No**									
	0	Mult1	**No**									
	0	Mult2	**No**									

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
1			FU				Load1					

Tomasulo Example Cycle 2

Instruction Status					Execution	Write						
Instruction		j	k	Issue	Complete	Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1				Load1	Yes	34+R2		
LD	**F2**	**45+**	**R3**	2				Load2	Yes	45+R3		
MULTD	**F0**	**F2**	**F4**					Load3	No			
SUBD	**F8**	**F6**	**F2**									
DIVD	**F10**	**F0**	**F6**									
ADDD	**F6**	**F8**	**F2**									

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	**No**									
	0	Add2	**No**									
	0	Add3	**No**									
	0	Mult1	**No**									
	0	Mult2	**No**									

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
2			FU		Load2		Load1					

Tomasulo Example Cycle 3

Instruction Status					Execution	Write						
Instruction		j	k	Issue	Complete	Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1	3			Load1	Yes	34+R2		
LD	**F2**	**45+**	**R3**	2				Load2	Yes	45+R3		
MULTD	**F0**	**F2**	**F4**	3				Load3	No			
SUBD	**F8**	**F6**	**F2**									
DIVD	**F10**	**F0**	**F6**									
ADDD	**F6**	**F8**	**F2**									

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	**No**									
	0	Add2	**No**									
	0	Add3	**No**									
	0	Mult1	**Yes**	MULTD		R[F4]	Load2					
	0	Mult2	**No**									

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
3			FU	Mult1	Load2		Load1					

Tomasulo Example Cycle 4

Instruction Status

Instruction		j	k	Issue	Execution Complete	Write Result
LD	**F6**	**34+**	**R2**	1	3	4
LD	**F2**	**45+**	**R3**	2	4	
MULTD	**F0**	**F2**	**F4**	3		
SUBD	**F8**	**F6**	**F2**	4		
DIVD	**F10**	**F0**	**F6**			
ADDD	**F6**	**F8**	**F2**			

	Busy	Address
Load1	No	
Load2	Yes	45+R3
Load3	No	

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
	0	Add1	**Yes**	SUBD	M[34+R2]			Load2
	0	Add2	**No**					
	0	Add3	**No**					
	0	Mult1	**Yes**	MULTD		R[F4]	Load2	
	0	Mult2	**No**					

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12	…	F30
4	FU	Mult1	Load2		M[34+R2]	Add1				

Tomasulo Example Cycle 5

Instruction Status

Instruction		j	k	Issue	Execution Complete	Write Result
LD	**F6**	**34+**	**R2**	1	3	4
LD	**F2**	**45+**	**R3**	2	4	5
MULTD	**F0**	**F2**	**F4**	3		
SUBD	**F8**	**F6**	**F2**	4		
DIVD	**F10**	**F0**	**F6**	5		
ADDD	**F6**	**F8**	**F2**			

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
	0	Add1	**Yes**	SUBD	M[34+R2]	M[45+R3]		
	0	Add2	**No**					
	0	Add3	**No**					
	0	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]		
	0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1	

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
5			FU	Mult1	M[45+R3]		M[34+R2]	Add1	Mult2			

Tomasulo Example Cycle 6

Instruction Status

Instruction		j	k	Issue	Execution Complete	Write Result
LD	**F6**	**34+**	**R2**	1	3	4
LD	**F2**	**45+**	**R3**	2	4	5
MULTD	**F0**	**F2**	**F4**	3		
SUBD	**F8**	**F6**	**F2**	4		
DIVD	**F10**	**F0**	**F6**	5		
ADDD	**F6**	**F8**	**F2**	6		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Resevation Stations

Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
2	Add1	**Yes**	SUBD	M[34+R2]	M[45+R3]		
0	Add2	**Yes**	ADDD		M[45+R3]	Add1	
0	Add3	**No**					
10	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]		
0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1	

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
6			FU	Mult1	M[45+R3]		Add2	Add1	Mult2			

Tomasulo Example Cycle 7

Instruction Status

Instruction		j	k	Issue	Execution Complete	Write Result			Busy	Address
LD	**F6**	**34+**	**R2**	1	3	4		Load1	No	
LD	**F2**	**45+**	**R3**	2	4	5		Load2	No	
MULTD	**F0**	**F2**	**F4**	3				Load3	No	
SUBD	**F8**	**F6**	**F2**	4	7					
DIVD	**F10**	**F0**	**F6**	5						
ADDD	**F6**	**F8**	**F2**	6						

Resevation Stations

Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
1	Add1	**Yes**	SUBD	M[34+R2]	M[45+R3]		
0	Add2	**Yes**	ADDD		M[45+R3]	Add1	
0	Add3	**No**					
9	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]		
0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1	

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12	…	F30
7	FU	Mult1	M[45+R3]		Add2	Add1	Mult2			

Tomasulo Example Cycle 8

Instruction Status												
		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6								

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	Yes	ADDD	M[]-M[]	M[45+R3]						
	0	Add3	No									
	8	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
8			FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2			

Tomasulo Example Cycle 9

Instruction Status												
		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6								

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	2	Add2	Yes	ADDD	M[]-M[]	M[45+R3]						
	0	Add3	No									
	7	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
9			FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2			

Tomasulo Example Cycle 10

Instruction Status

		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1	3	4		Load1	No			
LD	**F2**	**45+**	**R3**	2	4	5		Load2	No			
MULTD	**F0**	**F2**	**F4**	3				Load3	No			
SUBD	**F8**	**F6**	**F2**	4	7	8						
DIVD	**F10**	**F0**	**F6**	5								
ADDD	**F6**	**F8**	**F2**	6	10							

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
	0	Add1	**No**					
	1	Add2	**Yes**	ADDD	M[]-M[]	M[45+R3]		
	0	Add3	**No**					
	6	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]		
	0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1	

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
10			FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2			

Tomasulo Example Cycle 11

Instruction Status												
		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	5	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
11			FU	Mult1	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 12

Instruction Status

		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1	3	4		Load1	No			
LD	**F2**	**45+**	**R3**	2	4	5		Load2	No			
MULTD	**F0**	**F2**	**F4**	3				Load3	No			
SUBD	**F8**	**F6**	**F2**	4	7	8						
DIVD	**F10**	**F0**	**F6**	5								
ADDD	**F6**	**F8**	**F2**	6	10	11						

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk				
	0	Add1	**No**									
	0	Add2	**No**									
	0	Add3	**No**									
	4	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]						
	0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1					

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
12			FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2			

Tomasulo Example Cycle 13

Instruction Status

		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1	3	4		Load1	No			
LD	**F2**	**45+**	**R3**	2	4	5		Load2	No			
MULTD	**F0**	**F2**	**F4**	3				Load3	No			
SUBD	**F8**	**F6**	**F2**	4	7	8						
DIVD	**F10**	**F0**	**F6**	5								
ADDD	**F6**	**F8**	**F2**	6	10	11						

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk				
	0	Add1	**No**									
	0	Add2	**No**									
	0	Add3	**No**									
	3	Mult1	**Yes**	MULTD	M[45+R3]	R[F4]						
	0	Mult2	**Yes**	DIVD		M[34+R2]	Mult1					

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
13			FU	Mult1	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 14

Instruction Status												
		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	2	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
14			FU	Mult1	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 15

Instruction Status												
		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3	15			Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	1	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
15			FU	Mult1	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 16

Instruction Status					Execution	Write						
		j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	0	Mult1	No									
	0	Mult2	Yes	DIVD	M*F4	M[34+R2]						

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
16			FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 17

Instruction Status					Execution	Write						
		j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Resevation Stations					S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	0	Mult1	No									
	40	Mult2	Yes	DIVD	M*F4	M[34+R2]						

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
17			FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 18

Instruction Status					Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3	15	16		Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					

Resevation Stations					S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No								
	0	Add2	No								
	0	Add3	No								
	0	Mult1	No								
	39	Mult2	Yes	DIVD	M*F4	M[34+R2]					

Register result status												
Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
18			FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 56

Instruction Status

		j	k	Issue	Execution Complete	Write Result
LD	**F6**	**34+**	**R2**	1	3	4
LD	**F2**	**45+**	**R3**	2	4	5
MULTD	**F0**	**F2**	**F4**	3	15	16
SUBD	**F8**	**F6**	**F2**	4	7	8
DIVD	**F10**	**F0**	**F6**	5	56	
ADDD	**F6**	**F8**	**F2**	6	10	11

Load1	No	
Load2	No	
Load3	No	

Resevation Stations

Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	**No**					
0	Add2	**No**					
0	Add3	**No**					
0	Mult1	**No**					
1	Mult2	**Yes**	DIVD	M*F4	M[34+R2]		

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12	…	F30
56	FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

Tomasulo Example Cycle 57

Instruction Status

		j	k	Issue	Execution Complete	Write Result			Busy	Address		
LD	**F6**	**34+**	**R2**	1	3	4		Load1	No			
LD	**F2**	**45+**	**R3**	2	4	5		Load2	No			
MULTD	**F0**	**F2**	**F4**	3	15	16		Load3	No			
SUBD	**F8**	**F6**	**F2**	4	7	8						
DIVD	**F10**	**F0**	**F6**	5	56	57						
ADDD	**F6**	**F8**	**F2**	6	10	11						

Resevation Stations

	Time	Name	Busy	OP	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
	0	Add1	**No**					
	0	Add2	**No**					
	0	Add3	**No**					
	0	Mult1	**No**					
	0	Mult2	**No**					

Register result status

Clock				F0	F2	F4	F6	F8	F10	F12	…	F30
57			FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	M*F4/M			

Tomasulo Loop Example

```
Loop: LD      F0    0     R1
      MULTD   F4    F0    F2
      SD      F4    0     R1
      SUBI    R1    R1    #8
      BNEZ    R1    Loop
```

- Multiply takes 4 clock cycles
- Loads have cache misses

Loop Example Cycle 0

Instruction status

Instruction		j	k	iteration	Issue	Execution complete	Write Result
LD	F0	0	R1	1			
MULTD	F4	F0	F2	1			
SD	F4	0	R1	1			
LD	F0	0	R1	2			
MULTD	F4	F0	F2	2			
SD	F4	0	R1	2			

	Busy	Address	Qi
Load1	No		
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	No					
0	Mult2	No					

Code:

```
LD    F0   0  R1
MULTD F4   F0 F2
SD    F4   0  R1
SUBI  R1   R1 #8
BNEZ  R1   Loop
```

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12 ...	F30
0	80	Qi								

Loop Example Cycle 1

Instruction status

Instruction	j	k	iteration	Issue	Execution complete	Write Result
LD F0	0	R1	1	1		
MULTD F4	F0	F2	1			
SD F4	0	R1	1			
LD F0	0	R1	2			
MULTD F4	F0	F2	2			
SD F4	0	R1	2			

	Busy	Address	Qi
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	No					
0	Mult2	No					

Code:

```
LD    F0   0  R1
MULTD F4   F0 F2
SD    F4   0  R1
SUBI  R1   R1 #8
BNEZ  R1   Loop
```

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12 ...	F30
1	80	Qi	Load1							

Loop Example Cycle 2

Instruction status

Instruction	j	k	iteration	Issue	Execution complete	Write Result
LD F0	0	R1	1	1		
MULTD F4	F0	F2	1	2		
SD F4	0	R1	1			
LD F0	0	R1	2			
MULTD F4	F0	F2	2			
SD F4	0	R1	2			

	Busy	Address	Qi
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	Yes	MULTD		R(F2)	Load1	
0	Mult2	No					

Code:

```
LD    F0   0  R1
MULTD F4   F0 F2
SD    F4   0  R1
SUBI  R1   R1 #8
BNEZ  R1   Loop
```

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12 ...	F30
2	80	Qi	Load1		Mult1					

Loop Example Cycle 3

Instruction status

Instruction	j	k	iteration	Issue	Execution complete	Write Result
LD F0	0	R1	1	1		
MULTD F4	F0	F2	1	2		
SD F4	0	R1	1	3		
LD F0	0	R1	2			
MULTD F4	F0	F2	2			
SD F4	0	R1	2			

	Busy	Address	Qi
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	Yes	MULTD		R(F2)	Load1	
0	Mult2	No					

Code:

```
LD    F0   0  R1
MULTD F4   F0 F2
SD    F4   0  R1
SUBI  R1   R1 #8
BNEZ  R1   Loop
```

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12 ...	F30
3	80	Qi	Load1		Mult1					

Loop Example Cycle 4

Instruction status												
Instruction		*j*	*k*	*iteration*	*Issue*	*Executi complet*	*Write Result*		Busy	Address		
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			

Reservation Stations					*S1*	*S2*	*RS for*	*RS for k*				
	Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*	*Code:*			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loop	

Register result status												
Clock		R1		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	*...*	*F30*
4		80	*Qi*	Load1		Mult1						

Loop Example Cycle 5

Instruction status												
Instruction		*j*	*k*	*iteration*	*Issue*	*Executi complet*	*Write Result*		Busy	Address		
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			

Reservation Stations					*S1*	*S2*	*RS for*	*RS for k*				
	Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*	*Code:*			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loop	

Register result status												
Clock		R1		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	*...*	*F30*
5		**80**	*Qi*	Load1		Mult1						

Loop Example Cycle 6

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
0	Mult2	No						BNE	R1	Loop	

Register result status											
Clock	R1		F0	F2	F4	F6	F8	F10	F12	...	F30
6	72	Qi	Load2		Mult1						

Loop Example Cycle 7

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2	7			Store2	No			
SD	F4	0	R1	2				Store3	No			

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
7		72	Qi	Load2		Mult2						

Loop Example Cycle 7

	Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
In	LD	F0	0	R1	1	1			Load1	Yes	80		
LI	MUL	F4	F0	F2	1	2			Load2	Yes	72		
M	SD	F4	0	R1	1	3	4		Load3	No		Qi	
SI	SUBI	R1	R1	#8	1	4	5	6					
LI	BNE	R1	Loop		1	5	7	-					
M	LD	F0	0	R1	2	6			Store1	Yes	80	Mult1	
SI	MUL	F4	F0	F2	2	7			Store2	No			
R	SD	F4	0	R1	2				Store3	No			

	Reservation Stations				S1	S2	RS for	RS for k				
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
R	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loop	

C	Register result status											
	Clock	R1		F0	F2	F4	F6	F8	F10	F12	...	F30

Loop Example Cycle 8

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2	
SD	F4	0	R1	2	8			Store3	No			

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
8		72	Qi	Load2		Mult2						

Loop Example Cycle 9

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1	9		Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2	
SD	F4	0	R1	2	8	9		Store3	No			

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
9		72	Qi	Load2		Mult2						

Loop Example Cycle 10

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6	10		Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2	
SD	F4	0	R1	2	8	9		Store3	No			

Reservation Stations	Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for Qj	RS for k Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
10		72	Qi	Load2		Mult2						

Loop Example Cycle 11

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address		
LD	F0	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1	
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2	
SD	F4	0	R1	2	8	9		Store3	No			

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
4	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
0	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
11		64	Qi			Mult2						

Loop Example Cycle 12

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2			Load2	No		
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2
SD	F4	0	R1	2	8	9		Store3	No		

Reservation Stations	Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for Qj	RS for k Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	3	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	4	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
12		64	Qi			Mult2						

Loop Example Cycle 13

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2			Load2	No		
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2
SD	F4	0	R1	2	8	9		Store3	No		

Reservation Stations				S1	S2	RS for	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:		
0	Add1	No						LD	F0	0 R1
0	Add2	No						MUL	F4	F0 F2
0	Add3	No						SD	F4	0 R1
2	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1 #8
3	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loop

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
13		64	Qi			Mult2						

Loop Example Cycle 14

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2	14		Load2	No		
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mult1
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mult2
SD	F4	0	R1	2	8	9		Store3	No		

Reservation Stations	Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for Qj	RS for k Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	1	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	2	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
14		64	Qi			Mult2						

Loop Example Cycle 15

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2	14	15	Load2	No		
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(80)*R
MUL	F4	F0	F2	2	7	15		Store2	Yes	72	Mult2
SD	F4	0	R1	2	8	9		Store3	No		

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	No						SUB	R1	R1	#8
1	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loop	

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12	...	F30
15	64	Qi			Mult2						

Loop Example Cycle 16

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2	14	15	Load2	No		
SD	F4	0	R1	1	3	4	16	Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(80)*R
MUL	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(72)*R
SD	F4	0	R1	2	8	9		Store3	No		

Reservation Stations				S1	S2	RS for	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						MUL	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load3		SUB	R1	R1	#8
0	Mult2	No						BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
16		64	Qi			Mult1						

Loop Example Cycle 17

Instruction		j	k	iteration	Issue	complet	Result		Busy	Address	
LD	F0	0	R1	1	1	9	10	Load1	No		
MUL	F4	F0	F2	1	2	14	15	Load2	No		
SD	F4	0	R1	1	3	4	16	Load3	Yes	64	Qi
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(80)*R
MUL	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(72)*R
SD	F4	0	R1	2	8	9	17	Store3	No		

Reservation Stations	Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for Qj	RS for k Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loop	

Register result status												
Clock		R1		F0	F2	F4	F6	F8	F10	F12	...	F30
17		64	Qi			Mult1						