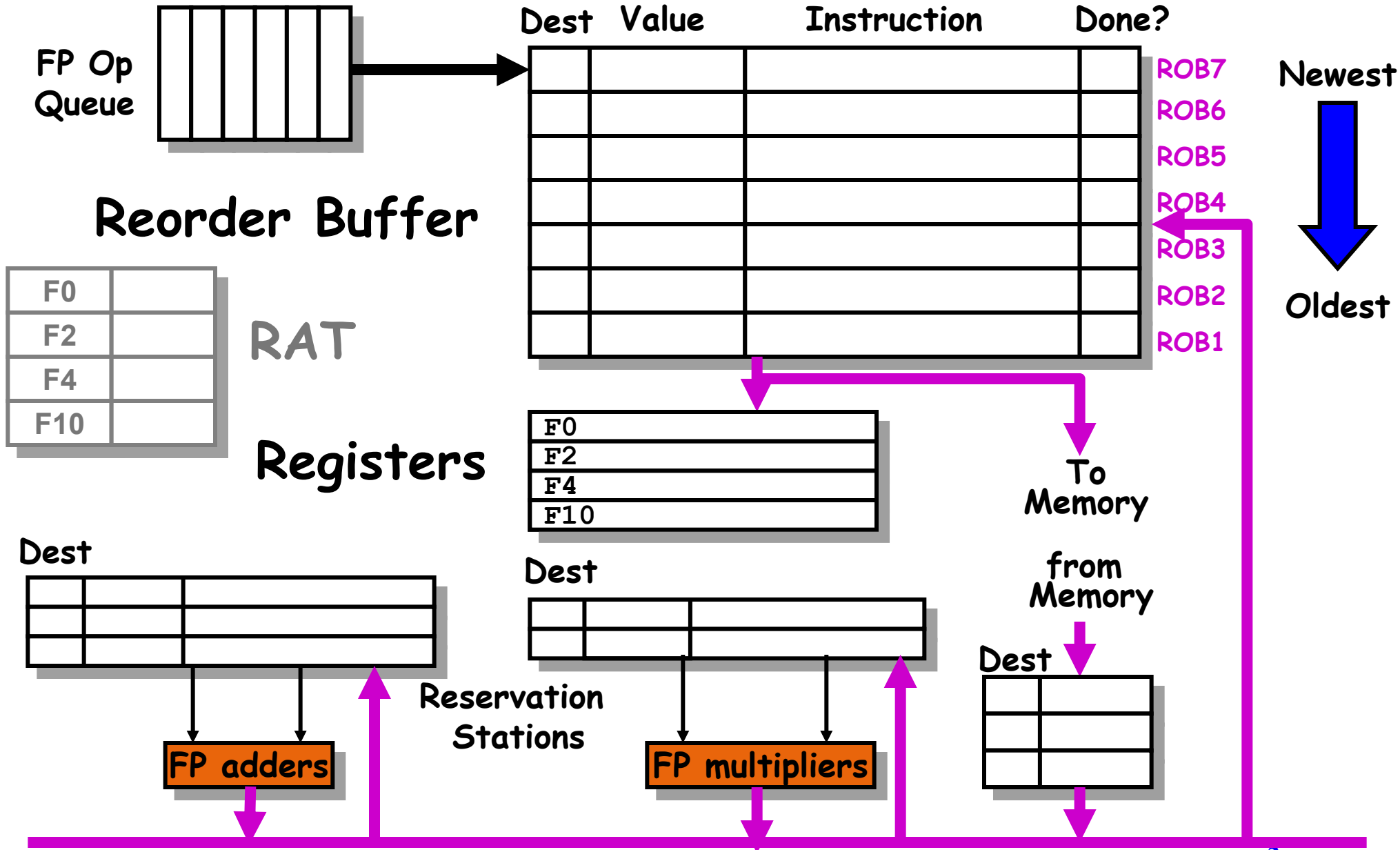


Example of code execution on a processor based on the Tomasulo architecture

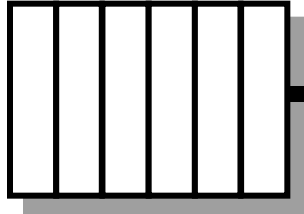
*Slides modified from Prof. Dave Patterson,
Prof. John Kubiawicz, Prof. Nancy Warter-Perez (Berkeley Un.), and
Zvika Guz (Technion)*

Tomasulo With Reorder buffer: architecture



Tomasulo With Reorder Buffer Structure

FP Op Queue



Reorder Buff

RAT

Registers

F0	
F2	
F4	
F10	

ROB2
ROB1

F0
F2
F4
F10

Dest

Reservation Stations

FP adders

FP multipliers

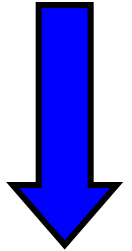
To Memory

from Memory

Dest

The Register Alias Table (RAT) is responsible for mapping between architectural and physical registers, thus implementing register renaming.

Newest



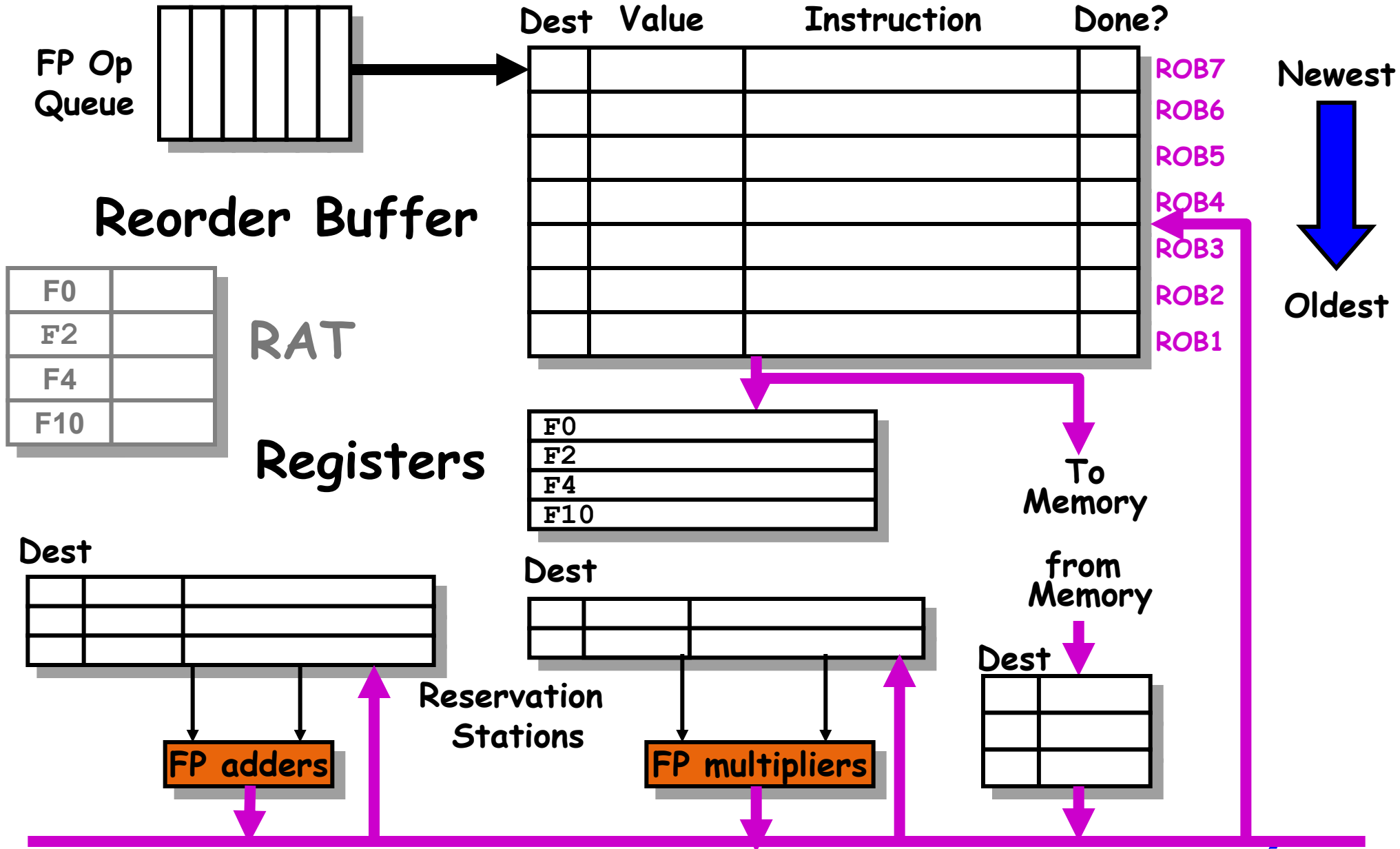
Oldest

Code example

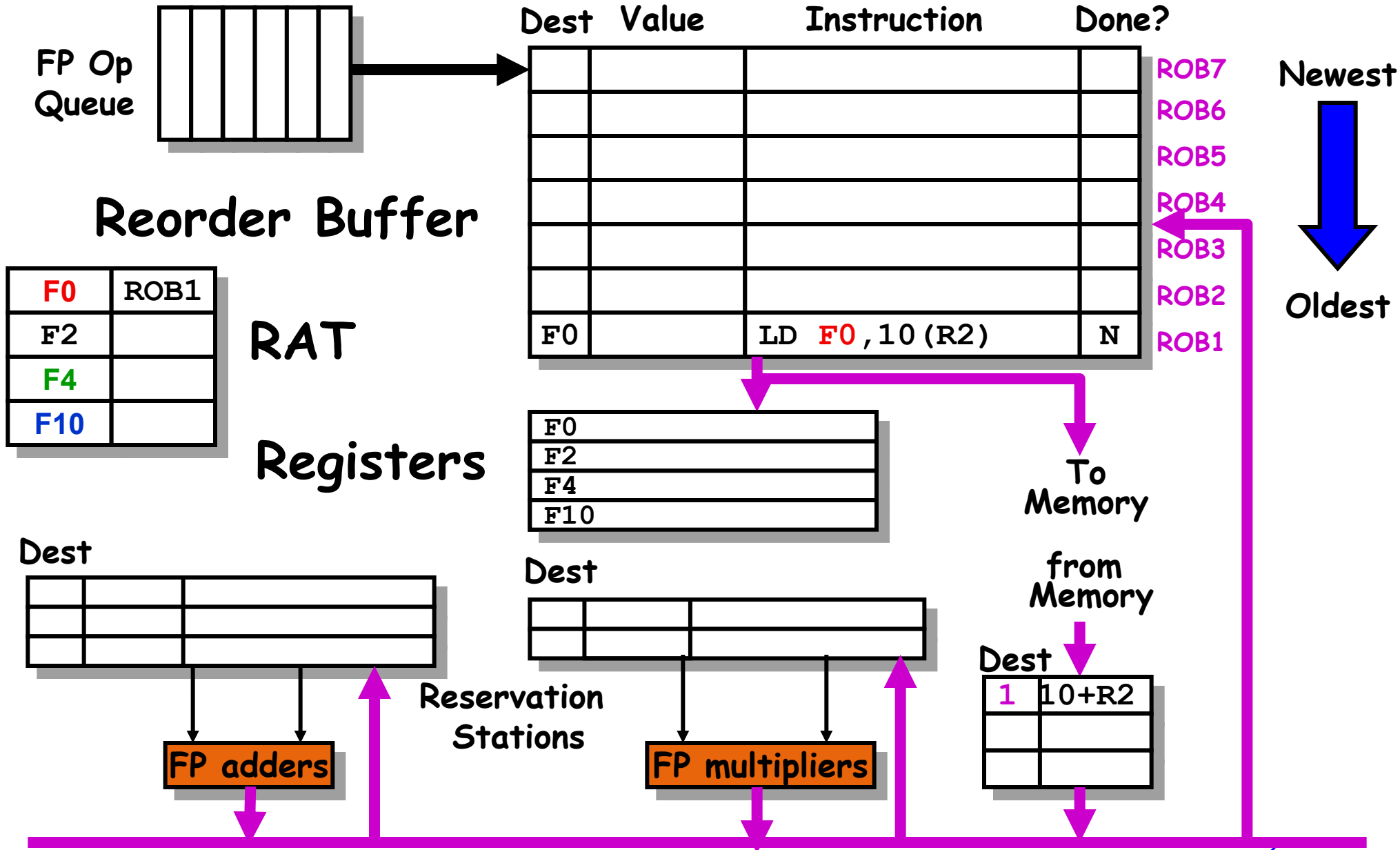
```
1. LD F0, 10(R2)
2. ADDD F10, F4, F0
3. DIVD F2, F10, F6
4. BNE F2, <LAB01>
5. LD F4, 0(R3)
6. ADDD F0, F4, F6
7. ADDD F0, F4, F6
```

<LAB01>

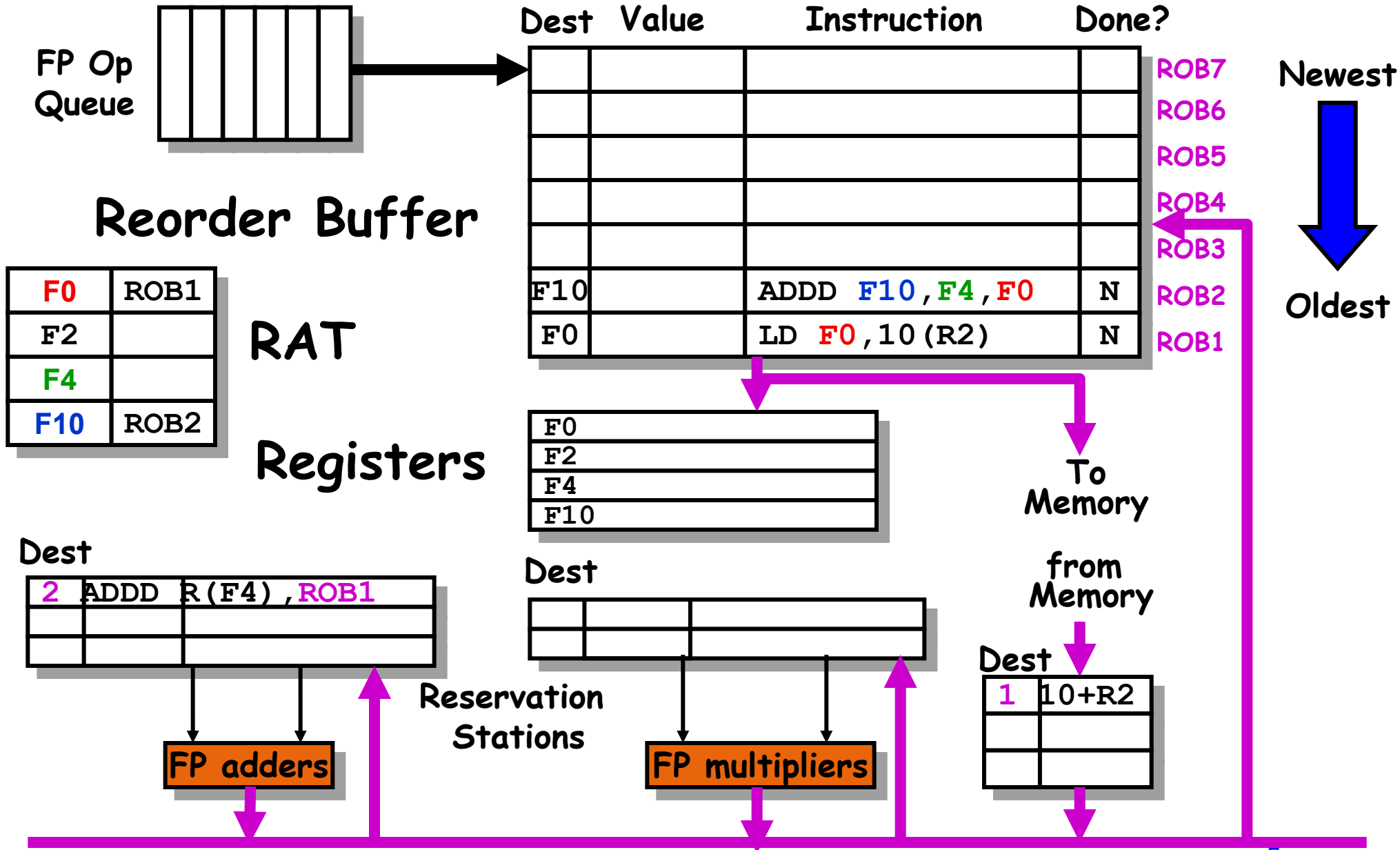
Tomasulo With Reorder buffer



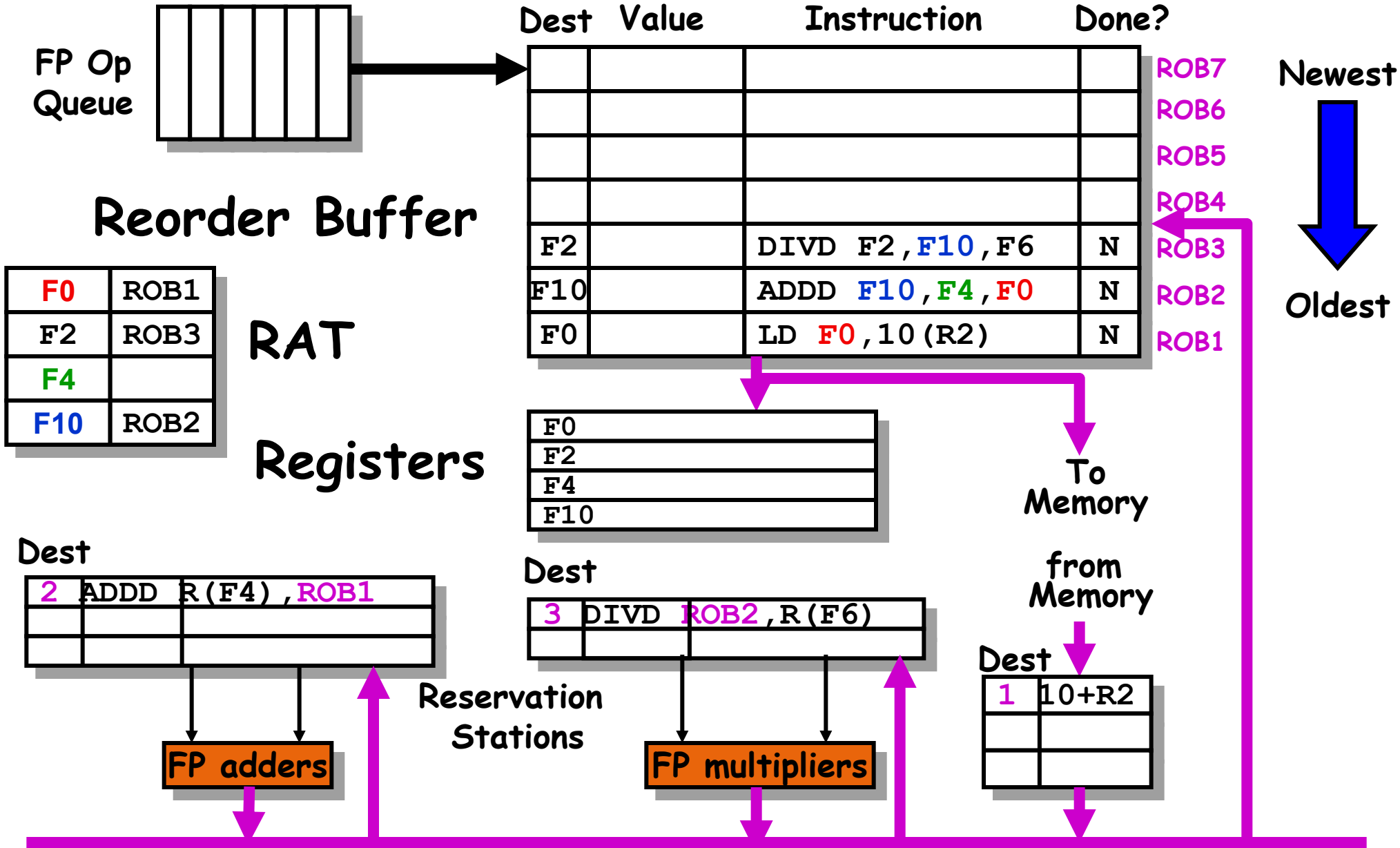
Tomasulo With Reorder buffer: 1



Tomasulo With Reorder buffer: 2

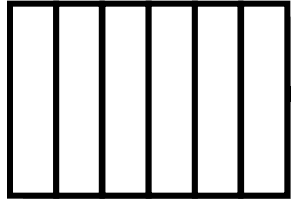


Tomasulo With Reorder buffer: 3



Tomasulo With Reorder buffer: 4, 5, 6

FP Op Queue



Reorder Buffer

F0	ROB6
F2	ROB3
F4	ROB5
F10	ROB2

RAT

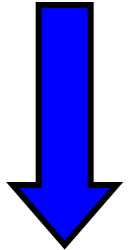
Registers

Dest Value Instruction Done?

F0		ADDD F0, F4, F6	N
F4		LD F4, 0 (R3)	N
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10		ADDD F10, F4, F0	N
F0		LD F0, 10 (R2)	N

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0
F2
F4
F10

To Memory

Dest

2	ADDD	R(F4), ROB1
6	ADDD	ROB5, R(F6)

FP adders

Dest

3	DIVD	ROB2, R(F6)

FP multipliers

Reservation Stations

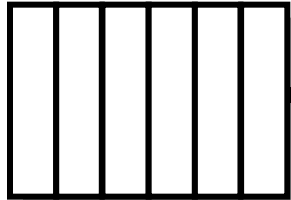
from Memory

Dest

1	10+R2
5	0+R3

Tomasulo With Reorder buffer: 7

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	ROB2

RAT

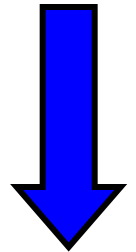
Registers

Dest Value Instruction Done?

F0		ADDD F0, F4, F6	N
F0		ADDD F0, F4, F6	N
F4		LD F4, 0 (R3)	N
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10		ADDD F10, F4, F0	N
F0		LD F0, 10 (R2)	N

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0
F2
F4
F10

To Memory

from Memory

Dest

2	ADDD	R(F4), ROB1
6	ADDD	ROB5, R(F6)
7	ADDD	ROB5, R(F6)

FP adders

Reservation Stations

Dest

3	DIVD	ROB2, R(F6)

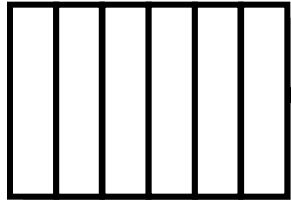
FP multipliers

Dest

1	10+R2
5	0+R3

Tomasulo With Reorder buffer: 8

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	ROB2

RAT

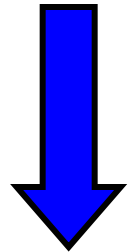
Registers

Dest Value Instruction Done?

F0		ADDD F0, F4, F6	N
F0		ADDD F0, F4, F6	N
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10		ADDD F10, F4, F0	N
F0		LD F0, 10 (R2)	N

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0
F2
F4
F10

To Memory

from Memory

Dest

2	ADDD	R(F4), ROB1
6	ADDD	M[10], R(F6)
7	ADDD	M[10], R(F6)

FP adders

Reservation Stations

Dest

3	DIVD	ROB2, R(F6)

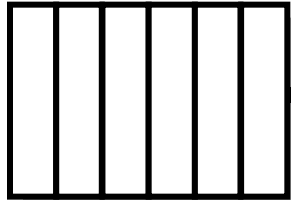
FP multipliers

Dest

1	10+R2

Tomasulo With Reorder buffer: 9

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	ROB2

RAT

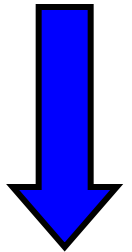
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10		ADDD F10, F4, F0	N
F0		LD F0, 10 (R2)	N

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0
F2
F4
F10

To Memory

from Memory

Dest

2	ADDD R(F4), ROB1

Dest

3	DIVD ROB2, R(F6)

Dest

1	10+R2

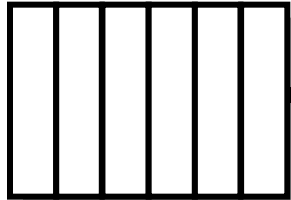
Reservation Stations

FP adders

FP multipliers

Tomasulo With Reorder buffer: 10

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	ROB2

RAT

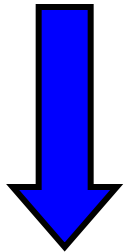
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10		ADDD F10, F4, F0	N
F0	M[2]	LD F0, 10 (R2)	Y

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0
F2
F4
F10

To Memory

from Memory

Dest

2	ADDD R(F4), M[2]

Dest

3	DIVD ROB2, R(F6)

Dest

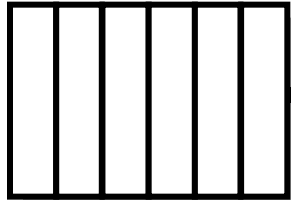
Reservation Stations

FP adders

FP multipliers

Tomasulo With Reorder buffer: 11

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	ROB2

RAT

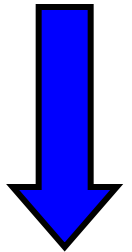
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2		DIVD F2, F10, F6	N
F10	<val4>	ADDD F10, F4, F0	Y
F0	M[2]	LD F0, 10 (R2)	C

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0 = M[2]
F2
F4
F10

To Memory

from Memory

Dest

FP adders

Reservation Stations

Dest

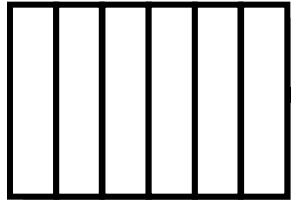
3	DIVD <val4>, R(F6)

FP multipliers

Dest

Tomasulo With Reorder buffer: 12

FP Op Queue



Reorder Buffer

F0	ROB7
F2	ROB3
F4	ROB5
F10	

RAT

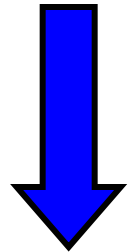
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2	<val5>	DIVD F2, F10, F6	Y
F10	<val4>	ADDD F10, F4, F0	C
F0	M[2]	LD F0, 10 (R2)	C

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0 = M[2]
F2
F4
F10 = <val4>

To Memory

Dest

FP adders

Reservation Stations

Dest

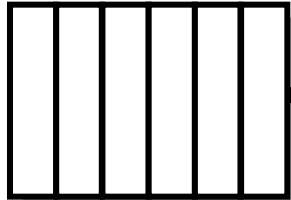
FP multipliers

from Memory

Dest

Tomasulo With Reorder buffer: 13

FP Op Queue



Reorder Buffer

F0	ROB7
F2	
F4	ROB5
F10	

RAT

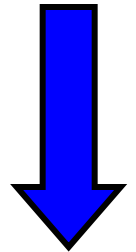
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	N
F2	<val5>	DIVD F2, F10, F6	C
F10	<val4>	ADDD F10, F4, F0	C
F0	M[2]	LD F0, 10 (R2)	C

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0 = M[2]
F2 = <val5>
F4
F10 = <val4>

To Memory

from Memory

Dest

FP adders

Reservation Stations

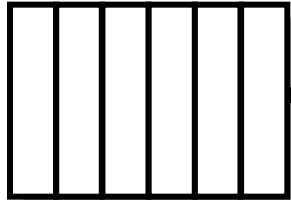
Dest

FP multipliers

Dest

Tomasulo With Reorder buffer: 14

FP Op Queue



Reorder Buffer

F0	ROB7
F2	
F4	ROB5
F10	

RAT

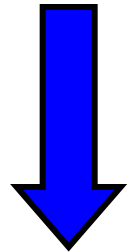
Registers

Dest Value Instruction Done?

F0	<val3>	ADDD F0, F4, F6	Y
F0	<val2>	ADDD F0, F4, F6	Y
F4	M[10]	LD F4, 0 (R3)	Y
--		BNE F2, <...>	C
F2	<val5>	DIVD F2, F10, F6	C
F10	<val4>	ADDD F10, F4, F0	C
F0	M[2]	LD F0, 10 (R2)	C

ROB7
ROB6
ROB5
ROB4
ROB3
ROB2
ROB1

Newest



Oldest

F0 = M[2]
F2 = <val5>
F4
F10 = <val4>

To Memory

Dest

FP adders

Dest

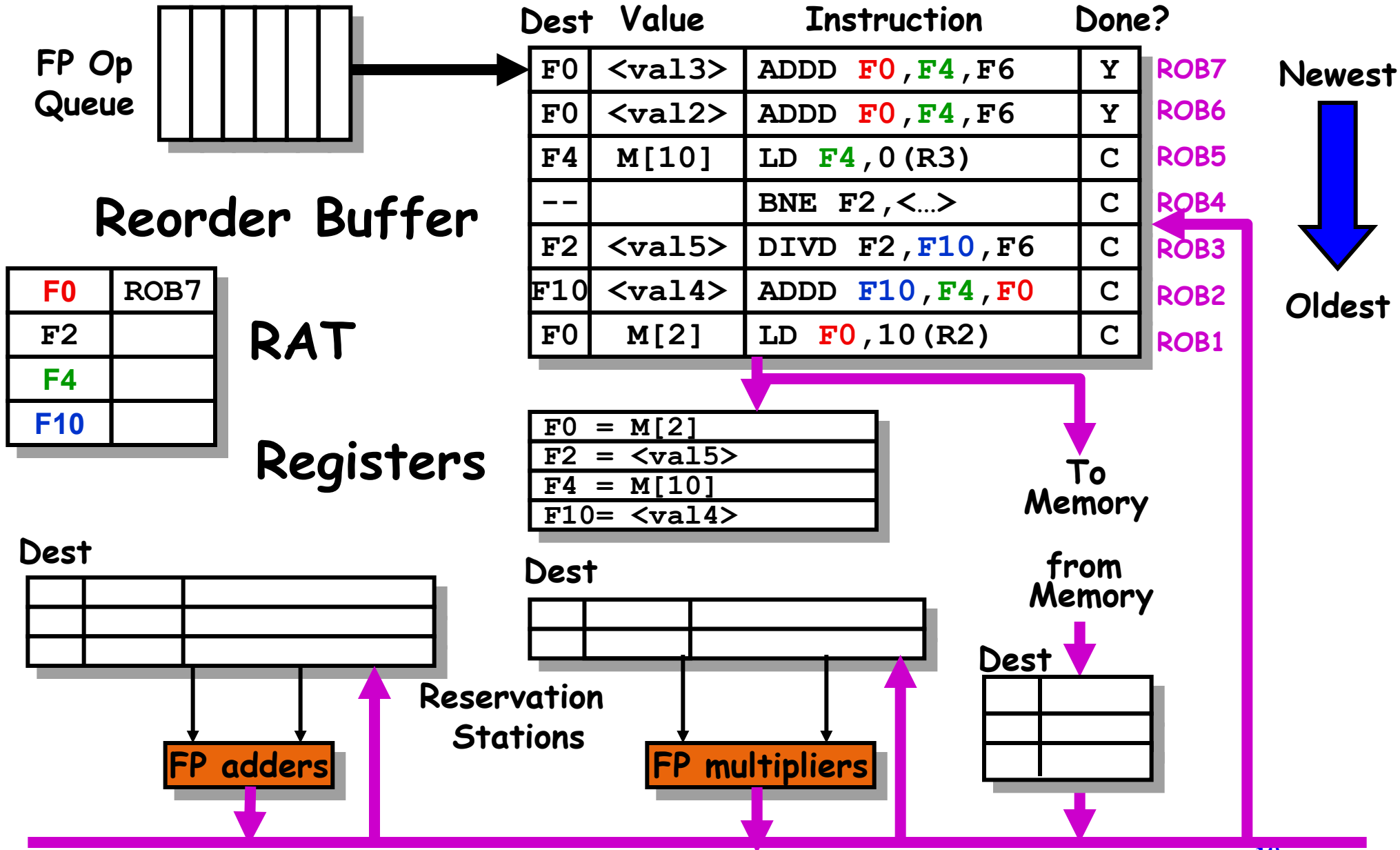
FP multipliers

Reservation Stations

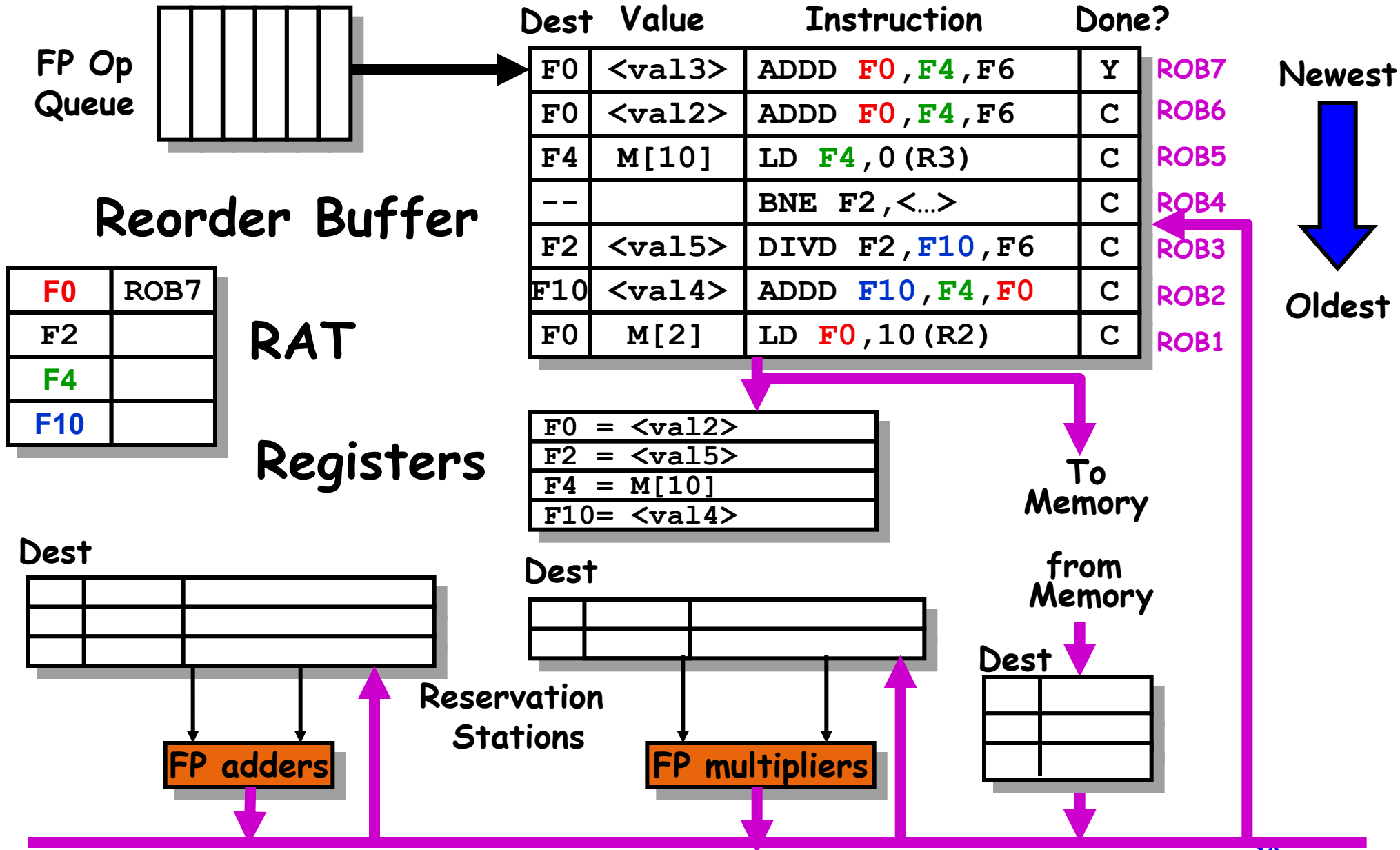
from Memory

Dest

Tomasulo With Reorder buffer: 15



Tomasulo With Reorder buffer: 16



Tomasulo With Reorder buffer: 17

