01-09-2025 – ASE exam

*Student Name and ID:*_____

Question 1

Considering the architecture of a RISC-V processor RV32G with single-precision FP operations presented in the following:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP multiplier unit: pipelined 8 stages
- FP arithmetic unit: pipelined 4 stages
- FP divider unit: not pipelined unit that requires 8 clock cycles
- branch delay slot: 1 clock cycle, and the branch delay slot disabled
- forwarding enabled
- it is possible to complete instruction EXE stage in an out-of-order fashion.

Using the following code fragment, show the timing of the presented loop-based program and compute how many cycles does this program take to execute?

```
for (i = 0; i < 100; i++) {
    v4[i] = v1[i] + v2[i];
    v5[i] = v2[i] * v3[i];
    v6[i] = v1[i] / v3[i]; }
```

																																			Clock cycles
V1: .word "100 values"																																			
V2: .word "100 values"																																			
V3: .word "100 values"																																			
V4: .word "100 zeroes"																																			
…																																			
.text																																			
main:																																			
addi x7, x0, 100	F	D	E	M	W																														5
la x1, V1																																			2
la x2, V2																																			2
la x3, V3																																			2
la x4, V4																																			2
la x5, V5																																			2
la x6, V6	D	E	M	W																															2
loop:																																			
flw f1, 0(x1)	F	D	E	M	W																														1
flw f2, 0(x2)		F	D	E	M	W																													1
fadd.s f4, f1, f2			F	D	S	A	A	A	A	M	W																								5
flw f3, 0(x3)				F	S	D	E	M	W																										0

01-09-2025 – ASE exam

*Student Name and ID:*____

fsw f4, 0(x4)						F	D	E	S	S	M	W																									1
fmul.s f5, f2, f3							F	D	X	X	X	X	X	X	X	X	M	W																			6
fsw f5, 0(x5)								F	D	S	E	S	S	S	S	S	S	M	W																		1
fdiv.s f6, f1, f3									F	S	D	/	/	/	/	/	/	/	/	M	W																2
fsw f6, 0(x6)											F	D	S	S	S	S	S	E	S	S	M	W															1
addi x1, x1, 4												F	S	S	S	S	S	D	S	S	E	M	W														1
addi x2, x2, 4																		F	S	S	D	E	M	W													1
addi x3, x3, 4																					F	D	E	M	W												1
addi x4, x4, 4																						F	D	E	M	W											1
addi x5, x5, 4																							F	D	E	M	W										1
addi x6, x6, 4																								F	D	E	M	W									1
addi x7, x7, -1																									F	D	E	M	W								1
bnez x7, loop																										F	S	D	E	M	W						2+1
nop																												F	-	-	-	-					1
TOTAL																																					2817

*Student Name and ID:*_____

Question 2

Considering the previous program, and in particular the following two instructions:

```
addi  x7, x7, -1
bnez  x7, loop
```

what type of hazard is caused by the use of register x7, and how is it resolved? Justify your answer.

➔ RAW

*Student Name and ID:*_____

Question 3

Considering the previous program, and in particular the following two instructions:

```
fdiv.s f6, f1, f3

fsw  f6, 0(x6)
```

what type of hazard is caused by the use of register F6, and how is it resolved? Justify your answer.

➔ RAW

➔ at the end a control hazard is also caused due to the possible access of two instructions to the MEM stage