CMPT 300 Assignment 1

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Problem 2

a. Direct mapping

There are 2048 cache slots. Initial state – Cache lines 0 ~549 are already in cache slots 0~549.

Loop 1 contains cache lines 400~950 that map to cache slots 400~950.

Loop 2a contains cache lines 4666~5028 that map to cache slots 570~932.

Loop 2b contains cache lines 16968~17314 that map to cache slots 584~930.

Loop 1 (Cycle 1)

- § Cache lines 400~549 are HITS due to the initial condition.
  =150 hits x 5 accesses = 750 hits
- § Cache lines 550~950 are loaded and accessed 5 times.
  - o Cache lines 550~950 are MISSES as these slots are empty.
    = 401 misses
  - o Once cache lines 550~950 are loaded, the lines are accessed 4 more times.
    = 401 lines x 4 accesses = 1,604 hits

Loop 1 (Subsequent 7 cycles)

- § Cache lines 400~950 are all HITS
  =551 hits x 5 accesses x 7 cycles = 19,285 hits

Loop 1 Total 750 +1604 + 19,285 = 21,639 hits, 401 misses

1st time through Loop 2a (Cycle 1)

- § Cache slots 400~950 are all occupied by the cache lines from loop 1.
- § Cache lines 4666~5028 are loaded:
  - o Cache lines 4666~5028, which map to cache slots 570~932, are MISSES.
    = 363 misses
  - o Once cache lines 4666~5028 are loaded, the lines are accessed 2 times.
    = 363 lines x 2 times = 726 hits

1st time through loop 2b (Cycle 1)

- § Cache lines 16968~17314 map to cache slots 584~930.
- § Cache slots 584~930 are occupied by the cache lines from loop 2a.
- § Cache lines 584~930 are loaded:
  - o Cache lines 16968~17314 (cache slots 584~930) are all MISSES.
    = 347 misses
  - o Once cache lines 16968 ~17314 are loaded, the lines are accessed 2 times

= 347 hits x 2 accesses = 694 hits

Total for Loop 2 (Cycle 1) 726+694 hits = 1,420 hits, 363+347 misses = 710 misses

Loop 2a (Subsequent 42 cycles)

cache lines 16968~17314 (cache slots 584~930) are all MISSES.
-> 347 misses * 42 cycles = **14,574 misses**
The cache lines are loaded to cache slots 584~930:
347 hits * 2 accesses * 42 cycles = 29,148 hits
CL 570~583 -> 14 hits
CL 931~932 -> 2 hits
-> 16 hits x 3 accesses x 42 cycles = 2016 hits

Loop 2b (Subsequent cycles)

CL 584~930 - > 347 misses
-> 347 misses * 42 cycles = **14,574 misses**
Appropriate cache lines are loaded to cache slots 584~930 = 347 hits
-> 347 hits x 2 accesses x 42 cycles = 29,148 hits

Total for loop 2 (Subsequent) 2016+29148 + 29148= **60312 hits** 14574+14574=**29,148** misses

Therefore Loop 1 and Loop 2 have the following figures,

Total for Loop 1: 750 +1604 + 19,285 = 21,639 hits, 401 misses

Total for Loop 2 (Cycle 1) 726+694 hits = 1,420 hits, 363+347 misses = 710 misses

Total for loop 2 (Subsequent) 2016+29148 + 29148= 60312 hits 14574+14574=29,148 misses

Total (loop 1 + loop 2)

21,639 + 1,420 + 60,312 = **83,362 hits**

401 + 710 + 29,148 = **30,259 misses**

Hit ratio = 83,362 hits / (83,362 hits + 30,259 misses) = **0.7337**

b. Four-way associative mapping

Loop 1 – 5 accesses per line, and Loop 2 – 3 accesses per line.

Initial – Cache lines 0~549 are already loaded in the cache slots.

First loop (Cycle 1)

- Load CL 400~950 -> First slots of Groups 0~511 are filled. Second slots of Group 0~37 are filled.
- **CL 400~549 are already loaded -> 150 cache hits x 5 accesses = 750 hits.**

- **For CL 550~950, we get 401 misses. This causes CL 550~950 to be loaded into second slots of Group 38~438. Then, we get 401x4 accesses = 1604 hits.**

750 + 1604 hits = 2354 hits

401 misses

First loop (Subsequent cycles)

- Cache lines 400~950 are already loaded. All hits.
  - 551 hits x 5 accesses x 7 cycles = 19,285 hits

Second loop (Cycle 1)

- **For Cl 4666~5028, we get 363 misses**. This causes Cl 4666~5028 to be loaded.
  - 3rd slots of Groups 58 to 420 are filled.
  - Once loaded, 2 accesses to each line = 363 lines *2 accesses = **726 hits**
- **For Cl 16968~17314, we get 347 misses**
  - 4th slots of Group 72~418 are filled.
  - Once loaded, 2 accesses to each line = 347 lines * 2 accesses = **694 hits**

726 + 694 =1420 hits

363+347=710 misses

Second loop (Subsequent cycles)

- Cache lines 4666~5028 and 16968~17314 are already loaded. All hits.
- 710 hits x 3 accesses = 2,130 hits
- 2,130 hits x 42 cycles = 89,460 hits

Total for the entire process

2354 + 19285 + 1420 + 89460 hits = 112,519 hits

401 + 710 misses = 1,111 miss

Hit ratio = 112519 hits / (112,519 hits + 1,111 misses) = 0.9902

Problem 3

Color	Meaning
	On the way to the center
10	**Running in the CPU (Cumulative run time of 10 ms)**
	Waiting in the ready queue
	Processing IO

Each cell represents a one-second interval.

a) Round-robin scheduling (no priorities)

Turnaround time

D - 43ms

C - 89 ms

A - 99 ms

B - 109 ms

Average turnaround time = 85 ms

Time (ms)	C	D	A	B	Ready Q	CPU	Print Q Then IO
1					{ }	{ }	{ }
2					{C}	{ }	{ }
3					{ }	{C}	{ }
4					{ }	{C}	{ }
5	6				{ }	{C}	{ }
6					{ }	{C}	{ }

7					{D}	{C}	{ }
8					{D, C}	{C}	{ }
9					{C}	{D}	{ }
10		3			{C}	{D}	{ }
11					{C}	{D}	{ }
12					{A}	{C}	{D}
13					{A}	{C}	{D}
14					{D, A}	{C}	{ }
15	12				{D, A}	{C}	{ }
16					{D, A}	{C}	{ }
17					{D, A}	{C}	{ }
18					{A, C}	{D}	{ }
19		6			{A, C, B}	{D}	{ }
20					{A, C, B}	{D}	{ }
21					{C, B, D}	{A}	{D}
22					{C, B, D}	{A}	{D}
23			6		{C, B, D}	{A}	{ }
24					{C, B, D}	{A}	{ }
25					{C, B, D}	{A}	{ }
26					{C, B, D}	{A}	{ }
27					{B, D, A}	{C}	{ }
28					{B, D, A}	{C}	{ }
29	18				{B, D, A}	{C}	{ }
30					{B, D, A}	{C}	{ }
31					{B, D, A}	{C}	{ }
32					{B, D, A}	{C}	{ }

33					{D, A, C}	{B}	{ }
34					{D, A, C}	{B}	{ }
35				6	{D, A, C}	{B}	{ }
36					{D, A, C}	{B}	{ }
37					{D, A, C}	{B}	{ }
38					{D, A, C}	{B}	{ }
39					{A, C, B}	{D}	{ }
40		9			{A, C, B}	{D}	{ }
41					{A, C, B}	{D}	{ }
42					{C, B}	{A}	{D}
43					{C, B}	{A}	{D}
44			12		{C, B}	{A}	{ }
45	C		A	B	{C, B}	{A}	{ }
46					{C, B}	{A}	{ }
47					{C, B}	{A}	{ }
48					{B, A}	{C}	{ }
49					{B, A}	{C}	{ }
50	24				{B, A}	{C}	{ }
51					{B, A}	{C}	{ }
52					{B, A}	{C}	{ }
53					{B, A}	{C}	{ }
54					{A, C}	{B}	{ }
55					{A, C}	{B}	{ }
56				12	{A, C}	{B}	{ }
57					{A, C}	{B}	{ }
58					{A, C}	{B}	{ }

59					{A, C}	{B}	{ }
60					{C, B}	{A}	{ }
61					{C, B}	{A}	{ }
62			18		{C, B}	{A}	{ }
63					{C, B}	{A}	{ }
64					{C, B}	{A}	{ }
65					{C, B}	{A}	{ }
66					{B, A}	{C}	{ }
67					{B, A}	{C}	{ }
68	30				{B, A}	{C}	{ }
69					{B, A}	{C}	{ }
70					{B, A}	{C}	{ }
71					{B, A}	{C}	{ }
72					{A, C}	{B}	{ }
73					{A, C}	{B}	{ }
74				18	{A, C}	{B}	{ }
75					{A, C}	{B}	{ }
76					{A, C}	{B}	{ }
77					{A, C}	{B}	{ }
78					{C, B}	{A}	{ }
79					{C, B}	{A}	{ }
80			24		{C, B}	{A}	{ }
81					{C, B}	{A}	{ }
82					{C, B}	{A}	{ }
83					{C, B}	{A}	{ }
84					{B, A}	{C}	{ }

85					{B, A}	{C}	{ }
86	36				{B, A}	{C}	{ }
87					{B, A}	{C}	{ }
88					{B, A}	{C}	{ }
89					{B, A}	{C}	{ }
90					{A}	{B}	{ }
91					{A}	{B}	{ }
92				24	{A}	{B}	{ }
93					{A}	{B}	{ }
94					{A}	{B}	{ }
95					{A}	{B}	{ }
96					{B}	{A}	{ }
97			28		{B}	{A}	{ }
98					{B}	{A}	{ }
99					{B}	{A}	{ }
100					{ }	{B}	{ }
101					{ }	{B}	{ }
102				34	{ }	{B}	{ }
103					{ }	{B}	{ }
104					{ }	{B}	{ }
105					{ }	{B}	{ }
106					{ }	{B}	{ }
107					{ }	{B}	{ }
108					{ }	{B}	{ }
109					{ }	{B}	{ }
					{ }	{ }	{ }

b) Round-robin scheduling (with preemptive priorities)

<u>Turnaround time</u>

D - 22 ms

B - 54 ms

C - 107 ms

A- 109 ms

Average turnaround time = 73 ms

Time (ms)	C 36	D 9	A 28	B 34	LP	HP	CPU	Print Q Then IO
1					{ }	{ }	{ }	{ }
2					{C}	{ }	{ }	{ }
3					{ }	{ }	{C}	{ }
4	5				{ }	{ }	{C}	{ }
5					{ }	{ }	{C}	{ }
6					{ }	{ }	{C}	{ }
7					{ }	{D}	{C}	{ }
8					{C}	{ }	{D}	{ }
9		3			{C}	{ }	{D}	{ }
10					{C}	{ }	{D}	{ }
11	7				{ }	{ }	{C}	{D}
12					{ }	{D}	{C}	{D}
13					{A, C}	{ }	{D}	{ }
14		6			{A, C}	{ }	{D}	{ }
15					{A, C}	{ }	{D}	{ }
16			2		{C}	{ }	{A}	{D}

17					{C}	{D}	{A}	{D}
18					{C, A}	{ }	{D}	{ }
19		9			{C, A}	{B}	{D}	{ }
20					{C, A}	{B}	{D}	{ }
21					{C, A}	{ }	{B}	{D}
22					{C, A}	{ }	{B}	{D}
. . .				34	{C, A}	{ }	{B}	{ }
					{C, A}	{ }	{B}	{ }
					{C, A}	{ }	{B}	{ }
54					{C, A}	{ }	{B}	{ }
60	13				{A}	{ }	{C}	{ }
66			8		{C}	{ }	{A}	{ }
72	19				{A}	{ }	{C}	{ }
78			14		{C}	{ }	{A}	{ }
84	25				{A}	{ }	{C}	{ }
90			20		{C}	{ }	{A}	{ }
96	31				{A}	{ }	{C}	{ }
102			26		{C}	{ }	{A}	{ }
107	36				{A}	{ }	{C}	{ }
109			28		{ }	{ }	{A}	{ }
					{ }	{ }	{ }	{ }

c) First come first served (non-preemptive priorities)

Turnaround time

C - 38 ms

B- 75ms

A - 106 ms

D - 111 ms

Average turnaround time = 82.5 ms

Time (ms)	C 36	D 9	A 28	B 34	LP	HP	CPU	Print Q Then IO
1					{ }	{ }	{ }	{ }
2					{C}	{ }	{ }	{ }
3					{ }	{ }	{C}	{ }
4					{ }	{ }	{C}	{ }
5					{ }	{ }	{C}	{ }
6					{ }	{ }	{C}	{ }
7					{ }	{D}	{C}	{ }
8					{ }	{D}	{C}	{ }
9					{ }	{D}	{C}	{ }
10	36				{ }	{D}	{C}	{ }
11					{ }	{D}	{C}	{ }
12					{A}	{D}	{C}	{ }
13					{A}	{D}	{C}	{ }
14					{A}	{D}	{C}	{ }
15					{A}	{D}	{C}	{ }
16					{A}	{D}	{C}	{ }
17					{A}	{D}	{C}	{ }
18					{A}	{D}	{C}	{ }
19					{A}	{D, B}	{C}	{ }
...					{A}	{D, B}	{C}	{ }

38					{A}	{D, B}	{C}	{ }
39					{A}	{B}	{D}	{ }
40		3			{A}	{B}	{D}	{ }
41					{A}	{B}	{D}	{ }
42					{A}	{ }	{B}	{D}
43					{A}	{ }	{B}	{D}
44				34	{A}	{D}	{B}	{ }
45					{A}	{D}	{B}	{ }
...					{A}	{D}	{B}	{ }
75					{A}	{D}	{B}	{ }
76					{A}	{ }	{D}	{ }
77		6			{A}	{ }	{D}	{ }
78					{A}	{ }	{D}	{ }
79					[ ]	{ }	{A}	{D}
80			28		{ }	{ }	{A}	{D}
81					{ }	{D}	{A}	{ }
...					{ }	{D}	{A}	{ }
106					{ }	{D}	{A}	{ }
107					{ }	{ }	{D}	{ }
108		9			{ }	{ }	{D}	{ }
109					{ }	{ }	{D}	{ }
110					{ }	{ }	{ }	{D}
111					{ }	{ }	{ }	{D}
112					{ }	{ }	{ }	{ }