# A Highly Linear Frequency Ramp Generator Based on a Fractional Divider Phase-Locked-Loop

Thomas Musch, Ilona Rolfes, and Burkhard Schiek

***Abstract*— A highly linear analog frequency ramp generator based on a fractional divider concept is presented. The frequency ramp linearity achievable in this fractional phase-locked-loop configuration is better than $10^{-4}$. This value is revealed by numerical simulations as well as by measurements performed with a prototype synthesizer implemented in a FMCW-radar system suitable for distance and velocity measurements.**

## I. Introduction

THE precision of radar systems based on the frequency modulated, continuous wave (FMCW) principle highly depends on the linearity of the frequency ramp generator. A variety of frequency synthesizer concepts exist. One possible way is to directly linearize a normal voltage controlled oscillator (VCO). The linearity that is achievable with a direct linearization circuit at the input of the VCO is rather poor. This is caused by the oscillator's nonlinear tuning curve, which can be compensated only partly with an analog linearization network.

The linearity of a VCO can be improved by controlling it within a phase-locked-loop (PLL). As the reference of the PLL-system is a high precision, longtime stable crystal-controlled-oscillator (XCO) the absolute precision and stability of the ramp is accordingly as good as the XCO itself. Consequently, a PLL linearization circuit can generate an analog frequency ramp with a good ramp linearity better than $10^{-4}$. The conventional PLL consists of a programmable frequency divider with a unity division ratio $N$. The analog ramp frequency results from the moving average of the reference frequency $f_{\mathrm{ref}}$ multiplied by $N$. The number of steps the divider executes on the ramp is limited by the fact that the frequency divider allows only unity steps.

The maximum number of steps $Z = Z_{\max} - Z_{\min}$ that the divider performs and the associated reference frequency $f_{\mathrm{ref}}$ at the phase-frequency-comparator are dependent of the ramp time $T$ and the ramp bandwidth $B$ with

$$Z = \sqrt{B \cdot T}$$
$$f_{\mathrm{ref}} = \sqrt{\frac{B}{T}}. \tag{1}$$

As the ramp time and the ramp bandwidth are often predefined by the radar system, the number of points $Z$ and the reference frequency are not variable. For example, the number of points with a ramp bandwidth $B$ of 1 GHz and a ramp time $T$ of 1 ms is $Z = 1000$. Problems can arise using a VCO with significant variations of the tuning curve slope. In order to achieve an excellent ramp linearity with a VCO showing rather abrupt changes in the tuning curve, a higher number of steps is desirable. For this purpose a fractional divider can be used advantageously. A fractional divider is programmable to make fractional steps in any step size instead of making only unity steps. This way many more division ratio steps can be executed on the ramp. Due to the fact that the reference frequency no longer influences the step size, the reference frequency is only limited by the speed of the digital components. For example, with a reference frequency of 50 MHz and a ramp time $T = 1$ ms, the number of points could be $Z_{\mathrm{frac}} = 50\ \mathrm{MHz} \cdot 1\ \mathrm{ms} = 50\,000$. With such a large number of steps the linearization effect of the PLL accordingly can be much better than in a system making only unity steps. The linearizing effect of the fractional PLL will be examined.

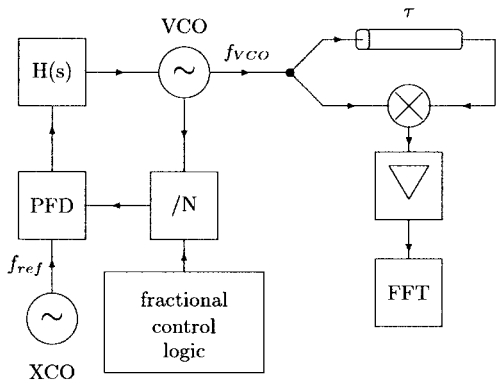


Fig. 1. Block diagram of a FMCW-system with a fractional ramp generator.

## II. Fractional Ramp Generator

A fractional synthesizer uses a divider whose division ratio is permanently changed so that its mean value is a fractional value. A block diagram of a fractional PLL ramp generator is shown in Fig. 1 together with a modified FMCW system for measuring the ramp quality. The VCO signal is divided and compared with the reference signal $f_{\mathrm{ref}}$ in a phase-frequency-discriminator (PFD). The output signal of the PFD is filtered by the loop filter $H(s)$. This loop filter has to suppress the reference frequency as well as the shaped quantization noise.

In order to inspect the ramp quality experimentally, a modified FMCW system with a long coaxial delay line is added to the fractional ramp generator. The divider $/N$ is programmed by the fractional control logic. Varying the division ratio rapidly causes quantization noise, resulting in phase noise on the PLL-controlled VCO. The fractional control logic

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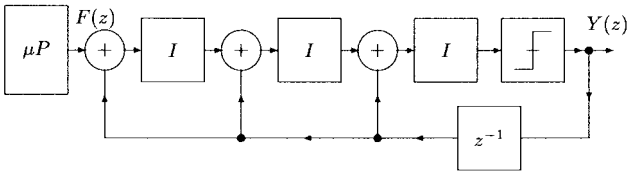


Fig. 2. Block diagram of the fractional control logic.

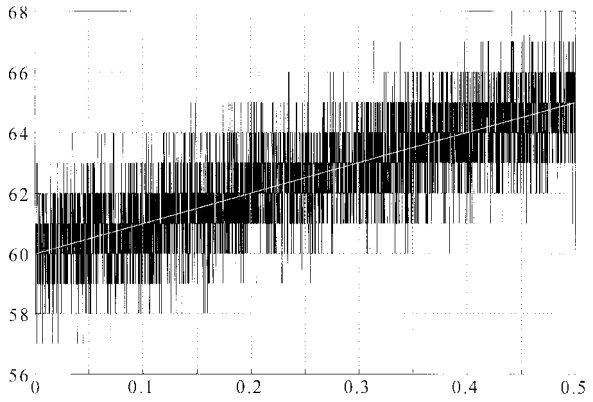


Fig. 3. Changes of the division ratio $N$.

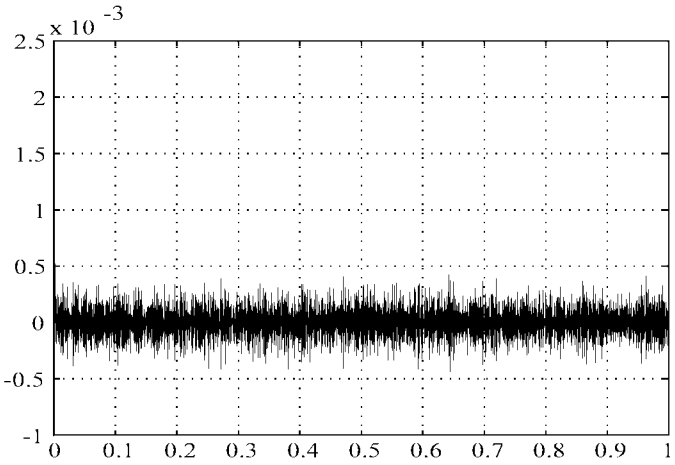


Fig. 4. Normalized deviation $\Delta f / f_{\mathrm{ref}}$ of the fractional generated ramp from the ideal ramp.

shapes this quantization noise to shift the spectral parts close to the carrier frequency further away from the carrier. The remaining noise at higher frequencies can be suppressed by the loop filter of the PLL. A block diagram of the fractional control logic of a three-stage unit is shown in Fig. 2 where a microprocessor $(\mu P)$ controls the fractional division ratio $F(s)$. The fractional control logic uses three integrators $(I)$ resulting in a 18 dB/octave slope in the noise shape.

The quantizer is a completely digital part. It only uses the most significant bits of the integrator as an output signal for the programmable divider. The fractional control logic can be described by the $z$-transform. If $F(z)$ is the input signal representing the fractional frequency information and $Q(z)$ is the quantization noise, the output signal $Y(z)$ that is given to the divider can be written as

$$Y(z) = F(z) + Q(z)(1 - z^{-1})^3 = F(z) + Q(z)D(z)^3. \quad (2)$$

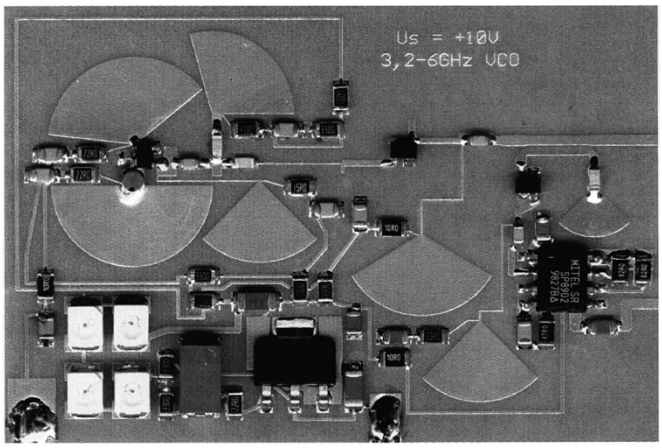


Fig. 5. Photo of the prototype 6 GHz-VCO.

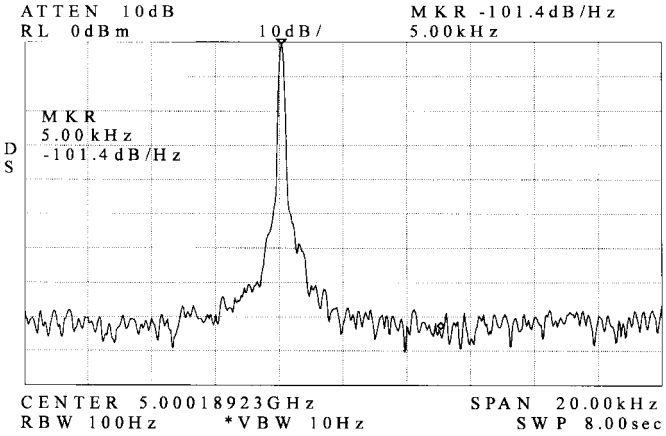


Fig. 6. VCO at 5 GHz with a phase noise of $-101.4$ dBc/Hz at a distance of 5 kHz.

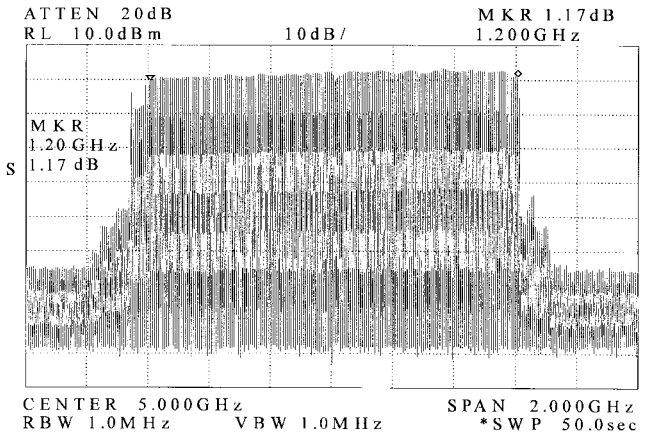


Fig. 7. Fractional frequency ramp with $B = 1.2$ GHz and $T = 13$ ms.

The term $D(z)$ represents the derivative in the $z$-transform. Therefore, the quantization noise $Q(z)$ is suppressed by $D(z)^3$ to lower frequencies while the fractional division ratio $F(z)$ is transmitted without any modification as desired.

## III. Simulations

The quantization noise has to be suppressed by the loop filter. In order to develop an optimum PLL circuit, especially with respect to the fractional quantization noise, several sim-

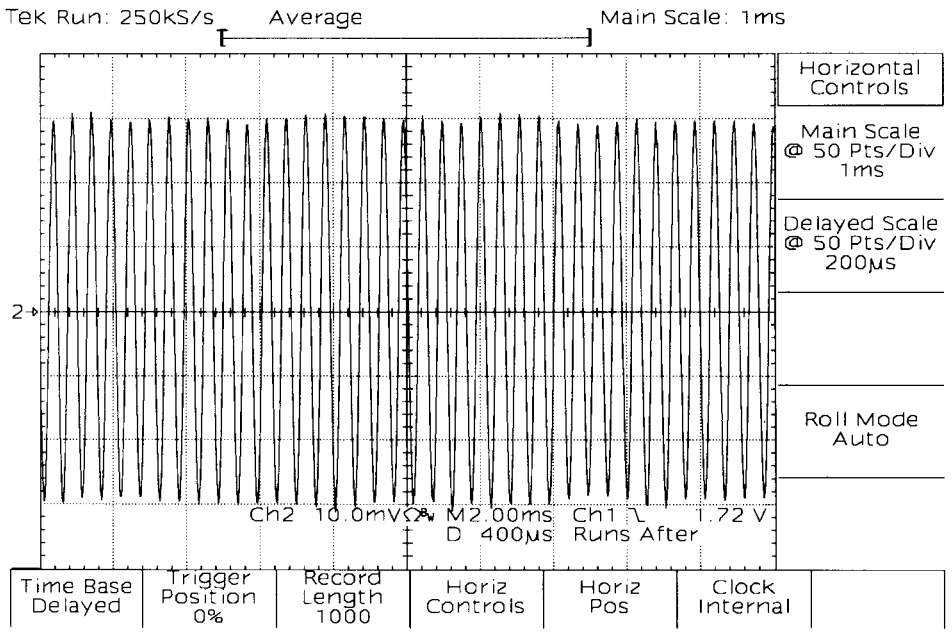


Fig. 8. IF-signal in the time domain.

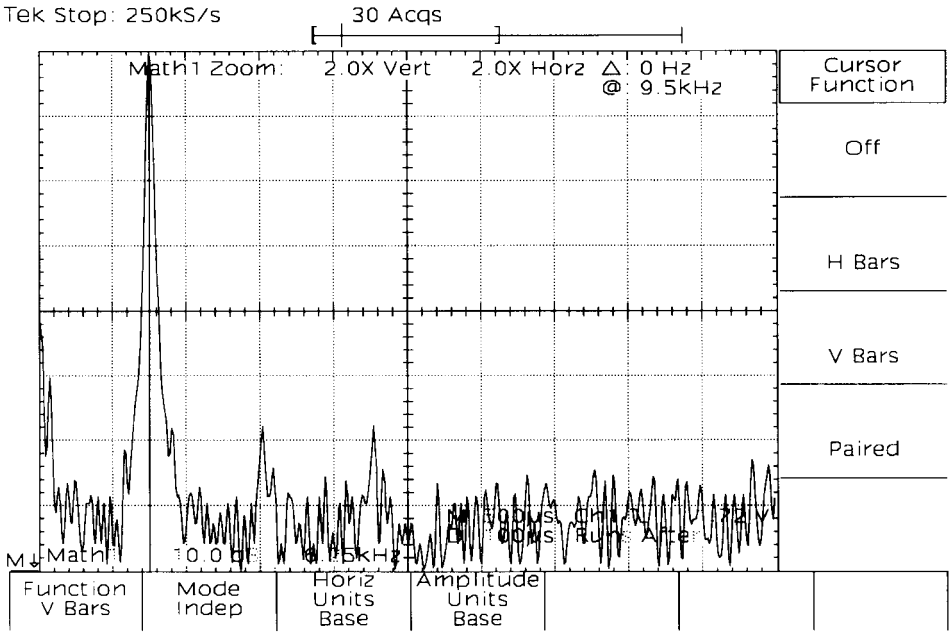


Fig. 9. Fourier-transformed IF-signal of the modified FMCW-system.

ulations are necessary. This quantization noise is caused by the necessary changes of the division ratio to produce the fractional value. Fig. 3 shows a calculated sequence of division ratios to produce a highly linear analog frequency ramp. The fractional value changes linearly with time.

A result in the time domain is shown in Fig. 4. It illustrates the deviation of the simulated frequency from the ideal ramp. It is important to realize the short settling time that the fractional loop needs to settle to the ramp. On the other hand, there is a low noise level present even when the VCO has settled. This is due to the remaining quantization noise after filtering the output signal of the phase-frequency-discriminator (PFD) with a lowpass filter. The noise level is not critical since it is in the same order as the normal phase noise present in every PLL. The simulation considers a loop filter with a Butterworth lowpass filter of the order ten aiming at the suppression of the quantization noise at higher frequencies. Its cutoff frequency is $f_{\mathrm{ref}}/10$.

## IV. Measurements

Some measurements have been made on the modified FMCW-radar prototype system having the simplified block diagram seen in Fig. 1. The quality of the fractionally generated analog frequency ramp is tested indirectly by inspecting the spectrum of the IF-signal of the FMCW-system. This spectrum is calculated using a FFT-algorithm after performing an analog-to-digital conversion. The bandwidth $B$ of the ramp is 1.2 GHz, sweeping from 4.4 GHz up to

5.6 GHz. The VCO used in this setup is a standard VCO using a MA46H070 type varactor and two silicon bipolar transistors. A photo of this oscillator can be seen in Fig. 5. The tuning linearity of the free running oscillator is not very high so that the fractional loop has to perform all the linearization.

The ramp bandwidth was measured on a spectrum analyzer as can be seen in Fig. 6. The sweep time of the ramp is 13 ms. With the ramp time $T$ and the bandwidth $B$, the ramp slope is

$$\dot{f}_{\mathrm{rf}} = \frac{B}{T} = 92.31\ \mathrm{GHz/s}. \tag{3}$$

With the ramp slope $\dot{f}_{\mathrm{rf}}$ and the measured delay $\tau = 105$ ns of the coaxial delay line, the IF-frequency $f_{\mathrm{if}}$ of the FMCW-system is derived as

$$f_{\mathrm{if}} = \dot{f}_{\mathrm{rf}} \cdot \tau = 105\ \mathrm{ns} \cdot 92.31 \frac{\mathrm{GHz}}{\mathrm{s}} = 9.69\ \mathrm{kHz}. \tag{4}$$

The mechanical length of the coaxial delay line is 25 m. The basic functional check of the fractional logic can be done with a fixed output frequency. The static output frequency can be measured directly with a spectrum analyzer. The result of this measurement is shown in Fig. 6. The fractional phase noise level is approximately $-101$ dBc/Hz at 5 kHz offset from the carrier. This fractional noise should be compared to the normal phase noise present in every PLL-circuit. The phase-frequency-comparator used here has a noise floor $W_{\mathrm{pfd}}$ of approximately $-155$ dBc/Hz at 5 MHz offset frequency. With a reference frequency $f_{\mathrm{ref}} = 12.5$ MHz at the phase-frequency-discriminator and a RF-frequency $f_{\mathrm{rf}}$ of 5 GHz, the phase noise level of the phase-locked VCO, $W_{\mathrm{rf}}$ for the nonfractional mode can be calculated as

$$\frac{W_{\mathrm{rf}}}{W_{\mathrm{pfd}}} = \left(\frac{f_{\mathrm{rf}}}{f_{\mathrm{ref}}}\right)^2 \Rightarrow W_{\mathrm{rf}} = -103\ \mathrm{dBc/Hz}. \tag{5}$$

Comparing this noise level with the measured noise level of the fractional divider loop (Fig. 6) shows that there is only a difference of approximately 2 dB. As the noise level of $-103$ dBc/Hz marks the absolute minimum in phase noise achievable with this phase-locked-loop, the measured noise level in case of the fractional mode is very close to the theoretically achievable value. This measurement is only a functional test of the fractional loop. The quality of the analog ramp is verified with the FMCW-system.

The IF-signal is measured using a digital storage oscilloscope for the analog-to-digital conversion. The measured IF-signal in the time domain is shown in Fig. 8. A remarkable fact is the very low amplitude modulation of the IF-signal due to a very flat frequency response in the microwave signal path. A more sensitive way to verify the high quality of the IF-signal is to examine it in the frequency domain. The spectrum of the IF-signal derived from a FFT is shown in Fig. 9. The narrow shape of the spectral peak proves the high ramp quality. The long delay of the coaxial cable makes the measurement quite sensitive to ramp nonlinearities. With such a long cable delay a very small ramp nonlinearity would widen the spectral peak significantly. Comparing the spectral peak to simulated peaks with different nonlinearities one can guess that the nonlinearity of this signal is below $10^{-4}$.

## V. Conclusion

A synthesizer generating highly linear analog frequency ramps has been presented. This synthesizer is a very useful component in every high precision radar system based on the FMCW principle. The achievable ramp linearity is better than $10^{-4}$ due to the great number of division ratios on the ramp. The accuracy of the frequencies is as good as the precision of the crystal reference oscillator itself, being in the range of $10^{-6}$. Measurements on a prototype circuit confirm the good ramp linearity of the synthesizer, which has been optimized considering the results of many simulations.

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