Issues in "Ahuja" Frequency Compensation Technique

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***Abstract* — This paper provides accurate analysis for the so-called "Ahuja" frequency compensation technique explaining why it performs poorly in certain cases. Analyses for two circuit variations are provided. From the understanding gained of the analyses, ways to improve the performance are looked into and finally the improvements claimed are verified by calculations and simulation results.**

***Index Terms* — Frequency compensation, integrated operational amplifiers, Miller compensation, Cascode compensation, Ahuja compensation, poles and zeros, frequency stability.**

I. Introduction

Miller compensation has been used extensively in the frequency compensation of integrated operational amplifiers and related circuits since the introduction of µA741 by Fairchild in 1968. An alternative form of compensation was proposed by R. Read and J. Wieser as early as in 1982 [1][2]. Nevertheless, it took some time for it to be accepted by the industry and the academia and as several of its benefits over the Miller compensation became slowly apparent, it quietly secured its place as an important alternative for on-chip frequency compensation. Although the authors of [1] named it "Cascode" compensation, it is widely known today as "Ahuja" compensation after the author of [2] who provided the very first analysis, implementation and measurement data.

The benefits of "Ahuja" compensation over Miller compensation are several such as better PSRR [1][2], higher unity-gain bandwidth using smaller compensation capacitor [2] and ability to cope better with heavy capacitive [3] and resistive [4] loads. One of the objectives of this paper is to highlight that despite the improvements, the technique is associated with a problem: clean Miller-like compensation may be difficult to achieve sometimes. The other objectives are to show why such difficulties are faced and look into possible ways to overcome them.

II. Review of the "Ahuja" Compensation Technique

A single-supply adaptation of the implementation in [2] and a more practical as well as popular version are shown in Figs. 1 and 2 respectively. Devices with subscripts A and B are identical unless indicated. There are a few essential differences between the two. Firstly, the circuit in Fig. 2 can provide higher DC gain than that in Fig. 1. Secondly, the open-loop transfer functions of the two do not have exactly the same form. This is because, in Fig. 1, the feedback compensation signal is added to the signal current from the first stage at the drain of compensation transistor MP_{3A}. However, in Fig. 2, this addition is done at the source of compensation transistor MN_{3A}. It will be shown later that expression wise the zeros of the two circuits are different though the poles are the same.

In [2], the transconductance g_{m3} of the compensation transistor was assumed to be infinite. The transfer function has two widely separated poles and no zeros under such an assumption. It was pointed out later [3] that, in practice, there would be a left half plane zero and a high-frequency pole too. The expressions for those were found in [4] assuming g_{m3} to be unrealistically high.

The simulated open-loop gain and phase responses of Figs. 1 and 2 are shown in Figs. 3 and 4. The small-signal parameters are given in section V, part *B*. As can be seen, these results do not look good around the unity-gain frequency and this cannot be explained adequately with the analyses presented in [2][3][4].

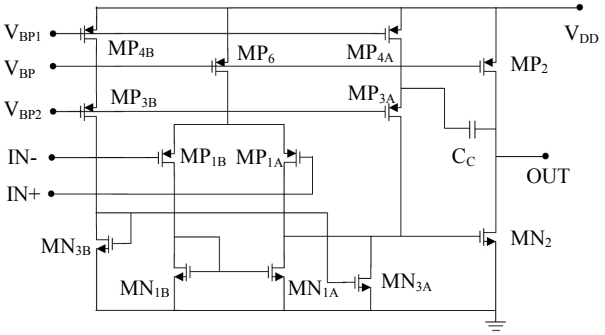

Fig. 1. Original version of "Ahuja" compensation circuit.

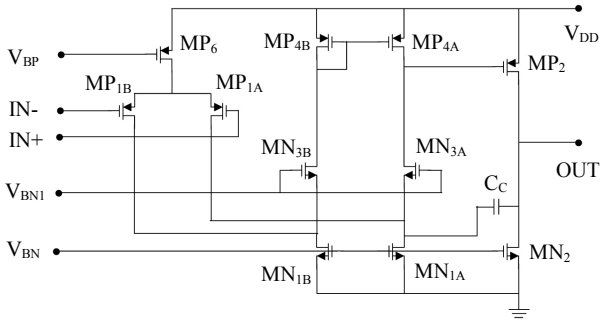

Fig. 2. Popular version of "Ahuja" compensation circuit.

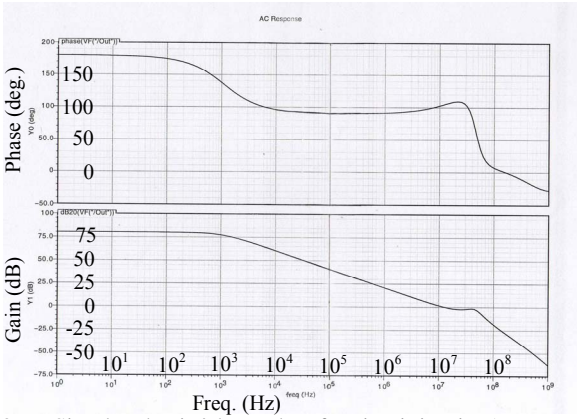

Fig. 3. Simulated gain/phase plots for circuit in Fig. 1.

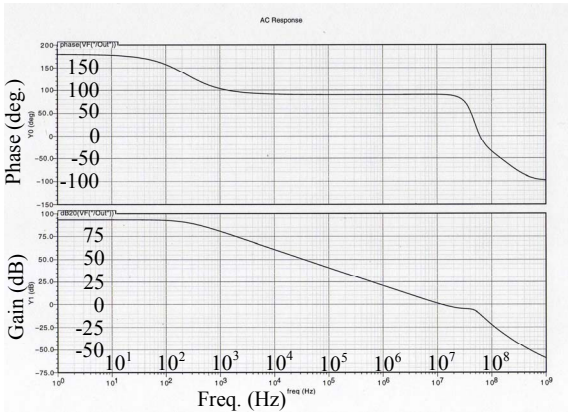

Fig. 4. Simulated gain/phase plots for circuit in Fig. 2.

III. Realistic Analysis of the "Ahuja" Compensation

A. Analysis

We shall assume C_1 and C_2 to be the net capacitances loading the output resistances r_1 and r_2 of the first and second stages with transconductances g_{m1} and g_{m2} respectively for the circuits shown in Figs. 1 and 2. The compensation transistor has a transconductance g_{m3} and a parasitic gate-source capacitance C_3. Small-signal analyses of the above circuits yield results (1) and (2) for the open-loop transfer functions $A_1(s)$ and $A_2(s)$ respectively after suitable approximations. A_0 and $\omega_0 = 2\pi f_0$ are the DC gain and the unity-gain bandwidth respectively.

$$A_1(s) = A_0 \frac{\left(\frac{s}{s_z}+1\right)}{\left(\frac{s}{s_{p1}}+1\right)\left[\frac{s^2}{\omega_n^2}+\left(\frac{2\zeta}{\omega_n}\right)s+1\right]} \qquad (1)$$

Where:

$$A_0 = g_{m1}g_{m2}r_1r_2,\ \ s_{p1} = -\frac{g_{m1}}{A_0C_C},\quad s_z = -\frac{g_{m3}}{\sigma C_C},$$

$$\omega_n = \sqrt{\frac{g_{m2}g_{m3}}{\rho C_1C_2}},\qquad \zeta = \frac{1}{2}\sqrt{\frac{C_1g_{m3}}{\rho C_2g_{m2}}}\left(1+\frac{C_2}{C_C}\right),$$

$$\sigma = 1+\frac{C_3}{C_C},\qquad \rho = 1+\frac{C_3}{C_C}+\frac{C_3}{C_2},\qquad \omega_0 = \frac{g_{m1}}{C_C}.$$

And:

$$A_2(s) = A_0 \frac{\left(\frac{s^2}{s_{z1,2}^2}-1\right)}{\left(\frac{s}{s_{p1}}+1\right)\left[\frac{s^2}{\omega_n^2}+\left(\frac{2\zeta}{\omega_n}\right)s+1\right]} \qquad (2)$$

Where:

$$s_{z1,2} = \pm\sqrt{\frac{g_{m2}g_{m3}}{C_1C_C}}$$

The rest of the parameters are the same as those in (1).

B. Discussion

As shown above, expressions of the low-frequency pole s_{p1} and the second-order high frequency pole-pair $s_{p2,3}$ with natural frequency $\omega_n = 2\pi f_n$ and damping factor ζ are the same for the circuits in Figs. 1 and 2. However, the latter circuit has a pair of L.H.P. and R.H.P. zeros $s_{z1,2}$ ($|s_{z1,2}| = \omega_{z1,2} = 2\pi f_{z1,2}$) as opposed to a single L.H.P. zero s_z ($|s_z| = \omega_z = 2\pi f_z$) for the former. The parameters σ, ρ are close to unity, modeling the effect of C_3.

For usual values of the circuit parameters, ζ is less than unity implying that the pair $s_{p2,3}$ is complex and not real as in [4]. The small valued capacitor C_1 can be seen to be present in the expressions of both ω_n and ζ. This helps ω_n to be sufficiently high but results in small values of ζ at the same time. Complex non-dominant poles with small damping factors are undesirable because those can cause loss in phase and/or gain margins, poor transient behavior and, in extreme cases, instability. If C_1, C_2 and g_{m2} are decided based on other factors then, for large values of ζ, g_{m3} needs to be high and/or C_C small. A value of ζ close to 0.5 will be adequate in most cases. It is easy to show that ω_n is expression-wise equal to magnitude of the non-dominant pole described in [2] when $\zeta = 0.5$.

The zero in the circuit of Fig. 1 is usually located just before the complex poles and the resulting magnitude curve shows pronounced peaking after the unity-gain crossover, sometimes popping over the unity-gain line again, if ω_n and ζ are small. The phase response also shows a rise because of the zero. The circuit in Fig. 2 has

zeros with mirror-symmetry on the left and right half planes at higher frequencies compared to the complex poles and, therefore, do not contribute much to the shapes of gain and phase characteristics near the unity-gain frequency. That, therefore, is decided mostly by the complex non-dominant poles.

IV. Transconductance of Compensation Transistor

A. Direct transconductance enhancement

As expected, (1) and (2) show that a large value of g_{m3} improves the compensation in an all-round manner by shifting the non-dominant poles and zeros to higher frequencies and increasing the damping factor of the complex poles. The simplest way to do this is to choose a large bias current and a large aspect ratio for the compensation transistor. This method is suitable for the circuit in Fig. 1. But it cannot be applied conveniently to the circuit in Fig. 2 because the bias current of the compensation transistor needs to be duplicated. In any case, this method will consume a lot of power if substantial increase in g_{m3} is required.

B. Active transconductance multiplication

Indirect enhancement of g_{m3}, as shown in Fig. 5, may be employed if large values of g_{m3} are required with reasonable amounts of power consumption. An auxiliary amplifier with gain A amplifies v_s, the small-signal voltage at the source of MP_3, and this appears at the latter's gate as $-Av_s$. The small-signal gate-source voltage of MP_3 is then $-(1+A)v_s$ and the resulting drain current i_d is $-(1+A)g_{m3}v_s$. Thus, g_{m3} appears to be multiplied by a factor (1+A). There is something more that we need to consider. The increase in gate-source voltage of MP_3 by a factor (1+A) increases the current through C_3 and the effect, therefore, is equivalent to a magnification of C_3 by the same factor. Consequently, σ and ρ increase adversely affecting the increase in ω_z, ω_n and ζ but not that of $\omega_{z1,2}$, according to (1) and (2). However, this effect is noticeable only for large values of C_3 and/or A.

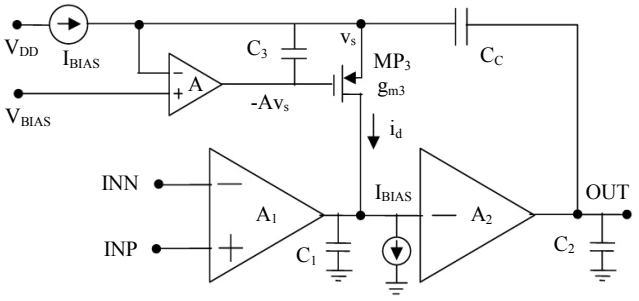

Fig. 5. Concept of active transconductance multiplication.

C. Practical considerations

We shall look into the effects of bandwidth limitation of the auxiliary amplifier in this subsection. We assume that the amplifier has a single pole at frequency ω_p for this purpose. Then the second-order factor in the denominator of either (1) or (2) modifies to a third-order one. For all the roots of this modified denominator to be in the left half plane one can show, applying Routh-Hurwitz criterion, the following should hold:

$$\omega_p > \left(\frac{g_{m2}}{C_a}\right) \quad \text{where} \quad C_a = C_1\left(1+\frac{C_2}{C_C}\right) \tag{3}$$

It can be noted that g_{m2}/C_a is the magnitude of the non-dominant pole as given in [2]. According to (3), the –3-dB bandwidth of the g_{m3} amplifier must be larger than that. Otherwise, the complex pole-pair of the modified open-loop transfer function could be located in the right half plane. It can be shown that the same restriction applies to the closed-loop transfer function too. Thus (3) imposes an additional requirement for stability with active g_{m3} multiplication. It is clear now that the auxiliary amplifier needs to be a wide-band one indeed.

V. Experiments, Results and Discussion

A. Circuit modifications for improvement

For the circuit in Fig. 1, the *m*-multipliers of MP_{4A}, MP_{3A} and MN_{3A} were increased to M times those of MP_{4B}, MP_{3B} and MN_{3B} respectively. This, in effect, multiplied the transconductance g_{m3} of MP_{3A} by a factor M. For the circuit in Fig. 2, the transconductance g_{m3} of MN_{3A} was multiplied using an auxiliary amplifier formed by MN_{5A} with transconductance g_{m5} and identical load resistors R_{AA} and R_{AB} as shown in Fig. 6. The bias current supplied by MP_3 split equally between MN_{5A} and MN_{5B} because of symmetry in the circuits around them. In this case, one can work out $M = 2(1+g_{m5}R_A)$, where R_A stands for the value of any one of the resistors.

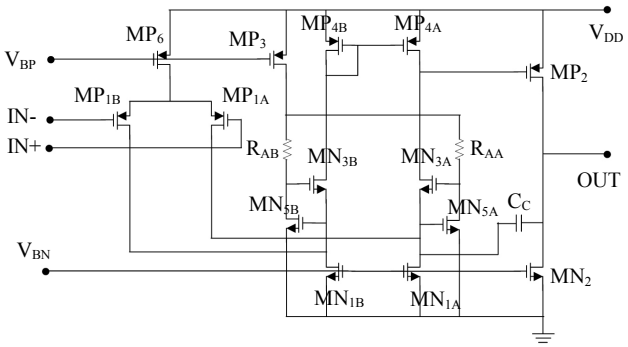

Fig. 6. Active transconductance multiplication for Fig. 2.

B. Experimental results and discussion

The circuits in Figs. 1, 2 and 6 were designed using the 3-V transistors of UMC 65-nm CMOS process. The circuit parameters for Fig. 1 were: g_{m1} = 70.36µS, g_{m2} = 766.88µS, g_{m3} = 124.33µS, C_1 = 0.11pF, C_2 = 10pF, C_3 = 0.007pF and C_C = 1.0pF. Those for Fig. 2 were: g_{m1} = 70.41µS, g_{m2} = 717.27µS, g_{m3} = 140.65µS, C_1 = 0.23pF, C_2 = 5pF, C_3 = 0.002pF and C_C = 1.0pF. For Fig. 6, g_{m5} = 137.30µS and R_A = 10kΩ are to be added to the latter set.

Figs. 7 and 8 show the improvements over Figs. 3 and 4 respectively using the abovementioned modifications. The simulation results depicted in Figs. 3 and 7 are compiled and compared with the corresponding calculated values in Table I. Likewise, the results for Figs. 4 and 8 are summarized in Table II. While doing simulations, pole-zero analyses were conducted to find the high frequency poles and zeros. I_B in the tables is the total bias current fed to the compensation circuitry and auxiliary amplifiers. G_m and ϕ_m stand for gain and phase margins respectively.

TABLE I
RESULTS FOR CIRCUIT IN FIG. 1

Parameter	Normal g_{m3} (sim.)	Normal g_{m3} (cal.)	High g_{m3} (sim.)	High g_{m3} (cal.)
M	1.00		4.00	
I_B (µA)	10.00		40.00	
f_0 (MHz)	13.56	11.20	11.48	11.20
ϕ_m (Deg.)	105.80	-	87.60	-
G_m (dB)	20.51	-	31.14	-
f_z (MHz)	19.30	19.79	78.86	79.12
f_n (MHz)	46.21	46.65	92.91	93.30
ζ	0.25	0.23	0.48	0.47

TABLE II
RESULTS FOR CIRCUITS IN FIG. 2 AND FIG. 6

Parameter	Fig. 2 (sim.)	Fig. 2 (cal.)	Fig. 6 (sim.)	Fig. 6 (cal.)
M	1.00		4.75	
I_B (µA)	20.00		40.00	
f_0 (MHz)	12.23	11.21	11.30	11.21
ϕ_m (Deg.)	89.18	-	79.29	-
G_m (dB)	9.43	-	16.82	-
$f_{z1,2}$ (MHz)	105.21	106.57	231.97	232.27
f_n (MHz)	48.48	47.66	104.50	103.88
ζ	0.27	0.28	0.60	0.62

The above results show that active transconductance multiplication is power wise more efficient compared to a direct enhancement of g_{m3} for large values of M. The –3-dB bandwidth of the auxiliary amplifier MN_{5A} in Fig. 6 exceeded 1.0GHz, satisfying (3). Unlike the one described in [5], this amplifier was direct coupled being configured as a regulated cascode with MN_{1A} and MN_{3A}.

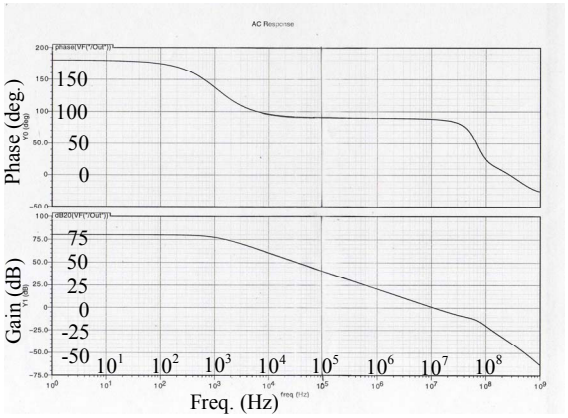

Fig. 7. Simulated gain/phase plots for Fig. 1 (high g_{m3}).

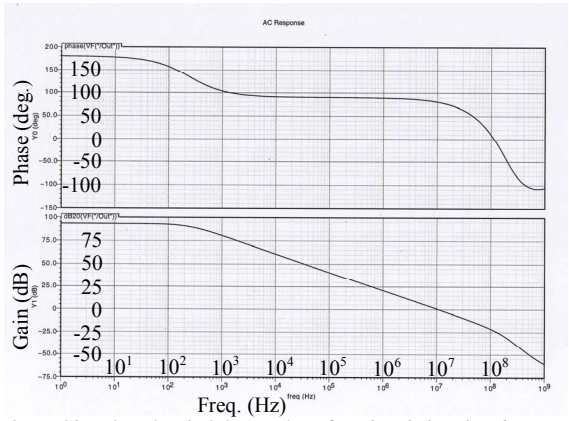

Fig. 8. Simulated gain/phase plots for circuit in Fig. 6.

VI. CONCLUSION

In this paper we have attempted to provide more insight into some aspects of "Ahuja" compensation applied to practical situations. We have also shown ways to improve the compensation at circuit level and verified the results with simulations and calculations. Good matches between simulated and calculated parameter values validate the accuracy of the analysis presented in the paper.

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