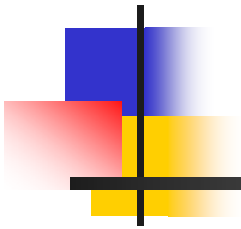

Design of DC-DC Converters

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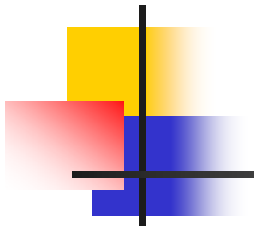
IEEE SSCS Dallas Chapter, October 2007



Design of DC-DC Converters

- DC-DC Converter Basics
  - Topology and Operation of DCDC Converters
  - Control Scheme for DCDC
- DC-DC Converter Design Techniques
  - System Level Modeling and Design
  - Building Block Design Considerations

DC-DC Converter Basics

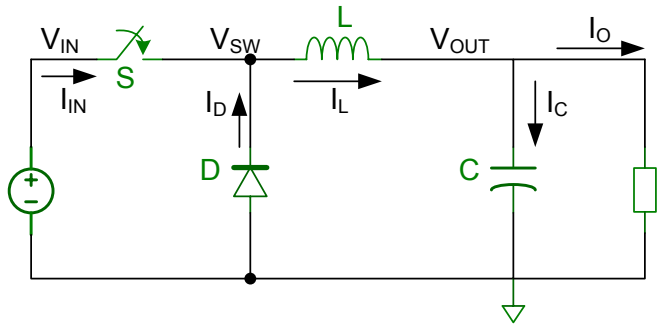
- DC-DC Converter is a Voltage Regulator
  - Use Switches, Inductor and Capacitor for Power Conversion
  - Switched Mode Operation
- Why DC-DC Converters?
  - High Efficiency
  - Can Step-Down, Step-up, or Both, or Invert
  - Can Achieve Higher Output Power

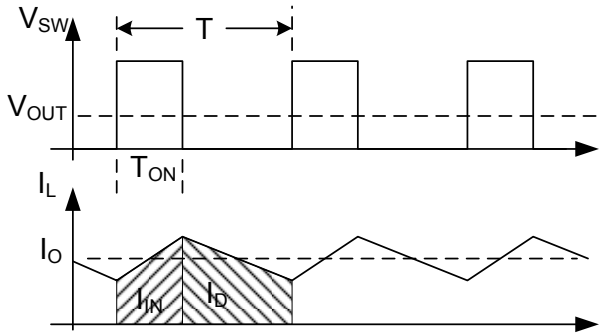
DC-DC Converter Basics

- Why not DC-DC Converters?
  - Complex Control Loop
  - Higher Noise and Output Ripple
  - More External Components
- Basic DC-DC Converter Topologies
  - Majority of DC-DC uses PWM Control Operated in CCM Mode

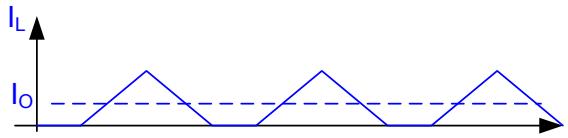
DC-DC Converter Basics

- Step-down (Buck)





Continuous Conduction Mode (CCM)



Discontinuous Conduction Mode (DCM)

Basic Relationships

- CCM Mode
  - I_L always supplies load
  - I_C small, independent of load

$$V_{OUT} = \frac{T_{ON}}{T} V_{IN} = D \cdot V_{IN}$$

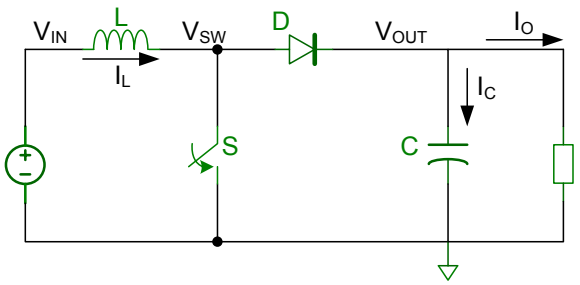
$$I_{IN} = D \cdot I_{OUT}$$

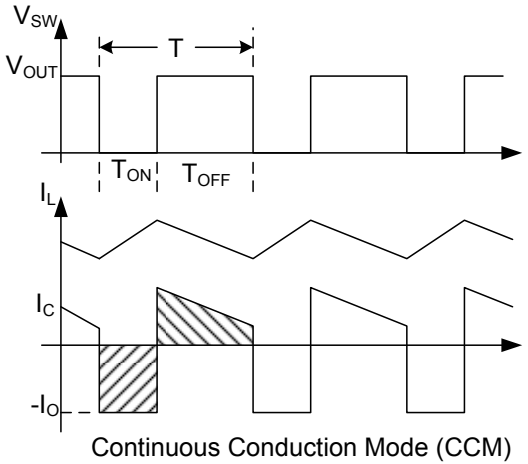
- DCM Mode

$$V_{OUT} = \frac{T_{ON}^{\ 2}}{T_{ON}^{\ 2} + \frac{2 I_O \cdot L \cdot T}{V_{IN}}} V_{IN}$$

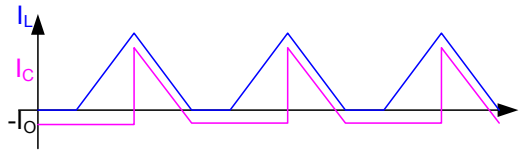
DC-DC Converter Basics

- Step-up (Boost)





Continuous Conduction Mode (CCM)



Discontinuous Conduction Mode (DCM)

Basic Relationships

- CCM Mode
  - I_L only supplies load during T_{OFF} period
  - I_C large and load dependent

$$V_{OUT} = \frac{T}{T_{OFF}} V_{IN} = \frac{1}{1-D} \cdot V_{IN}$$

$$I_{IN} = I_L = \frac{1}{1-D} \cdot I_{OUT}$$

- DCM Mode

$$V_{OUT} = \frac{T_{ON}^{\,2} + \frac{2I_O \cdot L \cdot T}{V_{IN}}}{T_{ON}^{\,2}} V_{IN}$$

Common Control Architectures

- Modulation Scheme
  - PFM (Pulse-Frequency-Modulation)
    - Pulse Skipping, Hysteretic, Constant-on etc.
    - High Efficiency at Light Load
    - Inherently Higher Output Ripple
    - Unmanaged Spectrum Noise
  - PWM (Pulse-Width-Modulation)
    - Fixed Frequency with Variable Duty Cycle
    - Better Transient Response (except Hysteretic?)
    - Most Widely Used

Common Control Architectures

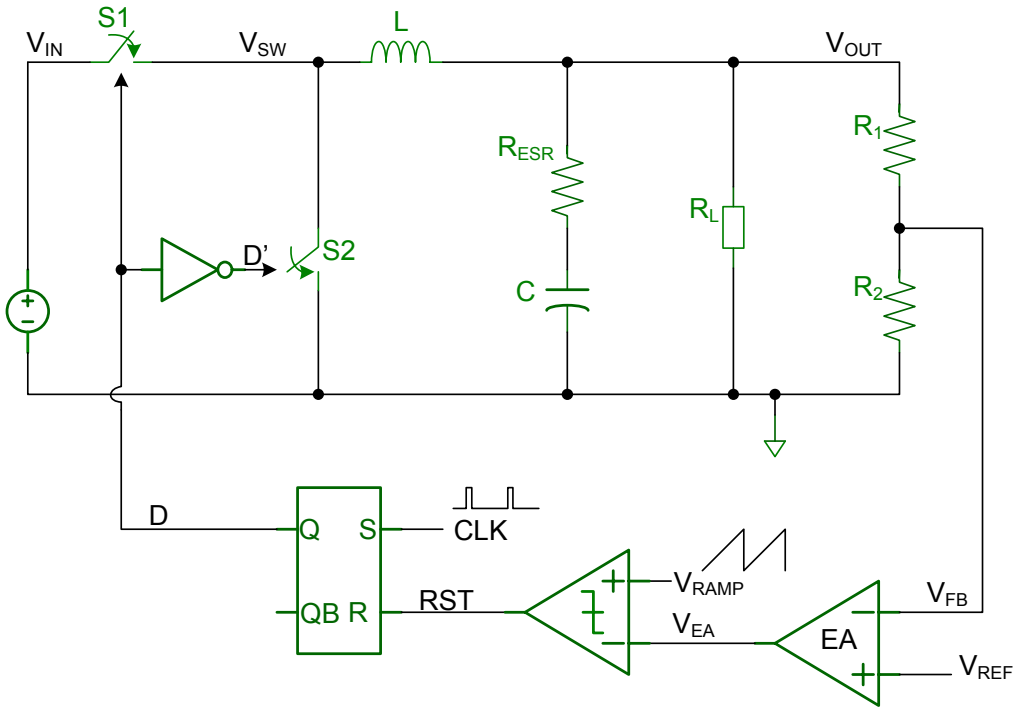
- Control Method (for PWM)
  - Voltage Mode
    - Regulates Output Voltage by Adjusting Duty Cycle
    - Constant Ramp for Modulation, Better Noise Immunity
    - LC Filter Contributes to Complex Conjugate Poles
    - Loop Has No Information on Inductor Current
    - Slower Response to Input Voltage Change
    - Bandwidth Varies with Input Voltage
    - Current Limit Done Separately

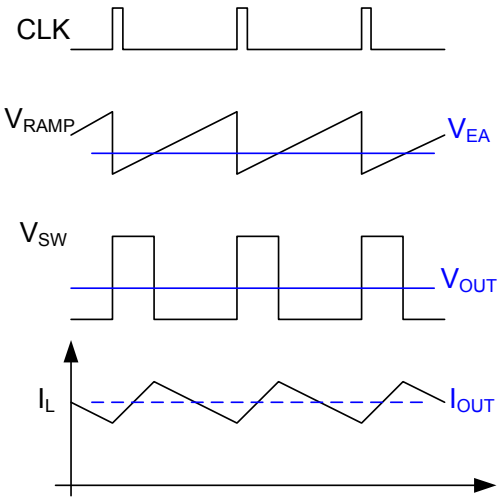
Common Control Architectures

- Current Mode
  - PCM (Peak-Current-Mode) Most Commonly Used
  - Regulates Inductor Current to Satisfy Load Demand and Maintain Output Voltage
  - Fast Current Loop makes Inductor to be a VCCS, eliminates Complex Conjugate Poles
  - Easy Built-in Cycle-to-Cycle Current Limit
  - Naturally Suitable for Multi-Phase Operation
  - Current Sense Susceptible to Noise
  - Need Slope Compensation for >50% Duty Cycle Operation

DC-DC Converter Design

- Examples of Common DC-DC Converters
  - Voltage Mode Buck





Voltage Mode Buck

Voltage Mode Buck Transfer Functions:

$$\frac{v_O}{d} \approx V_{IN} \frac{(1+sCR_{ESR})}{s^2LC + s(\frac{L}{R_L} + CR_{ESR}) + 1} = V_{IN} \frac{(1+sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}, Q = \frac{1}{\frac{1}{R_L}\sqrt{\frac{L}{C}} + R_{ESR}\sqrt{\frac{C}{L}}}$$

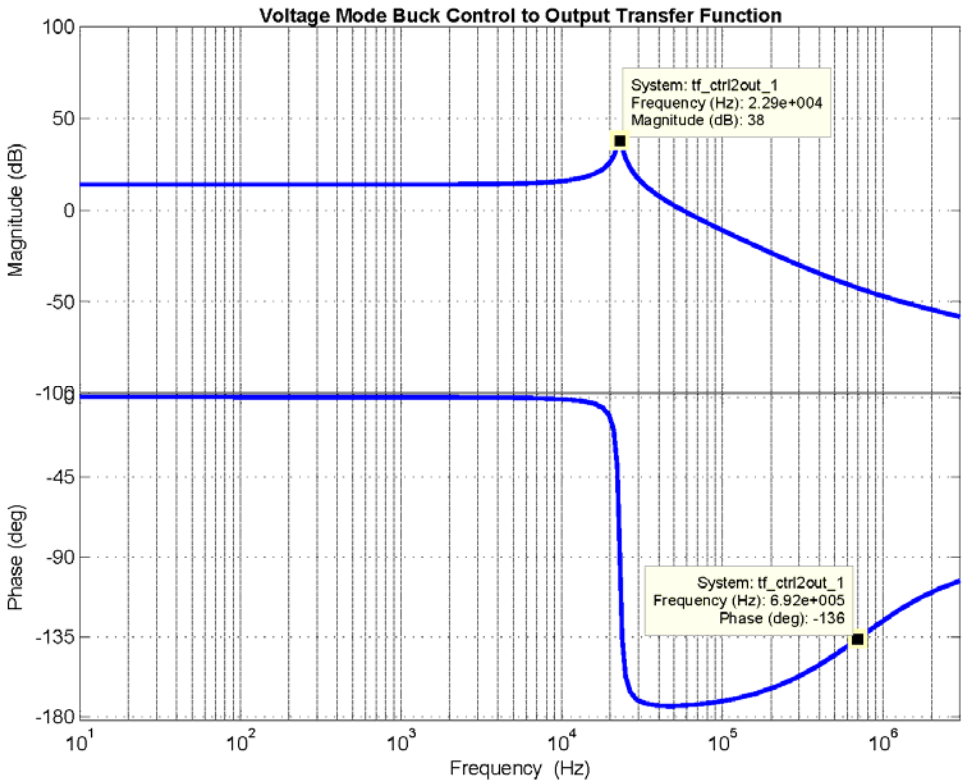
and

$$\frac{d}{v_{FB}} = \frac{1}{V_R} a(s)$$

where $a(s)$ is the transfer function of the error amplifier

Voltage Mode Buck

Control (Duty Cycle) to Output Transfer Function:

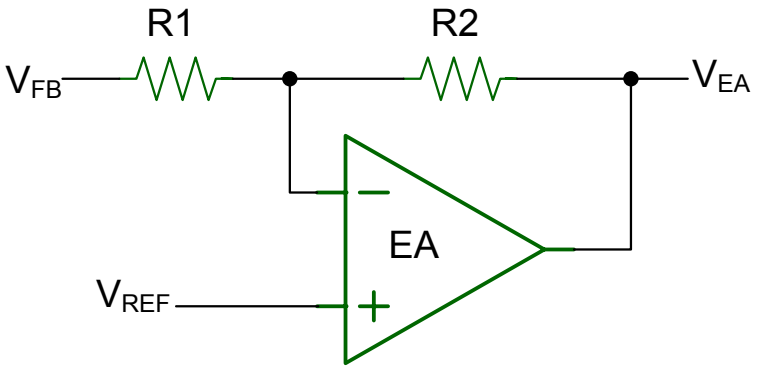


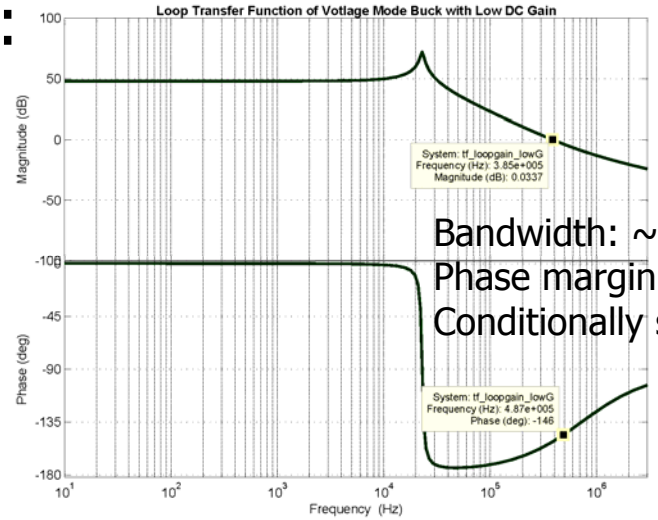
Example:
L=2.2uH, C=22uF,
R_{ESR}=10m Ohm
V_{IN}=5V, V_{OUT}=3.3V
R_L=10 Ohm
F_{SW}=1.5MHz
V_{RAMP}=100mV

ω_0 = 22.9kHz
Q = ~15.8
ω_Z = 700kHz

Voltage Mode Buck - Error Amp Ex. 1

Use low DC gain to set the bandwidth so that the phase margin is acceptable:



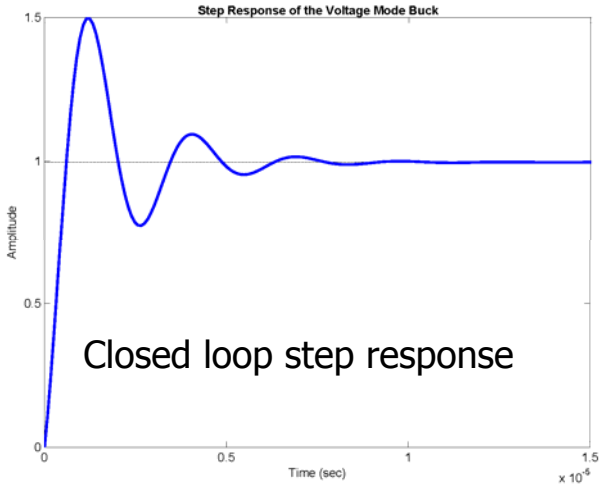


Bandwidth: ~400kHz
Phase margin: ~35°
Conditionally stable

$$V_{EA} = V_{REF} + \frac{R_2}{R_1}(V_{REF} - V_{FB})$$

$$v_{EA} = -\frac{R_2}{R_1} v_{FB}$$

$$LG = -\frac{R_2}{R_1} \cdot \frac{V_{IN}}{V_R} \frac{(1 + sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$



Closed loop step response

Example: R2=500k, R1=100k, V_R=100mV

Voltage Mode Buck - Error Amp Ex. 1

Some Improvements Can Be Added:

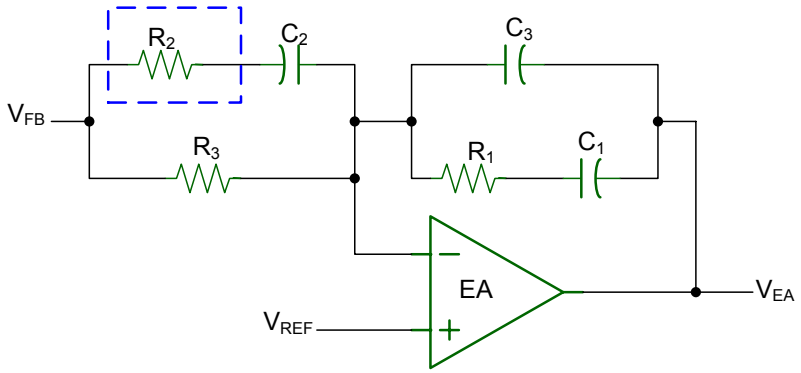
- Make V_{RAMP} proportional to V_{IN} -> Constant Bandwidth
- Add Feed-forward Cap on Feedback Resistor String -> better phase margin

Limitations of Low DC Gain:

- Loose Output Regulation
- Need some ESR to Stabilize the Loop
- Small Modulation Ramp Sensitive to Noise
- DC Offset if Output Cap has large ESR

Voltage Mode Buck - Error Amp Ex. 2

Use Type-III Compensation Network to Re-Shape Loop Frequency Response:



$$\frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{(1+sC_1R_1)[1+s(R_3+R_2)C_2]}{[1+sR_3(1+A_0)(C_1+C_3)](1+sR_2C_2)(1+sR_1C_3 \,||\, C_1)}$$

$$LG \approx -A_0 \frac{(1+sC_1R_1)(1+sR_3C_2)}{[1+sR_3A_0C_1](1+sR_2C_2)(1+sR_1C_3)} \cdot \frac{V_{IN}}{V_R} \frac{(1+sCR_{ESR})}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}}$$

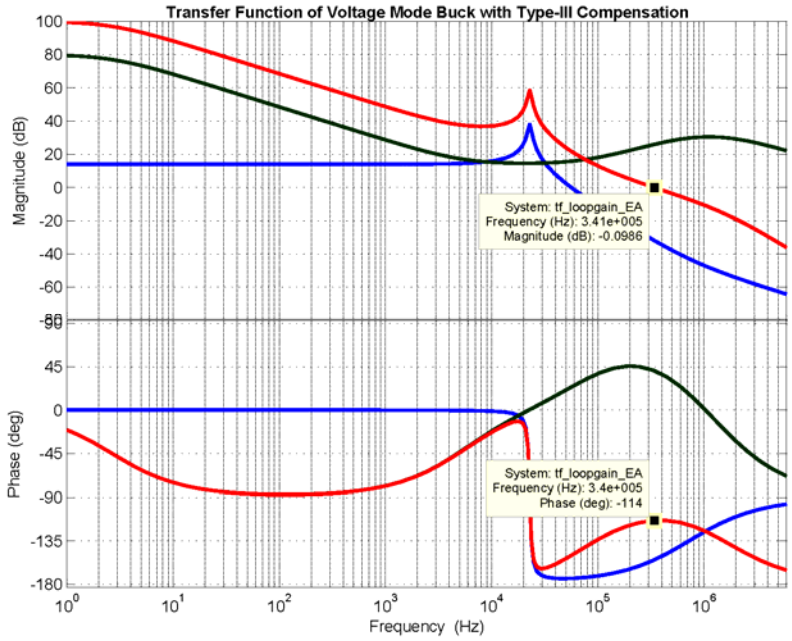
$$UGBW \approx R_1C_2 \cdot \frac{V_{IN}}{V_R} \cdot \frac{1}{LC}$$

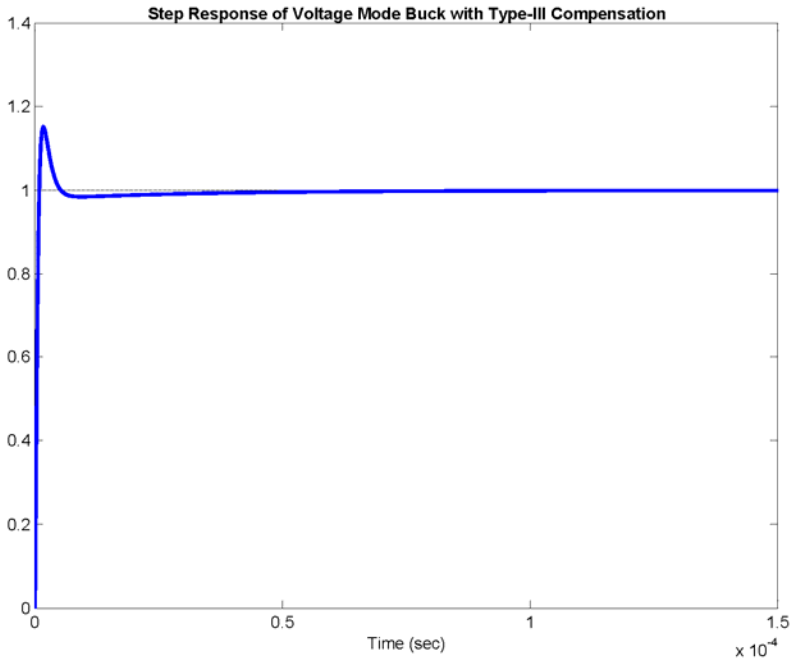
- High DC gain rolls off by dominant pole and, phase shift recovered by 1st zero before ω_0
- 2nd zero brings back phase shift above ω_0
- 2nd and 3rd pole attenuates high frequency noise

Example Design Steps:

1. Set R_1C_2=100uS for desired BW of ~300kHz
2. Set 1st zero to be 1/5 of ω_0: R_1=1Meg, C_1=30pF, ω_{z1}=5.3kHz
3. Set 2nd zero to be 4x of ω_0: C_2=10pF, R_3=200k, ω_{z2}=79.5kHz
4. mid-band DC gain of 5: R_3=200k
5. Set 2nd and 3rd pole to near switching frequency for high frequency noise attenuation: C_3=0.2pF, ω_{p2}=795kHz; R_2=10k, ω_{p3}=1.5MHz

Voltage Mode Buck - Error Amp Ex. 2





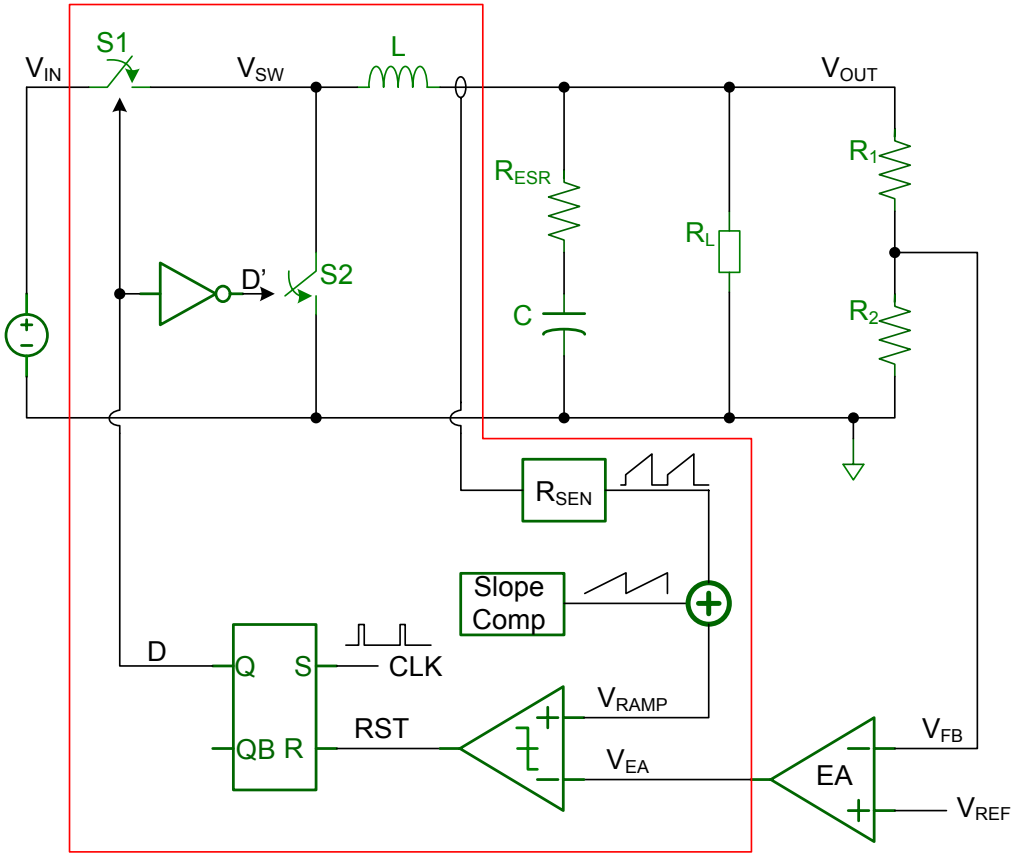
- Modulation ramp V_{RAMP} increased to 500mV for better noise immunity
- Blue: control to output transfer function
- Green: Type-III compensation error Amp transfer function
- Red: Complete loop transfer function bandwidth: ~340kHz, PM: ~65 degree

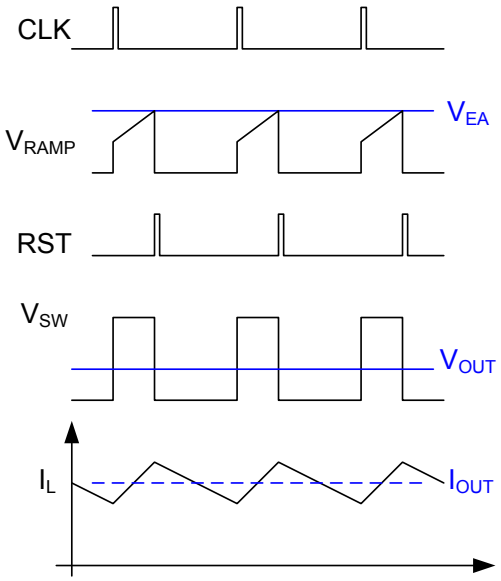
Compare to Error Amp Ex. 1:

- Step response has less overshoot due to better phase margin
- Settling is much slower due to 1st zero at low frequency

DC-DC Converter Design

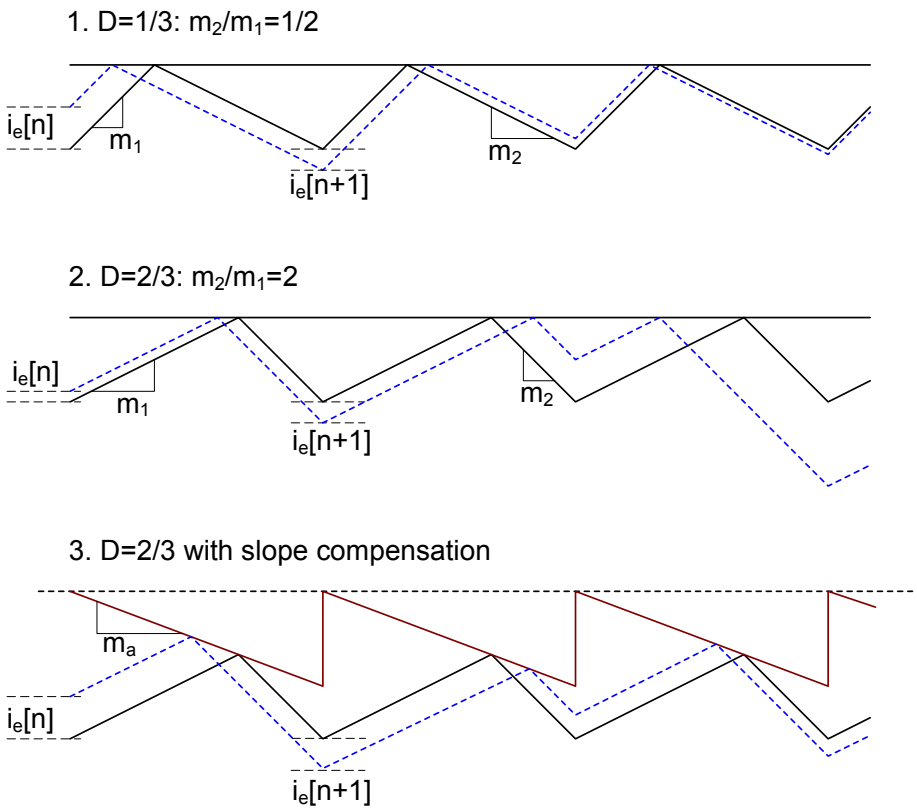
- Current Mode Buck (Peak Current Control)





Current Mode Buck

Inductor Current Instability for Duty Cycle > 50%:



$$i_e[n+1] = i_e[n] \cdot (-\frac{m_2}{m_1}) = i_e[0] \cdot \left(-\frac{m_2}{m_1}\right)^n$$

$\left|\frac{m_2}{m_1}\right| < 1$: i_e attenuates over cycles

$\left|\frac{m_2}{m_1}\right| > 1$: i_e grows over cycles

Requires Slope Compensation:

$$i_e[n+1] = i_e[n] \cdot (-\frac{m_2 - m_a}{m_1 + m_a})$$

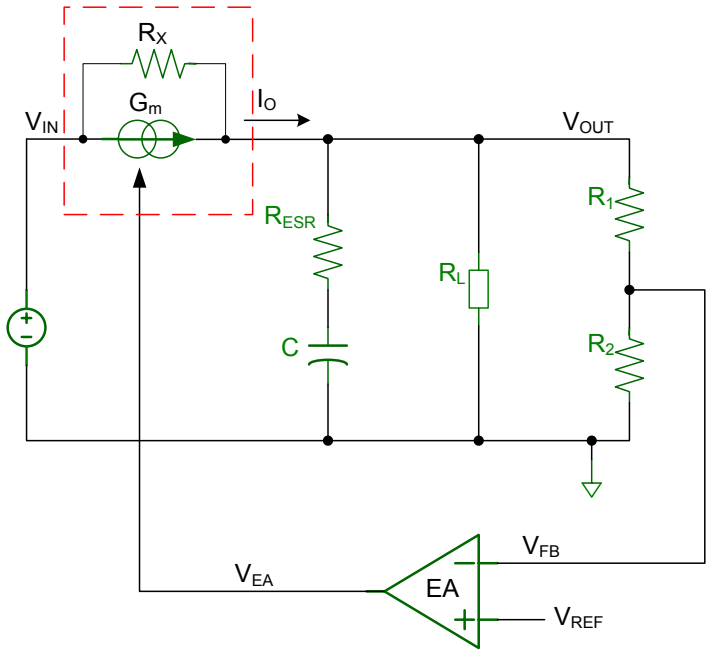
m_a is chosen so that $\left|\frac{m_2 - m_a}{m_1 + m_a}\right| < 1$

$\text{ex}: m_a = \frac{m_2}{2}$, guaranteed stable

$m_a = m_2$, 1 cycle correction

Current Mode Buck

- Fast current loop regulates inductor peak current, can be modeled as a VCCS with output impedance Rx
- Slower voltage loop provides reference for current loop



$$G_m = \frac{i_o}{v_{EA}} = \frac{1}{R_{SEN}} \frac{1}{1+\frac{R_L T_S}{L}[(1+\frac{m_a}{m_1})(1-D)-0.5]} = \frac{1}{R_{SEN}} \frac{1}{1+\frac{R_L}{R_X}}$$

where $R_X = \frac{L}{T_S[(1+\frac{m_a}{m_1})(1-D)-0.5]}$

Switched Operation results in delay and sampling effect :

$$H_e(s) = \frac{1+\alpha}{1+\alpha \cdot e^{-sT_S}} \frac{1-e^{-sT_S}}{sT_S} \qquad \text{where } \alpha = \frac{m_2 - m_a}{m_1 + m_a}$$

Complete VCCS transconductance including frequency response :

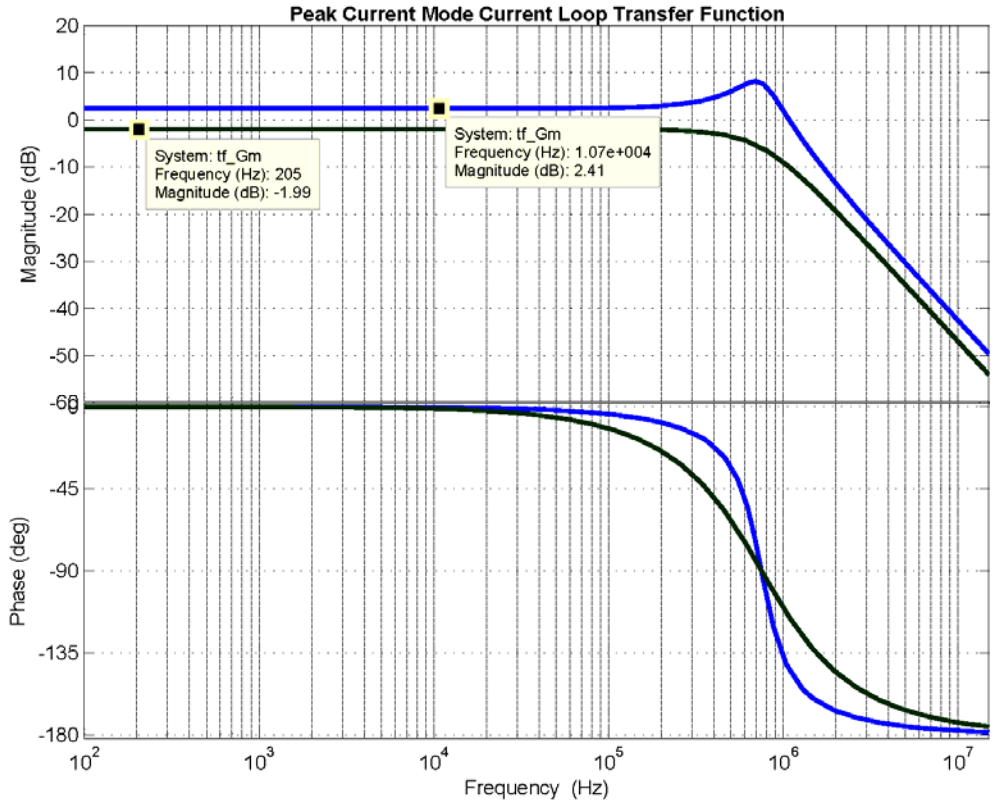
$$G_m(s) = \frac{1}{R_{SEN}} \frac{1}{1+\frac{R_L T_S}{L}[(1+\frac{m_a}{m_1})(1-D)-0.5]} \frac{1+\alpha}{1+\alpha \cdot e^{-sT_S}} \frac{1-e^{-sT_S}}{sT_S}$$

$$G_m(s) \approx \frac{1}{R_{SEN}} \frac{1}{1+\frac{R_L}{R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+\frac{s^2}{\omega_S^2}}$$

$$Q = \frac{2}{\pi} \frac{1}{(1+\frac{m_a}{m_1})(1-D)-0.5} = \frac{2}{\pi} \frac{1}{1-2D(1-\frac{m_a}{m_2})}$$

Current Mode Buck

Peak Current Mode Current Loop Transfer Function



Example:
L=2.2uH, V_{IN}=5V,
V_{OUT}=3.3V, R_L=10 Ohm
R_{SEN} = 0.5 Ohm
F_{SW} = 1.5MHz

Blue: $m_a=0.5*m_2$
R_X=19.4 Ohm
Gm=1.32 A/V
Q=1.87

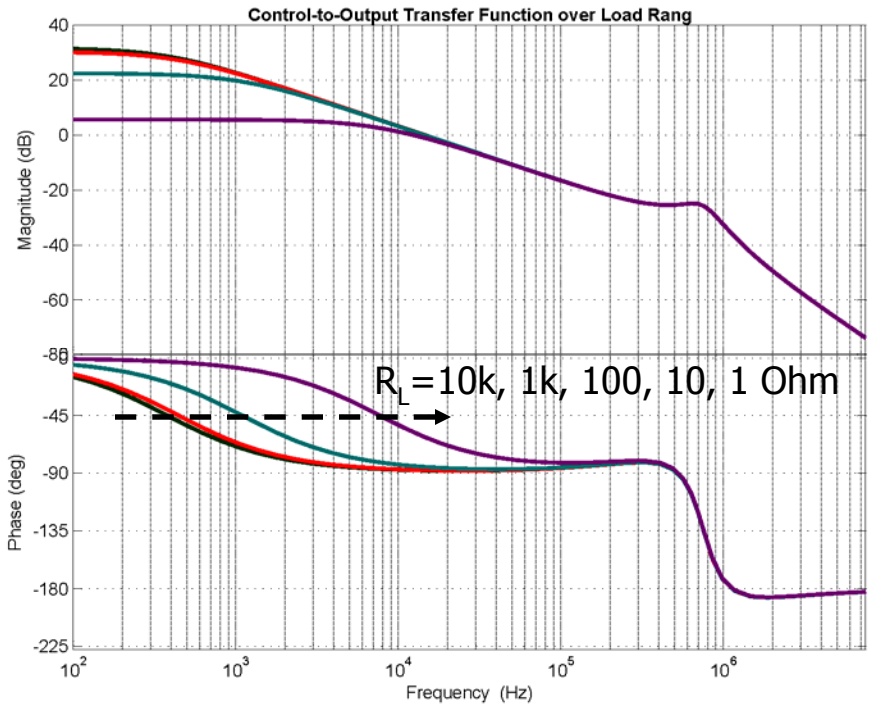
Green: $m_a=m_2$
R_X=6.6 Ohm
Gm=0.80 A/V
Q=0.64

Current Mode Buck

Control to Output Transfer Function

Equivalently Single-Pole System with Current Source Input

$$\frac{v_o}{v_{EA}} = G_m \cdot Z_O = \frac{R_L}{R_{SEN}} \frac{1}{1+\frac{R_L}{R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+(\frac{s}{\omega_S})^2} \frac{1+sCR_{ESR}}{[1+sC(R_L \parallel R_X)]}$$

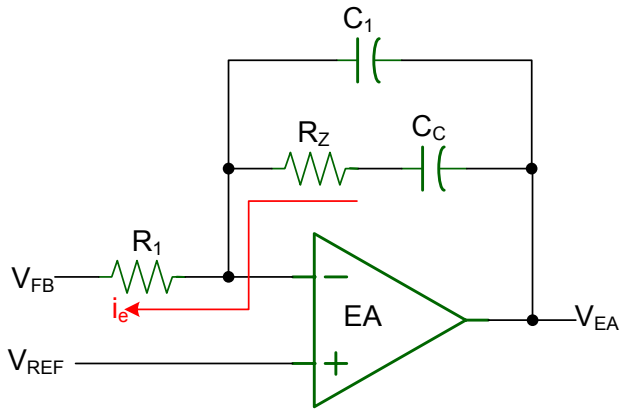


Example:
C=22uF, R_{ESR}=10m Ohm
R_{SEN} = 0.5 Ohm
F_{SW} = 1.5MHz
R_X=19.4 Ohm

R_L=10k, 1k, 100, 10, 1 Ohm

Current Mode Buck – Error Amp

Error Amplifier Example:



$$a(s) = \frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{1 + sC_C R_Z}{[1 + sC_C(r_o + g_m R_1 r_o + R_Z)](1 + sC_1 R_Z)}$$

$(C_C >> C_1)$

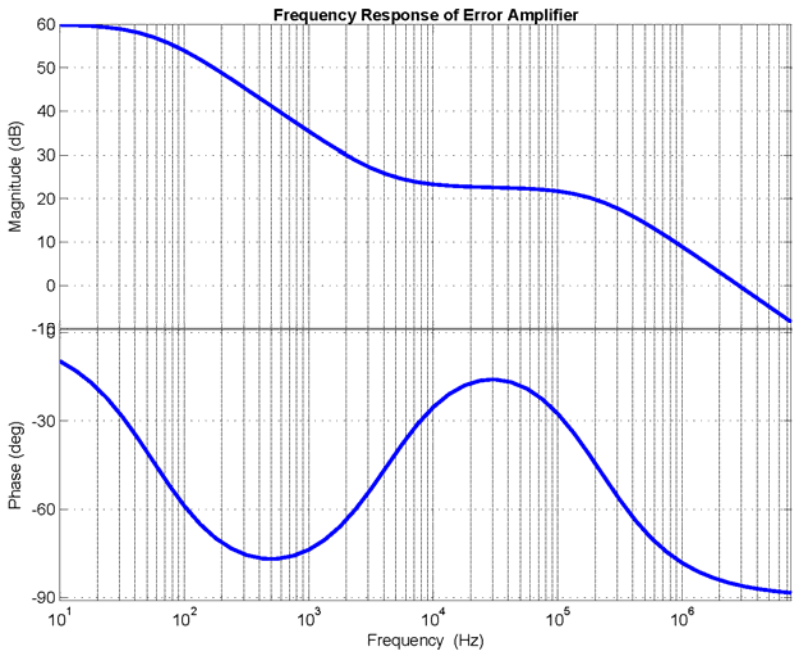
where : g_m is the transconductance of the error amp

r_o is the output impedance

- Bandwidth defined by R_1 and C_1
- Much smaller C_C, need large R_Z
- VFB more error during transient

Example:

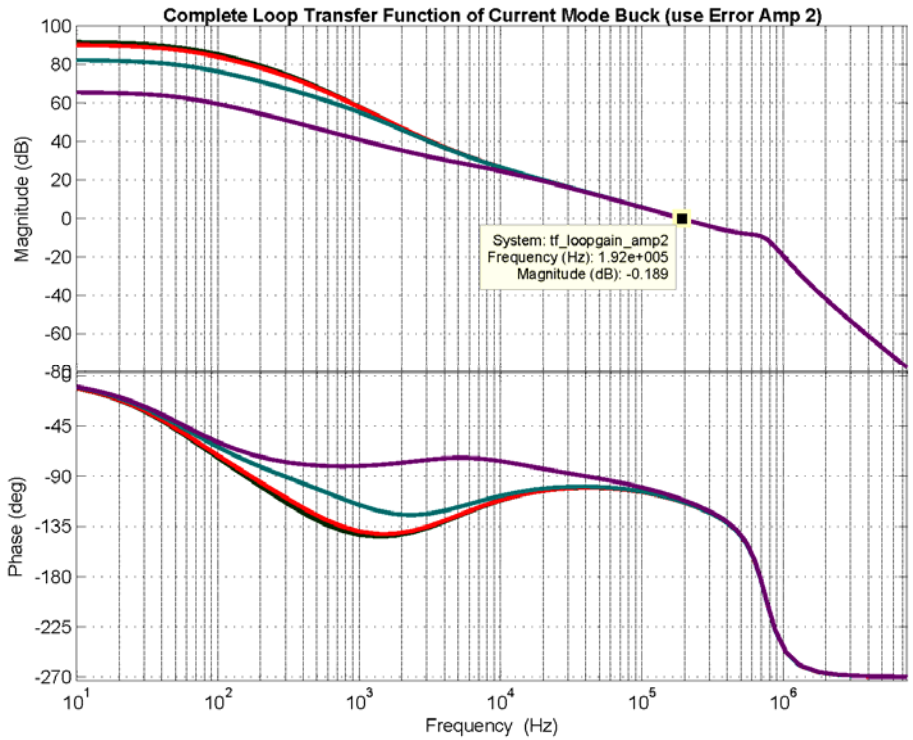
g_m=100uS, r_o=10MOhm,
R_1=100kOhm, C_C=25pF,
R_Z=1.5MOhm, C_1=0.3pF



Current Mode Buck – Error Amp

Complete Loop Transfer Function of Current Mode Buck:

$$LG = -\frac{R_L}{R_{SEN}} \frac{1}{1+\frac{R_L}{R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+(\frac{s}{\omega_S})^2} \cdot \frac{1+sCR_{ESR}}{[1+sC(R_L \parallel R_X)]} \cdot A_0 \frac{1+sC_C R_Z}{[1+sC_C(r_o+g_m r_o R_1+R_Z)](1+sC_1 R_Z)}$$



- 1st zero of error amp placed near output filter pole
- ESR zero and 2nd pole of error amp are placed out of loop bandwidth

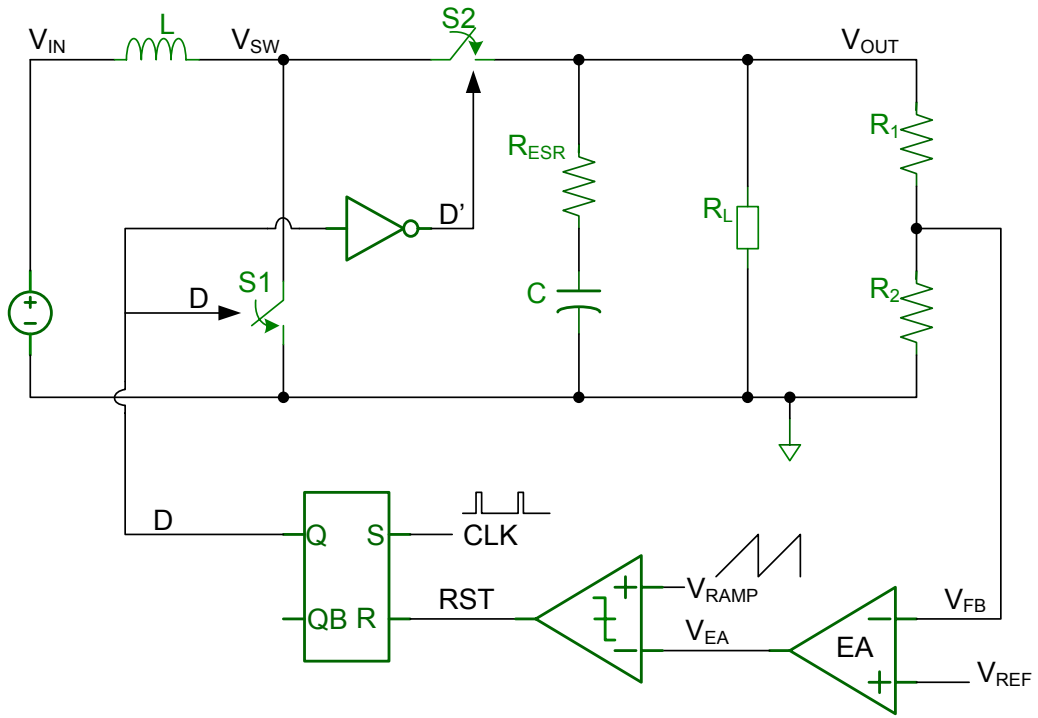
BW obtained by setting $|LG|=1$:

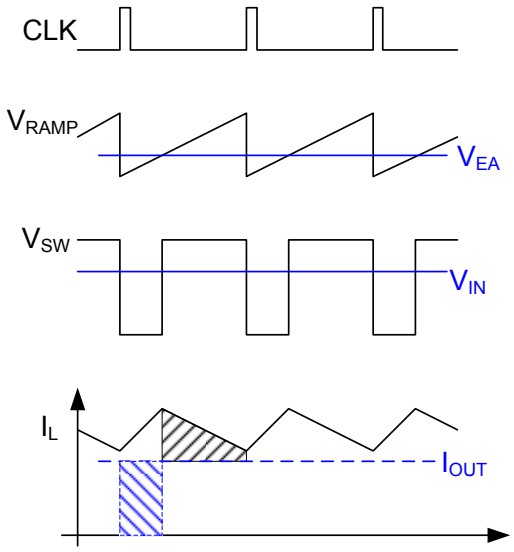
$$|LG(s_{BW})| \approx \frac{1}{R_{SEN}} \cdot \frac{1}{s_{BW}C} \cdot \frac{R_Z}{R_1} = 1$$

$$BW = \frac{1}{2\pi} \frac{R_Z}{R_1} \frac{1}{R_{SEN}C}$$

DC-DC Converter Design

- Voltage Mode Boost





Voltage Mode Boost

Voltage Mode Boost Transfer Functions:

$$\frac{v_O}{d} \approx \frac{V_{IN}}{(1-D)^2} \frac{(1+sCR_{ESR})(1-s\frac{L}{R_L(1-D)^2})}{s^2\frac{LC}{(1-D)^2}+s(\frac{L}{R_L(1-D)^2}+CR_{ESR})+1} = \frac{V_{IN}}{(1-D)^2} \frac{(1+\frac{s}{\omega_Z})(1-\frac{s}{\omega_{RHP}})}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0{}^2}}$$

$$\omega_0 = \frac{(1-D)}{\sqrt{LC}}, \quad \omega_{RHP} = \frac{R_L(1-D)^2}{L}, \quad Q = \frac{1}{\frac{1}{(1-D)R_L}\sqrt{\frac{L}{C}}+(1-D)R_{ESR}\sqrt{\frac{C}{L}}}$$

and

$$\frac{d}{v_{FB}} = \frac{1}{V_R}a(s)$$

where $a(s)$ is the transfer function of the error amplifier

Voltage Mode Boost - Effective Inductance

Perturbation from Output to Inductor Current:

$$L\frac{di_L}{dt} = V_{IN} - (1-D)V_O \Rightarrow i_L = \frac{(1-D)v_o}{sL}$$

and

$$I_O = \overline{I_L}(1-D) \Rightarrow i_o = i_L(1-D)$$

Impedance looking into the Inductor from Output:

$$Z_O = \frac{v_o}{i_o} = \frac{sL}{(1-D)^2}$$

Thus the Effective Inductance $L_{eff} = \frac{L}{(1-D)^2}$

This makes the ω_0 of the LC Filter to Move with D

Voltage Mode Boost - RHP Zero

Perturbation from Duty Cycle to Output Current:

$$I_O = \overline{I_L}(1-D) \Rightarrow i_o = i_L(1-D) - d \cdot \overline{I_L} = i_L(1-D) - d \cdot \frac{I_O}{1-D}$$

$$L\frac{di_L}{dt} = DV_{IN} + (1-D)(V_{IN} - V_O) \Rightarrow i_L \approx \frac{d \cdot V_O}{sL}$$

Right-Half-Plan Zero forms at frequency where:

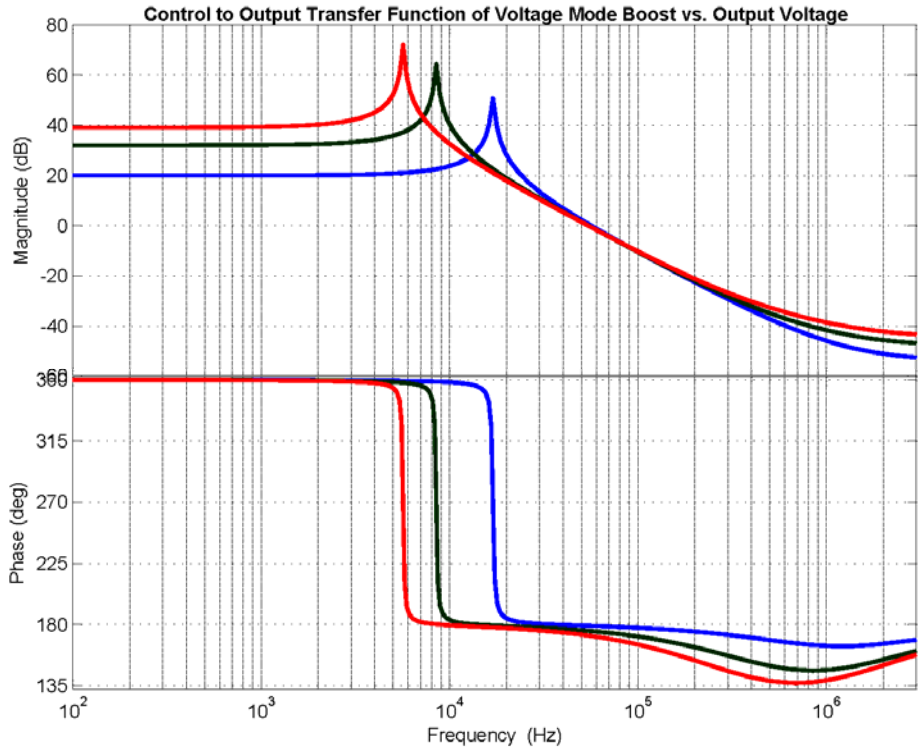
$$\left| \frac{d \cdot V_O}{j\omega_{RHP} L}(1-D) \right| = \left| d \cdot \frac{I_O}{1-D} \right|$$

$$\omega_{RHP} = \frac{R_L(1-D)^2}{L}$$

Right-Half-Plan Zero exists for both Voltage Mode and Current Mode Boost

Voltage Mode Boost

Control (Duty Cycle) to Output Transfer Function:

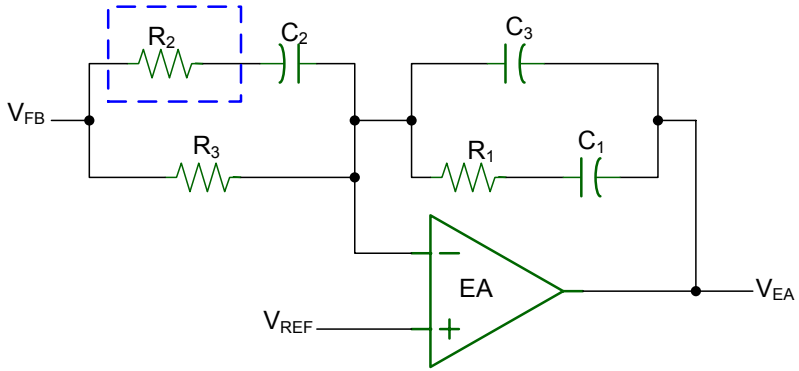


Example:
L=2.2uH, C=10uF,
R_{ESR}=10m Ohm,
V_{IN}=2.5V,
V_{OUT}=5V, 10V, 15V,
I_{OUT}=100mA
F_{SW}=1.5MHz

ω_0 and ω_{RHP} moves lower with increased duty cycle

Voltage Mode Boost – Type-III Error Amp

Usually Type-III Compensation Network is Required:



$$\frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{(1+sC_1R_1)[1+s(R_3+R_2)C_2]}{[1+sR_3(1+A_0)(C_1+C_3)](1+sR_2C_2)(1+sR_1C_3 \,||\, C_1)}$$

$$LG \approx -A_0 \frac{(1+sC_1R_1)(1+sR_3C_2)}{[1+sR_3A_0C_1](1+sR_2C_2)(1+sR_1C_3)} \cdot \frac{V_{IN}}{V_R(1-D)^2} \frac{(1+\frac{s}{\omega_Z})(1-\frac{s}{\omega_{RHP}})}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^{\,2}}}$$

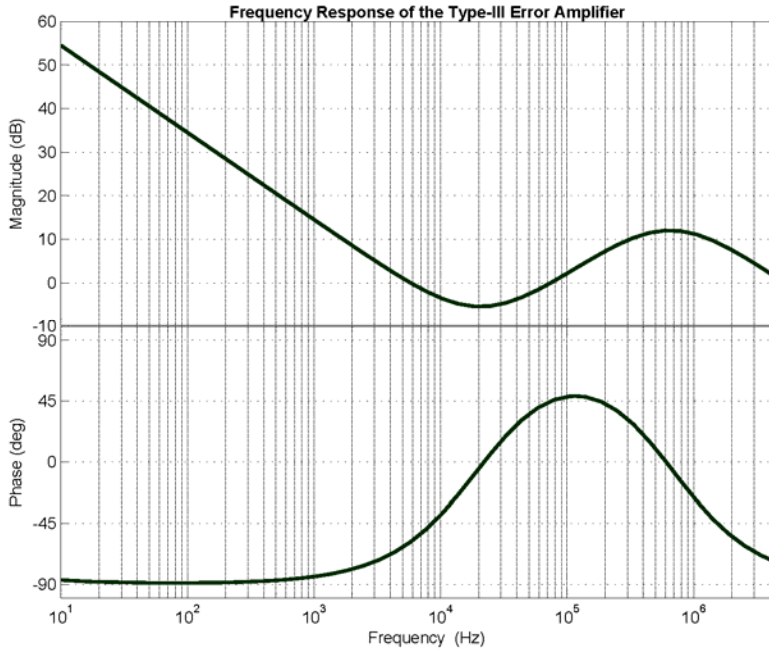
Set BW to be lower than ω_Z and ω_{RHP} :

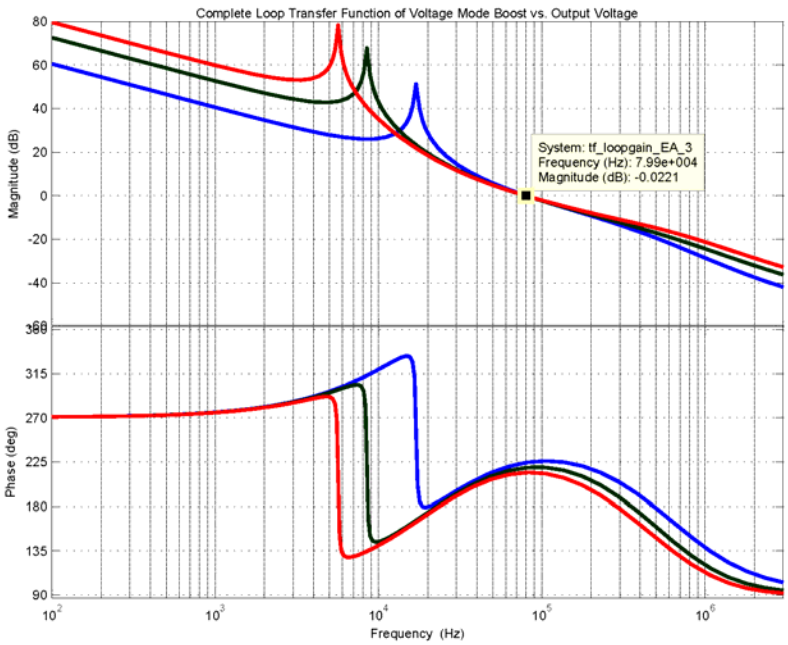
$$BW : R_1 \cdot C_2 \cdot \frac{V_{IN}}{V_R} \frac{1}{s_{BW}LC} = 1 \Rightarrow BW = \frac{1}{2\pi} \frac{R_1 \cdot C_2 \cdot \frac{V_{IN}}{V_R}}{LC}$$

Example Design Steps:

1. Estimate worst case ω_{RHP}=300kHz
2. Set BW<100k: R_1C_2<2.75µs
3. Set both zeros near ω_0: R_1=100k, C_1=100pF, R_3=300k, C_2=20pF, ω_{z1}=16.0kHz, ω_{z2}=26.5kHz
4. Bandwidth: f_{BW}= 80kHz
5. Mid-band DC gain of 1/3
6. Set 2nd and 3rd pole to beyond ω_{RHP} : R_2=10k, C_3=3pF ω_{p2}=530kHz, ω_{p3}=790kHz

Voltage Mode Boost – Type-III Error Amp



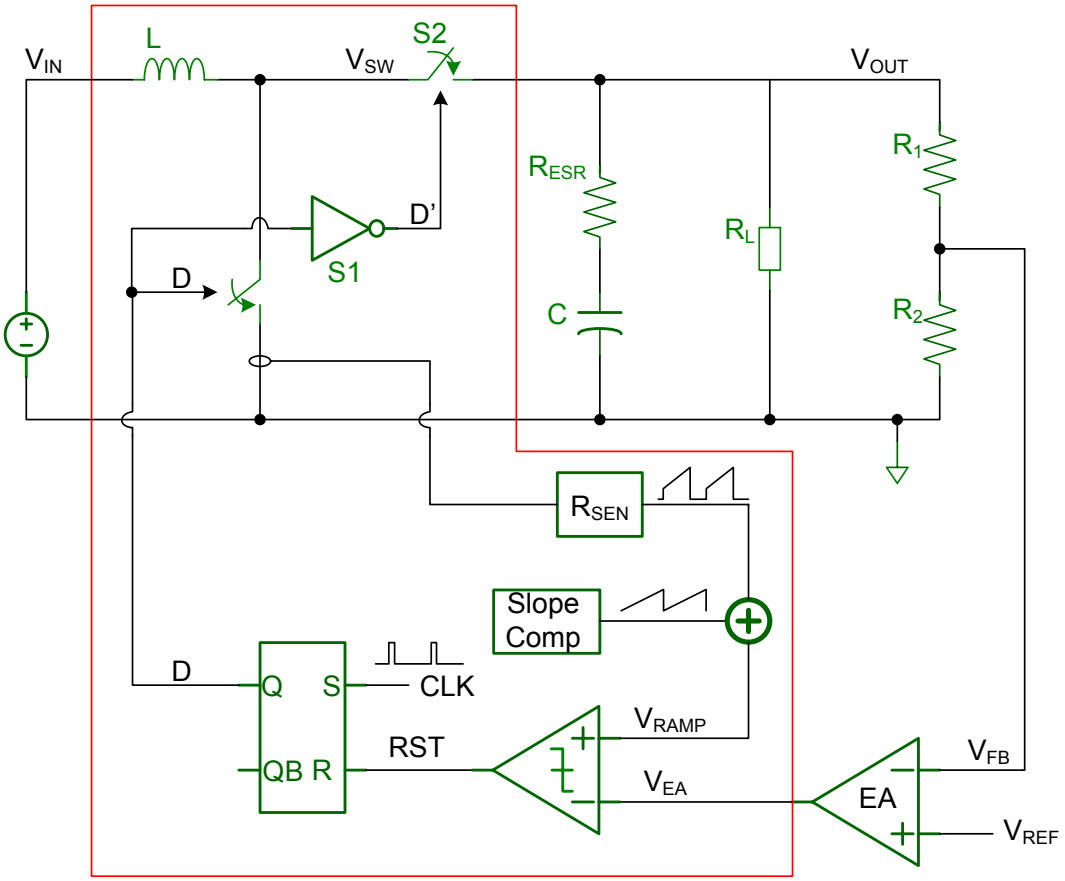


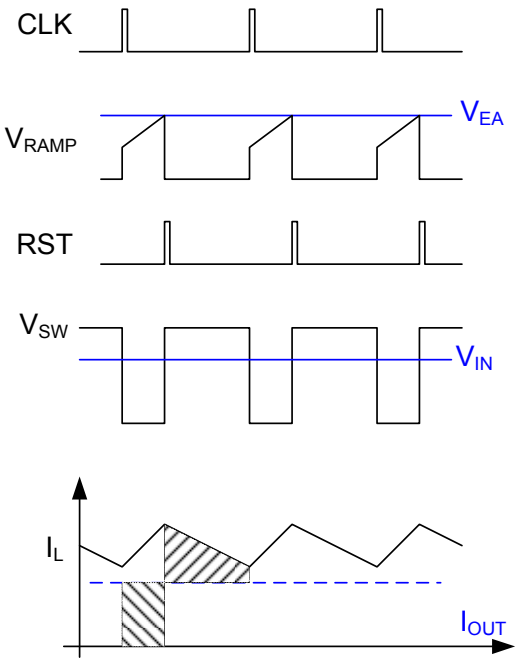
- Adjust C_1 to move 1st zero
- Adjust R_3 to move 2nd zero and mid-band gain
- 2nd pole and 3rd poles suppress high frequency noise

- Phase shift exceeds 180° at ω_0 -> conditionally stable
- Move 1st zero lower to improve phase shift -> much larger C_1

DC-DC Converter Design

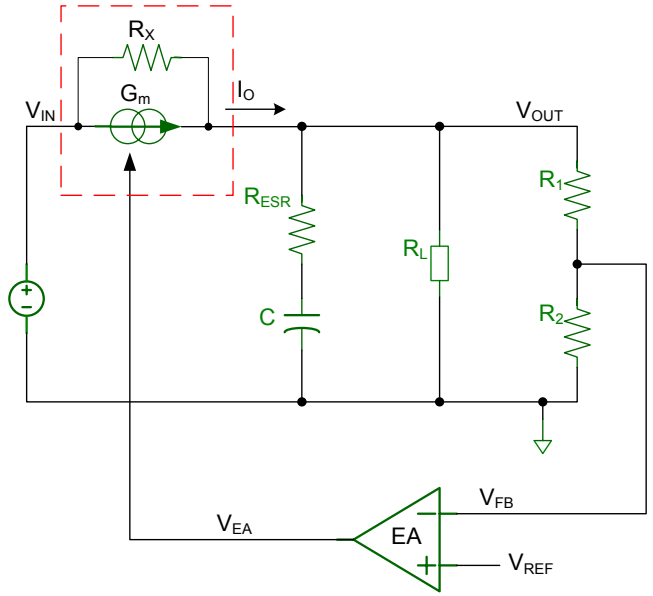
- Current Mode Boost





Current Mode Boost

Transfer Function of the Current Loop:



$$G_m = \frac{i_o}{v_{EA}} = \frac{1-D}{R_{SEN}} \frac{1}{1+\frac{R_L}{2R_X}}$$

where $R_X = \frac{1}{(1-D)^2}\left(\frac{L}{T_S[(1+\frac{m_a}{m_1})(1-D)-0.5]} \parallel \frac{2L}{DT_S}\right)$

Similar to Peak Current Mode Buck

Delay and sampling effect results in a 2 - pole system :

$$G_m(s) \approx \frac{1-D}{R_{SEN}} \frac{1}{1+\frac{R_L}{2R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+\frac{s^2}{\omega_S{}^2}}$$

$$\omega_S = \frac{\pi}{T_S}$$

$$Q = \frac{2}{\pi} \frac{1}{(1+\frac{m_a}{m_1})(1-D)-0.5} = \frac{2}{\pi} \frac{1}{1-2D(1-\frac{m_a}{m_2})}$$

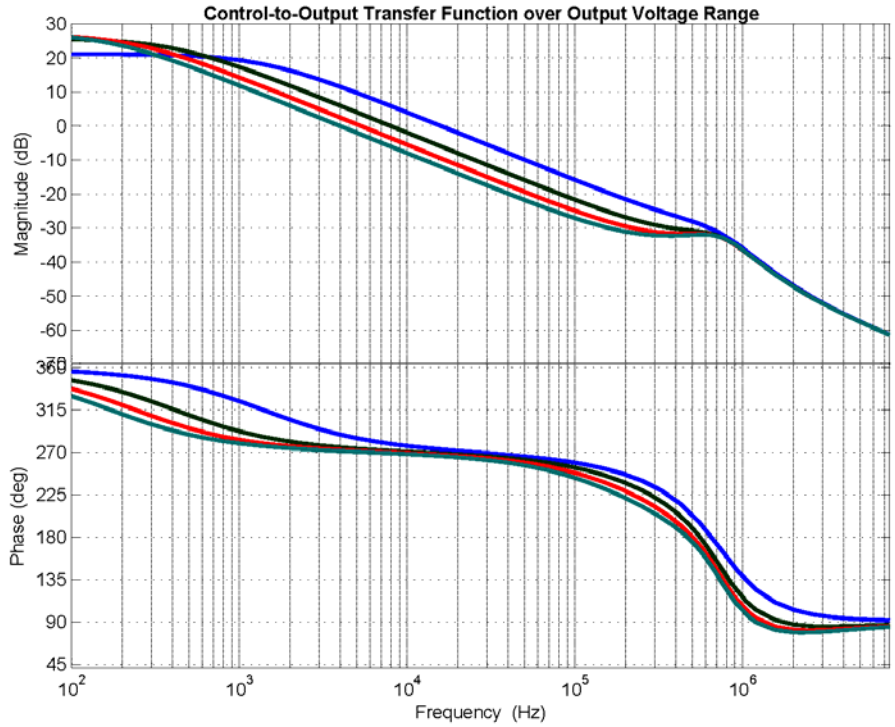
Current Mode Boost

Control to Output Transfer Function:

$$\frac{v_o}{v_{EA}} = G_m(s)\cdot Z_O = \frac{(1-D)R_L}{2R_{SEN}} \frac{1}{1+\frac{R_L}{2R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+(\frac{s}{\omega_S})^2} \cdot \frac{(1+sCR_{ESR})(1-\frac{s}{\omega_{ZRHP}})}{[1+sC(\frac{R_L}{2}\,\|\,R_X)]}$$

$$\omega_{RHP} = \frac{R_L(1-D)^2}{L}$$

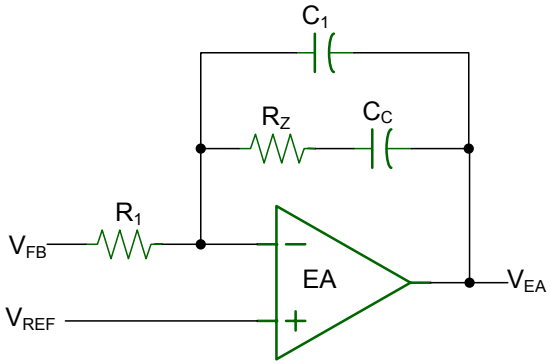
Example:
V_{IN}=2.5V
V_{OUT}= 5V, 10V, 15V, 20V
L=2.2uH, C=10uF
R_{ESR}=10m Ohm
I_{OUT} = 100mA
R_{SEN} = 0.5 Ohm
F_{SW} = 1.5MHz



Current Mode Boost – Error Amp Ex.

Use the same error amp structure as on page 22:

The Complete Loop Transfer Function:



$$T(s) = -\frac{(1-D)R_L}{2R_{SEN}} \frac{1}{1+\frac{R_L}{2R_X}} \frac{1}{1+\frac{s}{Q\omega_S}+(\frac{s}{\omega_S})^2} \cdot \frac{(1+sCR_{ESR})(1-s\frac{s}{\omega_{ZRHP}})}{[1+sC(\frac{R_L}{2}\,\|\,R_X)]} \cdot A_0 \frac{1+sC_CR_Z}{[1+sC_C(r_o+g_mr_oR_1+R_Z)](1+sC_1R_Z)}$$

Generally Guideline:

- To ensure loop stability, the unity-gain bandwidth is set to be 3-5x lower than the worst case RHP zero
- The ESR zero and 2nd pole of the amplifier is placed higher than the RHP zero
- The current loop poles are usually much higher than RHP zero

Current Mode Boost – Error Amp Ex.

Loop Bandwidth can be estimated as:

$$BW = \frac{1}{2\pi}\frac{(1-D)}{R_{SEN}C}\cdot\frac{R_Z}{R_1} \le \frac{\omega_{RHP}}{3}$$ (RHP zero contributes $< 18°$ phase shift)

Since $\omega_{RHP} \propto R_L(1-D)^2 = R_L(\frac{V_{IN}}{V_O})^2 = \frac{V_{IN}^{\ 2}}{V_O \cdot I_O}$, $BW \propto (1-D)$

Bandwidth should be set at max. duty cycle and load

Example:

V_{IN}=2.5V, V_{OUT}=5V, I_O=500mA

L=2.2uH, C=10uF,

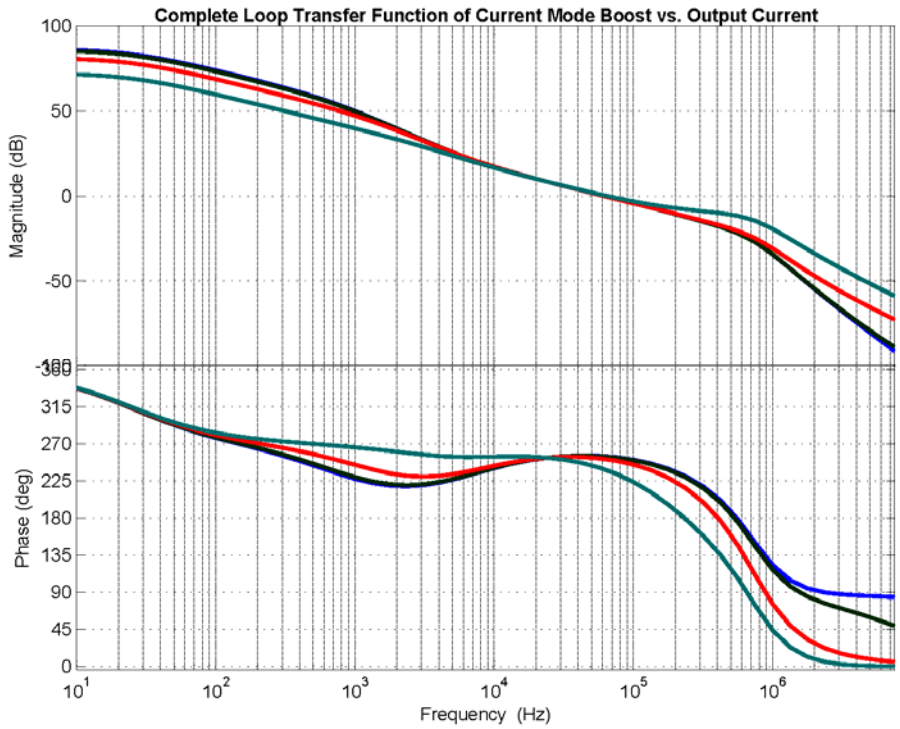
R_{SEN}=0.5 Ohm, R_Z=1M Ohm,

ω_{ZRHP}=181kHz, BW chosen to be ~60kHz

Calculate: R_1:~300k Ohm

Current Mode Boost

Complete Loop Transfer Function of Current Mode Boost Converter:



Error Amplifier Example:

R_1=250k, R_Z=1M

C_C=25pF, C_1=0.3pF

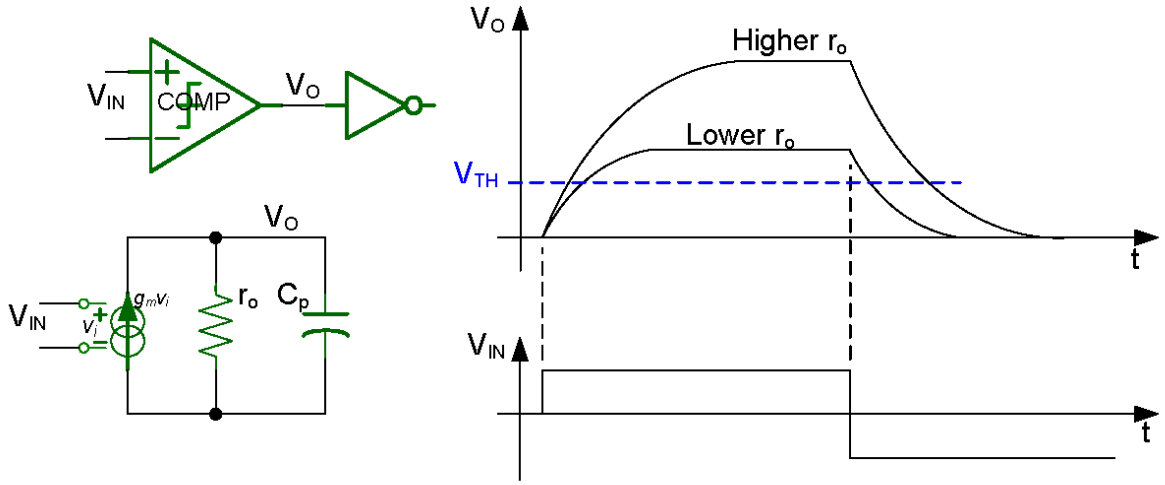
Output Current:

1mA, 10mA, 100mA, 500mA

Loop BW: ~60kHz

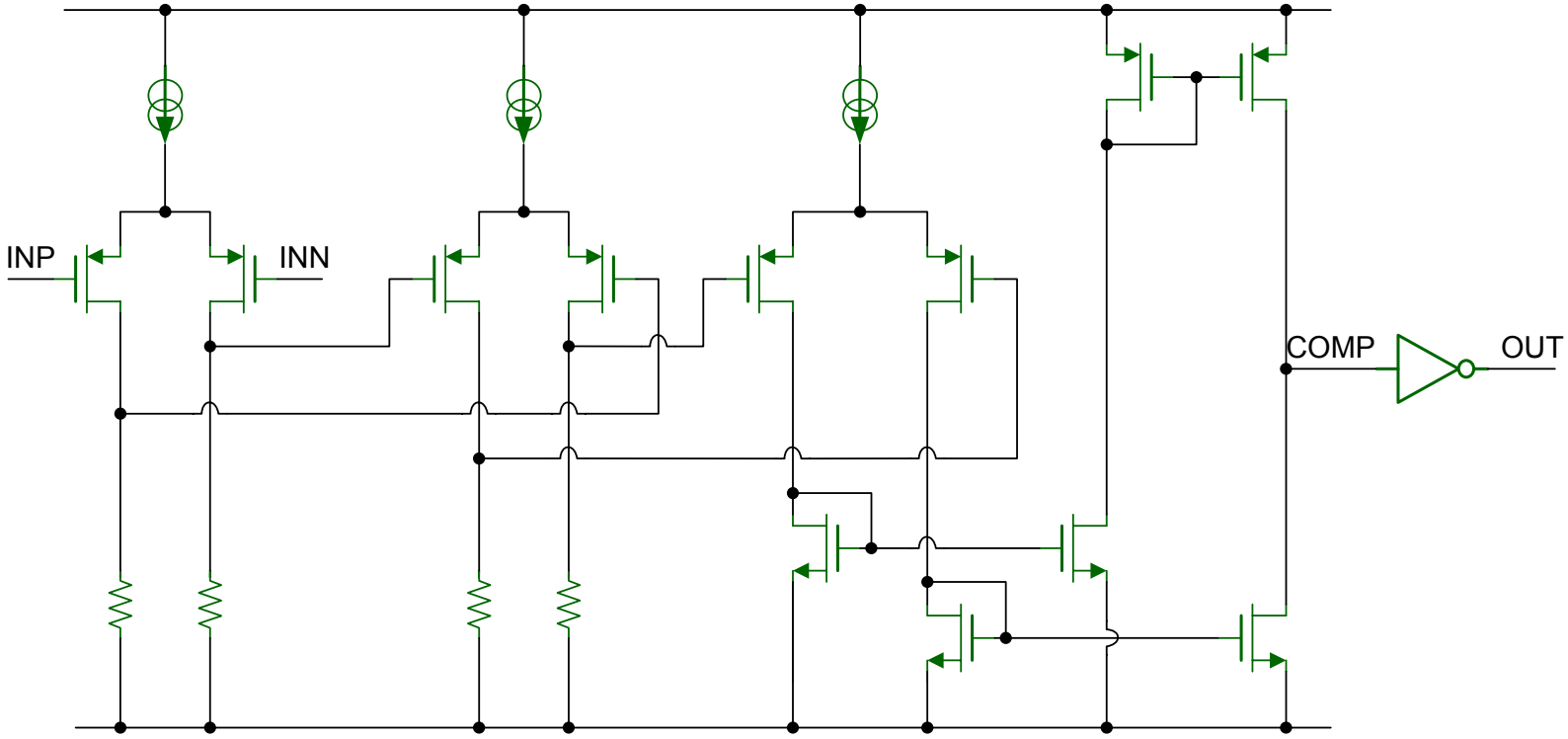
DC-DC Converter – Building Blocks

- PWM Comparator
  - Multi-Stage Gain -> Faster For Small Input Signal
  - But, High-Gain Stage Has Longer Recovery Time
  - So, Usually Low-Gain Amp(s) Followed by High-Gain Comparator



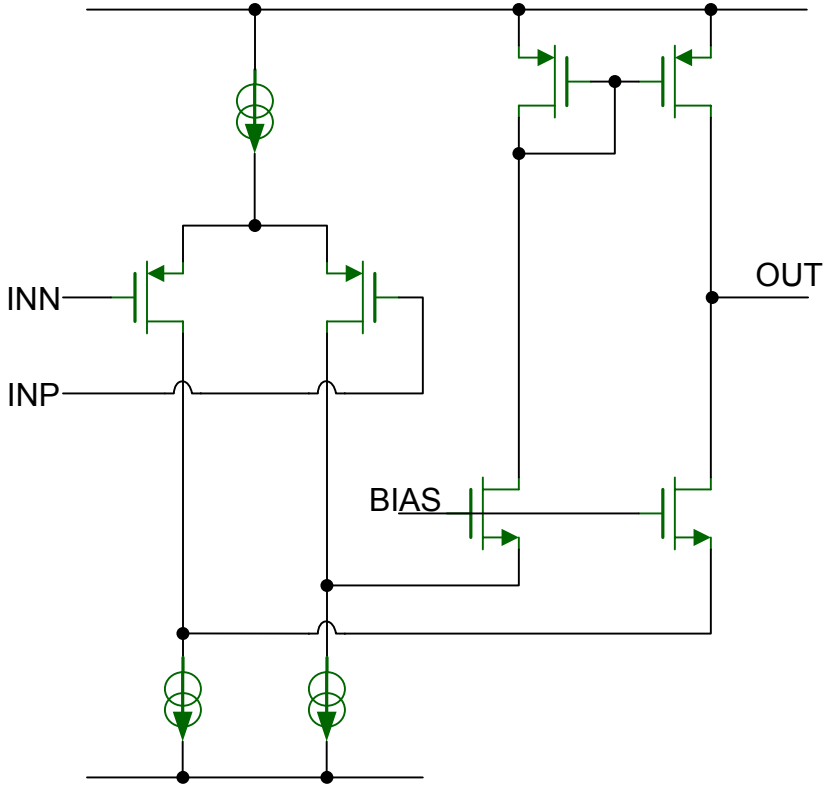
Building Blocks – PWM Comparator

OTA based comparator with pre-amps



Building Blocks – Error Amplifiers

- Error Amplifiers
  - Folded-Cascode Error Amplifier

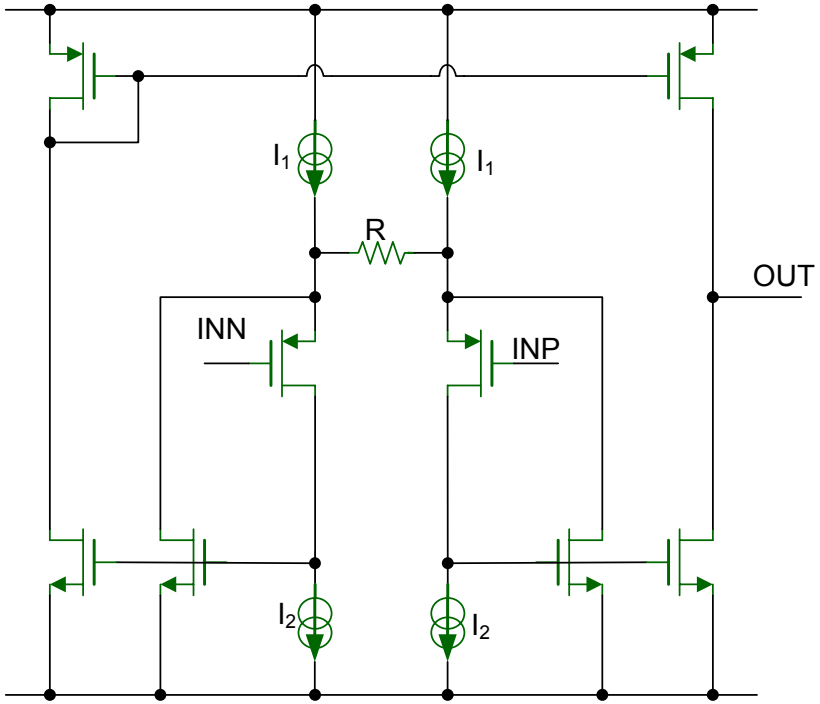


Good:
- Input Common Mode Down to Ground
- Smaller Input Offset than OTA

But:
- Difficult to get large Gm

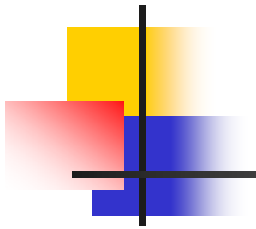
Building Blocks – Error Amplifiers

- Constant Gm Error Amplifier



Good:
- Constant Gm Defined by R
- Scalable Gm by Current Mirrors

But:
- Higher Input Offset due to Even More Current Mirrors
- Additional Gm Regulation Loop



DC-DC Converter Design

Acknowledgement:
Jian Zhou etc. for Review and Suggestions

Thank You For Your Attendance