A Sub-1-V Low-Noise Bandgap Voltage Reference

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***Abstract*—A new sub-1-V bandgap voltage reference is presented in this paper, which has advantages over the prior arts in terms of output noise and compatibility with several fabrication processes. The topology allows the reference to operate with a supply voltage as low as 1 V by employing the reverse bandgap voltage principle (RBVP). It also has an attractive low-noise output without the use of a large external filtering capacitor. The design was fabricated with a 0.5-μm BiCMOS process, but it is compatible with most CMOS and BiCMOS fabrication processes. The entire die area is approximately 0.4 mm^2, including all test pads and dummy devices. Theoretical analysis and experimental results show that the output noise spectral density is 40 nV/$\sqrt{\text{Hz}}$ with a bias current of 20 μA. Moreover, the peak-to-peak output noise in the 0.1–10 Hz band is only 4 μV. The untrimmed reference has a mean output voltage of 190.9 mV at room temperature, and it has a temperature coefficient in the $-40\,^{\circ}$C to $+125\,^{\circ}$C range of 11 ppm/°C (mean) with a standard deviation of 5 ppm/°C.**

***Index Terms*—BiCMOS, low noise, low voltage, noise measurement, peak-to-peak noise, sub-1-V bandgap voltage reference, temperature coefficient, 1-V supply.**

I. Introduction

A VOLTAGE reference is a critical building block in analog and mixed-signal circuits such as data converters and voltage regulators. Some of the key requirements for an ideal voltage reference are the following:

1) output voltage is temperature-independent;
2) output voltage is supply-independent;
3) operation over a wide range of supply voltages;
4) output voltage can be easily scaled.

One representative reference satisfying all of these key parameters is the bandgap voltage reference [1, pp. 338–346]. To the knowledge of the authors, this type of reference was first reported by Widlar in the development of the LM109 5-V output voltage regulator from National Semiconductor in the early 1970s [2]. Modifications to [2] allowed the output voltage of the reference to be scaled to 10 V [3] and 2.5 V [4]. In each of these cases, the bandgap output voltage is realized by adding a voltage that is complementary-to-absolute-temperature (CTAT) to another voltage which is proportional-to-absolute-temperature (PTAT) to yield a first-order temperature-compensated voltage.

The generation of the first-order temperature-compensated voltage $V_{\rm REF}(T)$ can be explained with the bandgap voltage reference [1, p. 344] shown in Fig. 1. This circuit produces the output voltage

$$V_{\rm REF} = V_{\rm BE1} + \left(\frac{R_2}{R_3}\right)\ln\left(\frac{R_2}{R_1}N\right)V_T \approx 1.2\ \text{V} \qquad (1)$$

Manuscript received December 12, 2006; revised June 18, 2007.

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Digital Object Identifier 10.1109/JSSC.2007.907226

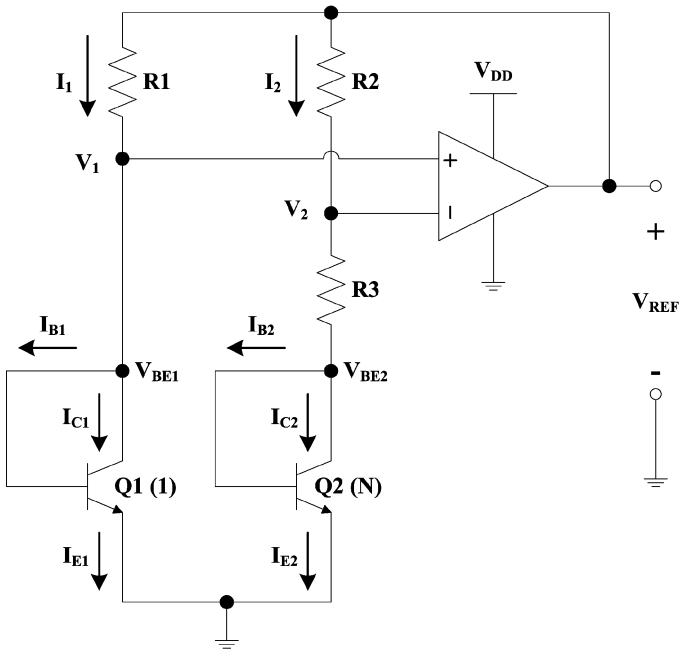


Fig. 1. Bandgap voltage reference with diode-connected NPN transistors in [1].

where N is the ratio of the emitter area of *Q2* to *Q1*. The $V_{\rm BE1}$ and V_T terms in (1) are the CTAT and PTAT voltages, respectively. The values of the resistors and N in (1) should be selected in order for the temperature effects due to the CTAT and PTAT voltages to cancel each other. When the temperature effects have been cancelled, the value of $V_{\rm REF}$ in (1) is approximately equal to the bandgap voltage of silicon extrapolated to zero degrees Kelvin or 1.2 V.

Although this bandgap voltage reference meets all of the desired characteristics mentioned above, this type of reference has a disadvantage in terms of the minimum supply voltage ($V_{\rm DD,min}$). Assuming the amplifier in Fig. 1 has a CMOS class AB output stage with a maximum $V_{\rm DS,sat}$ of 200 mV for the output drivers, the minimum supply voltage for the bandgap voltage reference is

$$V_{\rm DD,min} \geq \text{MAX}\left(V_{\rm REF} + V_{\rm DS,sat}\right) \approx 1.4\ \text{V}. \qquad (2)$$

As the minimum feature size of new fabrication processes is reduced, the power supply voltage for the circuits implemented with these processes has to be decreased in order to satisfy the smaller breakdown voltage requirements. Hence, voltage references which can operate with supply voltages less than 1.4 V are in high demand.

Recently, new voltage references have been reported in literature to overcome the low supply voltage problem [5]–[7]. These references generate a temperature-independent current, which

is then mirrored to a resistor to create a sub-1-V output voltage. These circuits are capable of operating with a supply voltage as low as 1 V, and they can be implemented in alternative processes such as BiCMOS [6] and CMOS [5], [7]. However, most of them suffer from high flat-band and $1/\mathrm{f}$ output noise due to the presence of the MOS current mirror in the topologies of these circuits. Another type of low-voltage reference, which is based on the weighted difference in gate-source voltages between MOS devices, uses an external filtering capacitor at the output to filter out the noise [8]. Unfortunately, the required capacitance is too large (greater than 100 nF) to be integrated. Furthermore, external components should be avoided because they increase the cost and volume of the system.

In this paper, a new bandgap voltage reference is presented, which can operate with supply voltages down to 1 V. In addition, it features a low-noise output without the need for a large external filtering capacitor. The circuit architecture is portable to both CMOS and BiCMOS processes. The rest of this paper is organized as follows. In Section II, the prior arts of low-voltage reference design are reviewed. Two types of sub-1-V references are analyzed, which are current-mode references and voltage-mode references. The operation and critical design problems in these reference circuits are discussed. Section III covers the proposed design solution with details of the operation principle and circuit schematic. A brief comparison with the prior arts is also included in this section. The noise and power of the proposed reference are analyzed in Section IV. Insight into optimizing these two parameters is also revealed. The experimental results are presented in Section V to verify the proposed design ideas, and the research efforts of this project are concluded in Section VI.

II. Prior Arts of Low-Voltage Reference Design

A. Current-Mode References

A traditional bandgap reference [1, p. 344] usually requires a supply voltage that is greater than its output voltage of 1.2 V. There have been several new current-mode references reported in literature which can operate with supply voltages below 1.2 V [5]–[7]. They can also be implemented in different processes such as CMOS [5], [7] and BiCMOS [6]. Current-mode references generate a temperature-independent current by summing CTAT currents with PTAT currents. The temperature-independent current is then mirrored to a resistor to yield a temperature-compensated reference voltage. The operation of this type of sub-1-V reference can be explained with the circuit shown in Fig. 2 [5]. The reference voltage $V_{\mathrm{REF\_IMODE}}$ in Fig. 2 is

$$V_{\mathrm{REF\_IMODE}} = \left(\frac{W_2}{W_1}\right)\left(\frac{R4}{R2}\right)\left[V_{\mathrm{EB1}} + M_{\mathrm{IMODE}} V_T\right] \quad (3)$$

where the scale factor M_{IMODE} is

$$M_{\mathrm{IMODE}} = \left(\frac{R_2}{R_3}\right)\ln\left(\frac{W_0}{W_1 N}\right). \quad (4)$$

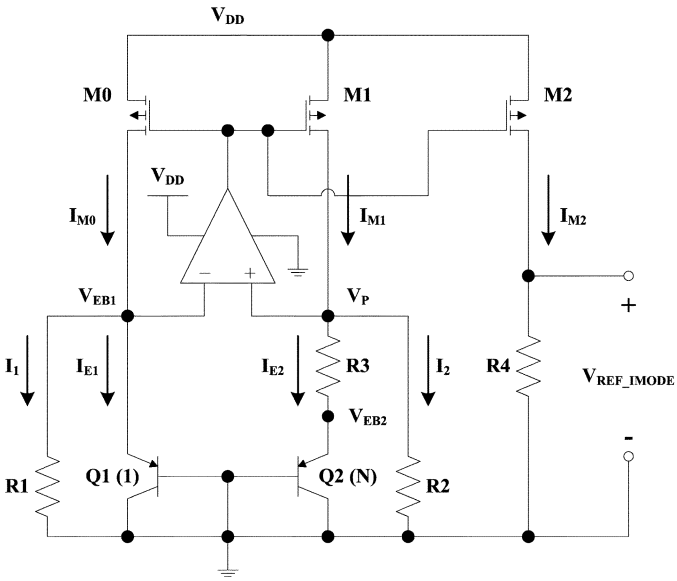


Fig. 2. Current-mode reference from [5].

Even though current-mode references have advantages in terms of low supply voltage operation and portability to different processes, this type of sub-1-V bandgap voltage reference suffers from high flat-band and $1/\mathrm{f}$ output noise due to the PFET current mirror in Fig. 2. This can be derived with the use of Fig. 3, which shows the simplified small-signal circuit of the one in Fig. 2 with RMS noise sources. The RMS noise source E_{g2} is the input-referred voltage noise of PFET *M2* in Fig. 2. The RMS noise source $E_{R4} = \sqrt{4kT\,(R4)}$ is the thermal noise voltage due to resistor *R4*. The noise sources of all the remaining components in the circuit propagate to the gate of *M2* in order to get to the output node, so the RMS noise voltage from the core is represented by E_{BGAP}. Since the current-mode reference circuits in [5]–[7] use bias currents in the microampere range, the small-signal source-drain impedance of *M2* ($r_{o2} \propto (1/\lambda I_{\mathrm{M2}})$) is greater than 1 MΩ. Therefore, its contribution to the output noise calculations can be neglected.

Since the noise sources are uncorrelated, the total RMS output noise spectral density $v_{\mathrm{NT\_IMODE}}$ is just the square root of the total mean square contributions from each noise source

$$v_{\mathrm{NT\_IMODE}} = (g_{m2}R4)\sqrt{E_{g2}^2 + E_{\mathrm{BGAP}}^2 + \left(\frac{E_{R4}}{g_{m2}R4}\right)^2}. \quad (5)$$

If *M2* is in the saturation region and in weak inversion, the expression for E_{g2} is [9]

$$E_{g2} = \sqrt{\left(\frac{2qI_{\mathrm{M2}}}{(g_{m2})^2}\right) + \left[\frac{1}{(g_{m2})^2}\frac{KF}{f}\frac{(I_{\mathrm{M2}})^{AF}}{C_{\mathrm{OX}}(L_2)^2}\right]} \quad (6)$$

with the transconductance [10, p. 167]

$$g_{m2} = \frac{I_{\mathrm{M2}}}{n_{\mathrm{SUB}} V_T}. \quad (7)$$

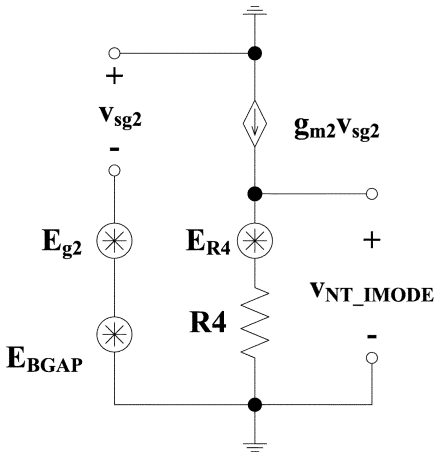


Fig. 3. Small-signal model of current-mode reference with RMS noise sources.

The first term under the square root of (6) is the input-referred shot noise of *M2*. The second term under the square root of (6) is the input-referred flicker noise with parameters KF (units of Farads $\times$ [Ampere^{3-AF}]) and AF (no units) for the PFET devices in the process. From Fig. 2

$$I_{\mathrm{M2}} = \frac{V_{\mathrm{REF\_IMODE}}}{R4}. \tag{8}$$

By substituting (6)–(8) into (5), the total RMS output noise spectral density is as shown in (9) at the bottom of the page. Inspection of (9) reveals that the only parameter that can be changed to reduce the flat-band output noise is resistor *R4*. However, reducing *R4* will increase the power dissipation of the circuit for a fixed reference voltage. The flicker noise term in (9) can only be reduced by increasing L_2 which will impact the size of the chip. Another important issue is the coefficient of E_{BGAP}^2 in (9). The coefficient is proportional to $1/T^2$, so noise due to E_{BGAP}^2 will increase as temperature decreases.

The noise analysis of the circuit in Fig. 3 shows the best method of reducing the output noise spectral density is to reduce the value of resistor *R4*. Unfortunately, this translates into an increase in power dissipation. Furthermore, the flicker noise of an FET is usually 10 to 50 times larger than a bipolar transistor of the same size and bias current [11, p. 19]. Instead of increasing the size of *M2* to reduce the flicker noise, an external filter capacitor can be placed between the output node and ground in order to reduce the noise bandwidth of the circuit below the 1/f corner frequency of *M2* [8]. Unfortunately, the required filter capacitor is usually too large (100 nF in [8]) to be integrated. An external filter capacitor increases the cost and volume of the application.

B. Voltage-Mode References

In addition to the current-mode references discussed in Section II-A, there is another type of sub-1-V bandgap voltage references called the voltage-mode references. These references have an output equal to a fraction of the voltage in (1). The result in (1) can be represented as

$$V_{\mathrm{REF}} = V_{\mathrm{BE1}} + M_V V_T \ln\left(\frac{I_{C1}}{I_{C2}}N\right) \tag{10}$$

where the scale factor M_V is

$$M_V = \frac{R2}{R3} \approx 6. \tag{11}$$

Dividing (10) by (11) produces a reference voltage $V_{\mathrm{REF\_}V}$ which is

$$V_{\mathrm{REF\_}V} = \frac{V_{\mathrm{BE1}}}{\mathrm{M_V}} + V_T \ln\left(\frac{I_{C1}}{I_{C2}}N\right) \approx 200\ \mathrm{mV}. \tag{12}$$

The method described by (12) uses the reverse bandgap voltage principle (RBVP). Instead of adding a V_{BE} voltage to a scaled V_T voltage, voltage-mode sub-1-V references add a V_T voltage to an attenuated V_{BE} voltage. Circuits employing this technique do not require the current mirror used in current-mode references such as *M0–M1–M2* in Fig. 2. Therefore, the output noise of voltage-mode references tends to be lower than current-mode ones for the same power dissipation and die area.

A voltage-mode reference which uses RBVP is shown in Fig. 4 [12]. The output voltage of this reference circuit is

$$V_{\mathrm{REF\_VMODE}} = \left(\frac{R2}{R1}\right)V_{\mathrm{BE1}} + V_T \ln\left(\frac{I_{E2}}{I_{C2}}N\right) + I_{B1}R2. \tag{13}$$

If I_{B1} is negligible and $I_{B2} \ll I_{C2}$ such that $I_{C2} \approx I_{E2}$, then (13) reduces to

$$V_{\mathrm{REF\_VMODE}} \approx \frac{V_{\mathrm{BE1}}}{\mathrm{M_{VMODE}}} + V_T \ln(N) \approx 200\ \mathrm{mV} \tag{14}$$

where the scale factor M_{VMODE} is

$$M_{\mathrm{VMODE}} = \frac{R1}{R2}. \tag{15}$$

It is clear the circuit in Fig. 4 uses RBVP since (14) has the same form as (12).

The output noise from the circuit in Fig. 4 can be calculated by using the small-signal model with RMS noise sources shown in Fig. 5. Transistor *Q2* in Fig. 4 is being treated as a diode in the noise analysis. The steady-state currents (I_{DC}) in the circuit from [12] are in the microampere range, so the small-signal output impedances (r_o) of the bias source, transistor *Q1*, and diode-connected transistor *Q2* are very large be-

$$v_{\mathrm{NT\_IMODE}} = V_{\mathrm{REF\_IMODE}}\sqrt{2q\left(\frac{R4}{V_{\mathrm{REF\_IMODE}}}\right) + \frac{KF}{f}\frac{1}{C_{\mathrm{OX}}(L_2)^2}\left(\frac{V_{\mathrm{REF\_IMODE}}}{R4}\right)^{AF-2} + \left(\frac{E_{\mathrm{BGAP}}}{n_{\mathrm{SUB}}V_T}\right)^2 + \frac{4kT(R4)}{(V_{\mathrm{REF\_IMODE}})^2}} \tag{9}$$

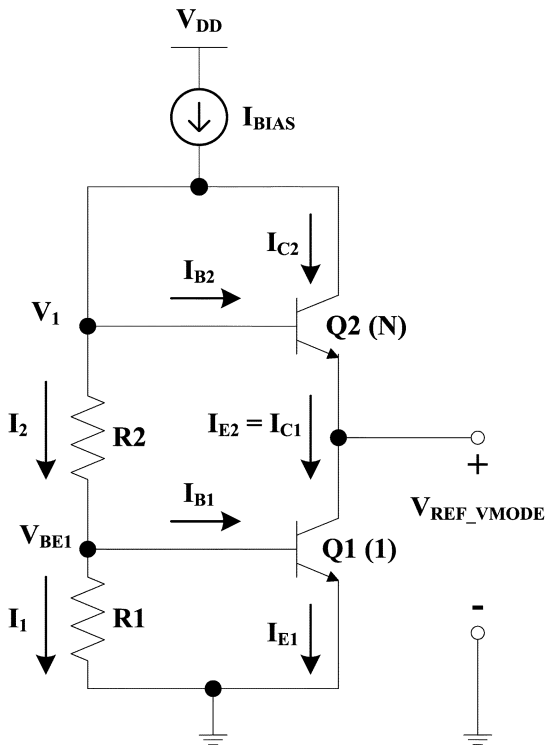


Fig. 4. Voltage-mode reference from [12].

cause $r_o \propto 1/I_{\rm DC}$. Hence, they can be neglected in the output noise calculations. The spectral density per $\sqrt{\text{Hz}}$ of the RMS voltage noise sources of the resistors and the RMS current noise sources of *Q1*, *Q2* in Fig. 5 are [1, pp. 720, 724–728]

$$E_{\rm Rx} = \sqrt{4kT\left(R_X\right)}, \quad x = 1, 2, ; \tag{16}$$

$$I_{nb1} = \sqrt{2q\left(\frac{I_{C1}}{\beta_1}\right) + \frac{K_1}{f}\left(\frac{I_{C1}}{\beta_1}\right)^a}, \tag{17}$$

$$I_{nc1} = \sqrt{2qI_{C1}}, \tag{18}$$

$$I_{nd2} = \sqrt{N\left(I_{nd2\_\rm unit}\right)^2} = \sqrt{2qI_{C2}\left(1+\frac{1}{\beta_2}\right)+\left(\frac{1}{N^{a-1}}\right)\left[\frac{K_1}{f}\left(\frac{I_{C2}}{\beta_2}\right)^a\right]}. \tag{19}$$

The currents I_{C1} and I_{C2} are the steady-state collector currents of transistors *Q1* and *Q2* in Fig. 4. Since the noise sources are uncorrelated, the total RMS output noise spectral density $v_{\rm NT\_VMODE}$ is just the square root of the total mean square contributions from each noise source, as shown in (20) at the bottom of the page, where the X factors are

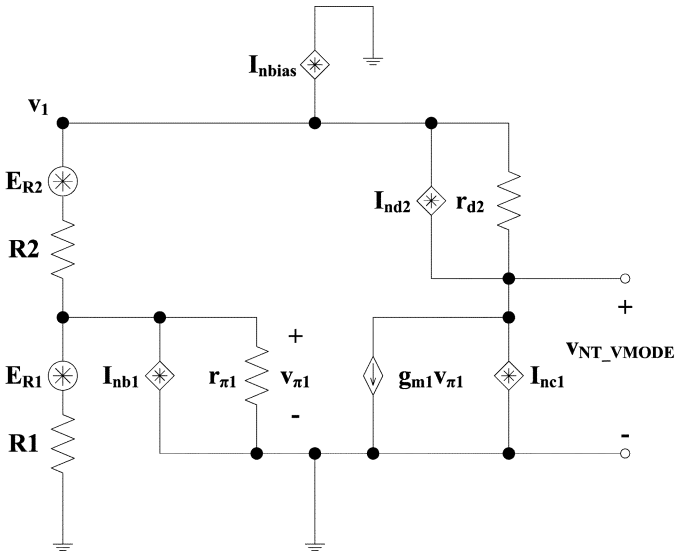


Fig. 5. Small-signal model of voltage-mode reference with RMS noise sources.

$$X_D = 1 + \frac{R1}{r_{\pi 1}} + g_{m1}R1, \tag{21}$$

$$X_1 = \left|-g_{m1}R2\right|, \tag{22}$$

$$X_2 = 1 + (R2 + r_{d2})\left(\frac{1}{R1} + \frac{1}{r_{\pi 1}}\right), \tag{23}$$

$$X_3 = R2\left(\frac{1}{R1} + \frac{1}{r_{\pi 1}}\right). \tag{24}$$

If $X_2 > X_1 > X_3$, then the dominant RMS noise sources in (20) are the thermal noise voltage of resistor *R2* (E_{R2}^2), the shot and flicker noise of diode-connected transistor *Q2* ($[I_{nd2}r_{d2}]^2$), and the collector current shot-noise of *Q1* ($[I_{nc1}R1]^2$) [13].

The main advantage of the circuit in Fig. 4 is lower output noise than the current-mode reference in Fig. 2 for the same current consumption. The total current consumption $I_{\rm VMODE}$ for the circuit in Fig. 4 is

$$I_{\rm VMODE} = \frac{V_{\rm BE1}}{R1} + I_{B1V} + I_{C1V} + I_{\rm BIASCORE} \tag{25}$$

where $I_{\rm BIASCORE}$ is the current consumed by the bias circuit in [12] and I_{C1V} and I_{B1V} are the collector and base currents of

$$v_{\rm NT\_VMODE} = \sqrt{E_{R2}^2 + \left(I_{nd2}r_{d2}\right)^2 + \left(\frac{X_1}{X_D}\right)^2\left[E_{R1}^2 + \left(I_{nb1}R1\right)^2\right] + \left(\frac{X_2}{X_D}\right)^2\left(I_{nc1}R1\right)^2 + \left(\frac{X_3}{X_D}\right)^2\left(I_{nbias}R1\right)^2} \tag{20}$$

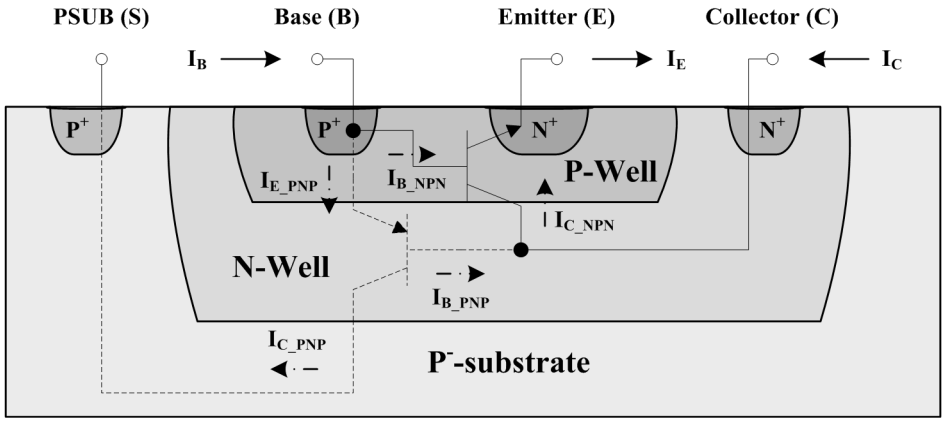


Fig. 6. Cross-section of vertical NPN transistor in twin-well CMOS process.

Q1 in Fig. 4, respectively. Assuming the lengths of the PFETs in the mirror of Fig. 2 are the same, the total current consumption $I_{\rm IMODE}$ for the circuit in Fig. 2 is

$$I_{\rm IMODE} = \left(\frac{W_1 + W_2}{W_0} + 1\right)\left(\frac{V_{\rm EB1}}{R1} + I_{E1I}\right) + I_{\rm OPAMP} \tag{26}$$

where $I_{\rm OPAMP}$ is the current consumed by the amplifier and I_{E1I} is the emitter current of *Q1*. If both circuits have the same current consumption, then (25) and (26) can be equated to yield

$$I_{C1V} = \left(\frac{W_1}{W_2} + 1\right) I_{\rm M2} + I_{E1I} + I_{\rm OPAMP} - (I_{B1V} + I_{\rm BIASCORE}) \tag{27}$$

where

$$I_{\rm M2} = \frac{W_2}{W_0}\left(\frac{V_{\rm EB1}}{R1} + I_{E1I}\right). \tag{28}$$

Even if $W_1 = W_2$ and $I_{\rm BIASCORE} = I_{\rm OPAMP} + I_{E1I} - I_{B1V}$, the value of I_{C1V} in Fig. 4 is twice the current $I_{\rm M2}$ in the output stage of Fig. 2 based on (27). The output noise due to I_{nd2} in (20) will decrease since $r_{d2} \propto 1/I_{C1V}$. Furthermore, $X_D \propto I_{C1V}$ due to the transconductance term in (21). Since all but two of the noise terms in (20) are divided by X_D^2, the output noise of the circuit in Fig. 4 will decrease as I_{C1V} increases. Based on these results, the output noise of the circuit in Fig. 4 will be lower than that in Fig. 2 for the same current consumption.

Even though a traditional voltage-mode reference such as the one in Fig. 4 has the benefit of low output noise, it suffers from several drawbacks. One of them is the key transistor *Q1* operates in the deep saturation region. Transistors *Q1* and *Q2* in [12] were fabricated with a low-voltage twin-well CMOS process. Fig. 6 shows a cross-section of a vertical NPN transistor formed in a twin-well process with a p-type substrate. When the NPN device is fabricated, a parasitic PNP device is formed from the base and collector of the NPN to the p-type substrate. When the NPN device is saturated, the parasitic PNP device begins operating in the forward-active region since the emitter-base voltage ($V_{\rm EB}$) of the PNP is equal to $V_{\rm BC}$ of the NPN. Assuming the substrate voltage (V_{PSUB}) is the lowest potential in the system, the terminal currents for the collector (I_C), base (I_B), and emitter (I_E) of the NPN device in terms of the voltages $V_{\rm BE}$ and $V_{\rm BC}$ in Fig. 6 can be described by the following Ebers–Moll equations [1, p. 23]:

$$I_C = I_{S\_\rm NPN}\exp\left(\frac{V_{\rm BE}}{V_T}\right) - \left[I_{S\_\rm NPN} - I_{S\_\rm PNP}\left(\frac{1}{\beta_{R\_\rm PNP}}\right)\right] - \left[I_{S\_\rm NPN}\left(\frac{\beta_{R\_\rm NPN}+1}{\beta_{R\_\rm NPN}}\right) + I_{S\_\rm PNP}\left(\frac{1}{\beta_{F\_\rm PNP}}\right)\right] \times \left[\exp\left(\frac{V_{\rm BC}}{V_T}\right) - 1\right], \tag{29}$$

$$I_B = I_{S\_\rm NPN}\left(\frac{1}{\beta_{F\_\rm NPN}}\right)\exp\left(\frac{V_{\rm BE}}{V_T}\right) - \left[I_{S\_\rm NPN}\left(\frac{1}{\beta_{F\_\rm NPN}}\right) - I_{S\_\rm PNP}\right] + \left[I_{S\_\rm NPN}\left(\frac{1}{\beta_{R\_\rm NPN}}\right) + I_{S\_\rm PNP}\left(\frac{\beta_{F\_\rm PNP}+1}{\beta_{F\_\rm PNP}}\right)\right] \times \left[\exp\left(\frac{V_{\rm BC}}{V_T}\right) - 1\right], \tag{30}$$

$$I_E = I_{S\_\rm NPN}\left(\frac{\beta_{F\_\rm NPN}+1}{\beta_{F\_\rm NPN}}\right)\left[\exp\left(\frac{V_{\rm BE}}{V_T}\right) - 1\right] - I_{S\_\rm NPN}\left[\exp\left(\frac{V_{\rm BC}}{V_T}\right) - 1\right] \tag{31}$$

where β_F, β_R are the current gains of the NPN and parasitic PNP in the forward-active and reverse-active regions, respectively. According to Fig. 4, the base-collector voltage $V_{\rm BC1}$ is

$$V_{\rm BC1} = V_{\rm BE1} - V_{\rm CE1} = V_{\rm BE1} - V_{\rm REF\_VMODE}. \tag{32}$$

Typical base-emitter ($V_{\rm BE}$) voltages for fabricated bipolar devices operating in the forward-active region at room temperature are between 0.5 and 0.7 V [11, p.13]. The NPN devices in [12] were characterized with $V_{\rm BE}$ set to 0.7 V. Since $V_{\rm REF\_VMODE}$ is 0.2 V,

$$V_{\rm BC1} = V_{\rm BE1} - V_{\rm CE1} = 0.7 - V_{\rm REF\_VMODE} = 0.5\ \rm V. \tag{33}$$

The result in (33) means *Q1* is saturated. Once $V_{\rm CE1}$ of *Q1* in Fig. 4 is less than $V_{\rm BC1}$ with $V_{\rm BE1}$ fixed, the ratio $\beta_{F1} = I_{C1}/I_{B1}$ decreases. This means I_{B1} is not negligible as assumed in (14). Since the $V_{\rm BC}$ term is in the exponents

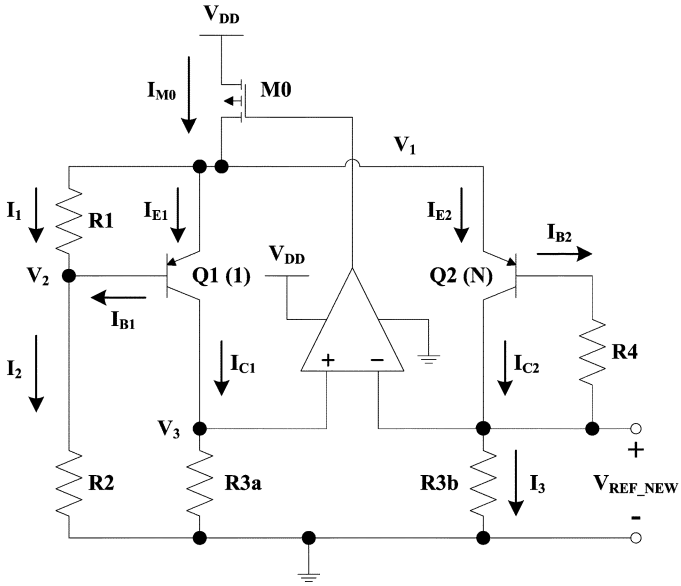


Fig. 7. Proposed voltage reference.

of (29)–(31), slight changes in V_{CE1} when *Q1* is saturated will make significant changes in I_{B1}. This in turn will cause variations in the reference voltage due to the $I_{B1}R2$ error term in (13).

The second disadvantage is the topology of the voltage-mode reference in [12] depends on processes which offer NPN devices. In [12], a NPN transistor was implemented in a twin-well CMOS process. Bipolar or BiCMOS processes which offer NPN transistors would also be good candidates for fabricating this circuit. Unfortunately, these processes will be more expensive than an N-well CMOS process since they require additional processing steps.

Another disadvantage is that the circuit in [12] requires a separate bias current source for proper operation instead of using a feedback system to control the current of the reference core. The use of a separate current source causes the currents inside the natural logarithm of (13) to rely on temperature-dependent parameters instead of ratios of resistors as in (1) or ratios of transistor sizes as in (3). Hence, it complicates the calculation of the scale factor in (15).

The last problem with the circuit in Fig. 4 is the output impedance of the bias current source degrades the line regulation or DC power supply rejection ratio (PSRR) of the reference voltage. This is supported by the information in Table I of Section V.

III. Proposed Sub-1-V Low-Noise Voltage Reference

A. Circuit Architecture and Operation Principle

A new sub-1-V bandgap voltage reference [13], [14] has been developed to overcome the issues discussed in Section II. The circuit schematic of the proposed reference is shown in Fig. 7. It produces an output voltage based on RBVP just like the voltage-mode references described in Section II. Transistor *Q1* and resistors *R1*, *R2* form a V_{BE}-multiplier which creates a scaled V_{EB1} voltage at node V_1. The reference voltage $V_{\mathrm{REF\_NEW}}$ is produced by subtracting V_{EB2} from V_1, and the equation describing $V_{\mathrm{REF\_NEW}}$ has the same form as (12).

The operation of the proposed reference can be described by performing a DC analysis on the circuit in Fig. 7. As a result, the voltage V_1 can be represented as

$$V_1 = \left(1 + \frac{R2}{R1}\right) V_{\mathrm{EB1}} + I_{B1}R2. \tag{34}$$

The KVL equation around V_1, the emitter-base of transistor *Q2*, and $V_{\mathrm{REF\_NEW}}$ yields

$$V_{\mathrm{REF\_NEW}} = V_1 - V_{\mathrm{EB2}} - I_{B2}R4. \tag{35}$$

The substitution of (34) for V_1 in (35) yields

$$\mathrm{V_{REF\_NEW}} = \left(\frac{\mathrm{R2}}{\mathrm{R1}}\right) \mathrm{V_{EB1}} + (\mathrm{V_{EB1}} - \mathrm{V_{EB2}}) + (I_{B1}R2 - I_{B2}R4). \tag{36}$$

The reason resistor *R4* is added between the base of *Q2* and the node $V_{\mathrm{REF\_NEW}}$ is to cancel the error in (36) due to I_{B1}. If the value of resistor *R4* is selected to be

$$R4 = R2\left(\frac{I_{B1}}{I_{B2}}\right), \tag{37}$$

then (36) reduces to

$$V_{\mathrm{REF\_NEW}} = \left(\frac{R2}{R1}\right) V_{\mathrm{EB1}} + (V_{\mathrm{EB1}} - V_{\mathrm{EB2}}). \tag{38}$$

Obviously, the ratio I_{B1}/I_{B2} needs to remain constant over temperature and supply voltage in order for the error due to I_{B1} in (36) to be eliminated. Complete cancellation of the error term in (36) will not occur if there is a mismatch between resistors *R2* and *R4*. Also, the error term will not be removed if I_{B1}/I_{B2} changes over temperature and supply. Even if resistor *R4* does not completely cancel the error from I_{B1}, it does reduce the constraint that currents I_1, I_2 have to be considerably larger than I_{B1} to minimize the error term as in [12] and [15]. Furthermore, this method is easy to implement, and it does not increase the current consumption.

The difference in the emitter-base voltages in (38) can be represented in terms of the collector currents I_{C1} and I_{C2} of transistors *Q1* and *Q2*, respectively, by using the equation

$$V_{\mathrm{EB1}} - V_{\mathrm{EB2}} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}N\right). \tag{39}$$

When (39) is substituted into (38), the value of the reference voltage becomes

$$V_{\mathrm{REF\_NEW}} = \left(\frac{R2}{R1}\right) V_{\mathrm{EB1}} + V_T \ln\left(\frac{I_{C1}}{I_{C2}}N\right) \tag{40}$$

where N is the ratio of the *Q2* emitter area to the *Q1* emitter area. Assuming the input bias currents of the operational amplifier (opamp) in Fig. 7 can be neglected, the value of I_{C1} can be represented by the KCL equation at node V_3 which is

$$I_{C1} = \frac{V_3}{R3a}. \tag{41}$$

The value of I_{C2} is derived from the KCL equation at the node $V_{\mathrm{REF\_NEW}}$ which is

$$I_{C2} = I_3 - I_{B2}. \tag{42}$$

Inspection of the circuit in Fig. 7 shows

$$I_3 = \frac{V_{\mathrm{REF\_NEW}}}{R3b}. \tag{43}$$

Substitution of (43) into (42) simplifies I_{C2} to

$$I_{C2} = \frac{V_{\mathrm{REF\_NEW}}}{R3b} - I_{B2}. \tag{44}$$

By substituting (41) and (44) into (40), the value of $V_{\mathrm{REF\_NEW}}$ becomes

$$V_{\mathrm{REF\_NEW}} = \left(\frac{R2}{R1}\right) V_{\mathrm{EB1}} + V_T \ln\left(\frac{V_3}{\left(\frac{R3a}{R3b}\right) V_{\mathrm{REF\_NEW}} - I_{B2} R3a} N\right). \tag{45}$$

The opamp and the PFET current source *M0* in Fig. 7 form a feedback loop which forces V_3 to be the same as $V_{\mathrm{REF\_NEW}}$. Assuming the opamp has no input voltage offset error and the loop gain in the circuit is sufficiently high, the value of V_3 is

$$V_3 = V_{\mathrm{REF\_NEW}}. \tag{46}$$

Using (46) in (45) simplifies the expression for $V_{\mathrm{REF\_NEW}}$ to

$$V_{\mathrm{REF\_NEW}} = \left(\frac{R2}{R1}\right) V_{\mathrm{EB1}} + V_T \ln\left(\frac{N}{\left(\frac{R3a}{R3b}\right) - \left(\frac{I_{B2} R3a}{V_{\mathrm{REF\_NEW}}}\right)}\right). \tag{47}$$

As long as $V_{\mathrm{REF\_NEW}} \gg I_{B2} R3a$, then (47) simplifies to

$$V_{\mathrm{REF\_NEW}} \approx \frac{V_{\mathrm{EB1}}}{\mathrm{M_{NEW}}} + V_T \ln\left(\frac{R3b}{R3a} N\right) \approx 200\ \mathrm{mV} \tag{48}$$

where the scale factor M_{NEW} is

$$M_{\mathrm{NEW}} = \frac{R1}{R2}. \tag{49}$$

Comparison of (48) with (12) shows the two equations are equal to each other when $R3a = R3b$. This supports the claim that the circuit in Fig. 7 uses RBVP.

The supply voltage (V_{DD}) is related to $V_{\mathrm{REF\_NEW}}$ by solving the KVL equation in the output branch of the circuit in Fig. 7. Performing this action results in the expression

$$V_{\mathrm{DD}} = V_{\mathrm{REF\_NEW}} + I_{B2} R4 + V_{\mathrm{EB2}} + V_{\mathrm{SD0,sat}} \tag{50}$$

where $V_{\mathrm{SD0,sat}}$ is the source-drain saturation voltage of current source *M0*. If $I_{B2}R4$ is negligible and the maximum V_{EB2} and $V_{\mathrm{SD0,sat}}$ voltages over the temperature range of interest are 600 mV and 200 mV, respectively, then (50) along with (48) provide the minimum supply voltage ($V_{\mathrm{DD,min}}$) for the circuit: $V_{\mathrm{DD,min}} \geq 1$ V. Thus, the proposed reference circuit has the capability of operating with a supply voltage down to 1 V.

Mismatch errors between resistors *R1* and *R2*, *R3a* and *R3b*, and *R2* and *R4* cause the reference output voltage to deviate from the ideal value in (47). So does an input offset voltage error (V_{OS}) associated with the amplifier in Fig. 7. A DC analysis can be performed on the circuit in Fig. 7 to determine the amount of error introduced into the reference output voltage due to these errors. The mismatch errors can be defined by the following resistor ratios:

$$\frac{R2}{R1x} = (1 + \Delta x1)\left(\frac{R2}{R1}\right), \tag{51}$$

$$\frac{R3a}{R3b_x} = (1 + \Delta x2)\left(\frac{R3a}{R3b}\right), \tag{52}$$

$$\frac{R4x}{R2} = (1 + \Delta x3)\left(\frac{R4}{R2}\right) \tag{53}$$

where $\Delta x1$, $\Delta x2$, and $\Delta x3$ are the amount of mismatch error in the ideal ratios of $R2/R1$, $R3a/R3b$, and $R4/R2$, respectively. An input offset voltage error of the amplifier will cause (46) to become

$$V_{3\_\Delta X4} = V_{\mathrm{REF\_}\Delta X4} \pm V_{\mathrm{OS}} \tag{54}$$

where $V_{3\_\Delta X4}$, $V_{\mathrm{REF\_}\Delta X4}$ are the voltages V_3, $V_{\mathrm{REF\_NEW}}$ in Fig. 7 when there is an offset voltage with the amplifier. The actual reference voltage $V_{\mathrm{REF\_}\Delta Xi}$ for the proposed reference due to each error can be defined as

$$V_{\mathrm{REF\_}\Delta Xi} = V_{\mathrm{REF\_NEW}} + V_{\Delta Xi}, \quad i = 1, 2, 3, 4 \tag{55}$$

where $V_{\mathrm{REF\_NEW}}$ is the ideal output voltage described by (47) and $V_{\Delta X1}$–$V_{\Delta X3}$ are the error voltages associated with (51)–(53), respectively. The error voltage $V_{\Delta X4}$ is associated with the V_{OS} term in (54).

Ideally, the value of resistor *R4* is selected to satisfy (37) such that

$$R4 = R2\left(\frac{R3b}{R3a}\right)\left(\frac{\beta_2 + 1}{\beta_1}\right). \tag{56}$$

Assuming $V_{\mathrm{REF\_NEW}} \gg I_{B2} R3b$ and $\beta_2/(\beta_2 + 1) \approx 1$, the errors in the reference output voltage from each resistor mismatch are approximately

$$V_{\Delta X1} \approx \frac{(\Delta x1)\, V_{\mathrm{EB1}}}{\frac{R1}{R2} - \frac{V_T(1+\Delta x1)}{V_{\mathrm{REF\_NEW}}}}, \tag{57}$$

$$V_{\Delta X2} \approx \frac{-(\Delta x2)\, V_{\mathrm{REF\_NEW}}\left[\frac{V_T}{V_{\mathrm{REF\_NEW}}} + \frac{R4}{(\beta_2+1)R3b}\right]}{1 + (\Delta x2)\left[\frac{V_T}{V_{\mathrm{REF\_NEW}}} + \frac{R4}{(\beta_2+1)R3b}\right] - \left(\frac{R2}{R1}\right)\left(\frac{V_T}{V_{\mathrm{REF\_NEW}}}\right)}, \tag{58}$$

$$V_{\Delta X3} \approx \frac{-(\Delta x3)\,\frac{R4(V_{\mathrm{REF\_NEW}})}{(\beta_2+1)R3b}}{1 + \frac{R4(\Delta x3)}{(\beta_2+1)R3b} - \left(\frac{R2}{R1}\right)\left(\frac{V_T}{V_{\mathrm{REF\_NEW}}}\right)}, \tag{59}$$

$$V_{\Delta X4} \approx \frac{\pm V_{\mathrm{OS}}\left[\left(1 + \frac{R2}{R1}\right)\left(\frac{V_T}{V_{\mathrm{REF\_NEW}}}\right) + \frac{R2}{\beta_1 R3a}\right]}{1 - \left(\frac{R2}{R1}\right)\left(\frac{V_T}{V_{\mathrm{REF\_NEW}}}\right)}. \tag{60}$$

Assuming resistors *R1* and *R2* are made of the same material, the denominator of (57) will be approximately temperature-independent since $R1/R2 \gg V_T/V_{\mathrm{REF\_NEW}}$. This means the temperature dependence of $V_{\Delta X1}$ is CTAT due to the V_{EB1} term in the numerator. The error voltage $V_{\Delta X1}$ will be small since $R1/R2 \gg V_{\mathrm{EB1}}$. The fractional terms in the denominators of (58) and (59) are considerably less than 1 due to the β_2 and $V_{\mathrm{REF\_NEW}}$ terms. Therefore,

$$V_{\Delta X2} \approx -(\Delta x2)\left[V_T + \frac{R4}{R3b}\left(\frac{V_{\mathrm{REF\_NEW}}}{\beta_2+1}\right)\right] \tag{61}$$

and

$$V_{\Delta X3} \approx -(\Delta x3)\left(\frac{R4}{R3b}\right)\left(\frac{V_{\mathrm{REF\_NEW}}}{\beta_2+1}\right). \tag{62}$$

The error voltage $V_{\Delta X2}$ should increase in absolute value as temperature increases due to the V_T term in (61), while the error voltage $V_{\Delta X3}$ should remain relatively constant as temperature increases due to the $V_{\mathrm{REF\_NEW}}$ term in (62). These observations are valid as long as the temperature drift of β_2 is negligible and resistors *R3b*, *R4* are made with the same material (same temperature coefficient). Furthermore, the results show that $V_{\Delta X2}$ and $V_{\Delta X3}$ can be minimized by using PNP transistors with high β and having $R3b > R4$. Inspection of (60) shows $V_{\Delta X4}$ should have a temperature dependence proportional to $V_T/(1-V_T)$ as long as the temperature drift of V_{OS}, β_1 are negligible and resistors *R2*, *R3a* are made with the same material (same temperature coefficient). Furthermore, $V_{\Delta X4}$ can be minimized by using PNP transistors with high β and having $R3a > R2$.

B. Comparison to the Prior Arts

The proposed reference has several advantages over the prior arts in Section II. One of them is the temperature coefficient (TC) of each collector current is well defined. The difference in the calculation of M_{NEW} for this design versus the scale factor calculations in Section II-B lies in fact that the collector currents I_{C1} and I_{C2} are controlled by the feedback loop in Fig. 7. As shown in the natural logarithm terms of (40) and (48),

$$\frac{I_{C1}}{I_{C2}} \approx \frac{R3b}{R3a}. \tag{63}$$

This result reveals the collector currents are set by resistors *R3a* and *R3b* instead of V_{BE1} as in [12] or the reference voltage and V_{BE1} as in [15]. Furthermore, the currents I_{C1} and I_{C2} are proportional to $V_{\mathrm{REF\_NEW}}$ in (41) and (44). This means the currents are temperature-independent. These conditions allow the value of M_{NEW} to be easily calculated without relying on computer simulations and accurate component models to find it by trial and error.

The next advantage of the proposed reference is the key transistor $Q1$ operates away from the deep saturation region. A disadvantage with the circuit in [12] is transistor *Q1* operates in the deep saturation region. This causes a variation in the reference voltage due to increased base current I_{B1}. The circuit in Fig. 7, on the other hand, has *Q1* operating in the forward-active region. The voltage across the collector-base junction of *Q1* in Fig. 7 is

$$V_{\mathrm{CB1}} = V_{\mathrm{EB1}} - V_{\mathrm{EC1}}. \tag{64}$$

Inspection of the circuit shows

$$V_{\mathrm{EC1}} = V_1 - V_3. \tag{65}$$

By using (34) and (46) in (65), the expression for V_{EC1} becomes

$$V_{\mathrm{EC1}} \approx \left(1+\frac{R2}{R1}\right)V_{\mathrm{EB1}} - V_{\mathrm{REF\_NEW}}. \tag{66}$$

Assuming I_{B1} can be neglected, substitution of (48) and (66) into (64) yields

$$V_{\mathrm{CB1}} \approx V_T \ln\left(\frac{R3b}{R3a}N\right). \tag{67}$$

By using (67) for V_{BC} in (29)–(31), the reduction of I_{C1}, I_{E1} and the increase of I_{B1} are proportional to

$$\exp\left(\frac{V_{\mathrm{CB1}}}{V_T}\right) - 1 = N\left(\frac{R3b}{R3a}\right) - 1. \tag{68}$$

The result in (68) indicates the changes in I_{C1}, I_{B1}, and I_{E1} due to V_{CB1} stay constant over temperature if resistors *R3a* and *R3b* are made with the same material (identical temperature coefficients). The base-collector voltage V_{BC1} of *Q1* in [12] is expressed by (32). Substituting (32) for V_{BC} in (29)–(31) shows the reduction of I_{C1}, I_{E1} and the increase of I_{B1} are proportional to

$$\exp\left(\frac{V_{\mathrm{BC1}}}{V_T}\right) - 1 = \exp\left(\frac{V_{\mathrm{BE1}} - V_{\mathrm{REF\_VMODE}}}{V_T}\right) - 1. \tag{69}$$

The result in (69) indicates the changes in I_{C1}, I_{B1}, and I_{E1} due to V_{BC1} will vary with temperature since V_{BE1} and V_T in the exponential are temperature-dependent variables. Furthermore, the results in (68) and (69) show the base-collector voltage of *Q1* in [12] impacts the collector, base, and emitter currents more than the collector-base voltage of *Q1* in the proposed design since

$$\exp\left(\frac{V_{\mathrm{BE1}} - V_{\mathrm{REF\_VMODE}}}{V_T}\right) \gg \left(\frac{R3b}{R3a}\right)N. \tag{70}$$

This analysis indicates the error in (36) from I_{B1} is better controlled by the circuit in Fig. 7 than the same error in [12]. Hence, variations in V_{EC1} and V_{EB1} of *Q1* due to mismatches in the circuit should not significantly reduce the effect of resistor *R4* to cancel the error term from I_{B1} in (36).

In addition to the advantages discussed above, the design is compatible with low-cost N-well CMOS processes. The circuit uses PNP devices to create the V_{EB1} and V_{EB2} voltages in the reference core. Unlike the NPN transistors in [12] and [15], PNP transistors can be implemented as lateral devices in modern low-cost N-well CMOS processes with p-type substrates [16].

Finally, there is no mismatch between the collector currents in the proposed reference due to the Early voltage. It is desirable to have the same emitter-collector voltages for *Q1* and *Q2* in order to eliminate errors or mismatch in the collector currents due to base-width modulation. The collector current (I_C) of a PNP bipolar transistor is related to the emitter-collector voltage (V_{EC}) and the Early voltage (V_A) by [1, p. 19]

$$I_C = I_S \exp\left(\frac{V_{\mathrm{EB}}}{V_T}\right)\left(1+\frac{V_{\mathrm{EC}}}{V_A}\right). \tag{71}$$

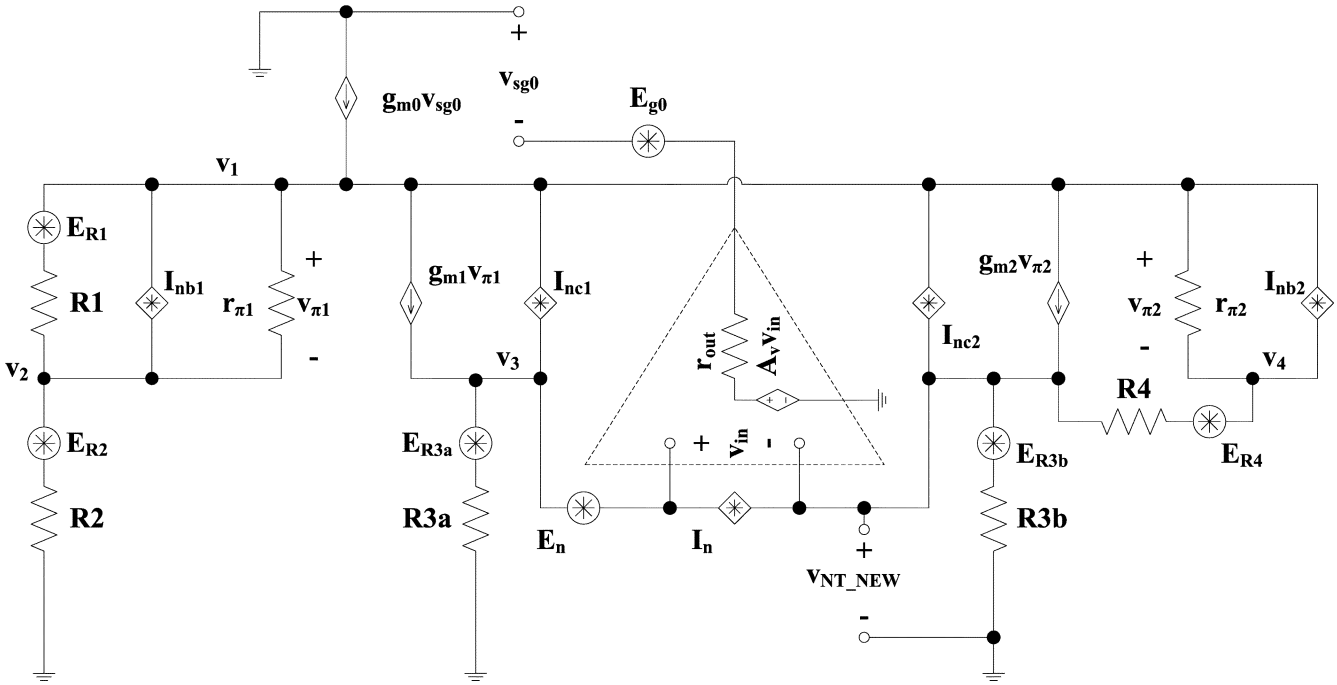


Fig. 8. Small-signal circuit of the proposed reference with RMS noise sources.

Substitution of (71) for $V_{\rm EB1}$ and $V_{\rm EB2}$ in (38) along with using (41), (44), and (46) yields

$$V_{\rm REF\_NEW} = \frac{V_{\rm EB1}}{\rm M_{NEW}} + V_T \ln\left[\frac{N}{\left(\frac{R3a}{R3b}\right) - \left(\frac{I_{B2}R3a}{V_{\rm REF\_NEW}}\right)}\left(\frac{1+\frac{V_{\rm EC2}}{V_A}}{1+\frac{V_{\rm EC1}}{V_A}}\right)\right]. \quad (72)$$

The Early voltage for lateral PNP devices in a bulk CMOS process tends to be less than 10 V due to the short base width. If this is the case, then $V_{\rm REF\_NEW}$ will no longer just depend on the ratio of *R3a* and *R3b*. Since the emitter terminals of *Q1* and *Q2* are connected together in Fig. 7, the dependence of $V_{\rm REF\_NEW}$ on the Early voltages of *Q1* and *Q2* can be removed if the collector voltages of *Q1* and *Q2* are the same. The derivation of (63) shows the amplifier in Fig. 7 forces the voltages at nodes $V_{\rm REF\_NEW}$ and V_3 to be the same. Due to the condition in (46), $V_{\rm EC1}$ and $V_{\rm EC2}$ are equal. Therefore, the mismatch between I_{C1} and I_{C2} due to V_A is removed with the topology of the proposed reference. The voltage-mode references in [12] and [15] do not have the same collector-emitter voltages for *Q1* and *Q2*, so the collector currents I_{C1} and I_{C2} in each of these circuits will have errors due to the Early voltage.

IV. Design Optimization

A. Noise Optimization

In order to optimize the noise performance of the proposed design, the output noise of the circuit first needs to be analyzed. The output noise for the circuit can be calculated using the small-signal model with RMS noise sources shown in Fig. 8. The parasitic capacitances of transistors *Q1* and *Q2* are not included. The focus of this analysis is the low frequency output noise spectral density. If the total integrated output noise is desired, the parasitic capacitances would have to be included to determine the proper limits of integration from the noise bandwidth [1, pp. 768–773]. The amplifier is being treated as a noiseless amplifier with input-referred voltage (E_n) and current (I_n) noise sources [17, pp. 38–39].

The RMS noise spectral densities (Volts/$\sqrt{\rm Hz}$) of the resistors in Fig. 8 are [1, p. 720]

$$E_{\rm Rx} = \sqrt{4kT\,(\rm Rx)}, \quad x = 1, 2, 3a, 3b, 4. \quad (73)$$

Assuming *M0* is biased in weak inversion while being saturated ($V_{\rm SD0} > V_{\rm SG0} - |V_{\rm THP0}|$ and $V_{\rm SG0} < |V_{\rm THP0}|$), the RMS input-referred noise spectral density (Volts/$\sqrt{\rm Hz}$) of *M0* is the same as (6) with g_{m0} equal to (7). The current noise sources from *Q1* and *Q2* in Fig. 8 are

$$I_{nb1} = \sqrt{2q\left(\frac{I_{C1}}{\beta_1}\right) + \frac{K_1}{f}\left(\frac{I_{C1}}{\beta_1}\right)^a}, \quad (74)$$

$$I_{nc1} = \sqrt{2qI_{C1}}, \quad (75)$$

$$I_{nb2} = \sqrt{N\left(I_{nb2\_\rm unit}\right)^2} = \sqrt{2q\left(\frac{I_{C2}}{\beta_2}\right) + \left(\frac{1}{N^{a-1}}\right)\left[\frac{K_1}{f}\left(\frac{I_{C2}}{\beta_2}\right)^a\right]}, \quad (76)$$

$$I_{nc2} = \sqrt{2qI_{C2}}. \quad (77)$$

The currents I_{C1} and I_{C2} are the steady-state collector currents of transistors *Q1* and *Q2*. The noise sources are from separate devices in the circuit, so they are uncorrelated [1, p. 730]. Hence, the total RMS output noise spectral density $v_{\rm NT\_NEW}$ is the square root of the sum of the mean square contributions from

each RMS noise source in Fig. 8. The expression for $v_{\mathrm{NT\_NEW}}$ is given in (78) at the bottom of the page, where

$$Y_1 = g_{m1} R3a, \tag{79}$$

$$Y_2 = 1 + \frac{R2}{R1} + \frac{R2}{r_{\pi 1}}, \tag{80}$$

$$Y_3 = \left(\frac{g_{m1} r_{\pi 2}}{1 + g_{m2} r_{\pi 2}}\right)\left(1 + \frac{R4}{r_{\pi 2}}\right), \tag{81}$$

$$Y_4 = \left(\frac{g_{m1} r_{\pi 2}}{1 + g_{m2} r_{\pi 2}}\right)(1 - g_{m2} R4), \tag{82}$$

$$\begin{aligned} Y_D &= \left[Y_1 + \left(\frac{R3a}{R3b}\right) Y_3\right] - Y_2 \\ &= \left[g_{m1} R3a + \left(\frac{R3a}{R3b}\right)\left(\frac{g_{m1} r_{\pi 2}}{1 + g_{m2} r_{\pi 2}}\right)\left(1 + \frac{R4}{r_{\pi 2}}\right)\right. \\ &\quad \left. - \left(1 + \frac{R2}{R1} + \frac{R2}{r_{\pi 1}}\right)\right]. \end{aligned} \tag{83}$$

The RMS output noise spectral density in (78) can be reduced by maximizing Y_D while minimizing Y_1–Y_4. The relationship in (83) shows Y_D is maximized when

$$Y_1 + \left(\frac{R3a}{R3b}\right) Y_3 \gg Y_2. \tag{84}$$

Substituting (79)–(81) into (84) requires

$$g_{m1} R3a + \left(\frac{R3a}{R3b}\right)\left(\frac{g_{m1} r_{\pi 2}}{1 + g_{m2} r_{\pi 2}}\right)\left(1 + \frac{R4}{r_{\pi 2}}\right) \gg 1 + \frac{R2}{R1} + \frac{R2}{r_{\pi 1}} \tag{85}$$

in order for Y_D to be maximized. The quantity $R2/R1$ is equal to $1/\mathrm{M_{NEW}}$ from (49). M_{NEW} is fixed for the design since it is used to minimize the TC of the reference voltage in (48). Therefore, this quantity cannot be adjusted to achieve the condition in (85). From (41), (44), and (46),

$$R3a = \frac{V_{\mathrm{REF\_NEW}}}{I_{C1}} \tag{86}$$

and

$$R3b = \frac{V_{\mathrm{REF\_NEW}}}{I_{C2}\left(1 + \frac{1}{\beta_2}\right)}. \tag{87}$$

Substitution of (86) and (87) into (85) and representing g_{m1}, g_{m2}, $r_{\pi 1}$, and $r_{\pi 2}$ in (85) in terms of collector currents I_{C1} and I_{C2} produces the following condition when Y_D is maximized:

$$V_{\mathrm{REF\_NEW}} - \left(\frac{V_T}{\mathrm{M_{NEW}}}\right) \gg R2\left(\frac{I_{C1}}{\beta_1}\right) - R4\left(\frac{I_{C2}}{\beta_2}\right). \tag{88}$$

Substitution of (37), (47), and (49) into (88) yields

$$I_{B2} \gg \frac{V_{\mathrm{REF\_NEW}}}{R3b} - \left(\frac{V_{\mathrm{REF\_NEW}}}{R3a}\right) \times N \exp\left[\left(\frac{1}{\mathrm{M_{NEW}}}\right)\left(\frac{V_{\mathrm{EB1}}}{V_T} - 1\right)\right]. \tag{89}$$

Using (86) and (87) in (89) provides the following condition which needs to be met in order for (84) to be valid:

$$I_{C1} \gg \left(\frac{I_{C2}}{N}\right) \exp\left[-\left(\frac{1}{\mathrm{M_{NEW}}}\right)\left(\frac{V_{\mathrm{EB1}}}{V_T} - 1\right)\right]. \tag{90}$$

Under these conditions, Y_D will be maximized such that all of the scale factors for the noise terms in (78) will be reduced.

Although the RMS output noise spectral density of the proposed reference can be reduced by meeting the condition in (90), it requires the collector current in *Q1* to be considerably larger than the collector current in *Q2*. This might cause problems for the circuit to operate at supply voltages down to 1 V. The KVL equation around the branch containing *Q1* in Fig. 7 is

$$V_{\mathrm{DD}} = \left(\frac{R2}{R1} + 1\right) V_{\mathrm{EB1}} + I_{B1} R2 + V_{\mathrm{SD0,sat}}. \tag{91}$$

If the maximum saturation voltage of current source *M0* over temperature is 200 mV and I_{B1} is negligible, the condition which needs to be met in order for the reference to operate with a 1-V supply is $V_{\mathrm{EB1,max}} \leq 0.8$ V. The limit for I_{C1} is thus

$$I_{C1} \leq I_{S1} \exp\left(\frac{0.8}{V_T}\right). \tag{92}$$

If I_{C1} is set to meet (92) but does not meet (90), then Y_D in (78) will not be maximized. If this is the situation, the current noise terms in (78) that are multiplied by $R2^2$, $R3a^2$, and $R3b^2$ can be reduced by decreasing the values of these resistors. A reduction in *R2* also reduces the values of *R4* and *R1* due to (37) and (49), respectively. By decreasing these resistors, the thermal noise voltages of these components are also reduced due to (73). Therefore, the RMS output noise spectral density of the proposed reference can be greatly reduced by decreasing the values of the resistors in the circuit. In order to compare the noise performance of the proposed reference with the ones from the circuits in Figs. 2 and 4, the power of the proposed reference needs to be analyzed. This is done in the next section.

B. Power Optimization

It was shown in the previous section that the RMS output noise spectral density of the proposed reference can be reduced by decreasing the values of the resistors in the circuit. However, the reduction in the resistors impacts the power consumed by the circuit. The power consumption of the proposed reference

$$v_{\mathrm{NT\_NEW}} = \left(\frac{1}{Y_D}\right) \sqrt{\begin{array}{c} Y_1^2\left[\left(E_{R1}\left(\frac{R2}{R1}\right)\right)^2 + E_{R2}^2 + E_{R4}^2 + \left(I_{nb1} R2\right)^2\right] + Y_2^2\left[E_{R3a}^2 + \left(I_{nc1} R3a\right)^2 + \left(\frac{E_{g0}}{A_v}\right)^2 + E_n^2\right] \\ + Y_3^2\left[\left(E_{R3b}\left(\frac{R3a}{R3b}\right)\right)^2 + \left(I_{nc2} R3a\right)^2\right] + Y_4^2\left(I_{nb2} R3a\right)^2 + \left(Y_2 + Y_3\right)^2 \left(I_n R3a\right)^2 \end{array}} \tag{78}$$

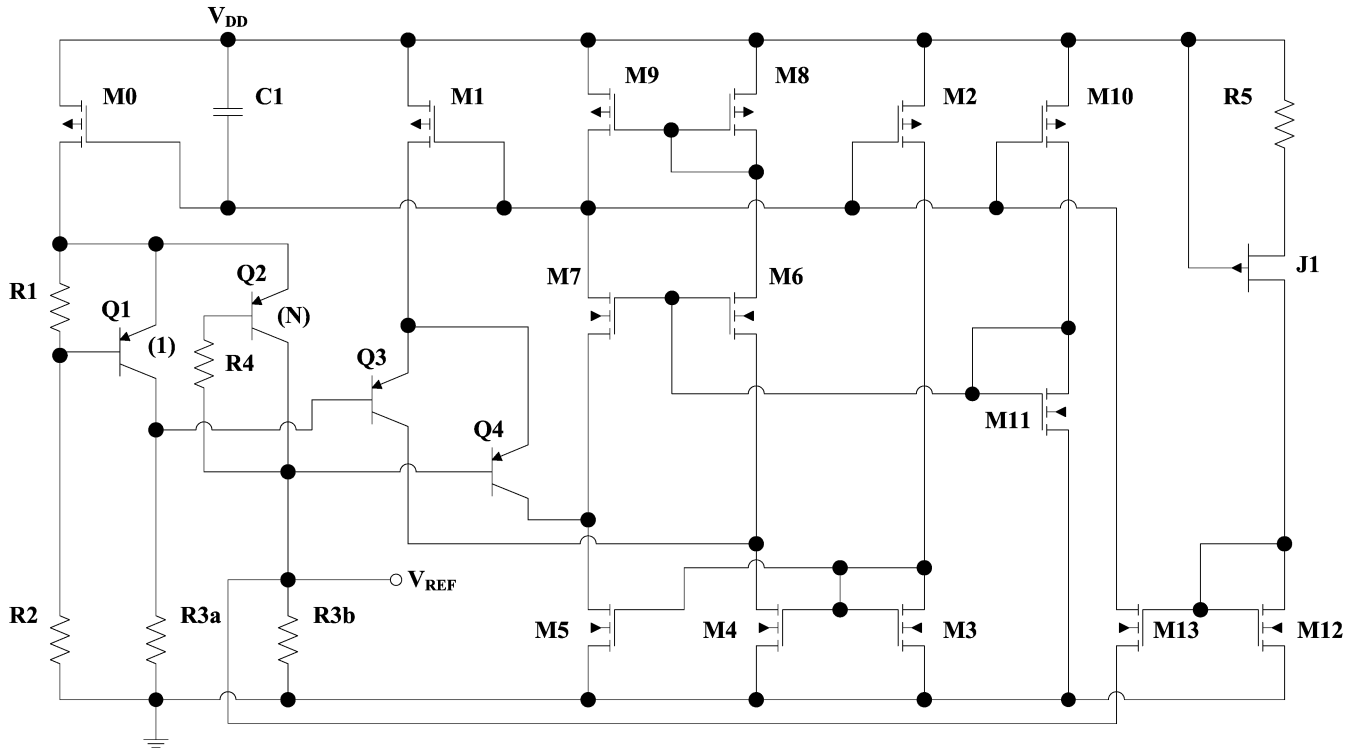


Fig. 9. Circuit schematic of the proposed voltage reference.

can be explained with the circuit in Fig. 7. The total current consumed by the reference is

$$I_{\mathrm{TOTAL}} = I_{\mathrm{M0}}\,(1+H) \tag{93}$$

where H is a factor which takes into account the bias current of the amplifier that is mirrored from the current source *M0*. The current supplied to the reference core from *M0* is

$$I_{\mathrm{M0}} = I_1 + I_{E1} + I_{E2}. \tag{94}$$

The value of I_1 can be determined by the KVL equation around resistor *R1* and the base-emitter junction of *Q1*. The result from the KVL equation is $I_1 = V_{\mathrm{EB1}}/R1$. The emitter current of *Q1* is just the sum of I_{C1} and I_{B1}. The result in terms of I_{C1} is $I_{E1} = I_{C1}\,(1 + (1/\beta_1))$. By using the value of I_{C1} in (86), I_{E1} can be expressed as

$$I_{E1} = \left(\frac{V_{\mathrm{REF\_NEW}}}{R3a}\right)\left(1+\frac{1}{\beta_1}\right). \tag{95}$$

Similarly

$$I_{E2} = \frac{V_{\mathrm{REF\_NEW}}}{R3b}. \tag{96}$$

By using the results from (94)–(96), the total current consumed by the reference is

$$I_{\mathrm{TOTAL}} = (1+H) \times \left(\frac{V_{\mathrm{EB1}}}{R1} + \frac{V_{\mathrm{REF\_NEW}}}{R3b}\left[1+\frac{R3b}{R3a}\left(1+\frac{1}{\beta_1}\right)\right]\right). \tag{97}$$

The total power consumption of the proposed reference is the supply voltage (V_{DD}) multiplied by the total current consumption or

$$P_{\mathrm{TOTAL}} = V_{\mathrm{DD}}\,(1+H) \times \left(\frac{V_{\mathrm{EB1}}}{R1} + \frac{V_{\mathrm{REF\_NEW}}}{R3b}\left[1+\frac{R3b}{R3a}\left(1+\frac{1}{\beta_1}\right)\right]\right). \tag{98}$$

The value of $V_{\mathrm{REF\_NEW}}$ is approximately 200 mV from (48) regardless of the DC current values in the circuit. Furthermore, $V_{\mathrm{EB1}} \propto \ln(I_{C1})$, which indicates V_{EB1} will not increase too much as I_{C1} is increased. Since the voltages in (98) remain relatively constant, reducing the values of resistors *R1*, *R3a*, and *R3b* in order to reduce the RMS output noise spectral density of the reference will increase the power consumption. This would exclude the use of the circuit in low-power applications.

If the proposed reference has the same current consumption as the circuit in Fig. 4, the value of I_{C1V} in (25) will be higher than $I_{C1} \approx I_{C2} \approx V_{\mathrm{REF\_NEW}}/R3b$ in the proposed reference by a factor of 2 if β_1 is large and $R3a = R3b$ in (97). Since $Y_D \propto I_{C1}$ due to g_{m1} in (83), the total RMS output noise of the proposed reference in (78) will not be reduced as much as the output noise from the circuit in Fig. 4 based on the discussion in Section II-B. Hence, the output noise of the proposed reference is expected to be slightly higher than the circuit in Fig. 4 under these circumstances. However, the output noise of the proposed reference will be lower than the noise of the circuit in Fig. 2 since the signal from the core does not have to go through a PFET current mirror. It was shown in (5) that the PFET current mirror amplifies the noise from the core of the circuit in Fig. 2 to the output node by $g_{m2}R4$. This does not occur in the proposed reference.

V. Experimental Results

The schematic of the proposed reference is shown in Fig. 9. The reference core consists of resistors *R1–R4*, PNP devices *Q1* and *Q2*, and PFET current source *M0*. *Q1* is one unit PNP cell while *Q2* is made up of 24 unit PNP cells. Therefore, the ratio of the *Q2* emitter area to the *Q1* emitter area is $N = 24$. This ratio allows *Q1* and *Q2* to be placed in a (5 unit cell) $\times$ (5 unit cell) common-centroid layout on the test chip with *Q1* in the center. The values of resistors *R1–R4* were selected such that the current consumed by the entire reference circuit would be 20 μA at room temperature. This level of current consumption is similar to other sub-1-V references in literature. Furthermore, the current level allowed an acceptable level of output noise while keeping the area occupied by the resistors on the test chip to a minimum.

The amplifier used to force the collectors of *Q1* and *Q2* to be at the same potential is a folded-cascode operational transconductance amplifier (OTA). It consists of the differential PNP input pair *Q3*, *Q4* along with the folded-cascode structure formed by the NFET cascode current sinks *M4–M7* and PFET current mirror *M8, M9*. The bias currents for the amplifier are derived by mirroring current from *M0* to devices *M1*, *M2*, and *M10*. The tail current for the differential input pair comes from *M1*, while *M2* and *M3* mirror current to the current sinks *M4* and *M5*. The bias voltage for the cascode devices *M6* and *M7* is created by the PFET current source *M10* and the diode-connected NFET transistor *M11*. In order for the circuit to be stable, the loop gain ($A_{\rm OL}(s)$) formed by the OTA, *M0*, and the branches containing *Q1*, *R3a* and *Q2*, *R4*, *R3b* should have sufficient phase margin so the loop gain does not change sign when the magnitude approaches 0 dB [10, pp. 564–568]. The compensation capacitor *C1* in Fig. 9 sets the dominant pole ω_0 at the output of the OTA. Since ω_0 is lower in frequency than the other poles and zeroes in the circuit, $A_{\rm OL}(s)$ rolls off at 20 dB/decade for frequencies above ω_0 and achieves the necessary phase margin for stability.

The start-up circuit for the reference in Fig. 9 consists of resistor *R5*, junction FET *J1*, and NFET current mirror *M12*, *M13*. Once the supply voltage is applied to the circuit, current begins to flow through *R5–J1–M12*. This current is then mirrored from *M12* to *M13*. Device *M13* pulls down on the output of the amplifier while pulling up on the negative input of the amplifier. This creates the positive feedback loop which allows current to flow in the reference core and amplifier. As the reference output voltage increases, the gate-source voltage ($V_{\rm GS13}$) of *M13* decreases. Once the reference voltage increases to the point where $V_{\rm GS13} \ll V_{\rm THN13}$, *M13* shuts off softly to not affect the operation of the reference circuit. In order to minimize the continuous current ($I_{\rm STARTUP}$) flowing through *R5–J1–M12* and control the amount of current injected into the circuit during start-up, the gate of *J1* is connected to the supply ($V_{\rm DD}$) in order for it to act like a voltage-controlled resistor (R_{J1}). The current through *R5–J1–M12* is

$$I_{\rm STARTUP} = \frac{V_{\rm DD} - V_{\rm GS12}}{R5 + R_{J1}} \tag{99}$$

where $V_{\rm GS12}$ is the gate-source voltage of *M12*. As $V_{\rm DD}$ increases, R_{J1} increases. This allows $I_{\rm STARTUP}$ to stay at a reasonable value and control the start-up injection current as $V_{\rm DD}$ increases.

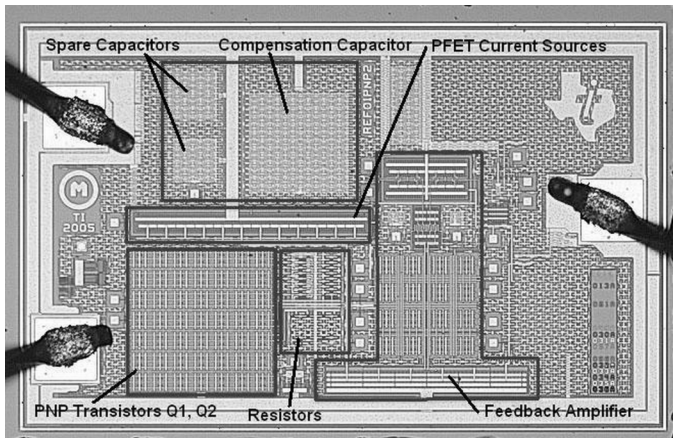


Fig. 10. Chip micrograph of the proposed voltage reference.

The test chip of the proposed voltage reference was fabricated with a 0.5-μm BiCMOS process [14]. Lateral PNP transistors were used to construct *Q1–Q4* in Fig. 9, since the transconductances of these devices are larger than the transconductances of PFET devices for the same size and bias currents. Furthermore, the flicker and flat-band noise of bipolar devices is lower than FET devices of the same size and bias currents [11, p. 19]. Another component available in the process is a P-channel JFET. This component was used for *J1* in the start-up circuit of the proposed reference. Devices *M0–M11* were implemented with standard $V_{\rm THN}$ (threshold voltage) NFETs and standard $V_{\rm THP}$ PFETs with nominal threshold voltages of $+0.6$ V and -0.8 V, respectively. Devices *M12* and *M13* are natural or low $V_{\rm THN}$ NFETs with nominal threshold voltages of $+0.3$ V. The source of *M13* is connected to $V_{\rm REF}$ in Fig. 9. Once the circuit starts up, $V_{\rm REF}$ is approximately 200 mV. Since the nominal threshold voltage of *M13* is $+0.3$ V, *M13* is essentially in cutoff once the reference circuit starts up. If *M12* and *M13* were standard $V_{\rm THN}$ NFETs, *M13* would still be on after the reference circuit starts up. The micrograph of the test chip is shown in Fig. 10. The major blocks in the chip micrograph, such as the amplifier; PFET current sources *M0–M2*, *M10*; and bipolar transistors *Q1*, *Q2* are labeled. The total die area of the test chip is around 0.4 mm^2. This includes the seal ring and the bond pads with associated ESD cells for the supply pin (right-hand side of the chip micrograph), the ground pin (upper left-hand side of the chip micrograph), and the reference output pin.

A total of 32 test chips from one wafer lot were assembled in open-cavity 8-pin ceramic dual in-line packages (CerDIPs). The units were characterized over supply voltage and temperature in order to collect data for the untrimmed reference output voltage, the untrimmed temperature coefficient, low-frequency output noise spectral density, and line regulation. The distribution of the measured untrimmed reference output voltage at room temperature with a 1-V supply is shown in Fig. 11. Based on the data collected, the reference voltage has a mean value of 190.91 mV with a 3σ variation of 1.083 mV. This means the distribution of the untrimmed error in the reference voltage is less than $\pm 0.6\%$. Based on the data, the mismatch in the zero-bias

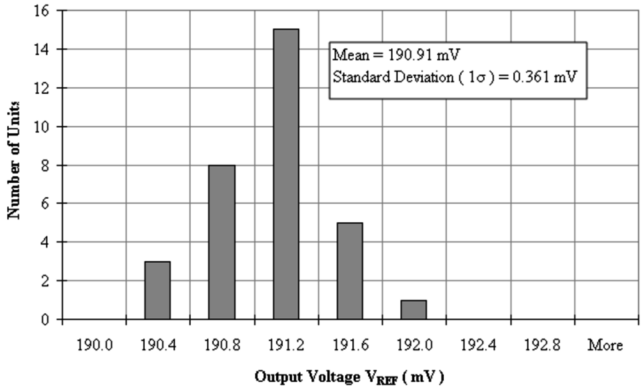


Fig. 11. Measured untrimmed reference voltage distribution at room temperature.

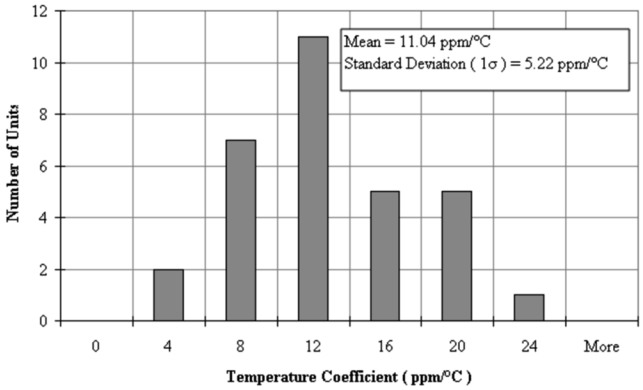


Fig. 12. Measured untrimmed temperature coefficient distribution.

threshold voltages of the current sinks *M4* and *M5* in Fig. 9 had the highest contribution to the variation in the untrimmed reference output voltage.

The distribution of the measured untrimmed TC with a 1-V supply is shown in Fig. 12. Each unit was drifted from $-40\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$. The TC (units of ppm/°C) for each chip was calculated using the box method which is [1, p. 343]

$$\mathrm{TC} = \frac{1}{V_{\mathrm{REF\_NOM}}}\left(\frac{V_{\mathrm{REF\_MAX}} - V_{\mathrm{REF\_MIN}}}{T_{\mathrm{MAX}} - T_{\mathrm{MIN}}}\right) \qquad (100)$$

where $V_{\mathrm{REF\_NOM}}$ is the reference voltage at room temperature ($T_{\mathrm{NOM}} = 27\,^{\circ}\mathrm{C}$), $V_{\mathrm{REF\_MAX}}$ and $V_{\mathrm{REF\_MIN}}$ are the maximum and minimum reference voltages over the temperature drift range, and T_{MAX} and T_{MIN} are the maximum and minimum temperatures used to drift the chips. The measurements show the proposed reference has a mean TC of 11.04 ppm/°C with a standard deviation (1σ) of 5.22 ppm/°C. The measured mean TC of the proposed reference is less than the values documented for the sub-1-V reference circuits in [6] (version without second-order curvature correction) and [7], [8], [12].

The measurement and simulation results of the output noise spectral density at room temperature and 1-V supply for the proposed reference are presented in Fig. 13. The measurement results closely match the simulation results. The flat-band noise spectral density is 40 nV/$\sqrt{\mathrm{Hz}}$, and the $1/\mathrm{f}$ corner frequency is 20 Hz.

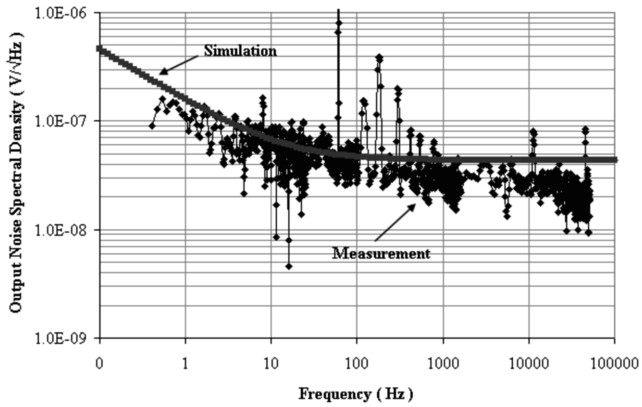


Fig. 13. Measurement and simulation results of output noise spectral density.

The total peak-to-peak output noise between 0.1 and 10 Hz was measured using the test circuit shown in Fig. 14. The output of the bandpass filter in Fig. 14 was connected to an oscilloscope with a minimum resolution of 2 mV/division. Since the simulated peak-to-peak output noise from 0.1 to 10 Hz is less than 5 μV, the gain of 100.9 V/V from the bandpass filter would not amplify the noise from the proposed reference within the resolution of the oscilloscope. Hence, the 200-mV output from the reference needed to be amplified prior to running it through the bandpass filter. If the 200-mV output from the reference is amplified by 100 V/V, the amplified output would be 20 V. Since the operational amplifiers used to amplify the signal in Fig. 14 were powered with the maximum specified supply voltages of ± 15 V, the output of the operational amplifiers would be driven to the $+15$-V rail. In order to circumvent this problem while amplifying the output noise of the reference, a high-input impedance difference amplifier was used along with two reference test chips. As shown in Fig. 11, the untrimmed reference voltage at room temperature has a 3σ variation less than 2 mV. Hence, a 2-mV difference between Reference #1 and Reference #2 in Fig. 14 can be amplified by 100 V/V with a difference amplifier using ± 15-V supplies without any problems. The gain (A_{diff}) of the difference amplifier in Fig. 14 was set to $A_{\mathrm{diff}} = (1 + R2/R1) = 101$ V/V. Since the bandpass filter has a gain (A_{bandpass}) of 100.9 V/V, the output noise of the reference test chips will be amplified by a total gain (A_{total}) of $A_{\mathrm{total}} = A_{\mathrm{diff}} A_{\mathrm{bandpass}} = 10190.9$ V/V. The measured peak-to-peak output noise ($v_{\mathrm{p2p\_total}}$) of this configuration is shown in Fig. 15. The value of the total peak-to-peak output noise of the two reference chips, the difference amplifier, and the bandpass filter is $v_{\mathrm{p2p}\_total} \approx 60$ mV. Thus, the peak-to-peak output noise of one reference test chip ($v_{\mathrm{p2p\_vref}}$) can be obtained from

$$v_{\mathrm{p2p\_total}}^2 = v_{\mathrm{p2p\_noref}}^2 + 2\left(A_{\mathrm{total}} v_{\mathrm{p2p\_vref}}\right)^2 \qquad (101)$$

where $v_{\mathrm{p2p\_noref}} \approx 8$ mV is the peak-to-peak output noise contributed from just the difference amplifier and bandpass filter. The reason why the term $(A_{\mathrm{total}} v_{\mathrm{p2p\_vref}})^2$ in (101) is multiplied by a factor of 2 is two reference test chips were used for the peak-to-peak output noise measurement. Since

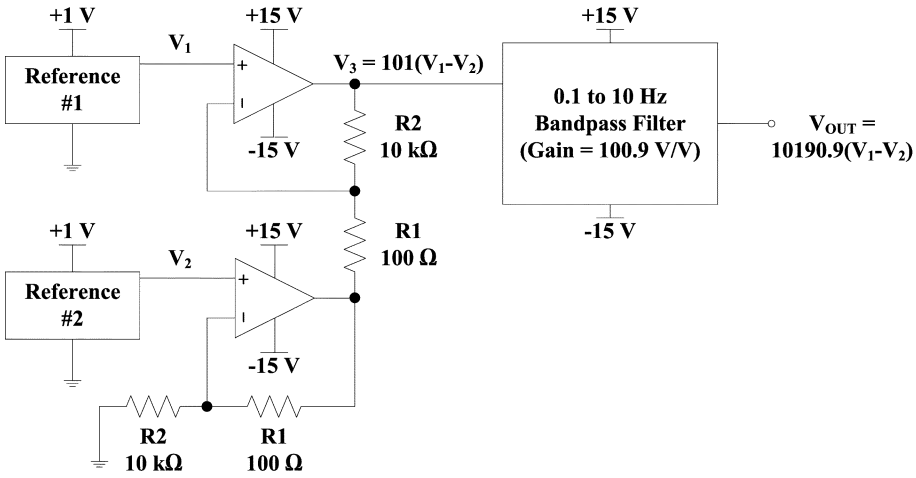


Fig. 14. Test circuit for measuring total peak-to-peak output noise from 0.1 to 10 Hz.

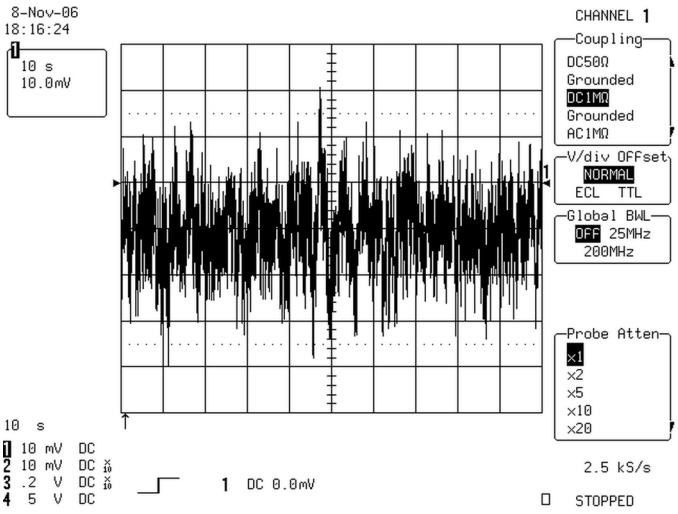


Fig. 15. Total peak-to-peak output noise of the test system in Fig. 14.

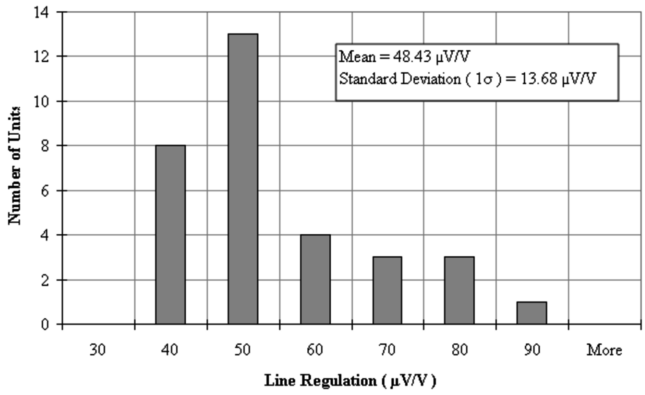


Fig. 16. Measured line regulation distribution at room temperature.

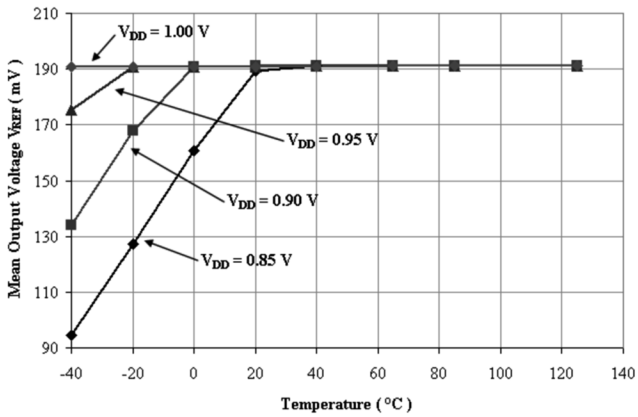


Fig. 17. Mean output voltage over temperature for various supply voltages.

the noise from these two test chips is uncorrelated, the mean square of the peak-to-peak output noise from each one can be added together. By using the results from these measurements along with (101), the value of $v_{\mathrm{p2p\_vref}}$ is determined to be 4.126 μV.

The distribution of the measured line regulation from 1 to 5 V at room temperature is shown in Fig. 16. From Fig. 16, the proposed reference has a mean line regulation of 48.43 μV/V or less than -86 dB. The measured mean line regulation of the proposed reference is less than the values documented for the sub-1-V reference circuits in [6]–[8], [12]. Furthermore, the supply voltage range used for the measurements exceeds the ranges used in the prior arts. Since the proposed reference can operate with supply voltages between 1 and 5 V, it can be used in a multitude of applications with a wide range of supply voltages without requiring a separate regulator circuit.

Measurements of the mean reference output voltage over the $-40\,^{\circ}$C to $+125\,^{\circ}$C temperature range for various supply voltages are shown in Fig. 17. The minimum supply voltage ($V_{\mathrm{DD,min}}$) for the reference occurs when the mean output voltage stays relatively constant over the entire temperature range. As shown in Fig. 17, $V_{\mathrm{DD,min}}$ is 1 V. The measurements of the minimum supply voltage over the $-40\,^{\circ}$C to $+125\,^{\circ}$C temperature range support the analysis in Section III. Moreover, the reference can operate with supply voltages less than 1 V as shown in Fig. 17 if the temperature range is reduced.

TABLE I
COMPARISON OF LOW VOLTAGE REFERENCES AT 1-V SUPPLY

	This work	[6]	[7]	[8]	[12]
Technology	0.5-μm BiCMOS	0.8-μm BiCMOS	0.6-μm CMOS	0.6-μm CMOS	0.18-μm CMOS
TC (ppm/°C)	11 (-40 to +125 °C)	20[a] (0 to +80 °C)	15 (0 to +100 °C)	36.9 (0 to +100 °C)	63[b] (-20 to +100 °C)
Line Regulation (μV/V)	48 (1.0 to 5.0 V)	114 (0.95 to 2.0 V)	4231[c] (0.98 to 1.5 V)	256.73[d] (1.4 to 3.0 V)	1100 (0.95 to 2.5 V)
Noise Density @ 100Hz (nV/√Hz)	40	N/A	N/A	152 (C_{OUT} = 100 nF)	N/A
$V_{REF} \pm 3\sigma$ (mV)	190.9 ± 1.083	536	603	309.31 ± 19.26	169.4
Minimum Supply (V)	1.0[e]	0.95	0.98	1.4	0.95
Supply Current (μA)	20	92	18	9.7 (max)	2.4

a. Without curvature correction.
b. Converted from 0.76 % to 63 ppm/°C with V_{REF} = 169.4 mV.
c. Converted from 2.2 mV over supply range to 4231 μV/V.
d. Converted from 0.083 %/V to 256.73 μV/V with V_{REF} = 309.31 mV.
e. Minimum supply voltage at -40 °C.

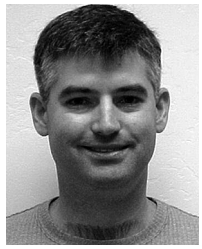
A summary of the measurement results for the proposed reference along with a comparison of performance between other sub-1-V references is shown in Table I. The results show the proposed reference out-performs the competition in almost every category.

VI. CONCLUSION

A voltage reference with a 190.91 mV ± 1.083 mV (3σ) output and a mean TC of 11.04 ppm/°C from −40 °C to +125 °C with a 1-V supply, 20-μA static current is presented. Besides having excellent TC and untrimmed accuracy, the output noise is very low without the need for external filter capacitors. The flat-band output noise spectral density is 40 nV/$\sqrt{}$Hz with a corner frequency of 20 Hz. Furthermore, the peak-to-peak output noise from 0.1 to 10 Hz is 4 μV. Moreover, the proposed reference has a typical line regulation of −86 dB. Finally, the topology of the circuit allows it to be portable to several different processes such as BiCMOS and CMOS with minimal re-design effort.

REFERENCES

[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley, 1993.
[2] R. J. Widlar, "New developments in IC voltage regulators," *IEEE J. Solid-State Circuits*, vol. SC-6, no. 1, pp. 2–7, Feb. 1971.
[3] K. E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SC-8, no. 3, pp. 222–226, Jun. 1973.
[4] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 388–393, Dec. 1974.
[5] H. Banba *et al.*, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.
[6] P. Malcovati *et al.*, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1076–1081, Jul. 2001.
[7] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.
[8] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 146–150, Jan. 2003.
[9] E. A. Vittoz, "Very low power circuit design: Fundamentals and limits," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'93)*, May 1993, vol. 2, pp. 1439–1442.
[10] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. New York: Wiley-IEEE Press, 1998.
[11] V. V. Ivanov and I. M. Filanovsky, *Operational Amplifier Speed and Accuracy Improvement*. Boston, MA: Kluwer, 2004.
[12] H. Lin and C.-J. Liang, "A sub-1 V bandgap reference circuit using subthreshold current," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'05)*, May 2005, vol. 5, pp. 4253–4256.
[13] K. E. Sanborn, "A sub-1V low-noise bandgap voltage reference," M.S.E.E. thesis, Univ. Arizona, Tucson, AZ, 2006.
[14] K. E. Sanborn, D. Ma, and V. V. Ivanov, "A sub-1-V low-noise bandgap voltage reference," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC'06)*, Sep. 2006, pp. 607–610.
[15] R. Widlar, "Low voltage techniques," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, pp. 838–846, Dec. 1978.
[16] W. T. Holman and J. A. Connelly, "A compact low noise operational amplifier for a 1.2 μm digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 30, no. 6, pp. 710–714, Jun. 1995.
[17] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*. New York: Wiley, 1993.



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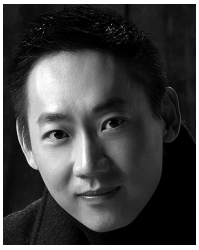

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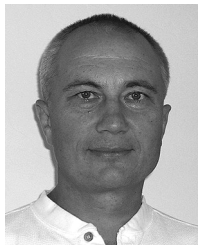
Dr. Ma is a senior member of IEEE and a member of ASEE. He serves as technical committee member and session chair in several premier technical conferences including IEEE ISCAS, IEEE ISQED, and IEEE/ACM ISLPED.



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