TPS62660 1000-mA, 6-MHz High-Efficiency Step-Down Converter in Chip Scale Packaging

1 Features

- 91% Efficiency at 6-MHz Operation
- 31-µA Quiescent Current
- Wide V_{IN} Range from 2.3 V to 5.5 V
- 6-MHz Regulated Frequency Operation
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Automatic PFM or PWM Mode Switching
- Low Ripple Light-Load PFM Mode
- Fast Turnon Time: < 60-µs Start-Up Time
- Integrated Active Power-Down Sequencing (Optional)
- Current Overload and Thermal Shutdown Protection
- Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Complete Sub 1-mm Component Profile Solution
- Total Solution Size <12 mm^2
- Available in a 6-Pin NanoFree™ (DSBGA)

2 Applications

- Cell Phones and Smart Phones
- PDAs and Pocket PCs
- Portable Hard Disk Drives
- DC-DC Micro Modules

3 Description

The TPS6266x device is a high-frequency synchronous step-down DC-DC converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS6266x supports up to 1000-mA peak load current, and allows the use of low-cost chip inductor and capacitors.

With a wide input voltage range of 2.3 V to 5.5 V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 1.2 V to 2.3 V.

The TPS6266x operates at a regulated 6-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 31 µA (typical) during light load and standby operation. For noise-sensitive applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA.

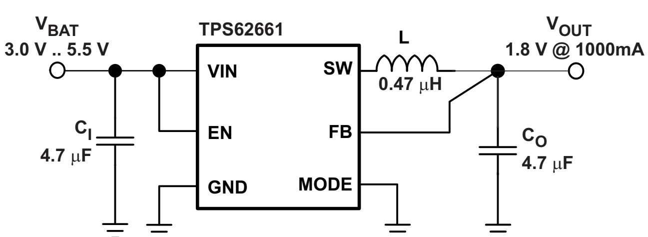
The TPS6266x is available in an 6-pin chip scale package (DSBGA).

Device Information(1)

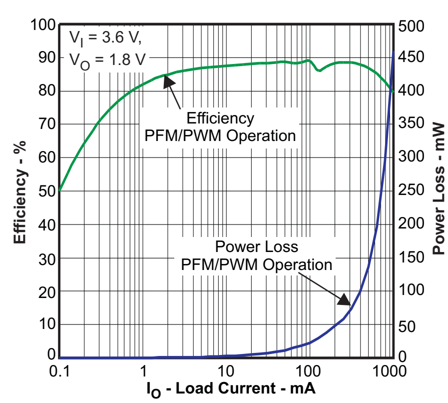
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62660	DSBGA (6)	1.30 mm × 0.93 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Smallest Solution Size Application



Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2011) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Removed *Ordering Information* table; see POA at the end of the data sheet 1

Changes from Revision B (September 2010) to Revision C **Page**

- Changed in ELEC CHARA table, Shutdown current row, Max from 1 to 2.5 4

Changes from Revision A (March 2010) to Revision B **Page**

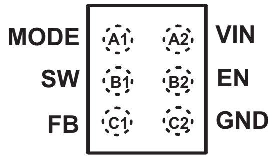
- Deleted " Product Preview " footnote associated with TPS62665YFF device 1

Changes from Original (February 2010) to Revision A **Page**

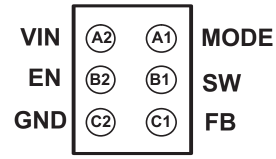
- Deleted Product Preview banner for device release to production. 1

5 Pin Configuration and Functions

YFF Package
6-Pin DSBGA
Top View



YFF Package
6-Pin DSBGA
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the output of the converter.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C2	—	Ground pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Voltage at VIN, SW(2)	–0.3	7	V
	Voltage at FB(2)	–0.3	3.6	V
	Voltage at EN, MODE (2)	–0.3	V_I + 0.3	V
I_O	Peak output current		1000	mA
	Power dissipation	Internally limited		
T_A	Operating temperature(3)	–40	85	°C
T_J (max)	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1000	
		Machine model (MM)	±200	

(1) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Supply voltage	2.3		5.5	V
IOUT	Maximum output current			1000	mA
	Effective inductance	0.3	0.47	1.3	µH
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS626xx YFF (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum values are at V_I = 2.3 V to 5.5 V, V_O = 1.8 V, EN = 1.8 V, AUTO mode and T_A = –40°C to 85°C; circuit in the *Parameter Measurement Information* (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 1.8 V, EN = 1.8 V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.3		5.5	V
I_Q	Operating quiescent current		I_O = 0 mA. Device not switching		31	55	µA
			I_O = 0 mA, PWM mode		7.6		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	2.5	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage			1			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET ON-resistance	TPS6266x	V_I = $V_{(GS)}$ = 3.6 V, PWM mode		270		mΩ
			V_I = $V_{(GS)}$ = 2.5 V, PWM mode		350		
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5 V, –40°C ≤ T_J ≤ 85°C			1	µA

Electrical Characteristics (continued)

Minimum and maximum values are at V_I = 2.3 V to 5.5 V, V_O = 1.8 V, EN = 1.8 V, AUTO mode and T_A = –40°C to 85°C; circuit in the *Parameter Measurement Information* (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 1.8 V, EN = 1.8 V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	N-channel MOSFET ON-resistance	TPS6266x	$V_I = V_{(GS)}$ = 3.6 V, PWM mode		140		mΩ
			$V_I = V_{(GS)}$ = 2.5 V, PWM mode		200		
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5 V, –40°C ≤ T_J ≤ 85°C			2	µA
r_{DIS}	Discharge resistor for power-down sequence	TPS62665			15	50	Ω
	P-MOS current limit		2.3 V ≤ V_I ≤ 4.8 V, open loop	1400	1500	1750	mA
	Input current limit under short-circuit conditions		V_O shorted to ground		19		mA
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS6266x	I_O = 0 mA, PWM mode	5.4	6	6.6	MHz
OUTPUT							
$V_{(OUT)}$	Regulated DC output voltage	TPS6266x	2.3 V ≤ V_I ≤ 2.7 V, 0 mA ≤ I_O ≤ 600 mA 2.7 V ≤ V_I ≤ 3 V, 0 mA ≤ I_O ≤ 800 mA 3 V ≤ V_I ≤ 4.8 V, 0 mA ≤ I_O ≤ 1000 mA PFM/PWM operation	0.98 × V_{NOM}	V_{NOM}	1.03 × V_{NOM}	V
			3 V ≤ V_I ≤ 5.5 V, 0 mA ≤ I_O ≤ 1000 mA PFM/PWM operation	0.98 × V_{NOM}	V_{NOM}	1.04 × V_{NOM}	
			2.3 V ≤ V_I ≤ 2.7 V, 0 mA ≤ I_O ≤ 600 mA 2.7 V ≤ V_I ≤ 3 V, 0 mA ≤ I_O ≤ 800 mA 3 V ≤ V_I ≤ 5.5 V, 0 mA ≤ I_O ≤ 1000 mA PWM operation	0.98 × V_{NOM}	V_{NOM}	1.02 × V_{NOM}	
	Line regulation		$V_I = V_O$ + 0.5 V (min 2.3 V) to 5.5 V, I_O = 200 mA		0.13		%/V
	Load regulation		V_I = 3.6 V, I_O = 0 mA to 1000 mA		–0.00025		%/mA
	Feedback input resistance			480			kΩ
ΔV_O	Power-save mode ripple voltage	TPS62660	I_O = 1 mA		20		mV_{PP}
		TPS62661	I_O = 1 mA L = 1 µH (muRata LQM2MPN1R0NG0) C_O = 10 µF, 4 V 0402 (muRata GRM155R60G106M)		9		
		TPS62665	I_O = 1 mA		24		
	Start-up time	TPS62660	I_O = 0 mA, time from active EN to V_O		120		µs
		TPS62661	R_L = 2 Ω, time from active EN to V_O		55		

6.6 Dissipation Ratings(1)

PACKAGE	$R_{\theta JA}$ (2)	$R_{\theta JB}$ (2)	POWER RATING T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
YFF-6	125°C/W	53°C/W	800 mW	8 mW/°C

(1) Maximum power dissipation is a function of T_J(max), $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)-T_A] / R_{\theta JA}$.
(2) This thermal data is measured with high-K board (4-layer board according to JESD51-7 JEDEC standard).

6.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs load current	Figure 1, Figure 2, Figure 3, Figure 4
		vs input voltage	Figure 5
	Peak-to-peak output ripple current	vs load current	Figure 6, Figure 7

Typical Characteristics (continued)

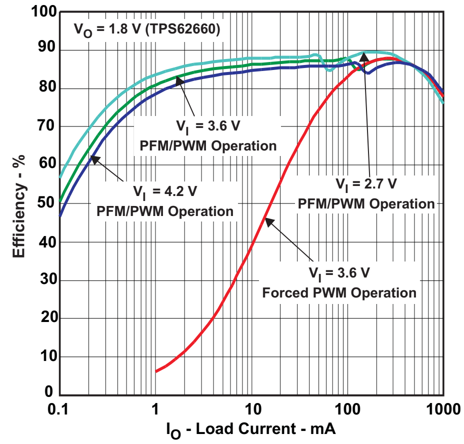


Figure 1. Efficiency vs Load Current

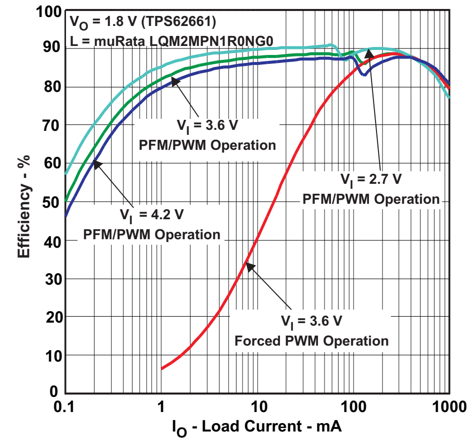


Figure 2. Efficiency vs Load Current

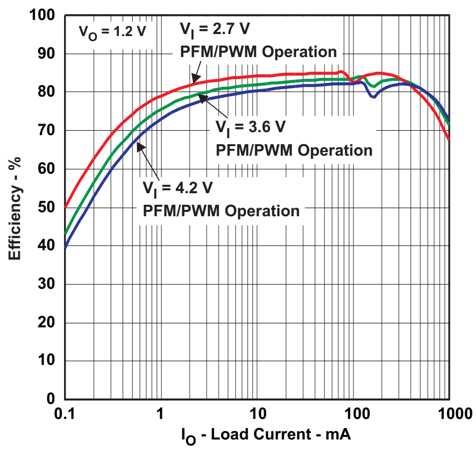


Figure 3. Efficiency vs Load Current

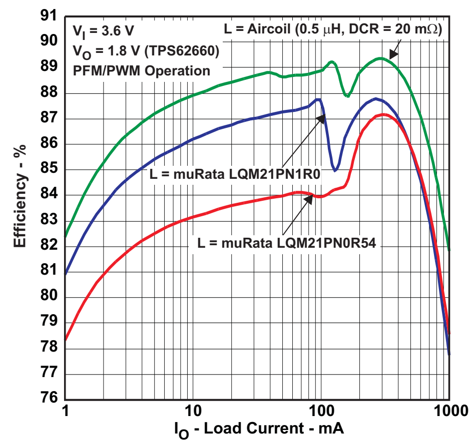


Figure 4. Efficiency vs Load Current

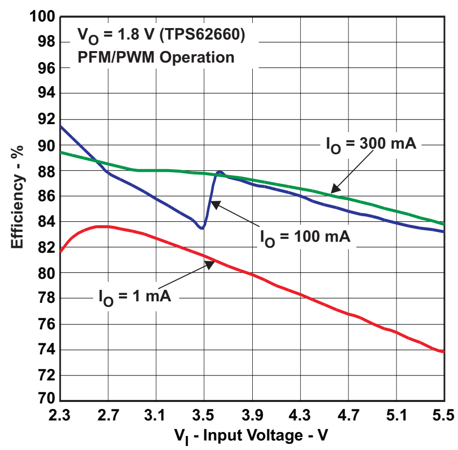


Figure 5. Efficiency vs Input Voltage

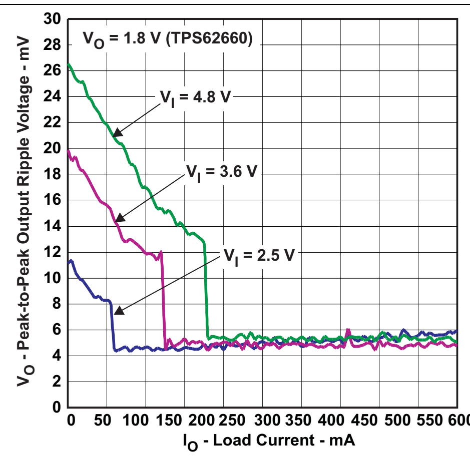


Figure 6. Peak-to-Peak Output Ripple Voltage vs Load Current

Typical Characteristics (continued)

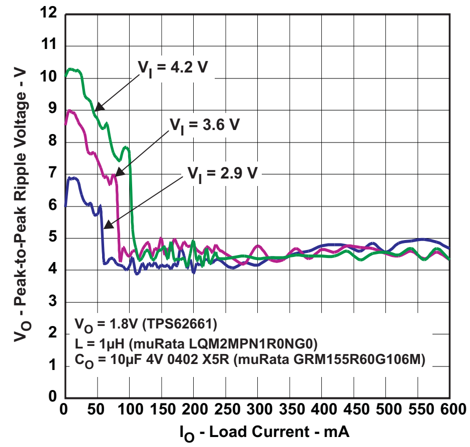
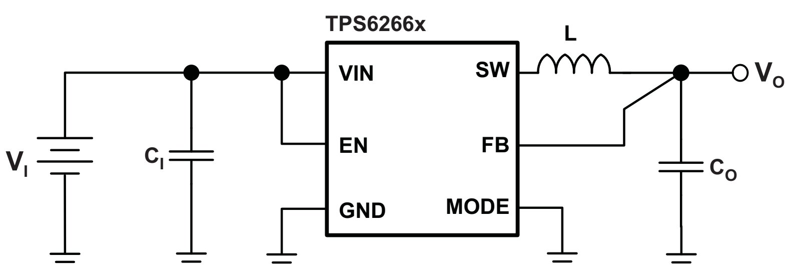


Figure 7. Peak-to-Peak Output Ripple Voltage vs Load Current

7 Parameter Measurement Information



List of components:

- L = MURATA LQM21PN1R0NGR
- C_I = MURATA GRM155R60J475M (4.7 µF, 6.3 V, 0402, X5R)
- C_O = MURATA GRM155R60J475M (4.7 µF, 6.3 V, 0402, X5R)

8 Detailed Description

8.1 Overview

The TPS6266x is a synchronous step-down converter typically operates at a regulated 6-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6266x converter operates in power-save mode with pulse frequency modulation (PFM).

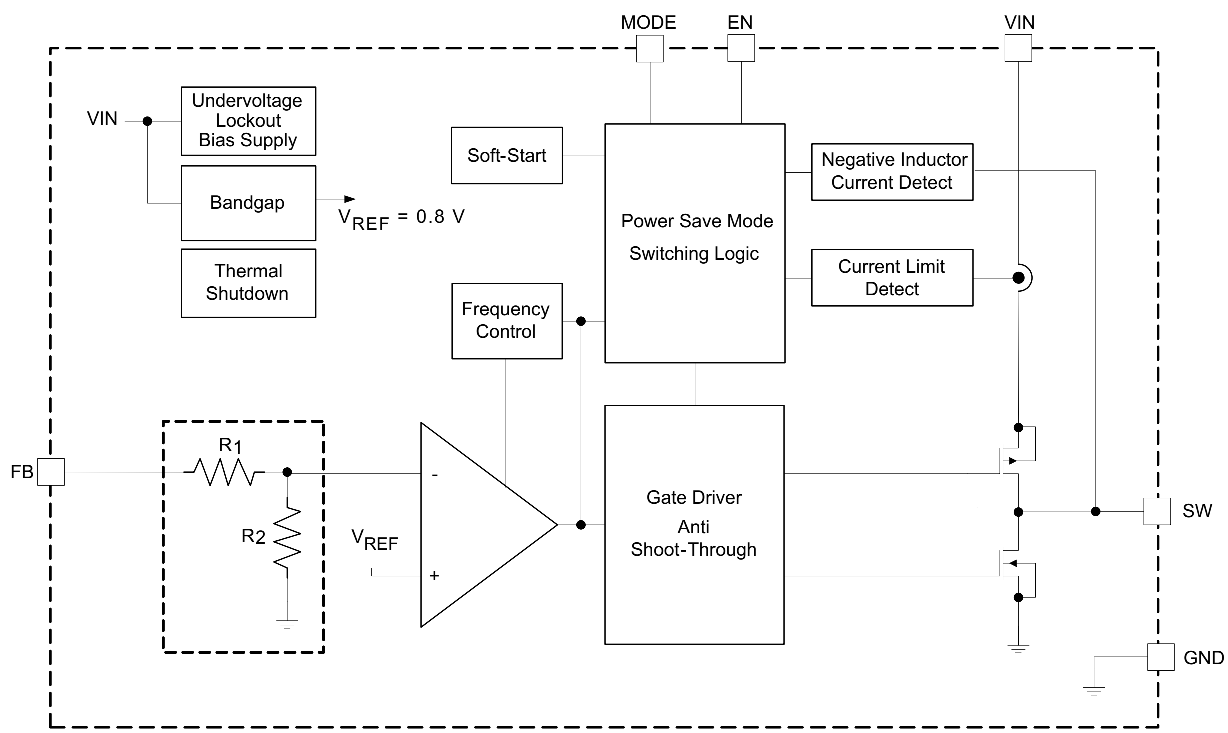
The converter uses a unique frequency-locked, ring-oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feedback loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6266x is inherently stable over a range of L and C_O.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 31 μA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Switching Frequency

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10 MHz to 12 MHz, which is controlled to approximately 6 MHz by a frequency-locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6 MHz. The tendency is for the converter to operate more towards a *constant inductor peak current* rather than a *constant frequency*. In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6-MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feedback input, thus decreasing its propagation delay, hence increasing the switching frequency.

8.3.2 Mode Selection

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide-load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

8.3.3 Enable

The device starts operation when EN is set high and starts up with the soft start. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1 μA. In this mode, the P- and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

8.3.4 Soft Start

The TPS6266x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the ON-time from a minimum pulse-width of 35 ns as a function of the output voltage. This mode of operation continues for approximately 100 μs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSFET remains on until the inductor current has reset. After a further 100 μs, the device ramps up to the full current limit operation if the output voltage has risen above 0.5 V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

The TPS62661 device starts up immediately into a nominal current limit mode, thereby ramping up the output voltage with maximum speed (<60 μs typically). The start-up time mainly depends on the output capacitor and load current.

Feature Description (continued)

8.3.5 Output Capacitor Discharge

The TPS6266x device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 15 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value.

8.3.6 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6266x device have a UVLO threshold set to 2.05 V (typical). Fully functional operation is permitted down to 2.1-V input voltage.

8.3.7 Short-Circuit Protection

The TPS6266x integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below approximately 0.4 V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5 V. Consider this when a load acting as a current sink is connected to the output of the converter.

8.3.8 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

8.4 Device Functional Modes

8.4.1 Power-Save Mode

If the load current decreases, the converter enters power-save mode operation automatically. During power-save mode, the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady-state. The PFM ON-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned approximately 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

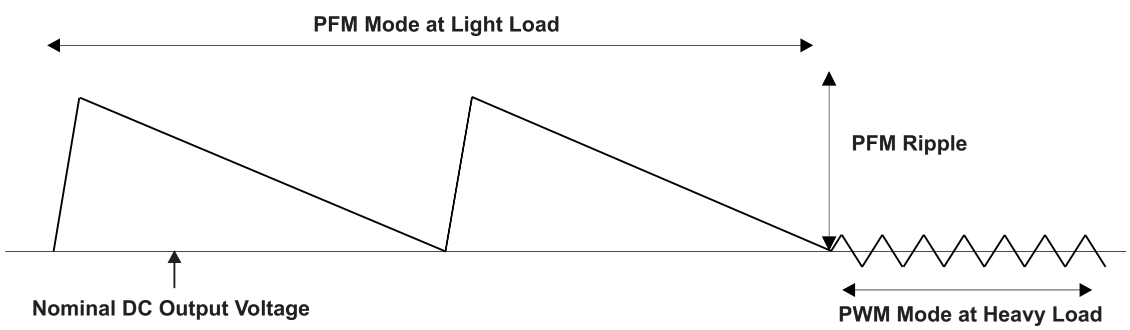


Figure 8. Operation in PFM Mode and Transfer to PWM Mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62660 is a high-efficient synchronous step-down converter providing up to 1000-mA output current.

9.2 Typical Application

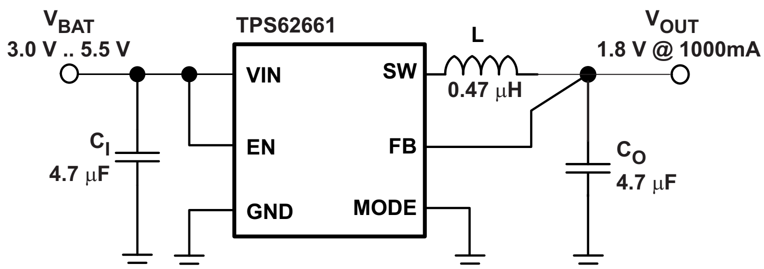


Figure 9. TPS62661 1.8-V Output Voltage

9.2.1 Design Requirements

The device operates over an input voltage range from 2.3 V to 5.5 V.

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The TPS62660 series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3 µH to 1.3 µH and with output capacitors in the range of 4.7 µF to 10 µF. The internal compensation is optimized to operate with an output filter of L = 0.47 µH and C_O = 4.7 µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see *Checking Loop Stability*.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - VO}{L \times f_{sw}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

where

- f_{SW} = switching frequency (6 MHz typical)
- L = inductor value
- ΔI_L = peak-to-peak inductor ripple current
- $I_{L(MAX)}$ = maximum inductor current (1)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high-efficiency operation, take care in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Typical Application (continued)

The total losses of the coil consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62660 converters.

Table 2. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
MURATA	LQM21PN1R0NGR	2.0 × 1.2 × 1.0 max. height
	LQM21PNR54MGC	2.0 × 1.2 × 1.0 max. height
	LQM2MPN1R0NG0	2.0 × 1.6 × 1.0 max. height
PANASONIC	ELGTEAR82NA	2.0 × 1.2 × 1.0 max. height
TOKO	MDT2012-CX1R0A	2.0 × 1.2 × 1.0 max. height
TAIYO YUDEN	NM2012NR82, NM2012N1R0	2.0 × 1.2 × 1.0 max. height
FDK	MIPS2012D1R0-X2	2.0 × 1.2 × 1.0 max. height

9.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6266x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device must operate within a minimum effective output capacitance of 1.6 μF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 4.7-μF capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is 1% of the nominal output voltage V_O.

The output voltage ripple during PFM mode operation can be kept very small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger once. Increasing the output capacitor value and the effective inductance minimizes the output ripple voltage.

9.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 4.7-μF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy is probably found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional *bulk* capacitance (electrolytic or tantalum) must in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

9.2.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times$ ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

9.2.3 Application Curves

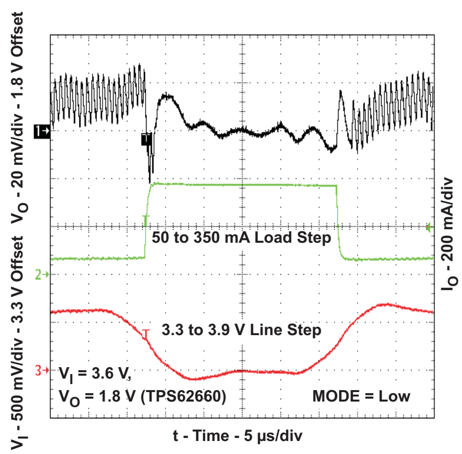


Figure 10. Combined Line and Load Transient Response

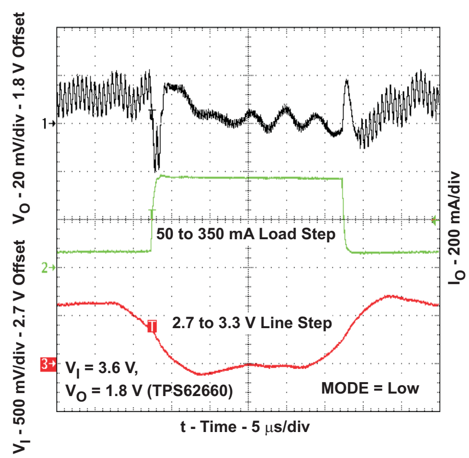


Figure 11. Combined Line and Load Transient Response

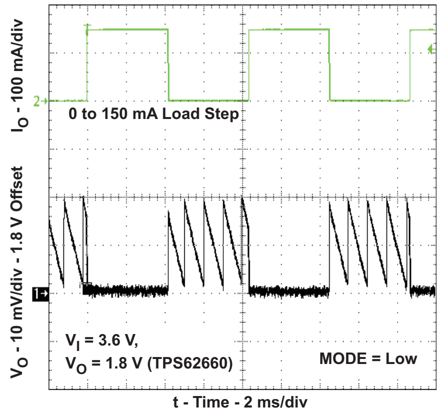


Figure 12. Load Transient Response in PFM/PWM Operation

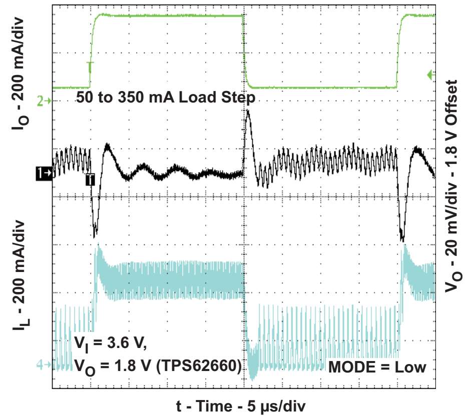


Figure 13. Load Transient Response in PFM/PWM Operation

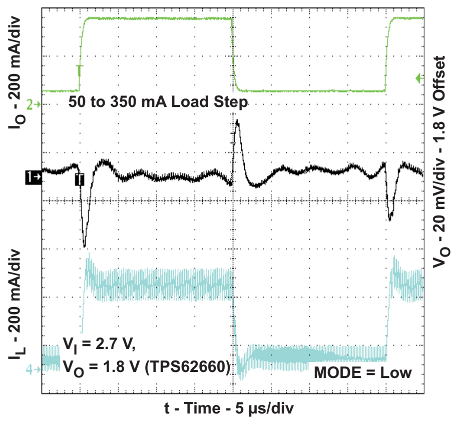


Figure 14. Load Transient Response in PFM/PWM Operation

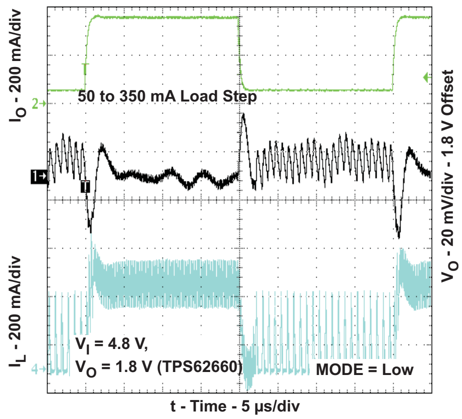


Figure 15. Load Transient Response in PFM/PWM Operation

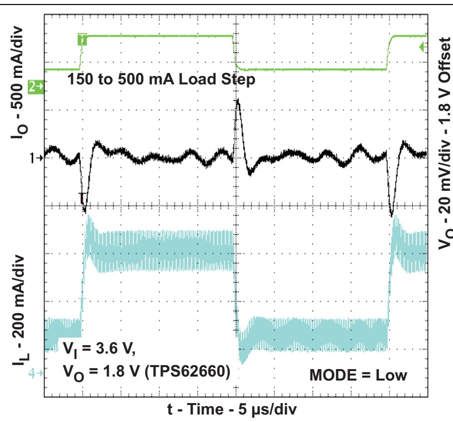


Figure 16. Load Transient Response in PFM/PWM Operation

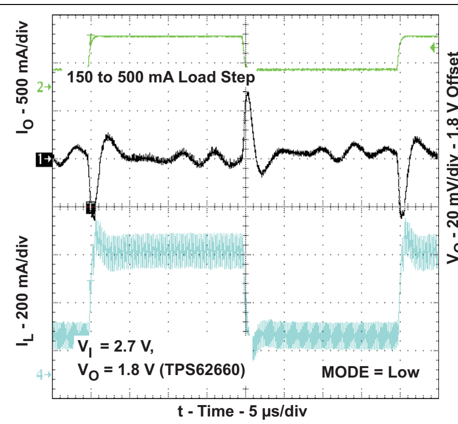


Figure 17. Load Transient Response in PFM/PWM Operation

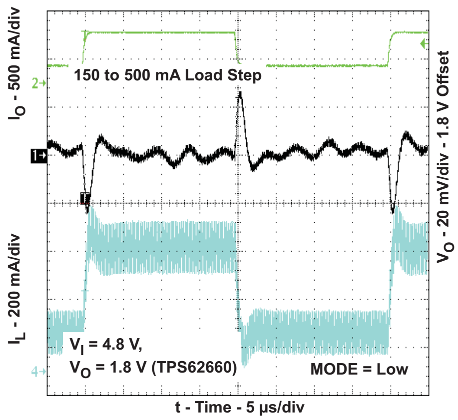


Figure 18. Load Transient Response in PFM/PWM Operation

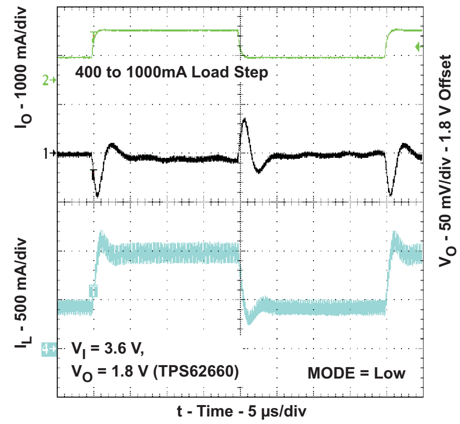


Figure 19. Load Transient Response in PFM/PWM Operation

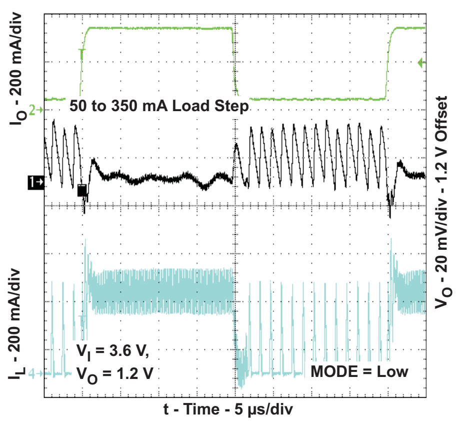


Figure 20. Load Transient Response in PFM/PWM Operation

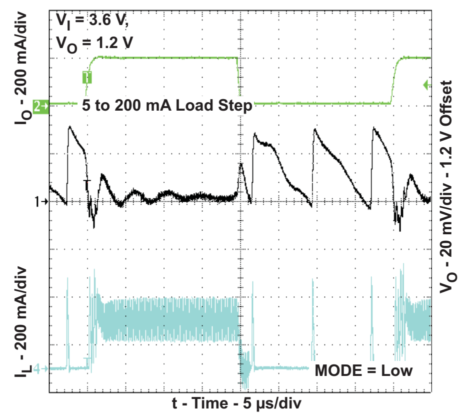


Figure 21. Load Transient Response in PFM/PWM Operation

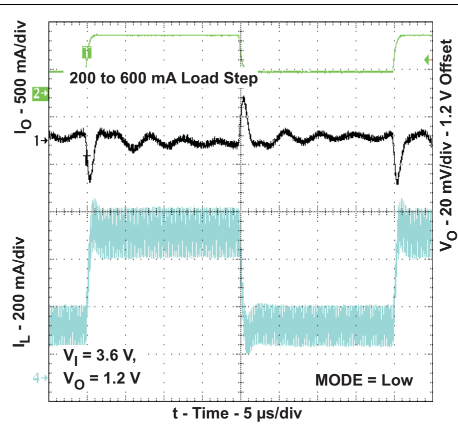


Figure 22. Load Transient Response in PFM/PWM Operation

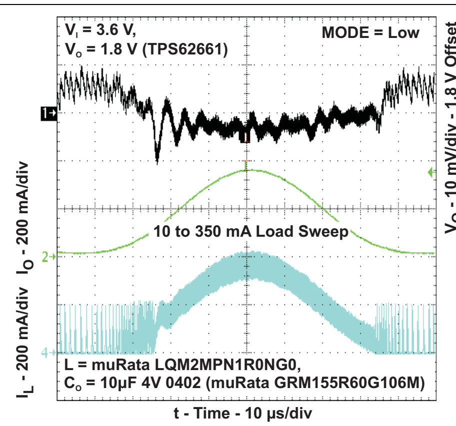


Figure 23. AC Load Transient Response

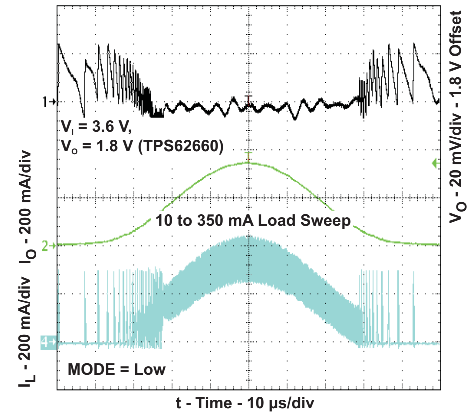


Figure 24. AC Load Transient Response

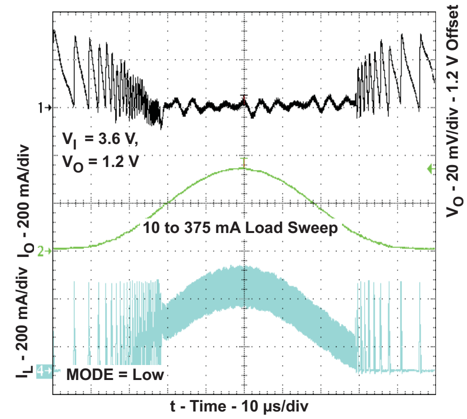


Figure 25. AC Load Transient Response

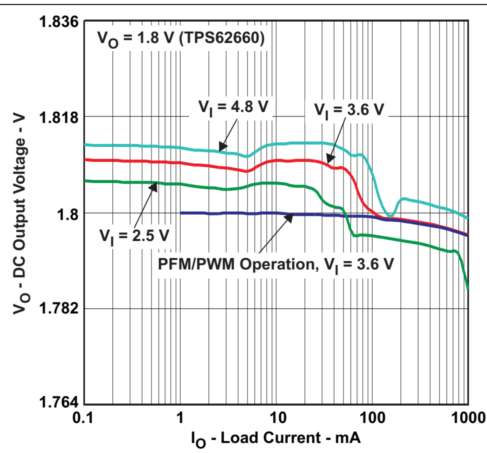


Figure 26. DC Output Voltage vs Load Current

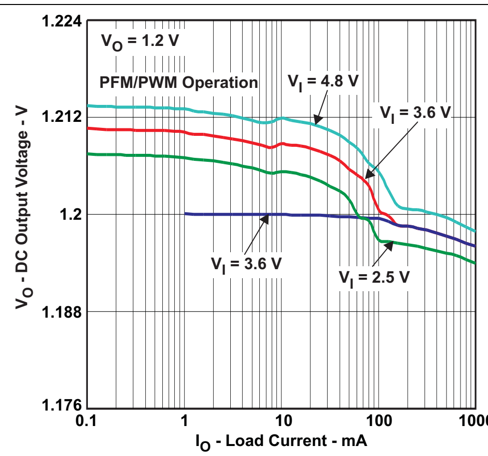


Figure 27. DC Output Voltage vs Load Current

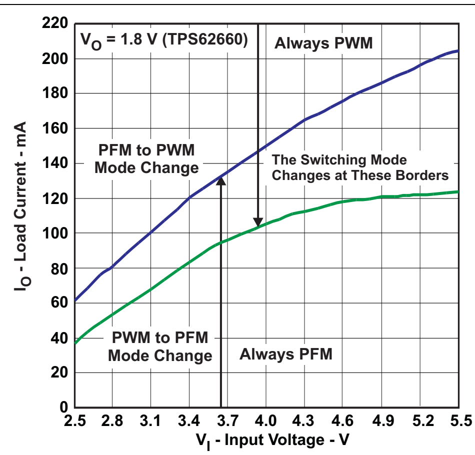


Figure 28. PFM/PWM Boundaries

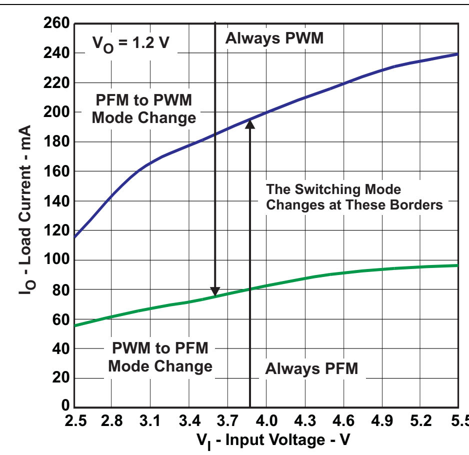


Figure 29. PFM/PWM Boundaries

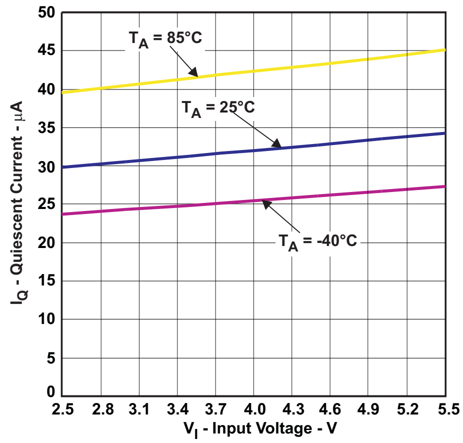


Figure 30. Quiescent Current vs Input Voltage

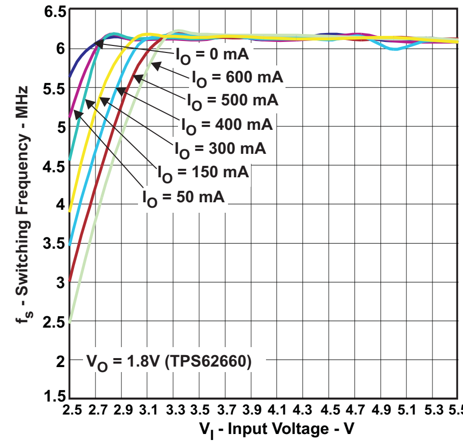


Figure 31. Switching Frequency vs Input Voltage

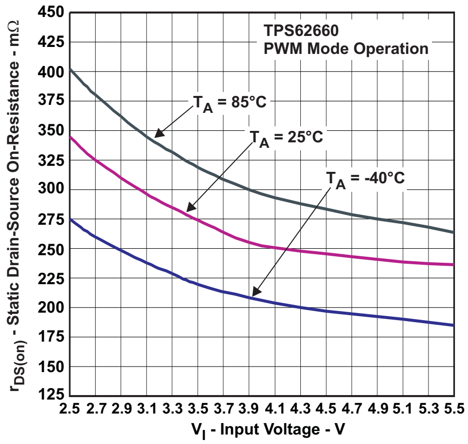


Figure 32. P-Channel $r_{DS(ON)}$ vs Input Voltage

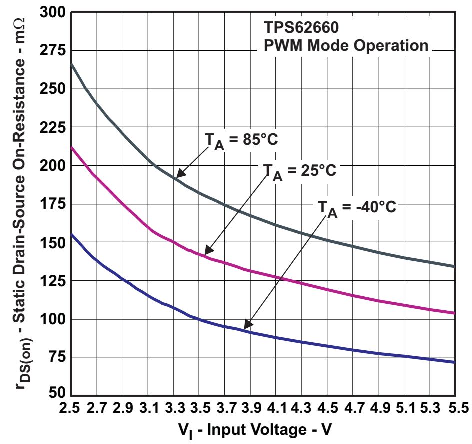


Figure 33. N-Channel $r_{DS(ON)}$ vs Input Voltage

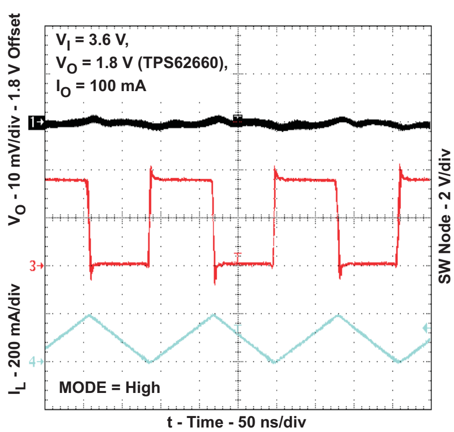


Figure 34. PWM Operation

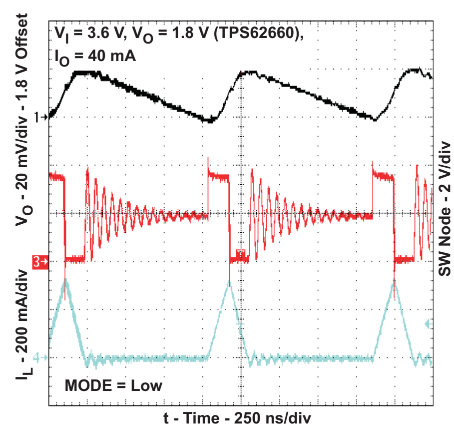


Figure 35. Power-Save Mode Operation

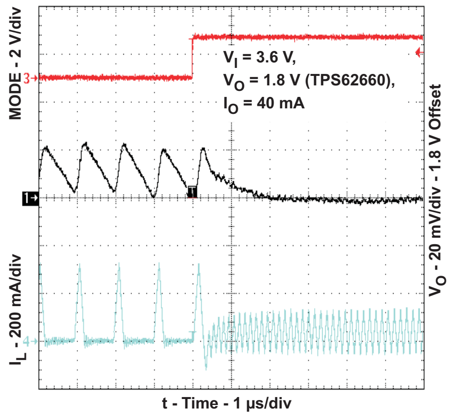


Figure 36. Mode Change Response

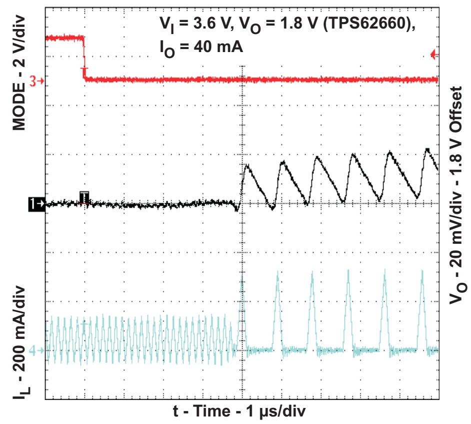


Figure 37. Mode Change Response

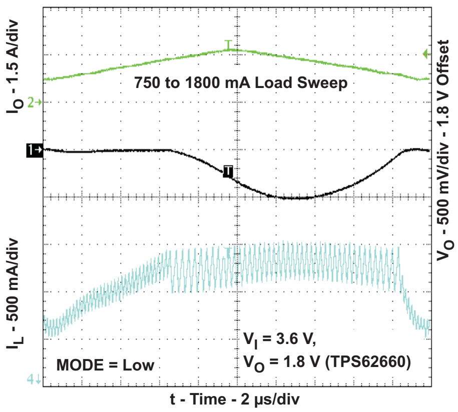


Figure 38. Overcurrent Fault Operation

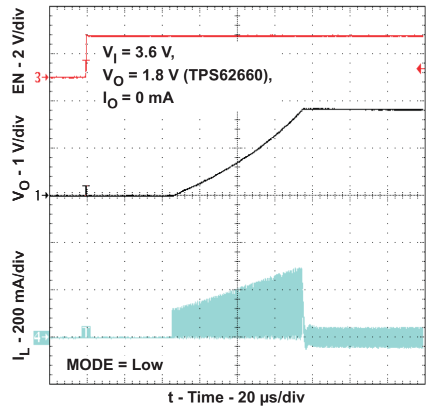


Figure 39. Start-Up

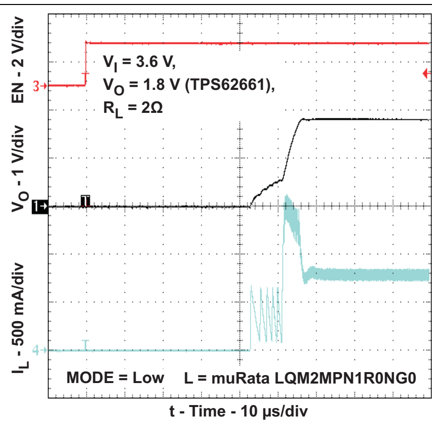


Figure 40. Start-Up

10 Power Supply Recommendations

The TPS6266x device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6266x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6266x devices demand careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line or load regulation, stability and switching frequency issues, as well as EMI problems. It is critical to provide a low-inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) must be taken in the output capacitor path, approximately 1 mm away for it. The feedback line must be routed away from noisy components and traces (that is, SW line).

11.2 Layout Example

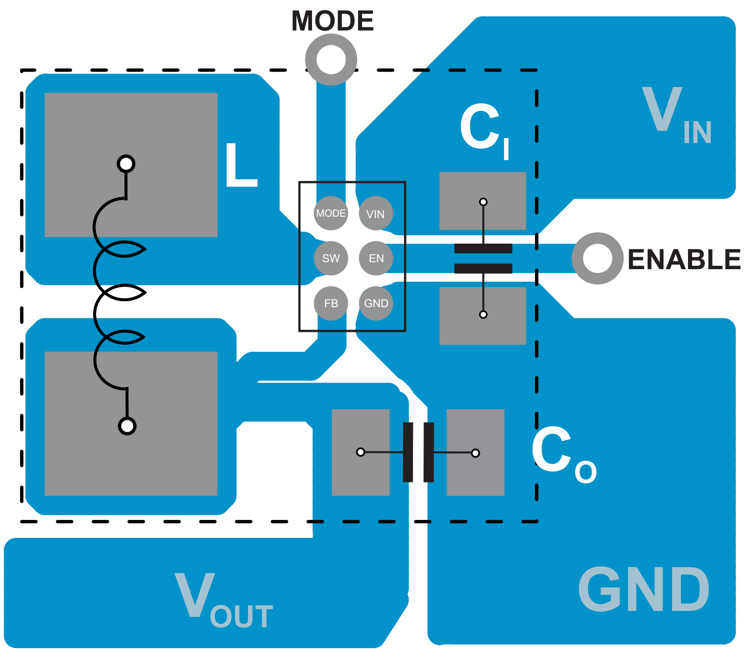


Figure 41. Suggested Layout (Top)

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power dissipation limits of a given component

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6266x devices is 105°C. The thermal resistance of the 6-pin DSBGA package (YFF-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum ambient temperature T_A of 85°C. Therefore, the maximum steady-state power dissipation is about 160 mW.

$$P_{D(MA)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{125°C/W} = 160\ mW \quad (2)$$

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62660YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OO	Samples
TPS62660YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OO	Samples
TPS62665YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RS	Samples
TPS62665YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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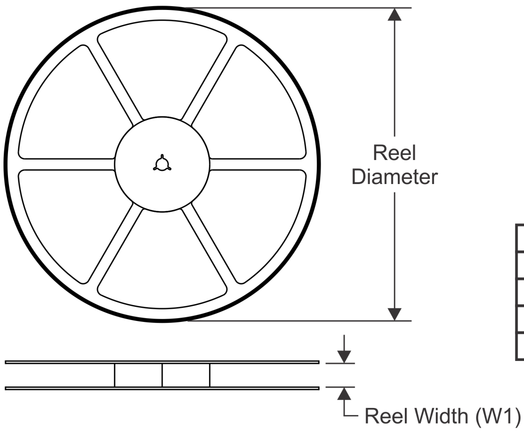
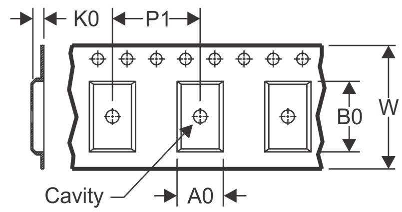
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

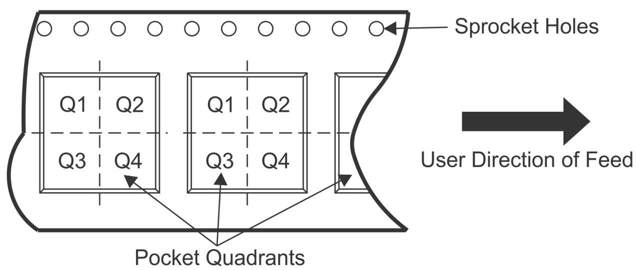


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

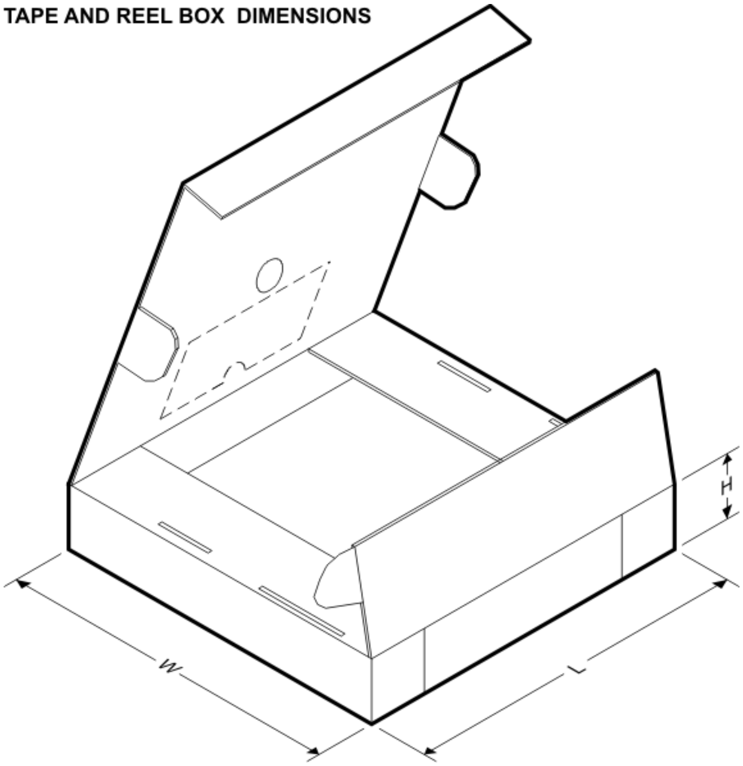
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

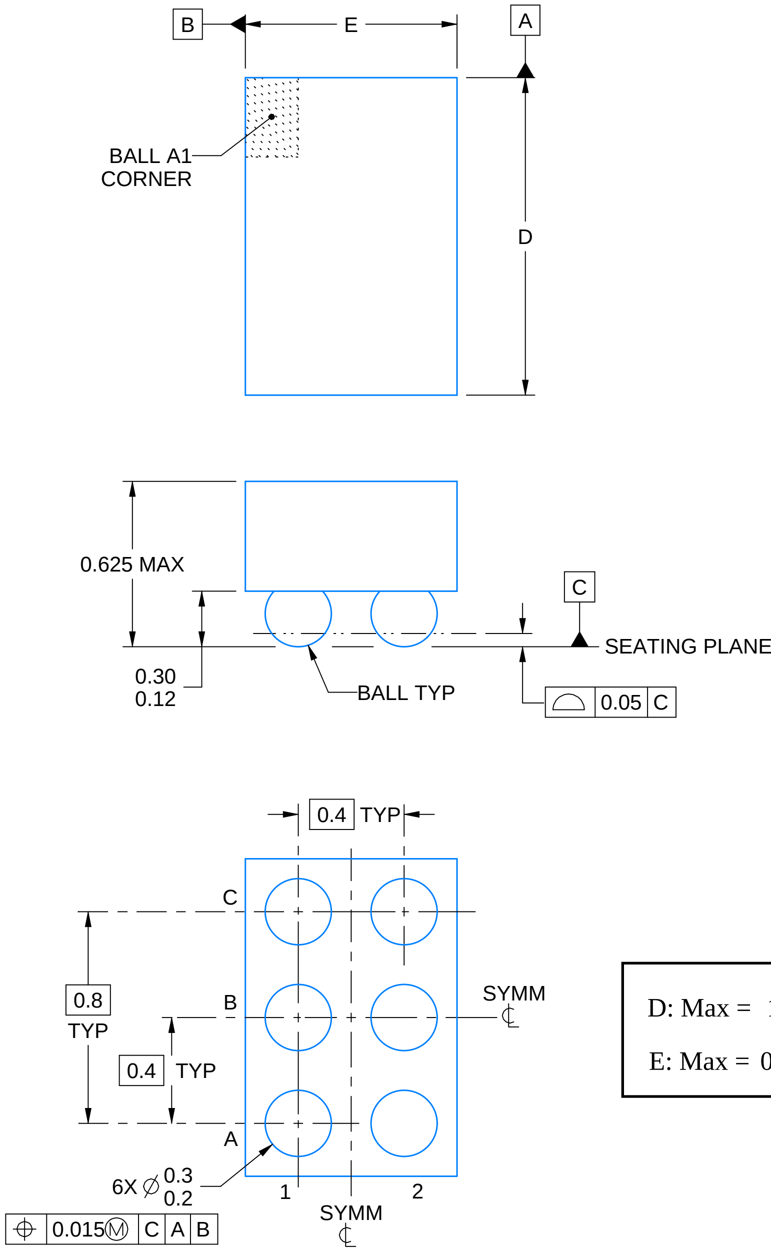
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62660YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62660YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62665YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62665YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62660YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62660YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62665YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62665YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0



D: Max = 1.33 mm, Min = 1.27 mm	
E: Max = 0.956 mm, Min =0.896 mm	

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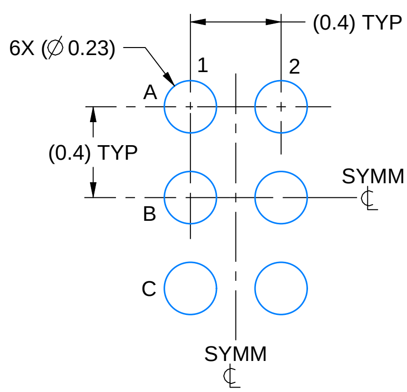
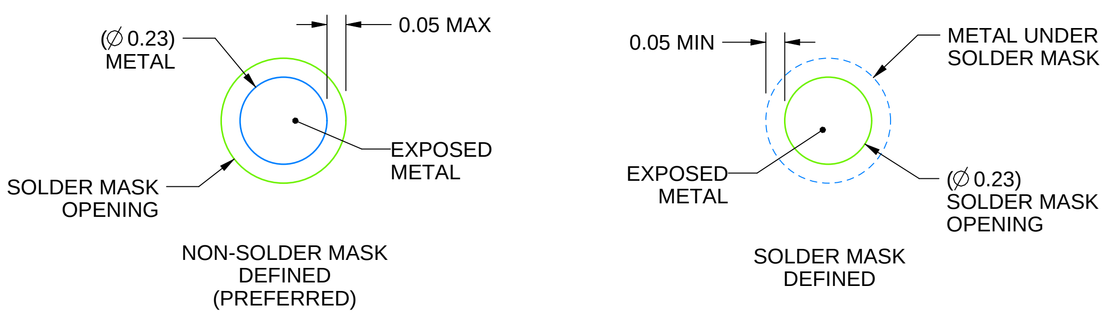
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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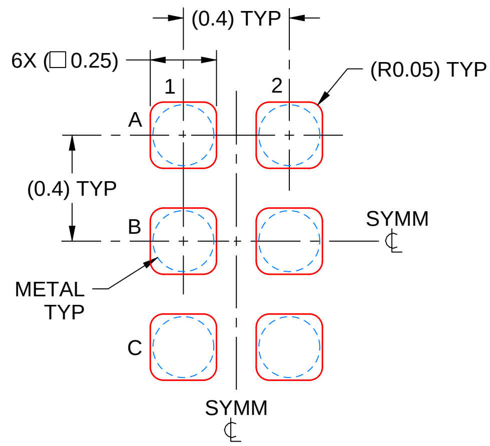
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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