Final Project (Jul–Nov 2018)

EE5325 –Power Management Integrated Circuits

Design a synchronous switching buck converter for the following specifications:

Technology	0.18µm CMOS process
Input voltage (V_{IN})	1.8V +/-10%
Output voltage (V_O) Digitally programmable	0.8V, 1.2V, 1.5V
Load current (I_{LOAD})	0 to 1A
Switching Frequency (F_{SW})	8MHz
Variation in F_{SW}	±10%
DC output voltage accuracy in PWM mode ($\%\Delta V_{O\_PWM}$)	±1% (including error due to bandgap reference, line regulation, load regulation)
DC output voltage accuracy in PFM mode ($\%\Delta V_{O\_PFM}$)	±5%
Settling Time (T_{SET}) (measured when output settles within 2% of the programmed output voltage) (should be measured in no. of PWM clock cycles)	< 10 PWM clock cycles
% Undershoot/Overshoot during load transient ($\Delta V_{UV\_LOAD}/\Delta V_{OV\_LOAD}$) (measured with load transient step of 1mA to 1A and 1A to 1mA with slew rate of 1A/100ns)	±5% of the programmed output voltage
Undershoot/Overshoot during line transient $\Delta V_{UV\_LINE}/\Delta V_{OV\_LINE}$) (measured with line transient step of 1.7V/1.9V to 1.9V/1.7V with slew rate of 100mV/100ns)	±1% of the programmed output voltage
Inductor (L)	Select from the inductor selection table
Output Capacitor (C)	Select between 1µF, 2.2µF, 4.7µF, 10µF, 22µF and 47µF.
Tolerance in Capacitors	±20%

Capacitor ESR (R_{ESR})	10mΩ
Capacitor ESL (L_{ESL})	1nH
Efficiency (%η) (for I_{LOAD} = 1mA to 1A)	> 90%
Max. peak-to-peak output voltage ripple in PWM mode (ΔV_{O_PWM})	<5mV
Max. peak-to-peak output voltage ripple in PFM/PSM mode (ΔV_{O_PFM})	<20mV
Soft start time (t_{ss})	1ms
Output Current Limit, (I_{LIM})	2A±10%
Maximum duty cycle limit (D_{max})	Max. possible (could be 100% if converter remains stable)
Minimum duty cycle limit (D_{min})	Min. possible (could be 0% if converter remains stable)

Inductor Selection Table

Inductor Value (L)	**DCR**	**Isat**
1µH +/-30%	60mΩ	2.7A
0.47µH +/-30%	32mΩ	3.8A
0.24µH +/-30%	22mΩ	5A
0.15µH +/-30%	18mΩ	6.2A

Important Notes:

- All building blocks of the buck converter must be transistor level (no behavioral model). You can reuse blocks from your previous designs or assignments.
- Standard cell library can be used for digital circuits.
- Each building block should have symbol and converter must be designed using hierarchical schematic (not flat).
- Any of the buck topologies (voltage mode, current mode, hysteretic etc.) can be used in the project.
- Design should be verified across all variations/tolerances of inductors, capacitors, process (TT,FF,SS) and temperature (-40ºC, 25ºC,125ºC).

Project Evaluation:

1. Presentation:

Students are required to prepare 15 minutes presentations with no more than 20 slides (excluding title and references slides) and present before the class. There will be 5 minutes Q&A session after the presentation.

Presentation should contain following three main sections:

i. Introduction, topology and component selection (4-5 slides)
ii. Architecture, power FET sizing and design of building blocks (10-12 slides)
iii. Simulation Results and Performance Table with FoM (4-5 slides)

Any circuits used from paper must be cited in the presentation. Any innovations/novelty in the design should be highlighted. Performance table must be based on the following format:

Parameters	**Results/Values**
Input Voltage Range	?
Output Range	?
Load Current Range	?
Switching Frequency (Fsw)	?
Inductor (L)	?
Output Capacitor (C)	?
DC output voltage accuracy in PWM mode (%ΔV_{O_PWM})	?
DC output voltage accuracy in PFM mode (%ΔV_{O_PFM})	?
Settling Time (no. of PWM clock cycles)	?
Undershoot as % of V_O when load transient is applied (ΔV_{UV_LOAD})	?
Overshoot % of V_O during load transient, (ΔV_{OV_LOAD})	?
Undershoot as % of V_O during low line transient (ΔV_{UV_LINE})	?
Overshoot as % of V_O during high line transient (ΔV_{OV_LINE})	?
% Efficiency (η)	?
Peak-to-peak output voltage ripple in PWM mode	?
Peak-to-peak output voltage ripple in PFM/PSM mode	?
Figure of Merit: **FoM1 (with both PWM and PFM mode enabled)** **FoM2 (with only PWM i.e. forced CCM mode enabled)**	 **?** **?**

Figure of Merit will be calculated using following expression:

$$FoM1 = \left(\frac{\%\eta_{min}+\%\eta_{max}}{180}\right) x \left(\frac{10^{-12}}{LxC}\right) x \left(\frac{25}{\%V_{UV_{LOAD}} x \%V_{OV_{LOAD}}}\right) x \left(\frac{1}{\%V_{UV_{LINE}} x \%V_{OV_{LINE}}}\right) x \left(\frac{10}{T_{SET}}\right) x \left(\frac{200x10^{-6}}{\Delta V_{O_{PWM}} x \Delta V_{O_{PFM}}}\right) \left(\frac{10^{-6}}{R_{TOTAL} x C_{TOTAL}}\right)$$

$$FoM2 = \left(\frac{\%\eta_{min}+\%\eta_{max}}{180}\right) x \left(\frac{10^{-12}}{LxC}\right) x \left(\frac{25}{\%V_{UV_{LOAD}} x \%V_{OV_{LOAD}}}\right) x \left(\frac{1}{\%V_{UV_{LINE}} x \%V_{OV_{LINE}}}\right) x \left(\frac{10}{T_{SET}}\right) x \left(\frac{10x10^{-3}}{\Delta V_{O_{PWM}}}\right) \left(\frac{10^{-6}}{R_{TOTAL} x C_{TOTAL}}\right)$$

R_{TOTAL} and C_{TOTAL} are total on-chip resistors (including feedback resistors) and capacitors (excluding output capacitor), respectively, used in the design.

2. **Schematic Review:**

   All students will have to get their schematics reviewed with live simulations.

Grading: Total Marks = 20

- Presentation = 5 Marks
- Schematics Review = 5 Marks
- Innovations/novelty = 5 Marks
- Specifications/FoM = 5 Marks

Bonus Points:

Student who meet all the specifications with highest figure of merit will get 5 bonus points that will be added to his/her final marks.

Dates:

- Presentation - Friday, Nov 09, 2018
- Schematic Review - Saturday, Nov 10, 2017

Detailed schedule with venue and time slots will be emailed later. Schematics will be reviewed at your workstations or in my office as per your choice.