

Linear Integrated Circuits and its Applications



SSQU016



Contents

Foreword.....	11
1 Introduction to Operational Amplifiers and Characteristics	13
1.1 Introduction	14
1.2 Linear integrated circuits and op-amp	15
1.3 Block diagram	16
1.4 Characteristics and equivalent circuits of an ideal op-amp	17
1.4.1 Characteristics of Ideal Op-amp:.....	18
1.4.2 Equivalent circuit of op-amp	19
1.5 Various Types of operational amplifiers and applications	20
1.6 Power Supply Configurations of Op-Amp	21
1.7 Inverting and non inverting amplifier configurations	23
1.7.1 Open loop operation of Op-Amp	23
1.7.2 Closed loop configuration of Op-Amp	24
1.7.3 Inverting-configuration using ideal op amp	25
1.7.4 Non Inverting-configuration using ideal op amp.....	26
1.8 Summary.....	28
1.9 Review Questions	29
1.10 Exercises:.....	30
2 Practical Operational Amplifiers.....	32
2.1 Introduction	33
2.2 Effect of Finite Loop Gain on Closed Loop Gain	34
2.3 Effect of finite loop gain on Input Resistance R_{in}	42
2.4 Effect of finite gain on output resistance R_{out}	44
2.5 Voltage follower or Buffer Amplifier	47
2.6 Input offset and Input Bias current.....	49
2.7 Input Offset Voltage	53
2.8 Thermal Drift	55
2.9 Common Mode Rejection ratio (CMRR)	57
2.10 Slew rate and its effects.....	59
2.11 Power Supply Rejection Ratio (PSRR).....	60
2.12 Frequency Response.....	61
2.12.1 Frequency Response of Non Inverting Amplifier	63
2.12.2 Frequency Response of Inverting Amplifier	65
2.12.3 Frequency response with double pole	67
2.13 Interpretation of TL082 Data sheet	68
2.13.1 Introduction.....	68

2.13.2 General Classification of Op-amps	68
2.13.3 About TL082	69
2.13.4 Major features of TL082	70
2.13.5 List of common data sheet parameters	70
2.13.6 DC and AC Electrical Characteristics	72
2.13.7 Application Notes for TL082	72
2.14 Summary	73
2.15 Review Questions	74
2.16 Exercises	75
3 Amplifiers and Oscillators.....	76
3.1 Introduction	77
3.2 Summing amplifier	78
3.2.1 Inverting Summing Amplifier	78
3.2.2 Inverting Summing Amplifier with Unity Gain	79
3.2.3 Inverting Summing Amplifier with Gain Greater than Unity	79
3.2.4 Non-inverting Summing Amplifier	79
3.3 Averaging Amplifier	81
3.4 Scaling Amplifier	82
3.5 Integrator	83
3.6 Differentiator	86
3.7 Instrumentation amplifier	89
3.8 Differential Input and Differential Output Amplifiers	92
3.8.1 Differential Input Amplifier	92
3.8.2 Differential Output Amplifier	93
3.9 Feedback Amplifiers	94
3.9.1 Voltage series feedback amplifier	96
3.9.2 Voltage shunt feedback amplifier	100
3.10 Log / Antilog Amplifiers	102
3.10.1 Log Amplifiers	102
3.10.2 AntiLog Amplifier	104
3.11 Isolation Amplifiers	105
3.11.1 TI ISO 124 Precision Low Cost Isolation Amplifier	106
3.12 Triangular/ Rectangulaer Wave Generator	107
3.13 Oscillators	109
3.13.2 Weinbridge Oscillator	113
3.14 Analog Multiplier	115
3.14.1 TI MPY 634 Wide bandwidth precision Analog Multiplier	116
3.15 Voltage Controlled Oscillator: (VCO)	119
4 Active Filters.....	122
4.1 Introduction	123
4.2. Characteristics of Filters	125
4.2.1. Filter parameters	125
4.3. Classification of Filters	126

4.4. Magnitude and Frequency response	127
4.4.1. Phase Response	127
4.4.2. Impulse Response.....	127
4.4.3. Step Response.....	128
4.5. Fundamentals of Low-Pass Filters	128
4.6 Butterworth Low-Pass Filters	129
4.6.1 First order Low-Pass Filter Design.....	130
4.6.2. First-Order Unity-Gain Low-Pass Filter.....	132
4.6.3. Second-Order Low-Pass Filter.....	135
4.7. High-Pass Filter Design	138
4.7.1 First-Order Butterworth High-Pass Filter.....	139
4.7.2. Multiple Feedback Topology	143
4.8. Band-Pass Filter Design	144
4.8.1. Second-Order Butterworth Band-Pass Filter	144
4.8.2. Sallen-Key Topology	145
4.9. Characteristics of Chebyshev Low-Pass Filters	150
4.9.1. Type I Chebyshev Filters	150
4.9.2. Type 2 II Chebyshev filters.....	151
4.10. Band-Rejection Filter Design	152
4.10.1 Active Twin-T Filter	153
4.10.2 Active Wien-Robinson Filter.....	154
4.11 All-Pass Filter Design.....	159
4.11.1 First-Order All-Pass Filter.....	160
4.11.2 Second-Order All-Pass Filter	161
4.11.3 Higher-Order All-Pass Filter	161
4.12 Self -tuned Filters	164
4.12.1 Multiplier as a Phase Detector	165
4.13 Summary.....	171
4.14 Review Questions	172
4.15 Exercises.....	175
5 Comparators and Converters	178
5.1 Introduction	179
5.2 Comparators	180
5.2.1 Non-inverting Op-amp Comparator Circuit	180
5.2.2 Inverting Op-amp Comparator Circuit	182
5.3 Zero Crossing Detector Using OPAMP	184
5.4 Op-Amp Monostable Multivibrator	185
5.5 Astable Multivibrator Using Op-Amp.....	186
5.6 Schmitt Trigger Circuit	188
5.7 Voltage Limiter Circuit Using Op-amp	189
5.8 Clippers and Clampers	193
5.8.1 Positive Clipper	193
5.8.2 Negative Clipper.....	194
5.8.3 Positive and Negative Clampers	196

5.9 Absolute value circuit:	197
5.9.1 Op-amp absolute value amplifier	199
5.10 Op-Amp Peak Detector.....	200
5.11 Sample and Hold Circuit Using Op-Amp	201
5.12 Precision Rectifiers	203
5.12.1 A Simple Precision Rectifier Circuit.....	203
5.13 Voltage-to-current signal conversion	203
5.13.1 Voltage to current converter.....	203
5.14 Current to Voltage converter.....	204
5.15 Summary.....	206
5.16 Review Questions	207
5.17 Exercises:.....	209
6 Advanced Applications of Operational Amplifiers	211
6.1 Introduction	212
6.1.1 Need for Voltage Regulators.....	212
6.1.2 Voltage Regulation.....	212
6.2 Series Voltage Regulation	214
6.3 Shunt Voltage Regulation	218
6.4.1 Step-down type	220
6.4.2 Step-up type.....	221
6.5 Switching Regulators	222
6.5.1 Buck Regulator.....	223
6.5.2 Boost Regulator.....	224
6.5.3 Buck-Boost Regulator	224
6.5.4 Flyback Regulator	225
6.6 Dual Power supply	227
6.7 Characteristics of standard regulator ICs – TPS40200, TPS40210	227
6.8 Phase Locked Loops	229
6.8.1 How does PLL work?	230
6.8.2 Transfer Characteristics of PLL.....	235
6.8.3 CD4046B Monolithic PLL	236
6.8.4 Frequency Shift Keying - Modulation and Demodulation.....	239
6.8.5 IMPLEMENTATION OF FSK Modulation and Demodulation using PLL	241
6.9 Automatic Gain Controller (AGC)/Automatic Volume Control (AVC) using op-AMP and analog multipliers:.....	242
6.10 Amplitude modulation using analog multiplier	245
6.11 Summary:.....	246
6.12 Review Questions	247
6.13 Exercises.....	248
7 Authors	249

List of Figures

Fig 1.1 Tone controller for guitar amplifier.....	15
Fig 1.2 Temperature deviation indicator.....	15
Fig 1.3 Dual-input differential operational amplifier.....	16
Fig 1.4 Block diagram of an operational amplifier	16
Fig 1.5 Symbol of operational amplifier	17
Fig 1.6 Ideal operational amplifier	18
Fig 1.7 Equivalent circuit of operational amplifier.....	19
Fig 1.8 Power supply configuration using two power supplies.....	21
Fig 1.9 Power supply configuration using single power supply	22
Fig 1.10 Power supply configuration using Zener diodes	22
Fig 1.12 Open loop operation of operational amplifier	24
Fig 1.13 Inverting amplifier	25
Fig 1.14 Non-Inverting amplifier	26
Fig 1.15 Design of inverting operational amplifier	27
Fig 1.16 Design of inverting operational amplifier	28
Fig 2.1 Analysis of Inverting Amplifier with finite open loop Gain.....	34
Fig 2.2 Simulation result of inverting opamp when $A_0 = 1000$	36
Fig 2.3 Simulation result of inverting opamp when $A_0 = 10000$	37
Fig 2.4 Analysis of non-inverting Amplifier with finite open loop Gain	37
Fig 2.5 Simulation result of non-inverting OpAmp when $A_0 = 1000$	39
Fig 2.6 Simulation result of non-inverting opamp when $A_0 = 10000$	40
Fig 2.7 Simulation result of non-inverting opamp when $A_0 = 100000$	41
Fig 2.8 Analysis of Inverting Amplifier for Input Resistance	42
Fig 2.9 Non-inverting amplifier with a differential resistance of R_{di}	43
Fig 2.10 Inverting Amplifier with a non-zero output resistance operational amplifier.....	44
Fig 2.11 Non-inverting amplifier with R_o as the output resistance of the op amp.....	46
Fig 2.12 Voltage Follower	48
Fig 2.13 (a) Direct Connection of source and load.....	48
Fig 2.13 (b) Connection via a voltage follower	49
Fig 2.14 Offset and Bias current.....	50
Fig 2.15 Output Error estimation	50
Fig 2.16 Inverting Amplifier circuit with compensating resistor R_c	51
Fig 2.17 Input offset voltage model	53
Fig 2.18 Offset Adjustment Pins	54
Fig 2.19 Inverting Op Amp External offset Trim method	54
Fig 2.20 Operational Amplifier with Common mode voltage	57
Fig 2.21 Op Amp circuit with separate input voltages	58
Fig 2.22 Slewling distortion	60
Fig 2.23 Op Amp Frequency Response	61
Fig 2.24 Frequency Response with compensation	61
Fig 2.25 Closed Loop op Amp Frequency response	62
Fig 2.26 Frequency Response of Non-Inverting amplifier.....	64
Fig 2.27 Two pole frequency response	67
Fig 2.28 Pin connection diagram of TL082.....	69
Fig 3.1 Inverting Summing Amplifier	78
Fig 3.2 Inverting Summing Amplifier Audio Mixer	79
Fig 3.3 Non-inverting Summing Amplifier	80
Fig 3.4 Averaging Amplifier	81
Fig 3.5 Scaling Amplifier	82
Fig 3.6 Scaling Amplifier as Analog to Digital Converter.....	83
Fig 3.7 Basic Inverting Integrator	83
Fig 3.8 The input square waveform and the output triangular waveform.....	84

Fig 3.9 Frequency response of basic and practical integrator	85
Fig 3.10 Integrator as a Function Generator	86
Fig 3.11: Inverting Differentiator	86
Fig 3.12 The input triangular waveform and the output square waveform	87
Fig 3.13 Frequency response of basic and practical differentiator	87
Fig 3.14 Practical Inverting Differentiator	88
Fig 3.16 Instrumentation Amplifier with external gain setting resistor R_G	90
Fig 3.17 Instrumentation Amplifier in ECG Measurement.....	91
Fig 3.18 Differential input amplifier	92
Fig 3.19 Difference between standard and fully differential amplifier	93
Fig 3.20 Feedback configurations	96
Fig 3.21. Voltage series feedback amplifier	97
Fig 3.22 Voltage shunt feedback amplifier	100
Fig 3.23 Log Amplifier.....	102
Fig 3.24. Anti log amplifier	104
Fig 3.25 Op- amp isolation amplifier.....	105
Fig 3.26 Transformer coupled isolation amplifier	105
Fig 3.27 Symbol of ISO 124	106
Fig 3.29 Practical triangular wave generator.....	108
Fig 3.30 Triangular wave generator- output waveforms.....	108
Fig 3.31 Feedback Oscillator.....	110
Fig 3.32 Oscillation for $A_{cl}> 1$ and $A_{cl} =1$	110
Fig 3.33 RC Phase Shift Oscillator.....	111
Fig 3.34 RC feedback network	111
Fig 3.35 OP-amp wein bridge oscillator	113
Fig 3.36 Wein bridge oscillator- Lead lag configuration	114
Fig 3.37 Basic building block of an Analog amplifier	115
Fig 3.38 Quadrant multiplier	116
Fig 3.39 Block diagram of MPY 634 analog multiplier	117
Fig 3.40 Pin diagram of MPY 634 Analog Multiplier.....	117
Fig 3.41 Basic Multiplier	118
Fig 3.42 Analog Multiplier and Integrator in Automatic Gain Control	119
Fig 3.43 Function Generator.....	119
Fig 3.44. Function generator output	120
Fig 3.45 Voltage Controlled Oscillator(VCO).....	121
Fig 4.1 Public Address System	124
Fig 4.2 Desired or Ideal frequency response of different filters.....	125
Fig 4.3 Magnitude and Phase response of Low pass filter	127
Fig 4.4 Low pass filter basic response curve	128
Fig 4.5 First-Order Passive RC Low-Pass Filter	129
Fig 4.6 Magnitude and Phase response of Butterworth low Pass Filter	130
Fig 4.7 First-Order Non-inverting Low-Pass Filter.....	130
Fig 4.8 First-Order Inverting Low-Pass Filter	131
Fig 4.9 First-Order Non-inverting Low-Pass Filter with Unity Gain	132
Fig 4.11 Circuit diagram and Simulation result of Low pass filter design- Chebyshev 1 st order (with passband frequency of 10 KHz)	134
Fig 4.12 General Sallen-Key Low-Pass Filter	135
Fig 4.13 Unity-Gain Sallen-Key Low-Pass Filter	135
Fig 4.14 Second-Order MFB Low-Pass Filter	137
Fig 4.15 High pass filter basic response curve.....	138
Fig 4.17 First-Order Non-inverting High-Pass Filter.....	139
Fig 4.18 First-Order Inverting High-Pass Filter.....	140
Fig 4.19 Unity-Gain Sallen-Key High-Pass Filters	140
Fig 4.20 Circuit diagram and Simulation result of High pass filter design- Chebyshev- 1 st order	142

Fig 4.21 Second-Order MFB High-Pass Filter.....	143
Fig 4.22 Low-Passes to Band-Pass Transition	144
Fig 4.23 Sallen-Key Band-Pass filter.....	145
Fig 4.24 MFB Band-Pass Filter	146
Fig 4.26: Second-order band-pass filter with $f_0 = 1 \text{ KHz}$, $\text{BW}=100\text{Hz}$	149
Fig 4.27 Frequency response of second-order band-pass filter with $f_0 = 1 \text{ KHz}$, $\text{BW} = 100 \text{ Hz}$	150
Fig 4.28 Frequency response of Chebyshev I Low pass filter	151
Fig 4.29 Frequency response of Chebyshev II Low pass filter	152
Fig 4.30 Passive Twin-T Filter.....	153
Fig 4.31 Active Twin-T Filter.....	153
Fig 4.32 Passive Wien-Robinson Bridge.....	154
Fig 4.33 Active Wien-Robinson Filter	155
Fig 4.34 Circuit diagram and Simulation result of Band stop filter design - Chebyshev - 2 nd order.....	156
Fig 4.35 Circuit Diagram and Simulation result of second-order notch filter with $f_0 = 60 \text{ Hz}$ and $\text{BW} = 5 \text{ Hz}$	158
Fig 4.36 Input and Output Waveforms of All pass filters	159
Fig 4.37 First-Order All-Passes	160
Fig 4.38 Second-Order All-Pass Filter.....	161
Fig 4.39 Seventh-Order All-Pass Filter.....	162
Fig 4.40 Circuit diagram and Simulation result of All pass filter design- Bessel - 2 nd order.....	163
Fig 4.41 Multiplier and its output	164
Fig 4.42 Multiplier as a phase detector	164
Fig 4.43 Voltage controlled filter with frequency $\propto (1 / V_c)$	165
Fig 4.44 Voltage controlled filter with frequency $\propto V_c$	166
Fig 4.45 A self-tuned filter based on a voltage controlled filter or voltage controlled phase generator.....	166
Fig 4.46 A simple voltage-controlled phase generator that can become part of a self-tuned filter	167
Fig 4.48 Effects of the filter order on the frequency response	172
Fig 4.49 Second order Butterworth Band pass filter	172
Fig 4.50 Frequency response for various Q values	173
Fig 5.1 Circuit for a basic operational amplifier comparator.....	180
Fig 5.2 OPAMP Non-Inverting Comparator Circuit	180
Fig 5.3 Op-Amp Non-Inverting Comparator Waveform	182
Fig 5.4 Op-amp Inverting Comparator Circuit	182
Fig 5.5 Op-Amp Inverting Comparator Waveform	183
Fig 5.6 Zero-Crossing Detector Using op-amp.....	184
Fig 5.7 Zero-Crossing Detector Waveforms	185
Fig 5.8 Monostable multivibrator using Op-amp	185
Fig 5.9 Input and output waveforms	186
Fig 5.10 Op-amp Astable multivibrator	187
Fig 5.11 Capacitor waveforms	187
Fig 5.12 Schmitt Trigger	188
Fig 5.13 Input and Output Waveforms of Schmitt Trigger	188
Fig 5.14 Voltage limiter using op-amp	189
Fig 5.15 Voltage limiter waveforms	190
Fig 5.16 Voltage limiter circuit with two zener diodes	191
Fig 5.18 Voltage limiter circuit with one zener diode	192
Fig 5.19 Voltage limiter waveforms	192
Fig 5.20 Positive clipper	193
Fig 5.22 Negative clipper circuit	194
Fig 5.23 output waveforms of negative clipper	195
Fig 5.24 Positive clamer circuit.....	196
Fig 5.25 Negative clamer circuit	196
Fig 5.26 Positive clamer output waveform	197

Fig 5.27 Negative clamper output waveform.....	197
Fig 5.28 Absolute Value Circuit	198
Fig 5.29 Op-amp absolute value amplifier.....	199
Fig 5.30 Op-amp absolute value amplifier if $V_{in} > 0$	199
Fig 5.31 Op-amp absolute value amplifier if $V_{in} < 0$	200
Fig 5.32 Op-amp peak detector.....	201
Fig 5.33 Sample and Hold circuit using op-amp.....	202
Fig 5.34 Input and output waveforms - Sample and hold circuit	202
Fig 5.35 Precision Rectifier.....	203
Fig 5.36 Voltage to current converter	204
Fig 5.37 Inverting Transimpedance amplifier (TIA) with a reverse biased photodiode	205
Fig 6.1 Linear Regulator (Series Regulation)	214
Fig 6.2 Linear Regulator (Series Type)	214
Fig 6.3 Constant Current Regulator	216
Fig 6.4 Regulator with fold-back current limiting	217
Fig 6.5 Linear Voltage Regulator - Shunt type	218
Fig 6.6 Shunt type voltage regulator	219
Fig 6.7 Step-down type shunt voltage regulator.....	220
Fig 6.8 Step-up type shunt voltage regulator	221
Fig 6.9 Buck Regulator	223
Fig 6.10 Current through the inductor in a buck regulator.....	223
Fig 6.11 Boost Regulator.....	224
Fig 6.12 Buck-Boost Regulator	224
Fig 6.13 Flyback Regulator.....	225
Fig 6.14 Multiple output Flyback regulator	226
Fig 6.15 TPS54340 Split Rail Power Supply.....	227
Fig 6.16 Schematic of TPS40200.....	228
Fig 6.17: Schematic of TPS40210.....	229
Fig 6.18: Block diagram of PLL	230
Fig 6.19 Digital Phase Detector.....	231
Fig 6.20 Digital Phase Detector Response	231
Fig 6.22 Analog Phase Detector	232
Fig 6.23 Analog Phase Detector Response	232
Fig 6.24 PLL Spectrum.....	234
Fig 6.25 Transfer characteristics of PLL.....	235
Fig 6.26 CD4046B Monolithic PLL	236
Fig 6.27 CD4046B Phase Comparator.....	237
Fig 6.28 CD4046B Voltage Controlled Oscillator	238
Fig 6.29 FSK Modulation	240
Fig 6.30 FSK Parameters	240
Fig 6.31 PLL as FSK modulator	241
Fig 6.32 PLL as FSK demodulator	241
Fig 6.33 Analog Multiplier	242
Fig 6.34 MPY634 Analog Multiplier	243
Fig 6.35 AGC LOOP.....	244
Fig 6.36 Automatic Gain Control (AGC)/Automatic Volume Control (AVC)	244
Fig 6.37 Input-Output Characteristics of AGC/AVC	245
Fig 6.38 MPY634 Amplitude modulation setup	246

Table of Figures

Table 1.1 Comparison between digital and analog circuits.....	14
Table 1.2 Various types of operational amplifiers by Texas Instruments.....	20
Table 2.1 Parameter values for ideal and non-ideal operational amplifiers	33
Table 2.2 Typical Op-Amp Input offset voltage	53
Table 2.3 Thermal drift parameters	55
Table 4.1 Second order filter coefficients for Butterworth and Chebyshev filters	136

Foreword

While it may appear that the world is going digital in all areas of applications ranging from automotive technologies to Personal electronics to consumer appliances, the role of analog has evolved to an extent that the modern day electronics has more analog content than ever. Take a cell phone for example though it is a digital system, it has a significant amount of analog content like sensors, amplifiers, filters, power management, and RF.

Current analog system design practices in Industry require the use of the intelligent macro model approach to study the input/output behavior of any analog subsystem. This approach starts with the building block and their macro models and uses it to design complex analog systems. It is also important to study the characteristics of the building block by studying the parameters of the macro model. One must understand the significance of these parameters and their corresponding effect on the system behavior to meet varied application needs. There is a greater need in the industry for application engineers who can judiciously use the analog integrated circuits (ICs) to design efficient analog systems. Therefore, engineering students should be first exposed to the applications so that they appreciate the analog processing still required in today's digitally dominated signal processing systems. Universities across the world are restructuring their analog curriculum and are adopting the analog system design approach to bridge the gap between industry and the academia to offer their students an advantage when they enter in the industry.

All electronic systems today require a low power, low noise front-end and high power, high efficiency back-end which are purely analog systems. With the evolution of devices, analog circuit has migrated from vacuum tubes to Bipolar Junction Transistors [BJTs] to MOSFET, which may be replaced by new devices of the future. However, the building blocks like op amps, multipliers and comparators will always remain the basic functional blocks of a system design, irrespective of the device technology used for them. Therefore, teaching should be geared towards designing with these building blocks. The primary goal is to get students excited about the current analog signal processing practices at an application level and then move towards designing analog sub-systems. Hence, the curriculum should start with applications leading to designing of analog sub systems using building blocks like op-amps, comparators & multipliers followed by device theory.

To effectively absorb analog system design using the basic building blocks apart from simulation, the lab must expose the students to hands-on exercises and should be an integral part of the theory course. It must not be isolated from the theory course. The lab must correlate with the flow of the theory sessions and have the same faculty teaching both theory and lab to ensure students experience what they learn in the class. Each experiment should be focused on measuring and analysing macro model parameters input/output and transfer characteristics of integrated circuits (ICs) and their effects. Students must also practice fault finding in circuits with deliberately introduced faults to build problem solving skills. It is with this approach, we have designed the ASLK PRO and the Analog System Lab Manual.

In this book, we have incorporated certain features to ensure that the students effectively learns about the analog systems design

1. Systems approach for teaching analog systems. We have followed analog systems approach while explaining and designing various application circuits wherein op-amps, multipliers and comparators are considered as the basic building block for building any application.
2. Through analysis of analog systems. In view of the systems approach the focus is on the analysis of systems parameters of the building blocks to help understand the behavior of the system in a comprehensive manner.
3. Worked out practical examples and exercises. Adequate problems and solutions are included in the text book to help students analyze and correlate the system behavior for varies applications in simulation and practical implementation.

As an outcome of this approach, we expect the students to be able to understand and analyse the characteristics of any analog IC, select analog ICs based on specifications of a given application, design efficient analog systems and be able to perform any fault diagnosis of an electronic systems. It will also help the universities to be able to bridge the gap between academia and Industry by ensuring the students have the right skills when they join the Industry.

Introduction to Operational Amplifiers and Characteristics

This chapter seeks to introduce readers to elementary concepts regarding Linear Integrated Circuits (LIC) and operational amplifiers (Op-Amp). It covers topics such as the need for LICs and Op-Amps, their basic components, configurations (open and closed loop) and various types of Op-Amps.

As powering the Op-Amp plays a major role in its applications, this chapter also delves into various power supply configurations of Op-Amps.

The knowledge acquired in this chapter will serve as a solid base for students as they learn how to build their own application circuits in subsequent chapters.

Topic	Page
1.1 Introduction	14
1.2 Linear integrated circuits and op-amp	15
1.3 Block diagram	16
1.4 Characteristics and equivalent circuits of an ideal op-amp	17
1.5 Various Types of operational amplifiers and applications	20
1.6 Power Supply Configurations of Op-Amp	21
1.7 Inverting and non inverting amplifier configurations	23
1.8 Summary	28
1.9 Review Questions	29
1.10 Exercises	30

1.1 Introduction

Integrated circuits (IC) have revolutionized the world of electronics. They are used in virtually all electronic equipment today in applications including audio and radio communication, medical electronics and instrumentation control. Computers, mobile phones and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of integrated circuits.

There are several parameters that need to be measured in real-life for various applications. These include temperature, humidity, air pressure etc., the values of which can change continuously. Sensors are used to monitor parameters and reflect any change in values on a continuous basis in the monitored range. Signals from these sensors can be measured either in analog or digital form. In most cases, the sensor produces an electrical voltage or current value that corresponds proportionally to the monitored physical quantities. These signals are then processed further to obtain useful information about the environment condition.

Standard electrical signal values are the norm while using this processing technology. In general, sensor output values vary between current values of 4 to 20 mA or voltage values of 0 to 10 V, corresponding to the value of the physical quantity being measured.

Circuit design plays a major role in instrumentation system design. Electronic circuits for some of the applications listed above can be designed in either analog circuit design or digital circuit design

Operational amplifier is an important linear IC. Generally, Op-Amps are depicted as circuit blocks in amplifier circuits as this is much easier and clearer than specifying all their individual circuit elements like transistors and resistors.

Table 1.1: Comparison between digital and analog circuits

	Digital Circuits	Analog Circuits
Pros	Less susceptible to noise (small, undesired variations in voltage)	Enable a wide range of complexity right from a simple configuration (like two resistors combined to make a voltage divider) to very elegant designs with many components
Cons	Use more energy than analog circuits to accomplish the same tasks, thus producing more heat and increasing complexity of circuits (needs the inclusion of heat sinks). Inherently limited in their precision because they must count in fixed units. (Example: Most digital thermometer shave only one digit to the right of the decimal point. Can indicate a temperature of 98.6 or 98.7 but not 98.65)	Usually much more susceptible to noise. Small changes in the voltage level of an analog signal may produce significant errors when being processed.

Op-Amps have several applications in day to day life.

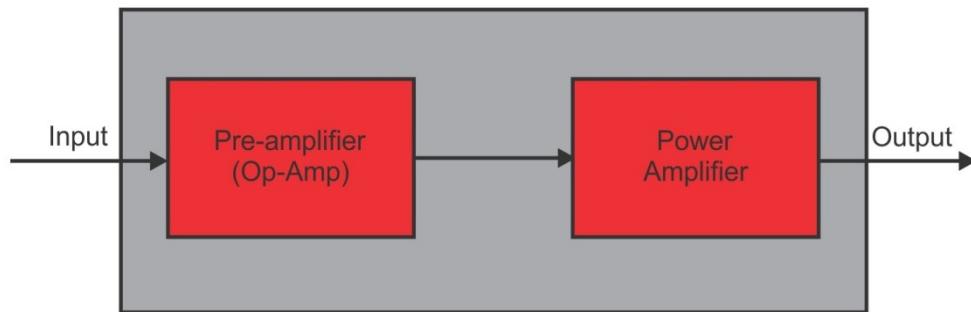


Fig 1.1 Tone controller for guitar amplifier

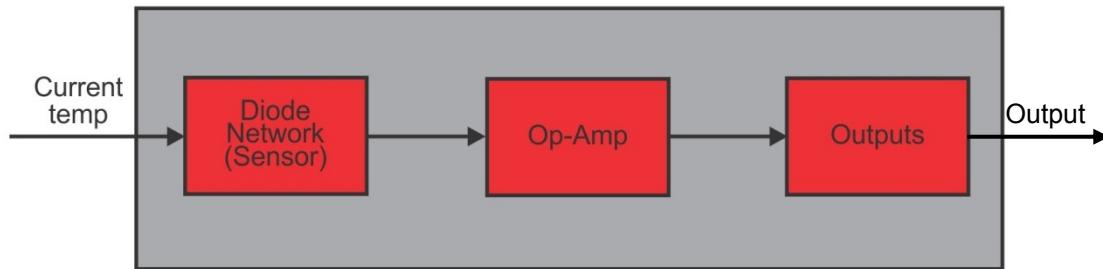


Fig 1.2 Temperature deviation indicator

1.2 Linear integrated circuits and op-amp

A linear integrated circuit (linear IC) is an analog device that operates over a continuous range of input levels. In contrast, a digital IC has a finite number of discrete input and output states. Linear integrated circuits are found in four main areas - power amplifiers, high frequency amplifiers, differential operational amplifiers and voltage regulators.

They have a wide variety of day-to-day applications. For instance, Integrated Circuits are a major component in microphones, power supply (AC to Dc conversion) etc.

The most commonly used and popular Linear IC is the Operational amplifier. Differential operational amplifiers exemplify the type of circuit that is used in all the four areas listed above and is suited for integrated-circuit (IC) technology.

An operational amplifier has multiple terminals and is internally quite complex. It is an extremely efficient and versatile device. Its applications span the broad electronic industry especially in signal conditioning, special transfer functions, analog instrumentation, analog computation, and special systems design.

Operational amplifiers

Originally, the term, "Operational Amplifier," was used in the computing field to describe amplifiers that performed various mathematical operations. It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of feedback components, operational amplifier circuits could be used to add, subtract average, integrate and differentiate.

As practical operational amplifier techniques became more widely known, it was apparent that these feedback techniques could be useful in many control and instrumentation applications. Op-amp was originally used to perform mathematical functions like addition, integration, differentiation and sign-changing but now is found in many control system applications.

Today, the general use of operational amplifiers has been extended to include such applications as DC & AC Amplifiers, Comparators, Servo Valve Drivers, Deflection Yoke Drivers, Low Distortion Oscillators, AC to DC Converters, Multi-vibrators and a host of others. With a good working knowledge of their characteristics, the user will be able to exploit the useful properties of op-amps.

The IC is considered as a “black box” device and referred to its schematic structure as in Fig. 1.3. The general purpose op-amp is of the differential type with both inverting and non-inverting inputs.

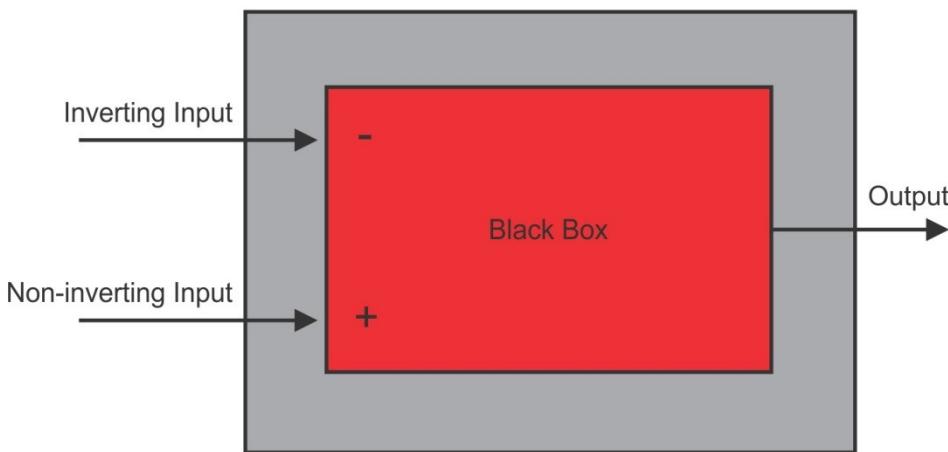


Fig 1.3 Dual-input differential operational amplifier

1.3 Block diagram

The operational amplifier is built upon the four discrete electronic circuits in cascade as given in Fig 1.4.

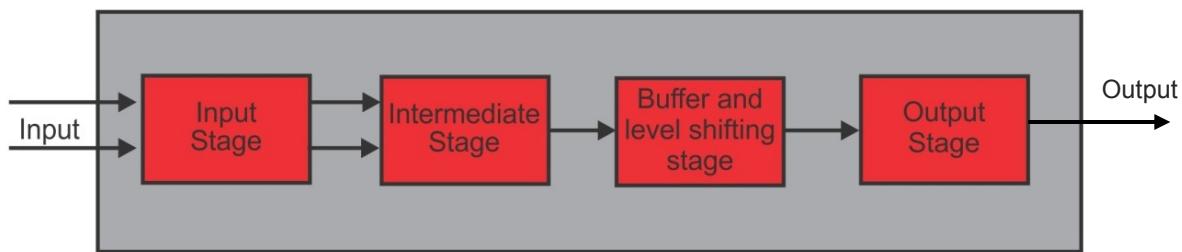


Fig 1.4 Block diagram of an operational amplifier

Input stage

It consists of a dual input, balanced output differential amplifier. Its function is to amplify the difference between the two input signals. It provides high differential gain, high input impedance and low output impedance.

Intermediate stage

The overall gain requirement of an Op-Amp is very high. Since the input stage alone cannot provide such a high gain. Intermediate stage is used to provide the required additional voltage gain. It consists of another differential amplifier with dual input, and unbalanced (single ended) output.

Buffer and Level shifting stage

As the Op-Amp amplifies even D.C. signals, the small D.C. quiescent voltage level of previous stages may get amplified and get applied as the input to the next stage causing distortion the final output. Hence the level shifting stage is used to bring down the D.C. level to ground potential, when no signal is applied at the input terminals. Buffer usually consists of an emitter follower used for impedance matching.

Output stage

It consists of a push-pull complementary amplifier which provides large A.C. output voltage swing and high current sourcing and sinking along with low output impedance.

1.4 Characteristics and equivalent circuits of an ideal op-amp

Op-Amps have five basic terminals. The circuit schematic is represented as a triangle with one output terminal, two input terminals (inverting and non-inverting) and two power supply terminals (positive V+ and negative V-). The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal. The symbol of op amp is shown in Fig 1.5.

If $V_1=0$, output V_0 will be 180° out of phase with the input signal V_2

If $V_2=0$, output V_0 will be in phase with the input signal V_1

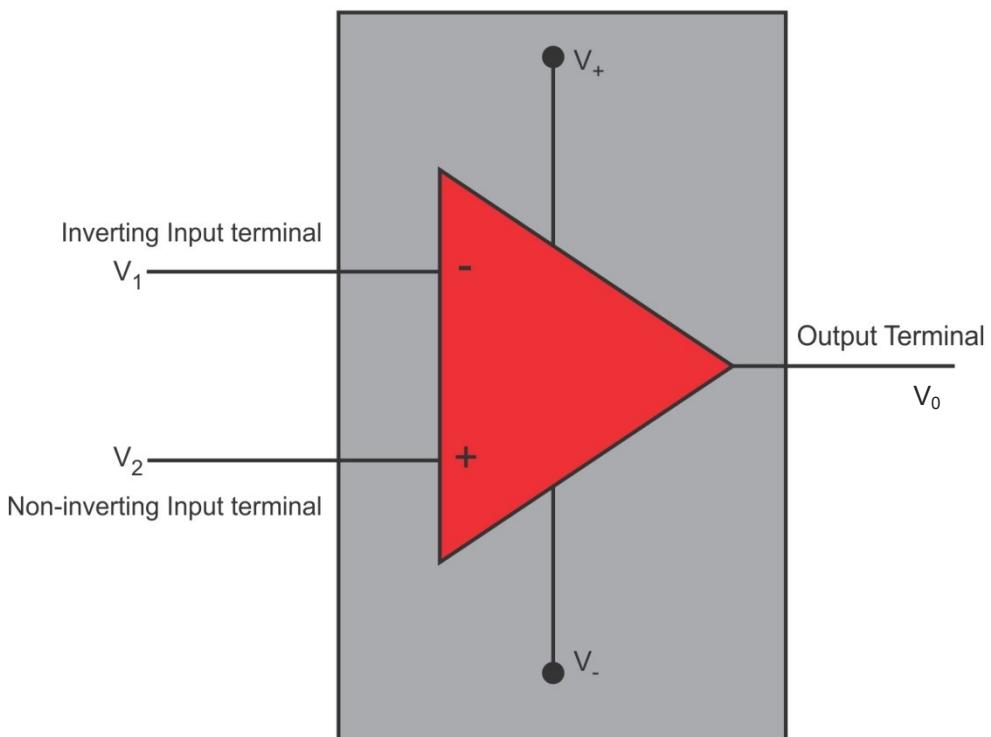


Fig 1.5 Symbol of operational amplifier

1.4.1 Characteristics of Ideal Op-amp:

Although Op-Amps do not exhibit ideal behavior in practical applications, it is important to understand an ideal op-amp model since it simplifies the mathematics involved in op-amp circuits. The process of modifying these equations to eliminate errors in real-world applications is discussed in chapter 2.

The ideal op-amp draws no current at both the input terminals ($i_1 = i_2 = 0$) as shown in Fig 1.6. Due to infinite input impedance any signal source can drive it. There is no loading on the preceding driver stage.

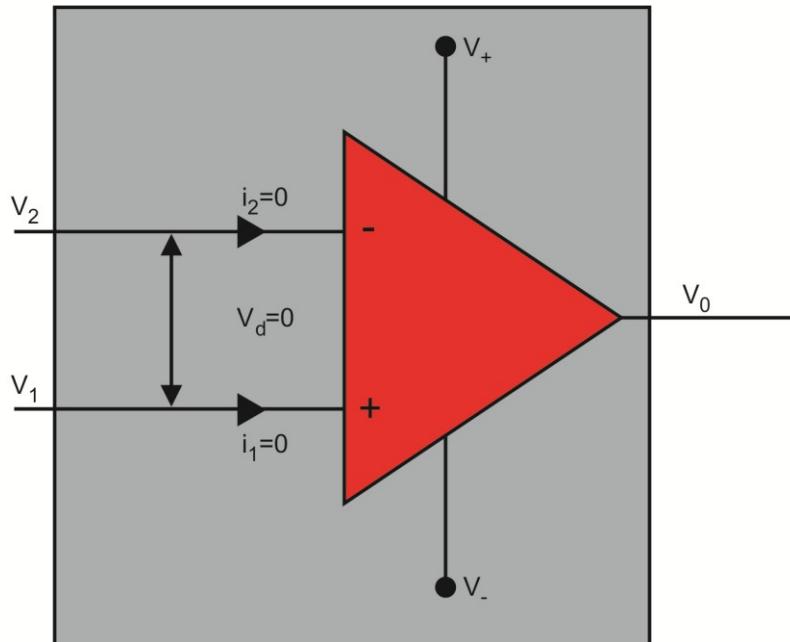


Fig 1.6 Ideal operational amplifier

The voltage between inverting and non-inverting input terminals is called difference input voltage $V_d = (V_1 - V_2)$ is zero for finite output voltage V_0 . The output voltage V_0 is independent of the current drawn from the output as $R_o = 0$. The output can drive an infinite number of other devices.

As mentioned above, a physical amplifier is not an ideal one and will not behave in the same as the ideal one. So the gain and input resistance is not infinite and the output impedance is not zero.

The op-amp is said to be ideal if it has the following characteristics.

- Infinite voltage gain A.
Voltage gain A is defined as the ratio of output voltage to input voltage i.e.

$$\begin{aligned} A &= \frac{V_0}{V_{in}} \\ &= \frac{V_0}{V_d} \end{aligned}$$

Differential voltage of an ideal op-amp is zero i.e. $V_d = 0$

$$A = \frac{V_0}{0}$$

$$A = \infty$$

- Infinite input resistance R_i .
Ideal op-amp offers infinite input resistance and hence the ideal op-amp draws no current ($i_1=i_2=0$).
- Zero output resistance R_o .
Ideal op-amp offers zero output resistance so that the output can drive an infinite number of other devices.
- Zero output offset.
The output offset is the output voltage of an amplifier when both inputs are grounded output voltage, when input voltage is zero. Ideal op-amp possesses zero output offset.
- Infinite bandwidth.
An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies without attenuation.
- Infinite common mode rejection ratio.
Common-mode rejection ratio (CMRR) is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification.

$$A = \frac{A_{DM}}{A_{CM}}$$

A_{DM} – Differential mode gain

A_{CM} – Common mode gain

Ideally, this ratio would be infinite with common mode voltages being totally rejected. The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, a change the bias point changes the offset voltage. This, in turn, changes the output voltage.

In a Op-Amp data sheets, the CMRR is given as a positive number in decibels (dB). CMRR, as published in data sheets, is a DC parameter. When graphed vs. frequency, CMRR falls off as the frequency increases.

- Infinite slew rate.
Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are $V/\mu s$ or V/ms . Higher the slew rate, faster is the op-amp. Ideal Op-Amp has Infinite slew rates o that output voltage changes occur simultaneously with input voltage changes.

1.4.2 Equivalent circuit of op-amp

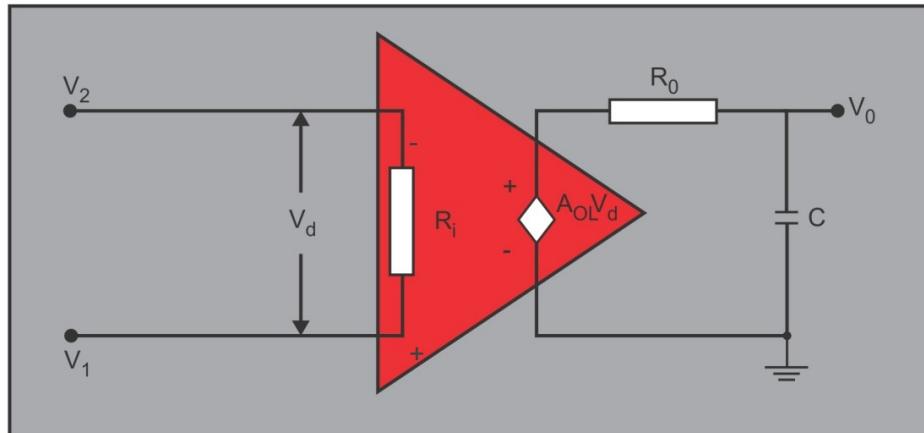


Fig 1.7 Equivalent circuit of operational amplifier

An Op-Amp can be realized by Thevenin's equivalent circuit and given in Fig 1.7. Where voltage controlled source $A_{OL}V_d$ is an equivalent Thevenin voltage source and R_0 is the Thevenin resistance.

1.5 Various Types of operational amplifiers and applications

Modern op amps fall into several categories and their parameters are tabulated as given in Table 2.

The very first series of modular solid-state op-amps were introduced by Burr-Brown Research Corporation and G.A. Philbrick Researches Inc. in 1962. The first solid-state monolithic op-amp, designed by Bob Widlar and offered to the public in 1963 was the μ A702.

Manufactured by Fairchild Semiconductors, it had very unusual supply voltages such as +12 and -6 volts and had a tendency to burn out when it was temporarily shorted. It had higher gain, a larger bandwidth, lower input current, and a more user-friendly supply voltage requirement of approximately +/- 15 Volt DC.

Table 1.2: Various types of operational amplifiers by Texas Instruments

Op-Amp types	Slew rate at unity gain	CMRR (typical)	Input impedance	Total power dissipation
General Purpose (μ A741)	0.5V/ μ S	90dB	2 Mega Ω	100mW
FET inputs(TL082-Q1)	13V/ μ S	86dB	1 Tera Ω	75mW
CMOS (LMC6482QML)	0.9V/ μ S	62dB	10 Tera Ω	160mW
Chopper stabilized(LTC1052)	4 V/ μ S	120dB	>10 Tera Ω	100mW

In December 1968, an improved version of the LM101, the LM101A, was devised. This device provided better input control over the temperature and lower off set currents. National Semiconductor introduced the LM107, which had the frequency compensation capacitor built into the silicon chip. The LM107 came out at the same time as the LM101A. In 1968, Fairchild Semiconductor issued the μ A748. The device had essentially the same performance characteristics as the μ A741. The difference was external frequency compensation.

The first multiple Op-Amp device was Raytheon Semiconductor's RC4558 in 1974. Characteristics of this new device were similar to the μ A741 except that the latter used NPN input transistors.

Later in that same year, the LM324 quad Op-Amp from National Semiconductor became public to the delight of manufacturing industry. It was similar in characteristics in comparison with the μ A741 in speed and input current. The LM324 is especially useful for low-power consumption.

The first commercial Op-Amp by Texas Instruments, the K2-W, utilized two dual section tubes (4 active circuit elements) to facilitate differential inputs and outputs. It required a ± 300 V_{dc} power supply, dissipating 4.5 W of power. It had a corner frequency of 1 Hz, and a gain bandwidth product of 1 MHz. Texas Instruments introduced the TL084 Op-Amp in October 1976. It was quad JFET input Op-Amp; it also was an ion-implant JFET. Low bias current and high speeds were two of its beautiful attributes.

Today, the types of op amps available are increasing almost daily. There are varieties of Op-Amps that provide the users with essentially anything, including high common-mode rejection, low-input current frequency compensation, CMOS, and short-circuit protection.

Op-Amps are continually being improved, especially in the low noise areas. Op-Amps are further classified into RF amplifiers, audio and power amplifiers based on the output current ratings and applications.

1.6 Power Supply Configurations of Op-Amp

In the standard Op-Amp model, the V+ and V- power supply terminals are connected to two dc voltage sources. V+ is connected to positive terminal of one source and V- is connected to negative terminal of another source as shown in Fig 1.8. The voltage may range from $\pm 5V$ to $\pm 22V$. The common terminal of the V+ and V- sources is connected to a reference point or ground. The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it may damage op-amp. The main disadvantage of this power supply configuration is use of two power supplies.

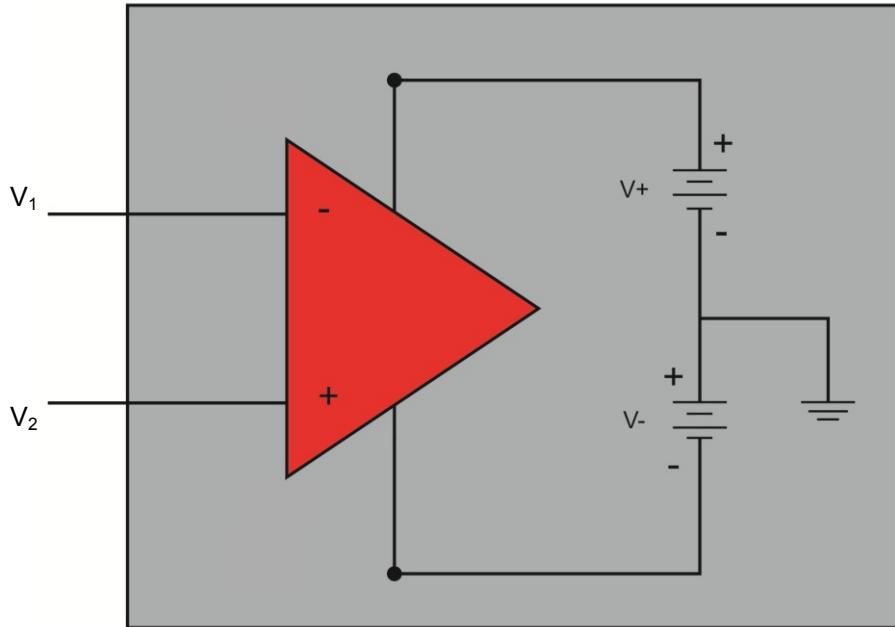


Fig 1.8 Power supply configuration using two power supplies

But it is possible to use a single power supply to obtain V+ and V- too as shown in Fig 1.9. In this circuit, R must be greater than $10K\Omega$ and capacitors provide decoupling of power supply and may range from $0.01\mu F$ to $10\mu F$.

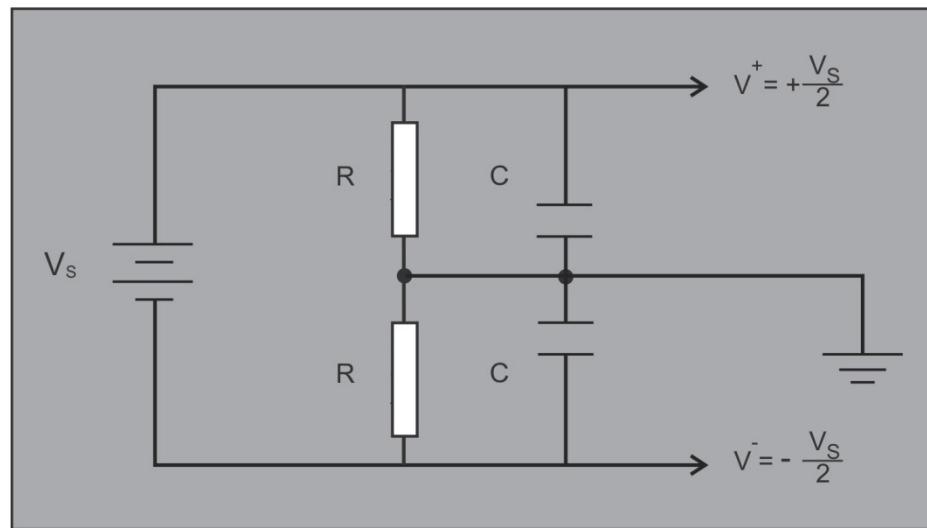


Fig 1.9 Power supply configuration using single power supply

In the circuit given in Fig 1.10, Zener diodes are used to give symmetrical supply voltages. R_s is chosen such that it supplies sufficient current for Zener diodes to operate in breakdown region.

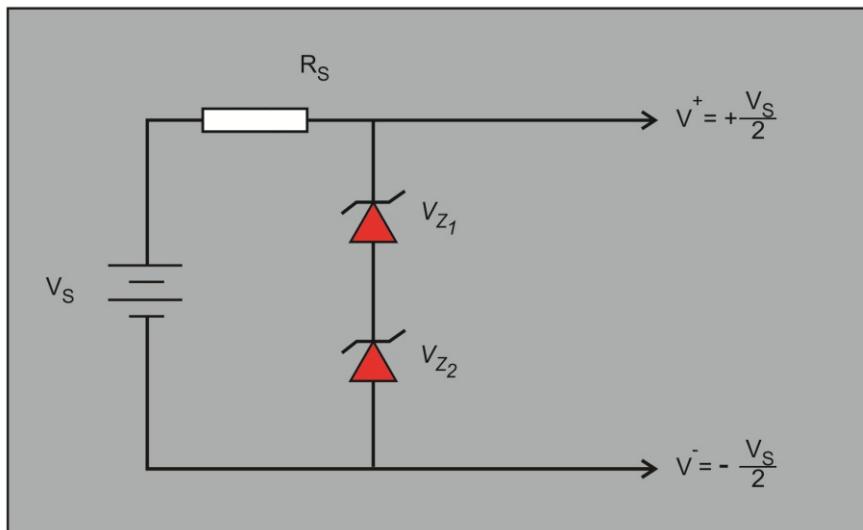


Fig 1.10 Power supply configuration using Zener diodes

A potentiometer can also be used to get equal voltage of V_+ and V_- as shown in Fig 1.11. D1 and D2 are used to protect the IC if positive and negative leads are accidentally reversed.

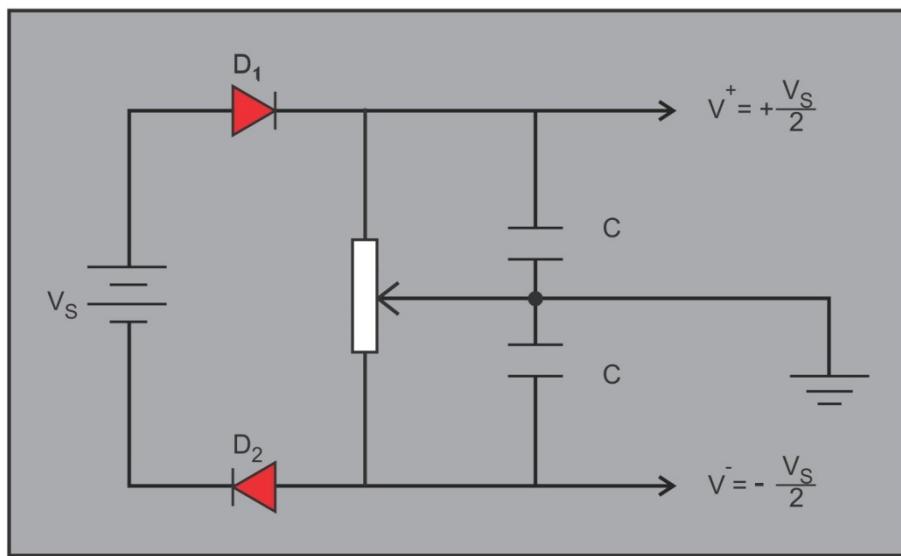


Fig 1.11 Power supply configuration potentiometer

1.7 Inverting and non inverting amplifier configurations

1.7.1 Open loop operation of Op-Amp

In the case of amplifiers, the term open loop indicates that no connection of any type exists between input and output terminals. The open loop configuration of Op-Amp is shown in Fig 1.12. That is, the output signal is not fed back in any form as part of the input signal .In open loop configuration, the Op-Amp functions as a high gain amplifier and switches its output between cut-off and saturation modes (Nonlinear operation).

Open loop gain is usually exceedingly high; in fact, an ideal operational amplifier has infinite open-loop gain. Typically an Op-Amp may have a maximal open-loop gain of around 10^5 . Normally, feedback is applied around the Op-Amp so that the gain of the overall circuit is defined and kept to a figure which is more usable.

The very high open-loop gain of the Op-Amp allows a wide range of feedback levels to be applied to achieve the desired performance. The open-loop gain of an operational amplifier falls very rapidly with increasing frequency. Along with slew rate, this is one of the reasons why operational amplifiers have limited bandwidth.

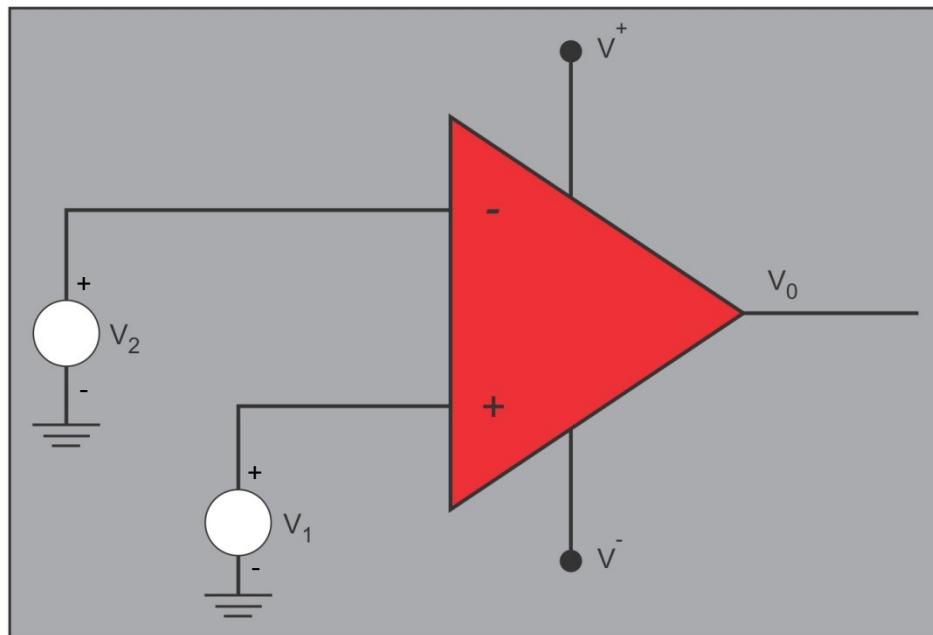


Fig 1.12 Open loop operation of operational amplifier

1.7.2 Closed loop configuration of Op-Amp

The open-loop operation is practical only when the operational amplifier is used as a comparator (a circuit which compares two input signals or compares an input signal to some fixed level of voltage). As an amplifier, the open-loop operation is not practical because the very high gain of the operational amplifier creates poor stability. (Noise and other unwanted signals are amplified in open-loop operation that the operational amplifier is usually not used in this way).

There are two feedback schemes employed in operational amplifiers, positive and negative feedback.

The negative feedback is an incredibly useful principle when applied to operational amplifiers. Negative feedback makes all these circuits stable and self-correcting. The basic principle of negative feedback is that the output tends to drive in a direction that creates a condition of equilibrium (balance). In an op-amp circuit with no feedback, there is no corrective mechanism, and the output voltage will saturate with the tiniest amount of differential voltage applied between the inputs.

Another type of feedback, namely positive feedback, also finds application in Op-Amp circuits. Unlike negative feedback, where the output voltage is “fed back” to the inverting (-) input, with positive feedback the output voltage is somehow routed back to the non-inverting (+) input.

Therefore, most operational amplifiers are used with negative feedback (closed-loop operation) for better stability. Closed loop configuration may also said to be linear operating mode of op-amp. Operational amplifiers are used with degenerative (or negative) feedback which reduces the gain of the operational amplifier but greatly increases the stability of the circuit.

This feedback is always degenerative (negative). In other words, the feedback signal always opposes the effects of the original input signal. One result of degenerative feedback is that the inverting and non-inverting inputs to the operational amplifier will be kept at the same potential. Closed-loop circuits can be of the inverting configuration or non-inverting configuration.

1.7.3 Inverting-configuration using ideal op amp

An operational amplifier in a closed-loop, inverting configuration is shown in Fig 1.13. Resistor R_f is used to feed part of the output signal back to the input of the operational amplifier. The node 'a' is said to be in virtual ground as $V_a = 0$.

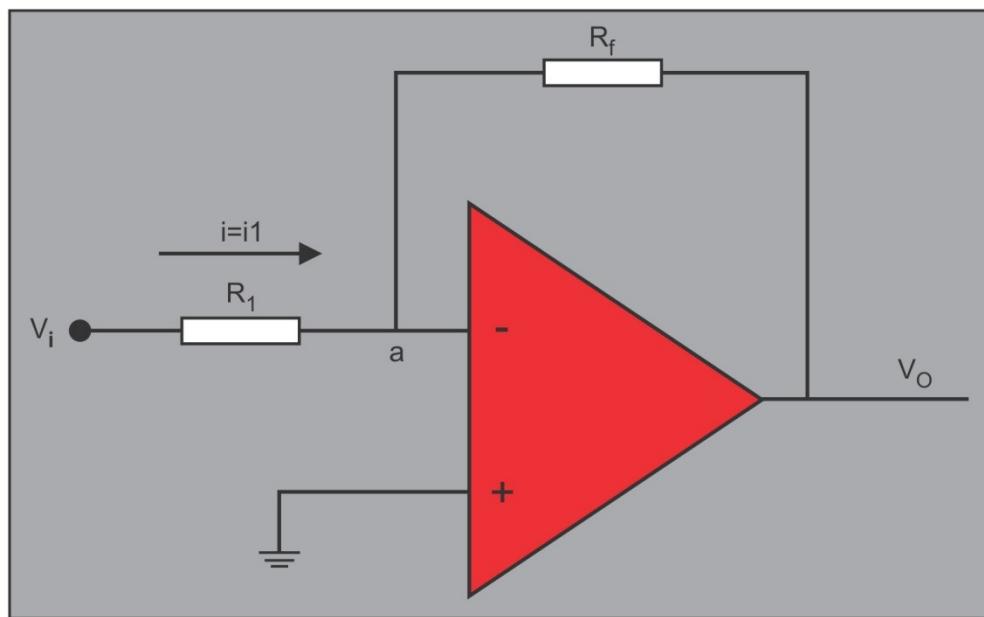


Fig 1.13 Inverting amplifier

Analysis

For simplicity, assume an ideal op-amp. As $V_a = 0$, node a is at ground potential and the current 'i', through R_1 is,

$$i_1 = \frac{v_i}{R_1} \quad (1.1)$$

$$v_i = i_1 R_1 \quad (1.2)$$

Also op-amp draws no current, all the current flowing through R_1 must also go through R_f .

$$v_o = -i_1 R_f \quad (1.3)$$

The gain of the inverting amplifier is

$$A_{CL} = \frac{v_o}{v_i} = \frac{-i_1 R_f}{i_1 R_1} = \frac{-R_f}{R_1} \quad (1.4)$$

The negative sign indicates a phase shift of 180° between v_i and v_o . The input impedance R_1 must be kept fairly large enough to avoid loading effect.

1.7.4 Non Inverting-configuration using ideal op amp

An operational amplifier in a closed-loop, non-inverting configuration is shown in Fig1.14.

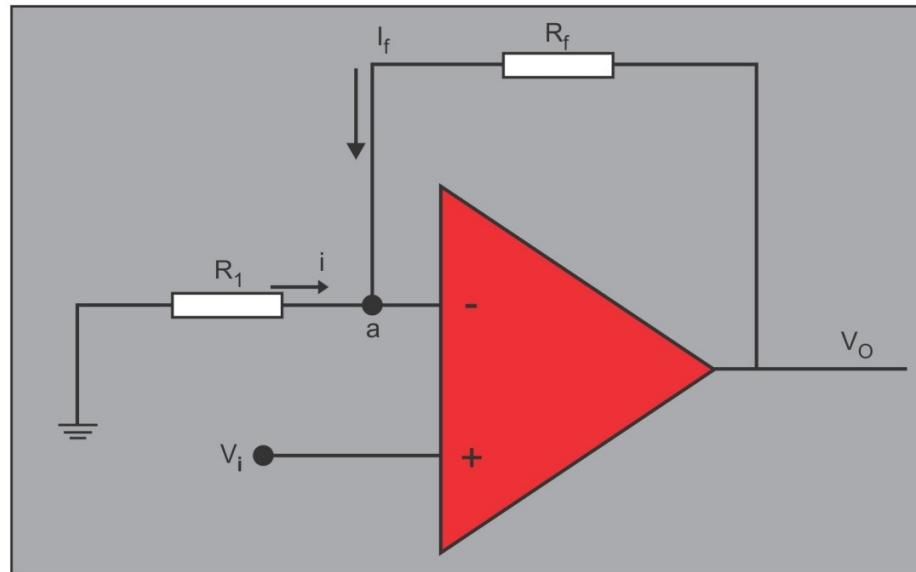


Fig 1.14 Non-Inverting amplifier

Resistor R_f is used to feed part of the output signal back to the input of the operational amplifier. The circuit amplifies without inverting the input signal. It is also a negative feedback system as output is fed back to the inverting input terminal.

Analysis

As the differential voltage at the input terminals of the op-amp is zero, at node 'a' using the potential divider network,

$$v_i = v_o \frac{R_1}{R_1 + R_f} \quad (1.5)$$

As no current flows into the op-amp

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} = A_{CL} \quad (1.6)$$

Alternatively, using Kirchoff's Current Law (KCL) at node 'a,'

$$\begin{aligned} \frac{v_i - v_o}{R_f} + \frac{v_i - 0}{R_1} &= 0 \\ v_i \left[\frac{1}{R_f} + \frac{1}{R_1} \right] &= \frac{v_o}{R_f} \end{aligned}$$

Simplifying the above,

$$v_i = v_o \frac{R_1}{R_1 + R_f}$$

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} = A_{CL} \quad (1.7)$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1 . The input resistance of non-inverting amplifier is extremely large as op-amp draws negligible current from the signal source.

Example 1.1

Design an amplifier with a gain of -10 and an input resistance of $10\text{ k}\Omega$.

Solution

Since the gain of the amplifier is negative, an inverting amplifier configuration has to be made. From (1.4)

$$A_{CL} = \frac{-R_f}{R_1}$$

$$\begin{aligned} R_f &= -A_{CL} R_1 \\ &= -(-10) \times 10 \text{ k}\Omega \\ &= 100 \text{ k}\Omega \end{aligned}$$

The design of above example is done in P-spice simulation software to check the output.

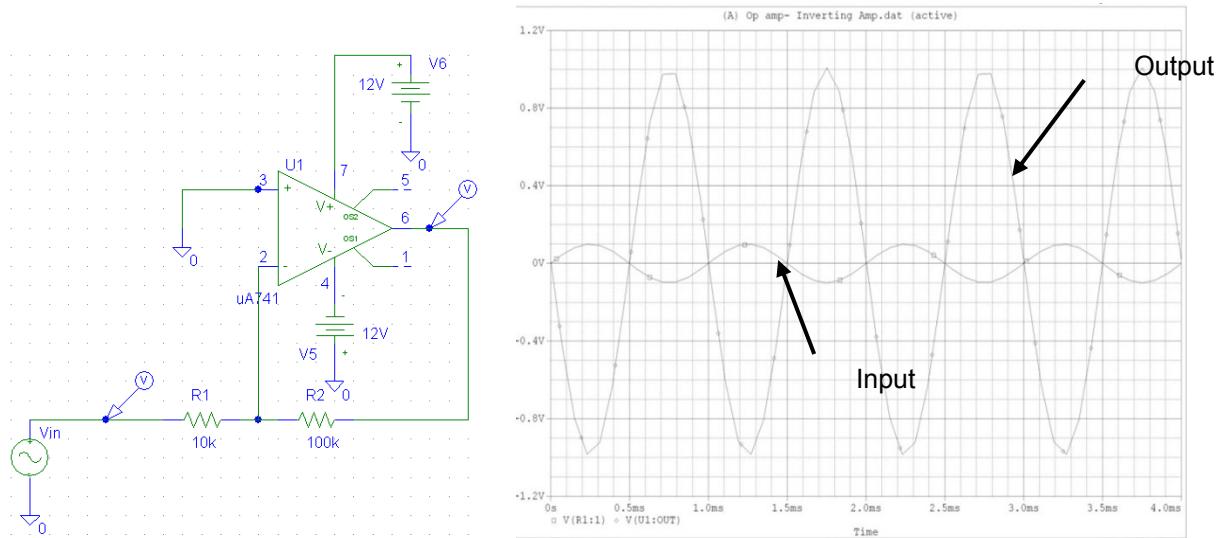


Fig 1.15 Design of inverting operational amplifier

Example 1.2

Design an amplifier with a gain of +5 using an op-amp.

Solution

Since the gain of the amplifier is positive, a non-inverting amplifier configuration has to be made. From (1.7)

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

Let $R_1 = 10 \text{ k}\Omega$

$$5 = 1 + \frac{R_f}{10\text{K}\Omega}$$

$$\begin{aligned} R_f &= 4 \times 10\text{K}\Omega \\ &= 40 \text{ K}\Omega \end{aligned}$$

The design of above example can be done in P spice simulation software to check the output.

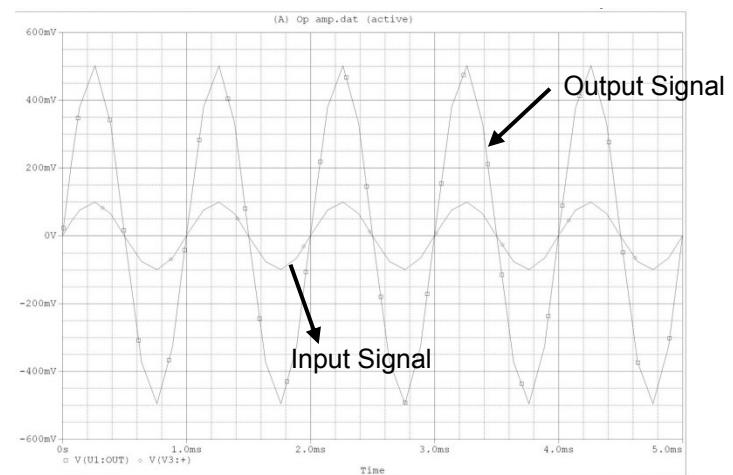
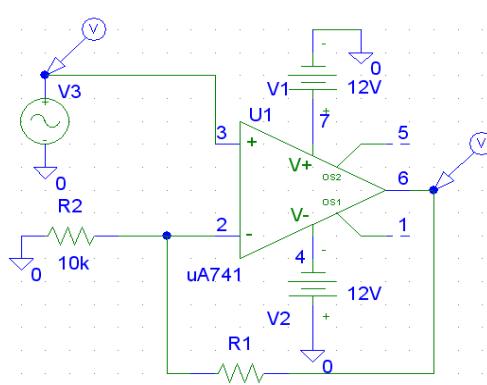


Fig1.16 Design of inverting operational amplifier

1.8 Summary

- An IC is a low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. An operational amplifier is the most commonly used type of a Linear IC.
- An Op-Amp has five basic terminals: two input terminals, one output terminal and two supply terminals
- Two power supply units must be used to power an operational amplifier.
- Various changes are made in op-amp manufacturing methods so as to cater various industrial applications.
- In open loop mode, the output of the Op-Amp is at positive or negative saturation level. It does not operate linearly in this mode.
- Negative feedback stabilizes gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.

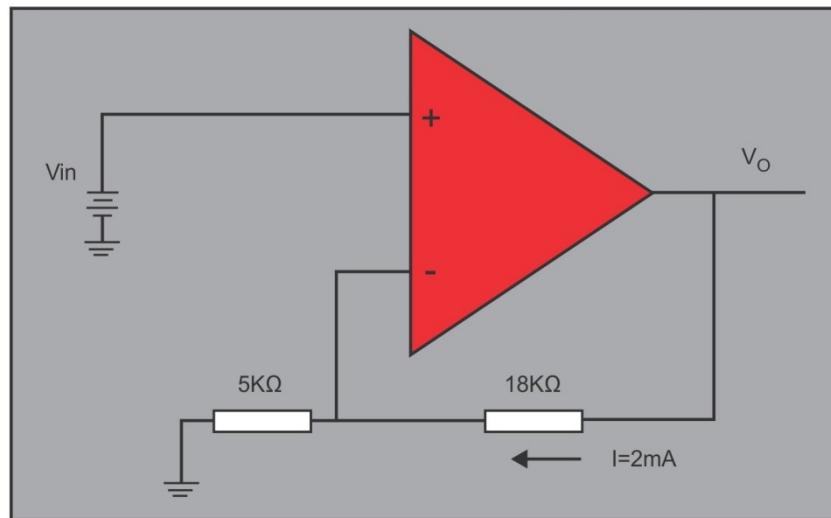
- With the knowledge acquired in the chapter 1, the readers will be able to build application circuits which are to be discussed in forthcoming chapters.

1.9 Review Questions

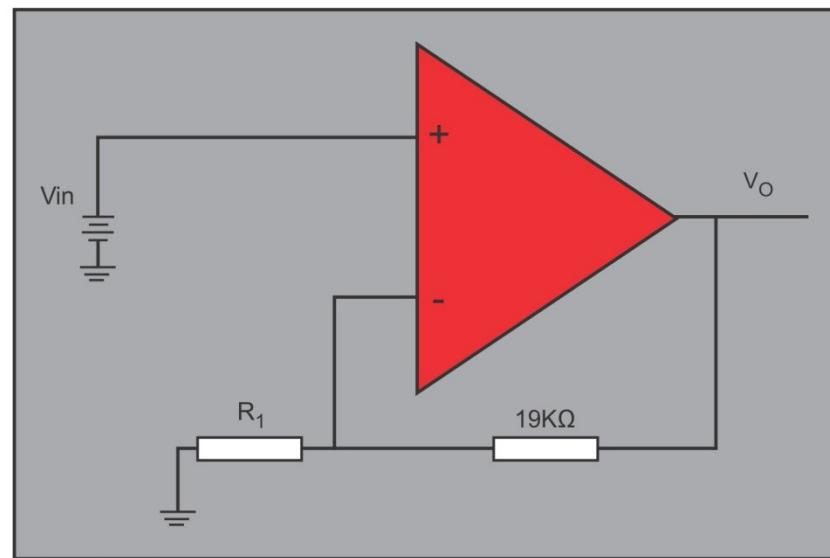
- Justify the term “operation” associated with respect to operational amplifier.
- Name the five basic terminals of an operational amplifier.
- How do you identify power supply common on a circuit schematic?
- When an operational amplifier is said to be operating in the linear region?
- What do you understand by the term “open loop gain of the operational amplifier”?
- List the characteristics of an ideal operational amplifier.
- Explain with figures how two supply voltages V+ and V- are obtained from single supply.
- Explain the meaning of open loop and closed loop operation of an op-amp.
- Derive an expression for output voltage in inverting amplifier configuration.
- Derive an expression for output voltage in non-inverting amplifier configuration.

1.10 Exercises:

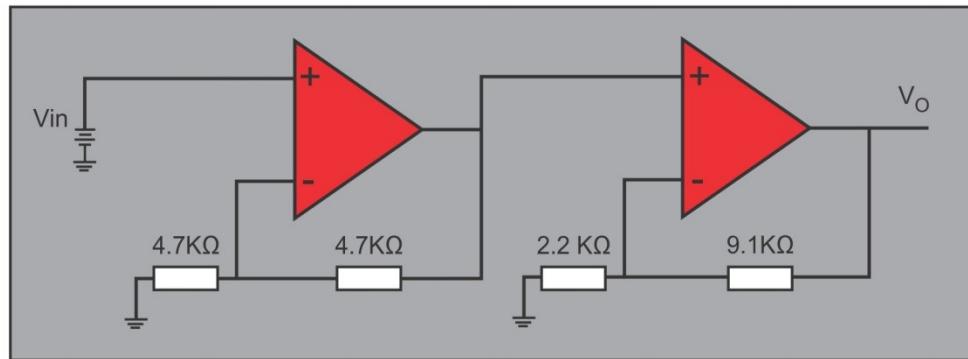
1. Determine both the input and output voltage in this circuit.



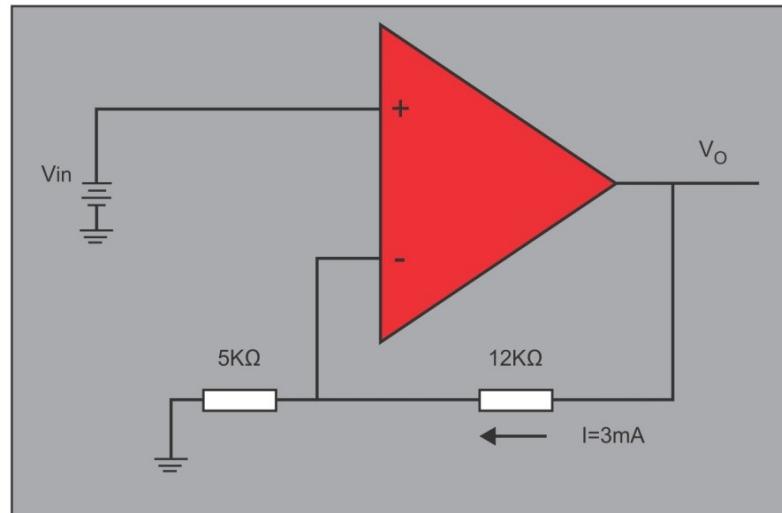
2. Calculate the necessary resistor value (R_1), in this circuit to give a voltage gain of 30.



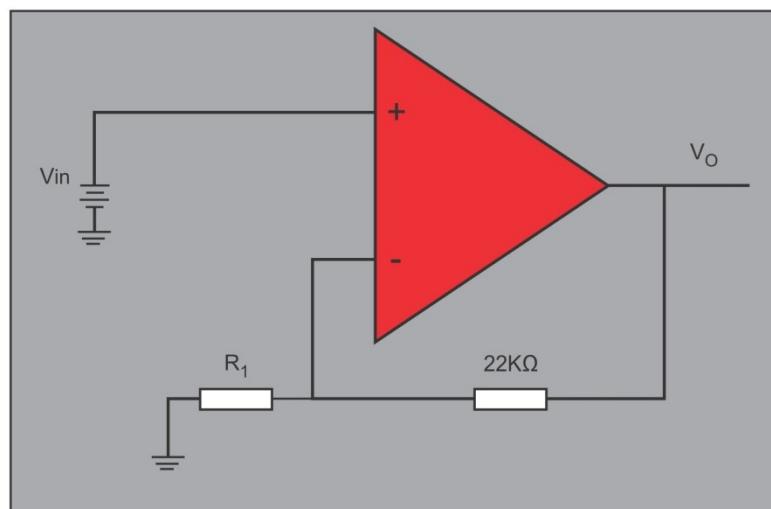
- 3. Calculate the voltage gain for each stage of this amplifier circuit, and then calculate the overall voltage gain.**



- 4. Determine both the input and output voltage in this circuit**



- 5. Calculate the necessary resistor value (R_1), in this circuit to give a voltage gain of 15.**



Practical Operational Amplifiers

The earlier chapter was focused on the characteristics of an ideal operational amplifier. In real life applications, operational amplifiers do not exhibit ideal characteristics, thereby introducing errors into results obtained.

This chapter covers parameters of various types of practical operational amplifier and ways to estimate the percentage error caused by finite gain when compared to that of ideal amplifier.

Specifically, we analyze the effect of finite loop gain on input and output resistances; cover methodology for evaluating offset voltage at the output of operational amplifier; estimating gain-bandwidth product and frequency response of an operational amplifier as well as interpreting parameters of TL082 and design amplifier circuits using TL082.

Topic	Page
2.1 Introduction.....	33
2.2 Effect of Finite Loop Gain on Closed Loop Gain.....	34
2.3 Effect of finite loop gain on Input Resistance R_{in}	42
2.4 Effect of finite gain on output resistance R_{out}	44
2.5 Voltage follower or Buffer Amplifier.....	47
2.6 <i>Input offset and Input Bias current</i>	49
2.7 Input Offset Voltage	53
2.8 Thermal Drift.....	55
2.9 Common Mode Rejection ratio (CMRR)	57
2.10 Slew rate and its effects	59
2.11 Power Supply Rejection Ratio (PSRR)	60
2.12 Frequency Response	61
2.13 Interpretation of TL082 Data sheet	68
2.14 Summary	73
2.15 Review Questions	74
2.16 Exercises.....	75

2.1 Introduction

The parameters of a practical Operational Amplifiers differ from that of an ideal device. When using an operational amplifier in real life applications, it becomes essential to estimate various errors caused by non-ideal parameters. The assumptions made for an ideal operational amplifier can be classified to two categories as given below:

Infinite value for parameters such as open loop gain, bandwidth, input resistance, common-mode rejection and power supply rejection

Zero value for input-bias currents, input offset current, input-offset voltage and output resistance.

Before we take up the analysis of circuits with non-ideal parameters, below is a comparison of the typical parameters of a few practical operational amplifiers. The table 2.1 below lists the parameters of an ideal Op-Amp versus a general purpose operational Amplifier LM741, high speed operational amplifier LM6171 and wide BW dual JFET operational amplifier TL082.

Table 2.1 Parameter values for ideal and non-ideal operational amplifiers

S.No	Parameters	Ideal Device	General purpose LM 741	High Speed LM 6171	Wide BW Dual JFET TL082
1	Open loop voltage gain, A_{in} in dB	∞	100	90	110
2	Input impedance, Z_{in} (Ω)	∞	2×10^6	40×10^6	10^{12}
	Output impedance, Z_{o} (Ω)	0	75	14	50 (Max)
4	Offset Current, I_{io} (nA)	0	20	30	0.025 (25 pA)
5	Offset Voltage, V_{io} (mV)	0	2	1.5	5
6	Bandwidth, BW (MHz)	∞	1	70	4
7	Slew rate, SR (V/ μ s)	∞	0.7	750	13
8	Commonmode rejection ratio in dB	∞	90	110	100
9	Supply voltage rejection ratio	∞	96	95	100

The non-ideal parameters of the practical operational amplifiers give rise to various errors in the performances of operational amplifier circuits when compared to the results obtained using ideal operational amplifier parameters. Therefore it is important to understand the effect of non-ideal parameters on the Finite gain, Input Resistance, Output resistance, Common mode rejection ratio, Bandwidth, Slew rate, Offset currents, Offset Voltages and Power supply rejection ratio.

In this chapter, we analyze the effect of non-ideal parameters on the performance of operational amplifier circuits by using the simplified equivalent circuit of the operational amplifier.

2.2 Effect of Finite Loop Gain on Closed Loop Gain

Case (i) Inverting Amplifier

Let us consider an inverting amplifier with a feedback resistance of R_2 and an input resistance of R_1 . Let v_i be the input voltage and v_o be the output voltage. The inverting amplifier equivalent circuit is shown in Fig 2.1.

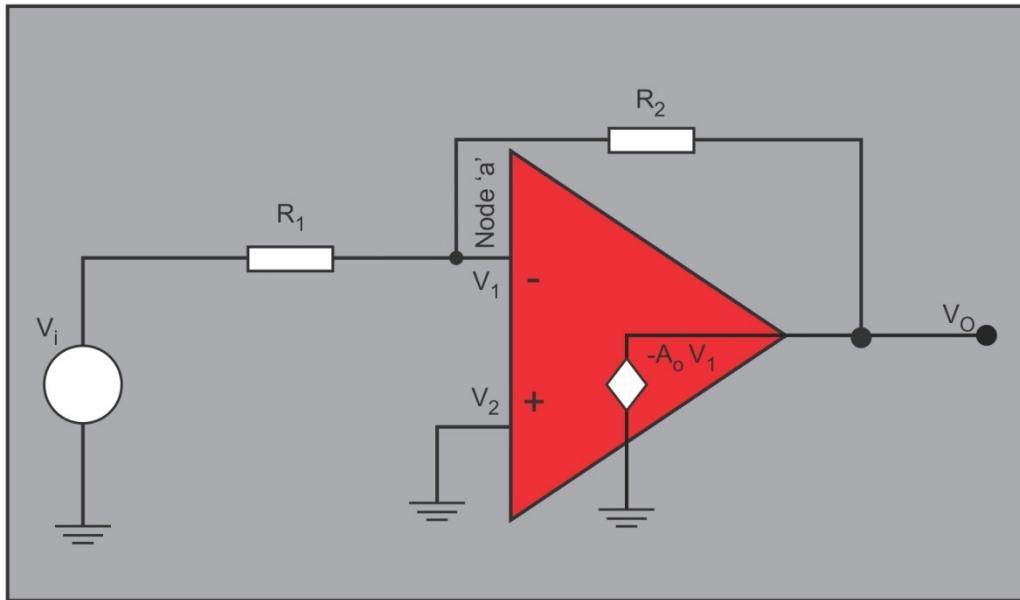


Fig.2.1 Analysis of Inverting Amplifier with finite open loop Gain

Consider the node 'a' shown in the Fig 2.1. Based on Kirchhoff's Current Law (KCL) we can write the nodal equation as given below

$$\frac{v_1 - v_i}{R_1} + \frac{v_1 - v_o}{R_2} = 0 \quad (2.1)$$

We know that output $v_o = -A_o(v_1 - v_2)$, $v_2 = 0$

$$\therefore v_1 = -\frac{v_o}{A_o}$$

Substituting in equation 2.1 we get

$$\begin{aligned} \frac{-\frac{v_o}{A_o} - v_i}{R_1} + \frac{-\frac{v_o}{A_o} - v_o}{R_2} &= 0 \\ \frac{v_o}{A_o R_1} - \frac{v_o}{A_o R_2} - \frac{v_o}{R_2} &= \frac{v_i}{R_1} \end{aligned}$$

$$\begin{aligned}
 -v_o \left[\frac{R_2 + R_1 + A_o R_1}{A_o R_1 R_2} \right] &= \frac{v_i}{R_1} \\
 \text{Non ideal gain } A_{iv} &= \frac{v_o}{v_i} = -\frac{A_o R_2}{R_2 + R_1 (1+A_o)} \\
 &= -\frac{R_2}{R_1 + \left(\frac{R_2 + R_1}{A_o} \right)} \\
 &= -\frac{R_2 / R_1}{1 + \frac{1}{A_o} (1 + \frac{R_2}{R_1})} \tag{2.2}
 \end{aligned}$$

Example 2.1 Evaluate % Error due to finite gains of value (i) $A_o = 10^3$ (ii) $A_o = 10^4$ (iii) $A_o = 10^5$, assuming R_1 as $10\text{K}\Omega$ and R_2 as $100\text{k}\Omega$.

For $A_o = 10^3$

$$\text{Non Ideal gain } A_{iv} = -\frac{100 \times 10^3}{10 \times 10^3 + \left\{ \frac{(100+10)10^3}{10^3} \right\}} = -\frac{100}{10 + 0.11} = -\frac{100}{10.11} = -9.89$$

$$\therefore \text{Error} = \frac{A_{ideal} - A_{iv}}{A_{ideal}} \times 100 = \frac{0.11}{10} \times 100 = 1.1\%$$

For $A_o = 10^4$

$$\text{Non ideal gain } A_{iv} = -\frac{100 \times 10^3}{10 \times 10^3 + \left\{ \frac{(100+10)10^3}{10^6} \right\}} = -\frac{100}{10 + 0.011} = -\frac{100}{10.011} = -9.99$$

$$\text{Error} = \frac{0.01}{10} \times 100 = 0.1\%$$

For $A_o = 10^5$

$$\begin{aligned}
 \text{Non ideal gain } A_{iv} &= -\frac{100 \times 10^3}{10 \times 10^3 + \left\{ \frac{110 \times 10^3}{10^7} \right\}} = -\frac{100}{10 + 0.0011} = -\frac{100}{10.0011} = -9.999 \\
 \text{Error} &= 0.01\%
 \end{aligned}$$

Effect of Finite Loop Gain on Closed Loop Gain
PSpice Simulation for Example 2.1:

```

Gain 1000
* Opamp
v.in 1 0 ac 3V sin( 0 3 50 0 0 0 )
Rg 1 2 10k
Rf 2 3 100k
X1 0 2 0 3 OpAmp
.SUBCKT OpAmp p_in n_in com out
Ex int com p_in n_in 1e3
Ri p_in n_in 200meg
Ro int out 75
.ENDS opamp
.TRAN 0.1MS 50MS
.probe
.end

```

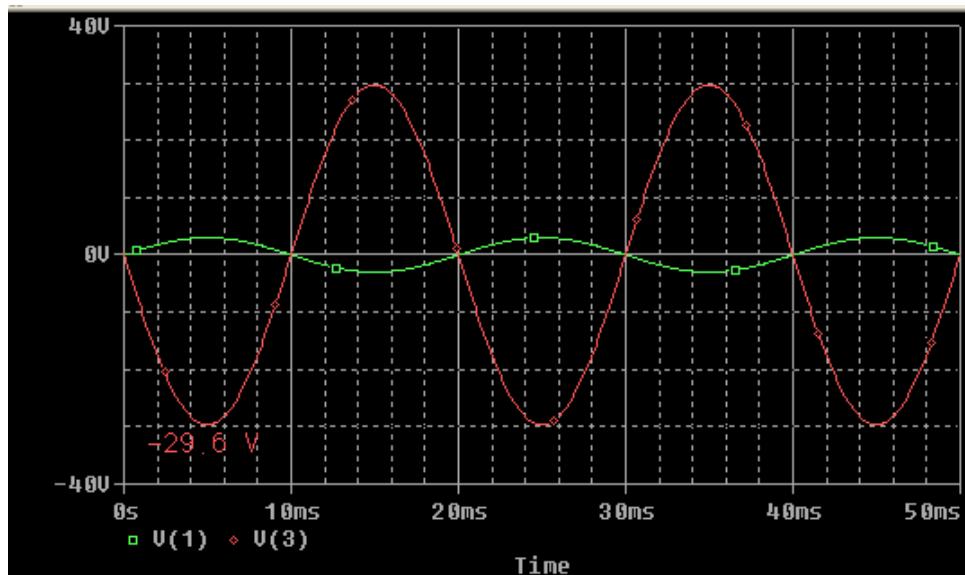


Fig 2.2 Simulation result of inverting opamp when $A_0 = 1000$

```

Gain 10000
* Opamp
v.in 1 0 ac 3V sin( 0 3 50 0 0 0 )
Rg 1 2 10k
Rf 2 3 100k
X1 0 2 0 3 OpAmp
.SUBCKT OpAmp p_in n_in com out

```

```

Ex int com p_in n_in 1e4
Ri p_in n_in 200meg
Ro int out 75
.ENDS opamp
.TRAN 0.1MS 50MS
.probe
.end

```

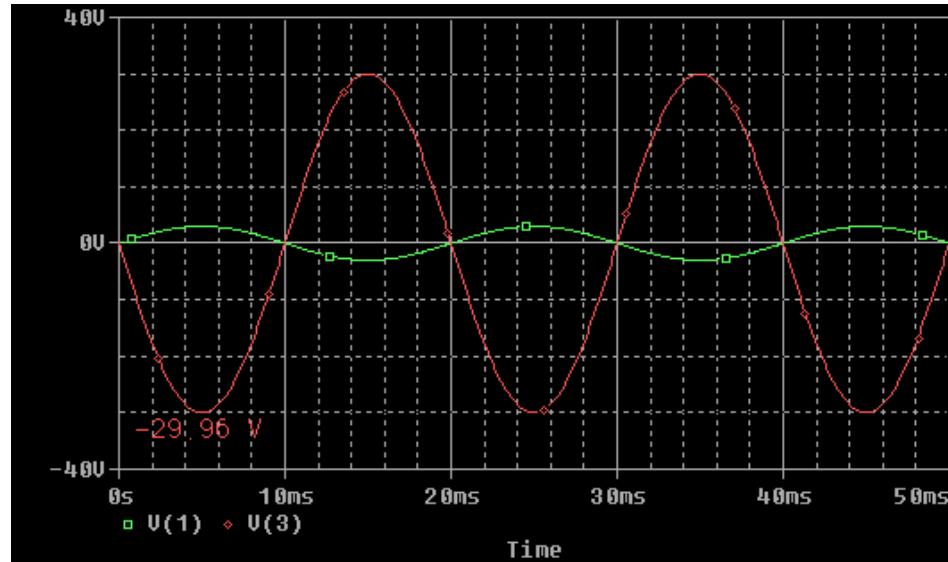


Fig 2.3 Simulation result of inverting opamp when $A_0 = 10000$

Case (ii) Non-inverting Amplifier

The equivalent circuit of the non-inverting amplifier is shown in Fig. 2.2

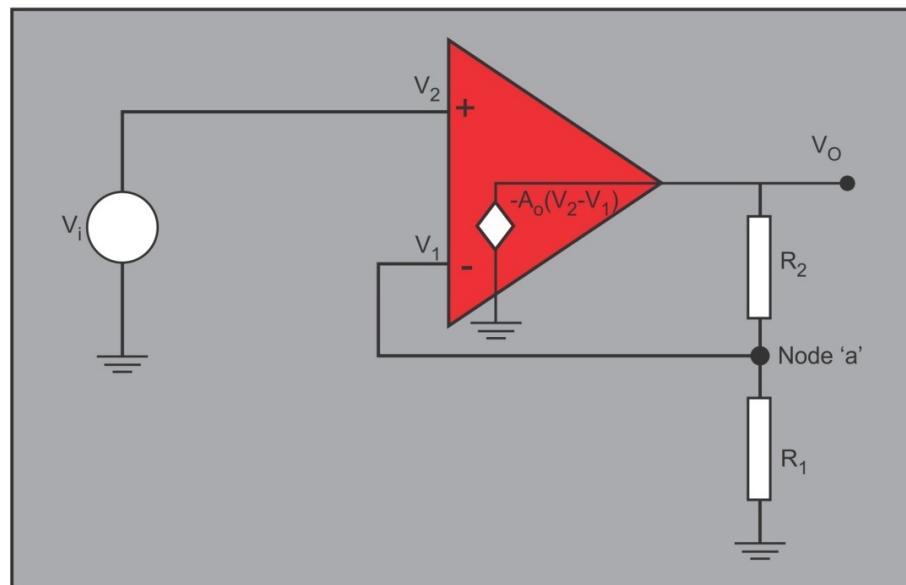


Fig.2.4 Analysis of non-inverting Amplifier with finite open loop Gain

Consider the node 'a' shown in the Fig 2.1. Based on KCL, we can write the nodal equation as given below

$$\frac{v_1}{R_1} + \frac{v_1 - v_0}{R_2} = 0 \quad (2.3)$$

We know that output voltage $v_0 = A_0(v_2 - v_1)$

$$\therefore v_1 = v_2 - \frac{v_0}{A_0}, v_2 = v_i$$

Substituting in Eq 2.3

$$\begin{aligned} \frac{v_i - (v_0/A_0)}{R_1} + \frac{(v_i - v_0/A_0) - v_0}{R_2} &= 0 \\ \frac{v_i}{R_1} - \frac{v_0}{A_0 R_1} + \frac{v_i}{R_2} - \frac{v_0}{A_0 R_2} - \frac{v_0}{R_2} &= 0 \\ v_0 \left[\frac{1}{A_0 R_1} + \frac{1}{A_0 R_2} + \frac{1}{R_2} \right] &= v_i \left[\frac{1}{R_1} + \frac{1}{R_2} \right] \\ v_0 \left[\frac{R_1 + R_2 + A_0 R_1}{A_0 R_1 R_2} \right] &= v_i \left[\frac{R_1 + R_2}{R_1 R_2} \right] \end{aligned}$$

$$\text{Closed loop gain } A_{ni} = \frac{v_0}{v_i} = \frac{A_0(R_1 + R_2)}{R_1 + R_2 + A_0 R_1}$$

$$A_{ni} = \frac{(R_1 + R_2)}{R_1 + (R_1 + R_2) \frac{1}{A_0}}$$

Dividing numerator and denominator by R_1 , we get

$$A_{ni} = \frac{1 + R_2/R_1}{1 + \frac{1}{A_0}(1 + R_2/R_1)} \quad (2.4)$$

Example 2.2: Find the % error introduced by the finite gain of the non – inverting amplifier with the following values $R_1 = 10 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $A_0 = 10^3, 10^4, 10^5$

Case (a) For $A_0 = 10^3$

$$A_{ideal} = 1 + \frac{R_2}{R_1} = 11$$

$$A_{ni} = \frac{1 + 10}{1 + \frac{11}{10^3}} = \frac{11}{1.011} = 10.88$$

$$\text{Error} = \frac{11 - 10.88}{11} = \frac{12}{11} = 1.09 \%$$

Case (b) For $A_0 = 10^4$

$$A_{ni} = \frac{1 + 10}{1 + \frac{11}{10^4}} = \frac{11}{1.0011} = 10.99$$

$$\% \text{ Error} = \frac{11 - 10.99}{11} \times 100 = \frac{1}{11} = 0.1\%$$

Case (c) For $A_0 = 105$

$$A_{ni} = \frac{11}{1 + \frac{11}{10^5}} = \frac{11}{1.00011} = 10.999$$

$$\% \text{ Error} = \frac{11 - 10.999}{11} \times 100 = 0.01\%$$

PSpice Simulation for Example 2.2

Gain = 1000

* Opamp

v.in 1 0 ac 3V sin(0 3 50 0 0 0)

R1 3 2 100k

R2 2 0 10k

Xopamp 1 2 3 OpAmp

.subckt OpAmp 1 2 4

Rin 1 2 200meg

Eamp 3 0 1 2 1e3

Rout 3 4 75

.ends OpAmp

.TRAN 0.1MS 50MS

.probe

.end

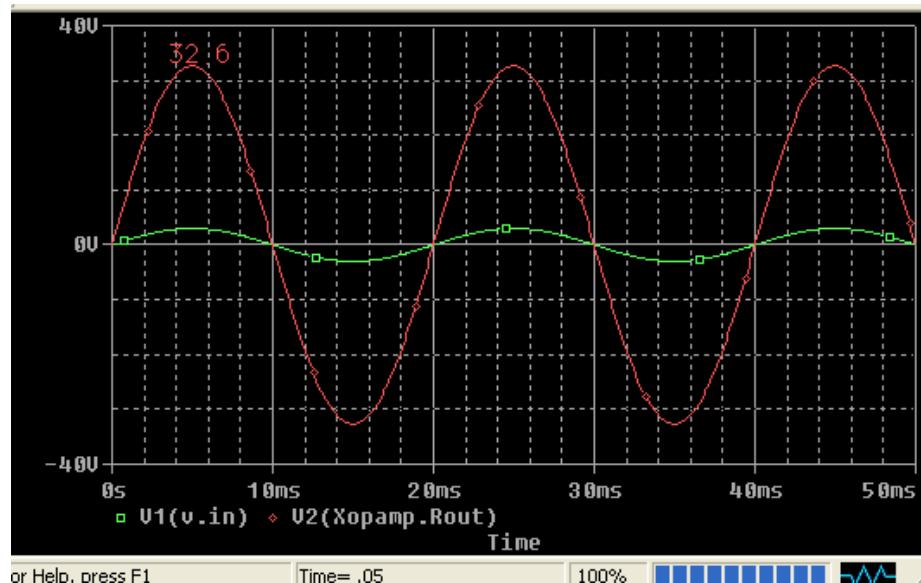


Fig 2.5 Simulation result of non-inverting OpAmp when $A_0 = 1000$

Gain = 10000

```
* Opamp
v.in 1 0 ac 3V sin( 0 3 50 0 0 0 )
R1 3 2 100k
R2 2 0 10k
Xopamp 1 2 3 OpAmp
.subckt OpAmp 1 2 4
Rin 1 2 200meg
Eamp 3 0 1 2 1e4
Rout 3 4 75
.ends OpAmp
.TRAN 0.1MS 50MS
.probe
.end
```

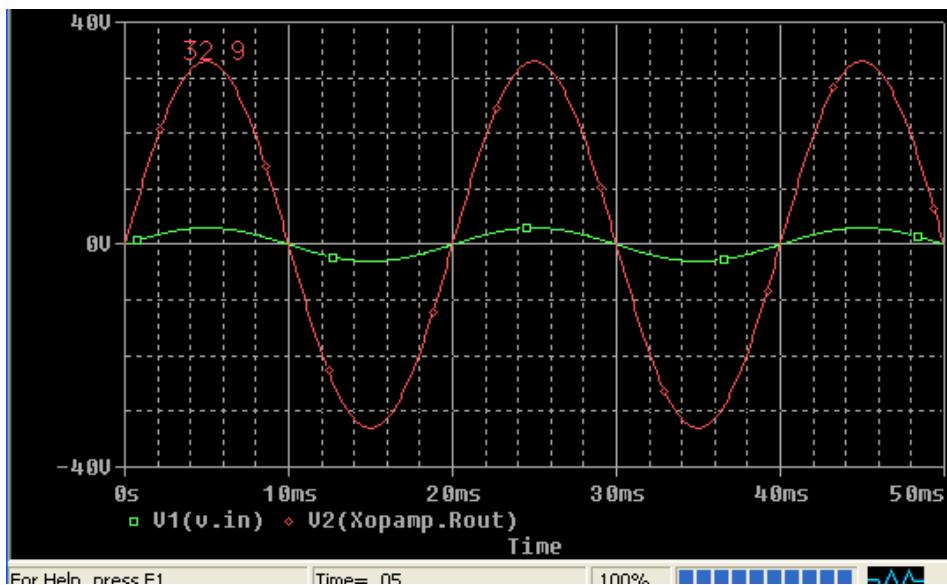


Fig 2.6 Simulation result of non-inverting opamp when A0 = 10000

Gain = 100000

```
* Opamp
v.in 1 0 ac 3V sin( 0 3 50 0 0 0 )
R1 3 2 100k
R2 2 0 10k
Xopamp 1 2 3 OpAmp
.subckt OpAmp 1 2 4
Rin 1 2 200meg
```

```
Eamp 3 0 1 2 1e5
```

```
Rout 3 4 75
```

```
.ends OpAmp
```

```
.TRAN 0.1MS 50MS
```

```
.probe
```

```
.end
```

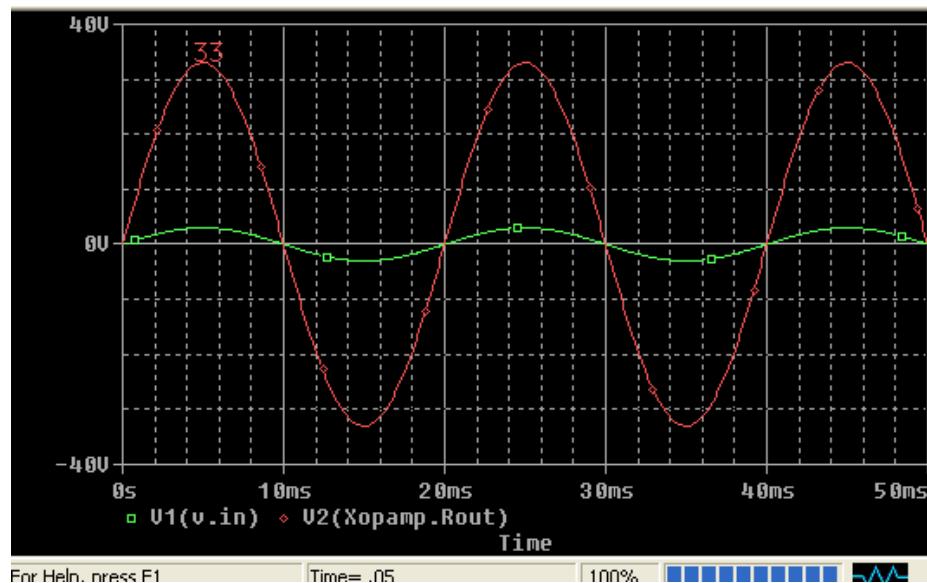


Fig 2.7 Simulation result of non-inverting opamp when $A_0 = 100000$

As we can see from the analysis above, the finite open loop gain of the operational amplifier has an effect on the closed loop gain of inverting and non-inverting amplifiers. There is an increase in percentage error when the open loop gain of the operational amplifier decreases.

Therefore, in practical applications, operational amplifier with required open loop gain must be selected while designing the amplifier, keeping in mind the permitted value of percentage error. For example, in both inverting and non-inverting amplifiers, an open loop gain of 10^4 leads to 0.1% error in the value of closed loop gain. This is more than adequate for most of applications.

2.3 Effect of finite loop gain on Input Resistance R_{in}

Case (i) Inverting Amplifier

The equivalent circuit of the inverting amplifier is shown in Fig 2.8

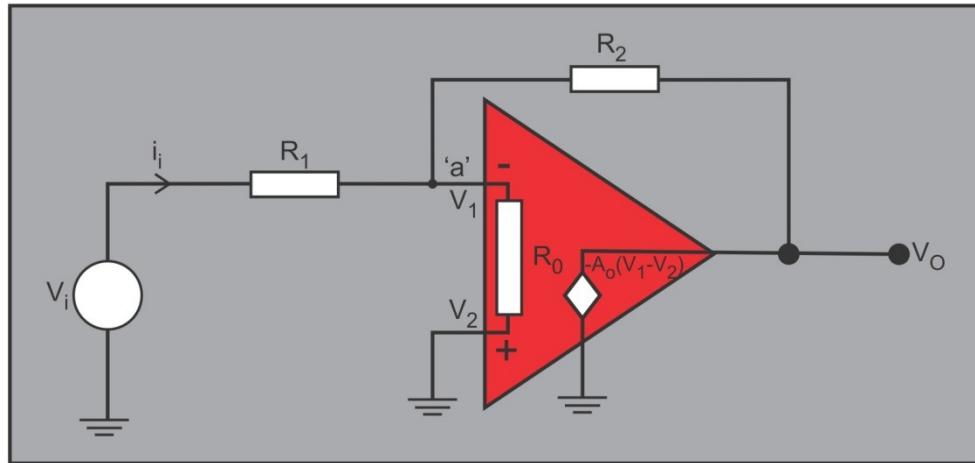


Fig 2.8 Analysis of Inverting Amplifier for Input Resistance

Consider the node 'a', based on KCL we can write the nodal equation as given below

$$\begin{aligned}
i_i &= \frac{v_1}{R_{di}} + \frac{v_1 - v_0}{R_2} \\
&= \frac{v_1}{R_{di}} + \frac{v_1}{R_2} + \frac{A_0 v_1}{R_2} \\
i_i &= v_1 \left[\frac{1}{R_{di}} + \frac{1 + A_0}{R_2} \right]
\end{aligned} \tag{2.5}$$

Considering the input circuit, We know that input resistance,

$$R_{in} = \frac{v_i}{i_i} = \frac{i_i R_1 + v_1}{i_i} = R_1 + \frac{v_1}{i_i}$$

Substituting the expression for i_i in Eq 2.5, we get

$$\begin{aligned}
R_{in} &= R_1 + \frac{1}{\frac{1}{R_{di}} + \frac{1 + A_0}{R_2}} \\
R_{in} &= R_1 + \frac{R_{di} R_2}{R_2 + R_{di}(1 + A_0)}
\end{aligned}$$

If A_0 is very large, $R_{in} \rightarrow R_1$

Case (ii) Non-inverting Amplifier

The equivalent circuit of a non-inverting amplifier is shown in Fig 2.9.

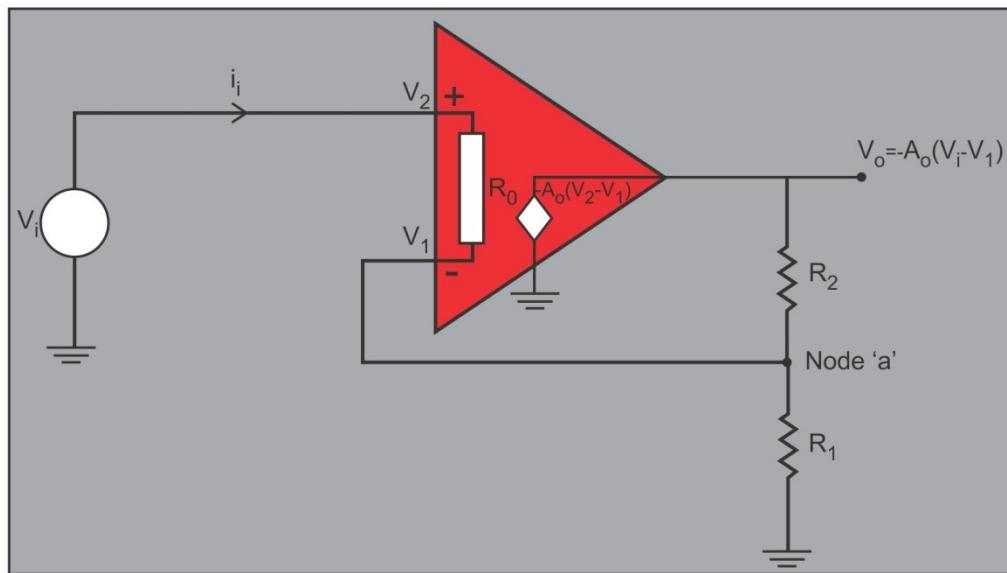


Fig. 2.9 Non-inverting amplifier with a differential resistance of R_{di}

Consider node 'a', based on KCL we can write the nodal equation as given below

$$\frac{v_1}{R_1} + \frac{v_1 - v_i}{R_{di}} + \frac{v_1 - v_0}{R_2} = 0$$

Since $v_0 = A_0(v_i - v_1)$

$$\begin{aligned} \frac{v_1}{R_1} + \frac{v_1 - v_i}{R_{di}} + \frac{v_1 - A_0(v_i - v_1)}{R_2} &= 0 \\ v_1 \left(\frac{1}{R_1} + \frac{1}{R_{di}} + \frac{1 + A_0}{R_2} \right) &= v_1 \left(\frac{1}{R_{di}} + \frac{A_0}{R_2} \right) \end{aligned} \quad (2.7)$$

$$\text{Input current } i_i = \frac{v_i - v_1}{R_{di}} = v_i \left(\frac{1 - \frac{v_1}{v_i}}{R_{di}} \right)$$

$$\text{Input Resistance } R_{in} = \frac{v_i}{i_i} = \frac{R_{di}}{1 - \frac{v_1}{v_i}}$$

Substituting equation 2.7 we get

$$R_{in} = \frac{R_{di}}{1 - \frac{\frac{1}{R_{di}} + \frac{A_0}{R_2}}{\left(\frac{1}{R_1} + \frac{1}{R_{di}} + \frac{1 + A_0}{R_2} \right)}}$$

$$\begin{aligned}
&= \frac{R_{di} \left(\frac{1}{R_1} + \frac{1}{R_{di}} + \frac{1}{R_2} + \frac{A_0}{R_2} \right)}{\frac{1}{R_1} + \frac{1}{R_2}} \\
&= \frac{R_{di} \left(\frac{R_1 R_2}{R_1 + R_2} + \frac{1}{R_{di}} + \frac{A_0}{R_2} \right)}{\frac{R_1 + R_2}{R_1 R_2}} \\
&= R_{di} \left(\frac{R_1 + R_2}{R_1 R_2} + \frac{1}{R_{di}} + \frac{A_0}{R_2} \right) \frac{R_1 R_2}{R_1 + R_2} \\
&= R_{di} \left(1 + \frac{R_1 R_2}{R_{di} (R_1 + R_2)} + \frac{A_0 R_1}{R_1 + R_2} \right)
\end{aligned}$$

Since,

$$\frac{R_1 R_2}{R_{di} (R_1 + R_2)} \ll 1$$

$$R_{in} = R_{di} \left(1 + \frac{A_0 R_1}{R_1 + R_2} \right) \quad (2.8)$$

The result of the analysis clearly indicates that there is not much change in input resistance. In fact, an increase in the value of input resistance leads to an improved performance of the operational amplifier with feedback.

2.4 Effect of finite gain on output resistance R_{out}

Case (i) Inverting Amplifier

The equivalent circuit of an inverting amplifier is shown in Fig 2.10 with $R_0 \Omega$ as the output resistance of the operational amplifier. The output resistance can be determined by applying a test voltage of v_t at the output and estimating the current i_t by short circuiting the independent voltage sources. The output resistance is given by

$$R_{out} = \frac{v_t}{i_t} \Omega$$

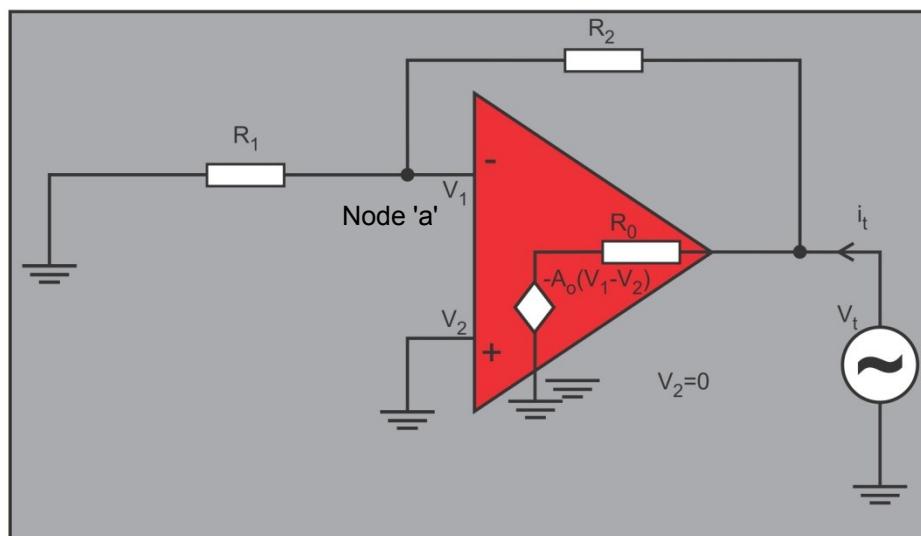


Fig. 2.10 Inverting Amplifier with a non-zero output resistance operational amplifier

Consider the node 'a' shown in Fig 2.10, based on KCL we can write the nodal equation as given below

$$\begin{aligned} i_t &= \frac{v_t - v_1}{R_2} + \frac{v_t + A_0(v_1 - v_2)}{R_0} \\ i_t &= v_t \left(\frac{1}{R_2} + \frac{1}{R_0} \right) - v_1 \left(\frac{1}{R_2} - \frac{A_0}{R_0} \right) \end{aligned} \quad (2.9)$$

We know that $v_1 = \frac{v_t R_1}{R_1 + R_2}$

Substituting in Eq 2.9, we get

$$\begin{aligned} i_t &= v_t \left(\frac{1}{R_0} + \frac{1}{R_2} \right) + \frac{v_t R_1}{R_1 + R_2} \left(\frac{A_0}{R_0} - \frac{1}{R_2} \right) \\ \therefore R_{out} &= \frac{v_t}{i_t} = \frac{1}{\left(\frac{1}{R_0} + \frac{1}{R_2} + \frac{A_0 R_1}{(R_1 + R_2) R_0} - \frac{R_1}{(R_1 + R_2) R_2} \right)} \end{aligned}$$

Multiply numerator and denominator by R_0 ,

$$R_{out} = \frac{R_0}{\left(1 + \frac{R_0}{R_2} + \frac{A_0 R_1}{(R_1 + R_2) R_0} - \frac{R_1 R_0}{(R_1 + R_2) R_2} \right)}$$

Since $\frac{R_0}{R_2} \ll 1$ and $\frac{R_1 R_0}{(R_1 + R_2) R_2} \ll 1$

$$R_{out} = \frac{R_0}{\left(1 + A_0 \left(\frac{R_1}{(R_1 + R_2)} \right) \right)}$$

Example 2.3: If $R_1 = 10 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $R_0 = 75\Omega$, $A_0 = 10^3$, find R_{out} in ohms.

Output resistance R_{out} is given by the equation 2.10

$$R_{out} = \frac{R_0}{\left(1 + A_0 \left(\frac{R_1}{(R_1 + R_2)} \right) \right)}$$

$R_0 = 75\Omega$, $A_0 = 10^3$, $R_1 = 10 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$

$$R_{out} = \frac{75}{\left(1 + 10^3 \left(\frac{10}{110} \right) \right)} = \frac{75}{90.9} = 0.825 \Omega$$

Output resistance = 0.825Ω

Case (ii) Non-inverting Amplifier

The equivalent circuit of a non-inverting amplifier is shown in Fig 2.11 with R_0 as the output resistance of the operational amplifier. The output resistance can be estimated as in the case of an inverting amplifier.

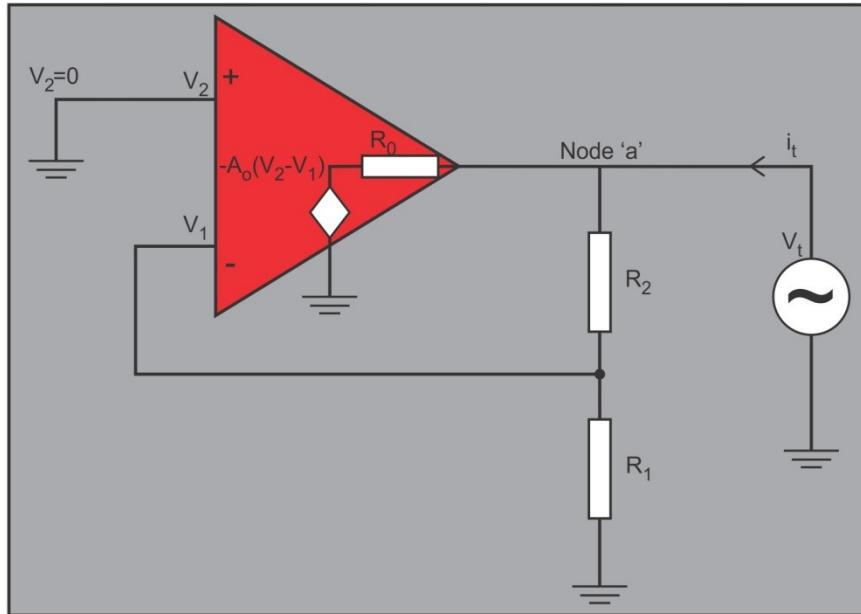


Fig. 2.11 Non-inverting amplifier with R_o as the output resistance of the op amp

Consider the node 'a' shown in Fig 2.6. Based on KCL we can write the nodal equation as

$$\begin{aligned} i_t &= \frac{v_t}{R_1 + R_2} + \frac{v_t - A_0(v_2 - v_1)}{R_0} \\ &= \frac{v_t - v_1}{R_2} + \frac{v_t}{R_0} + \frac{A_0 v_1}{R_0} \\ &= v_t \left(\frac{1}{R_2} + \frac{1}{R_0} \right) - v_1 \left(\frac{1}{R_2} - \frac{A_0}{R_0} \right) \end{aligned}$$

We know that $v_1 = \frac{v_t R_1}{R_1 + R_2}$

$$\begin{aligned} i_t &= v_t \left(\frac{1}{R_2} + \frac{1}{R_0} \right) - \frac{R_1}{(R_1 + R_2)R_2} + \left(\frac{A_0 R_1}{R_0 (R_1 + R_2)} \right) \\ &= \frac{v_t}{R_0} \left(\frac{R_0}{R_2} + 1 \right) - \frac{R_1 R_0}{(R_1 + R_2)R_2} + \frac{A_0 R_1}{R_1 + R_2} \end{aligned}$$

Since $\frac{R_0}{R_2} \ll 1$, $\frac{R_1 R_0}{(R_1 + R_2)R_2} \ll 1$

$$i_t \cong \frac{v_t}{R_0} \left[1 + \frac{A_0 R_1}{R_1 + R_2} \right]$$

∴ Output Resistance

$$R_{out} = \frac{v_t}{i_t} = \frac{R_0}{1 + \frac{A_0 R_1}{R_1 + R_2}} \quad (2.11)$$

This is same as that of an inverting amplifier.

The effect of finite open loop gain of the operational amplifier on the output resistance of inverting and non-inverting amplifiers clearly indicates that the output resistance decreases to a very low value. The typical value of output resistance of an operational amplifier is 75Ω . For an open loop gain of 1000, output resistance reduces to less than 1Ω . In most of the applications it enhances the overall performance of the operational amplifier.

2.5 Voltage follower or Buffer Amplifier

The input resistance of the non-inverting operational amplifier is given by equation 2.12

$$R_{in} = R_{di} + \frac{A_0 R_{di} R_1}{R_1 + R_2} \quad (2.12)$$

For setting very high input resistance it becomes essential to choose a very large value for R_1 and very low value for R_2 . If $R_1 \rightarrow \infty$ and $R_2 = 0$

$$R_{in(max)} = R_{di} + A_0 R_{di} = R_{di}(1 + A_0)$$

Let us find the output resistance for these values of R_1 and R_2 using Equation....

$$\begin{aligned} R_{out} &= R_0 \left(\frac{1}{1 + A \left(\frac{R_1}{R_1 + R_2} \right)} \right) \\ &= R_0 \left(\frac{1}{\infty} \right) = 0 \end{aligned}$$

The gain of non-inverting amplifier is given in equation

For $R_1 \rightarrow \infty$ and $R_2 = 0$

$$\begin{aligned} \text{Gain } A &= \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1}{A_0} \left(1 + \frac{R_2}{R_1} \right)} \\ &\approx \frac{A_0}{1 + A_0} \approx 1 \end{aligned}$$

The voltage gain of the amplifier is unity. The output voltage follows the input voltage, hence it is called as voltage follower or Buffer Amplifier and the circuit is shown in Fig 2.11

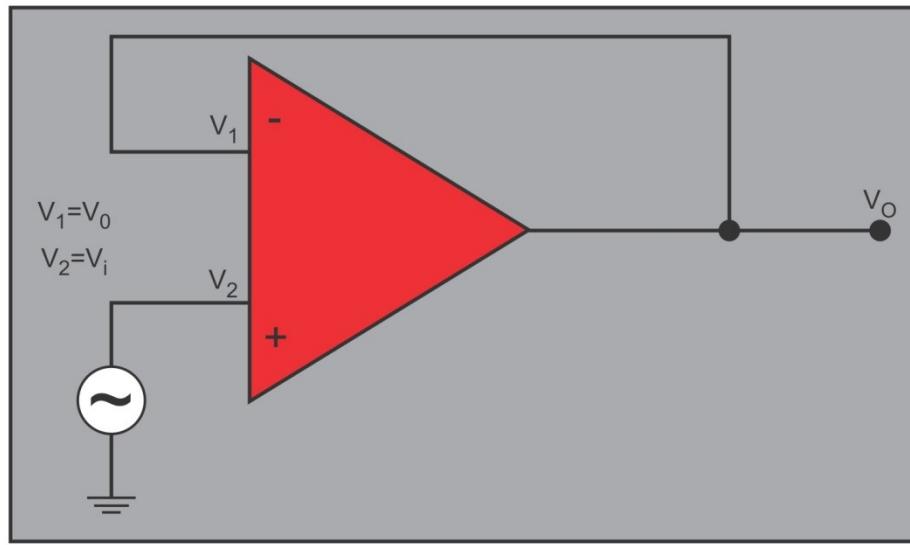


Fig 2.12 Voltage Follower

The important benefit of voltage follower is the elimination of loading effect on the signal source. Similarly, the output resistance of the op-amp is very small, the loading is also eliminated at the output of the device. Therefore it is called as resistance transformer.

In order to understanding the loading effect let us consider the following problem.

A source with an internal resistance, R_S is connected at the input and a load resistance R_L is connected to the output as shown in Fig 2.13

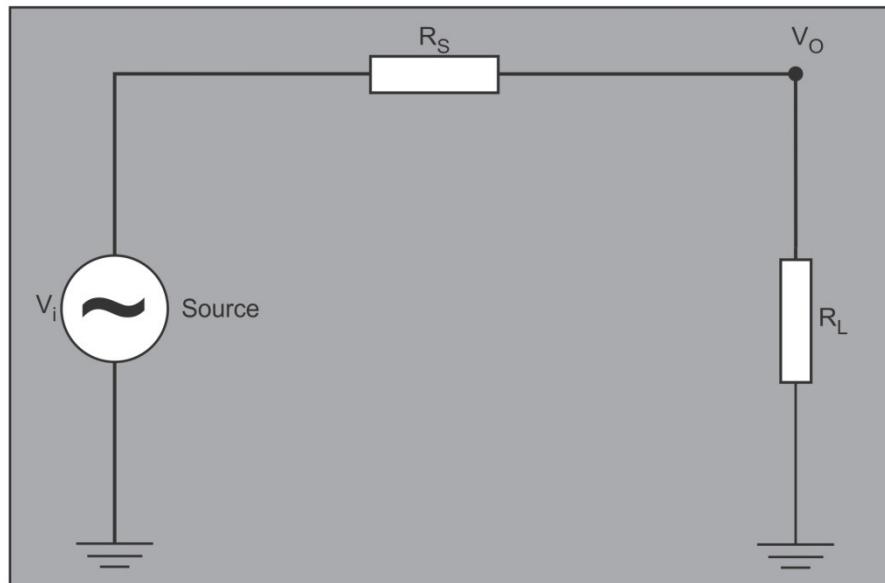


Fig.2.13 (a) Direct Connection of source and load

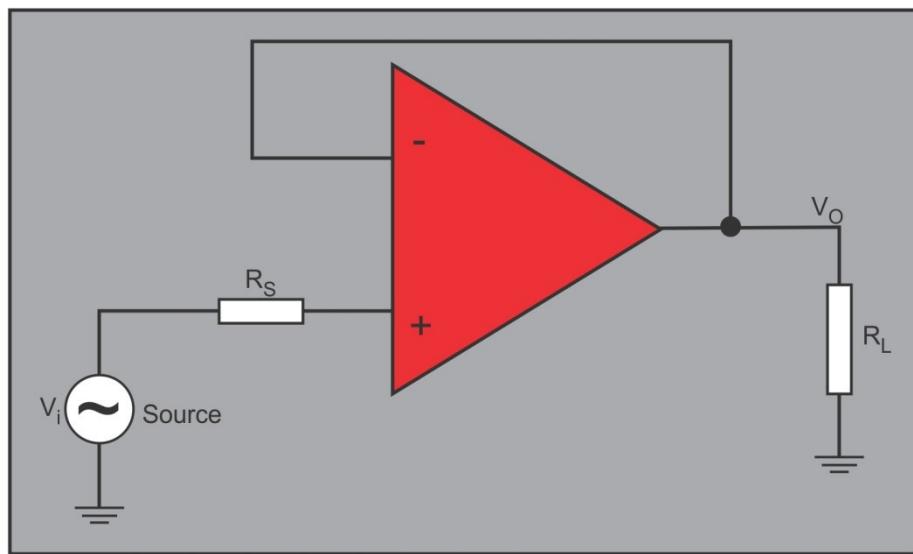


Fig.2.13 (b) Connection via a voltage follower

For direct connection to the output voltage v_o can be calculated as

$$v_o = \frac{v_i}{R_s + R_L} \times R_L$$

If $R_s = 5 \text{ k}\Omega$, $R_L = 5 \text{ k}\Omega$

$$v_o = v_i \frac{5 \cdot 10^3}{10 \cdot 10^3} = 0.5v_i$$

The output is only 50% of the input voltage which is very low when compared to input voltage.

If a voltage follower is inserted in between source and load, the output voltage is

$$v_o = \frac{A_0}{1 + A_0} v_2$$

The input current may be assumed a zero since the input impedance is very large, therefore $v_2 = v_i$

$$v_o = \frac{10^3}{1 + 10^3} v_i = 0.999v_i$$

Output voltage is more or less equal to input voltage. The load now sees the input source but it places no demand on the signal source. Therefore the source is isolated from the load.

2.6 Input offset and Input Bias current

The currents flowing into the input terminals of the ideal operational amplifier are always equal to zero. But for real operational amplifiers, there is always a small amount of current flowing into the inverting and non-inverting terminals as shown in Fig. 2.14.

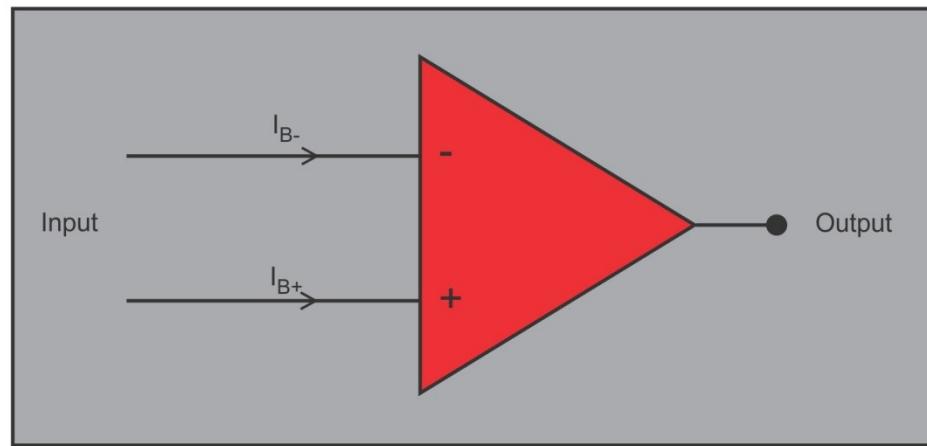


Fig. 2.14 Offset and Bias current

Let I_{B-} be the input current into non inverting terminal and I_{B+} be the input current into inverting terminal.

Input offset current is defined as $I_{IO} = |I_{B+} + I_{B-}|$

Input bias current is defined as $I_{IB} = \frac{|I_{B+} + I_{B-}|}{2}$

The values for input offset current and Input bias current can be found from data sheets of operational amplifiers.

For 741, operational amplifier the offset and bias currents are given below:

Input offset current $I_{IO} = 20 \text{ nA}$

Input bias current $I_{IB} = 80 \text{ nA}$

Let us study the offset of the current on the output voltage of an inverting amplifier as shown in Fig 2.15

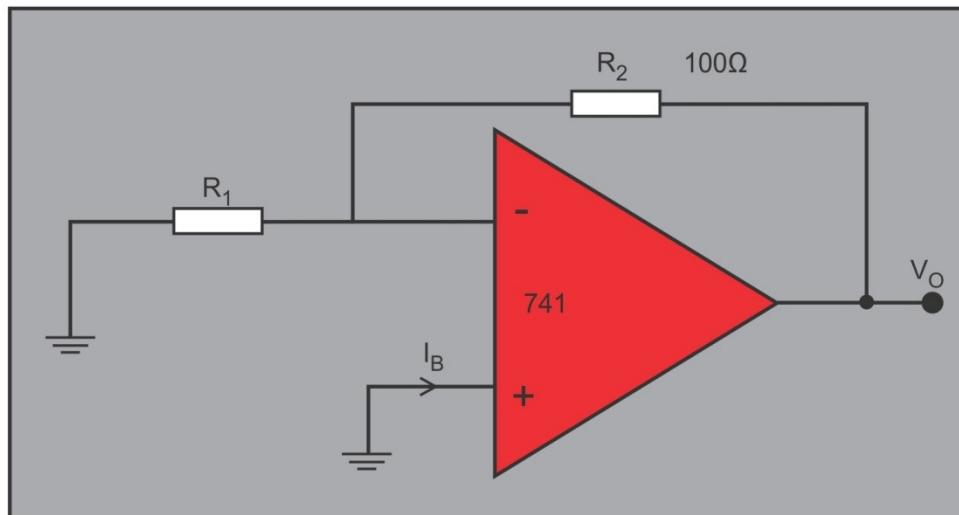


Fig.2.15. Output Error estimation

Assuming that input voltage is zero, let us calculate the output voltage due to Input offset current and Input bias current. For 741 operational amplifier $I_{IO} = 20 \text{ nA}$ and $I_{IB} = 80 \text{ nA}$

We know $I_{IO} = I_{B+} - I_{B-}$

$$I_{IB} = \frac{I_{B+} + I_{B-}}{2}$$

We can show that,

$$2I_{IB-} = 2I_{IB+} - I_{IO}$$

$$= (160) \text{ nA} = 140 \text{ nA}$$

$$I_{B-} = 70 \text{ nA}$$

$$\text{Output voltage } V_0 = I_{B-} \times R_2$$

$$= 70 \times 10^{-9} \times 100 \times 10^3$$

$$= 7 \times 10^{-3} \text{ V} = 7 \text{ mV}$$

$$\text{Error in output voltage} = 7 \text{ mV}$$

Since the error voltage is proportional to value of R_2 , one can reduce the error voltage at the output by reducing the resistance R_2 without violating the maximum output current or power consumption.

Another method of reducing the error voltage is introducing a compensating resistance R_c at the non-inverting input terminal as shown in Fig 2.16.

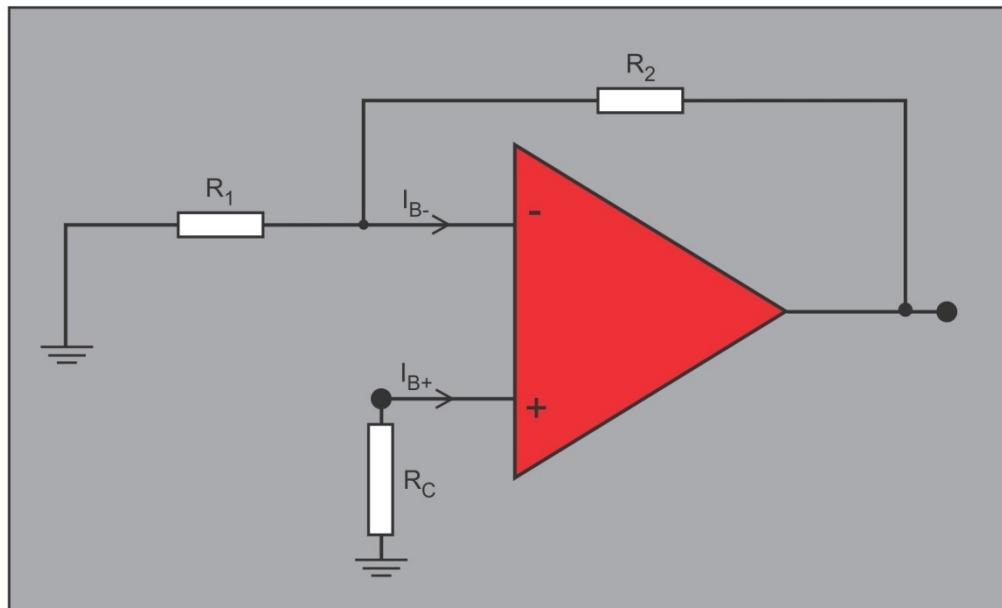


Fig 2.16 Inverting Amplifier circuit with compensating resistor R_c

By applying the superposition theorem for estimating the output voltage due to I_{B-} and I_{B+} we get

$$V_0 = I_{B-}R_2 - I_{B+}R_c \left(1 + \frac{R_2}{R_1}\right) \quad (2.13)$$

From the definition for offset current and bias current

$$I_{IO} = I_{B+} - I_{B-}$$

$$I_{IB} = \frac{I_{B+} + I_{B-}}{2}$$

$$2I_{IB} = I_{B+} + I_{B-}$$

$$I_{IO} = I_{B+} - I_{B-}$$

According to two equations we get,

$$2I_{IB} + I_{IO} = 2I_{B+}$$

$$\therefore I_{B+} = \frac{2I_{IB} + I_{IO}}{2} \quad (2.14)$$

Similarly by subtracting we can get

$$2I_{IB} - I_{IO} = 2I_{B-}$$

$$\therefore I_{B-} = \frac{2I_{IB} - I_{IO}}{2} \quad (2.15)$$

Substituting Eq 2.14 and Eq 2.15 in Eq 2.13

$$\begin{aligned} V_o &= \left(\frac{2I_{IB} - I_{IO}}{2} \right) R_2 - \left(\frac{2I_{IB} + I_{IO}}{2} \right) \left(1 + \frac{R_2}{R_1} \right) R_C \\ &= I_{IB} R_2 - \frac{I_{IO}}{2} R_2 - \left[\left(1 + \frac{R_2}{R_1} \right) R_C \left(I_{IB} + \frac{I_{IO}}{2} \right) \right] \\ &= I_{IB} \left[R_2 - R_C \left(1 + \frac{R_2}{R_1} \right) \right] - \frac{I_{IO}}{2} \left[R_2 + R_C \left(1 + \frac{R_2}{R_1} \right) \right] \end{aligned}$$

$$\begin{aligned} &= \left(1 + \frac{R_2}{R_1} \right) \left[\left(\frac{R_1 R_2}{R_1 + R_2} - R_C \right) I_{IB} - \left(\frac{R_1 R_2}{R_1 + R_2} + R_C \right) \frac{I_{IO}}{2} \right] \\ &\quad \underbrace{\qquad\qquad}_{\text{Bias term}} \qquad \underbrace{\qquad\qquad}_{\text{Offset Term}} \end{aligned}$$

For $I_{B+} = I_{B-}$, $I_{IO} = 0$

$$V_{\text{out}} = \left(1 + \frac{R_2}{R_1} \right) \left[\frac{R_1 R_2}{R_1 + R_2} - R_C \right] I_{IB}$$

$$\text{If } R_C = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{\text{out}} = 0$$

$$\text{For } I_{B+} \neq I_{B-}, R_C = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{\text{out}} = u \left(1 + \frac{R_2}{R_1} \right) \left[\frac{R_1 R_2}{R_1 + R_2} + R_C \right] \frac{I_{IO}}{2}$$

$$= - \left(\frac{R_1 + R_2}{R_1} \right) \left(\frac{R_1 R_2}{R_1 + R_2} \right) 2 \times \frac{I_{IO}}{2}$$

$$V_{out} = t I_{IO} R_2$$

The output error is proportional to the input offset current, which is less than the currents I_{B+} and I_{B-} .

2.7 Input Offset Voltage

The apparent voltage difference between the inputs even when the inputs are shorted is called as Input offset voltage. In practice, a small differential voltage is needed at the input to make the output voltage zero. This differential input voltage is the input offset voltage and is denoted as V_{os} . It is modeled as a voltage source, V_{os} in series with the inverting input terminal as shown in Fig 2.17.

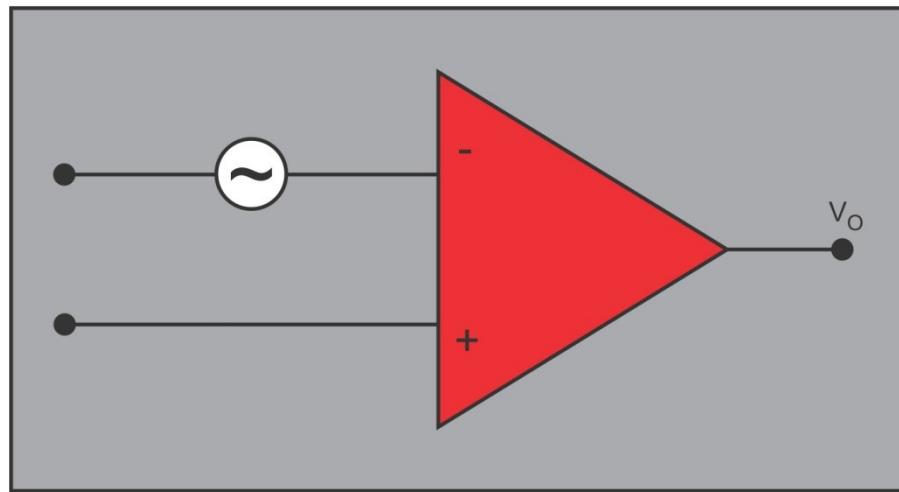


Fig 2.17 Input offset voltage model

The corresponding output offset voltage is obtained by multiplying the input offset voltage by the open loop gain, A_0 . For the LM 741A, the average input offset is 0.8mV with a maximum value of 3mV. If the circuit gain is 100, then the output is typically off by 80mV. Increase in temperature increases the input offset voltage. The typical values of Input offset voltage for different operational amplifiers are given in Table 2.2.

Table 2.2 Typical Op-Amp Input offset voltage

S. No	Type of Op- Amp	Input offset voltage	TI Op-Amp
1	Best bipolar Op-Amp	10-100 μ V	OPA177,TLE2021
2	General Purpose Precision Op-Amp	50-500 μ V	OPA827,LMP7721 OPA241,TLC2654
3	Best JFET Input Op-Amp	0.1mV-3mV	TL072,LF411 LF412,TL082
4	Untrimmed CMOS Op-Amp	0.5mV-50mV	LM613,LM725
5	Chopper stabilized Op-Amp	<1 μ V	LTC1052,TLC2652

Input offset voltage varies with temperature and its temperature coefficient is normally expressed in μ V/ $^{\circ}$ C. Typical value for temperature coefficient of general purpose precision operational amplifier

varies from $1\mu\text{V}/^\circ\text{C}$ to $10\mu\text{V}/^\circ\text{C}$. the offset voltage also changes as time passes or ages. Aging is generally specifies in $\mu\text{V}/\text{months}$ or $\mu\text{V}/1000$ hours.

The offset voltage adjustment can be done by using the pins available for optional offset null. To make use of this feature two pins are joined by a potentiometer and the wiper is connected to one of the supply through a resistance 'R₁' as show in Fig 2.18. This method for the Operational Amplifiers such as OPA 227, LM 725, TLC 070 and TLC 4011.

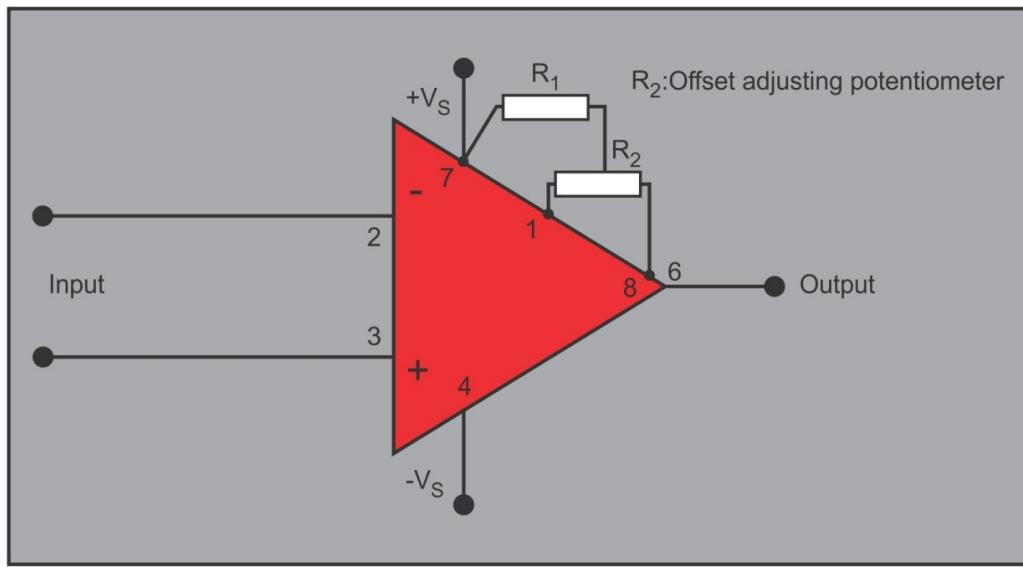


Fig 2.18 Offset Adjustment Pins

Another method (External method) of adjusting the offset voltage is by injecting a current into the inverting input of the operational amplifier as shown in Fig.2.19. A potentiometer is connected between the DC supply and the inverting input of the operational amplifier through a resistance 'R₃'. To avoid the effect of R₃ on the gain, we have to choose R₃ as large as possible when compared to R₁ and R₂. This method is applicable to all Operational Amplifiers.

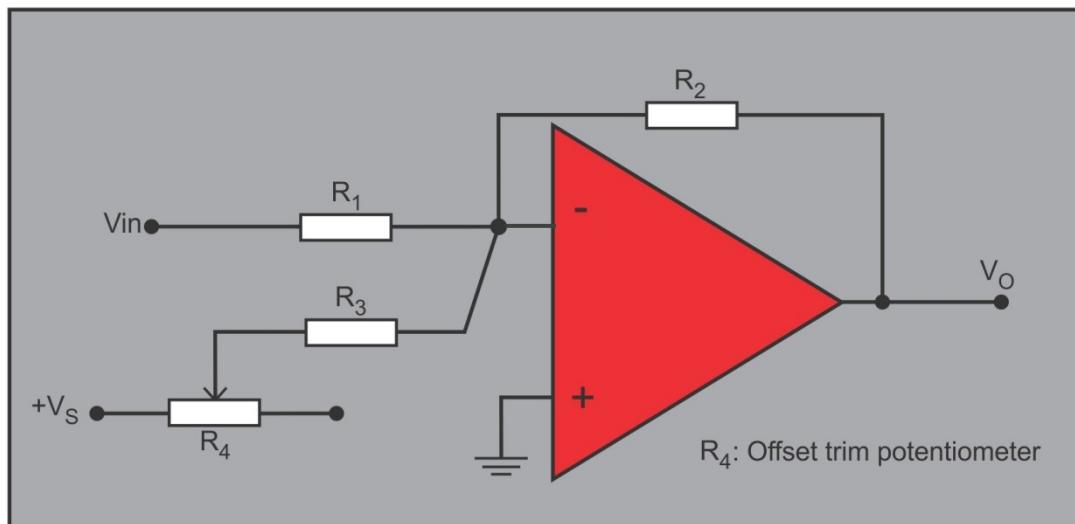


Fig 2.19 Inverting Op Amp External offset Trim method

The same method can be adopted by non-inverting operational amplifiers by injecting a current into the inverting input terminal. Hera also 'R₃' must be made much greater than R₁, otherwise the signal gain might be affected as the offset potentiometer is adjusted.

2.8 Thermal Drift

Normally, it is assumed that the input offset voltage V_{OS}, input offset current and input bias current I_B are constant for a given operational amplifier. In practice the following operating conditions affects these parameters loading to performance deterioration of operational amplifier applications.

- i. Change in temperature
- ii. Change in DC supply voltage

The change in temperature cause more variation in offset voltage and offset current leading to serious variation of the performance of the operational amplifier. The internal circuit of the operational amplifier is more sensitive to the variation in DC supply voltage. Hence the DC power supply used for operational amplifier circuit must have good regulation and low noise. The changes in DC power supply voltage will also change the offset voltage and offset current as in the case of variation in temperature.

The thermal drift in input offset current is defined as the average rate of change of input offset current denoted by $\frac{\Delta I_{OS}}{\Delta T} \text{ pA}/\text{°C}$. The thermal drift in input offset voltage is defined as the average rate of change of input offset voltage per unit change in temperature denoted by $\frac{\Delta V_{OS}}{\Delta T} \mu\text{V}/\text{°C}$.

The thermal drift in the input bias current is defined as the average rate of change of input bias current per unit change in temperature denoted by $\frac{\Delta I_B}{\Delta T} \text{ pA}/\text{°C}$. The operational amplifier manufacturers specify either an average or maximum drift for two temperature limits and a plot of variation of drift with respect to temperature. Typical values for 741 and TL082 are given below in table 2.3.

Table 2.3 Thermal drift parameters

S.No.	Parameters	741	TL082
1.	Input offset voltage(V _{OS}) TA=25°C	Typical: 1 mV Max: 5 mV $\pm 15 \mu\text{V}/\text{°C}$	Typical: 5 mV Max: 15 mV $\pm 10 \mu\text{V}/\text{°C}$
2.	Input offset Current (I _{OS}) TA=25°C	Typical: 3 nA Max: 30 nA $\pm 0.5 \text{nA}/\text{°C}$	Typical: 25 pA Max: 200 pA
3.	Input bias Current (I _B) TA=25°C	Typical: 30 nA Max: 80 nA	Typical: 50 pA Max: 400 pA

Example 2.4: The drift parameter of an operational amplifier used in a non-inverting amplifier is given below.

Input offset current variation= $\pm 15 \mu\text{V}/\text{°C}$

Input offset current variation= $\pm 0.5 \text{nA}/\text{°C}$

Assuming R_f = 1MΩ and R_i = 100KΩ and output V_o=0 at 25°C, find the output voltage at 60°C due to offset voltage variation and due to offset current variation .

- i. output voltage at 60°C due to offset voltage variation

$$V_{OS} = \pm 15 \times 10^{-6} \times (60 - 25) = \pm 5253 \mu\text{V}$$

$$\begin{aligned}
 \text{Output} &= \pm V_{OS} \left(1 + \frac{R_f}{R_i} \right) = \pm 525 \times 10^{-6} \times \left(1 + \frac{10^6}{100 \times 10^3} \right) \\
 &= \pm 525 \times 11 \times 10^{-6} \\
 &= \pm 0.526 V \\
 &= \pm 5.775 mV
 \end{aligned}$$

ii. output voltage at 60°C due to offset current variation

$$\begin{aligned}
 \Delta I_{OS} &= \pm 15 \times 10^{-9} \times (60 - 25) = \pm 17.5 \times 10^{-9} A \\
 \text{output voltage} &= \pm 17.5 \times 10^{-9} \times R_f \\
 &= \pm 17.5 \times 10^{-9} \times 1 \times 10^6 \\
 &= \pm 0.0175 V \\
 &= \pm 17.5 mV
 \end{aligned}$$

The change in output voltage due to the change in offset voltage and offset current

$$\begin{aligned}
 &= \pm (5.775 + 17.5) mV \\
 &= \pm 23.275 mV
 \end{aligned}$$

2.9 Common Mode Rejection ratio (CMRR)

Operational amplifiers are widely used in measuring instruments and controllers as a difference or differential amplifier at the input. The input to a difference amplifier, in general contains two components: a common mode and a difference mode signal. The purpose of the circuit is to amplify the difference between the input voltages and must have the capability to ignore the inputs when they are equal.

This function is vital as all electronic circuits are exposed to interference. Often such interference will result in a common mode signal at the input. One such example is the instrumentation amplifier used for amplifying bio-electric signals of bio-electric potential recorders such as Electrocardiograph (ECG), Electroencephalograph (EEG), Electromyograph (EMG) and Electroretinograph (ERG). An ideal difference amplifier will reject all such interference and amplify only the difference between the inputs. Ideally a difference amplifier affects the difference mode signals only. However the common mode signal is also amplified to some degree in practical amplifiers.

The operational amplifier is intended for amplifying differential input voltage. Ideally, the common mode voltage applied to inverting and non-inverting terminals should not affect the output voltage. But practical operational amplifiers respond to signal common to both inputs, called the common mode input voltage (V_{ic}).

To calculate the common mode voltage gain A_{CM} , a strategy similar to that used for input offset voltage can be adopted. Let the input voltage applied to the inverting and non – inverting terminals tied together be V_{CM} as shown in Fig.2.20.

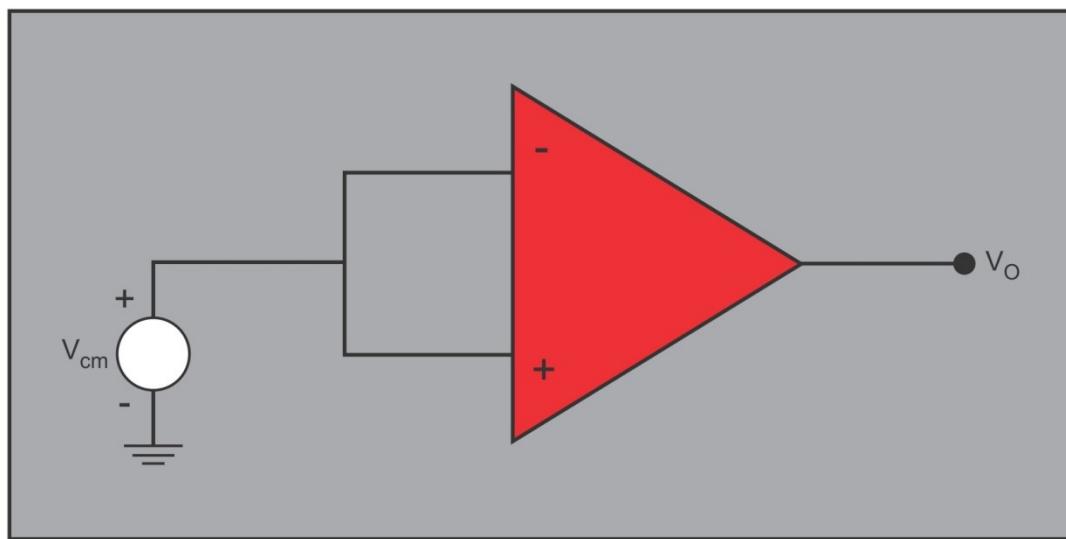


Fig 2.20 Operational Amplifier with Common mode voltage

For an ideal device the output would be zero and for a practical device, some output voltage V_o appears at the output.

$$\text{Therefore common mode gain } A_{CM} = \frac{V_0}{V_{CM}}$$

. For operational amplifiers the Common Mode Rejection Ratio (CMRR) is defined as the ratio of the differential voltage gain A_0 to the common mode voltage gain A_{CM} .

$$CMRR = \frac{A_0}{A_{CM}} \text{ or } CMRR \text{ in } dB = 20 \log \frac{|A_0|}{|A_{CM}|}$$

The CMRR values for ideal operational amplifier would be infinity. The typical values for practical amplifiers vary from 80 to 100dB.

The error in the output voltage introduced by A_{CM} and CMRR can be estimated using the operational amplifier circuit with input voltages v_1 and v_2 as shown in Fig. 2.21

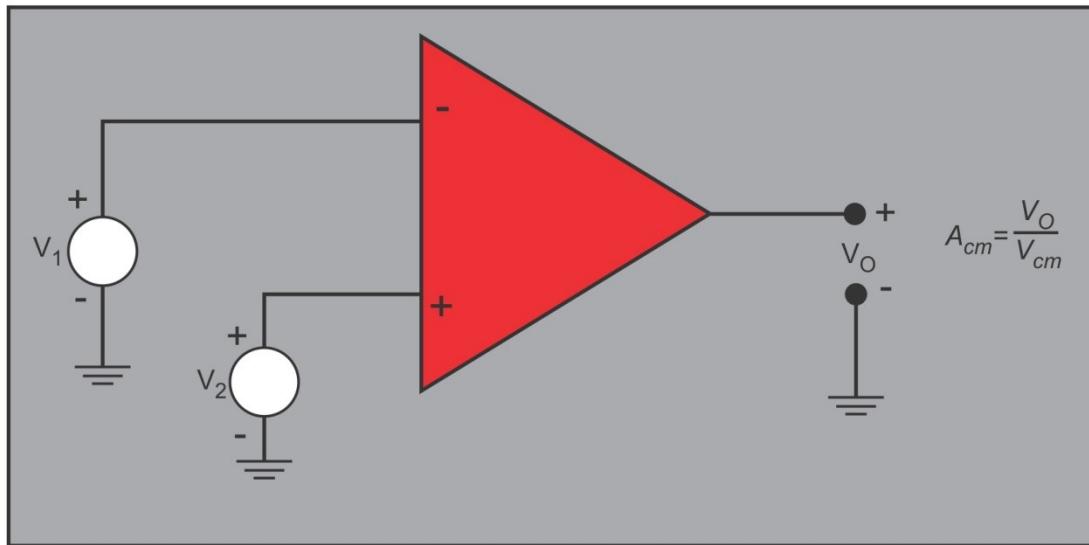


Fig 2.21 Op Amp circuit with separate input voltages

Let v_1 be the voltage applied to the inverting input terminal and v_2 be the voltage applied to non-inverting input terminal. Expression for output voltage can be written as

$$v_0 = A_0(v_2 - v_1) + A_{CM} \left(\frac{v_1 + v_2}{2} \right) \quad (2.16)$$

$$v_0 = A_0(v_{id}) + A_{CM}(v_{ic})$$

Where v_{id} is the differential input voltage and v_{ic} is the common mode input voltage.

$$v_2 - v_1 = v_{id}$$

$$v_2 + v_1 = 2v_{ic}$$

Adding two equations we get

$$2v_2 = v_{id} + 2v_{ic}$$

$$\therefore v_2 = \frac{v_{id}}{2} + v_{ic}$$

By subtracting one from the other, we can show that

$$v_1 = -\frac{v_{id}}{2} + v_{ic}$$

$$v_1 = v_{ic} - \frac{v_{id}}{2}$$

By substituting into the equation 2.14, we can get the output voltage

$$v_0 = A_0(v_{id}) + A_{CM} \left(\frac{2v_{ic}}{2} \right)$$

$$\begin{aligned}
 v_0 &= A_0 \left[v_{id} + \left(\frac{A_{CM} v_{ic}}{A_0} \right) \right] \\
 &= A_0 \left[v_{id} + \left(\frac{v_{ic}}{CMRR} \right) \right] \\
 \therefore Error voltage &= v_{ic} \times \frac{A_0}{CMRR}
 \end{aligned}$$

The error voltage is inversely proportional to CMRR. Larger value of CMRR would result in lesser error.

Example 2.5: Find the output voltage error introduced by CMRR = 80dB in an operational amplifier circuit with the following details.

Open loop gain $A_0 = 10^4$

Non inverting input $v_1 = 3.99$ V

Inverting input $v_2 = 4.00$ V

Solution:

Expression for output voltage as per equation 2.14,

$$v_0 = A_0 \left[v_{id} + \left(\frac{v_{ic}}{CMRR} \right) \right]$$

$$v_{id} = v_2 - v_1 = 4 - 3.99 = 0.01$$

$$v_{ic} = \frac{v_1 + v_2}{2} = \frac{4 + 3.99}{2} = \frac{7.99}{2} = 3.99$$

$$\text{CMRR in dB} = 80 = 20\log(\text{CMRR})$$

$$\log(\text{CMRR}) = 4$$

$$\text{CMRR} = 10^4$$

$$v_0 = 10^4 \left[0.01 + \left(\frac{3.99}{10^4} \right) \right] \text{ Volts}$$

$$= [10^4 \times 0.001 + 3.99] \text{ Volts}$$

$$= 100 + 3.99 = 103.99 \text{ Volts}$$

If $\text{CMRR} \rightarrow \infty$,

The output voltage = 100.

$$\begin{aligned}
 \text{Therefore Error voltage in \% value} &= \frac{(103.99 - 100)}{100} \times 100 \\
 &= 3.99 \%
 \end{aligned}$$

2.10 Slew rate and its effects

Slew rate is basically how fast an operational amplifier can change its output voltage. The slew rate limiting is directly responsible for the non-linear distortion of large output signals. The slew rate limitation is present in every practical operational amplifier. It indicates the inability of the operational amplifier output stage to follow the input signal. In extreme condition a step voltage applied at the input may appear as a ramp signal. The slope of the ramping signal is the slew rate. Therefore the slew rate is defined as the maximum possible rate change of the operational amplifier output voltage caused by a step voltage applied at the input. A general purpose operational amplifier may have a slew rate of 10Volts/ μ s. This means that when a large step voltage is applied at the input, the device would be able to provide an output change of 10 Volts in one microsecond.

The figures of slew rate depend upon the type of operational amplifier being used. Low power operational amplifiers may have figures of the order of $1V/\mu s$, whereas high speed operational amplifiers are capable of providing slew rate of $1000V/\mu s$. Operational amplifiers may have different slew rates for positive and negative going transitions because of the circuit configuration. However it is often assumed that they have reasonably symmetrical performance levels.

There are two major reasons for the slew rate limitation of most operational amplifiers. One reason is related to the limitations of output driver circuit, the low current levels limit the rate at which change can occur. The second reason is the external connection of compensating capacitance used for reducing the high frequency response. The slew rate introduces distortion in the output voltage. This can be seen even if the input signal is sinusoidal, the output may become triangular as shown in Fig 2.22

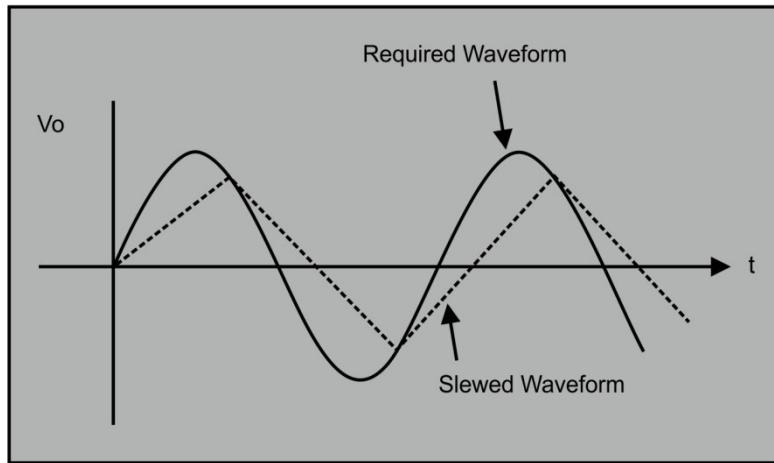


Fig 2.22 Slew rate distortion

The maximum rate of change of sine wave occurs at zero crossing circuit. A sine wave with a frequency of f Hz and peak voltage V volts requires an operational amplifier with a slew rate of ' $2\pi f V$ ' V/s. This is obtained from the maximum value of the first derivative of the sinusoidal signal.

2.11 Power Supply Rejection Ratio (PSRR)

The DC power supply voltage may vary due to variation in line voltage, change in load current and change in temperature. The permitted variation of DC power supply voltage is normally three to five percent of the normal supply voltage. These changes in power supply voltage, even though very small, will change the operational amplifier input and in turn output voltage. This can be considered as an additional offset voltage on the operational amplifiers input. The power supply rejection ratio (PSRR) mentioned in the data sheet may be used to find out the additional offset voltage.

The power supply rejection ratio (PSRR) is defined as the ratio of change in DC supply voltage of the operational amplifier to the equivalent output voltage it produces at the output, often expressed in decibels. The power supply rejection ratio (PSRR) of an ideal amplifier is infinite. Some manufacturers specify PSRR in terms of the offset voltage it causes at the amplifier inputs and others specify it in terms of the output. If PSRR is specified in terms of input offset voltage, the expression for PSRR is given by

$$\text{PSRR} = \frac{\Delta V_{CC}}{\Delta V_{OS}} \quad (2.17)$$

$$\text{PSRR in dB} = 20 \log_{10}(\text{PSRR})$$

Where ΔV_{CC} is the change in power supply voltage and ΔV_{OS} is the change in input offset voltage. The PSRR is usually specified in microvolt per volt ($\mu\text{V/V}$) or in decibels (dB). Typical specification for PSRR of an amplifier varies from 60 dB to 100 dB. It is not constant. The PSRR of 741 operational amplifier is 96 dB.

2.12 Frequency Response

The frequency response, bandwidth and gain bandwidth product of operational amplifiers are very important key parameters for any operational amplifier circuit. Typically Operational Amplifiers are used in low frequency circuits, but with the performance of these amplifiers improving all the time, much higher bandwidth Op Amps are now available in the market. The frequency response of the Op Amp circuit solely depends on the bandwidth of the Op Amp itself. The general purpose Op Amps are typically low-pass amplifiers with high gain at DC and a single pole frequency response for high frequencies as shown in Fig 2.23

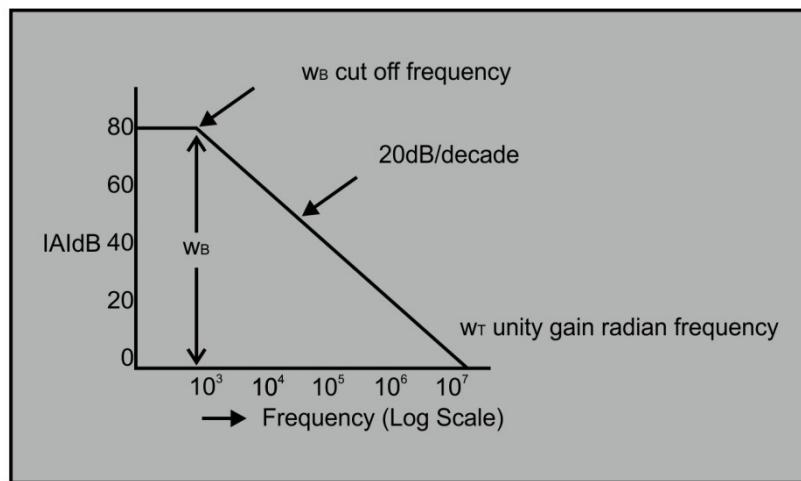


Fig: 2.23 Op Amp Frequency Response

The frequency response of the Op Amp will often start to fall at a very low frequency when operated in its open loop mode. The frequency at which the gain starts to roll off is known as the break point or -3 dB point. The stray capacitance in the chip may cause unwanted spurious high frequency oscillations. This problem can be solved by intentionally reducing the open loop gain at high frequencies.

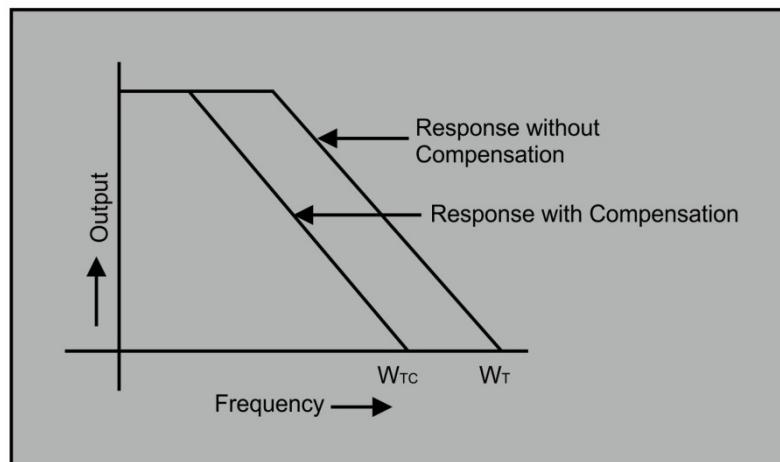


Fig: 2.24 Frequency Response with compensation

This is called compensation and it is normally implemented by bypassing one of the internal amplifier stages with a high pass filter. The aim is to reduce the gain to less than unity at frequencies where there could be a possibility of oscillation. The frequency response with and without compensation is given in Fig 2.24

Internal frequency compensation is the major reason for not using Op Amp circuit for high frequency applications. The frequency at which the Op Amp open loop gain falls to unity is called as unity gain frequency f_T . This frequency gives a good indication of the speed of operation of the Op Amp. Gain bandwidth product is equal to the voltage gain multiplied by the cut off frequency. It is a constant for voltage feedback amplifier. Bandwidth can be increased by applying feedback and reducing the open loop gain as shown in Fig 2.25.

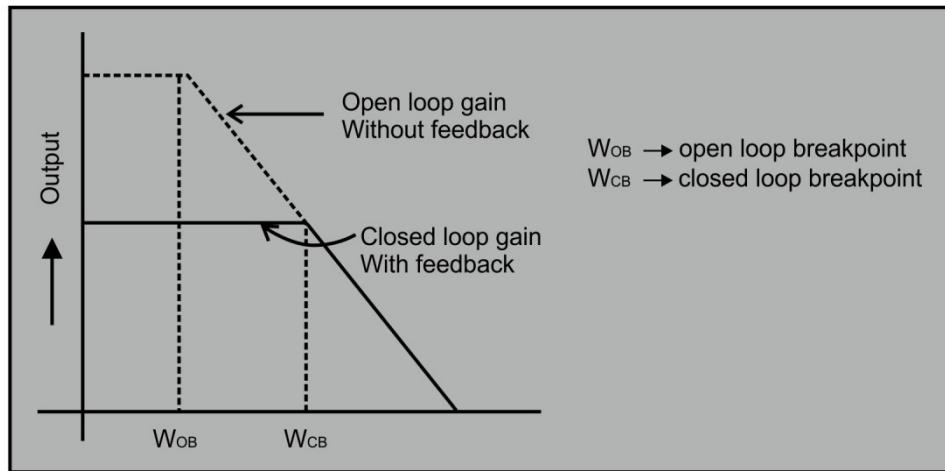


Fig: 2.25 Closed Loop op Amp Frequency response

The expression for Laplace Transform of single pole amplifier voltage gain is given by

$$Av(s) = \frac{Av(o)}{1 + s/w_B} = \frac{A_o w_B}{s + w_B} = \frac{w_T}{s + w_B}$$

Where w is the radian frequency, w_B is the dc open loop gain break point

w_T is unity gain radian frequency

The magnitude of the voltage gain is given by

$$|Av(j\omega)| = \frac{A_o w_B}{\sqrt{w^2 + w_B^2}} = \frac{A_o}{\sqrt{1 + w^2/w_B^2}}$$

For $w \gg w_B$,

$$|Av(j\omega)| = \frac{A_o w_B}{w} = \frac{w_T}{w}$$

For $w = w_T$,

$$|Av(j\omega)| = \frac{w_T}{w_T} = 1$$

For $w \gg w_B$, the product of magnitude of amplifier gain and frequency is a constant value equal to the unity gain frequency. Hence w_T is called as the gain bandwidth product. This is called a single pole amplifier with only one cut off frequency break point.

Example 2.6

Find the magnitude of cut off frequency and gain-bandwidth product in Hz for the Op. Amp with the following details

- i. Open loop gain for DC signal $A_o = 10^4$
- ii. The cut off radian frequency $w_B = 10^3$ rad/s

$$\text{The cut off frequency, } f_B = \frac{w_B}{2\pi} = \frac{10^3}{2\pi} = 159 \text{ Hz}$$

$$w_T = A_o w_B = 10^4 \times 10^3 = 10^7$$

$$f_T = \frac{w_T}{2\pi} = \frac{10^7}{2\pi} = 159 \times 10^4 \text{ Hz} = 1.59 \text{ MHz}$$

2.12.1 Frequency Response of Non Inverting Amplifier

Let us study the frequency response of a Non Inverting amplifier discussed earlier. The expression for the gain of a non-inverting amplifier as given in Eq 2.4 is

$$A_{ni} = \frac{1 + R_2/R_1}{1 + \frac{1}{A_o} (1 + R_2/R_1)} = \frac{A_v}{1 + \frac{A_v}{(1 + R_2/R_1)}}$$

where R_1 is the input side resistance and R_2 is the feedback resistance of the non-inverting amplifier.

$$\text{Let } \beta = \frac{1}{(1 + R_2/R_1)}$$

$$A_{ni} = \frac{A_v}{1 + A_v \beta}$$

$$\text{The single pole amplifier response } A_{v(s)} = \frac{A_o w_B}{s + w_B}$$

Substituting in the expression for A_{ni}

$$\begin{aligned} A_{ni} &= \frac{\frac{A_o w_B}{s + w_B}}{1 + \frac{A_o w_B \beta}{s + w_B}} = \frac{A_o w_B}{s + w_B (1 + A_o \beta)} \\ &= \frac{\frac{A_o}{1 + A_o \beta}}{1 + \frac{s}{w_B (1 + A_o \beta)}} \end{aligned}$$

$$\text{Let } w_H = w_B (1 + A_o \beta)$$

$$A_{ni}(s) = \frac{\frac{A_o}{1 + A_o \beta}}{1 + \frac{s}{w_H}}$$

$$\text{For, } A_o \beta \gg 1, A_{ni}(o) \approx \frac{1}{\beta}, w_H = w_B A_o \beta = w_T \beta$$

At low frequencies, gain is set by the feedback, but at high frequencies it follows the gain of the amplifier as shown in Fig.2.26

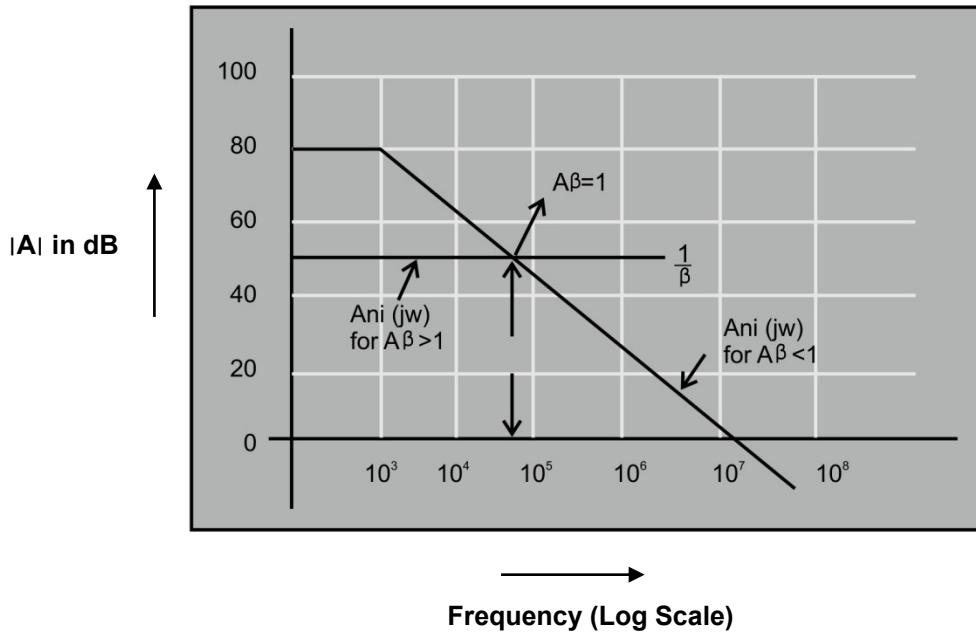


Fig 2.26 Frequency Response of Non-Inverting amplifier

Example 2.7

Find the closed loop Transfer Function of Non inverting amplifier with the following data

- (i) $A_o=10^5$ (ii) $f_T=10\text{MHz}$ (iii) $A_v=1000$

Assume that the amplifier is described by a single pole transfer function.

Solution

$$\text{Bandwidth, } f_B = \frac{f_T}{A_0} = \frac{10 \times 10^6}{10^5} = 100 \text{ Hz}$$

$$f_H = f_B(1 + A_o\beta)$$

$$= 100(1 + 10^5\beta)$$

$$\beta = \frac{1}{A_{v(0)}} = \frac{1}{1000} = \frac{1}{10^3}$$

$$f_H = 100(1 + 100) = 10100$$

$$= 10.1 \text{ kHz}$$

$$A_{v(0)} = \frac{w_T}{s + w_B(1 + A_o\beta)}$$

$$\text{Where } w_T = 2\pi f_T = 2\pi \times 10^7$$

$$w_B(1 + A_o\beta) = 2\pi \times 10^2(1 + 100) = 2\pi(1.01) \times 10^4$$

$$A_{v(0)} = \frac{2\pi \times 10^7}{s + 2\pi(1.01) \times 10^4}$$

2.12.2 Frequency Response of Inverting Amplifier

The expression for the voltage gain of an Inverting amplifier shown in Fig 2.1 is given by

$$A_{iv} = \frac{-\left(\frac{R_2}{R_1}\right)}{1 + \frac{1}{A_0}\left(1 + \frac{R_2}{R_1}\right)}$$

For single pole operational amplifier response is given by

$$A_{v(s)} = \frac{A_o w_B}{s + w_B}$$

Therefore,

$$\begin{aligned} A_{iv(s)} &= \frac{-\left(\frac{R_2}{R_1}\right)}{1 + \frac{s+w_B}{A_o w_B}\left(1 + \frac{R_2}{R_1}\right)} \\ &= \frac{-A_o w_B \left(\frac{R_2}{R_1}\right)}{A_o w_B + (s + w_B)\left(1 + \frac{R_2}{R_1}\right)} \\ &= \frac{-A_o w_B \left(\frac{R_2}{R_1}\right)}{A_o + \left(\frac{s}{w_B} + 1\right)\left(1 + \frac{R_2}{R_1}\right)} \end{aligned}$$

$$\text{Let, } \beta = \frac{1}{\left(1 + \frac{R_2}{R_1}\right)}$$

$$\begin{aligned} A_{iv(s)} &= \frac{-\left(\frac{R_2}{R_1}\right)}{1 + \left(\frac{s}{A_o w_B} + \frac{1}{A_o}\right) \frac{1}{\beta}} \\ A_{iv(s)} &= -\left(\frac{R_2}{R_1}\right) \frac{1}{1 + \frac{s}{A_o \beta w_B}} \end{aligned}$$

Therefore,

$$w_H = A_o \beta w_B = A_o w_T$$

Example 2.8

Find the open loop and closed loop transfer functions of an Inverting operational amplifier with the following specifications.

- i. Open loop gain $A_0 = 10^5$
- ii. Give Bandwidth product = 2.0 MHz
- iii. Desired voltage gain = -100
- iv. Assume that the amplifier is described by single pale transfer function.

Solution

$$\text{Bandwidth, } f_B = \frac{\text{Gain Bandwidth product(fT)}}{\text{Gain}}$$

$$= \frac{2 \times 10^6}{10^5} = 20 \text{ Hz}$$

$$\text{Feedback factor, } \beta = \frac{1}{1 + |A_{v(0)}|} = \frac{1}{101}$$

$$\begin{aligned} f_H &= f_B(1 + A_o\beta) = 20 \left(1 + 10^5 \times \frac{1}{101}\right) \\ &= 20 + 20 \times 990.1 = 20(1 + 990.1) \\ &= 9911 \times 2 = 19822 \text{ Hz} \\ &= 19.822 \text{ kHz} \end{aligned}$$

Open loop Transfer function

$$A_{v(s)} = \frac{w_T}{s + w_B}$$

$$= \frac{10^5 \times 20 \times 2\pi}{s + 20 \times 2\pi}$$

$$= \frac{4\pi \times 10^6}{s + 40\pi}$$

Inverting amplifier Transfer function

$$\begin{aligned} &= \frac{A_{v(0)}\beta w_T}{s + w_B (1 + A_o\beta)} \\ &= \frac{(-100) \times \frac{1}{101} \times 10^5 \times 20 \times 2\pi}{s + 40\pi \left(1 + 10^5 \times \frac{1}{101}\right)} \\ &= \frac{39.6\pi \times 10^5}{s + 40\pi(991)} \\ &= \frac{39.6\pi \times 10^5}{s + 39.64\pi \times 10^3} \end{aligned}$$

2.12.3 Frequency response with double pole

Most of the operational amplifiers will have single pole frequency response as mentioned in previous analysis, but some amplifier may have double pole frequency response as shown in Fig 2.27

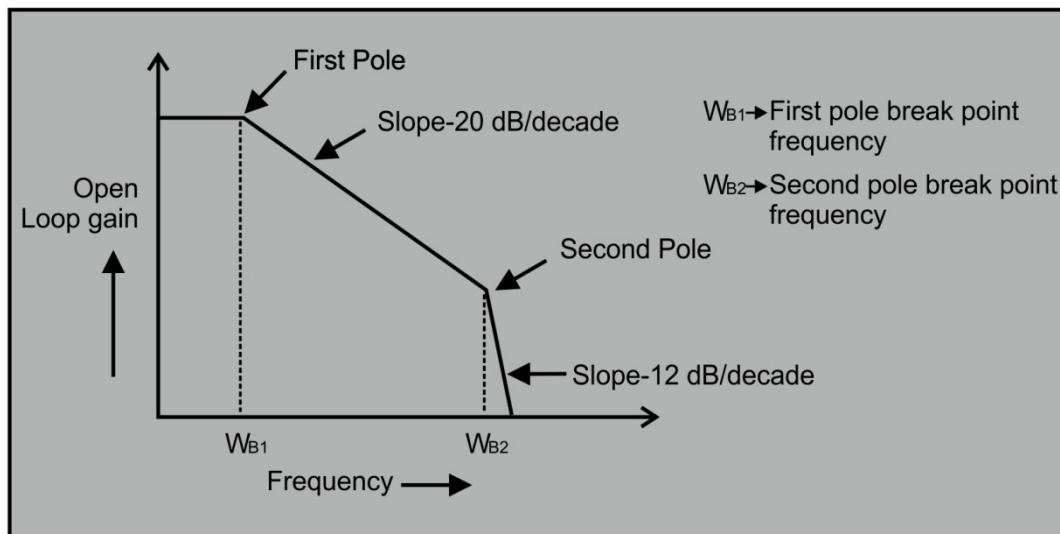


Fig 2.27 Two pole frequency response

The two pole transformation of the op Amp can be written as given below with two break point frequencies W_{B1} and W_{B2}

$$A_{V(s)} = \frac{A_{V(0)}}{\left(1 + \frac{s}{w b_1}\right) \left(1 + \frac{s}{w b_2}\right)}$$

Let $s = j\omega$

$$A_{V(j\omega)} = \frac{A_{V(0)}}{\left(1 + \frac{j\omega}{w b_1}\right) \left(1 + \frac{j\omega}{w b_2}\right)}$$

We know $\frac{w}{w b_1} = \frac{f}{f b_1}$ and $\frac{w}{w b_2} = \frac{f}{f b_2}$

$$|A_{V(j\omega)}| = \frac{A_0}{\sqrt{1 + \left(\frac{f}{f b_1}\right)^2} \sqrt{1 + \left(\frac{f}{f b_2}\right)^2}}$$

In decibel scale it can be written as

$$\begin{aligned} 20 \log |A_{V(j\omega)}| &= +20 \log A_0 - 20 \log \frac{f}{f b_1} - 20 \log \frac{f}{f b_2} \\ &= 20 \log A_0 - 20 \log \frac{f^2}{f b_1 + f b_2} \end{aligned}$$

At $f = f_T$, $20 \log |A_{V(j\omega)}| = 0$

$$\therefore 20 \log A_0 = 20 \log \frac{f_T^2}{f b_1 f b_2}$$

$$A_0 = \frac{f_T^2}{fb_1fb_2}$$

∴

$$f_T = \sqrt{A_0fb_1fb_2} \text{ Hz}$$

Example 2.9

Estimate the unity gain bandwidth of the operational amplifier with one pole at $fb_1 = 20 \text{ Hz}$ and another pole at $fb_2 = 50 \text{ Hz}$. Assume the open loop gain A_0 as 10^3 .

Solution

The expression for the unity gain Bandwidth is given by

$$\begin{aligned} f_T &= \sqrt{A_0fb_1fb_2} \text{ Hz} \\ &= \sqrt{1000 \times 20 \times 50} \\ &= \sqrt{10^6} \\ &= 1000 \text{ Hz} \end{aligned}$$

The unity gain bandwidth is 1000Hz

2.13 Interpretation of TL082 Data sheet

2.13.1 Introduction

The interpretation of data sheet of an operational amplifier is very essential for a designer. Designers must have a clear understanding of what op amp parameters mean and their impact on circuit design. They must be aware of the fact that different manufacturers use slightly different terminology. The data sheet generally has three columns for minimum, typical, and maximum values. Since it does not make sense to list values in all three columns, data is only listed for the appropriate columns for a given item, i.e. either minimum and typical or typical and maximum. For some parameters that are not controlled there may only be a typical value given.

The distribution of some parameters may have normal distribution. The typical value published in the data sheet is the mean or average value of the distribution. The typical value listed is the 1σ value. This means that in 68% of the devices tested, the parameter is found to be $\pm 1\sigma$ the typical value or better. Texas Instruments currently uses 6σ to define minimum and maximum values.

Usually, typical values are set when the part is characterized and never changes. Operational Amplifiers are generally classified into four categories namely, General purpose, Wideband, Precision and Special types (such as micro power, zero offset voltage and high output drive current).

2.13.2 General Classification of Op-amps

(i) General purpose Op Amps:

General purpose op amps are widely used in most of the applications where critical specifications are not important. They have decent specifications and are available at low cost. They generally have gain-bandwidth products in the range of 1 to 10 MHz and are very often unity gain stable.

(ii) Wideband Op Amps:

Wideband op-amps have gain-bandwidth products in the range of 10 MHz to over 1GHz. The DC specifications such as offset voltage, bias current, offset current etc. are often very inferior to other

types of op amps. Many of these op-amps are not unity gain stable and they must be operated with a minimum closed loop gain. Otherwise they may oscillate and become un-suitable for any applications. There is a special version of wideband op-amps that uses current feedback instead of voltage feedback. One has to study the application notes available in Data sheets.

(iii) Precision Op Amps:

These op-amps are designed for having premium DC specifications such as very low offset voltage and drift as well as very low bias current and drift. These tend to be expensive but are well worth it for the intended applications. The gain-bandwidth product is typically in the low 100 kHz range, which is really not important since the primary application is very low frequencies. These amplifiers are practically always unity gain stable. Some premium versions of these are rated for electrometer use and feature ultra-low bias current. These amplifiers also tend to have very low voltage and current noise.

(iv) Special feature operational Amplifiers:

Some special applications require op-amps with some special characteristic. The special characteristic is generally realized by a compromise of other characteristics. A short list of op-amp applications of this type would include micro-power, audio processing, high output drive current, etc. Some other special features include zero offset voltage, ultra-high common-mode voltage range and high power supply voltage amplifiers.

2.13.3 About TL082

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558, allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift. The connection diagram is shown in Fig. 2.28.

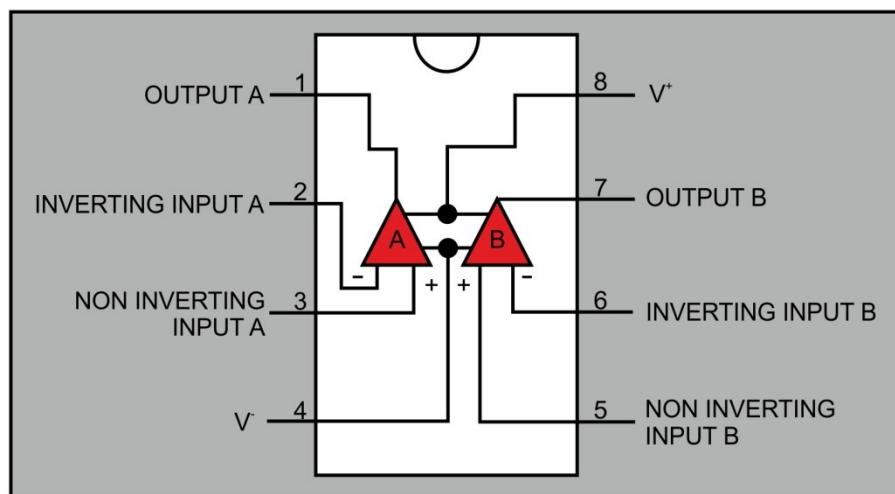


Fig 2.28 Pin connection diagram of TL082

2.13.4 Major features of TL082

- Internally Trimmed Offset Voltage: 15 mV
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16nV/ $\sqrt{\text{Hz}}$
- Low Input Noise Current: 0.01 pA/ $\sqrt{\text{Hz}}$
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/ μs
- Low Supply Current: 3.6 mA
- High Input Impedance: $10^{12} \Omega$
- Low Total Harmonic Distortion: $\leq 0.02\%$
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

2.13.5 List of common data sheet parameters

- (i) **Open-loop gain, A_0 :** The open-loop gain, A_0 is defined as the ratio of change in output voltage to the change in voltage across the input terminals. Usually the dc value and a graph showing the frequency dependence are shown in the data sheet. A_0 of an op-amp varies over a large range and may have values around 10,000 to over 10,00,000. A_0 varies with temperature and power supply voltage. A_0 for large signals is generally less than A_0 for small signals. A_0 is also expressed in dB scale as 80 dB to 120 dB. For LM 741 it varies from 50 dB to 200 dB and for TL082 it varies from 110 dB.
- (ii) **Input Offset voltage:** This refers to the apparent voltage difference between the inputs even when the inputs are shorted together. This voltage is typically in the single digit mille volts but can be over ten mille volts for very high speed op-amps. Some op-amps are factory trimmed so that the net offset voltage is well under 100 microvolts. The data sheet will show a guaranteed maximum and a typical value. A minimum value is never shown as it's not relevant. The offset voltage is not purely static. It varies with power supply voltage, temperature, common-mode voltage and other parameters. For LM741 it is 1 mV and for TL082 it is 5 mV.
- (iii) **Offset voltage drift:** This specification is usually given as it relates to drift with temperature and has typical units of microvolts per degree C. For LM741A the worst case drift is 15 microvolt per C0. For TL082 the average value of offset voltage drift is 10 μV .
- (iv) **Input bias current:** This value is typically in the nanoampere region but can be in the picoampere region for premium op amps and even the femtoampere region for op-amps made for what are known as electrometer applications. Bias current can be either positive or negative. Each input has its own bias current within the specified maximum magnitude on the data sheet. Bias current is not purely static. It varies with power supply voltage, temperature, common-mode voltage and other parameters. The maximum value shown on the data sheet often represents the worst case taking all parameters into account. Typical value for bias current of LM741 is 80 nA. The value of input bias current is 50 nA.
- (v) **Input offset bias current:** The difference between the bias current for the non-inverting input and the bias current for the inverting input is known as the offset bias current (often referred to as the offset current). The data sheet indicates a maximum value that is typically in the range of ten to thirty percent of the magnitude of the maximum bias current. Input offset bias current is

not purely static. It varies with power supply voltage, temperature, common-mode voltage and other parameters. For LM741 offset bias current is 200 nA (Max). For TL082 it is 200 p A (Max).

(vi) **Input bias current drift:** The input bias current drift due to temperature is usually given as picoamperes per degree C. The specification is usually given as a magnitude as the drift can be of either polarity. The average input offset current for LM741A is 0.5 nA (Max).

(vii) **Common-mode input voltage range:** This is the range of common-mode input voltage that, if exceeded, may cause the operational amplifier to cease functioning properly. This is sometimes taken as the voltage range over which the input offset voltage remains within a set limit. The common-mode input voltage must be between the specified limits in order for the op-amp to work. If the voltage is outside this range, then the output of the amplifier is undefined – it may go to either the positive or negative saturation levels. The range of common mode input voltage is from a few volts above the lower power supply voltage to a few volts below the upper power supply voltage. For TL082 it is +15 V to – 12 V.

(viii) **Maximum output voltage:** This specification is a measure of how close the output voltage can be to the upper power supply. Typically, this is roughly 2.5 volts which means that for a +15 volt VCC, the maximum output voltage of a common op-amp is about 12.5 volts. Some op-amps have what is known as rail-rail output stages and those can put out a voltage that is within millivolts of VCC. Maximum output voltage for TL082 is + 13.5 V for a supply voltage of +15V. The same voltage for LM741 is + 13V.

(ix) **Output Short Circuit Current:** The maximum current that the op amp can source or sink from the output pin is called output short circuit current. Typically most of the op amps can deliver more than 25 mA. Typical value for the LM741 op amp is 25 mA at 250 C.

(x) **Gain-bandwidth product:** This is the extrapolated unity gain frequency which by definition is the frequency at which the gain of the op-amp has dropped to 1.0. This is often at least several hundred kilohertz and could be over 1 GHz for some op-amps. The term, gain bandwidth product comes from multiplying the gain of the amplifier at DC by the frequency at which the gain has dropped by 3 dB (this is often around 10 Hz). The gain bandwidth product for TL082 is 4 MHz.

(xi) **Slew rate:** The slew rate is the maximum rate of change in the output voltage and has typical units of volts per microsecond. Low-bandwidth amplifiers may have a limit of less than a volt per microsecond. Wide bandwidth amplifiers may have a limit of over 50 volts per microsecond. The slew rate limit is usually different for positive going signals than for negative going signals. The slew rate for LM741 is 0.5 V/ μ s and the same for TL082C is 3 V/ μ s.

(xii) **Input resistance:** This is the input resistance with respect to circuit ground and is often many megohms, especially if the input stage of op amp is based on field-effect transistors. Except for wideband amplifiers, the input resistance is often treated as infinite. Input resistance for LM741 is 2 M Ω and that of TL082 is 1012 Ω .

(xiii) **Common-mode rejection ratio (CMRR):** It is a measure of how well the amplifier rejects common-mode signals at the inputs. An ideal amplifier would have infinite rejection. CMR is given at DC and has typical specs in the 60 to 100 dB range and decreases as the frequency is increased. Typical value for TL082C is 100 dB and for LM741 it is 90 dB.

(xiv) **Power supply rejection ratio (PSRR):** It is a measure of how well the amplifier protects the output voltage from variations on the power supply voltages. An ideal amplifier would have infinite rejection. PSRR is generally provided at some low frequency and has typical values in the range of 60 to 100 dB. It degrades as frequency is increased. At high frequencies, PSRR

may be only between -6 and 10 dB. PSRR for the negative supply is often worse than PSR for the positive supply. The PSSR for TL082C is 100 dB and for LM741 it is 96.

2.13.6 DC and AC Electrical Characteristics

DC Electrical Characteristics ⁽¹⁾

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S = 10 kΩ, T _A = 25°C Over Temperature		5	15	mV
					20	mV
ΔV _{OS} /ΔT	Average TC of Input Offset Voltage	R _S = 10 kΩ		10		μV/°C
I _{OS}	Input Offset Current	T _j = 25°C, ⁽¹⁾ ⁽²⁾ T _j ≤ 70°C		25	200	pA
					4	nA
I _B	Input Bias Current	T _j = 25°C, ⁽¹⁾ ⁽²⁾ T _j ≤ 70°C		50	400	pA
					8	nA
R _{IN}	Input Resistance	T _j = 25°C		10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S = ±15V, T _A = 25°C, V _O = ±10V, R _L = 2 kΩ Over Temperature	25 15	100		V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10 kΩ	±12	±13.5		V
V _{CM}	Input Common-Mode Voltage Range	V _S = ±15V	±11	+15 -12		V
CMRR	Common-Mode Rejection Ratio	R _S ≤ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	⁽³⁾	70	100		dB
I _S	Supply Current			3.6	5.6	mA

(1) These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j = T_A + θ_{JA} P_D where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

AC Electrical Characteristics ⁽¹⁾

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T _A = 25°C, f = 1Hz-20 kHz (Input Referred)		-120		dB
SR	Slew Rate	V _S = ±15V, T _A = 25°C	8	13		V/μs
GBW	Gain Bandwidth Product	V _S = ±15V, T _A = 25°C		4		MHz
e _n	Equivalent Input Noise Voltage	T _A = 25°C, R _S = 100Ω, f = 1000 Hz		25		nV/√Hz
i _n	Equivalent Input Noise Current	T _j = 25°C, f = 1000 Hz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A _V = +10, R _L = 10k, V _O = 20 Vp - p, BW = 20 Hz-20 kHz		<0.02		%

(1) These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

2.13.7 Application Notes for TL082

The TL082 is an operational amplifier with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a

latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range of 0°C to $+70^{\circ}\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that power supply to the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit. Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground. A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

2.14 Summary

In the first chapter, we discussed the need for operational amplifiers, its equivalent circuit and an analysis of inverting and non-inverting configurations. The purpose of the second chapter was to understand parameters of various types of practical operational amplifier and ways to estimate the percentage error caused by finite gain when compared to that of ideal amplifier. We started the chapter by comparing parameter values of typical operational amplifiers. Then, we studied the effect of finite loop gain on Closed loop gain, Input Resistance and Output resistance. The analysis was extended to Voltage follower or Buffer Amplifier. The method of estimating the offset voltage at the output was discussed along with methods to adjust the same.

This was followed by a detailed discussion on frequency response of operational amplifiers with one pole and double pole. We also included a detailed description of the parameters and application notes for TL082.

With this base, readers are well-quipped to understand the applications of operational amplifiers discussed in subsequent chapters.

2.15 Review Questions

1. What are the assumptions made for an ideal operational amplifier used for analysis?
2. Discuss the typical parameters of a general purpose operational amplifier.
3. Derive an expression for the gain of a non-Inverting amplifier in terms of feedback resistance R_2 , input side resistance R_1 , and open loop gain A_0 . Comment on the variation of gain with respect to open loop gain A_0 .
4. What do you mean by differential input resistance? Discuss the effect of open loop gain on the input resistance of an inverting Amplifier.
5. What is the specialty of an operational amplifier voltage follower? Mention few applications for the same.
6. Distinguish between Input offset current and Input bias current. How will you find the input current into non-Inverting terminal from the values of offset and bias currents?
7. Discuss the methods adopted for getting null offset voltage at the output of an operational amplifier. Compare their merits and demerits.
8. What do you mean by slew rate? How does it affect the output voltage waveform?
9. Discuss briefly the general classifications of operational amplifiers.

2.16 Exercises

1. In an inverting amplifier, the feedback resistance R_2 is $110\text{ K}\Omega$ and input side resistance R_1 is $2.2\text{ K}\Omega$. Estimate the gain for an ideal operational amplifier as well as for an operational amplifier with an open loop gain of 1000

Answer: [-50, -47.574]

2. Estimate the percentage error caused by the non-Inverting amplifier given below with a finite gain.

- (i) Feedback resistance $R_2 = 200\text{K}\Omega$
- (ii) Input side resistance $R_1 = 20\text{K}\Omega$
- (iii) Open loop gain $A_0 = 10,000$

Answer: [0.109 %]

3. Estimate the input Resistance R for a Von-Inverting amplifier specified below.

- (i) Feedback resistance $R_2 = 100\text{K}\Omega$
- (ii) Inverting input to ground resistance $R_1 = 10\text{K}\Omega$
- (iii) Differential input resistance of the operational amplifier $R_{di} = 2 \times 10^6\Omega$
- (iv) Open loop gain of the output is 1000.

Answer: [183.8 MΩ]

4. Find the output resistance of the Non-Inverting amplifier with $R_2 = 50\text{K}\Omega$, $R_1 = 10\text{K}\Omega$ output resistance of the operational amplifier = 65Ω and open loop gain = 10^3

Answer: [0.323 Ω]

5. Estimate the output voltage of the op Amp with the following details.

Non-Inverting input voltage $u_1 = 1.999$ voltage

Inverting input voltage $u_2 = 2.000$ Voltage

Open loop gain = 10^3 CMRR=80 d

Compare the result with an ideal op Amp.

Answer: [1 Volt, 1.1999 Volts]

Amplifiers and Oscillators

The first two chapters were dedicated to creating a basic understanding of operational amplifiers and their functioning. But signals generated by these devices are generally of very low magnitude. In order to be useful, these signals need to be modified/ amplified to suitable levels.

Therefore, this chapter is focused on the design of suitable amplifier circuits, understanding the effect of input parameter variation and influence of feedback path component in the output of Operational Amplifier.

Readers will also be able to identify suitable feedback mechanisms and oscillators required as per application. The chapter will also cover details on the availability and functionality of ICs for some specific applications.

Topic	Page
3.1 Introduction	77
3.2 Summing amplifier	78
3.3 Averaging Amplifier.....	81
3.4 Scaling Amplifier	82
3.5 Integrator	83
3.6 Differentiator	86
3.7 Instrumentation amplifier	89
3.8 Differential Input and Differential Output Amplifiers	92
3.9 Feedback Amplifiers	94
3.10 Log / Antilog Amplifiers	102
3.11 Isolation Amplifiers.....	105
3.12 Triangular/ Rectangular Wave Generator	107
3.13 Oscillators	109
3.14 Analog Multiplier	115
3.15 Voltage Controlled Oscillator: (VCO).....	119

3.1 Introduction

Most signals carrying useful information to this world are weak signals. Human physiological signals that enable disease diagnosis; signals broadcasted via radio receiver or telecasted through television receivers are all low level signals. There, it is required that we improve the strength of signals to recognize information without altering its nature. The amplifier does this job and is essential to learn about amplifiers for various applications.

There are various types of amplifiers that can be designed according to the need. Amplifiers have a tremendous impact on electronic system design, especially when it comes to real life applications. For example, let's consider how human body temperature is displayed in an electronic thermometer. The sensor produces analog output voltage and needs to be converted into digital for further processing. For the conversion of voltage into digital data, the converter requires sufficient input voltage from the sensor. Therefore, sensor output needs to be amplified by an amplifier to meet the requirement level of the digital converter. The digitized amplified voltage is processed further and displayed in the thermometer.

Similarly, oscillators are useful to construct the real life applications. The oscillator is a device used to produce waveforms such as sine, square, ramp, sawtooth etc. The frequency and amplitude of the waveforms i.e. oscillations can also be controlled according to the application. The oscillator can also convert DC energy into AC energy and hence, it is also called as DC to AC converter. Oscillators are used in laboratory testing and measuring instruments such as function generators and oscilloscopes.

They are effectively used in communication equipment such as AM and FM systems, RF receivers, Radio transmitters and radar systems etc. Oscillators are also used as clock sources for microcomputers and crystal oscillators. Various frequency ranges are available in the commercial market for applications development. For example, the logic chip designed for use in computers needs 24 MHz frequency of oscillation for its normal operation. A commercially available crystal oscillator with 24 MHz can be purchased or else the oscillator can be designed and directly connected with the chip to complete the requirement. Hence, it is also important to learn about oscillators.

Generally, based on the need of real time applications, devices which are used to construct those applications are expected to produce the linear output or non-linear output. An Operational Amplifier can produce both kind of outputs based on its configuration. Therefore, the Op-Amp based amplifiers which fall in to the category of linear systems and Op-Amp based oscillators which fall in to the category of non-linear systems are discussed in this chapter.

3.2 Summing amplifier

An op-amp amplifier designed to add each input and produce the output based on the configuration is called summing amplifier. The op-amp may be used to design the inverting summing amplifier with the gain of unity or gain greater than unity or non-inverting summing amplifier. The summing amplifier circuit can also be adjusted or modified to behave like an averaging amplifier or else the scaling amplifier.

The summing amplifiers are used to add different kind of signals to produce the common output signal expected for the application. The input signals can be given either to non-inverting terminal or to inverting terminal. The most popular application of summing amplifier is an Audio mixer.

3.2.1 Inverting Summing Amplifier

The figure 3.1 shows the two input inverting summing amplifier. The number of inputs can be increased any time. The voltage sources V_1 and V_2 are connected to the inverting terminal of op-amp through resistors R_1 and R_2 to produce the input current I_1 and I_2 . Since the point V_G is virtual ground, the current flow takes the direction of feedback path in which the resistor R_f is connected.

Therefore when $V_1=0$, V_2 = Input voltage supply, $I=I_2$,

$$\text{And, } V_{out} = \frac{-R_f}{R_2} \cdot V_2$$

Therefore when V_1 = Input voltage supply, $V_2=0$, $I=I_1$,

$$\text{And, } V_{out} = \frac{-R_f}{R_1} \cdot V_1$$

When $V_1=V_2$ =Input voltage supply, $I=I_1+I_2=I_t$

$$V_{out} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right) R_f \quad (3.1)$$

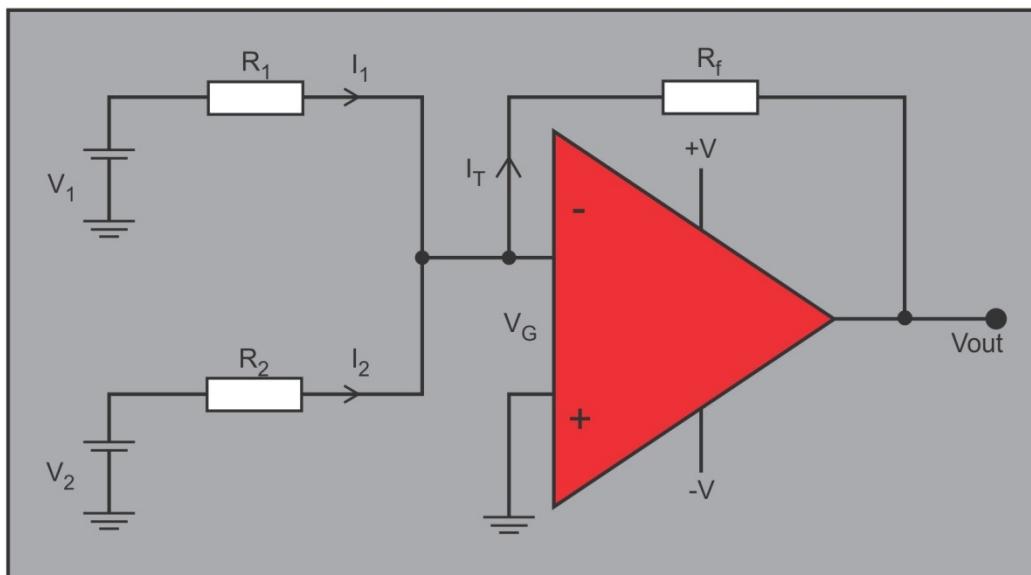


Fig 3.1 Inverting Summing Amplifier

For example, in music recording studios today, vocals and background music are recorded separately. They are both mixed in the audio mixer to produce the complete song with music.

Because of this facility, these events can be executed according to the convenience of the singers and music players. The op-amp inverting summing amplifier is used as an audio mixer to fulfill this application and is shown in figure 3.2.

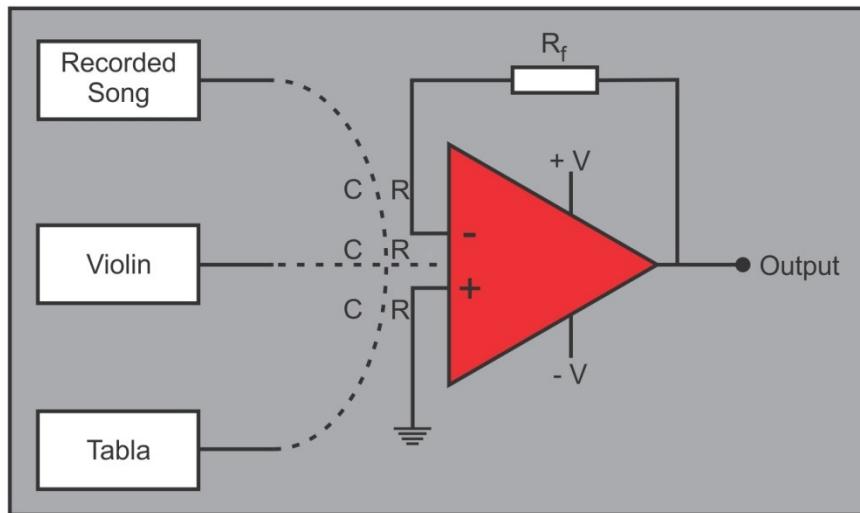


Fig 3.2 Inverting Summing Amplifier Audio Mixer

3.2.2 Inverting Summing Amplifier with Unity Gain

When the value of resistors R_1 , R_2 and R_f are equal in figure 3.1, the output gain of the amplifier is unity and can be expressed as,

$$V_{out} = -(V_1 + V_2) \quad [\text{Since } R_1=R_2=R_f] \quad (3.2)$$

Therefore the output is equal to the number of inputs since the gain is unity.

3.2.3 Inverting Summing Amplifier with Gain Greater than Unity

When R_f is greater than R [since $R=R_1=R_2$] in figure 3.1, the output gain of the amplifier is greater than unity and can be expressed as

$$V_{out} = -\frac{R_f}{R}(V_1 + V_2) \quad (3.3)$$

3.2.4 Non-inverting Summing Amplifier

The figure 3.3 shows two input non-inverting summing amplifier. The number of inputs can be increased any time. The voltage sources V_1 and V_2 are connected to the non-inverting terminal of op-amp through resistors R_1 and R_2 to produce the input current I_1 and I_2 .

Therefore when $V_1=0$, V_2 = Input voltage supply

$$V_{out} = \left(1 + \frac{R_f}{R}\right) \left(\frac{\frac{V_2}{R_2}}{\frac{1}{R_2}} \right) = \left(1 + \frac{R_f}{R_i}\right) V_2$$

When $V_2 = 0$, V_1 = Input voltage supply

$$V_{out} = \left(1 + \frac{R_f}{R}\right) \left(\frac{V_1}{R_1} \middle/ \frac{1}{R_1} \right) = \left(1 + \frac{R_f}{R_i}\right) V_1$$

When $V_1=V_2$ =Input voltage supply

$$V_{out} = \left(1 + \frac{R_f}{R_i}\right) \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} \middle/ \frac{1}{R_1} + \frac{1}{R_2} \right) = \left(1 + \frac{R_f}{R_i}\right) \left(\frac{V_1 + V_2}{2} \right) \quad (3.4)$$

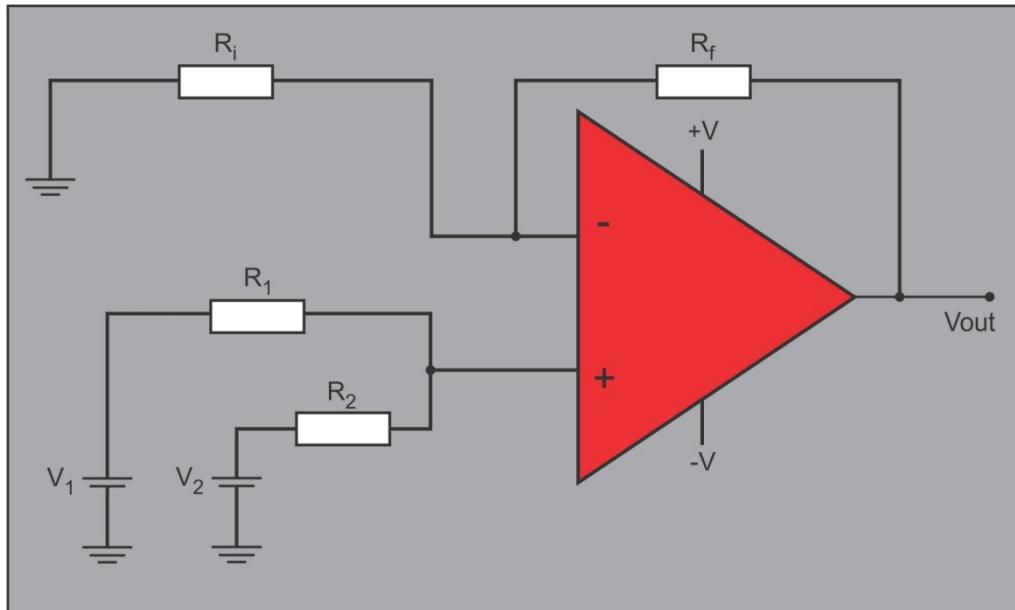


Fig 3.3 Non-inverting Summing Amplifier

The application shown in figure 3.2 can also be designed using non inverting summer. In biomedical signal acquisition such as ECG, sometimes the acquired signals are to be level shifted (negative to positive level) for further processing. The non-inverting summing amplifiers are implemented for this kind of level shifting applications also.

3.3 Averaging Amplifier

A summing amplifier designed such that the output voltage is equal to the average of all input voltages, is called an average amplifier. The average amplifier (shown in figure 3.4) output can be achieved by making a gain (i.e.) $\frac{R_f}{R_{in}}$ of summing amplifier equal to the reciprocal of number of inputs.

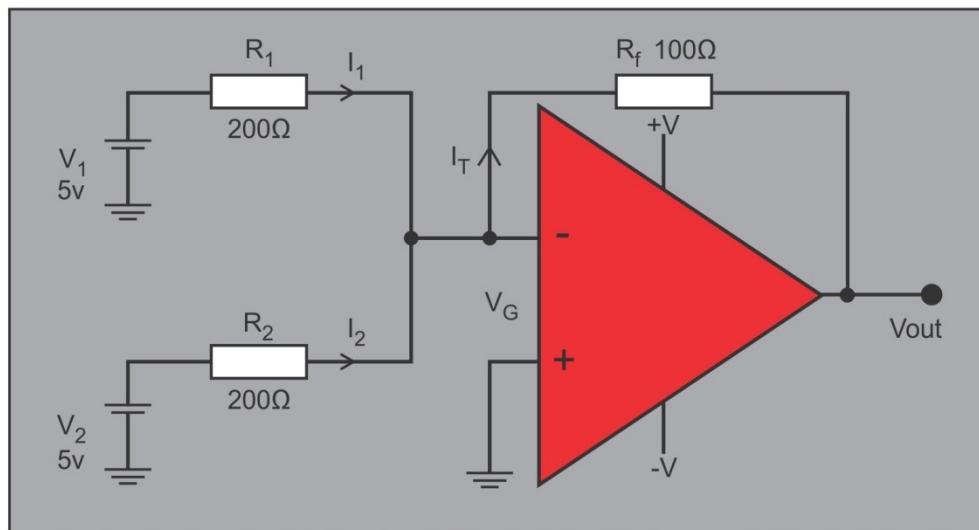


Fig 3.4 Averaging Amplifier

$$V_{out} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)R_f \quad (3.5)$$

Let $R_1 = R_2 = 200 \Omega$, $R_f = 100 \Omega$ and $V_1 = V_2 = 5 \text{ V}$

$$\begin{aligned} V_{out} &= -\left(\frac{5}{200} + \frac{5}{200}\right)100 \\ V_{out} &= -5 \text{ V} \end{aligned}$$

$$V_{inaverage} = \left(\frac{V_1 + V_2}{2}\right) \quad (3.6)$$

$$V_{inaverage} = \left(\frac{5 + 5}{2}\right) = 5V$$

By considering the application shown in figure 3.2, the signal levels i.e. voltage levels of different instruments may be different. But for better quality of audio output, the optimum level of signal mixing is important and an averaging amplifier does the job. Hence, suitable audio surround systems can be developed with additional amplifiers like power amplifiers.

3.4 Scaling Amplifier

The summing amplifier circuit designed with various values of input resistors is called scaling amplifier (shown in figure 3.5). This amplifier is also called a weighted amplifier since different weight is assigned to each input.

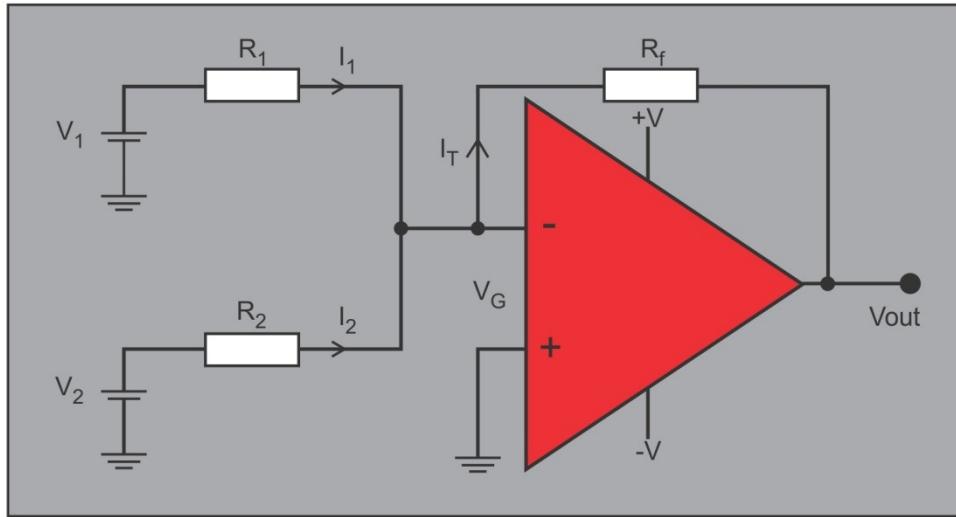


Fig 3.5 Scaling Amplifier

$$\begin{aligned} V_{out} &= -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right) \text{ OR} \\ V_{out} &= -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)R_f \end{aligned} \quad (3.7)$$

Let $R_1 = 200 \Omega$, $R_2 = 100 \Omega$ and $R_f = 400 \Omega$

$$\text{Weight for input A} = \frac{R_f}{R_1} = \frac{400}{200} = 2$$

$$\text{Weight for input B} = \frac{R_f}{R_2} = \frac{400}{100} = 4$$

$$V_{out} = -[(2[2]) + (4fo)]$$

$$V_{out} = -(4 + 16)$$

$$V_{out} = -20 V$$

Scaling amplifiers are used as digital to analog converters to convert the digital data into analog voltage, which is required to drive the output devices. The $R - 2R$ ladder type of weighted resistor network can be connected to the input terminal of the op-amp as shown in the figure 3.6.

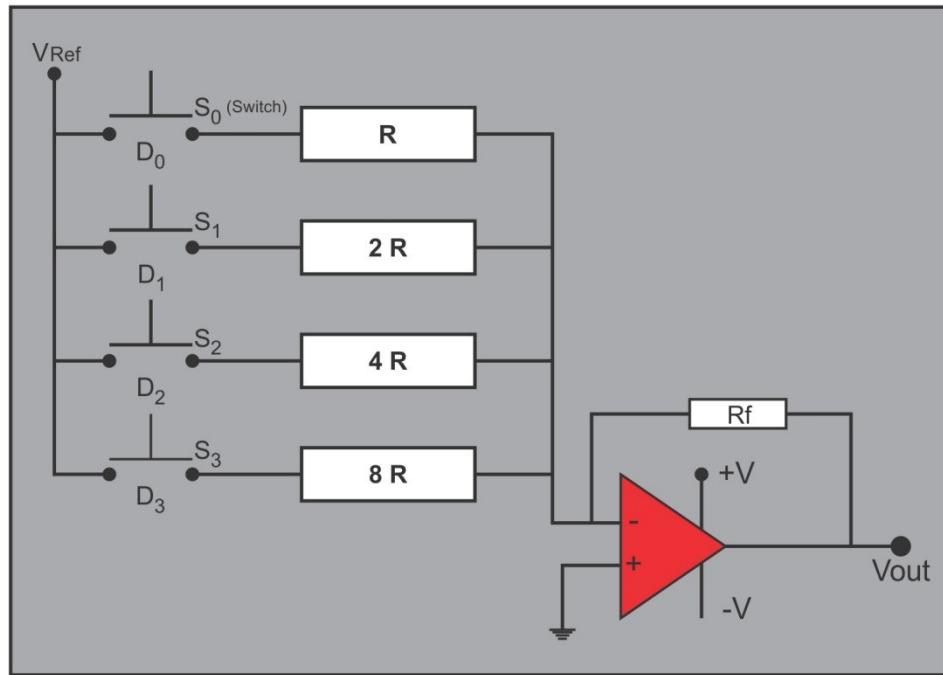


Fig 3.6 Scaling Amplifier as Analog to Digital Converter

3.5 Integrator

A circuit which produces the integral form of the input voltage wave form at the output is known as integrator. The feedback resistor R_f in the inverting amplifier is replaced by the capacitor C_F as shown in the figure 3.7 is able to achieve this integral output.

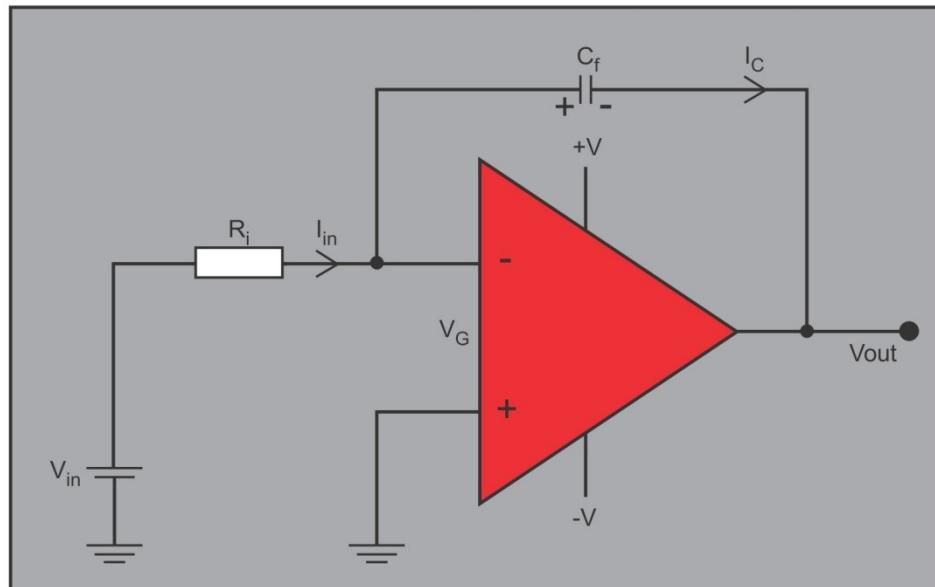


Fig 3.7 Basic Inverting Integrator

In a basic RC circuit, the capacitor is charged exponentially due to decreasing charging current. But in the integrator circuit, the capacitor charging is constant due to the presence of an op-amp and hence it

is linear. In the figure 3.7, the input current I_{in} for the applied voltage V_{in} is bypassed to the feedback path because of the virtual ground V_G and high input impedance of the op-amp. Hence the current I_c flowing through the capacitor C_f is equal to the input current I_{in} . This phenomenon causes the capacitor to charge linearly. Since the negative side of the capacitor is at op-amp's output side, the output voltage V_{out} starts decreasing from '0' while the capacitor charges and vice versa as shown in figure 3.8.

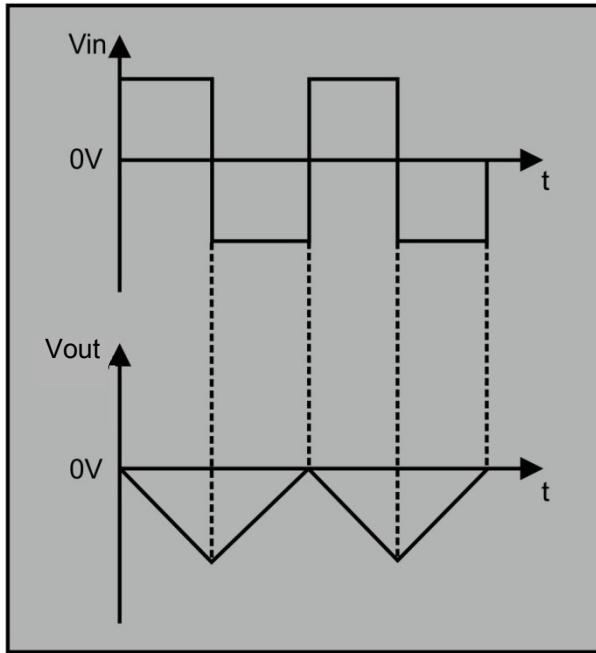


Fig 3.8 The input square waveform and the output triangular waveform

Therefore the integrator's output voltage change at the rate of

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{1}{R_i C_f} V_{in}$$

and can be rewritten as

$$V_o = -\frac{1}{R_i C_f} \int_0^t V_{in} dt + C \quad (3.8)$$

The equation 3.8 shows that the output voltage V_o is inversely proportional to time constant $R_i C_f$ and directly proportional to the negative integral of the input voltage V_{in} . 'C' is constant and is proportional to the output voltage V_o at time $t = 0$ s. Since the output voltage is negative; it is also referred as an inverting integrator.

The frequency response of the basic integrator and practical integrator are shown in figure 3.9. From the figure 3.9, the frequency response of basic integrator f_B is

$$f_B = \frac{1}{2\pi R_i C_f} \text{ at gain of } 0 \text{ db} \quad (3.9)$$

The figure also shows that the gain of the integrator is almost saturated at low frequencies. But the gain decreases at high frequencies.

In practical integrator circuit, the higher value of resistor ' R_f ' is connected in parallel to the capacitor C to achieve the following

- i. Avoid the saturation of integrator by limiting the gain at low frequency
- ii. The error voltage at the output
- iii. Stabilize the gain for the variation of input signal frequency after certain range

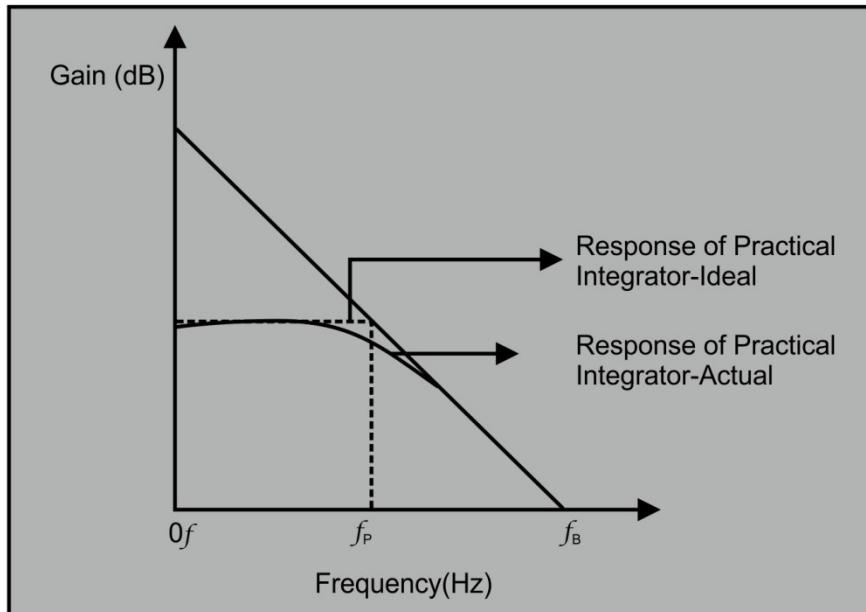


Fig 3.9 Frequency response of basic and practical integrator

The gain R_f/R is constant between the frequencies f and f_p . ' f ' is assumed as certain frequency and f_p is the critical frequency or frequency in practical where the real integrator function begins. Hence, between f_p and f_B , the circuit perfectly behaves as an integrator. Therefore, f_p is also referred as gain limiting frequency and can be written as

$$f_p = \frac{1}{2\pi R_f C_f} \quad (3.10)$$

For the perfect integration, the time period 'T' of the input signal should be greater than or equal to $R_f C_f$.

Function generator is a device which produces sinusoidal, square, triangular waves etc to test the other electronic devices. Integrator is the heart of the function generator shown in figure 3.10 which produces triangular wave. Along with the voltage comparator multivibrator, integrator produces square wave for the function generator. Along with the resistance diode network, integrator also produces sinusoidal waves. Integrator is also a part of PID controller.

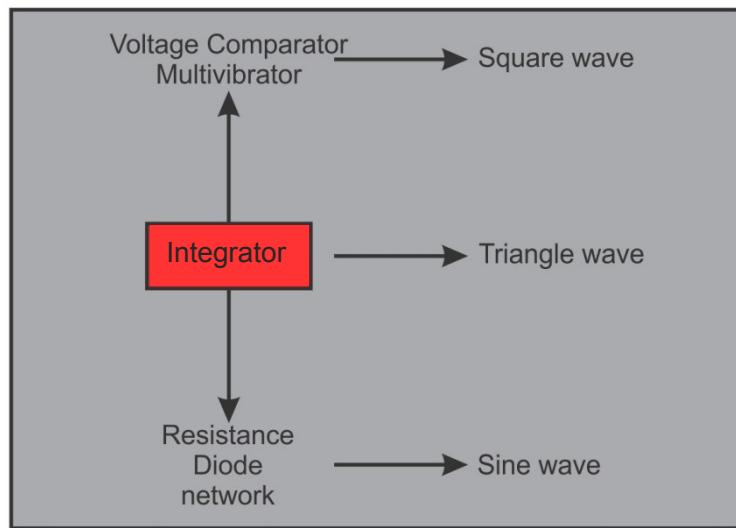


Fig 3.10 Integrator as a Function Generator

3.6 Differentiator

A circuit which produces the derivative of the output voltage waveform for the given input voltage waveform is known as differentiator. The input resistor R_i in the basic inverting amplifier is replaced by the capacitor C_i as shown in the figure 3.11 is able to achieve the differentiation output.

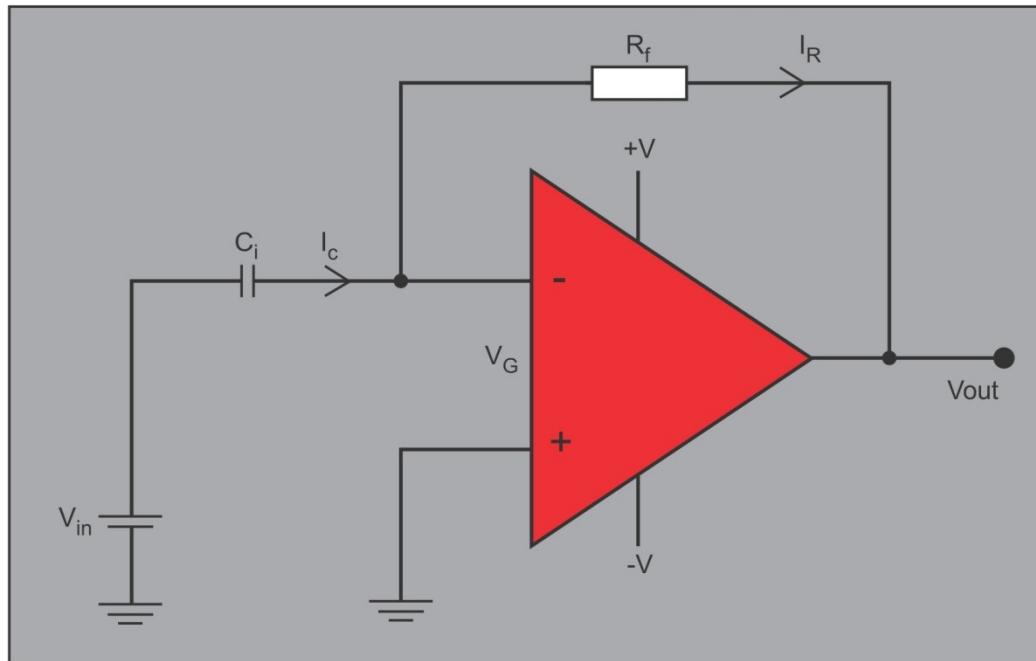


Fig 3.11: Inverting Differentiator

When the input voltage V_{in} is applied, the voltage across the capacitor V_c is same as V_{in} and current flowing through the capacitor I_c is equal to I_{in} due to virtual ground at inverting input of the op-amp. Therefore

$$V_{out} = I_r R_f = I_c R_f = -\frac{dV_c}{dt} C \cdot R_f \quad [\text{Since } I_c = \frac{dV_c}{dt} C]$$

$$V_{out} = -\frac{dV_{in}}{dt} C \cdot R_f \quad [\text{Since } V_c = V_{in}] \quad (3.11)$$

Therefore the output of the differentiator is negative going square pulse for positive going ramp and vice versa as shown in figure 3.12. The output voltage V_{out} is $-R_f C$ times the rate of change of the input voltage V_{in} with respect to time as shown in figure 3.12.

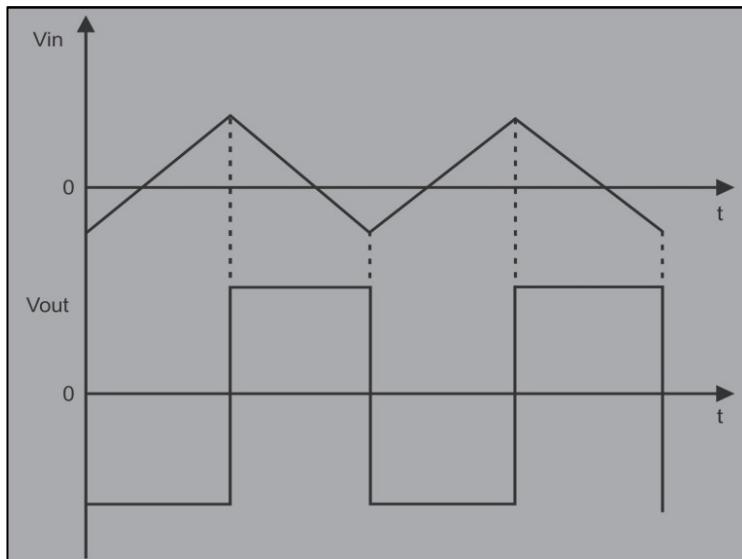


Fig 3.12 The input triangular waveform and the output square waveform

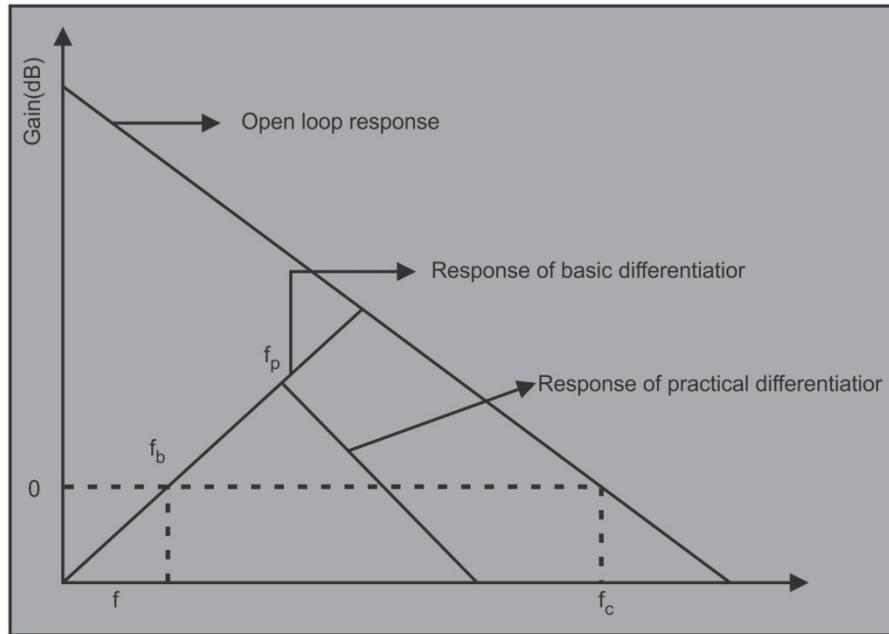


Fig 3.13 Frequency response of basic and practical differentiator

The frequency response of the basic differentiator and practical differentiator are shown in figure.3.13.

From the figures 3.11 and 3.13, the frequency response of basic differentiator is

$$fB = \frac{1}{2BR_f C_i} \text{ at gain of } 0 \text{ dB} \quad (3.12)$$

It is also clear that for the increase of frequency, the gain increases. Hence, the circuit is unstable.

In practical differentiator, resistor R_i in the input path and capacitor C_f which is in parallel to the resistor R_f in the feedback path are added as shown in the figure 3.14 to improve the stability as well as remove the high frequency noise for decreasing input impedance with increasing frequency for ac inputs.

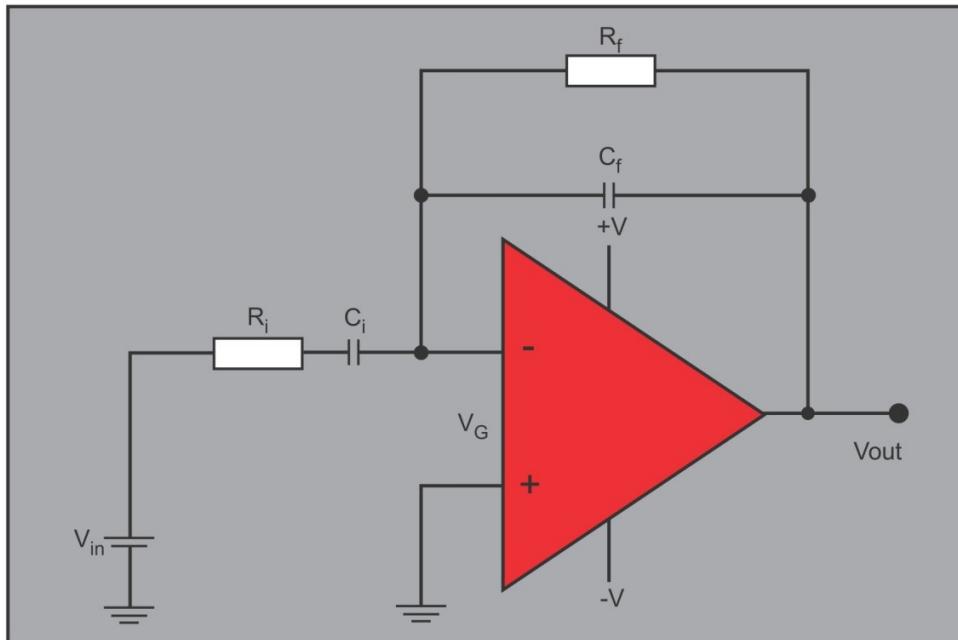


Fig 3.14 Practical Inverting Differentiator

The gain increases between the frequencies f and f_p . The change of gain is due to the combination of $R_i C_i$ and $R_f C_f$. Therefore the gain limiting frequency f_p is

$$f_p = \frac{1}{2\pi R_i C_i} \quad (3.13)$$

Where $R_i C_i = R_f C_f$

For the perfect differentiation, the time period 'T' of the input signal should be greater or equal to $R_f C_i$.

PID controller shown in figure 3.15 is referred as a Proportional – Integral – Derivative controller used in industrial process control systems to evaluate the error between the measured value and threshold set value. In this, the derivative of error in process is estimated by the differentiator circuit.

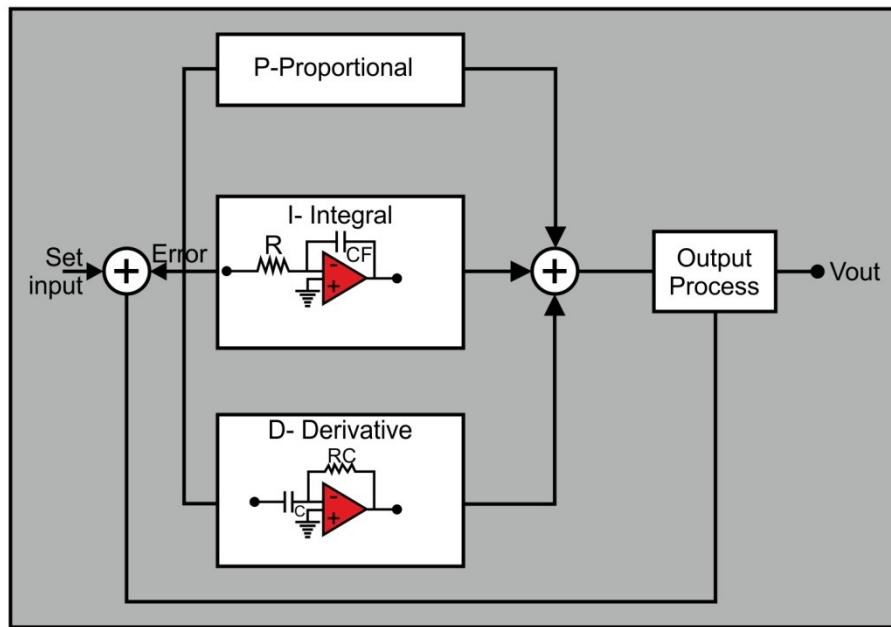


Fig 3.15 Differentiator and Integrator in PID Controller

3.7 Instrumentation amplifier

An instrumentation amplifier is a device that amplifies the difference between the voltages at its two input terminals and hence known as differential voltage gain amplifier. This amplifier can be used for accurate and low signal amplification of signals with the common mode input. The instrumentation amplifier has the characteristics such as

- High input impedance
- Low output impedance
- High Common Mode Rejection Ratio (CMRR)
- Low output offset (dc offset) and
- High gain stability

It can be used for the applications that include data acquisition systems where high common mode noise dominates, measurement of physical quantities such as temperature, humidity, bio signal measurement and optical signal intensity measurements.

The figure 3.16 shows the basic instrumentation amplifier circuit. The gain of the circuit can be adjusted by connecting the external gain setting resistor ' R_G ' shown in the figure 3.16.

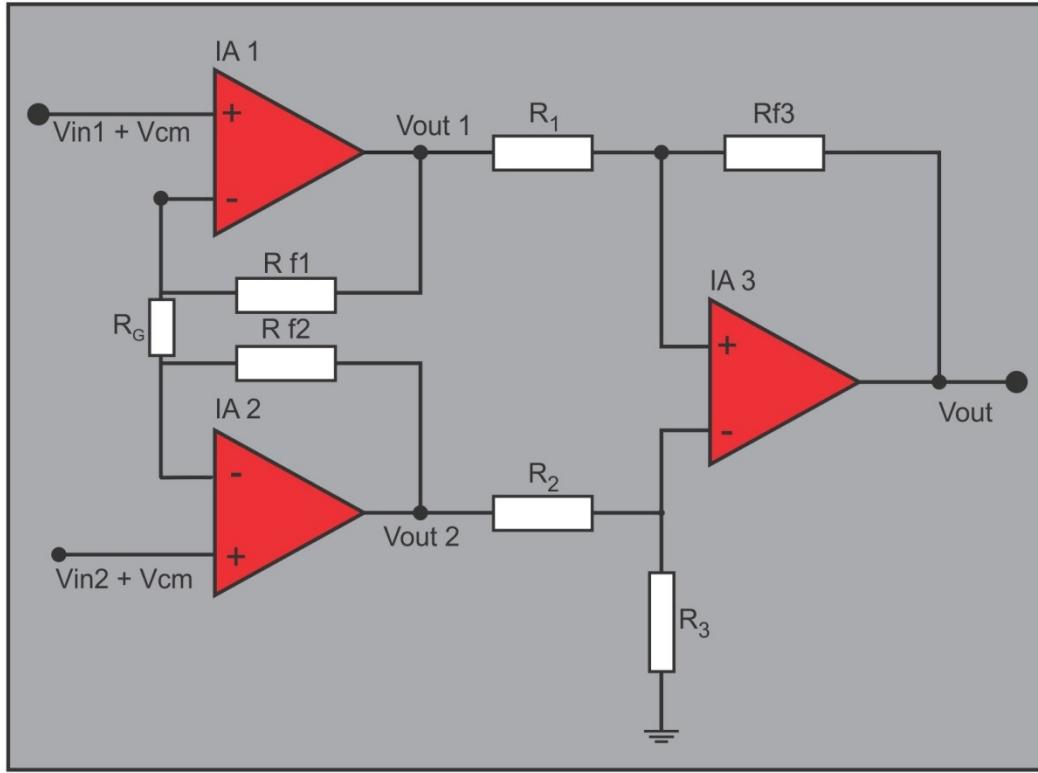


Fig 3.16 Instrumentation Amplifier with external gain setting resistor R_G

The input voltage V_{in1} is given to the non-inverting terminal of op-amp IA1 and the gain is

$$Av = 1 + \frac{R_{f1}}{R_G}$$

The inverting terminal of the op-amp IA1 is received the input from op-amp IA2 through resistors R_{f2} and R_G and the gain is

$$Av = \frac{R_{f1}}{R_G}$$

Therefore the total output voltage

$$V_{out1} = \left(1 + \frac{R_{f1}}{R_G}\right) V_{in1} - \left(\frac{R_{f1}}{R_G}\right) V_{in2} + V_{CM} \quad (3.14)$$

Since the V_{CM} is also amplified by the op-amp IA1 along with V_{in1} .

Similarly the output voltage V_{out2} of op-amp IA2 is

$$V_{out2} = \left(1 + \frac{R_{f2}}{R_G}\right) - \left(\frac{R_{f2}}{R_G}\right) V_{in1} + V_{CM} \quad (3.15)$$

The op-amp's IA1 and IA2 outputs are given to the inverting and non-inverting terminals of the op-amp IA3 respectively and hence the differential input voltage to the op-amp IA3 is $V_{out2} - V_{out1}$.

$$V_{out2} - V_{out1} = \left[\left(1 + \frac{R_{f2}}{R_G}\right) V_{in2} - \left(\frac{R_{f2}}{R_G}\right) V_{in1} + V_{CM}\right] - \left[\left(1 + \frac{R_{f1}}{R_G}\right) V_{in1} - \left(\frac{R_{f1}}{R_G}\right) V_{in2} + V_{CM}\right]$$

$$= \left[\left(1 + \frac{R_{f2}}{R_G} + \frac{R_{f1}}{R_G} \right) V_{in2} - \left(1 + \frac{R_{f2}}{R_G} + \frac{R_{f1}}{R_G} \right) V_{in1} + V_{CM} - V_{CM} \right]$$

When $R_{f2} = R_{f1} = R$

$$V_{out2} - V_{out1} = \left(1 + \frac{2R}{R_G} \right) V_{in2} - \left(1 + \frac{2R}{R_G} \right) V_{in1}$$

The common mode voltages V_{CM} have cancelled each other since they are equal.

Therefore the output voltage of op-amp IA3 is

$$V_{out} = V_{out2} - V_{out1} = \left(1 + \frac{2R}{R_G} \right) (V_{in2} - V_{in1}) \quad (3.16)$$

The closed loop gain

$$A_{cl1} = \frac{V_{out}}{V_{in2} - V_{in1}} = 1 + \frac{2R}{R_G} \quad (3.17)$$

From the equation (3.17) the gain setting resistor RG value can be calculated as $R_G = \frac{2R}{A_{cl1}}$

It is explained as follows,

$$A_{cl1} - 1 = \frac{2R}{R_G}$$

$$R_G (A_{cl1} - 1) = 2R$$

$$R_G = \frac{2R}{A_{cl1}}$$

They are used in instances where good impedance matching and perfect signal amplification is required from noisy environments. One good example is human physiological signal measurement. As shown in figure 3.17, the ECG signal measurement devices use instrumentation amplifiers to pick up the low level output signal from the human heart.

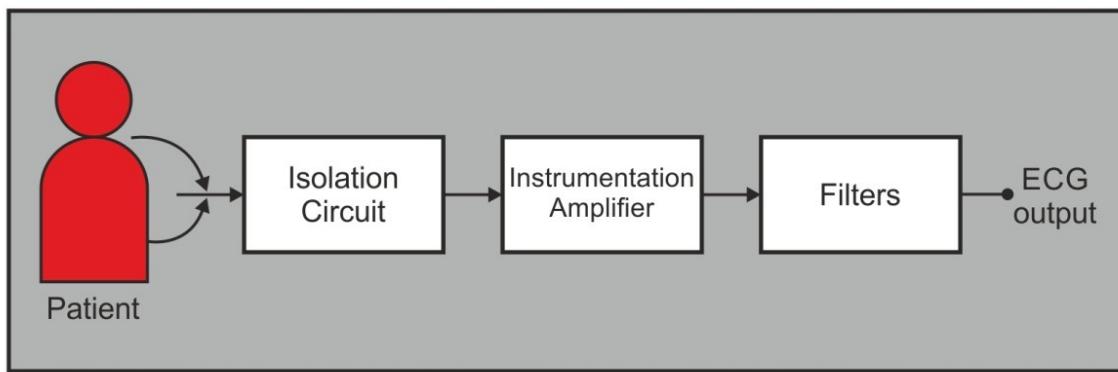


Fig 3.17 Instrumentation Amplifier in ECG Measurement

3.8 Differential Input and Differential Output Amplifiers

3.8.1 Differential Input Amplifier

Basically all inverting and non-inverting op-amps are considered as differential amplifiers due to their input connections. Since one of the input terminals is grounded in such configurations, the output voltage depends on the input signal and resistor combinations of another input terminal.

The figure 3.18 shows the exact differential amplifier which receives the input signal to both of its input terminals. The amplified output is the difference between the two input signals and hence is known as subtractor. By selecting the suitable values for external resistors the input signals can be adjusted and hence it is known as scaling amplifier. When the polarity of two input signals are opposite, it can be called as double-ended amplifier.

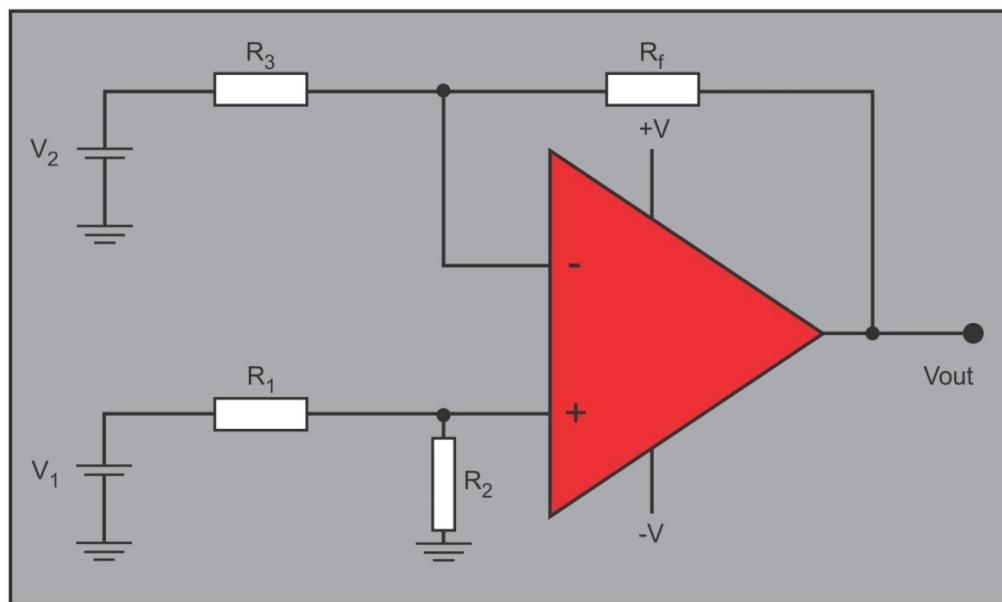


Fig 3.18 Differential input amplifier

The figure 3.18 also shows that it is a combination of inverting and non-inverting amplifier. When $V_2=0$, the circuit behaves as a non-inverting amplifier, the output voltage V_{out1} for input $V1$ according to the superposition theorem is

$$V_{out1} = V1 \left(\frac{R_2}{R_1+R_2} \right) \left(\frac{R_3 + R_f}{R_3} \right)$$

When $R_2 = R_f$ and $R_1=R_3$

$$V_{out1} = V1 \left(\frac{R_f}{R_3} \right) \quad (3.18)$$

Similarly when $V1=0$, the circuit behaves as an inverting amplifier and the output voltage V_{out2} for input $V2$ is

$$V_{out2} = V2 \left(-\frac{R_f}{R_3} \right) \quad (3.19)$$

Therefore the total output voltage i.e. the amplified difference between the two input voltages is

$$\begin{aligned}
 V_{out} &= V_{out1} + V_{out2} \\
 &= V1 \left(-\frac{R_f}{R_3} \right) + V2 \left(\frac{R_f}{R_3} \right) \\
 &= \left(\frac{R_f}{R_3} \right) (V2 - V1)
 \end{aligned}$$

Vout = (V2 - V1) when R_f=R₃ (3.20)

3.8.2 Differential Output Amplifier

The differential output amplifier is also known as integrated, fully –differential amplifier. Along with the inverting and non-inverting inputs, this amplifier has an additional input called V_{ocm} to control the output common mode voltage independent to the differential output voltage. The figure 3.19 shows the basic difference between standard differential and fully differential amplifier.

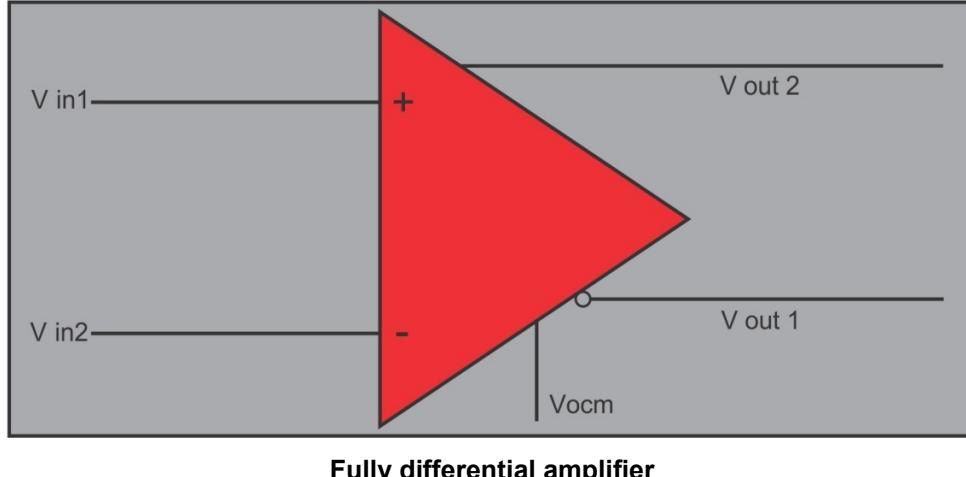
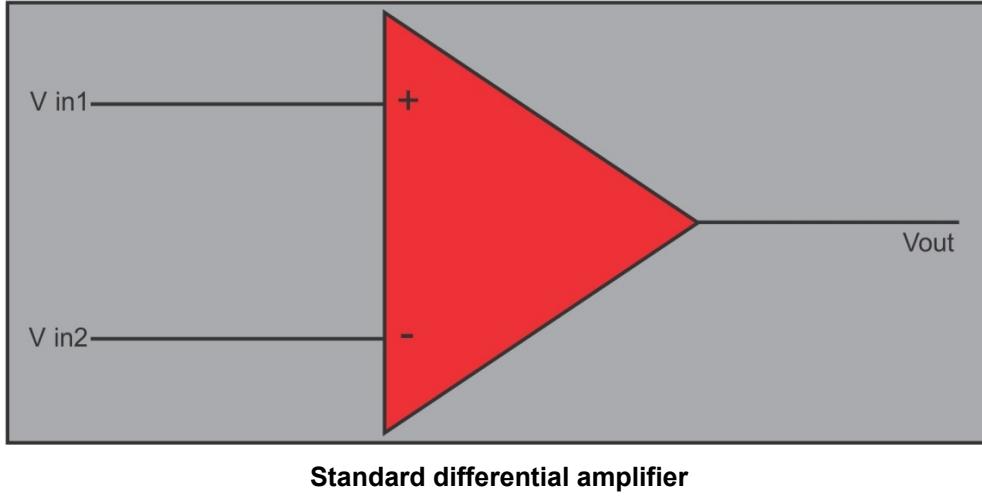


Fig 3.19 Difference between standard and fully differential amplifier

The fully differential amplifiers can also have multiple feedback paths rather than the single feedback path like standard differential amplifier.

The difference between the two input voltages V_{in1} and V_{in2} of the fully differential amplifier is known as input differential voltage V_{idiff} and is

$$V_{idiff} = V_{in2} - V_{in1} \quad (3.21)$$

The average of the two input voltages V_{in2} and V_{in1} is known as input common mode voltage V_{icomm} and is

$$V_{icomm} = \frac{V_{in2} + V_{in1}}{2} \quad (3.22)$$

The difference between the two output voltages V_{out2} and V_{out1} of the plus and minus output terminals is known as output differential voltage V_{odiff} and is

$$V_{odiff} = V_{out2} - V_{out1} \quad (3.23)$$

The average of the two output voltages V_{out2} and V_{out1} is known as output common mode voltage V_{ocomm} and is

$$V_{ocomm} = \frac{V_{out2} + V_{out1}}{2} \quad (3.24)$$

The output common mode voltage can be controlled by the voltage at V_{ocm} pin of the amplifier.

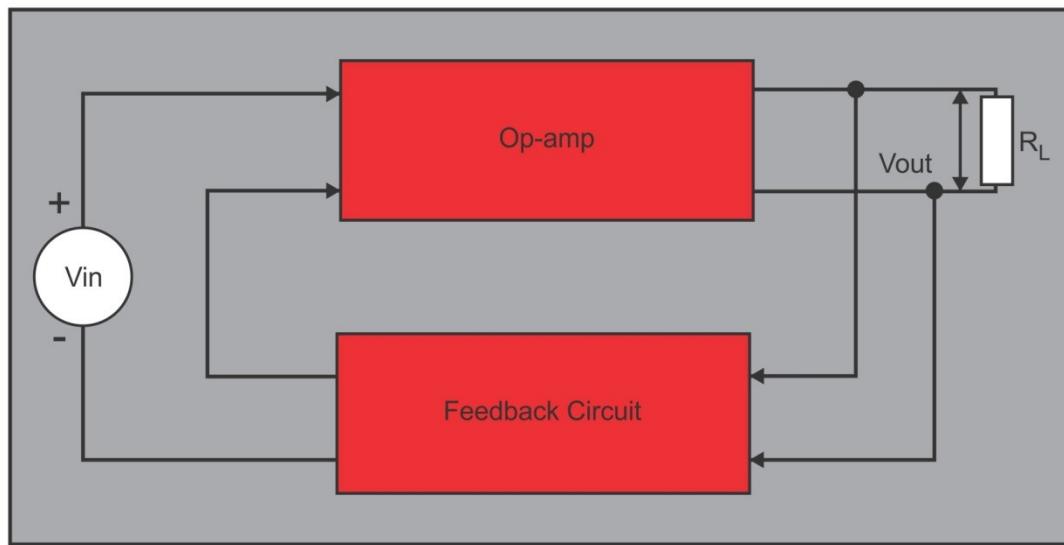
3.9 Feedback Amplifiers

Feedback means the output signal of the circuit is connected back to the input either directly or through any other network. Feedback signal may be in phase or out of phase with the input signal. When the feedback signal is in phase or has the same polarity as that of the input signal, the feedback system is called positive feedback. When the feedback signal is out of phase or has the opposite polarity compared to the input signal, the feedback system is called negative feedback. The negative feedback system is also called degenerative feedback and the positive feedback system is also called as regenerative feedback.

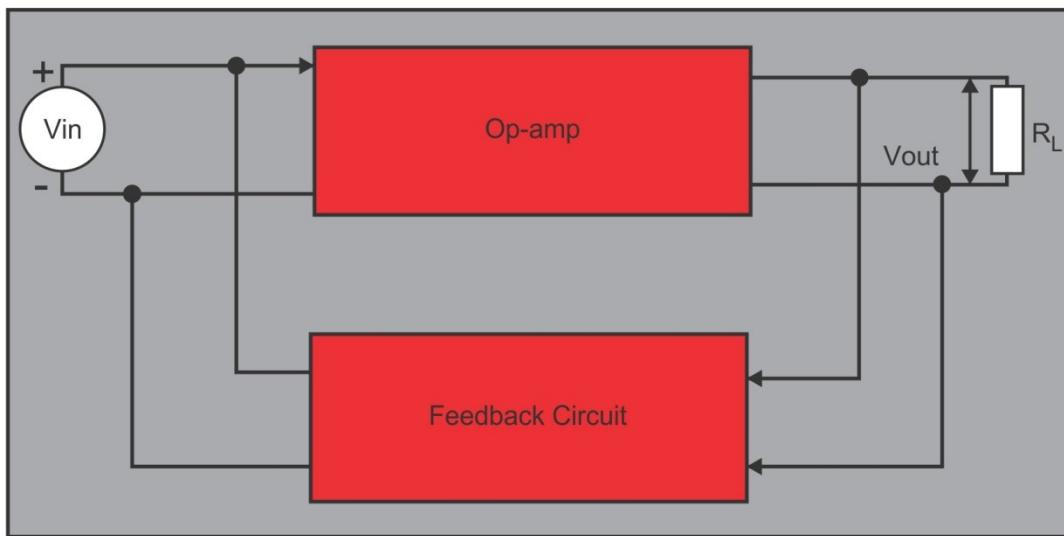
In general, oscillators always use positive feedback system and amplifiers use negative feedback system. In negative feedback system, the voltage gain of the amplifier is reduced but stabilized. The bandwidth of the output signal is increased and signal distortions reduced. This feedback amplifier is also called as closed loop amplifier and has two blocks such as op-amp and feedback circuit. The feedback circuit can be constructed using active components or passive components or else a combination of active and passive components. Based on the circuit configuration, the voltage or current can be fed back to the input of the amplifier from the output and have the following four possibilities exist.

- i. Voltage series feedback
- ii. Voltage shunt feedback
- iii. Current series feedback
- iv. Current shunt feedback

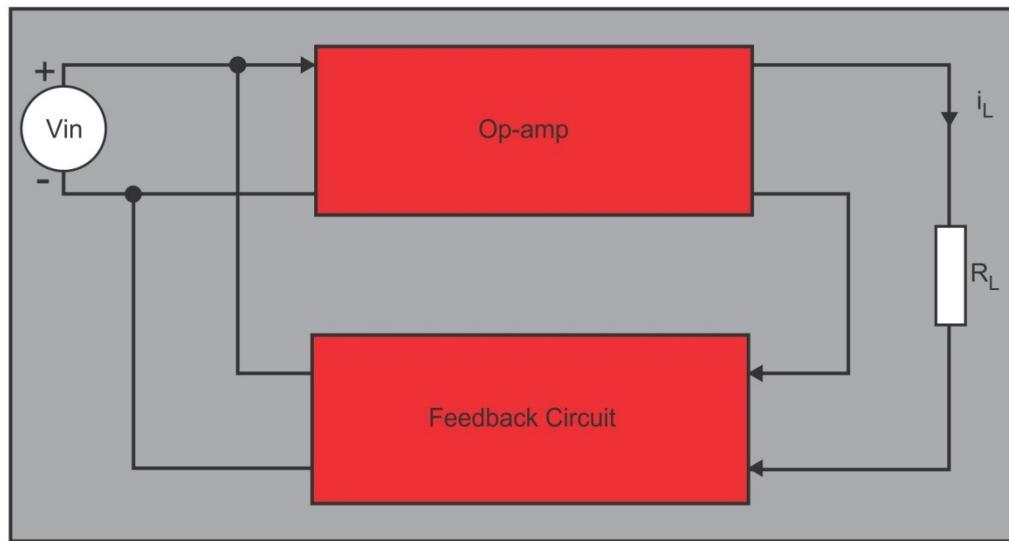
The figure 3.20 shows the four configurations of feedback system. In the figure 3.20 (a) and (b), voltage across the output load resistor R_L is the fed back to the input and in figure 3.20 (c) and (d) the load current i_L is directed in to the input section. Among these four configurations the voltage series and voltage shunt feedback systems are preferably followed for the applications.



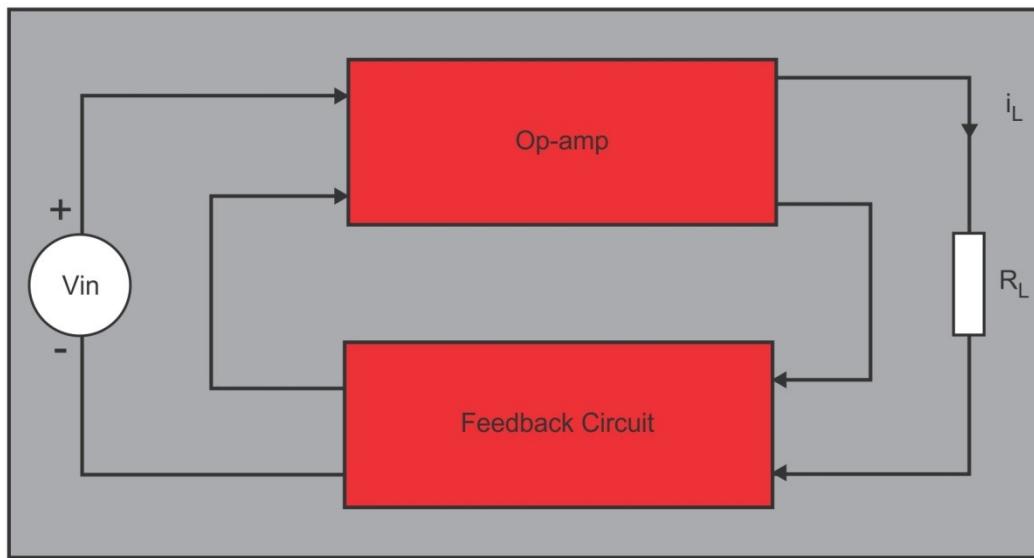
(a) Voltage series feedback



(b) Voltage shunt feedback



(c) Current shunt feedback



(d) Current series feedback

Fig.3.20 Feedback configurations

Feedback is effectively used in all types of amplifiers, including Audio frequency and Radio frequency amplifiers.

The process control system which uses the PID controller also uses the feedback mechanism. The wideband RF amplifiers are constructed using current feedback mechanism. The low frequency, but high gain amplification mechanism required for intermediate frequency (IF) amplifiers are constructed using voltage amplification system. IF amplifiers find application in television receivers.

3.9.1 Voltage series feedback amplifier

The figure 3.21 shows the circuit of a voltage series feedback amplifier. The circuit is designed using simple non-inverting amplifier with feedback network in inverting terminal. The feedback network is

composed with two resistors R_1 and R_f and the input voltage V_{in} is applied to the non-inverting terminal of op-amp.

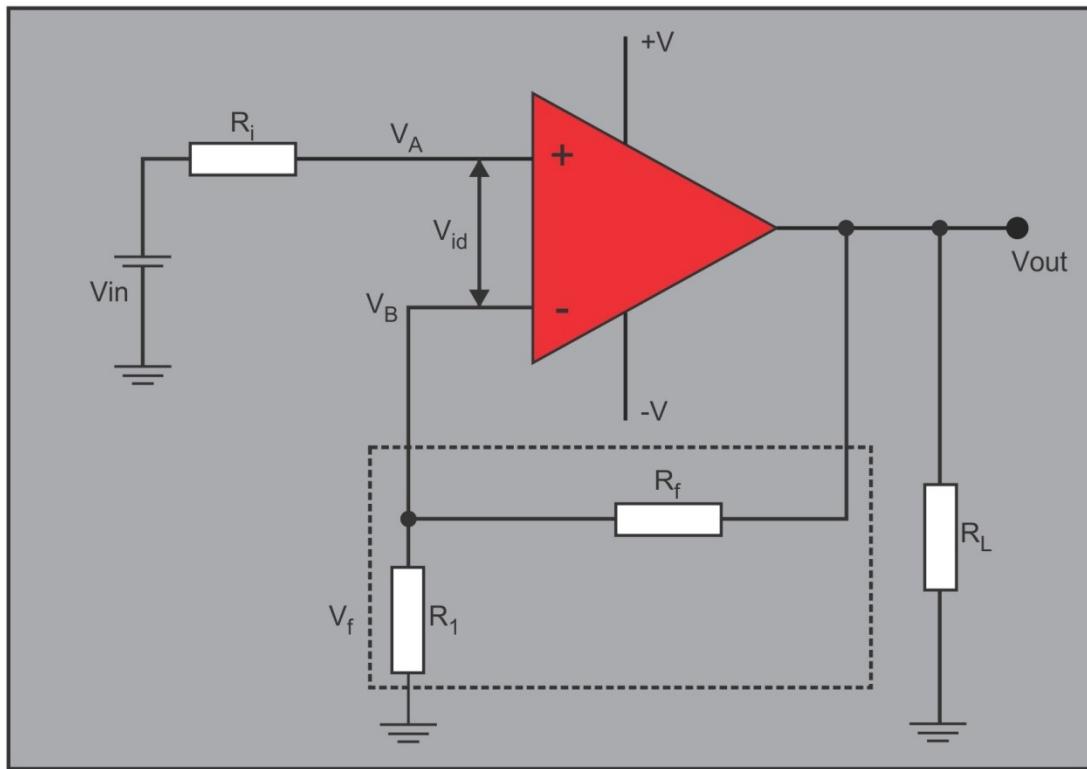


Fig.3.21. Voltage series feedback amplifier

Hence the feedback voltage V_f is applied to inverting terminal of op-amp. Therefore the differential input voltage V_{id} is amplified by the op-amp.

i.e.,

$$V_{id} = V_{in} - V_f$$

Where V_{id} = differential input voltage

V_{in} = Input voltage

V_f = Feedback voltage

Since the feedback signal V_f is 180° out of phase with the input signal V_i , circuit is said to be negative feedback amplifier.

The closed loop voltage gain of the circuit is $A_{cl} = V_{out} / V_{in}$

$$\text{But } V_{out} = A(V_A - V_B)$$

Since V_A is receiving input voltage V_i and V_B is receiving input voltage V_f , the V_A and V_B can be written as,

$$V_A = V_{in}$$

$$V_B = V_f$$

$$V_B = \frac{R_1}{R_1 + R_f} V_{out}$$

$$V_{out} = A (V_{in} - \frac{R_1}{R_1 + R_f} V_{out})$$

$$= A ((V_{in}(R1 + Rf) - R1V_{out}) / (R1 + Rf))$$

$$= A \frac{V_{in}(R1 + Rf)}{R1 + Rf} - \frac{AR1V_{out}}{R1 + Rf}$$

$$V_{out} \frac{AR1V_{out}}{R1 + Rf} = A \frac{V_{in}(R1 + Rf)}{R1 + Rf}$$

$$V_{out} (1 + \frac{AR1}{R1 + Rf}) = A \frac{V_{in}(R1 + Rf)}{R1 + Rf}$$

$$V_{out} = A \frac{V_{in}(R1 + Rf)}{R1 + Rf + AR1}$$

$$A_{CL} = \frac{v_{out}}{v_{in}}$$

$$A_{CL} = A \frac{(R1 + Rf)}{R1 + Rf + AR1} \quad (3.25)$$

Since $AR1 \gg R1 + Rf$ and $R1 + Rf + AR1 = AR1$

$$\text{AF} = \frac{v_{out}}{v_{in}}$$

$$= \frac{A(R1 + Rf)}{AR1} = \frac{AR1 + ARf}{AR1} = \frac{AR1}{AR1} + \frac{ARf}{AR1}$$

$$A_{CL} = 1 + \frac{R_f}{R_1} \quad (3.26)$$

The gain of the feedback circuit is considered as 'B' and can be written as

$$B = \frac{V_f}{V_{out}}$$

$$\text{Since } V_f = \frac{R_1}{R1 + Rf} \cdot V_{out}$$

$$B = \frac{R_1}{R1 + Rf} \quad (3.27)$$

Comparing equation 3.26 and 3.27

$$A_{CL} = \frac{1}{B} \quad (3.28)$$

Hence the gain of the feedback circuit is inversely proportional to the closed loop voltage gain of the circuit. Therefore, the closed loop gain A_{CL} is expressed using open loop gain A and feedback circuit gain B as Equation 1 is divided by $(R1 + Rf)$ both sides.

$$\begin{aligned} A_{CL} &= \frac{\frac{A(R1+RF)}{R1+RF}}{\frac{(R1+RF+AR1)}{R1+RF}} \\ &= \frac{A}{\frac{R1+RF}{R1+RF} + \frac{AR1}{R1+RF}} \\ &= \frac{A}{1 + \frac{AR1}{R1+RF}} \end{aligned}$$

$$\text{Since } \frac{R1}{R1 + RF} = B$$

$$A_{CL} = \frac{A}{1 + AB} \quad (3.29)$$

Where A_{CL} is closed loop voltage gain

A is the open loop voltage gain

B is gain of feedback circuit

The input resistance with feedback is

$$R_{iF} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\frac{V_{id}}{R_i}}$$

$$\text{Since } V_{id} = \frac{V_{out}}{A} \text{ and } V_{out} = \frac{A}{1 + AB} V_{in}$$

$$R_{iF} = R_i (1 + AB) \quad (3.30)$$

Therefore, the input resistance of the feedback amplifier is $(1+AB)$ times greater than of without feedback.

The output resistance of the feedback amplifier is

$$R_{OF} = \frac{R_o}{1+AB} \quad (3.31)$$

Therefore the output resistance of the feedback amplifier is $(\frac{1}{1+AB})$ times the output resistance R_o of the op-amp.

3.9.2 Voltage shunt feedback amplifier

Figure 3.22 shows the circuit of voltage shunt feedback amplifier.

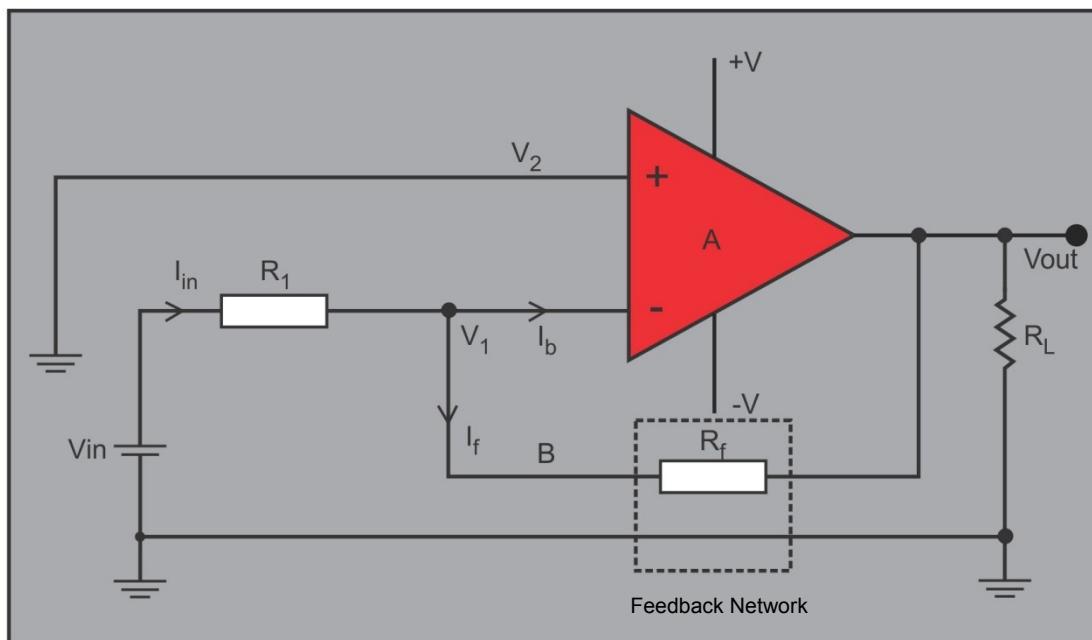


Fig.3.22 Voltage shunt feedback amplifier

The circuit is designed using an inverting amplifier. The input voltage V_{in} applied to the inverting terminal is amplified and applied to the input terminal back through the feedback resistor R_f . Since the feedback network has only one resistor ' R_f ', the circuit has one more resistor R_1 connected in the inverting terminal of operational amplifier.

The input current

$$I_{in} = I_F + I_B$$

The current I_b is very small since the input resistor R_1 is very large

Therefore, I_{in} can be

$$I_{in} \approx I_f$$

$$\text{Hence } \frac{V_{in}}{R_1} = \frac{V_1}{R_f} = \frac{1}{1+AB} \quad (3.32)$$

Therefore,

$$V_2 - V_1 = \frac{V_{out}}{A}$$

Where 'A' is gain

Since V_2 is 0V due to ground

$$V_1 = - \frac{V_{out}}{A} \quad (3.33)$$

Substituting equation (3.33) in (3.32),

$$\frac{V_{in} + \frac{V_{out}}{A}}{R_1} = \frac{-\left(\frac{V_{out}}{A}\right) - V_{out}}{R_f}$$

$$\frac{\frac{A V_{in} + V_{out}}{A}}{R_1} = \frac{\frac{-V_{out} - A V_{out}}{A}}{R_f}$$

$$\frac{A V_{in} + V_{out}}{A R_1} = \frac{-V_{out} - A V_{out}}{A R_f}$$

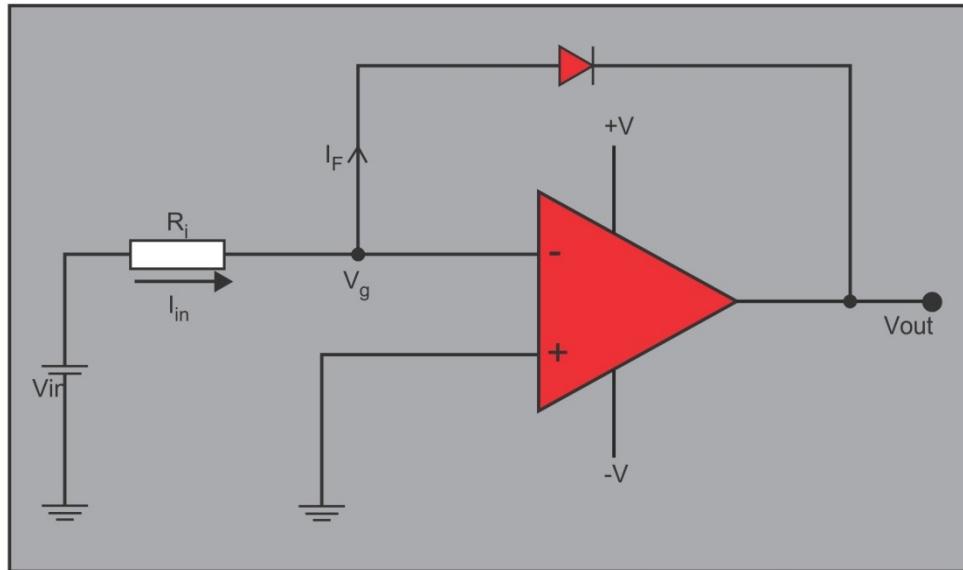
$$(A V_{in} + V_{out}) A R_f = (-V_{out} - A V_{out}) A R_1$$

$$\text{Therefore, feedback gain } A_f = \frac{V_{out}}{V_{in}} = -\frac{A R_f}{A R_1 + R_1 + R_f} \quad (3.34)$$

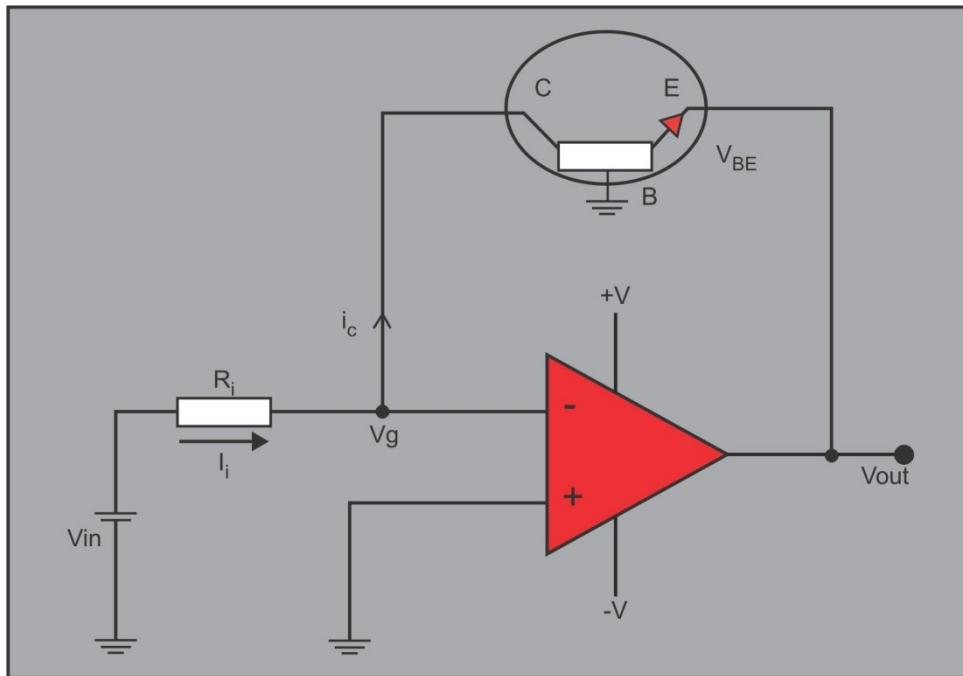
3.10 Log / Antilog Amplifiers

3.10.1 Log Amplifiers

Log amplifier means logarithmic amplifier. An amplifier whose output is proportional to logarithmic value of input is called a log amplifier.



(a) Log amplifier with feedback diode



(b) Log amplifier with transistor

Fig 3.23 Log Amplifier

Hence the op-amp based log amplifier feedback path must be connected with a component that exhibits logarithmic effect. Therefore, the feedback path of op-amp can be connected with a diode or transistor. The figure 3.23 a & b shows the log amplifier with feedback diode and transistor respectively.

In fig 3.23 (b), the collector of transistor is connected to virtual ground V_g of the transistor and base is also grounded. Therefore the transistor also behaves like a diode.

Let us consider the fig3.18 (a), the diode conducts for 0.7 V input i.e. V_F in forward biased characteristics and hence the current I_F flows through it which exhibits the non linear characteristics. This non linear curve is logarithmic in nature and hence the current I_F is represented as

$$I_F = I_R e^{qV_F / KT} \quad (3.35)$$

Where I_R = reverse leakage current

q = charge of an electron

K = Boltzmann's constant and

T = Absolute temperature in Kelvin

By taking natural logarithm on both sides of the equation 1, it can be written as

$$\begin{aligned} \ln I_F &= I_R e^{qV_F / KT} \\ &= \ln I_R + \ln e^{qV_F / KT} \\ &= \ln I_R + e^{qV_F / KT} \quad (\text{since } \ln(ab) = \ln a + \ln b) \\ \ln I_F - \ln I_R &= e^{qV_F / KT} \end{aligned}$$

Therefore $\ln(\frac{I_F}{I_R}) = e^{qV_F / KT}$ and

$$V_F = \left(\frac{KT}{q}\right) \ln\left(\frac{I_F}{I_R}\right) \quad (3.36)$$

Since the output voltage V_{out} is $-V_F$ when input is positive voltage and $I_F = I_i = (\frac{V_{in}}{R_i})$,

The equation 3.36 can be rewritten as

$$V_{out} = -\left(\frac{KT}{q}\right) \ln\left(\frac{V_{in}}{I_i R_i}\right) \quad (3.37)$$

The equation 3 shows that the output voltage of the circuit shown in figure 3.23 (a) is negative value of logarithmic function of input voltage.

In figure 3.23 (b), the voltage is V_{BE} and current is I_C ,

$$I_C = I_{EB} e^{qV_{BE} / KT} \quad (3.38)$$

Where I_{EB} = Emitter base leakage current

$$V_{out} = -\left(\frac{KT}{q}\right) \ln\left(\frac{V_{in}}{I_{EB} R_i}\right) \quad (3.39)$$

3.10.2 AntiLog Amplifier

The amplifier whose output is proportional to the exponential logarithmic value of input is called the antilog or anti logarithmic amplifier. To achieve the anti logarithmic form of output, the input of the op-amp can be connected with a transistor as shown in the figure 3.24.

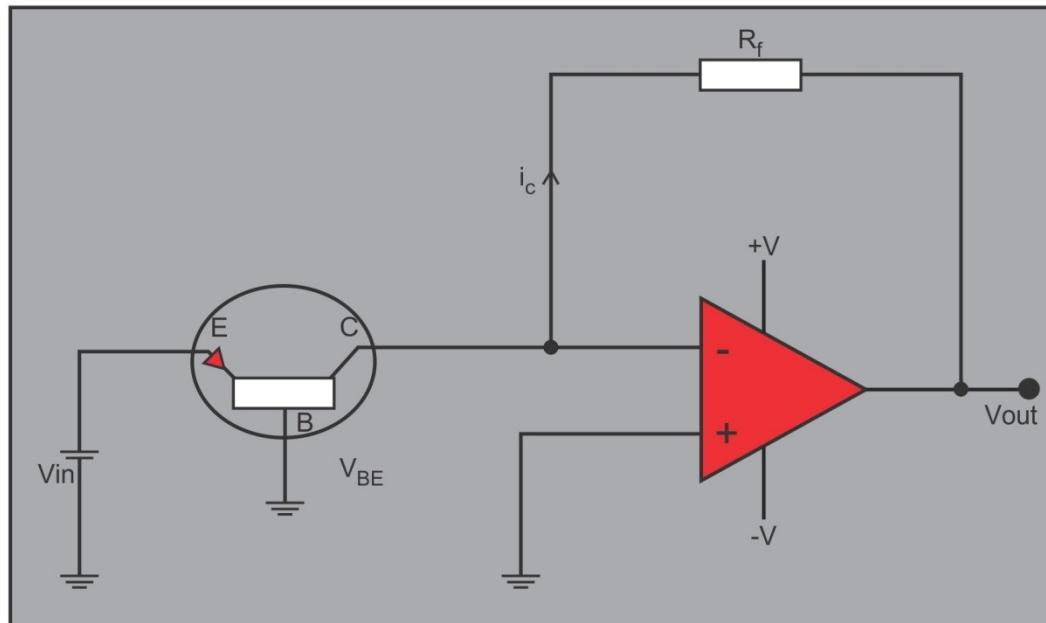


Fig.3.24. Anti log amplifier

According to Ohm's law the output voltage of the amplifier is

$$V_{out} = -R_f I_c$$

The current I_C characteristics curve of input transistor versus V_{BE} is

$$I_C = I_{EB} e^{qV_{BE}/KT}$$

$$V_{out} = -R_f I_{EB} e^{qV_{BE}/KT}$$

The exponential term is represented as anti logarithm and hence

$$V_{out} = -R_f I_{BE} \text{ antilog}(qV_{BE}/KT) \quad (3.40)$$

Since $V_{BE} = V_{in}$, equation (1) can be written as

$$V_{out} = -R_f I_{BE} \text{ antilog}(qV_{BE}/KT) \quad (3.41)$$

Most physical quantities such as optical signals are measured in wide range for the need, but they cannot be displayed in devices like multimeters. Hence, log amplifiers are used here to 'match' the systems. This means that the wide range of signals is compressed to match with the display systems. Log and Antilog amplifiers are also used in analog computations to improve computational speed. To get the real multiplied value of two log variables i.e. $\log A$ and $\log B$, it can be added together and given to the antilog amplifier. The resultant fastest multiplied answer is $A \times B$.

3.11 Isolation Amplifiers

An isolation amplifier is a device used between the input and output sections of the circuit to protect the life of the circuit components from harmful electrical signals due to leakage of power. The op-amp can act as an isolation amplifier and the figure 3.25 shows the basic circuit of an op-amp isolation amplifier:

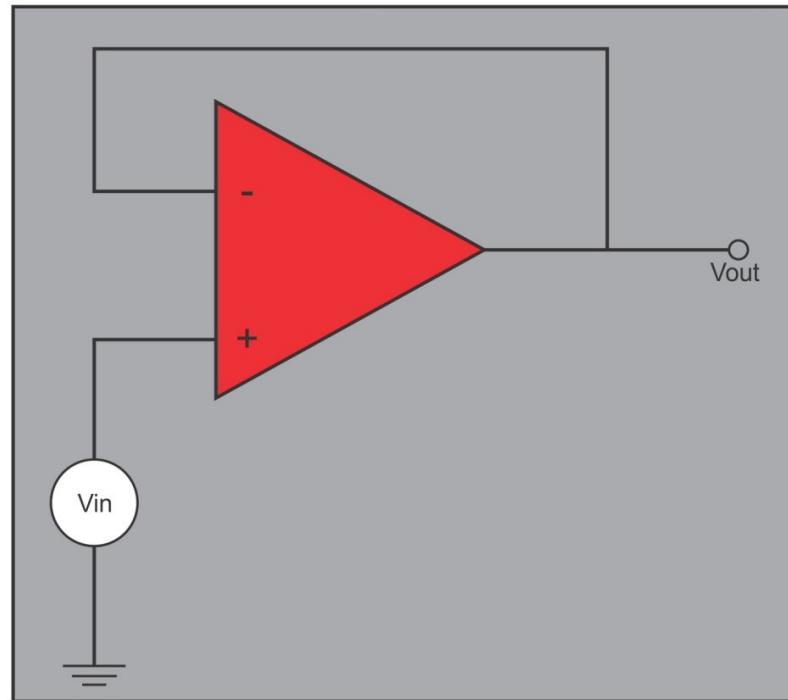


Fig 3.25 Op-amp isolation amplifier

Since the input impedance of a practical op-amp is very high, the current consumed from the input supply voltage is very less. Hence the output of the op-amp protects the circuit interfaced with the output side. The circuit in figure 3.25 is also called a Voltage follower since the total output voltage is fed back to the input. Since the gain of the circuit is 1, it is also referred to as a unity gain amplifier. Usually, the galvanic isolation principle is preferred since it prevents the current flow between the sections and protects equipment. Galvanic isolation technique also follows the isolated grounds for all sections in the circuit.

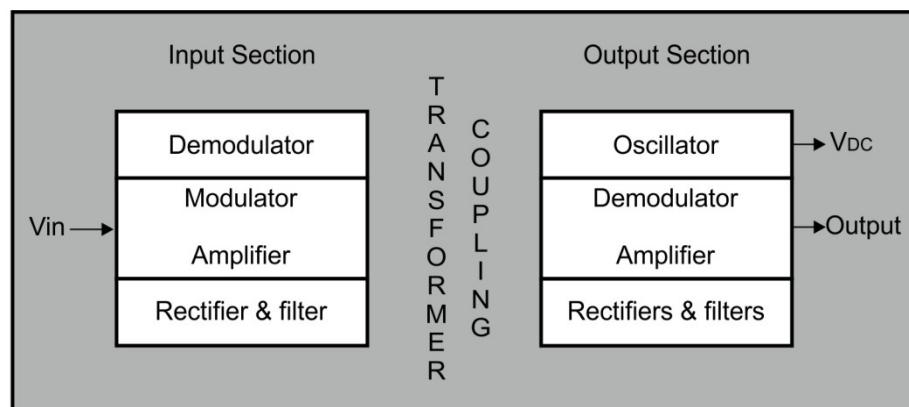


Fig.3.26 Transformer coupled isolation amplifier

The figure 3.26 shows the transformer coupled isolation amplifier. The isolation can also be achieved by using optical technique or capacitive technique. The circuit consists of an input section and output section and power supply sections. All the sections are also isolated from each other. The input, output and power supply sections of the amplifier are grounded independently.

The DC voltage VDC applied to the oscillator is converted into AC voltage since oscillator is a device used to convert DC into AC. The AC voltage is now converted into DC by the rectifier in the input and output sections and filtered for ripples since the sections are transformer coupled. Therefore the dual polarity DC voltage is generated for both the sections.

The output of the oscillator is also transformer coupled to modulator in the input section where this high frequency signal is modulated with the low frequency signal from the amplifier. The output of the modulator is demodulated by the demodulator in the output section due to transfer coupling. Therefore the real input signal is obtained in this section.

3.11.1 TI ISO 124 Precision Low Cost Isolation Amplifier

The chip ISO 124 is produced by Texas Instruments in the following two packages. The symbol of ISO 124 is shown in figure 3.27.

- i. **DIP- 16 package**
- ii. **SO- 28 plastic surface mount package**

This amplifier is used for many applications since it has advantages like

- **0.010% max non linearity**
- **Bipolar operation $\pm 10V$ (V_{out})**
- **50 KHz signal band width**
- **Power supply range of $\pm 4.5V$ to $\pm 18V$**
- **± 5.0 mA current on V_{S1} and**
- **± 5.5 mA current on V_{S2}**

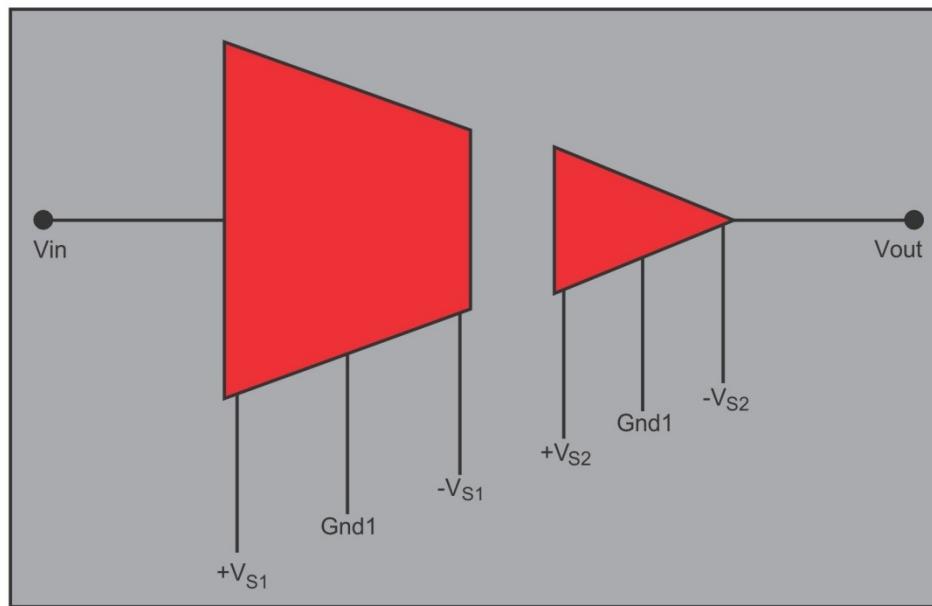


Fig.3.27 Symbol of ISO 124

Isolation amplifiers are effectively used in biomedical applications for patient's safety. To protect the patients from electrical hazardous and leakage currents, isolation amplifiers are used in between

patient's contact and patient monitoring systems as shown in figure 3.17. Isolation amplifiers are also employed in Watt – Hour meters.

3.12 Triangular/ Rectangulaer Wave Generator

The figure 3.28 (a) shows the basic triangular wave generator circuit whose output is same as the integrator circuit as shown in figure 3.28 (b)

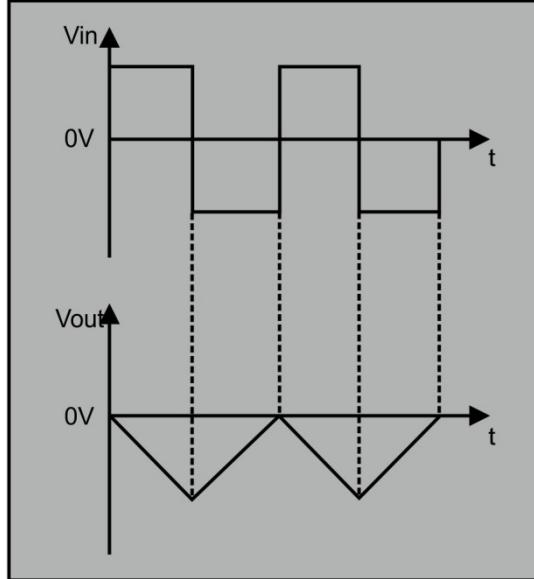
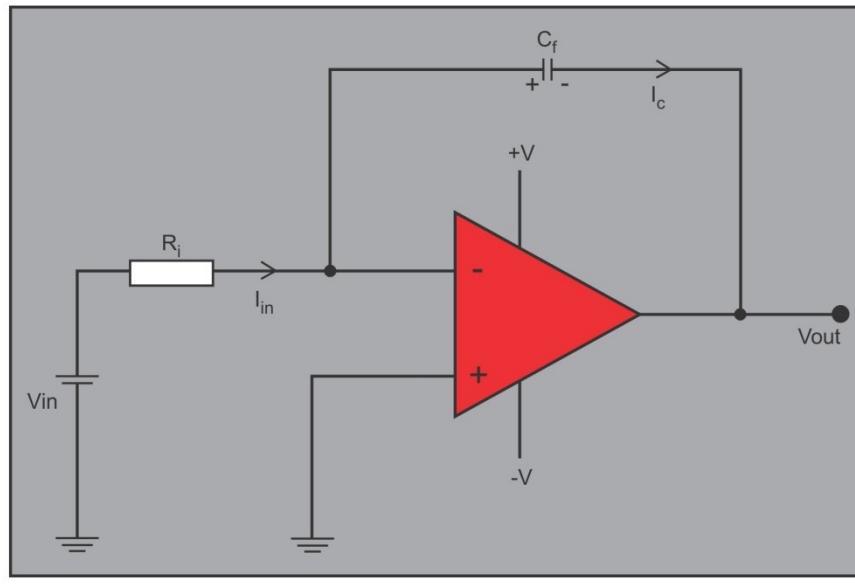


Fig.3.28 (a) Basic triangular wave generator (b) Input square and output triangular waveforms

When the input voltage of the circuit is positive, output is negative going ramp and vice versa. The practical triangular wave generator can be designed along with the op-amp comparator to produce the negative and positive input voltages. The figure 3.29 shows the practical triangular wave generator and its output waveform.

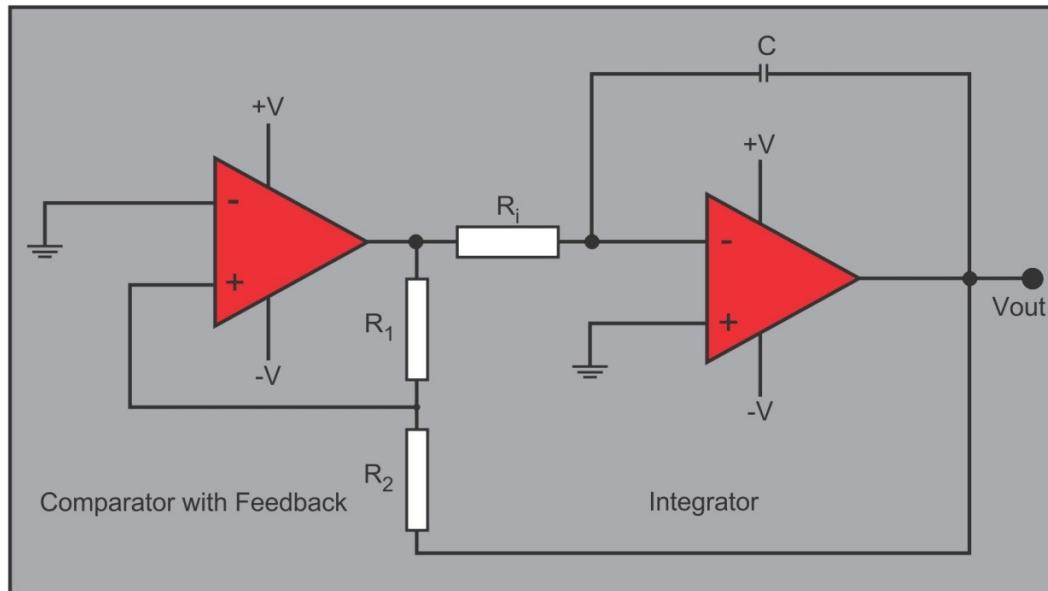


Fig.3.29 Practical triangular wave generator

Since the comparator produces the square wave output and integrator produces the triangular wave output, this circuit is also called as function generator.

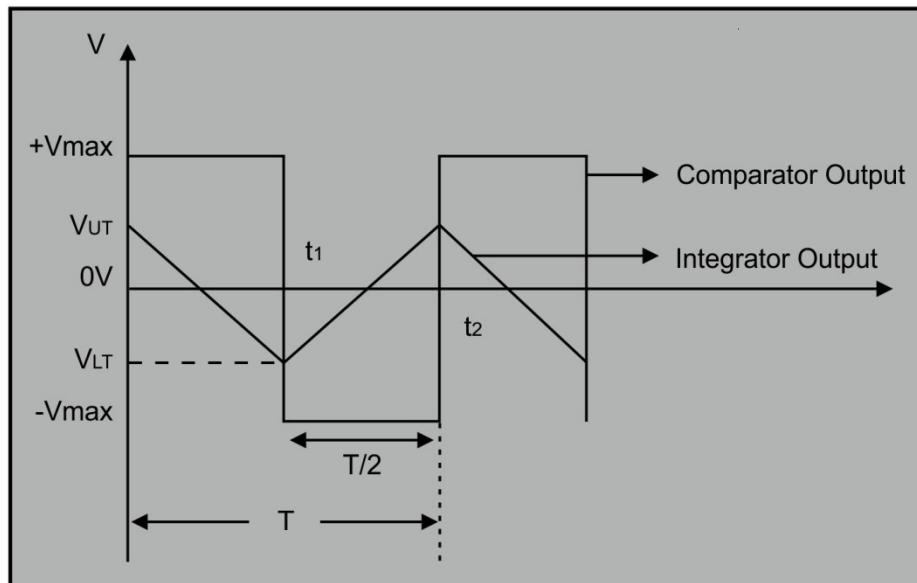


Fig.3.30 Triangular wave generator- output waveforms

The amplitude of the square wave output of the comparator is $\pm hV_{max}$ and the amplitude of triangular wave output of integrator is V_{UT} (upper threshold) and V_{LT} (lower threshold). The V_{UT} and V_{LT} depend on the resistors R_1 , R_2 and output voltage of the comparator.

$$V_{UT} = + V_{max} \left(\frac{R_2}{R_1} \right) \quad (3.42)$$

and

$$V_{LT} = -V_{max} \left(\frac{R_2}{R_1} \right) \quad (3.43)$$

At time t_1 , the negative going ramp reaches V_{LT} and the voltage at point TP is less than 0V. Hence the output of the comparator is shifted to $-V_{max}$. When comparator output is $-V_{max}$ output is positive going ramp as shown in figure 3.30.

At time t_2 , the positive going ramp reaches V_{UT} and the voltage at point TP is above 0V. Hence the output of the comparator is again shifted to $+V_{max}$.

When comparator output is $+V_{max}$, the integrator output is again negative going ramp as shown in the figure 3.30.

Therefore, when the comparator output is $+V_{max}$ output of integrator is negative going ramp and when the comparator output is $-V_{max}$, output of integrator is positive going ramp. Hence the triangular wave form is generated.

The output peak to peak voltage of integrator

$$\begin{aligned} V_{out}(PP) &= V_{UT} - V_{LT} \\ &= +V_{UT} - (-V_{UT}) \\ &= +V_{max} \left(\frac{R_2}{R_1} \right) - (-V_{max} \left(\frac{R_2}{R_1} \right)) \\ &= 2 V_{max} \left(\frac{R_2}{R_1} \right) \end{aligned} \quad (3.44)$$

The frequency of triangular wave form is same as square waveform and the frequency of oscillation 'f' depends on the R_iC time and resistors R_1 and R_2 . Hence 'f' is calculated as

$$f = \frac{1}{T} = \frac{1}{4R_iC} \left(\frac{R_1}{R_2} \right) \quad (3.45)$$

3.13 Oscillators

Oscillator is a circuit which can produce continuous wave form of constant amplitude and frequency without any external input signal.

The two general types of oscillators are

- i. Sinusoidal oscillator
- ii. Relaxation oscillator

Sinusoidal oscillator is constructed by amplifiers and RC combinations or amplifiers and LC combinations. The frequency of oscillation can be adjusted by these combinations.

Relaxation oscillators are constructed by op-amp and RC combinations to produce non-sinusoidal waveforms such as square, triangular, sawtooth etc.

The basic sinusoidal oscillator or sine wave oscillator is also called as feedback oscillator where the RC or LC combinations are feedback network. The positive feedback network transfers the portion of output voltage of the amplifier to the input with no phase shift as shown in the figure 3.31. It is also noted that in figure 3.31 A_v is the voltage of the amplifier and B is the transfer ratio. Therefore the feedback voltage is amplified and hence the signal is stabilized. This continuous sinusoidal output signal is called oscillation.

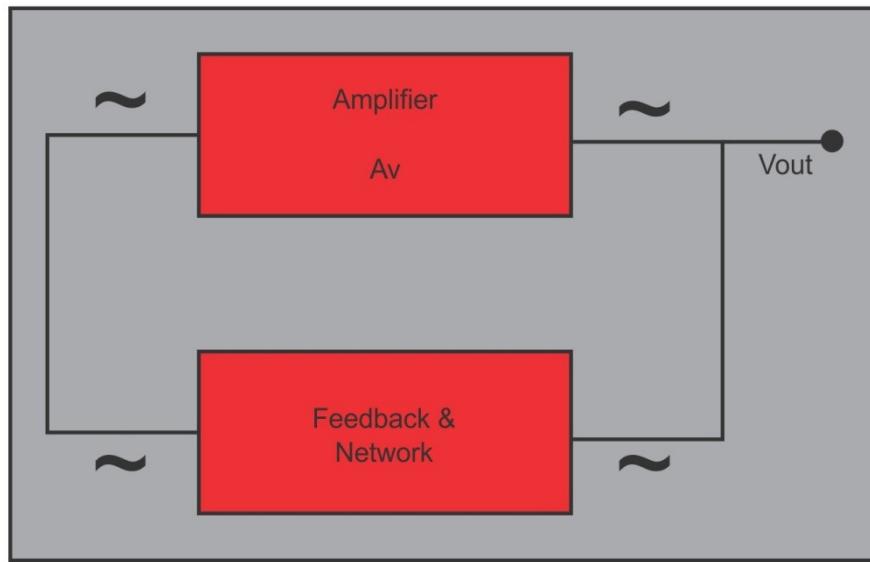


Fig 3.31 Feedback Oscillator

The following two conditions are to be satisfied to maintain the stabilized oscillation.

- (i) **The phase shift of the feedback network must be 0° .**
- (ii) **The closed loop voltage gain A_{cl} of the circuit must be equal to 1 or unity.**

$$\text{i.e., } A_{cl} = A_v \cdot B = 1$$

This is called Barkhausen criterion for oscillators. When A_{cl} is greater than 1, the output of the oscillator is distorted and is shown in figure 3.32.

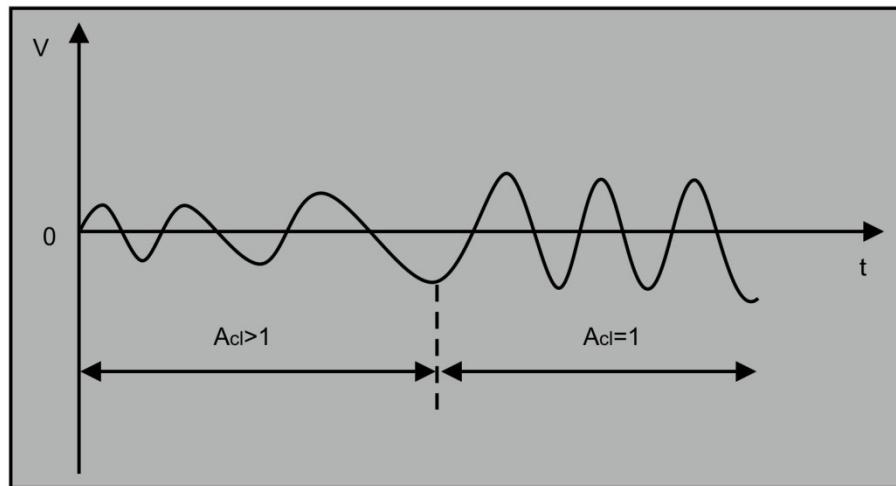


Fig 3.32 Oscillation for $A_{cl}>1$ and $A_{cl}=1$

Sinusoidal oscillators used in variety of applications which includes signal generators and oscilloscopes to produce frequency of oscillations. It is used in communication equipments like transmitters, computers to produce signals of required frequency.

Relaxation oscillators are used in horizontal deflection systems of television receivers to generate sawtooth waves or triangular waves. It is also used in function generators to produce square or triangular waves; oscilloscopes to produce saw tooth waves as well as in voltage controlled oscillators.

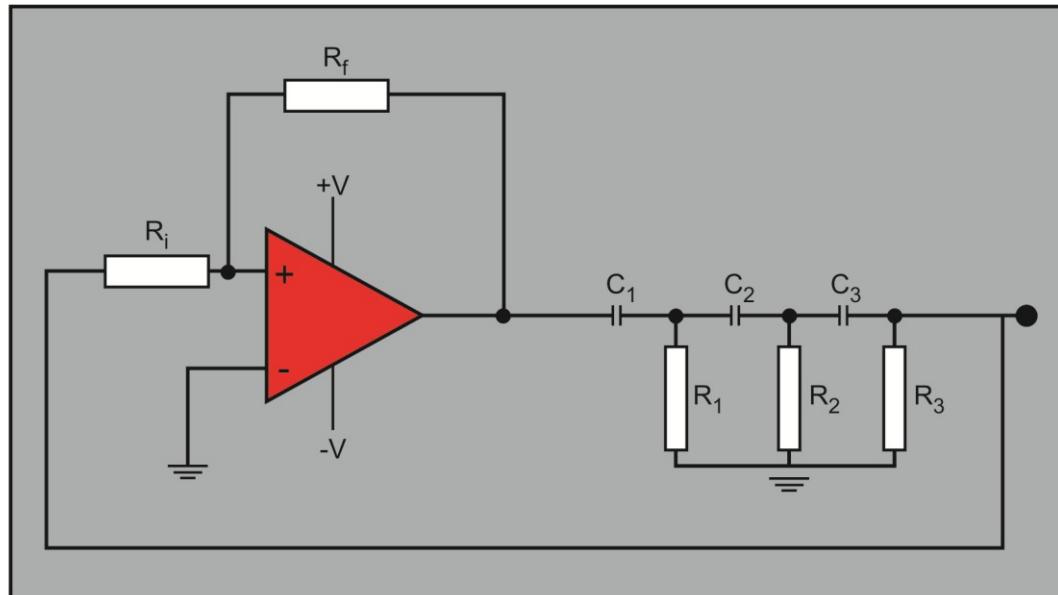


Fig 3.33 RC Phase Shift Oscillator

The input signal is given to the inverting terminal of the op-amp and hence the output is 180° phase shifted signal. But the feedback from the output to input should be the in-phase signal. Therefore the feedback circuit contributes 180° phase shift for the output signal of op-amp since each RC network shown in figure 3.34 provides 60° phase shift. Therefore the total phase shift of the circuit is 360° .

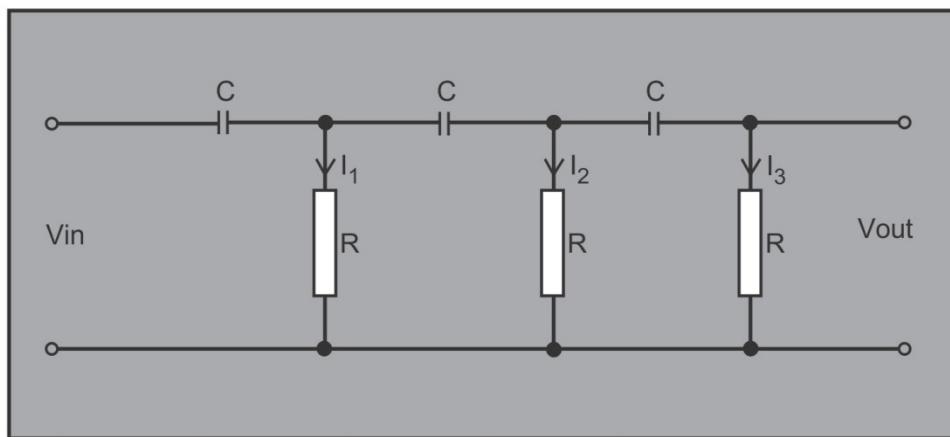


Fig.3.34 RC feedback network

All resistors and capacitors in the feedback network are equal in values and

$$\text{Let } 2R - \frac{j}{2\pi f c} = A$$

$$\text{Then } R - \frac{j}{2\pi f c} = A - R$$

$$(A - R)I_1 - RI_2 + 0I_3 = V_{in}$$

$$-RI_1 + AI_2 - RI_3 = 0$$

$$0I_1 - RI_2 + AI_3 = 0$$

Using Crammers rule

$$\Delta = \begin{vmatrix} A - R & -R & 0 \\ -R & A & -R \\ 0 & -R & A \end{vmatrix} = (A - R)[A^2 - R^2] + [-RA]$$

$$= A^3 - AR^2 - A^2R + R^3 - R^2A$$

$$\Delta = A^3 - 2AR^2 - A^2R + R^3$$

$$\Delta_{I_3} = \begin{vmatrix} A - R & -R & V_{in} \\ -R & A & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$\Delta_{I_3} = V_{in}R^2$$

$$I_3 = \frac{\Delta_{I_3}}{\Delta}$$

$$I_3 = \frac{V_{in}R^2}{A^3 - 2AR^2 - A^2R + R^3}$$

$$\frac{RI_3}{V_{in}} = \frac{R^3}{A^3 - 2AR^2 - A^2R + R^3}$$

$$= \frac{R^3}{\left(2R - \frac{j}{2\pi f c}\right)^3 - 2\left(2R - \frac{j}{2\pi f c}\right)R^2 - \left(2R - \frac{j}{2\pi f c}\right)^2 R + R^3}$$

Equating j term to zero

$$\frac{6R^2}{2\pi f c} - \frac{1}{8\pi^3 f^3 c^3} = 0$$

$$\frac{3R^2}{\pi f c} = \frac{1}{8\pi^3 f^3 c^3}$$

$$\frac{3R^2}{1} = \frac{1}{8\pi^2 f^2 c^2}$$

$$f^2 = \frac{1}{24 \pi^2 C^2 R^2}$$

$$f = \sqrt{\frac{1}{24 \pi^2 C^2 R^2}}$$

$$f_r = \frac{1}{2\pi R C \sqrt{6}} \quad (3.46)$$

$$\begin{aligned}
 \frac{V_{out}}{V_{in}} &= \frac{R^3}{R^3 - \frac{5R}{(\frac{1}{6R^2})}} \\
 &= \frac{R^3}{R^3 - 30R^3} \\
 \frac{V_{out}}{V_{in}} &= -\frac{1}{29} \tag{3.47}
 \end{aligned}$$

Therefore the attenuation factor of the feedback network, $B = 1/29$, where $B = R_3/R_f$. ' f_r ' is called the frequency of oscillation. The negative sign in the gain V_{out}/V_{in} is due to the 180° phase shift and for the gain greater than unity, closed loop voltage gain of the op-amp must be greater than 29.

3.13.2 Weinbridge Oscillator

The figure 3.35 shows the weinbridge oscillator circuit in which the input signal is given to the non-inverting terminal of the operational amplifier. Therefore the output signal of the circuit is 0° phase shift i.e. in phase signal and hence the feedback network does not require to produce phase shift like phase shift oscillator. Figure 3.36 shows the weinbridge circuit in between the inverting and non-inverting terminal of the operational amplifier. Out of four arms, one arm of the bridge has series RC network (i.e.) R & C , another arm has parallel combination of R_1 and C_1 and the other two arms are connected with resistors (i.e.) R_2 and R_3 . When the bridge is balanced, the circuit achieves 0° phase shift condition.

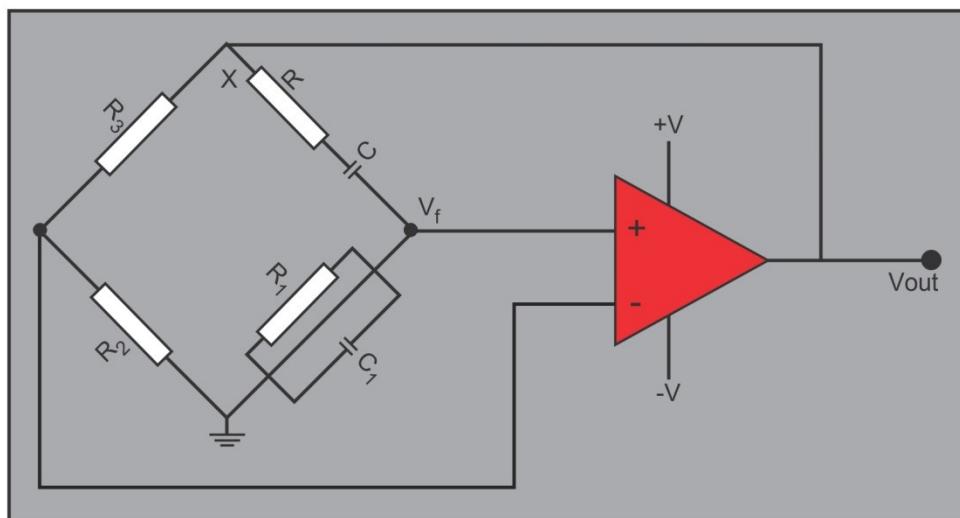


Fig 3.35 OP-amp wein bridge oscillator

The circuit shown in figure 3.35 is redrawn in figure 3.36. It is clearly shown that the inverting terminal of the op-amp is converted to voltage divider network and the non-inverting terminal of the op-amp is connected to lead lag circuit. The lead lag circuit has a resonant frequency f_r or f_0 , where the phase shift through the circuit is 0° .

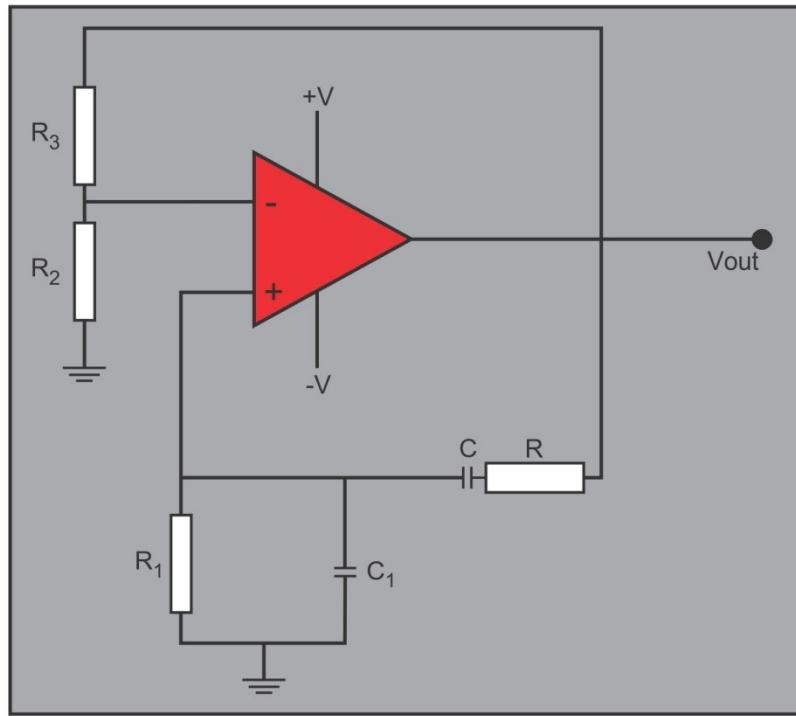


Fig.3.36 Wein bridge oscillator- Lead lag configuration

The output signal of the amplifier is feedback to the point X in the figure 3.35, and the attenuation factor of the circuit is 1/3 i.e., $V_{\text{out}}/V_{\text{in}} = 1/3$. The resonant frequency f_r is calculated as Let $R_1 = R_2 = R$

$$\begin{aligned} C_1 &= C_2 = C \\ Z_1 &= \frac{SRC + 1}{SC} \\ Z_1 &= \frac{j\omega RC + 1}{j\omega C} \end{aligned} \tag{3.48}$$

$$\begin{aligned} Z_2 &= \frac{R}{1 + SRC} \\ Z_2 &= \frac{R}{1 + j\omega RC} \end{aligned} \tag{3.49}$$

$$\beta = \frac{Z_2}{Z_1 + Z_2}$$

Put value of 3.48, and 3.49 in $\beta = \frac{Z_2}{Z_1 + Z_2}$ equating real and imaginary parts

$$\omega = \frac{1}{RC}$$

$$f = \frac{1}{2\pi RC}$$

At the frequency f, the gain A_V required for stable (or) sustained oscillation is $A_V = \frac{1}{\beta} = 3$

$$1 + \frac{R_3}{R_2} = 3$$

$$1 + R_3 = 3R_2$$

$$R_3 = 3R_2 - 1$$

$$R_3 = 2R_2$$

$$R_3 = R_f \text{ and } R_2 = R_a$$

$$\text{Therefore } R_f = 2R_a$$

To achieve the gain 3 for sustained oscillation the value of R_a should be twice the value of R_f . It is used in radio receivers since it is an audio frequency oscillator.

3.14 Analog Multiplier

An analog multiplier is a circuit which produces the output voltage equal to the product of two input voltages. The figure 3.37 shows the basic block of an analog multiplier which has two inputs V_A and V_B and output V_{out} .

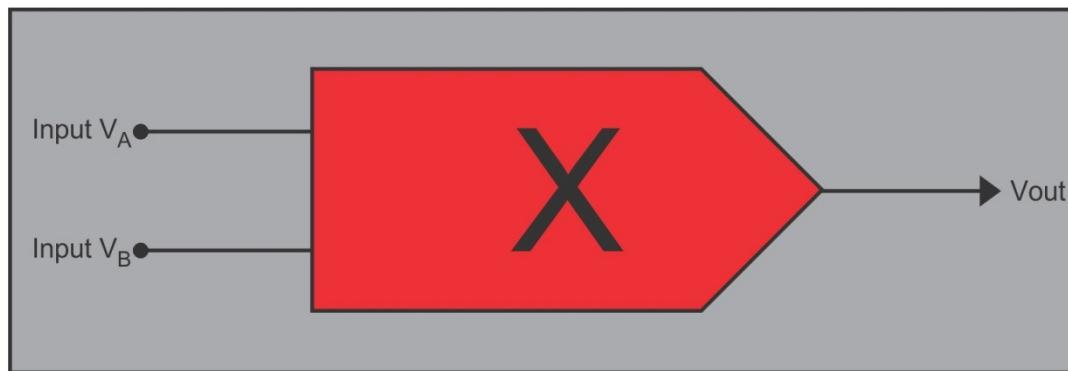


Fig.3.37 Basic building block of an Analog amplifier

V_{out} is the product of V_A and V_B and can be written as

$$V_{out} = k * V_A * V_B \quad (3.50)$$

Where 'k' is the scale factor and is equal to 1/10 V. This means that the input voltage V_A (or) V_B must not exceed +10 V or -10 V with respect to ground. Therefore the output voltage of the analog multiplier is the scaled product of the two input voltages. Hence the output expression can be rewritten as

$$V_{out} = \frac{V_A * V_B}{10 V} \quad (3.51)$$

The multiplier are classified as one quadrant, two quadrant, three quadrant and four quadrant multipliers based on the following conditions.

- i. **If the two input voltages V_A and V_B are positive, the multiplier is called as one quadrant multiplier,**

$$\text{Therefore, } V_{out} = \frac{V_A * V_B}{10} \quad (3.52)$$

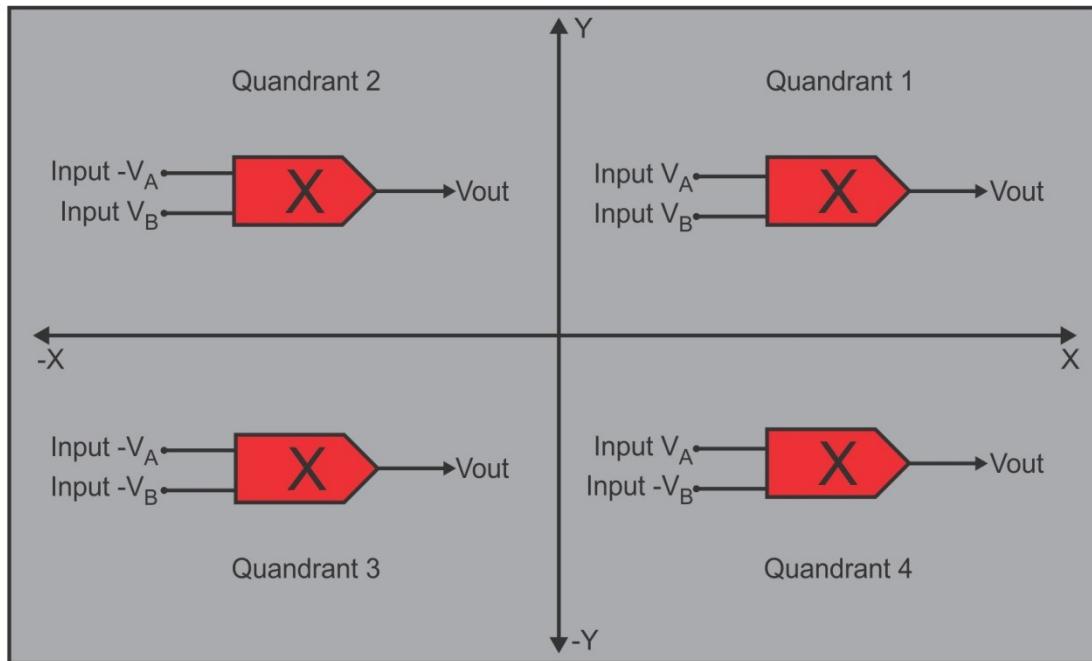


Fig.3.38 Quadrant multiplier

- ii. Similarly, if the input voltage V_A is positive and V_B is negative, the multiplier is called as four quadrant multiplier since V_A lies in x axis and V_B lies in $-y$ axis as shown in figure 3.38.

$$\text{Therefore } V_{out} = \frac{-V_A * V_B}{10} \quad (3.53)$$

- iii. For $-V_A$ and V_B ,

$$V_{out} = \frac{-V_A * V_B}{10} \quad (3.54)$$

- iv. And the multiplier is two quadrants as shown in figure 3.38.
For $-V_A$ and $-V_B$,

$$V_{out} = \frac{V_A * V_B}{10} \quad (3.55)$$

And the multiplier is three quadrants as shown in figure 3.38.

The multipliers are used for the applications such as frequency doubling, frequency shifting, power measurement, phase angle difference between the two signals, multiplying two signals, squaring the input signal, modulation and demodulation etc.

3.14.1 TI MPY 634 Wide bandwidth precision Analog Multiplier

Figure 3.39 shows the block diagram of MPY 634 analog multiplier.

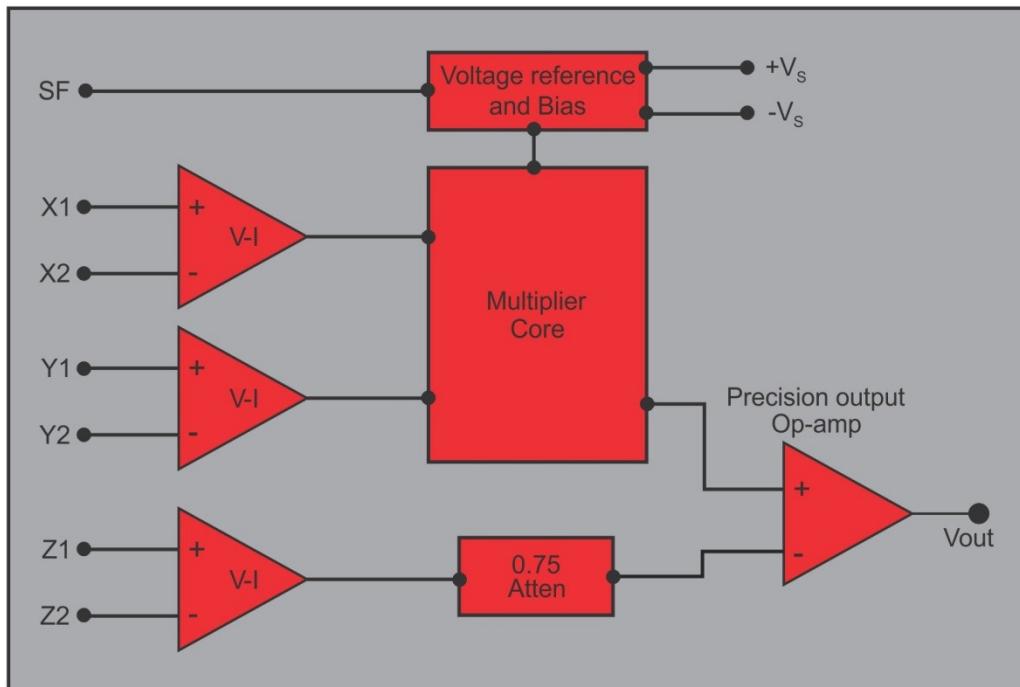


Fig.3.39 Block diagram of MPY 634 analog multiplier

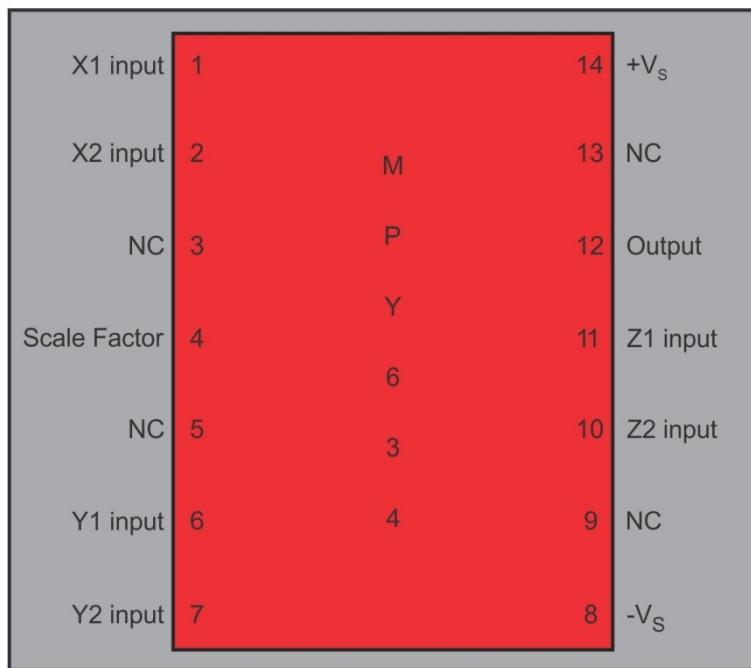


Fig.3.40 Pin diagram of MPY 634 Analog Multiplier

The MPY 634 analog multiplier from Texas Instruments is a four quadrant analog multiplier. This multiplier chip can also be used as a squarer, divider, square rooter, etc.,

The figure 3.40 shows the pin configuration of MPY 634 KP.

The output voltage V_{out} is,

$$V_{out} = A \left[\left((X_1 - X_2) * \frac{Y_1 - Y_2}{SF} \right) - (Z_1 - Z_2) \right] \quad (3.56)$$

Where A is an open loop gain of the output amplifier, SF is a scale factor and X, Y and Z are input voltages.

The scale factor is factory adjusted to 10V by connecting the potentiometer or resistor between the pins SF and $-V_s$, the scale factor can be varied and the resistance is calculated as,

$$R_{SF} = 5.4k\Omega \frac{SF}{10 - SF} \quad (3.57)$$

Therefore the full scale input voltage is equal to the selected SF value.

The MPY 634 provides high accuracy output with wide band width and the band width is not affected by the SF adjustment.

The supply voltage V_s is $\pm 15V$, but the operation is possible below $\pm 8V$ with the reduced input and output voltage ranges. V_s above $\pm 15V$ leads to greater output swing using output feedback attenuator.

Figure 3.41 shows the basic multiplier connection

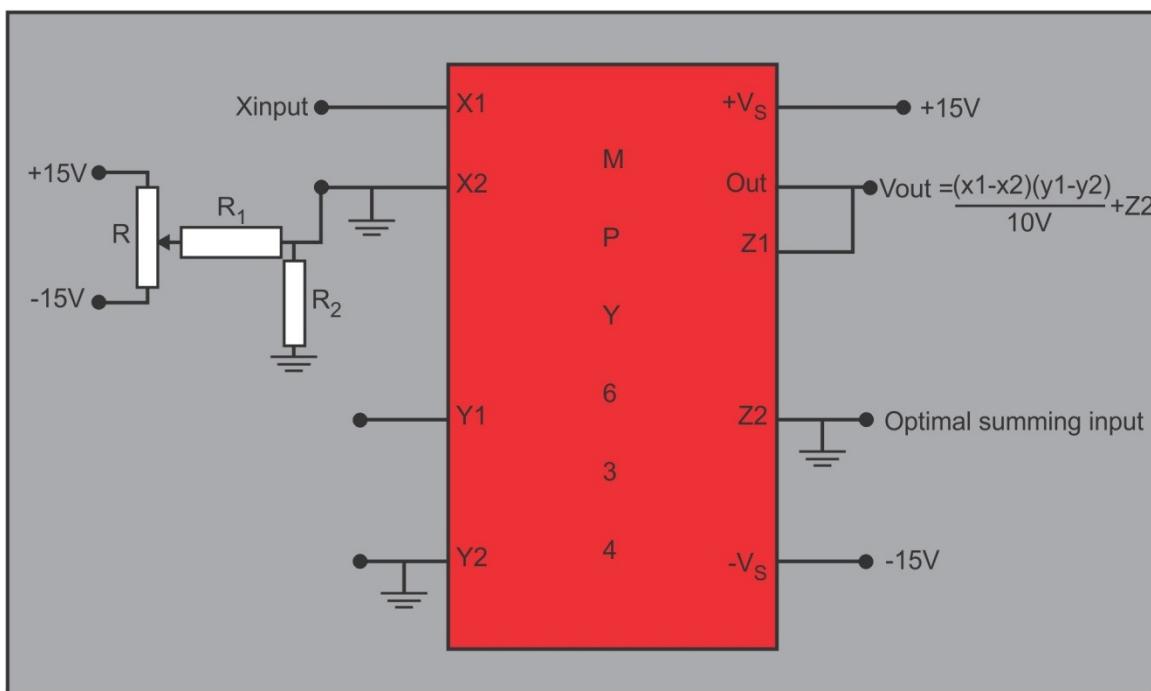


Fig.3.41 Basic Multiplier

The X2 input of the circuit is connected with offset voltage trimming circuitry which is required for some specific applications, but the accuracy of the circuit can be achieved without the additional trimming circuit. The trimming circuit can be used with one (or) more input. The differential Z input allows the offset to sum up with V_{out} and Z_2 serves as an output voltage ground reference. The output quantity is directly converted into current due to the flexibility of differential Z inputs. Due to internal output amplifier, the design complexity is reduced.

Analog multipliers are used to construct voltage controlled oscillators. It is also used in automatic gain control circuit shown in figure 3.42. The electronic volume control circuit is also employing the Analog Multiplier. It is also effectively used in analog computation systems, Watt Meters, Watt – Hour meters, Densitometers etc.

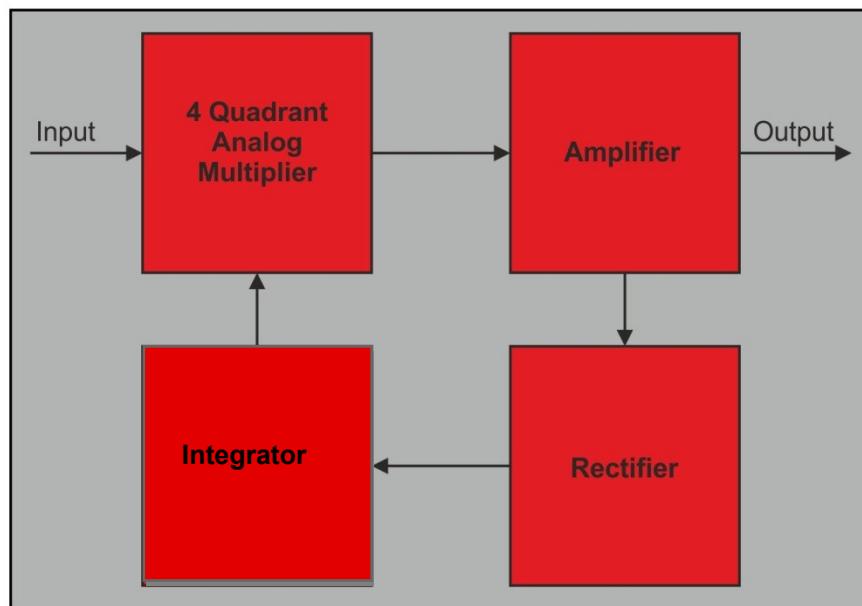


Fig.3.42 Analog Multiplier and Integrator in Automatic Gain Control

3.15 Voltage Controlled Oscillator: (VCO)

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. The voltage controlled oscillator is also called a voltage to frequency converter since the output frequency of the oscillator is controlled by the input voltage. VCO is an important analog circuit as it is used in FSK/FM generation and constitutes the modular part of MODEM. It is also used as a basic building block in PLL. It can also be used as reference oscillator for a Class D amplifier. IC form of voltage controlled oscillator (VCO) is also available and VCO can also be designed using op-amp. The VCO may be sinusoidal or non-sinusoidal. It can be designed to produce the sawtooth wave and is called voltage controlled sawtooth oscillator.

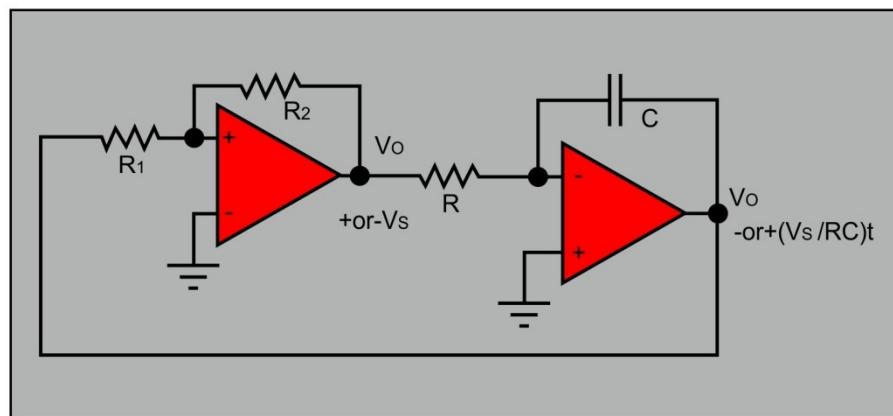


Fig.3.43 Function Generator

The function generator produces a square wave at the Schmitt Trigger output and a triangular wave at the integrator output.

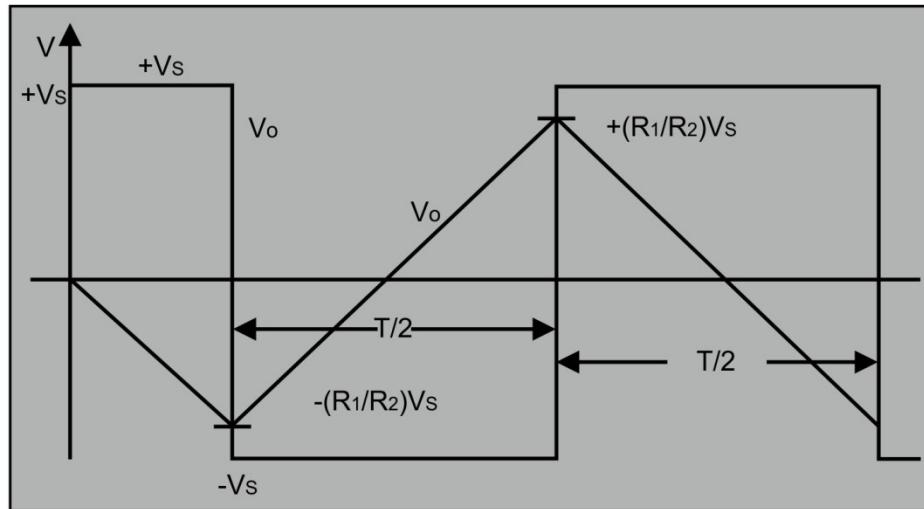


Fig.3.44. Function generator output

The frequency of oscillation is given by:

$$f = \frac{1}{4RC} \frac{R_2}{R_1}$$

Now if to this function generator we integrate an analog multiplier, it gives rise to a very important application called Voltage controlled oscillator(VCO). Further this can be used to build a Phase Locked Loop system (discussed in Chapter 6). The figure below shows how a function generator is converted into VCO by introducing a multiplier block, where one input of multiplier is given through integrator and other input is given externally in terms of voltage. The frequency of oscillation of such VCO can be controlled by external voltage called controlled voltage.

The Schmitt trigger is a regenerative circuit whose output can be only +/- Vs. Hence if this is fed as one of the input to multiplier, the output of multiplier after multiplying with control voltage Vc will be + or - (Vs Vc/10), where 10 is the reference or scaling factor of multiplier. This voltage will further either charge or discharge the capacitor depending on the potential and generating the slope accordingly concluding a triangular waveform.

The frequency of oscillation of the VCO becomes:

$$f' = \frac{V_c \cdot R_2}{4 \cdot RC \cdot V_r \cdot R_1}$$

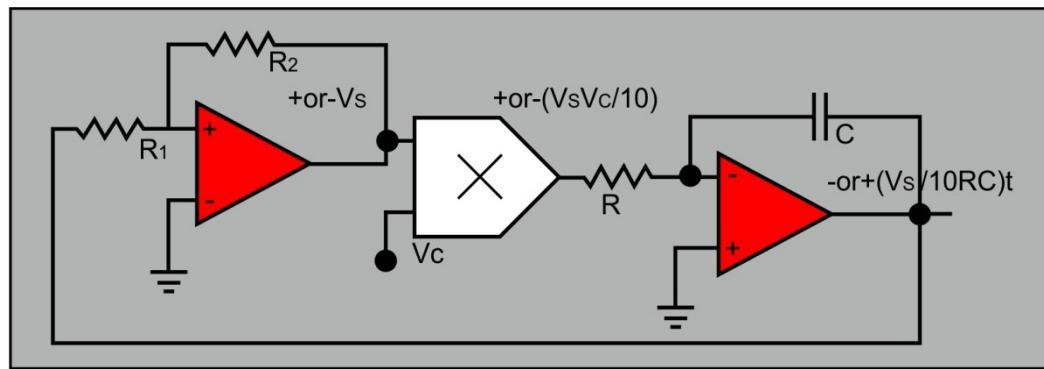


Fig 3.45 Voltage Controlled Oscillator(VCO)

Sensitivity of VCO is the important parameter and is given as Kvco and given by:

$$K_{VCO} = \frac{df'}{dV_c} = \frac{R_2}{4RC \cdot V_r V_1} = \frac{f}{V_c} \text{ Hz/Volts}$$

Active Filters

The previous chapter (Chapter 3) covered the study of amplifiers and oscillators including their functions and application. This chapter seeks to introduce readers to another important component of an electronic circuit – active filters. This chapter covers the description and classification of all types of filters; construction of Butterworth low-pass, high pass and band-pass active filters using Operational amplifiers as well as analysis and design of simple active filters.

At the end of this chapter, readers will be equipped to measure output frequency response of low-pass and high-pass band pass filters; modify filter circuit components to meet design specifications; construct active filter circuits using electronic design software and design and simulate band reject filters and all pass filters. The chapter also covers the need for self-tuned filter and its design.

Topic	Page
4.1 Introduction	123
4.2. Characteristics of Filters	125
4.3. Classification of Filters	126
4.4. Magnitude and Frequency response	127
4.5. Fundamentals of Low-Pass Filters	128
4.6 Butterworth Low-Pass Filters	129
4.7. High-Pass Filter Design	138
4.8. Band-Pass Filter Design	144
4.9. Characteristics of Chebyshev Low-Pass Filters	150
4.10. Band-Rejection Filter Design	152
4.11 All-Pass Filter Design	159
4.12 Self -tuned Filters	164
4.13 Summary	171
4.14 Review Questions	172
4.15 Exercises	175

4.1 Introduction

A filter is basically a circuit, which performs selection of frequency by removing unwanted components or features from a transmitted signal. Most often, this refers to the removal of certain frequencies rather than suppression of interfering signals or reduction of background noise.

Filters alter the amplitude and/or phase characteristics of an electrical signal with respect to its frequency. Since filters use resistors, inductors, or capacitor networks (RLC) within their design, there is an important relationship between the use of these reactive components and the circuit's frequency response characteristics.

Filters are essential to the operation of most electronic circuits. They are commonly used in high-performance stereo systems, where certain ranges of audio frequencies need to be amplified or suppressed for best sound quality and power efficiency. Some great examples of filters are equalizer and crossover networks, which are designed to accomplish filtering of certain frequencies.

Applications of filters

- (i) In Public addressing audio systems, engineers use these filters in crossover networks to send different frequencies to different speakers. In music industry, record and playback applications require control of frequency components.
- (ii) In communication Systems, active filters are used to suppress noise, to isolate single communication from many channels, to avoid spillover of adjacent bands and to recover the original message signal from modulated signal.
- (iii) In instrumentation systems, engineers use filters to select a desired frequency component and remove undesired ones. We can use these filters to limit the bandwidth of analog signals before converting them to digital signals. You also need these signals to convert digital signals back to analog signals.
- (iv) In biomedical systems, these filters are used to interface psychological sensors with data logging and diagnostic equipments

As an example of filter application consider a Public Addressing system. A public address system is an electronic sound amplification and distribution system with a microphone, mixer, amplifier, Equalizer and loudspeakers, used to allow a person to address a large public.

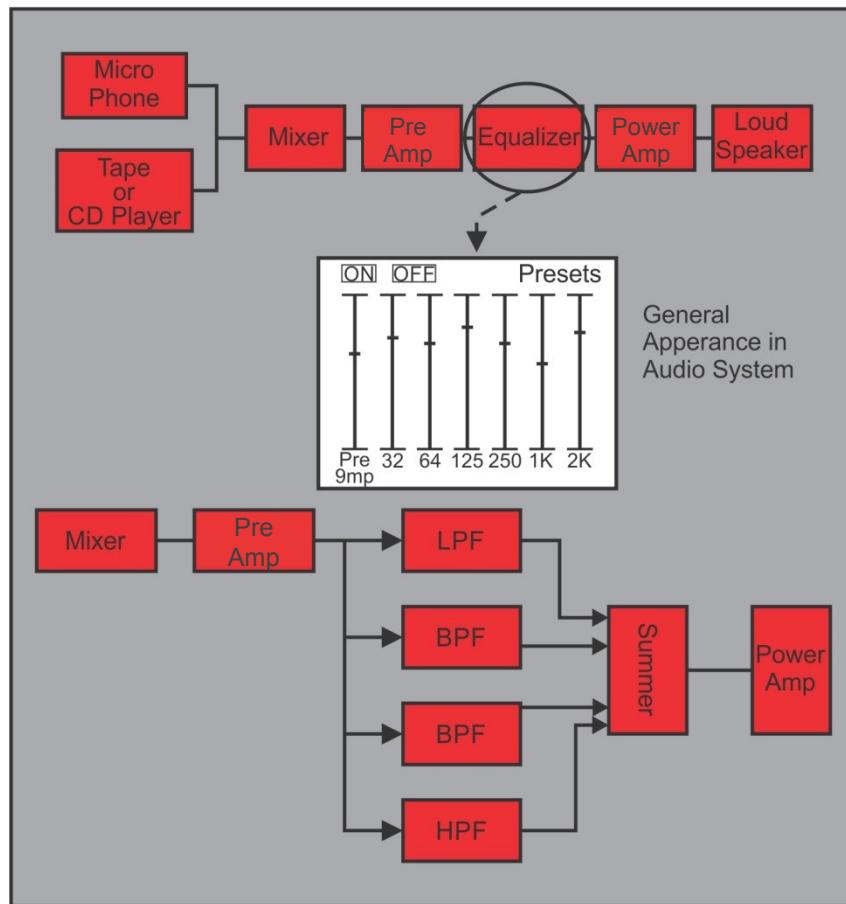


Fig. 4.1 Public Address System

A sound source such as compact disc player or radio may be connected to a PA system so that music can be played through the system. The process begins with a sound source (such as a human voice), which creates waves of sound (acoustical energy). These waves are detected by a microphone, which converts them to electrical energy. This signal is amplified in an amplifier up to a required level. Then Mixer is the device that controls how the input signals are routed to various signal processors and output devices (loudspeakers) connected to the system. Then Filters are used to modify the tone of a signal. Filters are the core components of equalizers. There are two common types of equalizers used in a PA system. Equalizers have many fixed-frequency bands, usually with a bank of faders to boost or reduce each band by a specified amount. These are typically used on any signal that is being sent to an output device (loudspeaker) in a sound system. Equalization at this stage compensates for the frequency response of the speakers and the acoustic response of the room. This signal is amplified in an amplifier up to a required level .Finally the loudspeaker converts the electrical signal back into sound waves, which are heard by human ears.

Filters are classified according to the functions that they are to perform, in terms of ranges of frequencies.

An active filter is a type of analog electronic filter that uses active components such as an amplifier. Amplifiers included in a filter design can be used to improve the performance and predictability of a

filter, while avoiding the need for inductors (which are typically expensive compared to other components). An amplifier prevents the load impedance of the following stage from affecting the characteristics of the filter.

4.2. Characteristics of Filters

Filters are networks that process signals in a frequency-dependent manner. The basic concept of a filter can be explained by determining the frequency dependent nature of the impedance of capacitors and inductors. The frequency response is defined as the mechanism that yields the frequency dependent change in the input/output transfer function.

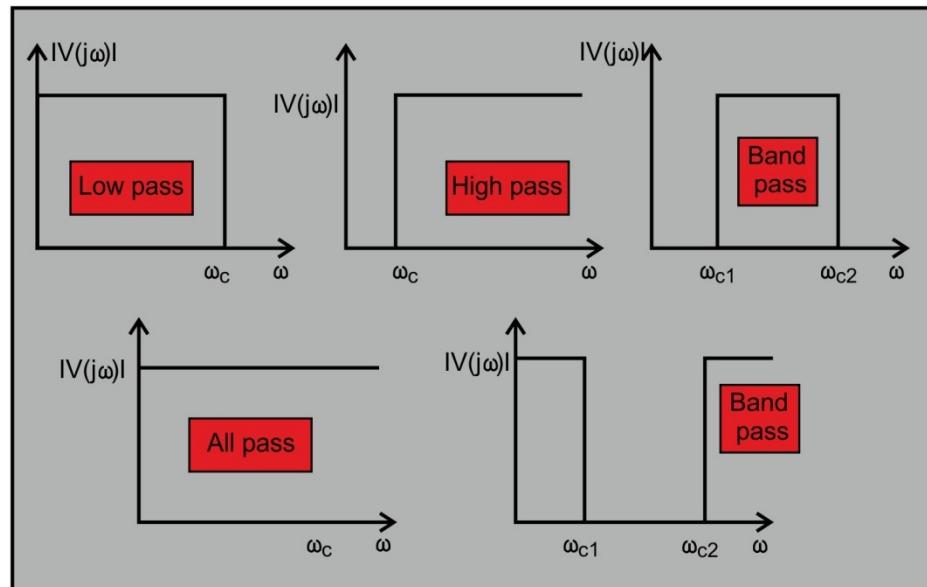


Fig. 4.2 Desired or Ideal frequency response of different filters

An ideal filter is a network that allows certain frequency signals to pass and blocks others. The passband is the frequency range that passes through the filter. The stopband is the range of frequency that filter attenuates. The gain of an ideal filter is one (0 dB) in the passband, so the amplitude of the signal neither increases nor decreases. In practical applications, ideal filters are not realizable.

4.2.1. Filter parameters

Cutoff frequency is the frequency beyond which the filter does not allow any signal to pass. It is usually measured at a specific attenuation such as 3dB. Roll-off is the rate at which attenuation increases beyond the cut-off frequency.

Transition band is the (usually narrow) band of frequencies between a passband and stopband. The variation in the filter's amplitude in passband is referred as Passband ripple and the variation in the filter's amplitude in stop band stop band ripple. The order of a filter is the degree of the approximating polynomial and in passive filters it corresponds to the number of elements required to build it. Increasing order increases roll-off and brings the filter closer to the ideal response. The equivalent design parameter to the filter order n is quality factor Q.

4.3. Classification of Filters

Filters can also be classified as passive and active filters. Passive filters are circuits that use only passive components like resistors, capacitors, and inductors while active filters are circuits that use an op-amp as the active device along with some resistors and capacitors.

The frequency response can be classified into a number of band forms describing which frequency bands the filter passes (the pass band) and which it rejects (the stop band):

- **Low-pass filter** – low frequencies are passed, high frequencies are attenuated.
- **High-pass filter** – high frequencies are passed, low frequencies are attenuated.
- **Band-pass filter** – only frequencies in a frequency band are passed.
- **Band-stop filter or band-reject filter** – only frequencies in a frequency band are attenuated.
- **Notch filter** – rejects just one specific frequency - an extreme band-stop filter.
- **All-pass filter** – all frequencies are passed, but the phase of the output is modified.

Filters are specified by family and bandform. A filter's family is specified by the approximating polynomial used and each leads to certain characteristics of the transfer function of the filter. Some common filter families and their particular characteristics are:

- **Butterworth filter** – no gain ripple in pass band and stop band, slow cutoff
- **Chebyshev filter (Type I)** – no gain ripple in stop band, moderate cutoff
- **Chebyshev filter (Type II)** – no gain ripple in pass band, moderate cutoff
- **Bessel filter** – no group delay ripple, no gain ripple in both bands, slow gain cutoff
- **Elliptic filter** – gain ripple in pass and stop band, fast cutoff

4.4. Magnitude and Frequency response

The characteristic of a filter is described by its frequency response which consists of both a magnitude and a phase response. The Magnitude response describes the gain of a filter at every frequency. A positive gain boosts the signal while a negative gain attenuates the signal. Phase response is determined by the ratio of the peak output amplitude to the peak input amplitude at a particular. A frequency response describes how the amplitude and phase of a sound's spectral components are changed by the filter. The magnitude and phase response are plotted versus frequency as shown in figure 4.3.

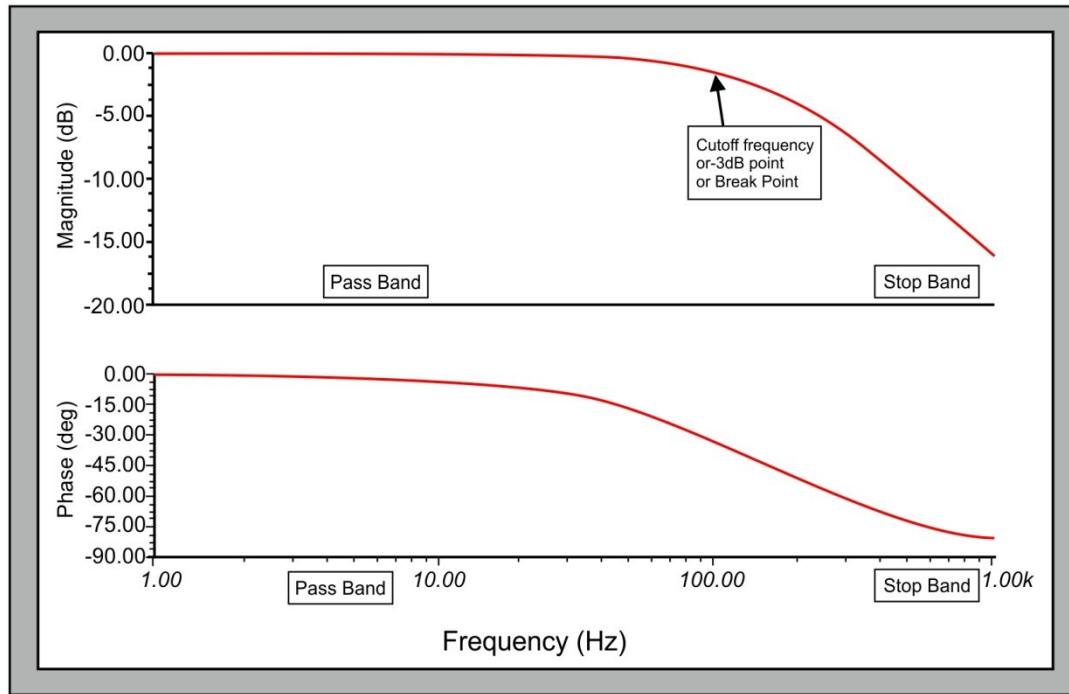


Fig 4.3 Magnitude and Phase response of Low pass filter

4.4.1. Phase Response

Each pole of a filter will add 45° of phase shift at the corner frequency. The phase varies from 0° (well below the corner frequency) to 90° (well beyond the corner frequency). The start of the change can be more than a decade away. In multipole filters, each pole will add phase shift, so that the total phase shift will be multiplied by the number of poles (180° total shift for a two pole system, 270° for a three pole system, etc).

The phase response of a single pole, low pass filter is:

$$\phi(w) = -\arctan \frac{w}{w_0} \quad (4.1)$$

4.4.2. Impulse Response

The impulse function is defined as an infinitely high, infinitely narrow pulse, with an area of unity. The impulse response of a filter in the time domain is proportional to the bandwidth of the filter in the frequency domain. For the narrow impulse, the bandwidth of the filter will be wide .The impulse

response also increases with increasing filter order. Higher filter order implies greater band limiting, therefore degraded time response.

4.4.3. Step Response

The step response of a filter is the integral of the impulse response. Many of the generalities of impulse response are applicable to the step response. The slope of the rise time of the step response is same as the peak response of the impulse. Just as the impulse has a function equal to unity, the step response has a function equal to $1/s$. The two most important parameters of a filter's step response are the overshoot and ringing.

4.5. Fundamentals of Low-Pass Filters

As the name implies, a low pass filter is a filter that passes the lower frequencies and rejects those at higher frequencies.

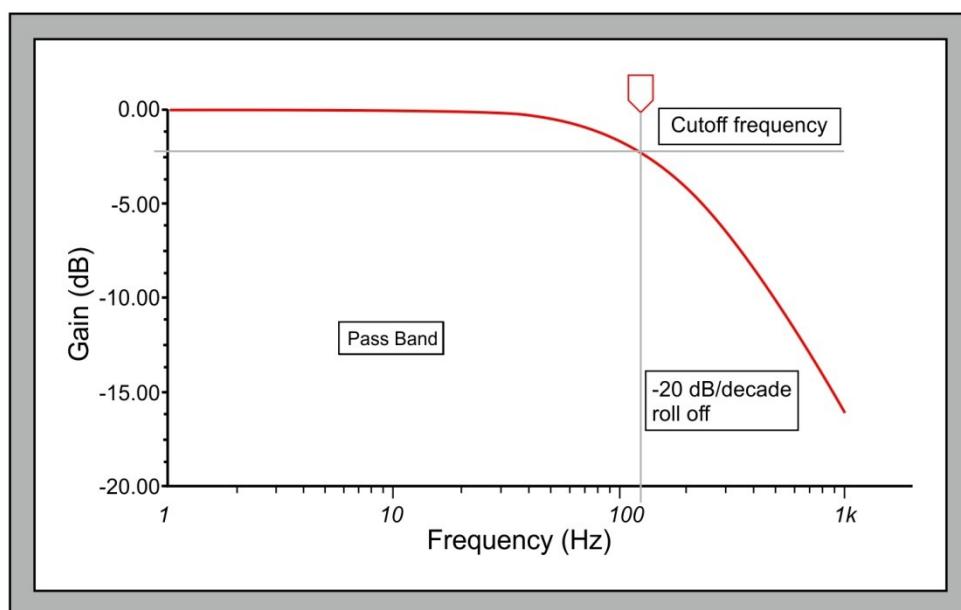


Fig 4.4 Low pass filter basic response curve

The cut-off frequency is normally taken as the point where the response has fallen by 3dB as shown. Another important feature is the final slope of the roll off. This is generally governed by the number of 'poles' in the filter. Normally there is one pole for each capacitor inductor in a filter.

The most simple low-pass filter is the passive RC low-pass network shown in Figure 4.5.

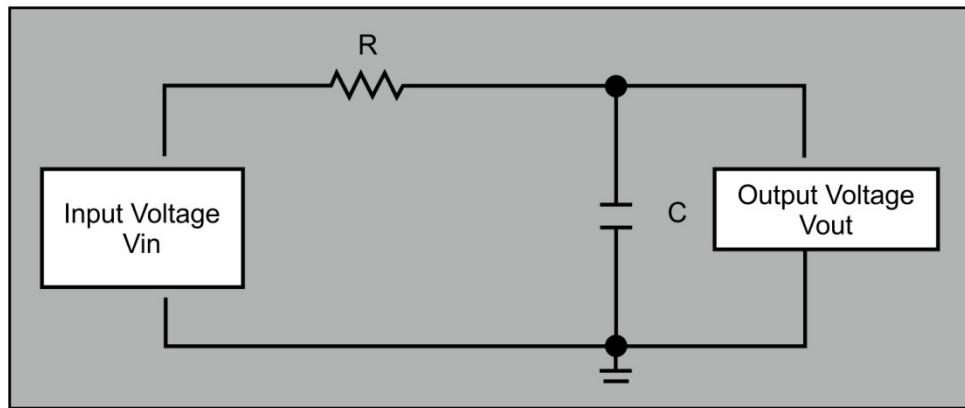


Fig 4.5 First-Order Passive RC Low-Pass Filter

Its transfer function is:

$$A(s) = \frac{\frac{1}{RC}}{s + \frac{1}{RC}} = \frac{1}{1 + sRC} \quad (4.2)$$

Where the complex frequency variable, $s = j\omega + \sigma$, allows for any time variable signals. For pure sine waves, the damping constant, σ , becomes zero and $s = j\omega$. For a normalized presentation of the transfer function, s is referred to the filter's corner frequency, or -3 dB frequency, ω_c , and has these relationships:

$$s = \frac{s}{\omega_c} = \frac{j\omega}{\omega_c} = j \frac{f}{f_c} = j\Omega \quad (4.3)$$

With the corner frequency of the low-pass in Figure 4.4 being $f_c = 1/2\pi RC$, s becomes $s = sRC$ and the transfer function $A(s)$ results in:

$$A(s) = \frac{1}{1 + s} \quad (4.4)$$

The magnitude of the gain response is:

$$|A| = \frac{1}{\sqrt{1 + \Omega^2}} \quad (4.5)$$

The simplest circuit low pass filter circuit using an operational amplifier simply places a capacitor across the feedback resistor.

4.6 Butterworth Low-Pass Filters

This filter is also called a maximally flat or flat filter. This class of filters approximates the ideal filter well in the pass band. The Butterworth filter has an essentially flat amplitude-frequency response up to the cutoff frequency. Although Butterworth filters achieve the sharpest attenuation, their phase-shift as a function of frequency is non-linear. It has a monotonic drop in gain with frequency in the cut-off region and a maximally flat response below cut-off frequency, as illustrated in figure 4.6.

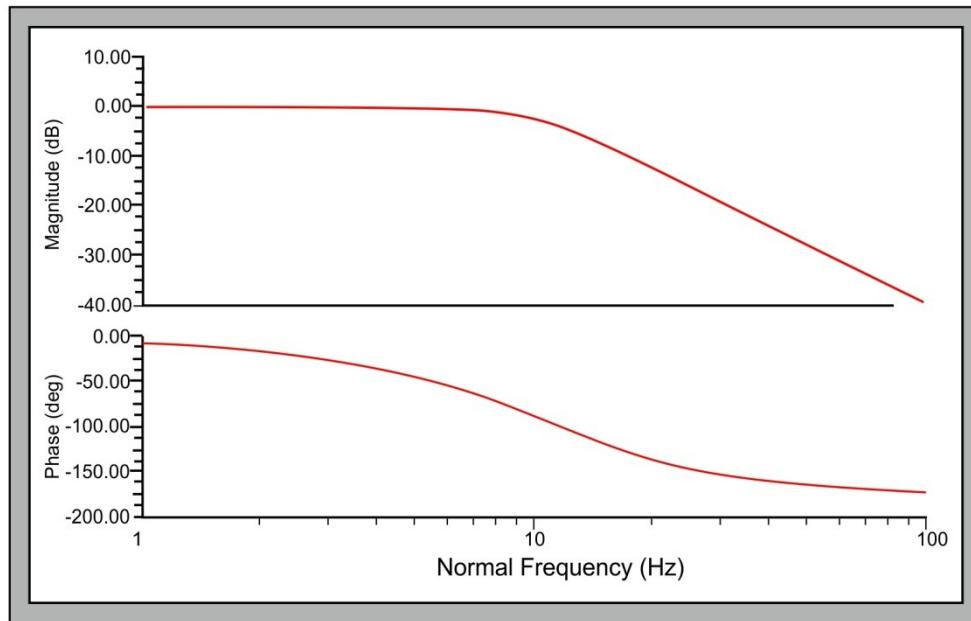


Fig 4.6 Magnitude and Phase response of Butterworth low Pass Filter

4.6.1 First order Low-Pass Filter Design

Fig 4.7 and Fig 4.8 show a first-order low-pass filter in the non-inverting and in the inverting configuration.

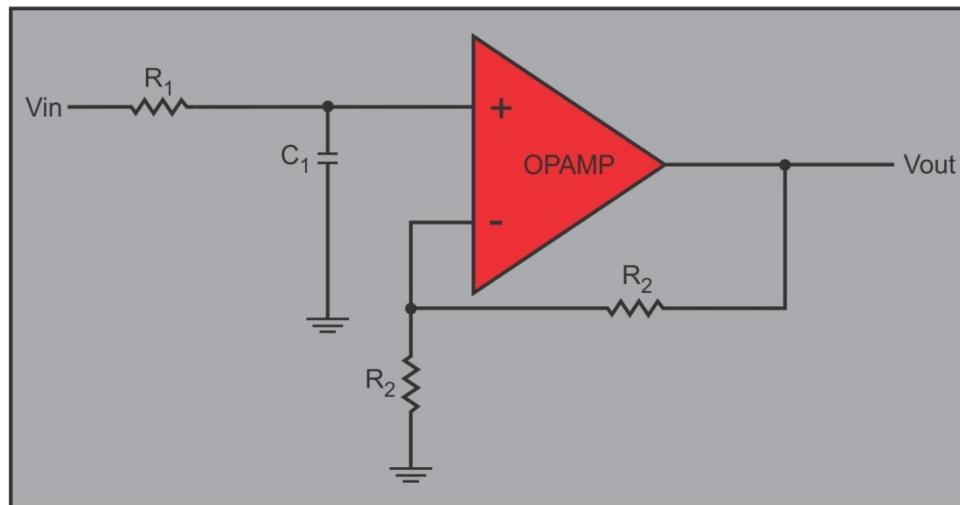


Fig 4.7 First-Order Non-inverting Low-Pass Filter

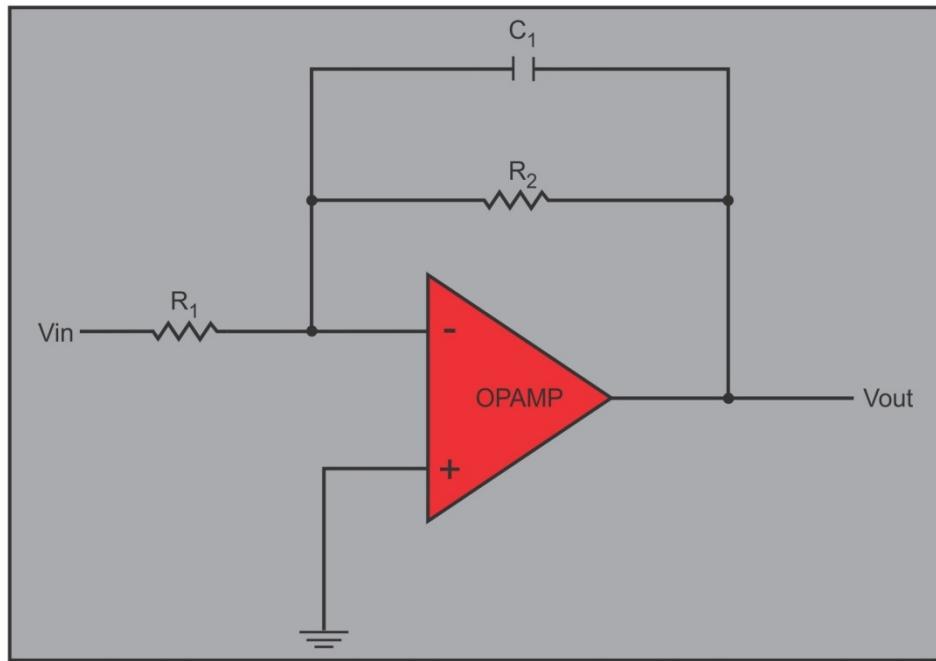


Fig 4.8 First-Order Inverting Low-Pass Filter

The transfer function of a single stage is:

$$A_i(s) = \frac{A_0}{1 + a_i s + b_i s^2} \quad (4.6)$$

For a first-order filter, the coefficient b is always zero ($b_1=0$), thus yielding:

$$A(s) = \frac{A_0}{1 + a_1 s} \quad (4.7)$$

The transfer functions of the circuits in 4.6 and 4.7 are:

$$A(s) = \frac{1 + \frac{R_2}{R_3}}{1 + w_C R_1 C_1 S} \quad \text{and} \quad A(s) = \frac{-\frac{R_2}{R_1}}{1 + w_C R_2 C_1 S} \quad (4.8)$$

The negative sign indicates that the inverting amplifier generates a 180° phase shift from the filter input to the output. The coefficient comparison between the two transfer functions yields,

$$A_0 = 1 + \frac{R_2}{R_3} \quad \text{and} \quad A_0 = -\frac{R_2}{R_1} \quad (4.9)$$

$$a_1 = w_C R_1 C_1 S \quad \text{and} \quad a_1 = w_C R_2 C_1 S$$

To dimension the circuit, specify the corner frequency (f_c), the dc gain (A_0), and capacitor C_1 , and then solve for resistors R_1 and R_2 :

$$R_1 = \frac{a_1}{2\pi f_c C_1} \text{ and } R_2 = \frac{a_1}{2\pi f_c C_1} \quad (4.10)$$

$$R_2 = R_3(A_0 - 1) \text{ and } R_1 = -\frac{R_2}{A_0}$$

Note, that all filter types are identical in their first order and $a_1 = 1$. For higher filter orders, however, $a_1 \neq 1$ because the corner frequency of the first-order stage is different from the corner frequency of the overall filter.

4.6.2. First-Order Unity-Gain Low-Pass Filter

For a first-order unity-gain low-pass filter with $f_c = 1$ kHz and $C_1 = 47$ nF, R_1 is:

$$R_1 = \frac{a_1}{2\pi f_c C_1} = \frac{1}{2\pi \cdot 10^3 \text{Hz} \cdot 47 \cdot 10^{-99} \text{F}} = 3.38 \text{k}\Omega$$

When operating at unity gain, the non-inverting amplifier reduces to a voltage follower (Figure 4.9), thus inherently providing a superior gain accuracy. In the case of the inverting amplifier, the accuracy of the unity gain depends on the tolerance of the two resistors, R_1 and R_2 .

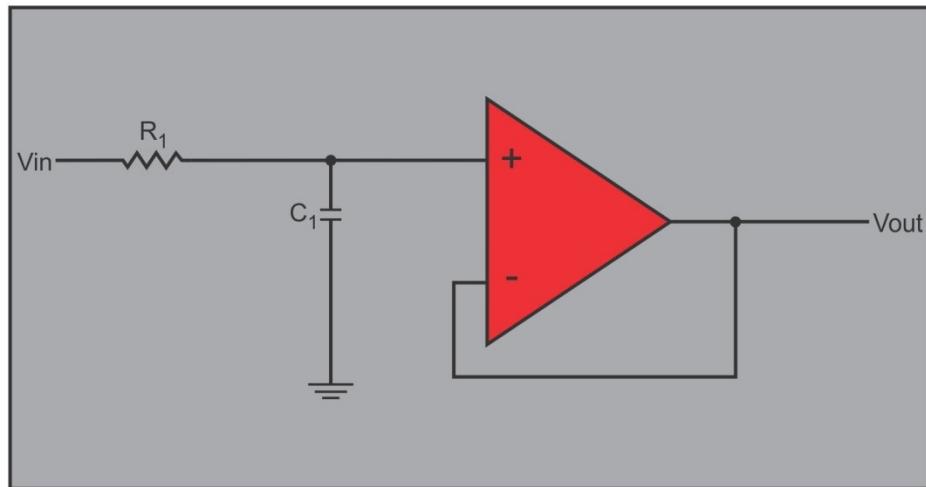


Fig 4.9 First-Order Non-inverting Low-Pass Filter with Unity Gain

Figure 4.10 and Figure 4.11 shows the circuit diagram and Simulation result of Low pass filter design-Chebyshev 1st order with passband frequency of 1KHz and 10 KHz using webench simulation tool.

Name: Lowpass, Real pole, Chebyshev, 1 dB

Part: Ideal OpAmp

Order: 1

Number of Stages: 1

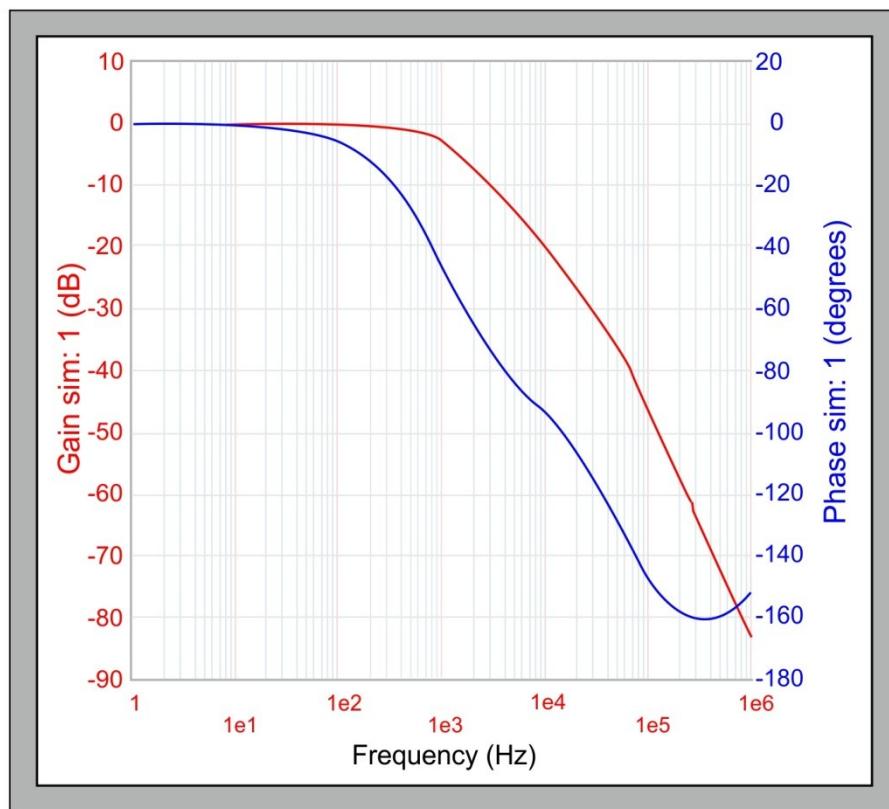
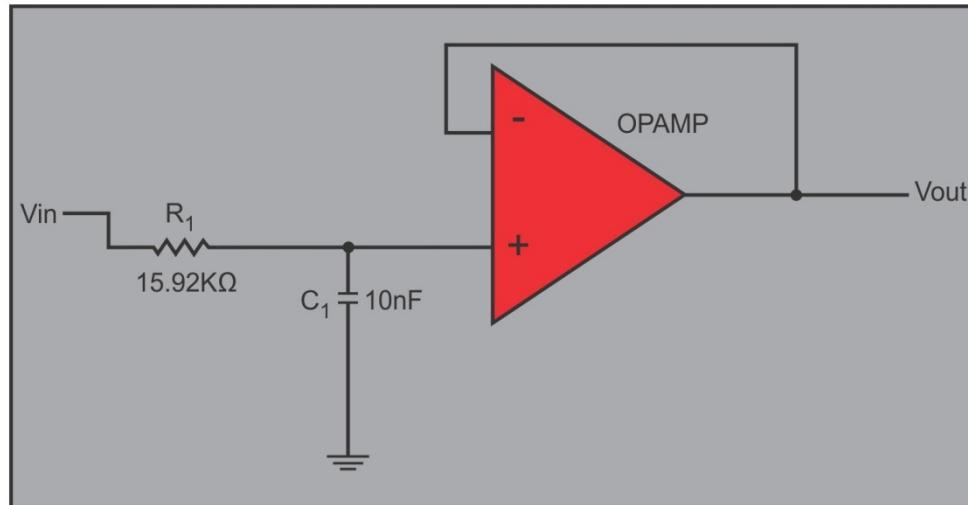
Gain: 1V/V (0 dB) **Allowable Passband Ripple:** 1 dB **Passband Frequency:** 1 kHz **Corner Frequency Attenuation:** -1 dB


Fig 4.10 Circuit diagram and Simulation result of Low pass filter design- Chebyshev, 1st order (with passband frequency of 1KHz)

Name: Lowpass, Real pole, Chebyshev, 1 dB

Part: Ideal OpAmp

Order: 1

Number of Stages: 1

Gain: 1V/V (0 dB) Allowable Passband Ripple: 1 dB Passband Frequency: 10 kHz Corner Frequency Attenuation: -1 dB

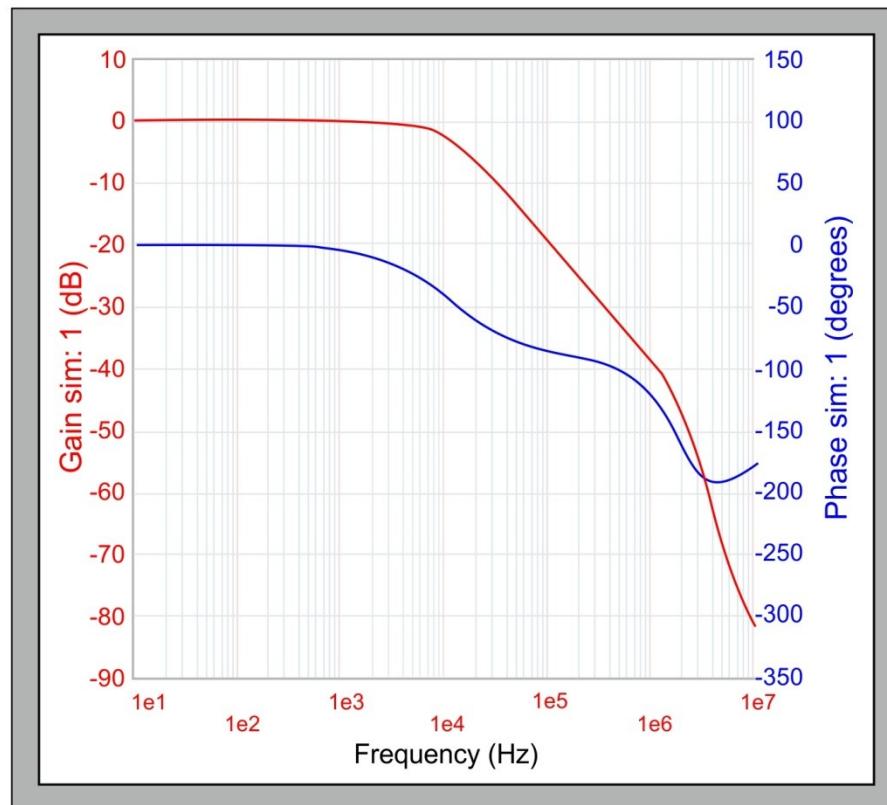
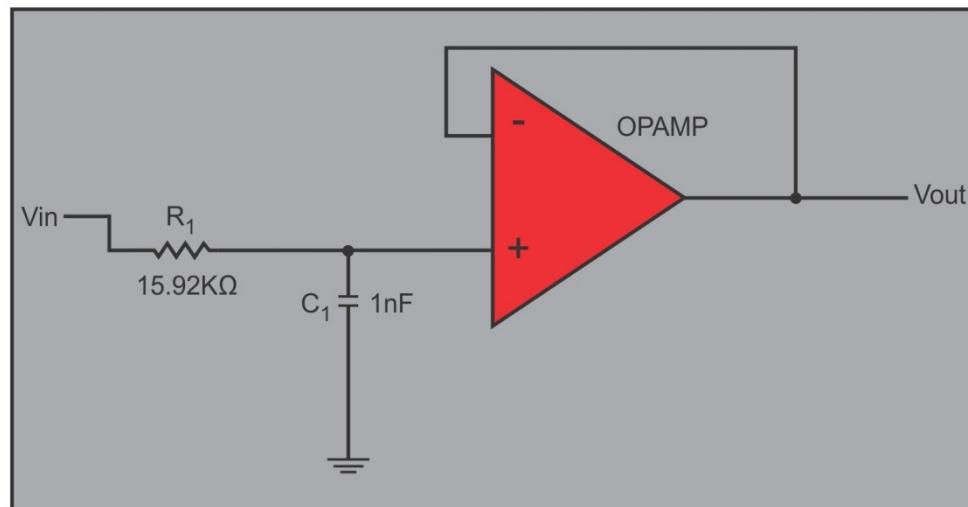


Fig 4.11 Circuit diagram and Simulation result of Low pass filter design- Chebyshev 1st order (with passband frequency of 10 KHz)

4.6.3. Second-Order Low-Pass Filter

There are two topologies for a second-order low-pass filter - the Sallen-Key and the Multiple Feedback (MFB) topologies.

4.6.3.1. Sallen-Key Topology

The general Sallen-Key topology in Figure 4.12 allows for separate gain setting via $A_0 = 1 + R_4/R_3$. However, the unity-gain topology in Figure 4.13 is usually applied in filter designs with high gain accuracy, unity gain, and low Qs ($Q < 3$).

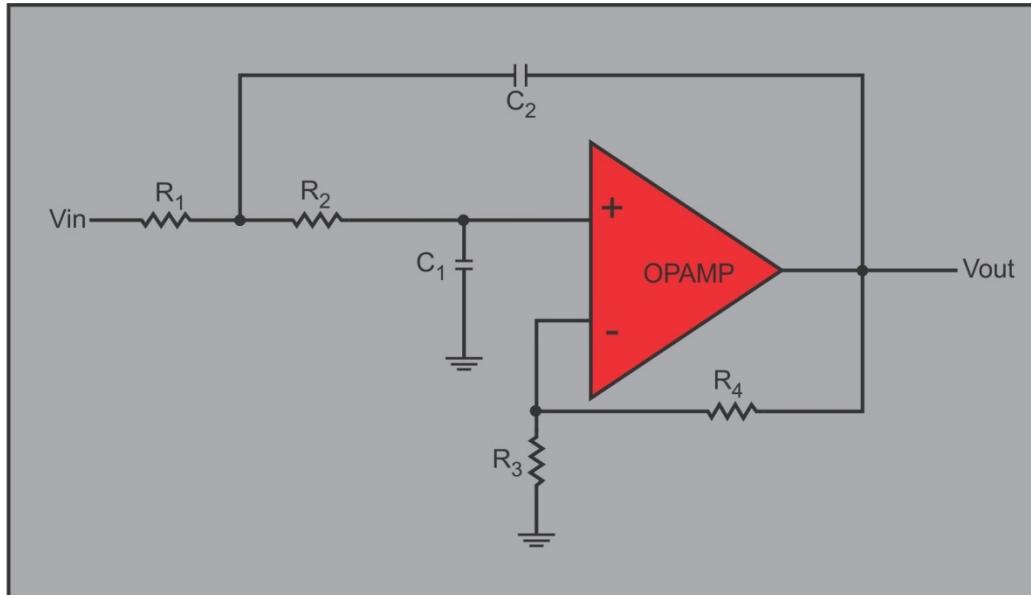


Fig 4.12 General Sallen-Key Low-Pass Filter

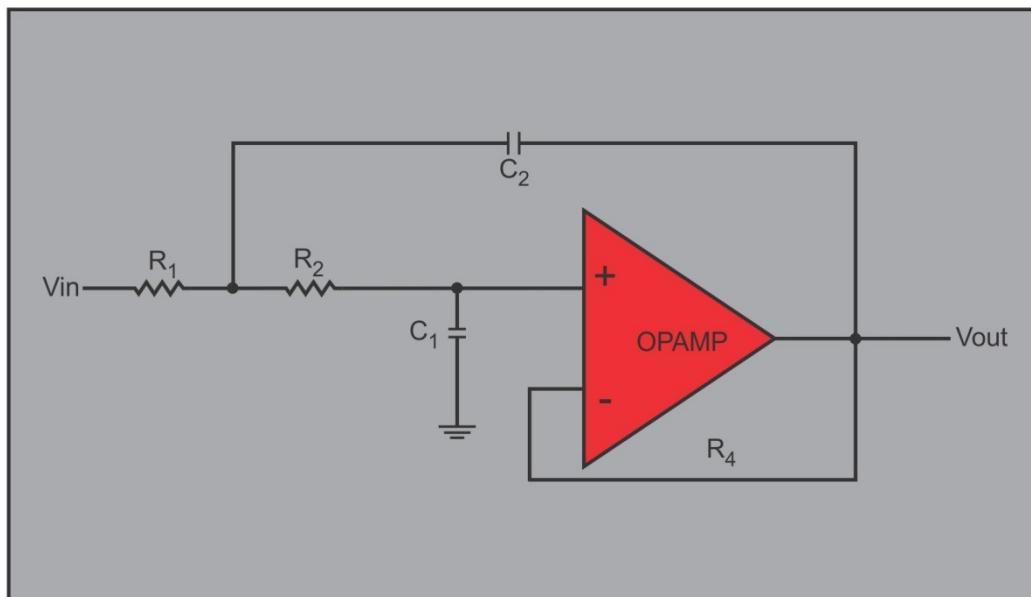


Fig 4.13 Unity-Gain Sallen-Key Low-Pass Filter

This configuration shows the least dependence of filter performance on the performance of the op amp because the op amp is configured as an amplifier, as opposed to an integrator, which minimizes the gain-bandwidth requirements of the op amp. Another advantage of this configuration is that the ratio of the largest resistor value to the smallest resistor value, and the ratio of the largest capacitor value to the smallest capacitor value (component spread) are low, which is beneficial for manufacturability.

While the Sallen-Key filter is widely used, a serious drawback is that the filter is not easily tuned, due to interaction of the component values on F₀ and Q. Another limitation is the relatively low maximum Q value obtainable.

The transfer function of circuit shown in figure 4.12 yields:

$$A(s) = \frac{A_o}{1 + w_c [C_1(R_1 + R_2) + (1 - A_o)R_1 C_2]s + w_c^2 R_1 R_2 C_1 C_2 s^2} \quad (4.11)$$

For the unity-gain circuit in Figure 4.12 ($A_o=1$), the transfer function simplifies to:

$$A(s) = \frac{1}{1 + w_c C_1 (R_1 + R_2) s + w_c^2 R_1 R_2 C_1 C_2 s^2} \quad (4.12)$$

The coefficient comparison between this transfer function yields:

$$\begin{aligned} A_o &= 1 \\ a_1 &= w_c C_1 (R_1 + R_2) \\ b_1 &= w_c^2 R_1 R_2 C_1 C_2 \end{aligned} \quad (4.13)$$

Given C₁ and C₂, the resistor values for R₁ and R₂ are calculated through:

$$R_{1,2} = \frac{a_1 C_2 \mp \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2}}{4\pi f_c C_1 C_2} \quad (4.14)$$

Table 4.1 Second order filter coefficients for Butterworth and Chebyshev filters

SECOND-ORDER	BUTTERWORTH	3- dB CHEBYSHEV
a1	1.4142	1.065
b1	1	1.9305
Q	0.71	1.3
R ₄ /R ₃	0.568	0.234

4.6.3.2. Multiple Feedback Topology

The MFB topology is commonly used in filters that have high Qs and require a high gain. Therefore, the dependence of the transfer function on the op amp parameters is greater than in the Sallen-Key realization. It is difficult to generate high Q, high frequency sections due to the limitations of the open-loop gain of the op amp. The peaking due to Q causes amplitude, A₀

$$A_0 = H Q \quad (4.15)$$

Where H is the gain of the circuit. The multiple feedback filter inverts the phase of the signal. This is equivalent to adding the resulting 180° phase shift to the phase shift of the filter itself.

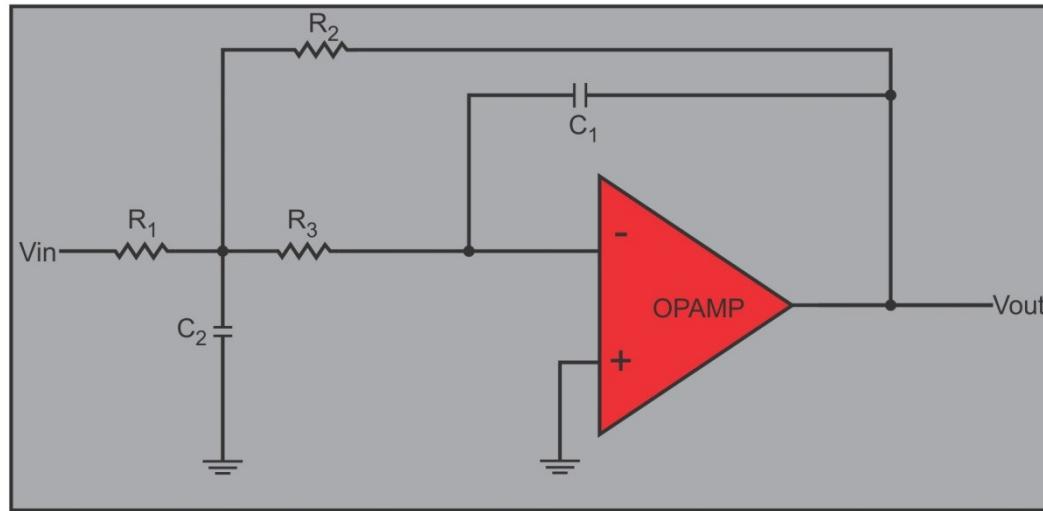


Fig 4.14 Second-Order MFB Low-Pass Filter

The transfer function of the circuit in Figure 4.14 is:

$$A(s) = -\frac{\frac{R_2}{R_1}}{1 + w_c C_1 (R_2 + R_3 + \frac{R_2 R_3}{R_1})s + w_c^2 R_3 R_2 C_1 C_2 s^2} \quad (4.16)$$

Through coefficient comparison with above equation one obtains the relation:

$$\begin{aligned} A_o &= -\frac{R_2}{R_1} \\ a_1 &= w_c C_1 (R_2 + R_3 + \frac{R_2 R_3}{R_1}) \\ b_1 &= w_c^2 R_2 R_3 C_1 C_2 \end{aligned} \quad (4.17)$$

Given C_1 and C_2 , and solving for the resistors R_1 - R_3 :

$$R_2 = \frac{a_1 C_2 - \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2 (1 - A_o)}}{4\pi f_c C_1 C_2} \quad (4.18)$$

$$R_1 = \frac{R_2}{-A_o} \quad \text{and} \quad R_3 = \frac{b_1}{4\pi^2 f_c^2 C_1 C_2 R_2}$$

In order to obtain real values for R_2 , C_2 must satisfy the following condition:

$$C_2 \geq C_1 \frac{4b_1(1 - A_o)}{a_1^2} \quad (4.19)$$

4.7. High-Pass Filter Design

As the name implies, a high pass filter is a filter that passes the higher frequencies and rejects lower frequencies (Fig 4.15). This may be useful in some audio applications to remove low frequency hum, or within RF to remove low frequency signals that are not required.

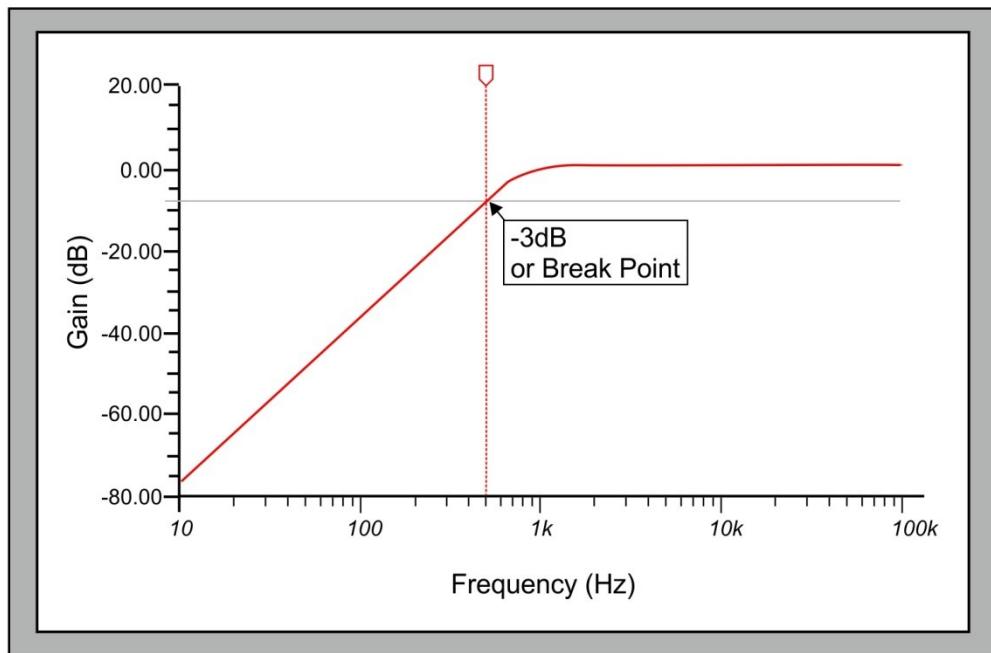


Fig 4.15 High pass filter basic response curve

By replacing the resistors of a low-pass filter with capacitors, and its capacitors with resistors, a high-pass filter is created (Figure 4.15).

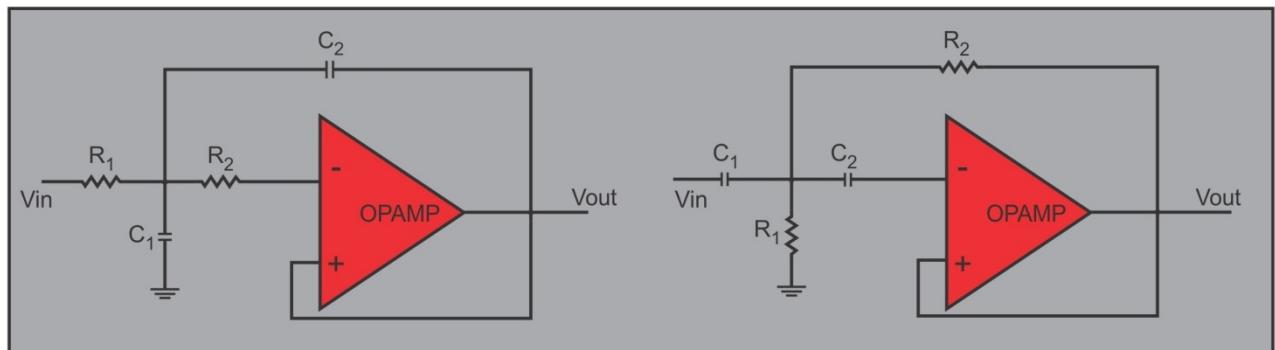


Fig 4.16 Low-Pass to High-Pass Transition through Components Exchange

The general transfer function of a high-pass filter is then:

$$A(s) = \frac{A_{\infty}}{\pi \left(1 + \frac{a_i}{s} + \frac{b_i}{s^2} \right)} \quad (4.20)$$

With A_{∞} being the passband gain

Since the above equation represents a cascade of second-order high-pass filters, the transfer function of a single stage is:

$$A_i(s) = \frac{A_\infty}{\left(1 + \frac{a_i}{s} + \frac{b_i}{s^2}\right)} \quad (4.21)$$

With $b=0$ for all first-order filters, the transfer function of a first-order filter simplifies to:

$$A(s) = \frac{A_o}{1 + \frac{a_i}{s}} \quad (4.22)$$

4.7.1 First-Order Butterworth High-Pass Filter

Fig 4.17 and Fig 4.18 show a first-order high-pass filter in the non-inverting and the inverting configuration.

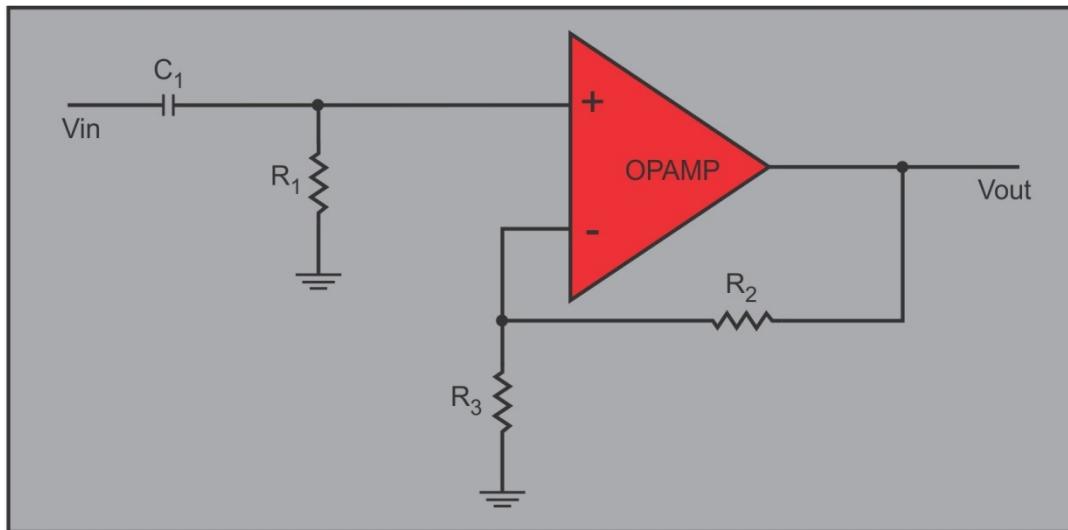


Fig 4.17 First-Order Non-inverting High-Pass Filter

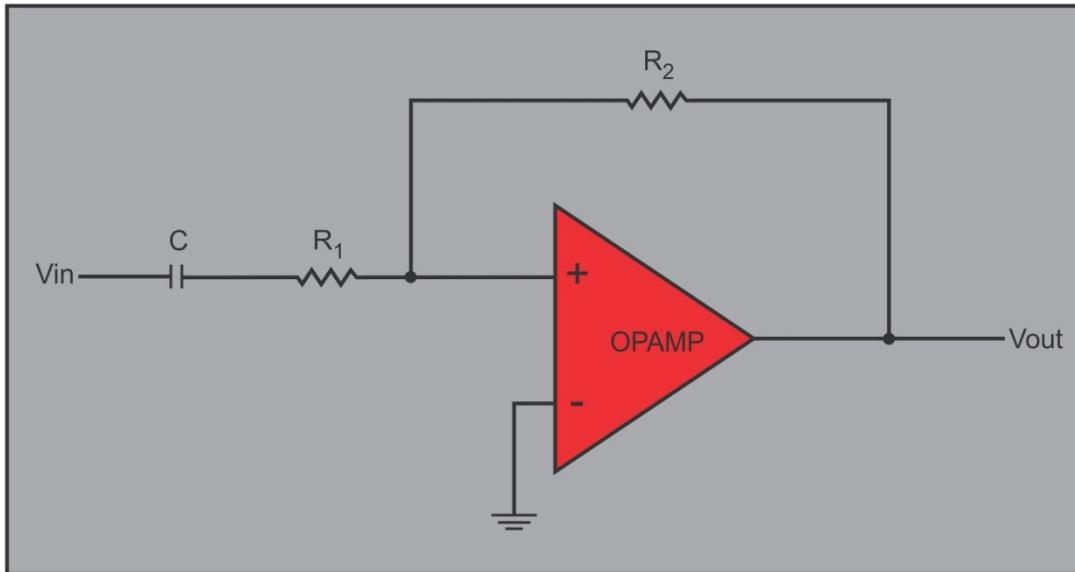


Fig 4.18 First-Order Inverting High-Pass Filter

The transfer function of the circuit is:

$$A(s) = \frac{\alpha}{1 + \frac{R_2(C_1+C_2)+R_1C_2(1-\alpha)}{\omega_C R_1 R_2 C_1 C_2} \cdot \frac{1}{s} + \frac{1}{\omega_C^2 R_1 R_2 C_1 C_2} \cdot \frac{1}{s^2}} \quad \text{with } \alpha = 1 + \frac{R_4}{R_3} \quad (4.23)$$

The unity-gain topology in Figure 4.19 is usually applied in low-Q filters with high gain accuracy.

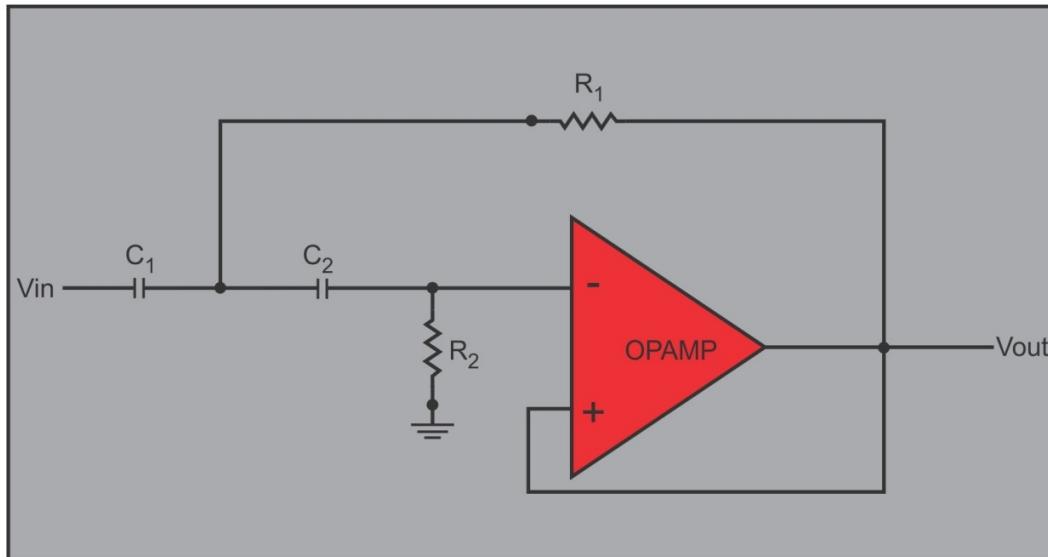


Fig 4.19 Unity-Gain Sallen-Key High-Pass Filters

To simplify the circuit design, it is common to choose unity-gain ($\alpha = 1$), and $C_1 = C_2 = C$. The transfer function of the circuit in Figure 4.18 then simplifies to:

$$A(S) = \frac{1}{1 + \frac{2}{\omega_C R_1 C} \cdot \frac{1}{S} + \frac{1}{\omega_C^2 R_1 R_2 C^2} \cdot \frac{1}{S^2}} \quad (4.24)$$

The coefficient comparison between this transfer function yields:

$$A_\infty = 1$$

$$a_1 = \frac{2}{\omega_C R_1 C}$$

$$b_1 = \frac{1}{\omega_C^2 R_1 R_2 C^2} \quad (4.25)$$

Given C, the resistor values for R₁ and R₂ are calculated through:

$$R_1 = \frac{1}{\pi f_C C a_1}$$

$$R_1 = \frac{a_1}{4\pi f_C C b_1} \quad (4.26)$$

Figure 4.20 shows the circuit diagram and Simulation result of High pass filter design- Chebyshev, butterworth, bessel- 1st order using webbench simulation tool.

Name: Highpass, Real pole, Chebyshev, 1 dB

Part: Ideal OpAmp

Order: 1

Number of Stages: 1

Gain: 1V/V (0 dB) **Allowable Passband Ripple:** 1 dB **Passband Frequency:** 10 kHz **Corner Frequency Attenuation:** -1 dB

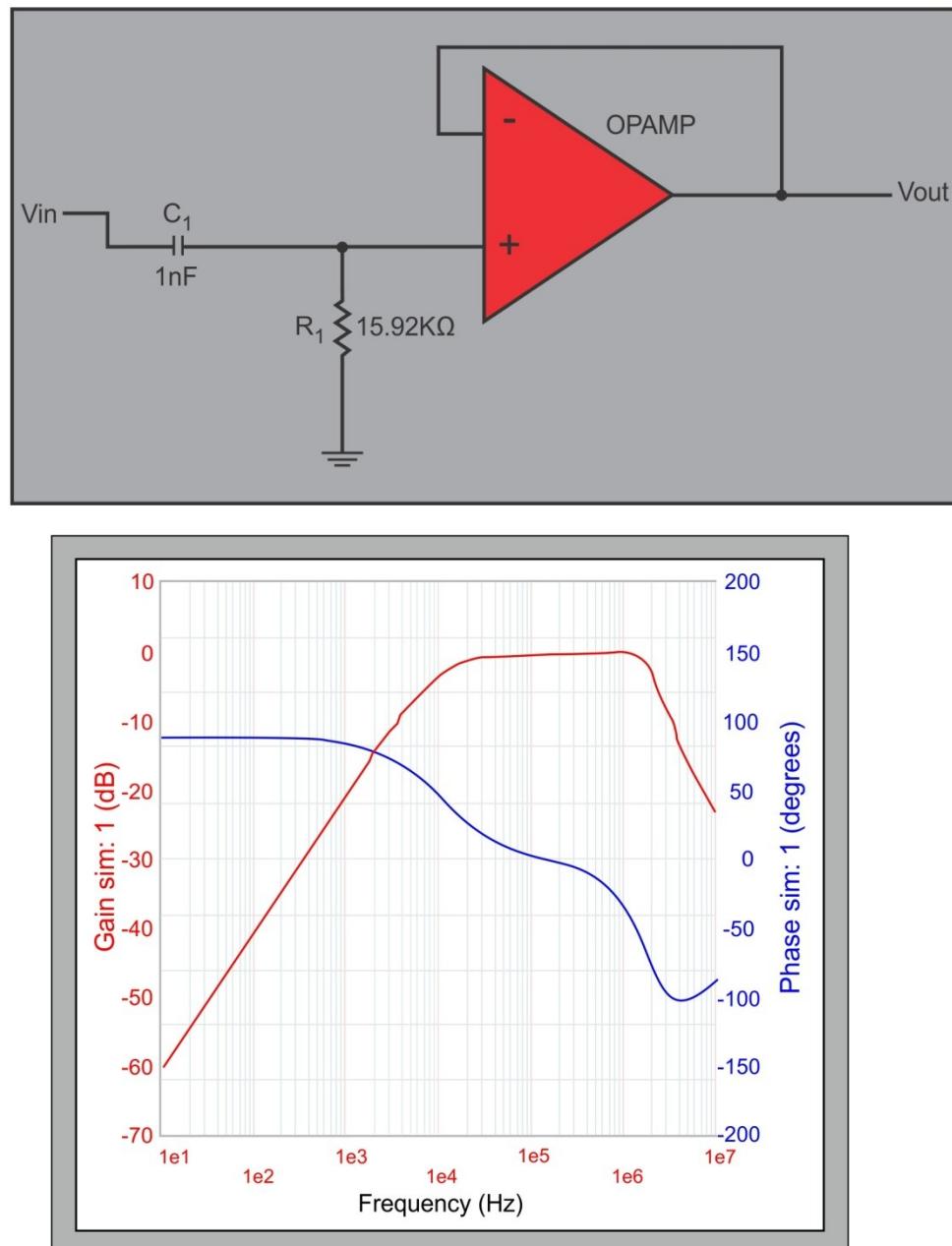


Fig 4.20 Circuit diagram and Simulation result of High pass filter design- Chebyshev- 1st order

4.7.2. Multiple Feedback Topology

The MFB topology is commonly used in filters that have high Qs and require a high gain. To simplify the computation of the circuit, capacitors C_1 and C_3 assume the same value ($C_1 = C_3 = C$) as shown in Figure 4.21.

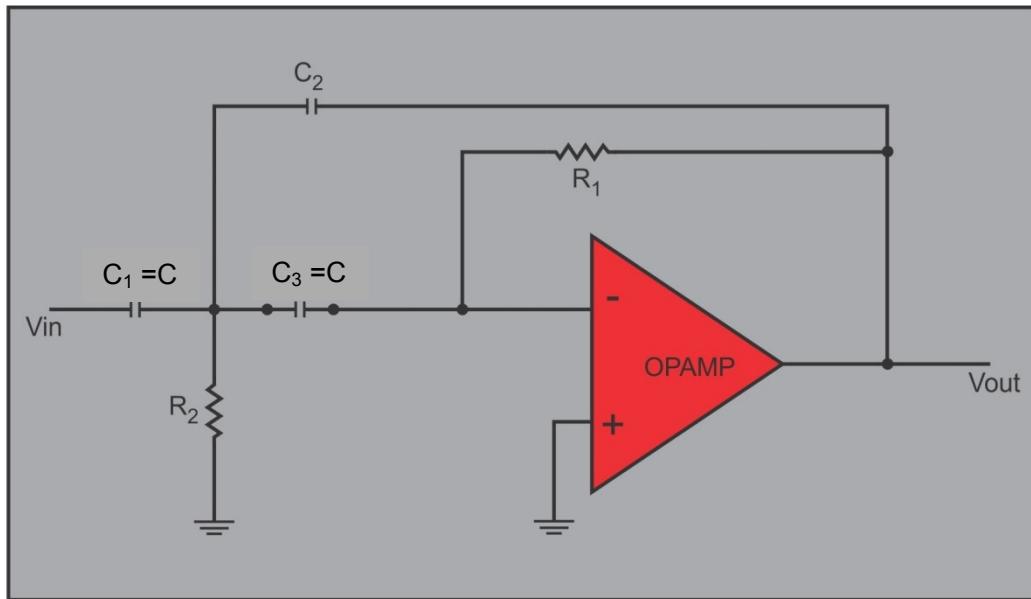


Fig 4.21 Second-Order MFB High-Pass Filter

The transfer function of the circuit in Figure 4.20 is:

$$A(s) = -\frac{\frac{C}{C_2}}{1 + \frac{2C+C_2}{\omega_C R_1 C C_2} \cdot \frac{1}{s} + \frac{2C+C_2}{\omega_C R_1 C C_2} \cdot \frac{1}{s^2}} \quad (4.27)$$

Through coefficient comparison, obtain the following relations:

$$\begin{aligned} A_\infty &= \frac{C}{C_2} \\ a_1 &= \frac{2C + C_2}{\omega_C R_1 C C_2} \\ b_1 &= \frac{2C + C_2}{\omega_C R_1 C C_2} \end{aligned} \quad (4.28)$$

Given capacitors C and C_2 , and solving for resistors R_1 and R_2

$$\begin{aligned} R_1 &= \frac{1 - 2A_\infty}{2\pi f_c C a_1} \\ R_2 &= \frac{a_1}{2\pi f_c b_1 C_2 (1 - 2A_\infty)} \end{aligned} \quad (4.29)$$

The passband gain (A_{∞}) of a MFB high-pass filter can vary significantly due to the wide tolerances of the two capacitors C and C_2 . To keep the gain variation at a minimum, it is necessary to use capacitors with tight tolerance values.

4.8. Band-Pass Filter Design

A high-pass response was generated by replacing the term S in the low-pass transfer function with the transformation $1/S$. Likewise, a band-pass characteristic is generated by replacing the S term with the transformation:

$$\frac{1}{\Delta\Omega} \left(s + \frac{1}{s} \right)$$

In this case, the passband characteristic of a low-pass filter is transformed into the upper passband half of a band-pass filter. The upper passband is then mirrored at the mid frequency, f_m ($\Omega=1$), into the lower passband half.

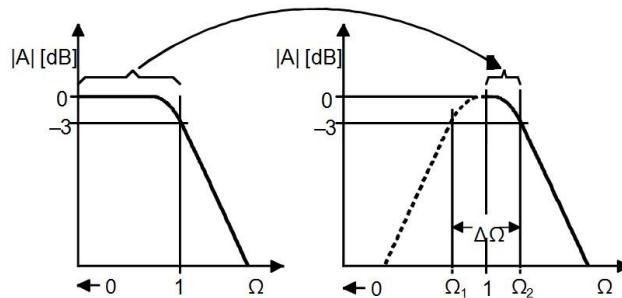


Fig 4.22 Low-Passes to Band-Pass Transition

The corner frequency of the low-pass filter transforms to the lower and upper -3 dB frequencies of the band-pass, Ω_1 and Ω_2 . The difference between both frequencies is defined as the normalized bandwidth, $\Delta\Omega = \Omega_2 - \Omega_1$. The normalized mid frequency, where $Q = 1$, is $\Omega_m = 1 = \Omega_1\Omega_2$.

In analogy to the resonant circuits, the quality factor Q is defined as the ratio of the mid frequency (f_m) to the bandwidth (B):

$$Q = \frac{f_m}{B} = \frac{f_m}{\Omega_2 - \Omega_1} = \frac{1}{\Omega_2 - \Omega_1} = \frac{1}{\Delta\Omega} \quad (4.30)$$

The simplest design of a band-pass filter is the connection of a high-pass filter and a lowpass filter in series, which is commonly done in wide-band filter applications. In comparison to wide-band filters, narrow-band filters of higher order consist of cascaded second-order band-pass filters that use the Sallen-Key or the Multiple Feedback (MFB) topology.

4.8.1. Second-Order Butterworth Band-Pass Filter

To develop the frequency response of a second-order band-pass filter, apply the transformation to a first-order low-pass transfer function:

$$A(S) = \frac{A_0}{1 + S} \quad (4.31)$$

Replacing S with $\frac{1}{\Delta\Omega} \left(s + \frac{1}{s} \right)$

Yields the general transfer function for a second-order band-pass filter:

$$A(S) = \frac{A_0 \cdot \Delta\Omega \cdot s}{1 + \Delta\Omega \cdot S + s^2} \quad (4.32)$$

When designing band-pass filters, the parameters of interest are the gain at the mid frequency (A_m) and the quality factor (Q), which represents the selectivity of a band-pass filter. Therefore, replace A_0 with A_m and $\Delta\Omega$ with $1/Q$ and obtain:

$$A(S) = \frac{\frac{A_m}{Q} \cdot s}{1 + \frac{1}{Q} \cdot S + s^2} \quad (4.33)$$

4.8.2. Sallen-Key Topology

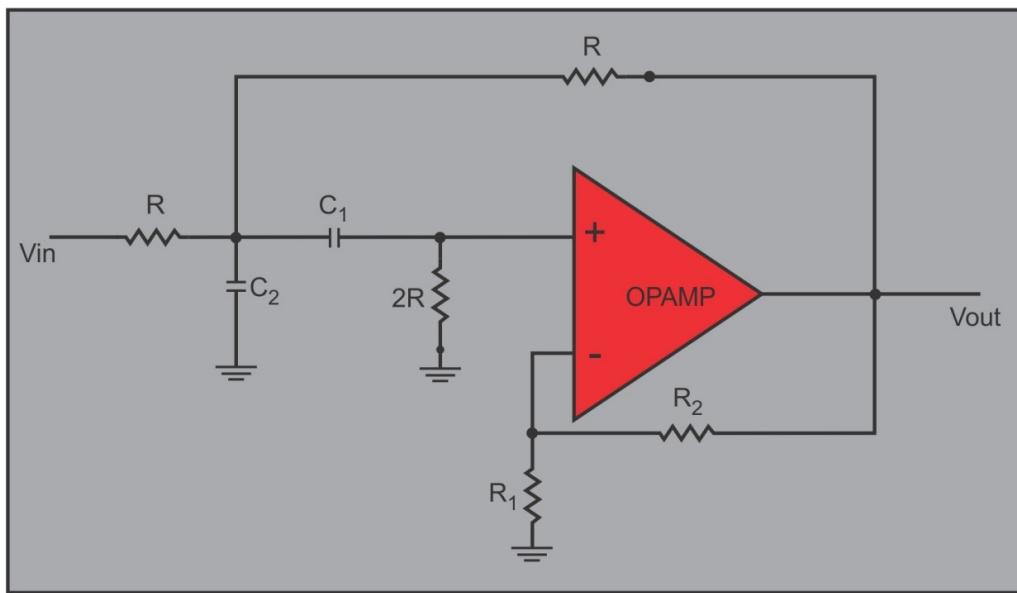


Fig 4.23 Sallen-Key Band-Pass filter

The Sallen-Key band-pass circuit in Figure 4.22 has the following transfer function:

$$A(s) = \frac{G \cdot RC \omega_m \cdot s}{1 + RC \omega_m (3 - G) \cdot s + R^2 C^2 \omega_m^2 s^2} \quad (4.34)$$

Then through coefficient comparison:

$$\text{Mid frequency: } f_m = \frac{1}{2\pi RC}$$

$$\text{Inner gain: } G = 1 + \frac{R_2}{R_1}$$

$$\text{Gain at } f_m : A_m = \frac{G}{3 - G}$$

$$\text{Filter quality: } Q = \frac{1}{3 - G}$$

The Sallen-Key circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (fm). A drawback is, however, that Q and A_m cannot be adjusted independently. To set the mid frequency of the band-pass, specify f_m and C and then solve for $R = \frac{1}{2\pi f_c C}$. Because of the dependency between Q and A_m , there are two options to solve for R_2 : either to set the gain at mid frequency, $R_2 = \frac{2A_m - 1}{1 + A_m}$ or to design for a specified Q, $R_2 = \frac{2Q - 1}{Q}$

4.8.2.1. Multiple Feedback Topology

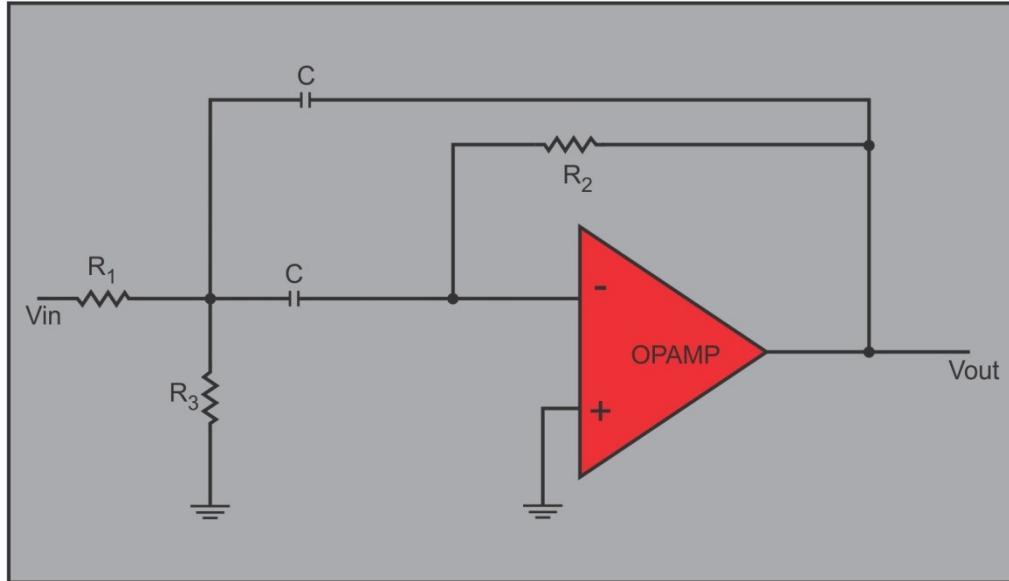


Fig 4.24 MFB Band-Pass Filter

The MFB band-pass circuit in Figure 4.23 has the following transfer function:

$$A(s) = \frac{-\frac{R_2 R_3}{R_1 + R_3} C \omega_m \cdot s}{1 + \frac{2R_1 R_3}{R_1 + R_3} C \omega_m \cdot s + \frac{R_1 R_2 R_3}{R_1 + R_3} C^2 \omega_m^2 s^2} \quad (4.35)$$

The coefficient comparison with equation yields the following equations:

$$\text{Mid-frequency: } f_m = \frac{1}{2\pi C} \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}}$$

$$\text{Gain at } f_m = -A_m = \frac{R_2}{2R_1}$$

$$\text{Filter quality: } Q = \pi f_m R_2 C$$

$$\text{Bandwidth: } B = \frac{1}{\pi R_2 C}$$

The MFB band-pass allows to adjust Q, A_m , and f_m independently. Bandwidth and gain factor do not depend on R_3 . Therefore, R_3 can be used to modify the mid frequency without affecting bandwidth, B,

or gain, A_m . For low values of Q, the filter can work without R3, however, Q then depends on A_m via:
 $-A_m = 2Q^2$

To design a second-order MFB band-pass filter with a mid-frequency of $f_m = 1$ kHz, a quality factor of $Q = 10$, and a gain of $A_m = -2$, assume a capacitor value of $C = 100$ nF, and solve the previous equations for R through R_3 in the following sequence:

$$R_2 = \frac{Q}{\pi f_{mc}} = \frac{10}{\pi \cdot 1\text{kHz} \cdot 100\text{nF}} = 31.8\text{k}\Omega$$

$$R_1 = \frac{R_2}{-2fA_m} = \frac{31.8\text{k}\Omega}{4} = 7.96\text{k}\Omega$$

$$R_3 = \frac{-A_m R_1}{2Q^2 + A_m} = \frac{2.796\text{k}\Omega}{200 - 2} = 80.4\Omega$$

Fig 4.25 shows the circuit diagram and Simulation result of Band pass filter design- Chebyshev 2st order using webbench simulation tool.

Name: Bandpass, Multiple Feedback, Chebyshev 1 dB **Part:** Ideal OpAmp **Order:** 2 **Number of stages:** 1

Gain: 1 V/V (0 dB) **Allowable Passband Ripple:** 1 dB **Passband Frequency:** 1 kHz **Corner Frequency Attenuation:** 0 dB
Passband Bandwidth: 100Hz

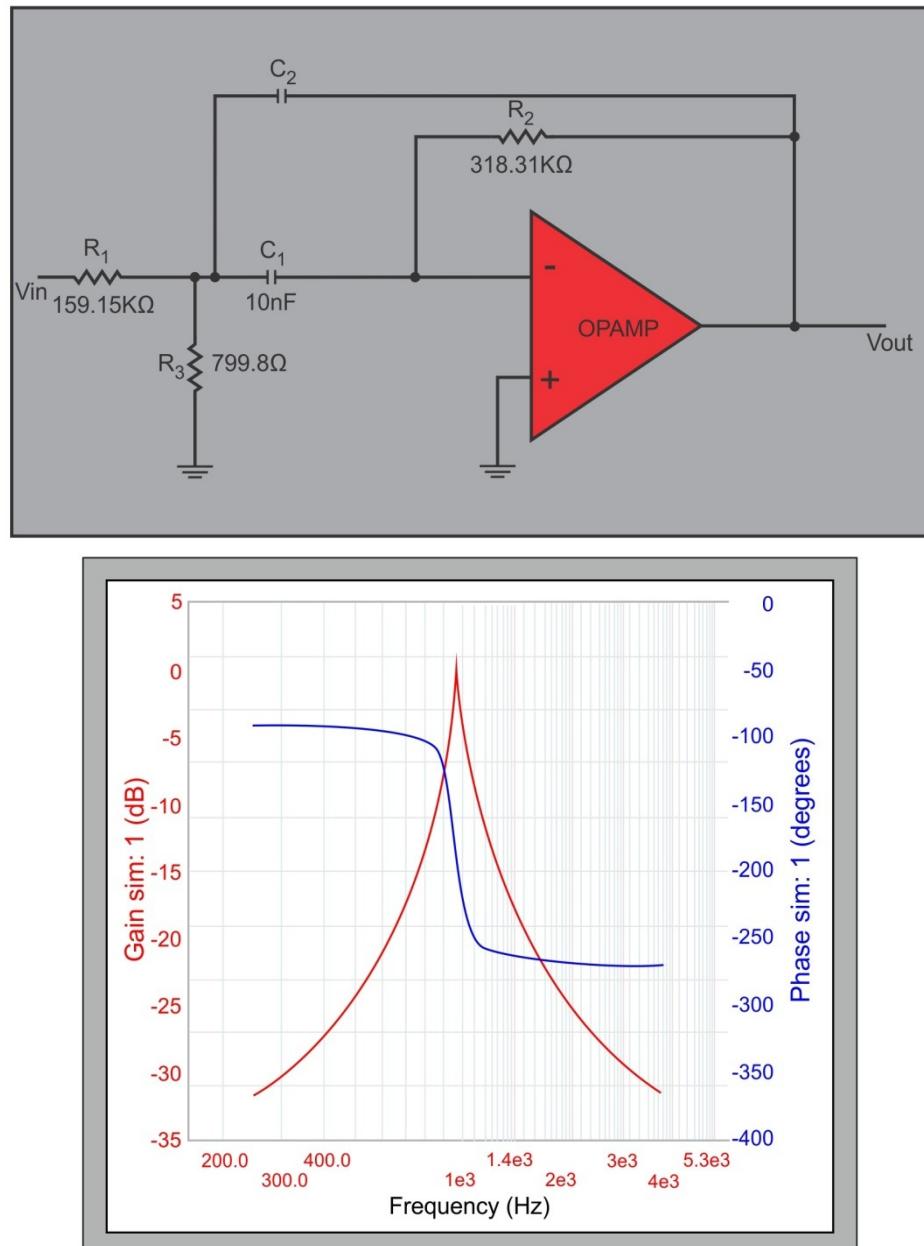


Fig 4.25 Circuit diagram and Simulation result of Band pass filter design- Chebyshev - 2nd order

Practical Design Example:

- (i) Design a second-order band-pass filter with $f_o=1\text{KHz}$, $\text{BW}=100\text{Hz}$. What is the resonance gain?
- (ii) Modify the circuit for a resonance gain of 20dB.

Solution:

- (i) Use the equal-component option with $C_1 = C_2 = 10\text{nF}$ and $R_1 = R_2 = R_3 = \sqrt{2/(2\pi f_o^2 \times 10^{-8})} = 22.5\text{k}\Omega$. We need $Q = f_o/\text{BW} = 10$, so $K = 4 - \sqrt{2}/10 = 3.858$. Pick $R_A = 10.0\text{k}\Omega$ or 1%. Then, $R_B = (K - 1) R_A = 28.58\text{k}\Omega$. The resonance gain is $K/(4 - K) = 27.28\text{V/V}$.
- (ii) Replace R_1 with two resistances R_{1A} and R_{1B} with $A_{\text{old}} = 27.28\text{V/V}$ and $A_{\text{new}} = 10^{20/20} = 10\text{V/V}$. This gives $R_{1A} = 61.9\text{k}\Omega$ or 1.9k and $R_{1B} = 35.7\text{k}\Omega$ or 5.7

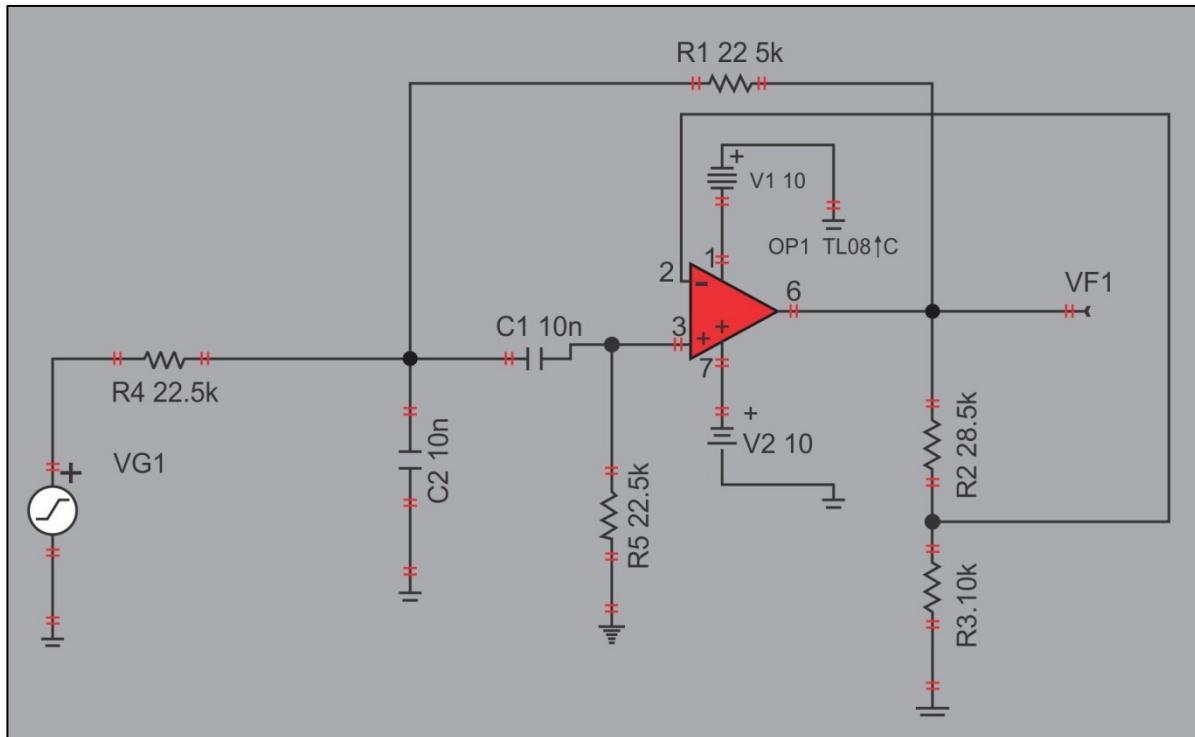
Circuit Diagram:


Fig 4.26: Second-order band-pass filter with $f_o= 1\text{ KHz}$, $\text{BW}=100\text{Hz}$

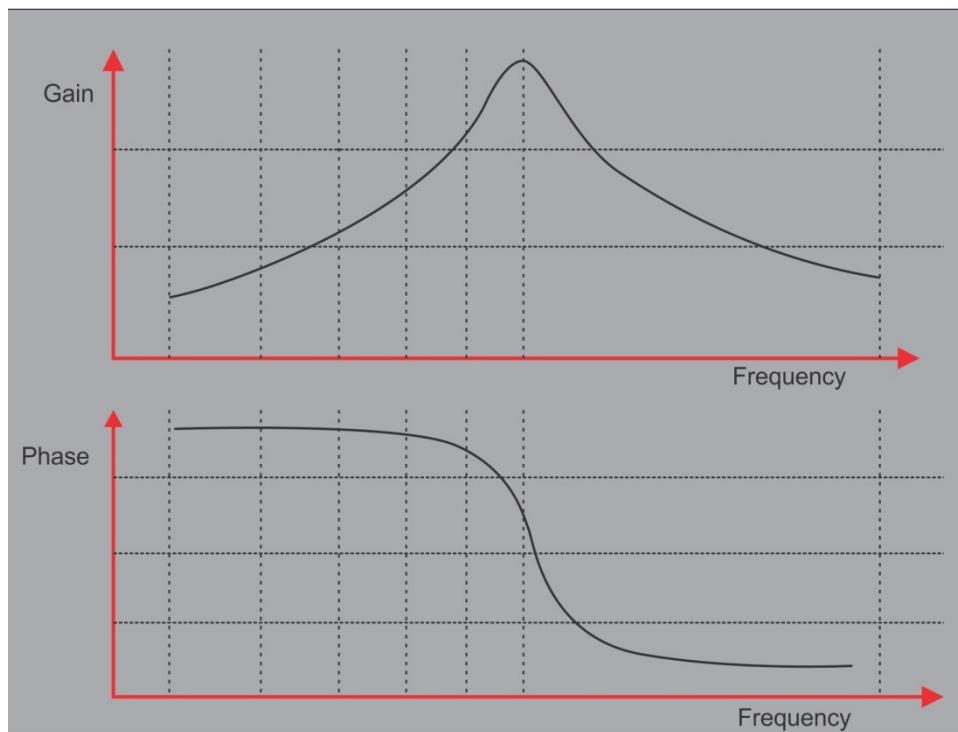
Simulation output:


Fig 4.27 Frequency response of second-order band-pass filter with $f_0 = 1 \text{ KHz}$, BW = 100 Hz

4.9. Characteristics of Chebyshev Low-Pass Filters

Chebyshev filters are analog or digital filters having a steeper roll-off and more passband ripple (type I) or stopband ripple (type II) than Butterworth filters. Chebyshev filters are used to separate one band of frequencies from another. Chebyshev filters are sharper than the Butterworth filter; they are not as sharp as the elliptic one, but they show fewer ripples over the bandwidth.

4.9.1. Type I Chebyshev Filters

Type I Chebyshev filters are the most common types of Chebyshev filters. It has no ripple in the stopband, but does have equiripple in the passband. The gain response as a function of angular frequency ω :

$$G_n(\omega) = |H_n(j\omega)| = \frac{1}{\sqrt{1 + \frac{1}{\epsilon^2 T_n^2(\frac{\omega_0}{\omega})}}} \quad (4.36)$$

where ϵ is the ripple factor,

ω_0 is the cutoff frequency,

T_n is a Chebyshev polynomial of the n th order,

$H_n(j\omega)$ is the transfer function n th-order low-pass filter. The passband exhibits equiripple behavior, with the ripple determined by the ripple factor ϵ . In the passband, the Chebyshev polynomial alternates between -1 and 1 so the filter gain alternate between maxima at $G = 1$ and minima at $G = \frac{1}{\sqrt{1+\epsilon^2}}$. At the cutoff frequency ω_0 the gain again has the value $\frac{1}{\sqrt{1+\epsilon^2}}$ but continues to drop into the

stop band as the frequency increases. The order of a Chebyshev filter is equal to the number of reactive components (for example, inductors) needed to realize the filter using analog electronics.

The ripple is often given in dB as, $20\log_{10} \sqrt{1 + \varepsilon^2}$ so that a ripple amplitude of 3 dB results from $\varepsilon = 1$. The frequency response is given in Figure 4.28.

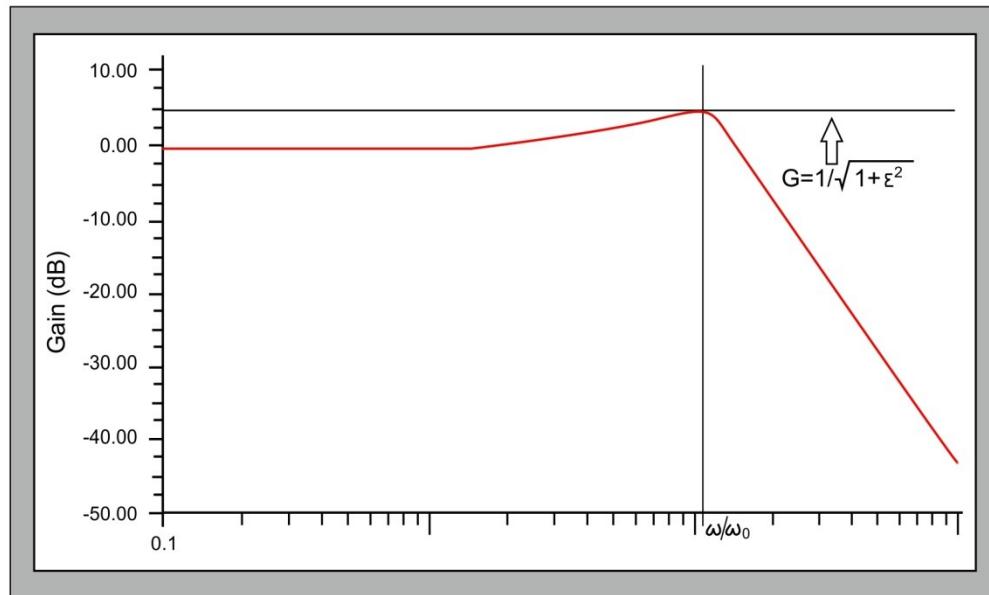


Fig 4.28 Frequency response of Chebyshev I Low pass filter

4.9.2. Type 2 II Chebyshev filters

Also known as inverse Chebyshev filters, the Type II Chebyshev filter type is less common because it does not roll off as fast as Type I and requires more components. It has no ripple in the passband, but does have equiripple in the stopband.

The gain is:

$$G_n(\omega, \omega_0) = \frac{1}{\sqrt{1 + \frac{1}{\varepsilon^2 T_n^2 \left(\frac{\omega_0}{\omega}\right)}}} \quad (4.37)$$

In the stopband, the Chebyshev polynomial oscillates between -1 and 1 and the smallest frequency at which this maximum is attained is the cutoff frequency ω_0 . The parameter ε is thus related to the stopband attenuation γ in decibels by,

$$\varepsilon = 1 / \sqrt{(10^{0.1\gamma} - 1)}$$

For a stopband attenuation of 5dB, $\varepsilon = 0.6801$; for an attenuation of 10dB, $\varepsilon = 0.333$. The frequency $f_0 = \omega_0/2\pi$ is the cutoff frequency. The 3dB frequency f_H is related to f_0 by

$$f_H = \frac{f_0}{\cosh^{-1} \cosh^{-1} \left(\frac{1}{\varepsilon} \right)} \text{. The Frequency Response is given in Figure 4.26.}$$

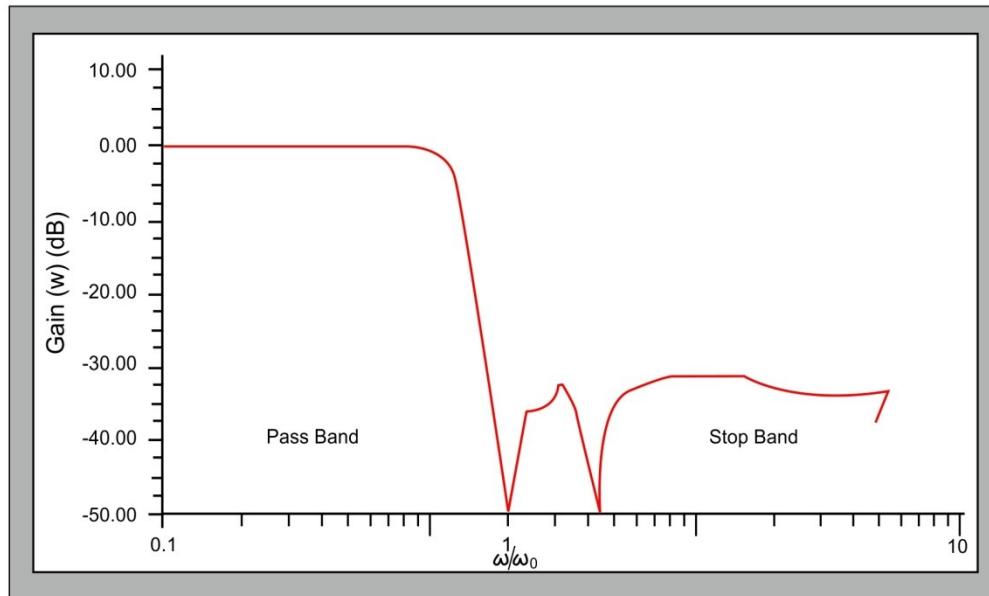


Fig 4.29 Frequency response of Chebyshev II Low pass filter

Chebyshev filters have 0 dB relative attenuation at dc. Odd order filters have an attenuation band that extends from 0 dB to the ripple value. Even-order filters have a gain equal to the passband ripple. Chebyshev filters are often used in filter banks, where the frequency content of a signal is of more importance than a constant amplification.

4.10. Band-Rejection Filter Design

The bandpass filter passes one set of frequencies while rejecting all others. The band-stop filter does just the opposite. It rejects a band of frequencies, while passing all others. This is also called a band-reject or band-elimination filter. Like bandpass filters, band-stop filters may also be classified as (i) wide-band and (ii) narrow band reject filters.

The narrow band reject filter is also called a notch filter. Because of its higher Q, which exceeds 10, the bandwidth of the narrow band reject filter is much smaller than that of a wide band reject filter.

Two of the most popular band-rejection filters are the active twin-T and the active Wien-Robinson circuit, both of which are second-order filters. To generate the transfer function of a second-order band-rejection filter, replace the S term of a first-order low-pass response with the transformation in $\frac{\Delta\Omega}{s + \frac{1}{s}}$, which gives:

$$A(s) = \frac{A_0(1 + s^2)}{1 + \Delta\Omega \cdot s + s^2} \quad (4.38)$$

Thus the passband characteristic of the low-pass filter is transformed into the lower passband of the band-rejection filter. The lower passband is then mirrored at the mid frequency, f_m ($\Omega=1$), into the upper passband half.

Identical to the selectivity of a band-pass filter, the quality of the filter rejection is defined as,

$$Q = \frac{f_m}{B} = \frac{1}{\Delta\Omega}$$

Therefore, replacing $\Delta\Omega$ in Equation A(s) with $1/Q$ yields:

$$A(s) = \frac{A_0(1 + s^2)}{1 + \frac{1}{Q} \cdot s + s^2} \quad (4.39)$$

4.10.1 Active Twin-T Filter

The original twin-T filter, shown in Figure 4.30, is a passive RC-network with a quality factor of $Q = 0.25$. To increase Q , the passive filter is implemented into the feedback loop of an amplifier, thus turning into an active band-rejection filter.

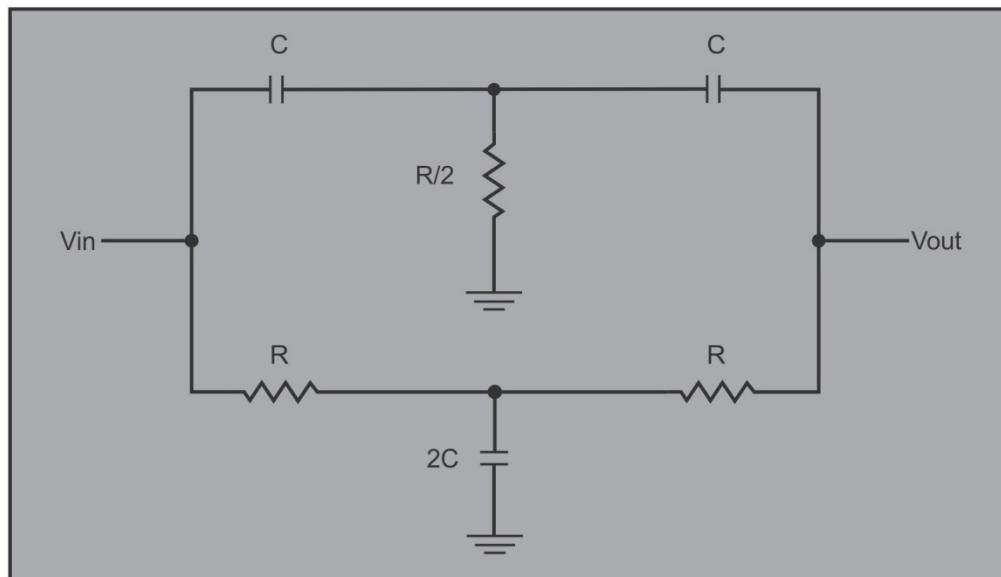


Fig 4.30 Passive Twin-T Filter

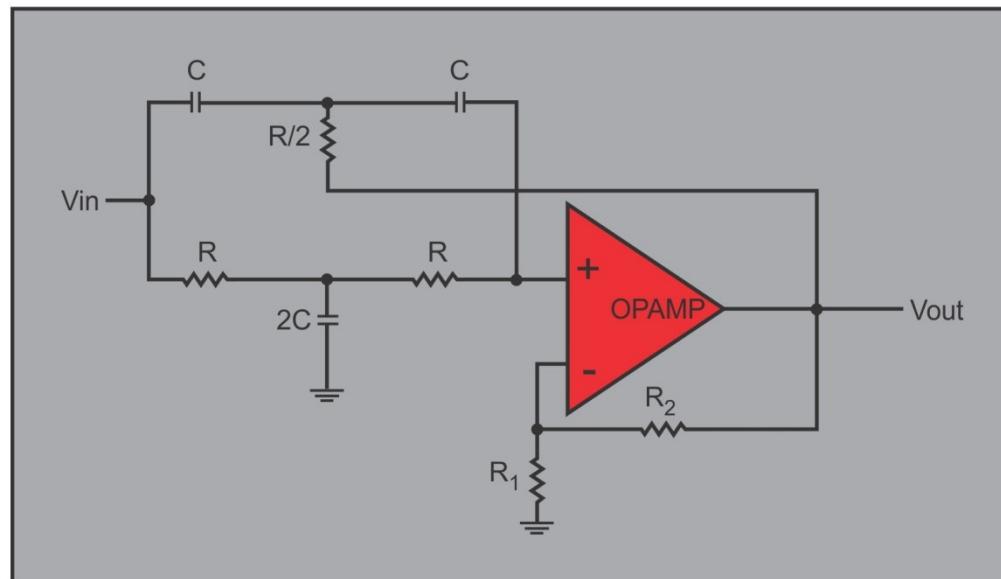


Fig 4.31 Active Twin-T Filter

The transfer function of the active twin-T filter is:

$$A(s) = \frac{k(1 + s^2)}{1 + 2(2 - k).s + s^2} \quad (4.40)$$

Comparing the variables of above A(s) equations it provides that to determine the filter parameters:

$$\text{Mid-frequency: } f_m = \frac{1}{2\pi RC}$$

$$\text{Inner gain: } G = 1 + \frac{R_2}{R_1}$$

$$\text{Pass band gain: } A_0 = G$$

$$\text{Rejection quality: } Q = \frac{1}{2(2 - G)}$$

The twin-T circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m). However, Q and A_m cannot be adjusted independently. To set the mid frequency of the band-pass, specify f_m and C, and then solve for $R = \frac{1}{2\pi f_m C}$

Because of the dependency between Q and A_m , there are two options to solve for R_2 : either to set the gain at mid frequency, $R_2 = (A_0 - 1).R_1$ or to design for a specific Q: $R_2 = R_1(1 - \frac{1}{2Q})$

4.10.2 Active Wien-Robinson Filter

The Wien-Robinson bridge in Figure 4.32 is a passive band-rejection filter with differential output. The output voltage is the difference between the potential of a constant voltage divider and the output of a band-pass filter. Its Q-factor is close to that of the twin-T circuit. To achieve higher values of Q, the filter is connected into the feedback loop of an amplifier.

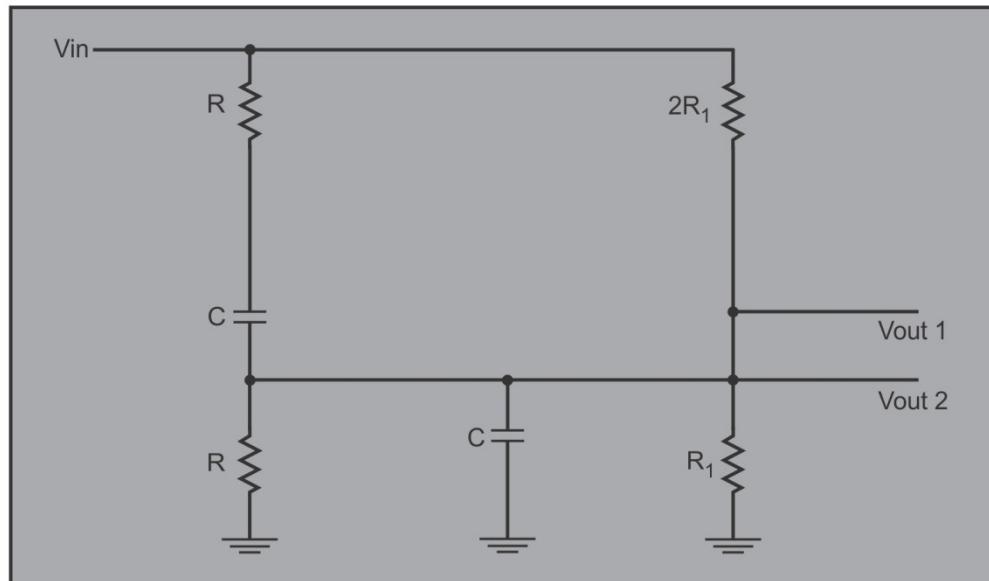


Fig 4.32 Passive Wien-Robinson Bridge

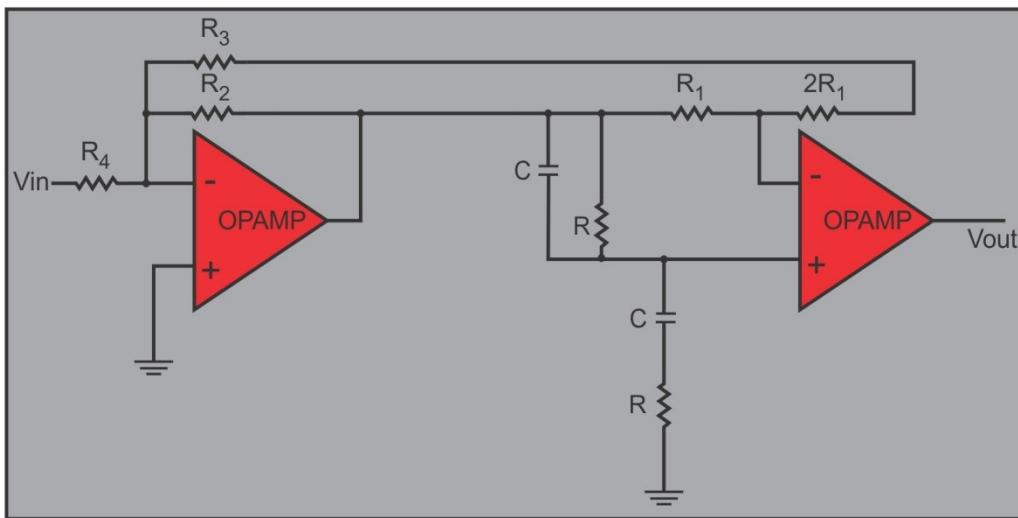


Fig 4.33 Active Wien-Robinson Filter

The active Wien-Robinson filter in Figure 4.33 has the transfer function:

$$A(s) = \frac{\frac{-\beta}{1+\alpha} (1 + s^2)}{1 + \frac{3}{1+\alpha} \cdot s + s^2} \quad (4.41)$$

$$\text{With } \alpha = \frac{R_2}{R_3} \text{ and } \beta = \frac{R_2}{R_4}$$

Comparing the variables of Equations A(S) provides the equations that determine the filter parameters:

$$\text{Mid-frequency: } f_m = \frac{1}{2\pi RC}$$

$$\text{Pass band gain: } A_0 = \frac{-\beta}{1 + \alpha}$$

$$\text{Rejection quality: } Q = \frac{1 + \alpha}{3}$$

The twin-T circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m). However, Q and A_m cannot be adjusted independently. To set the mid frequency of the band-pass, specify f_m and C, and then solve for $R = \frac{1}{2\pi f_m C}$

Because of the dependency between Q and A_m , there are two options to solve for R2: either to set the gain at mid frequency, $R_2 = (A_0 - 1) \cdot R_1$ or to design for a specific $R_2 = R_1 (1 - \frac{1}{2Q})$

In comparison to the twin-T circuit, the Wien-Robinson filter allows modification of the passband gain, A_0 , without affecting the quality factor, Q. If f_m is not completely suppressed due to component tolerances of R and C, a fine-tuning of the resistor $2R_2$ is required.

Figure 4.31 shows the circuit diagram and Simulation result of Band stop filter design- Chebyshev 2nd order using webbench simulation tool.

Name: Bandstop, Multiple Feedback, Chebyshev 1 dB **Part:** Ideal OpAmp **Order:** 2 **Number of stages:** 1

Gain: 1 V/V (0 dB) **Allowable Passband Ripple:** 1 dB **Passband Frequency:** 1 kHz **Corner Frequency Attenuation:** 0 dB

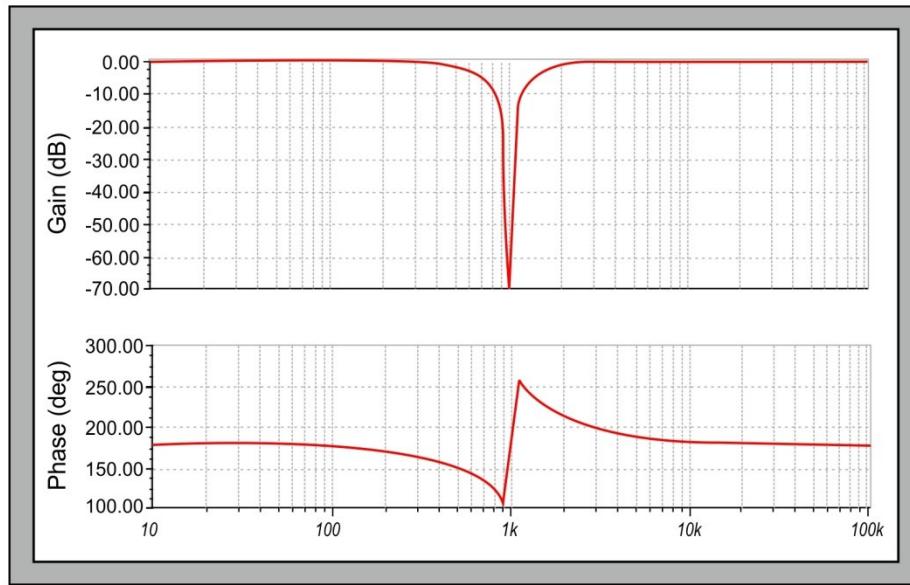
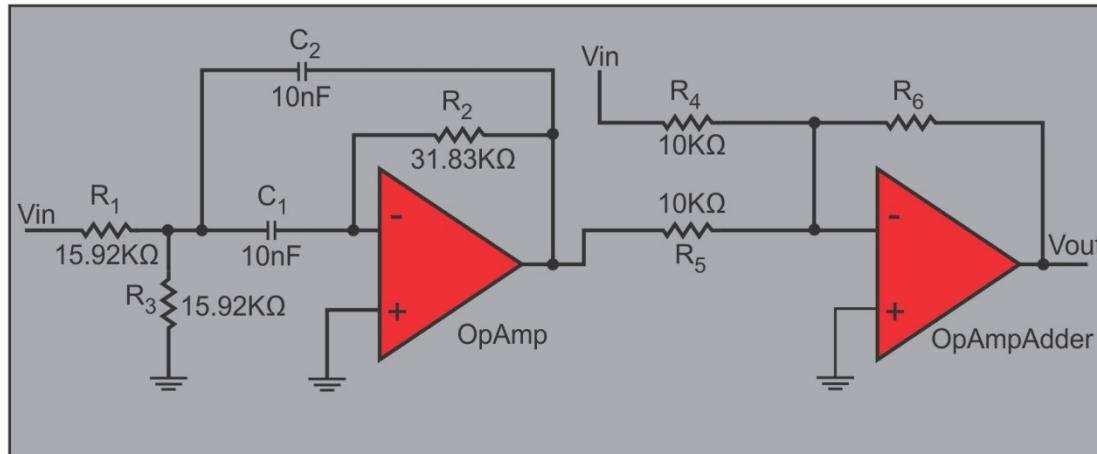


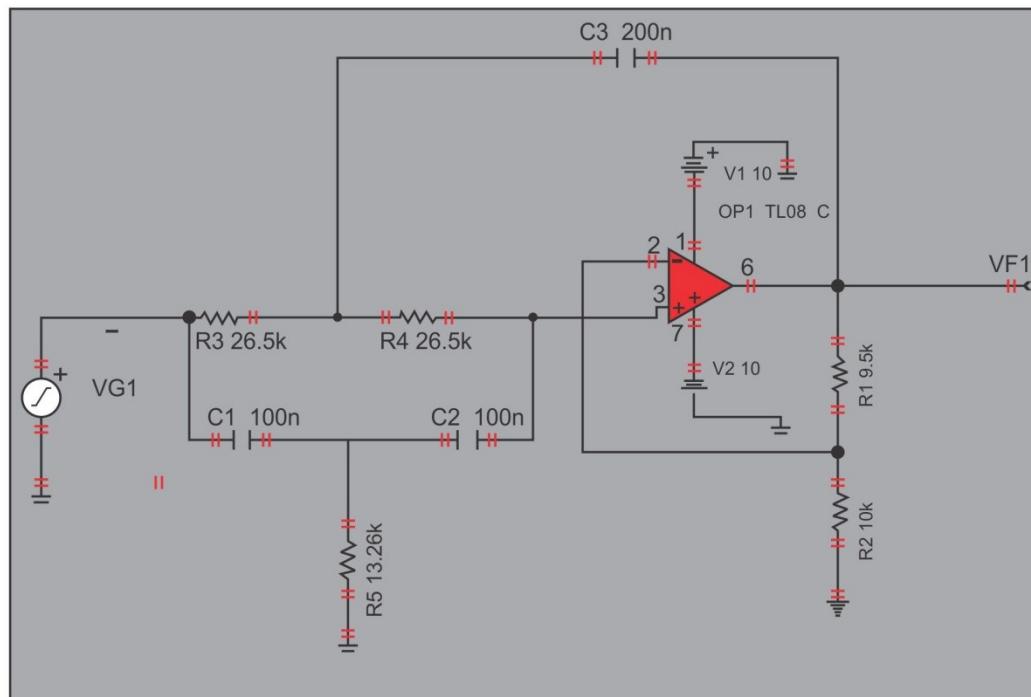
Fig 4.34 Circuit diagram and Simulation result of Band stop filter design - Chebyshev - 2nd order

Practical design example:

Design a second-order notch filter with $f_o = 60\text{Hz}$ and $BW = 5\text{Hz}$. What is the low- and high-frequency gain?

Solution:

Let $C=100\text{nF}$ and $2C=200\text{nF}$. Then, $R=1/(2\pi 60 \times 10^{-7})=26.53\text{k}\Omega$, and $R/2=13.26\text{k}\Omega$. Since $Q=60/5=12$, we get $2K=4-1/12$, or $K=47/24$, which represents the low- as well as the high frequency gain of the filter. Use $R_A=10.0\text{k}\Omega$ and $R_B=9.53\text{k}\Omega$.

Circuit diagram:


Simulation output:

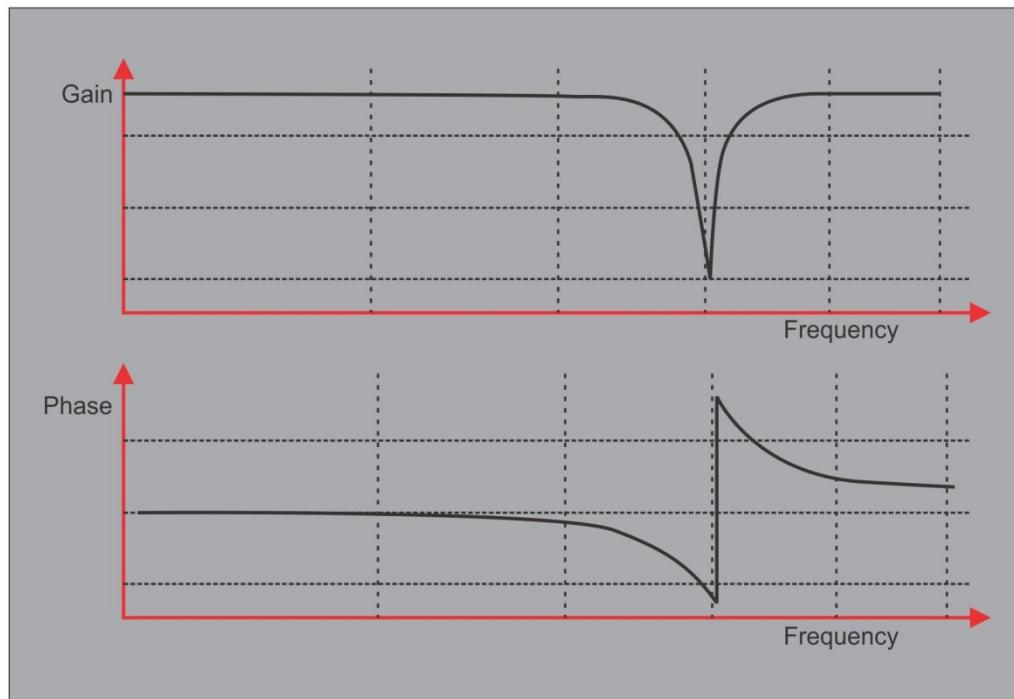


Fig 4.35: Circuit Diagram and Simulation result of second-order notch filter with $f_0 = 60$ Hz and BW = 5 Hz

14.11 All-Pass Filter Design

In comparison to the previously discussed filters, an all-pass filter has a constant gain across the entire frequency range, and a phase response that changes linearly with frequency. An all-pass filter is that which passes all frequency components of the input signal without attenuation but provides predictable phase shifts for different frequencies of the input signals. The all-pass filters are also called delay equalizers or phase correctors. Because of these properties, all-pass filters are used in phase compensation and signal delay circuits (Fig 4.36).

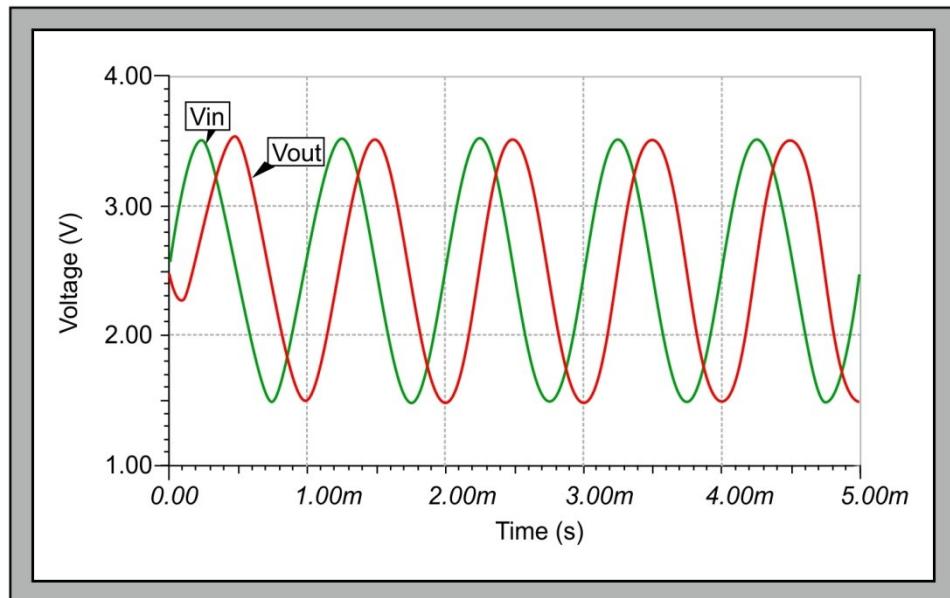


Fig 4.36: Input and Output Waveforms of All pass filters

Similar to the low-pass filters, all-pass circuits of higher order consist of cascaded first-order and second-order all-pass stages. To develop the all-pass transfer function from a low-pass response, replace A_0 with the conjugate complex denominator. The general transfer function of an all-pass is then:

$$A(s) = \frac{\prod_i (1 + a_i s + b_i s^2)}{\prod_i (1 + a_i s + b_i s^2)} \quad (4.42)$$

with a_i and b_i being the coefficients of a partial filter. Expressing above equation in magnitude and phase yields:

$$A(s) = \frac{\prod_i \sqrt{(1 + b_i \Omega^2)^2 + a_i^2 \Omega^2} \cdot e^{-j\alpha}}{\prod_i \sqrt{(1 + b_i \Omega^2)^2 + a_i^2 \Omega^2} \cdot e^{+j\alpha}} \quad (4.43)$$

This gives a constant gain of 1, and a phase shift Φ , of:

$$\phi = -2\alpha = -2 \sum_i \arctan \left(\frac{a_i \Omega}{1 + b_i \Omega^2} \right) \quad (4.44)$$

4.11.1 First-Order All-Pass Filter

Figure 4.37 shows a first-order all-pass filter with a gain of +1 at low frequencies and a gain of -1 at high frequencies. Therefore, the magnitude of the gain is 1, while the phase changes from 0° to -180°.

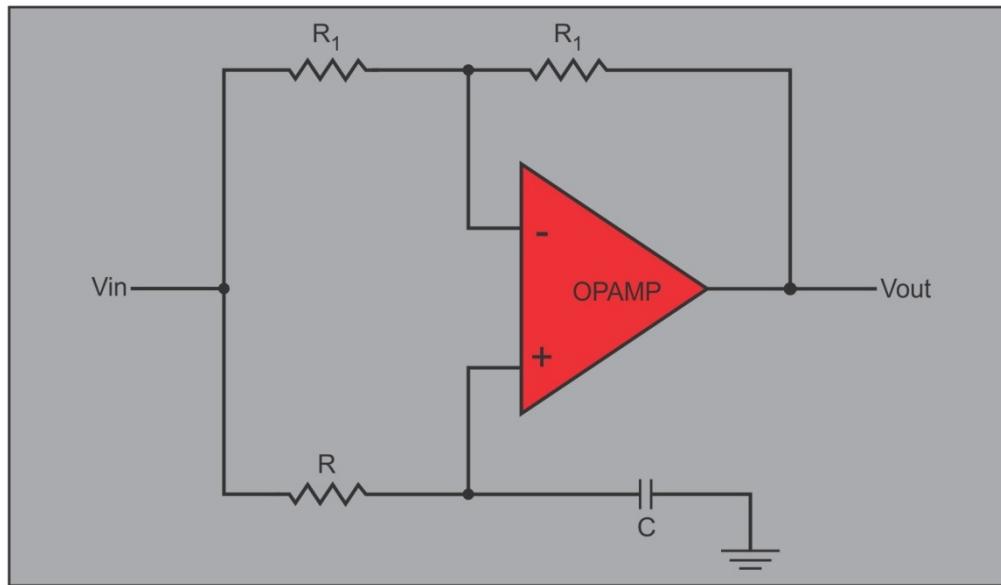


Fig 4.37 First-Order All-Passes

The transfer function of the circuit above is:

$$A(s) = \frac{1 - RC\omega_c \cdot s}{1 + RC\omega_c \cdot s} \quad (4.45)$$

On coefficient comparison (b1=1), results in, $a_i = RC \cdot 2\pi f_c$

To design a first-order all-pass, specify f_c and C and then solve for R , $R = \frac{a_i}{2\pi f_c \cdot C}$

Inserting above equations and substituting ω_c with Equation T_{gr} provides the maximum group delay of a first-order all-pass filter, $t_{gro} = 2RC$

4.11.2 Second-Order All-Pass Filter

Fig 4.38 shows that one possible design for a second-order all-pass filter is to subtract the output voltage of a second-order band-pass filter from its input voltage.

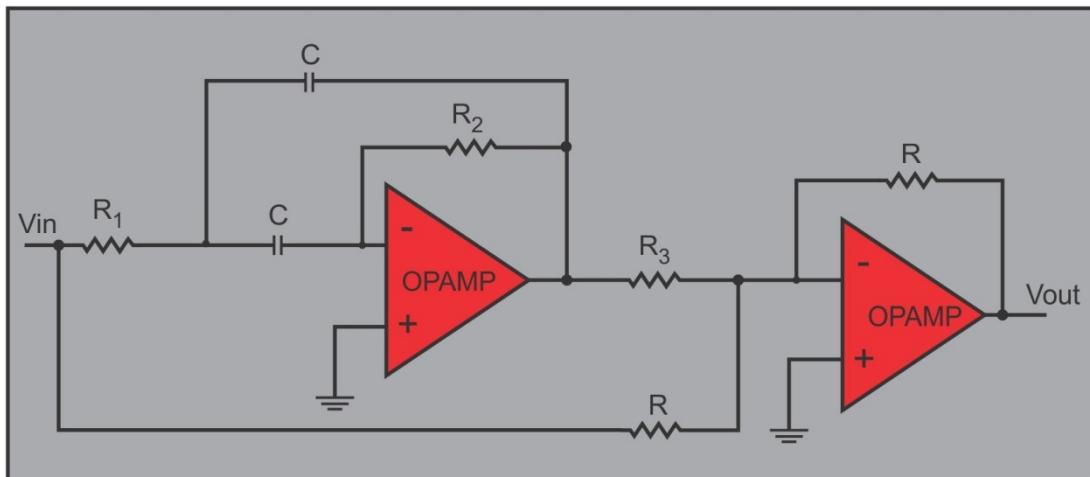


Fig 4.38 Second-Order All-Pass Filter

The transfer function of the circuit in Figure 4.34 is:

$$A(s) = \frac{1 + (2R_1 - \alpha R_2)C\omega_c \cdot s + R_1 R_2 C^2 \omega_c^2 s^2}{1 + 2R_1 C\omega_c \cdot s + R_1 R_2 C^2 \omega_c^2 s^2} \quad (4.46)$$

The coefficient comparison with Equation A(s) yields:

$$a_1 = 4\pi f_c R_1 C, \quad b_1 = a_1 \pi f_c R_2 C$$

$$\alpha = \frac{a_1^2}{b_1} = \frac{R}{R_3}$$

To design the circuit, specify f_c , C , and R , and then solve for the resistor values:

$$R_1 = \frac{a_1}{4\pi f_c \cdot C}, \quad R_2 = \frac{b_1}{a_1 \pi f_c \cdot C}, \quad R_3 = \frac{R}{\alpha}$$

Then maximum group delay of a second-order all-pass filter:

$$t_{gro} = 4R_1 C$$

4.11.3 Higher-Order All-Pass Filter

Higher-order all-pass filters consist of cascaded first-order and second-order filter stages. Example, Delay All-Pass Filter. A signal with the frequency spectrum, $0 < f < 1$ kHz, needs to be delayed by 2 ms. To keep the phase distortions at a minimum, the corner frequency of the all-pass filter must be $f_c \geq 1$ kHz. Equation Tgr determines the normalized group delay for frequencies below 1 kHz:

$$T_{gr0} = \frac{t_{gro}}{T_c} = 2ms \cdot 1KHz = 2$$

Figure 4.39 confirms that a seventh-order all-pass is needed to accomplish the desired delay. The exact value, however, is $T_{gr0} = 2.1737$. To set the group delay to precisely 2 ms, solve Equation T_{gr} for f_c and obtain the corner frequency:

$$f_c = \frac{T_{gr0}}{t_{gr0}} = 1.087 \text{ KHz}$$

To complete the design, look up the filter coefficients for a seventh-order all-pass filter, specify C, and calculate the resistor values for each partial filter. Cascading the first-order all-pass with the three second-order stages results in the desired seventh-order all-pass filter.

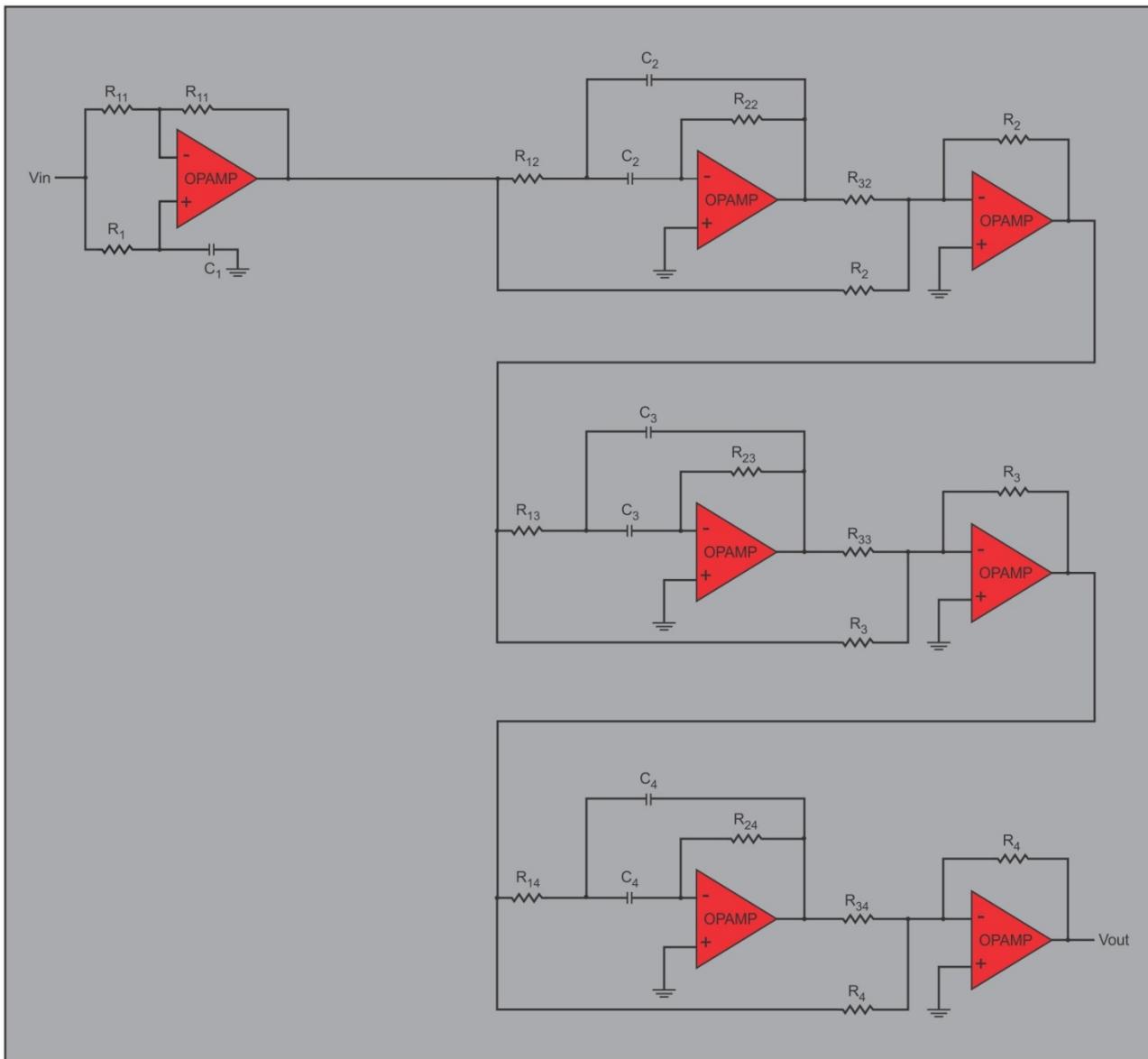


Fig 4.39 Seventh-Order All-Pass Filter

Figure 4.40 shows the circuit diagram and Simulation result of All pass filter design- bessel- 2nd order using webbench simulation tool.

Name: Allpass, Multiple Feedback, Chebyshev 1 dB **Part:** Ideal OpAmp **Order:** 2 **Number of stages:** 1

Gain: 1 V/V (0 dB) **Allowable Passband Ripple:** 1 dB **Passband Frequency:** 1 kHz **Corner Frequency Attenuation:** -3 dB
Time Delay: 175us **Phase Shift:** -63 (or 117) degrees

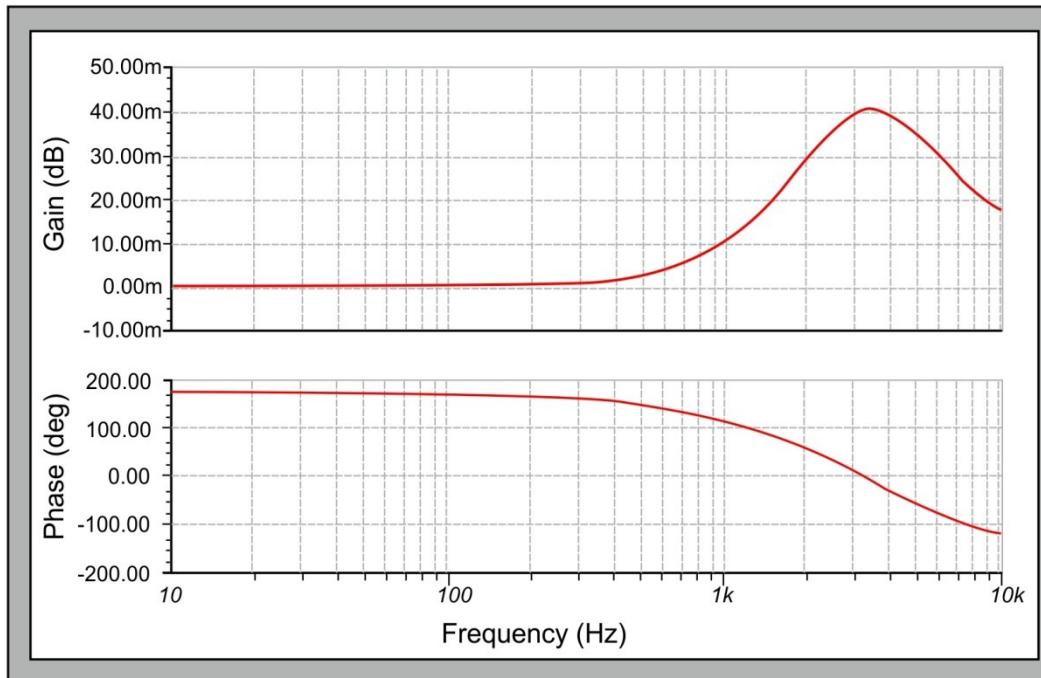
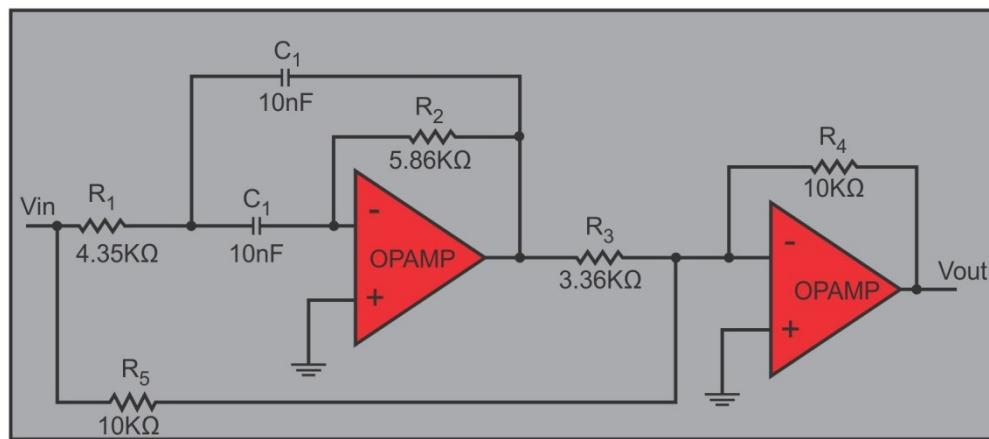


Fig 4.40 circuit diagram and Simulation result of All pass filter design- Bessel - 2nd order

4.12 Self -tuned Filters

In a self-tuned filter output frequency is tuned according to input frequency automatically. The idea of self-tuned filter is to adjust the RC time constants of the filter so that in-phase response of a Low Pass filter, the output phase with respect to input is exactly 90° at the incoming frequency. This principle is utilized in distortion analyzers and spectrum analyzers.

In order to design self-tuned filters, the main building block is the analog multiplier. The output of the multiplier when two sinusoidal waveforms are multiplied is shown in Fig 4.41. Note that the output of the multiplier depends on the phase difference between the two inputs and can, therefore, be used as a measure of the phase difference.

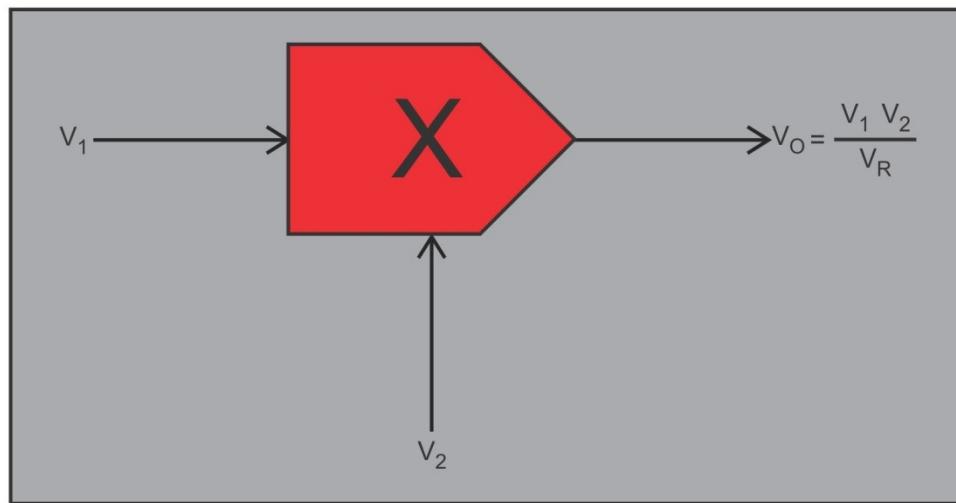


Fig 4.41 Multiplier and its output

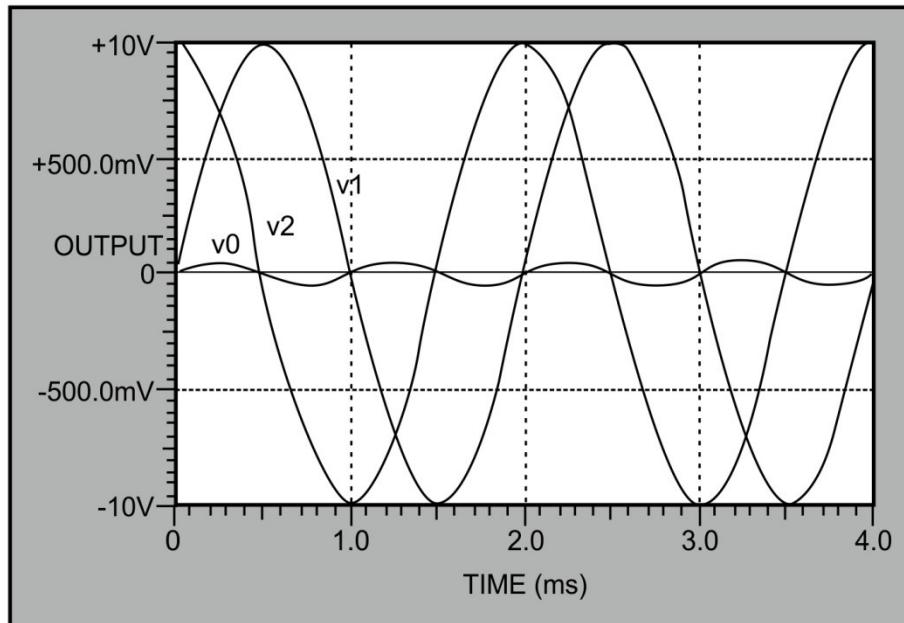


Fig 4.42 Multiplier as a phase detector

The multiplier output will be,

$$V_o = V_{offset} + K_x \times V_x + K_y \times V_y + K_o \times V_x \times V_y + \xi$$

where ξ is a non-linear term in V_x and V_y . K_x and K_y are called feed-through components and K_o is called the normalizing component. We define, $V_r = (1/K_0)$. For a precision multiplier, $V_r \leq V_x$ and $V_y \leq V_r$, where V_r is the parameter defined above. Hence, for precision amplifiers, $V_o = V_x \times V_y / V_r$.

On replacing the integrator with multiplier followed by integrator, the circuit becomes a Voltage Controlled Filter (or voltage Controlled Phase Generator) shown in Fig 4.43 and Fig 4.44.

This forms the basic circuit for tuned filter as in Fig 4.45. The output of the self-tuned filter for a square-wave input, including the control voltage waveform, is shown in Fig 4.47. The figure brings out the aspect automatic control and self-tuning.

A simpler version of the voltage controlled phase generator, which can be part a self-tuned filter, is shown in Fig 4.46.

4.12.1 Multiplier as a Phase Detector

In the circuit of Figure 4.37, assume that

$$V_x = V_p \sin(\omega t)$$

$$V_y = V_p \sin(\omega t + \varphi)$$

Then the output of the multiplier is,

$$V_o = \frac{V_p V_p'}{2V_r} [\cos\phi - \cos(\omega t + \phi)] \quad (4.47)$$

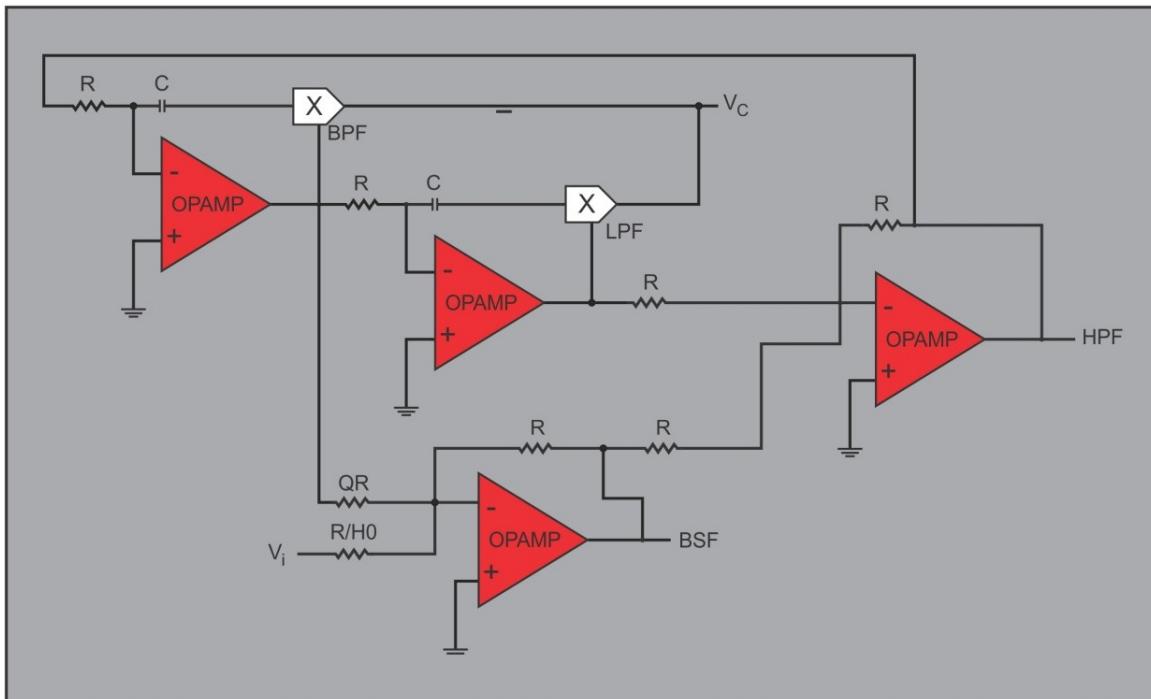


Fig 4.43 Voltage controlled filter with frequency $\propto (1 / V_c)$

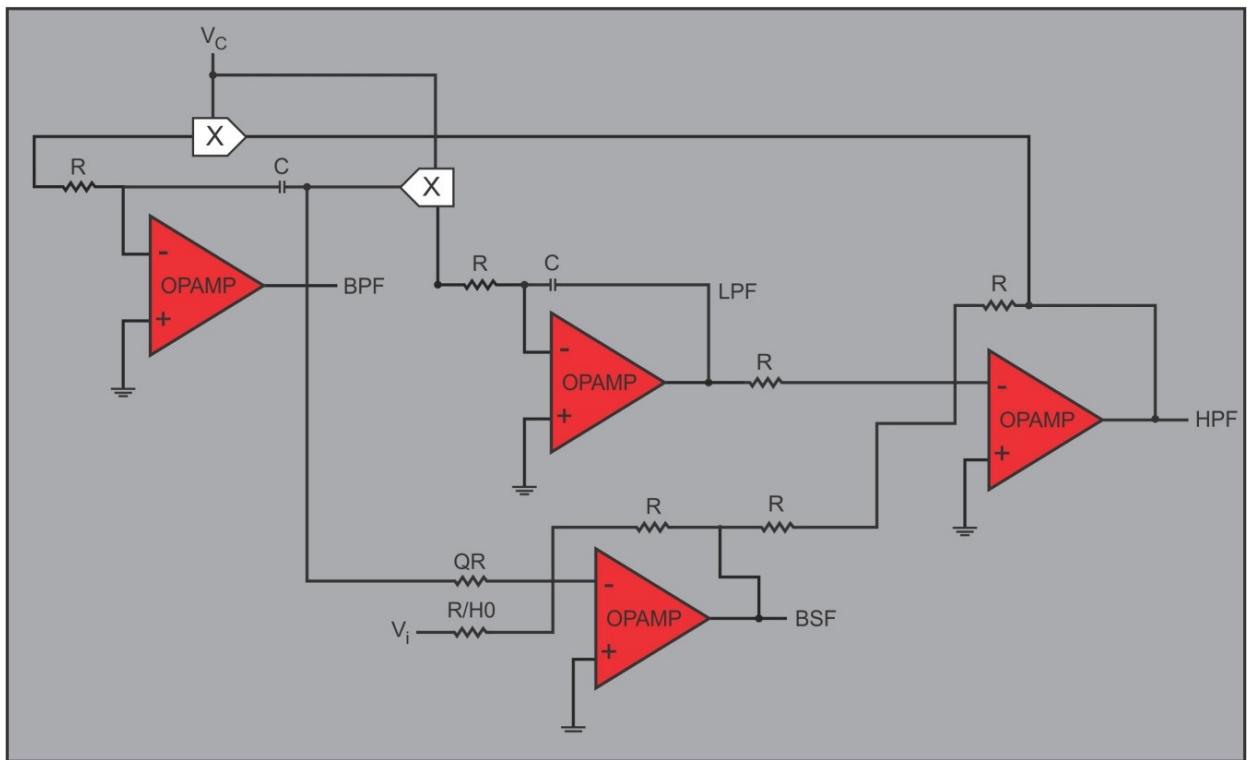


Fig 4.44 Voltage controlled filter with frequency $\propto V_C$

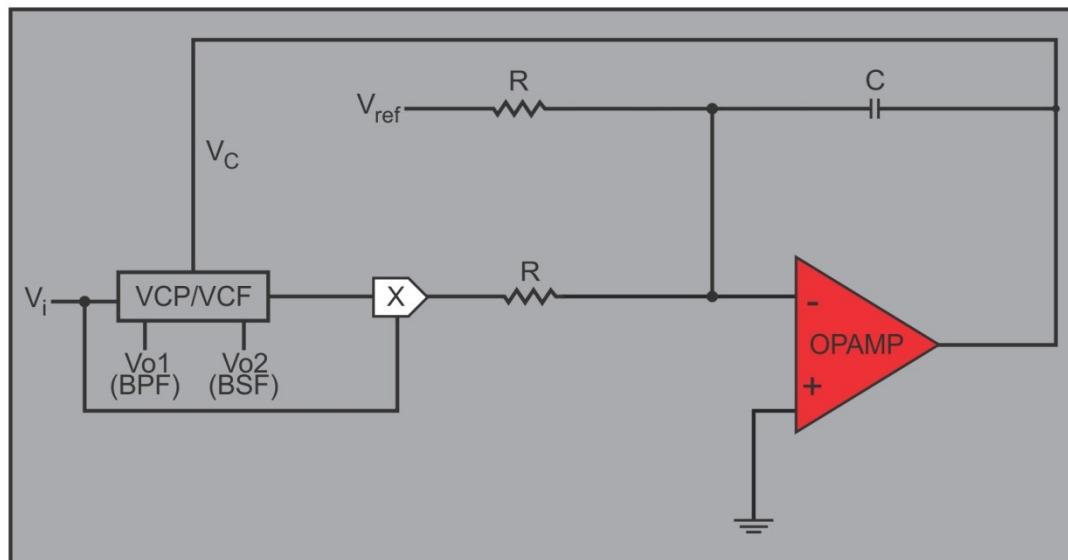


Fig 4.45 A self-tuned filter based on a voltage controlled filter or voltage controlled phase generator

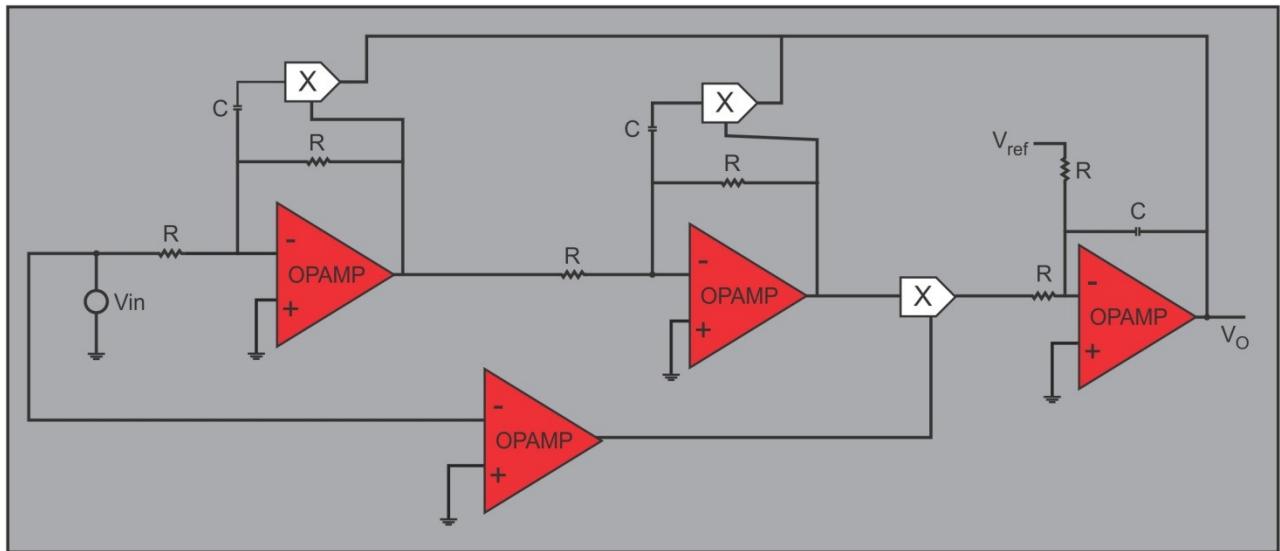


Fig 4.46 A simple voltage-controlled phase generator that can become part of a self-tuned filter

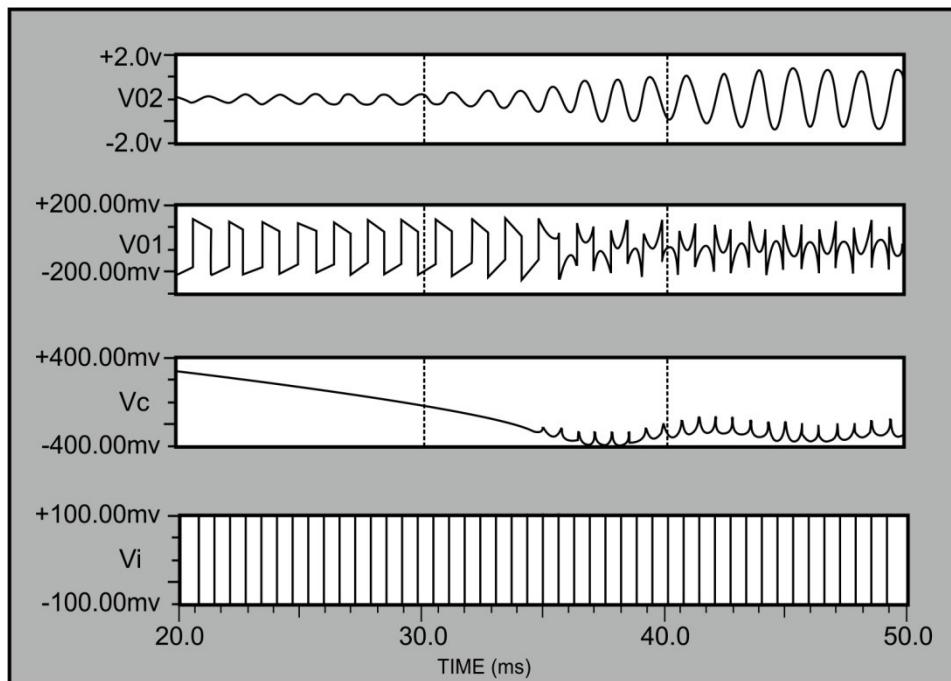


Figure 4.47 Output of the self-tuned filter based on simulation. V01 correspond to BPF, V02 corresponds to BSG, V_c is the control voltage and V_i is the input voltage

After passing through the LPF, the high frequency component gets filtered out and only the average value of output V_{av} remains.

$$V_{av} = \frac{V_p V'_p}{2V_r} \cos \phi$$

$$K_{pd} = \frac{dV_{av}}{d\phi}$$

K_{pd} is called the phase detector sensitivity and is measured in Volts/radians. For $\phi=90^\circ$, V_{av} becomes 0. This information is used to tune the voltage-controlled filter (VCF) automatically. ω_0 of the VCF is given by

$$\omega_0 = \frac{V_r}{V_c \cdot RC} \quad (4.48)$$

Therefore,

$$\frac{d\omega_0}{dV_c} = \frac{-V_r}{V_c^2 \cdot RC} = \frac{\omega_0}{V_c}$$

The sensitivity of VCF is $\frac{d\phi}{dV_c}$ radians/sec/Volts. Now,

$$\frac{d\phi}{dV_c} = \frac{d\phi}{d\omega_0} \cdot \frac{d\omega_0}{dV_c}$$

If we consider the low pass output, then

$$\frac{V_0}{V_i} = \frac{+H_0}{\left(1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}\right)} \quad (4.49)$$

$$\phi = \tan^{-1} \left[\frac{\left(\frac{\omega_r}{\omega_0 Q}\right)}{\left(1 - \frac{\omega_r}{\omega_0}\right)^2} \right] \quad (4.50)$$

$$\frac{d\phi}{d\omega_0} = 2Q/\omega_0$$

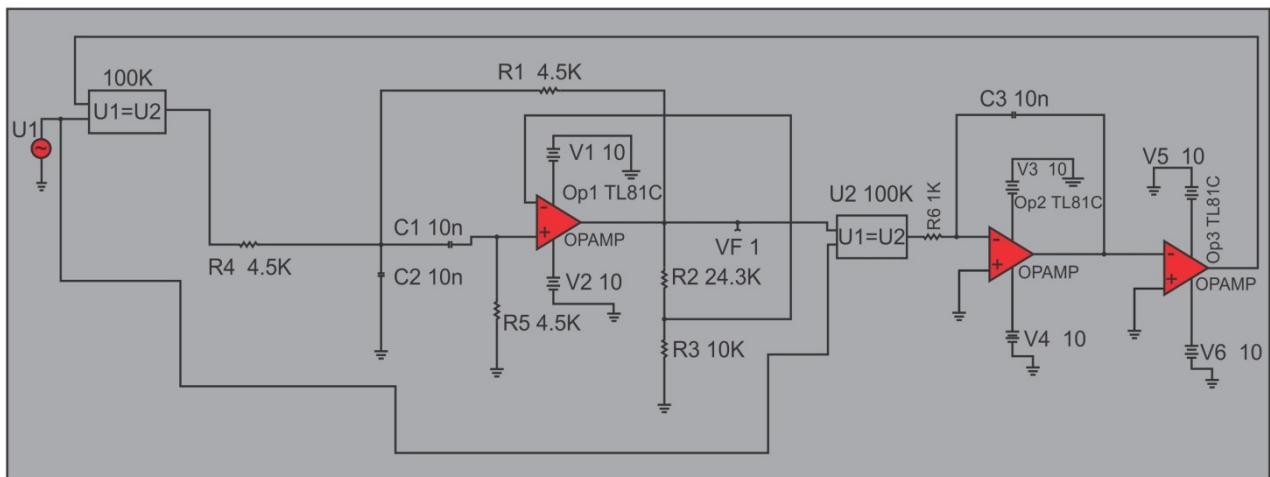
Hence, sensitivity of VCF (K_{VCF}) is equal to $\frac{d\phi}{dV_c} = -\frac{2Q}{V_c}$. For varying input frequency the output phase will always lock to the input phase with 90° phase difference between the two if $V_{av}=0$.

Practical Design Example:

Design a self-tuned band pass filter such that its output frequency follows the input frequency. Use a band pass filter whose center frequency is 5 KHz. For the input frequency of (a) 10 KHz, (b) 25 KHz (c) 50 KHz get the simulation results.

Solution: No solution

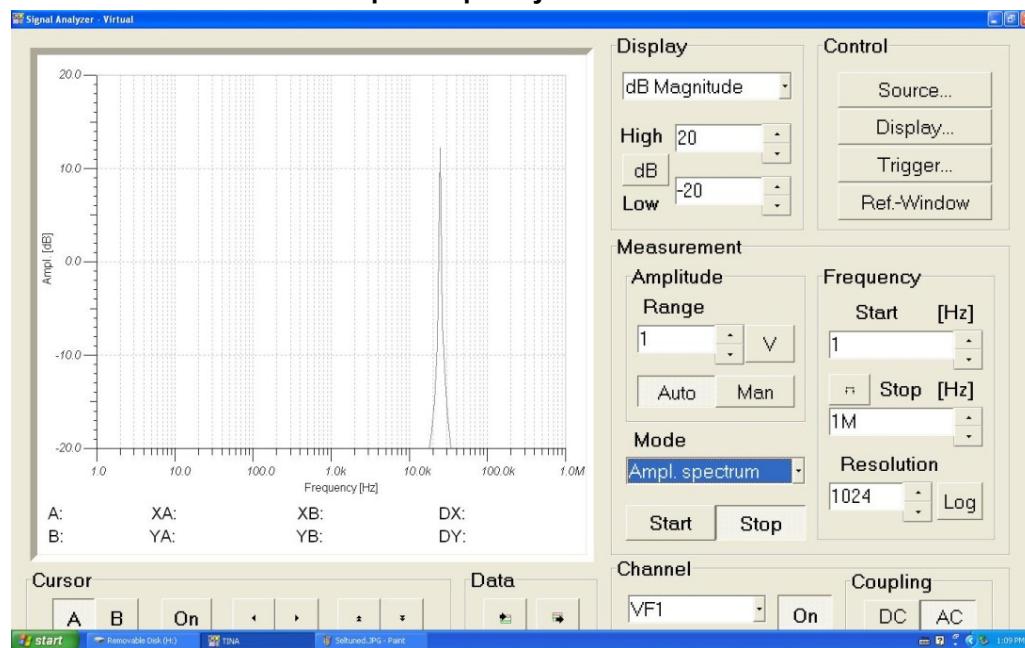
Circuit diagram

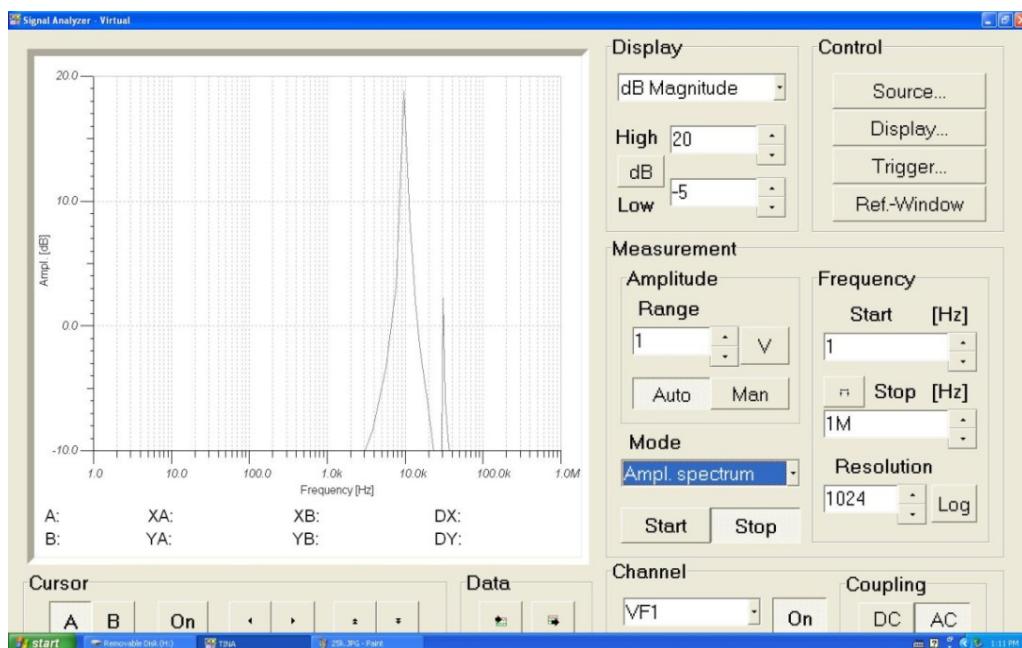
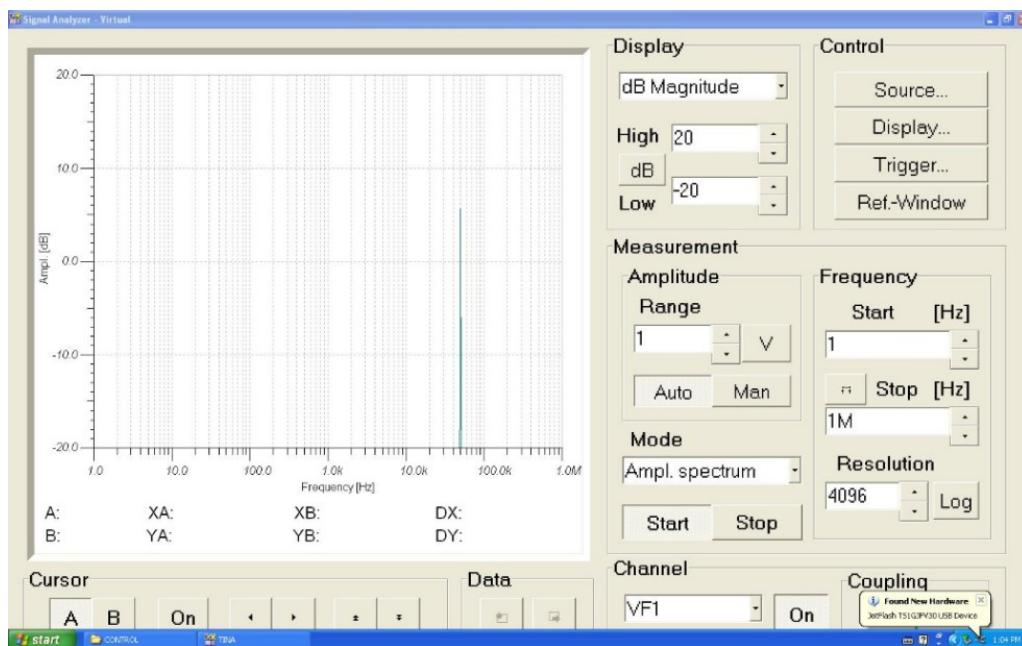


Simulation output:

The output gain responses for various input frequencies are given below and it can be seen that gain is maximum at the particular input frequency.

Input frequency = 10KHz



Input frequency = 25KHz

Input frequency = 50KHz


4.13 Summary

Electric filters are used in circuits which require the specification of signals according to their frequencies. Filters are widely used in communication and signal processing and in one form or other in almost all sophisticated electronic instruments. Such filters can be built from i) passive RLC Components ii) crystals iii) resistors, capacitors and op-amps. This Chapter dealt with the filter design using operational amplifier (Active filters). The basic principles of all types of filter design with as little mathematics as possible, leaning on the power of the SPICE –Electronic design software to explore filter performance.

An operational amplifier in the open loop configuration operates in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. The above applications will be dealt in the next chapter.

Points to Remember:

- Filter is a device or process that removes unwanted components or features from a transmitted signal
- An ideal filter is a network that allows signals of only certain frequencies to pass while blocking all others.
- Cutoff frequency, Transition band, Quality factor Q and the order of a filter are the main characteristics of filter.
- Filters can also be classified as passive and active filters.
- Active filters have more advantages over passive filters.
- The characteristic of a filter is described by its frequency response which consists of both a magnitude and a phase response.
- Low pass filter is a filter that passes the lower frequencies and rejects those at higher frequencies
- Butterworth filter is also called as maximally flat or flat filter.
- High pass filter is a filter that passes the higher frequencies and rejects those at lower frequencies
- The simplest design of a band-pass filter is the connection of a high-pass filter and a lowpass filter in series.
- Chebyshev filters are analog or digital filters having a steeper roll-off and more passband ripple (type I) or stop band ripple (type II) than Butterworth filters.
- Band Rejection filter rejects a band of frequencies, while passing all others.
- All-pass filter has a constant gain across the entire frequency range, and a phase response that changes linearly with frequency.
- Self tuned filter is a filter whose output frequency is tuned according to input frequency automatically.

4.14 Review Questions

1. Discuss the effect of order of the filter on frequency response

As the filter order increases, the transition from the pass band to the stop band gets steeper i.e., it will approach ideal filter frequency response.

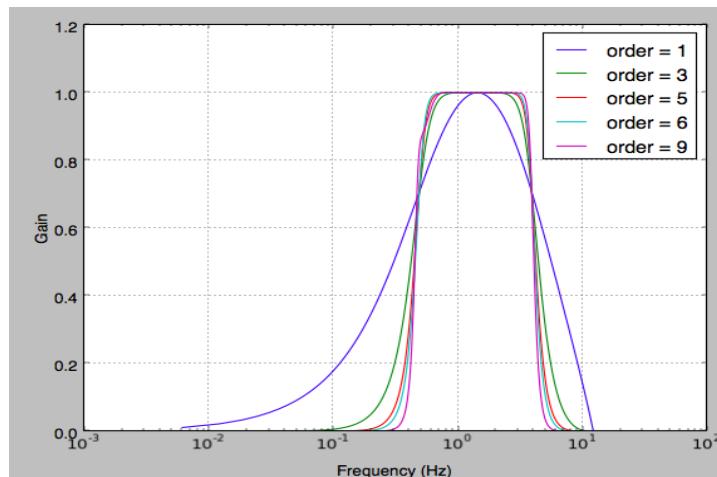


Fig.4.48. Effects of the filter order on the frequency response

2. How will you vary Q factor of the frequency response

The quality factor (Q) can be varied via the inner gain (G) without modifying the center frequency.

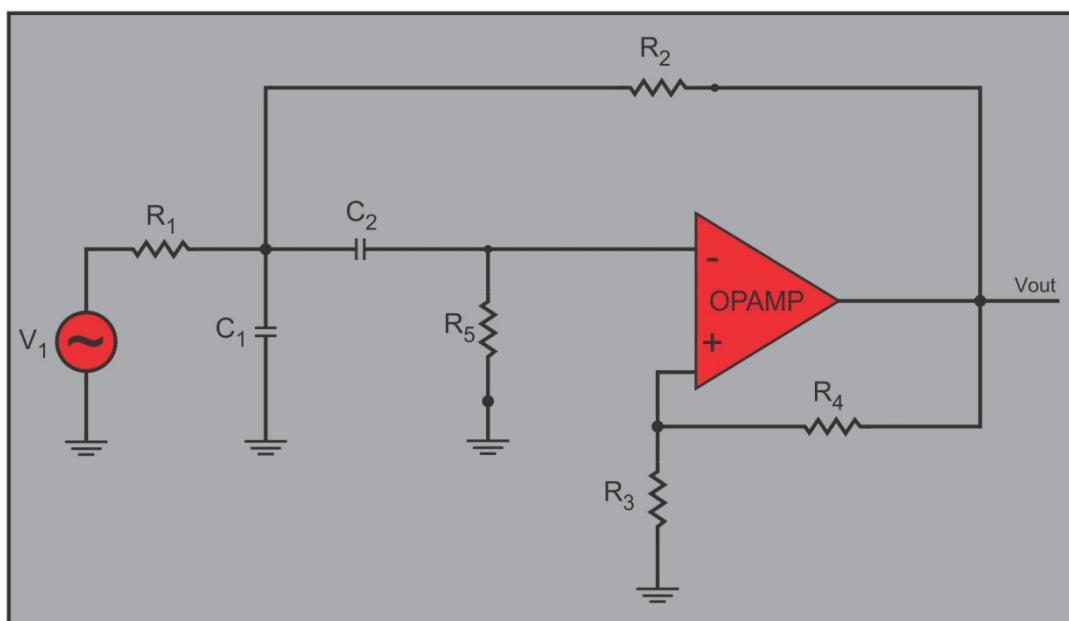


Fig.4.49. Second order Butterworth Band pass filter

The transfer function of the second order Sallen-Key band pass filter in Fig. 2 is:

$$H(s) = \frac{SC_2R_2R_5G}{S^2C_1C_2R_1R_2R_5 + S(C_2R_2R_5(1 - G) + C_2R_1R_5 + C_2R_1R_2 + C_1R_1R_2) + R_1 + R_2}$$

The above equation can be simplified by setting $R_1 = R_2 = R$, $R_5 = 2R$, $C_1 = C_2 = C$ this is known as the equal component Sallen-Key band-pass filter. Then,

$$H(s) = \frac{SCRG}{S^2C^2R^2 + SCR(3 - G) + 1}$$

Here, Quality factor: $Q = 1/(3-G)$; From above equation it can be seen that the quality factor is governed by the term G (op-amp gain). Hence, the quality factor (Q) can be varied via the inner gain (G) without modifying the center frequency. The Quality factor can be varied by varying the gain G through the resistor R4 or R3. If R3 is chosen to be constant at 10k, while R4 is chosen as the resistor to be varied. Thus, the different values of Q will be obtained for $R_4 = 10k, 16k, 17.5k, 18.75k, 19k, 19.9k$ from the table below:

Values of R4 and respective Q values

R_4 ($k\Omega$)	10	16	17.5	18.75	19	19.9
Q	1.0	2.5	4	8	10	100

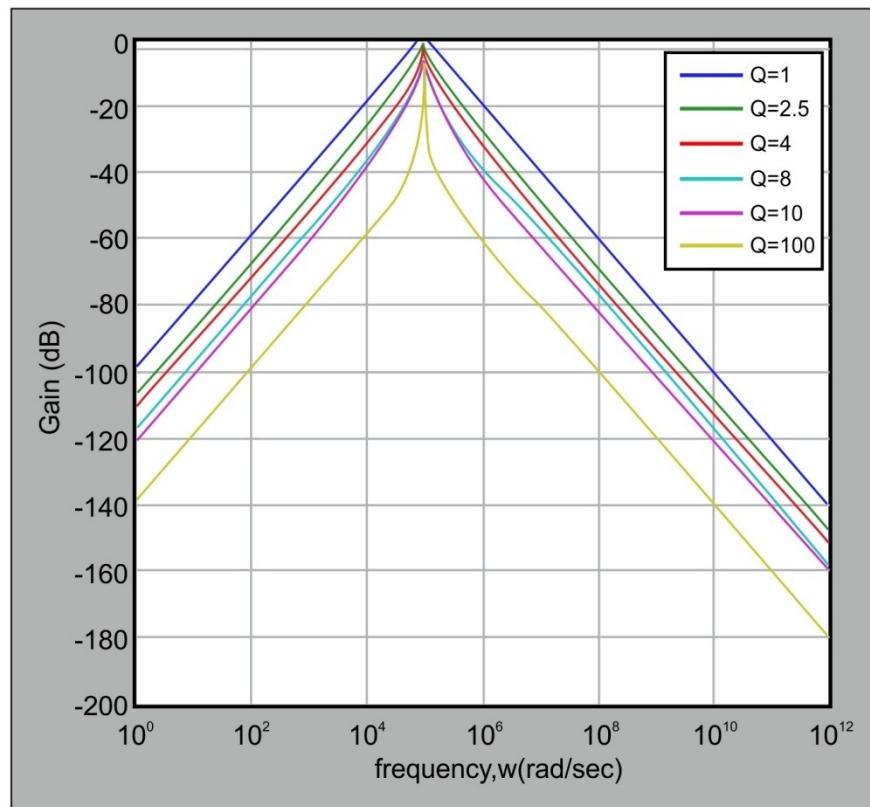


Fig 4.50 Frequency response for various Q values

3. Discuss the need for going to Sallen Key circuit:

Sallen key topology is widely used for its simplicity. One reason for this popularity is that this configuration shows the least dependence of filter performance on the performance of the op amp. This is because the op amp is configured as an amplifier, as opposed to an integrator, which

minimizes the gain-bandwidth requirements of the op amp. This infers that for a given op amp, one can design a higher frequency filter than with other topologies since the op amp gain-bandwidth product does not limit the performance of the filter as it would if it were configured as an integrator. In addition, since the op amp is configured as an amplifier, current feedback amplifiers, which cannot be configured as conventional integrators, can be used. This allows slightly more bandwidth from the filter. The signal phase through the filter is maintained (non-inverting configuration). Another advantage of this configuration is that the ratio of the largest resistor value to the smallest resistor value, and the ratio of the largest capacitor value to the smallest capacitor value (component spread) are low, which is beneficial for manufacturability. The frequency and Q terms are somewhat independent, but they are very sensitive to the gain parameter. The Sallen-Key is very Q-sensitive to element values, especially for high Q sections.

4. Explain the effect of supply frequency interference while amplifying sensor signals

Supply frequency interference causes the output information (embedded in the period/frequency, duty cycle or another time ratio of the output signal) to have uncertainty that limits the system resolution. The uncertainty of the output information depends on the frequency and the amplitude of the interference superimposed on the supply voltage.

5. Suggest a method for adjusting the Q factor of the frequency response of the notch filter

The twin-T circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m). However, Q and A_m cannot be adjusted independently.

To set the mid frequency of the band-pass, specify f_m and C, and then solve for, $R = \frac{1}{2\pi f_m C}$

Because of the dependency between Q and A_m , there are two options to solve for R_2 : either to set the gain at mid frequency, $R_2 = (A_0 - 1)R_1$ or to design for a specific Q, $R_2 = R_1 \left(1 - \frac{1}{2Q}\right)$

6. What is the purpose of going for Twin T notch filter circuit?

- The twin-T topology notch filter has a major advantage that it can be implemented with a single op amp.
- The twin-T circuit has another advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m).

7. Discuss the effect of the harmonics when a square wave is applied to the filter

When a square wave is applied to the filter, the harmonics will eliminate the sensitivity of phase detector to the amplitude changes as well as VCO frequency.

8. Determine the lock range of self-tuned filter

The range of frequencies from $f_i = f_{\min}$ to $f_i = f_{\max}$ where the closed loop system remains in the locked condition is called the lock range and it can be measured as $f_{\max} - f_{\min}$. If the closed loop is initially locked, and f_i becomes smaller than f_{\min} or if f_i exceeds f_{\max} , the closed loop fails to keep f_{osc} equal to f_i , and then it becomes unlocked.

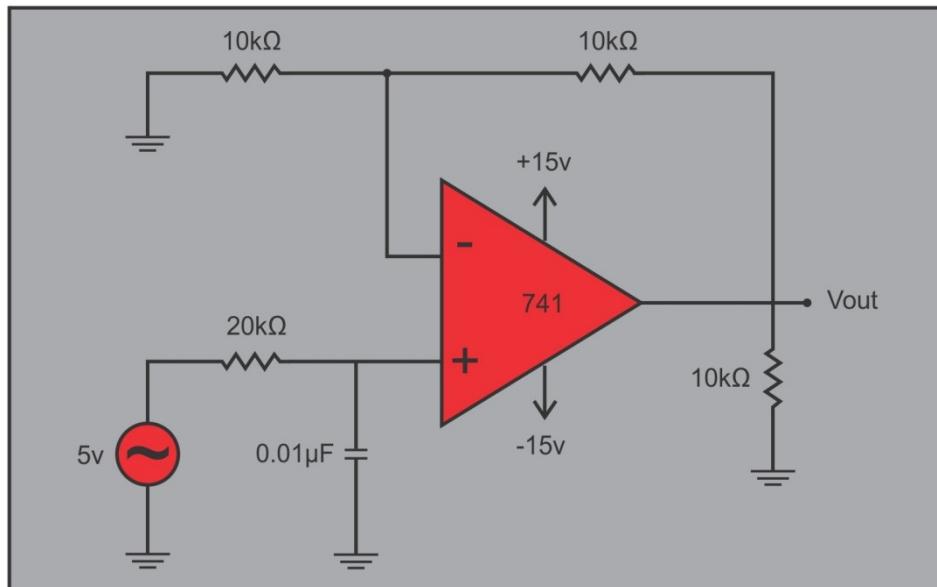
4.15 Exercises

1. Given the lower and higher cut-off frequency of a band-pass filter are 2.5kHz and 10kHz. Determine its bandwidth.

Answer:

Bandwidth of a band-pass filter is Bandwidth= $f_H - f_L$
 $= 10 \text{ kHz} - 2.5 \text{ kHz} = 7.5 \text{ kHz} = 7500 \text{ Hz}$.

2. Compute the pass band gain and high cut-off frequency for the first order high pass filter.



Answer:

The pass band gain of the filter, $A_F = 1 + (R_F/R_1)$
 $A_F = 1 + (10k\Omega/10k\Omega) = 2$. The high cut-off frequency of the filter, $f_H = 1/2\pi R C$
 $= 1/(2\pi \times 20k\Omega \times 0.01\mu F) = 1/1.256 \times 10^{-3} = 796.18 \text{ Hz}$.

3. Find the High cut-off frequency if the pass band gain of a filter is 10.

Answer:

High cut-off frequency of a filter, $f_H = 0.707 \times A_F = 0.707 \times 10$
 $f_H = 7.07 \text{ Hz}$.

4. Design a low pass filter at a cut-off frequency 1.6Hz with a pass band gain of 2.

Answer:

Assume, $C = 0.01\mu F$

Given, $f_H = 1 \text{ kHz}$,

$$R = 1/(2\pi f_H C) = 1/2\pi \times 0.01\mu F \times 1 \text{ kHz}$$

$R = 9.9k\Omega \cong 10k\Omega$. Since the pass band gain is 2.

$2 = 1 + (R_F/R_1)$. Therefore, R_F and R_1 must be equal.

5. Find the gain and phase angle of the second order low pass filter? Where pass band gain of the filter is 5, frequency and the high cut-off frequency of the filter are 3000Hz and 1kHz.

Answer:

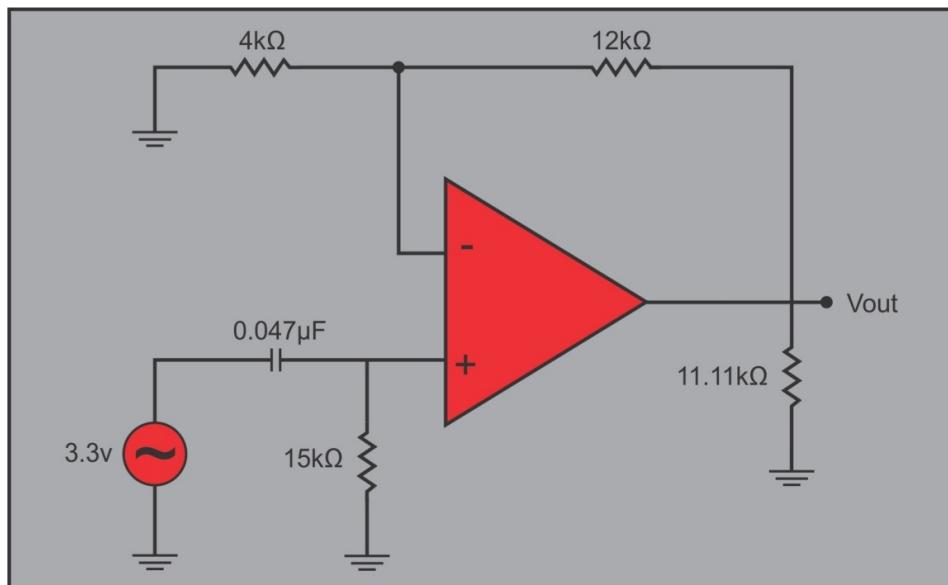
The gain of the second order low pass filter,

$$[V_o/V_{in}] = A_F / \sqrt{1 + (f/f_h)^2} = 5 / \sqrt{1 + (3000/1000)^4} = 5/9.055 = 0.55.$$

$$[V_o/V_{in}] = 20\log(0.55ss) = -5.19\text{dB}.$$

Phase angle of second order low pass filter is given as $\phi = \tan^{-1}(f/f_h)$
 $\Rightarrow \phi = 71.56^\circ$.

6. Compute the voltage gain for the following circuit with input frequency 1.5kHz.



Answer:

$$\begin{aligned}|V_o/V_{in}| &= [A_F \times (f/f_L)] / [\sqrt{1 + (f/f_L)^2}] = [4 \times (1.5\text{kHz}/225.86)] / \sqrt{1 + (1.5\text{kHz}/225.86)^2} \\ &= 26.56/6.716 = 3.955 = 20\log(3.955) = 11.9.\end{aligned}$$

$$|V_o/V_{in}| \approx 12 \text{ dB}$$

$$A_F = 1 + (R_F/R_1) = 1 + (12\text{k}\Omega/4\text{k}\Omega) = 4.$$

$$f_L = 1/(2\pi RC) = 1/2\pi \times 15\text{k}\Omega \times 0.047\mu\text{F} = 1/4.427 \times 10^{-3} = 225.86\text{Hz}.$$

7. The internal resistor of the second order high pass filter is equal to 10kΩ.
 Find the value of feedback resistor?

Answer:

Pass band gain for second order butterworth response, $A_F = 1.586$.

$$\Rightarrow A_F = [1 + (R_F/R_1)]$$

$$\Rightarrow R_F = (A_F - 1) \times R_1 = (1.586 - 1) \times 10\text{k}\Omega = 5.86\text{k}\Omega.$$

8. Determine voltage gain of second order high pass butterworth filter.
 Specifications $R_3 = R_2 = 33\Omega$, $f = 250\text{Hz}$ and $f_L = 1\text{kHz}$.

Answer:

Since $R_3 = R_2$

$$C_2 = 1/(2\pi \times f_L \times R_2) = 1/(2\pi \times 1\text{kHz} \times 33\Omega)$$

$$\Rightarrow C_3 = C_2 = 4.82\mu\text{F}.$$

$$\text{Voltage gain of filter } |V_o/V_{in}| = A_F / [\sqrt{1 + (f_L/f)^4}] = 1.586 / [1 + (1\text{kHz}/250\text{Hz})^4]$$

$$=1.586/252=6.17 \times 10^{-3} = 20\log(6.17 \times 10^{-3}) = -44.19 \text{ dB.}$$

- 9. From the given specifications, determine the value of voltage gain magnitude of first order and second order high pass butterworth filter?**

Pass band voltage gain=2;
Low cut-off frequency= 1kHz;
Input frequency=500Hz.

Answer:

For first order high pass filter,

$$|V_O/V_{in}| = A_F \times (f/f_L) / [\sqrt{1+(f/f_L)^2}] = (2 \times (500 \text{ Hz} / 1 \text{ kHz})) / \sqrt{[1+(500 \text{ Hz} / 1 \text{ kHz})^2]} \\ \Rightarrow |V_O/V_{in}| = 1/1.118 = 0.8944 = 20\log(0.8944) = -0.9686 \text{ dB.}$$

For second order high pass filter,

$$|V_O/V_{in}| = A_F / [\sqrt{1+(f_L/f)^4}] = 2 / \sqrt{[1+(1 \text{ kHz} / 500 \text{ Hz})^2]} \\ \Rightarrow |V_O/V_{in}| = 2/4.123 = 0.4851 = 20\log(0.4851) = -6.28 \text{ dB.}$$

- 10. Find the voltage gain magnitude of the wide band-pass filter where total pass band gain is=6, input frequency = 750Hz, Low cut-off frequency =200Hz and high cut-off frequency= 1 kHz.**

Answer:

Voltage gain of the filter,

$$|V_O/V_{in}| = [A_F \times (f/f_L)] / \{\sqrt{[1+(f/f_L)^2] \times [1+f/f_L]^2}\} \\ = [6 \times (750/20)] / \sqrt{[1+(750/200)^2] \times [1+(750/200)^2]} \\ = 22.5 / \sqrt{15.6 \times 1.56} = 5.519.$$

$$|V_O/V_{in}| = 20\log(5.519) = 14.837 \text{ dB.}$$

Design Problems:

- (i) Design a fist order low pass filter for a high cut-off frequency of 2 kHz and pass band gain of 2.
- (ii) Design a second order Butterworth low pass filter having upper cut-off frequency 1 kHz
- (iii) Design a High Pass Filter at a cutoff frequency of 1 kHz and pass band gain of 2.
- (iv) Design a wide-band filter having $f_l = 400$ Hz and $f_h = 2$ kHz and pass band gain of 4. Find the value of Q of the filter.
- (v) Design a 50 Hz notch filter.

Comparators and Converters

In the previous chapter, we covered all aspects of active filters. In this chapter, we will learn about comparators and convertors which are also important components of analog design.

This chapter will cover the description and classification of comparators; construction of astable and mono-stable multi-vibrators using Operational amplifiers and design of Schmitt Trigger circuits.

Readers will also learn to analyze and design Clipper and clamper circuits. Additionally, the chapter will help readers understand the need for precision rectifiers and their design as well as the construction of Voltage-to-current converter and Current-to-voltage converter using electronic design software.

Finally, it will also cover the design and simulation of comparators and converters.

Topic	Page
5.1 Introduction	179
5.2 Comparators	180
5.3 Zero Crossing Detector Using OPAMP	184
5.4 Op-Amp Monostable Multivibrator	185
5.5 Astable Multivibrator Using Op-Amp	186
5.6 Schmitt Trigger Circuit	188
5.7 Voltage Limiter Circuit Using Op-amp	189
5.8 Clippers and Clampers	193
5.9 Absolute value circuit:.....	197
5.10 Op-Amp Peak Detector	200
5.11 Sample and Hold Circuit Using Op-Amp	201
5.12 Precision Rectifiers	203
5.13 Voltage-to-current signal conversion	203
5.14 Current to Voltage converter	204
5.15 Summary	206
5.16 Review Questions	207
5.17 Exercises:	209

5.1 Introduction

Advances in VLSI technology have allowed designers to integrate digital and analog circuits on a single chip. When signals are taken from the analog world and processed with digital systems, they require the use of pre and post processing blocks such as converters, filters, sensors, buffers and actuators. Apart from operational amplifiers, we've learnt about various components such as amplifiers, oscillators, filters in previous chapter. In line with this, the current chapter will discuss comparators and converters.

Comparators are the second most widely used components in electronic circuits, after operational amplifiers. The comparator is an electronic decision making circuit that makes use of an operational amplifier's very high gain in its open-loop state. The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison. The output of these comparators is generally fed into a digital encoder, which converts the inputs into a binary value.

The most important application of a high-speed voltage comparator occurs in an analog-to-digital converter system. Other systems that may require voltage comparison are zero-crossing detectors, peak detectors, and full-wave rectifiers etc.

Most physical signals, such as those obtained at transducer outputs, exist in analog form. This is usually followed by a filter whose purpose is to eliminate interference (chapter 4). However, further signal processing is usually required, whether to simply obtain a measurement of signal strength or obtain the value of a particular system parameter of interest. System parameters, usually required for complex control function, are obtained by performing some algebraic manipulations on filter output.

A flash ADC (also known as a direct-conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages.

5.2 Comparators

Comparators are used to compare two voltages. When the input of one port is more than the other, the comparator circuit gives output one, and when the input condition is toggled, then the comparator output swings to next level. These types of circuits are mainly used as detectors to sense voltage levels.

An ideal comparator circuit will have one of the inputs at a given voltage. This may be considered as a potential divider from a supply or reference source voltages. The other input is taken to be sensed.

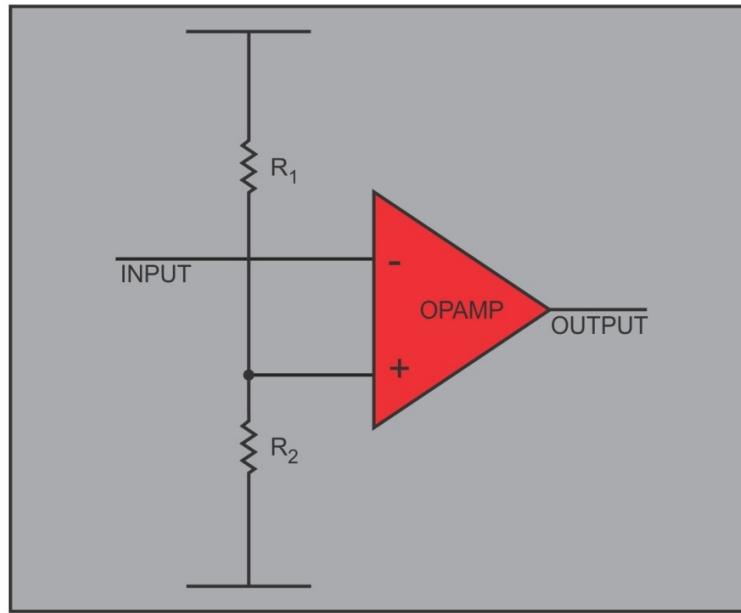


Fig 5.1 Circuit for a basic operational amplifier comparator

In this circuit, the resistors R_1 and R_2 form a potential divider between the two voltages. The voltage at the junction of those two resistors is the switching voltage for the circuit given in the above figure 5.1.

5.2.1 Non-inverting Op-amp Comparator Circuit

A non-inverting op-amp comparator circuit is shown in the figure (5.2) below.

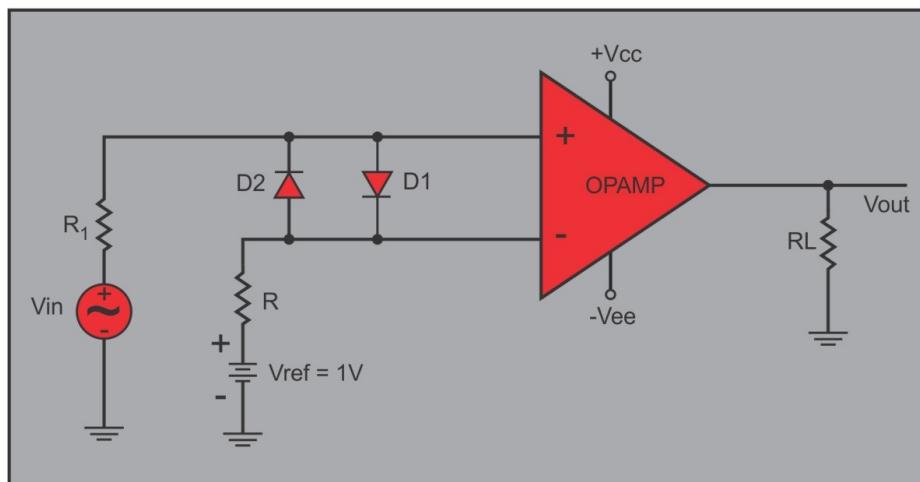
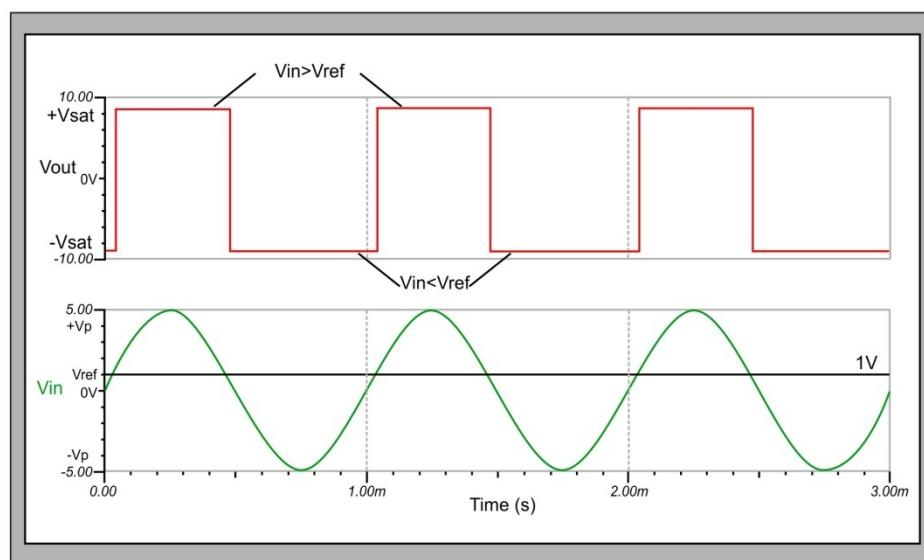


Fig 5.2 OPAMP Non-Inverting Comparator Circuit

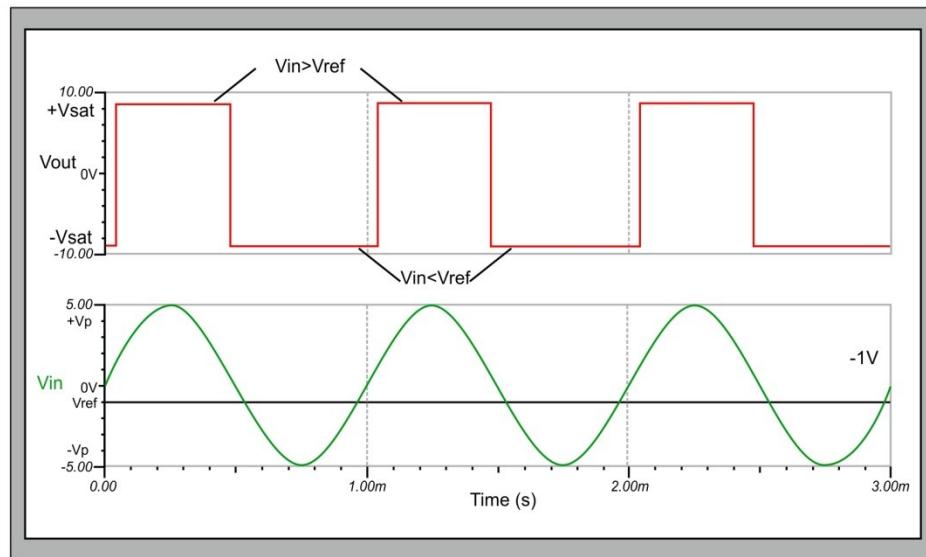
As the sinusoidal input signal V_{in} is applied to the non-inverting terminal it is called as a non-inverting comparator circuit. The fixed reference voltage V_{ref} gives rise to the inverting terminal (-) of the op-amp. When the value of the input voltage V_{in} is greater than the reference voltage V_{ref} , the output voltage V_o goes to positive saturation level. This is because the voltage at the non-inverting input is more than the voltage at the inverting input terminal.

The output voltage V_o goes to negative saturation region, when the value of the input voltage V_{in} is lesser than the reference voltage V_{ref} . This is due to the voltage at the non-inverting input being lesser than the voltage at the inverting input. Thus, output voltage V_o changes from positive saturation point to negative saturation point whenever the difference between V_{in} and V_{ref} changes. This is shown in the fig(5.3) below. The comparator can be called a voltage level detector.

The circuit diagram in figure5.2 shows that the diodes D1and D2 are used to protect the op-amp from damage due to increase in input voltage levels. As the diodes clamp the differential input voltages to the range of 0.7V or -0.7V, they are called clamp diodes. Resistance R1 is connected in series with the input voltage V_{in} and R is connected between the inverting input and reference voltage V_{ref} . R1 limits the current through the clamp diodes and R reduces the offset problem around the circuits.



a) Input and output waveform for positive V_{ref}



b) Inputs and Output Waveforms for Negative Vref

Fig 5.3 Op-Amp Non-Inverting Comparator Waveform

5.2.2 Inverting Op-amp Comparator Circuit

An inverting op-amp comparator circuit is shown in the Figure 5.4. As the sinusoidal input signal V_{in} is applied to the inverting terminal, it is called an inverting comparator circuit. The fixed reference voltage V_{ref} is given to the non-inverting terminal (+) of the op-amp. A potentiometer is used as a voltage divider circuit to obtain the reference voltage in the non-inverting input terminal. Both the ends of the POT are connected to the dc supply voltage $+V_{CC}$ and $-V_{EE}$. The wiper is connected to the non-inverting input terminal.

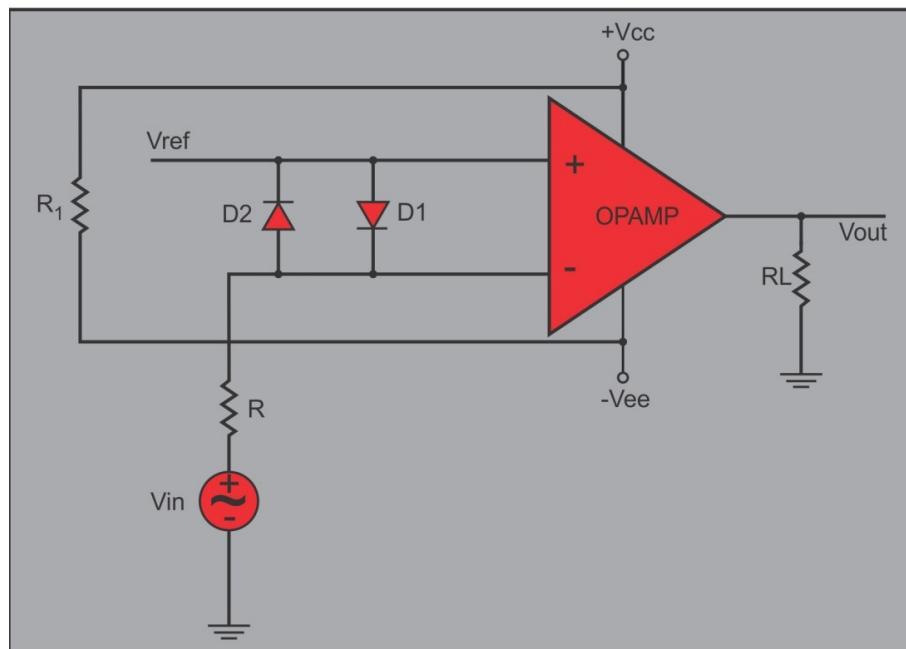
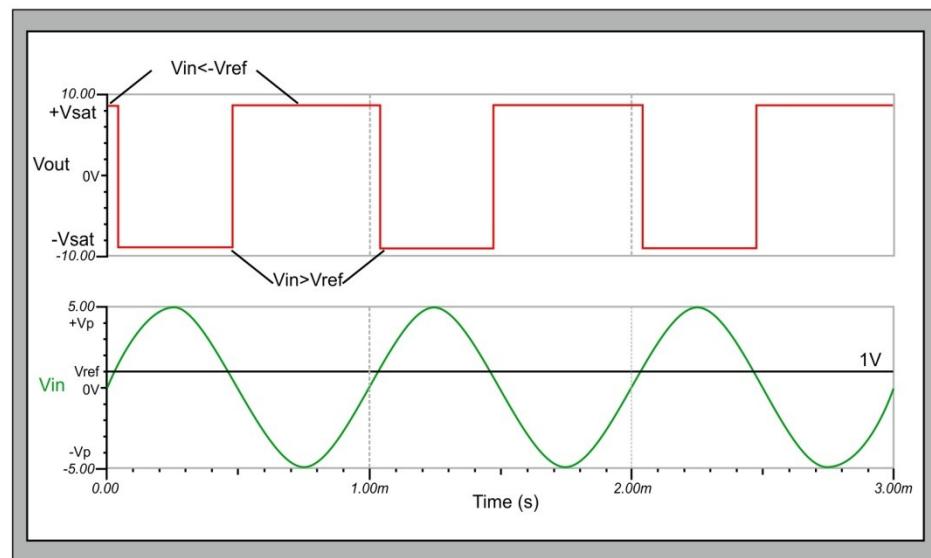
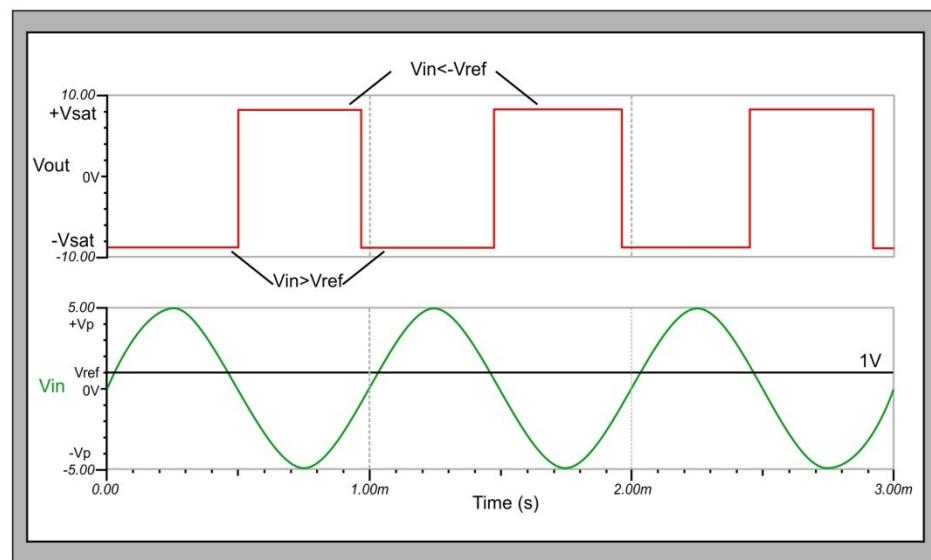


Fig 5.4 Op-amp Inverting Comparator Circuit

When the wiper is rotated to a value near +VCC, Vref becomes more positive, and when the wiper is rotated towards -VEE, the value of Vref becomes more negative. The waveforms are shown in the Figure 5.5.



a) Input and output waveform for positive V_{ref}



b) Inputs and Output Waveforms for Negative V_{ref}

Fig 5.5 Op-Amp Inverting Comparator Waveform

5.3 Zero Crossing Detector Using OPAMP

The zero crossing detector, also called as sine to square wave detector circuit is an important application of the op-amp comparator circuit.

Zero crossing detection is the most common method for measuring the frequency or the period of a periodic signal. Measuring multiple periods helps reduce errors caused by phase noise by making the perturbations in zero crossings small relative to the total period of the measurement. Depending upon the frequency for a particular application and the degree of signal processing, these methods can require high-speed processing components that are too expensive for low cost applications.

Either the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change is the reference voltage with which the input voltage is to be compared, must be made zero ($V_{ref} = 0V$). An input sine wave is given as V_{in} . These are shown in the circuit diagram in figure 5.6 and input and output waveforms in figure 5.7 of an inverting comparator with a 0V reference voltage.

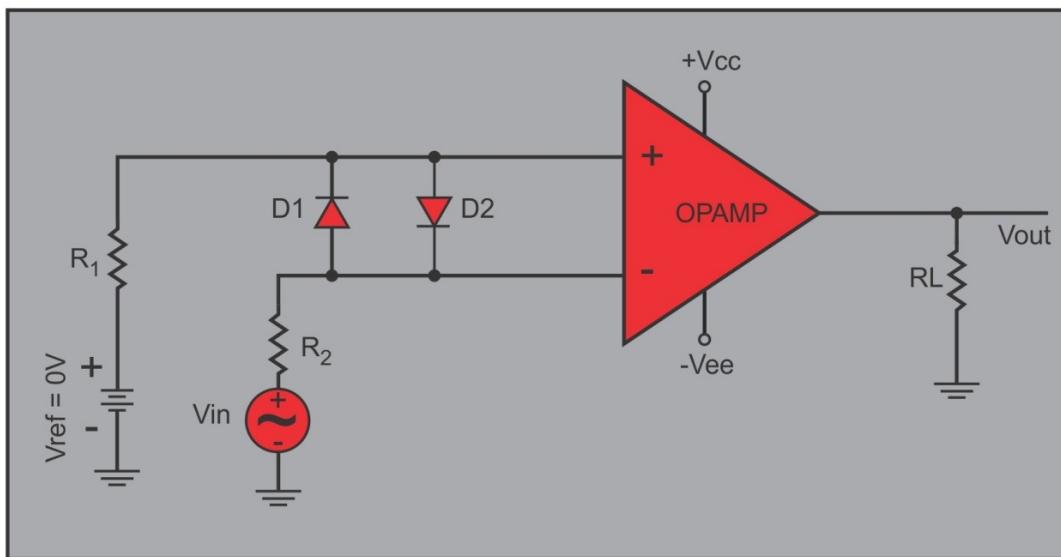


Fig 5.6 Zero-Crossing Detector Using op-amp

As shown in the waveform, for a reference voltage 0V, when the input sine wave passes through zero and goes up in the positive direction, the output voltage V_{out} is driven into negative saturation region. The diodes D1 and D2 are also called clamp diodes. They are used to protect the op-amp from damage due to increase in input voltage.

In some applications, the input voltage may be a low frequency waveform. This means that the waveform changes in a slow phase. This causes a delay in time for the input voltage to cross the zero-level and causes further delay for the output voltage to switch between the upper and lower saturation levels. At the same time, the input noise in the op-amp may cause the output voltage to switch between the saturation levels. Thus zero crossing is detected for noise voltages in addition to the input voltage levels. These difficulties can be removed by using a regenerative feedback circuit with a positive feedback that causes the output voltage to change faster thereby eliminating the possibility of any false zero crossing due to noise voltages at the op-amp input.

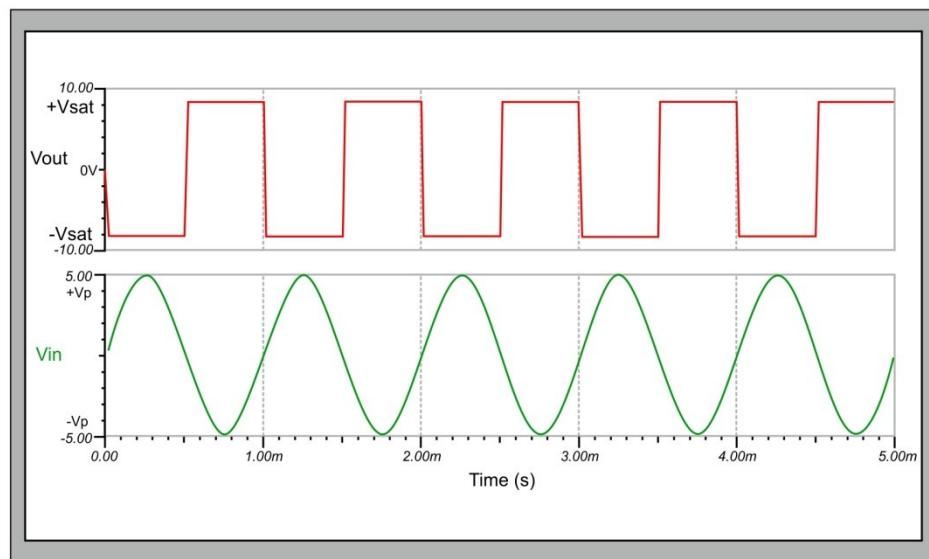


Fig 5.7 Zero-Crossing Detector Waveforms

5.4 Op-Amp Monostable Multivibrator

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

A monostable multivibrator is a circuit that has one stable output state. Its normal output voltage may be 1 or 0, and it stays in that state until triggered. When a triggering pulse is applied, the output switches to the opposite state for the time that is dependent on the RC components of the circuit.

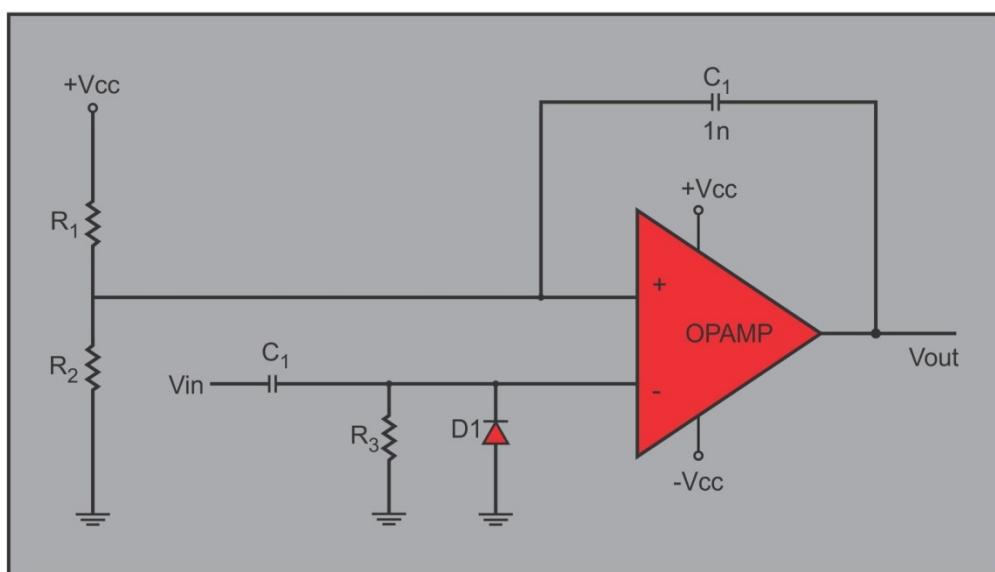


Fig 5.8 Monostable multivibrator using Op-amp

The circuit of a typical Monostable multivibrator using an op-amp is as shown in the figure 5.8 above. The inverting input terminal of the op-amp is grounded through resistor R_3 and the non-inverting input terminal is biased positively by resistors R_1 and R_2 . This causes the output to be at its positive saturation level normally, and the capacitor C_2 gets charged with the polarity as shown in figure 5.9. When an input pulse V_{in} is applied to capacitor C_1 , the input gets differentiated by C_1 and resistor R_3 , to produce positive and negative spikes at the op-amp inverting input terminal. The negative spike gets clipped at -0.7V by the diode D_1 , so the negative spike has no effect on the circuit. However, when the output goes to negative saturation, the capacitor C_2 drives the non-inverting input voltage. This holds the non-inverting input terminal below ground level after the spike has disappeared, thus keeping the output at the negative saturation level.

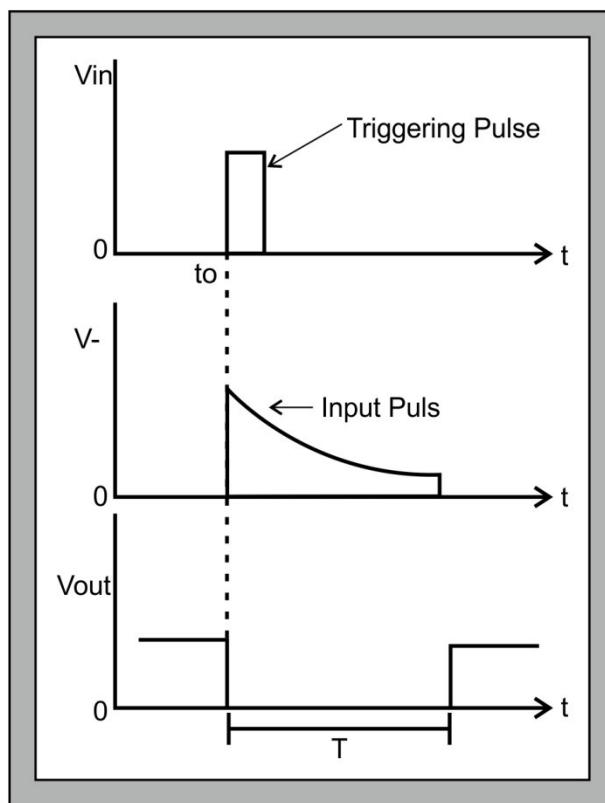


Fig 5.9 Input and output waveforms

When the output is at its negative saturation level, the capacitor C_2 starts discharging via resistors R_1 and R_2 , gradually raising the non-inverting input voltage to ground level. When the non-inverting input voltage raises slightly above ground level, the output of the op-amp switches to its positive saturation level immediately, and the circuit is returned to its original state. The input and the output waveforms of a Monostable multivibrator are shown in the figure 5.9.

5.5 Astable Multivibrator Using Op-Amp

An op-amp astable multivibrator circuit is designed by adding external components to zero crossing detectors. An astable multivibrator is a non-linear circuit configuration using op-amp, which generates square waves without any external triggering. This circuit has no stable output state, only two quasi-states. An astable multivibrator is basically an oscillator, since it requires no external pulse to trigger it. The circuit diagram of an astable multivibrator using operational amplifier is shown in figure 5.10.

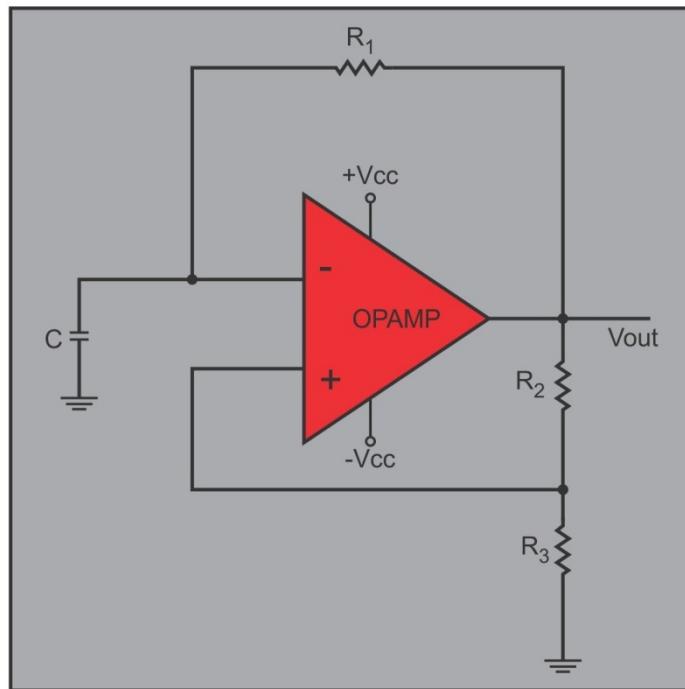


Fig 5.10 Op-amp Astable multivibrator

When the Astable multivibrator circuit output is at its positive saturation level, current flows through the feedback resistor R_1 into the capacitor C . The capacitor gets charged until its voltage reaches the upper trigger voltage of the Schmitt trigger (explained in next section). At this point, the output of the circuit switches to its negative saturation level immediately. No current flows into the capacitor and then the capacitor starts discharging. The discharging of the capacitor continues till the capacitor voltage reaches the lower trigger voltage of the Schmitt trigger. The output switches to its positive saturation level and the cycle repeats. The output and the capacitor voltage waveforms of an Astable multivibrator are shown in the figure 5.11.

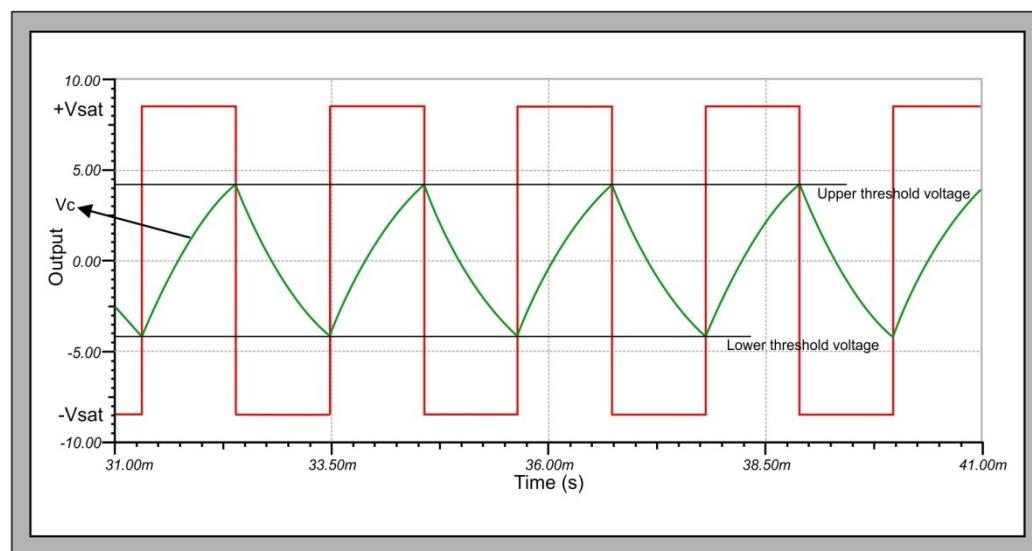


Fig 5.11 Capacitor waveforms

Unlike the monostable or bistable, the Astable multivibrator has two states, neither of which is stable as it is constantly switching between these two states with the time spent in each state which is controlled by the charging or discharging of the capacitor through a resistor.

5.6 Schmitt Trigger Circuit

The Schmitt trigger is often used when interfacing an analog signal to digital circuitry. Schmitt trigger devices are typically used in signal conditioning applications to remove noise from signals used in digital circuits, particularly mechanical contact bounce. They are also used in closed loop negative feedback configurations to implement relaxation oscillators, used in function generators and switching power supplies.

A Zero Crossing detector circuit with a positive feedback connection constitutes the Schmitt trigger.

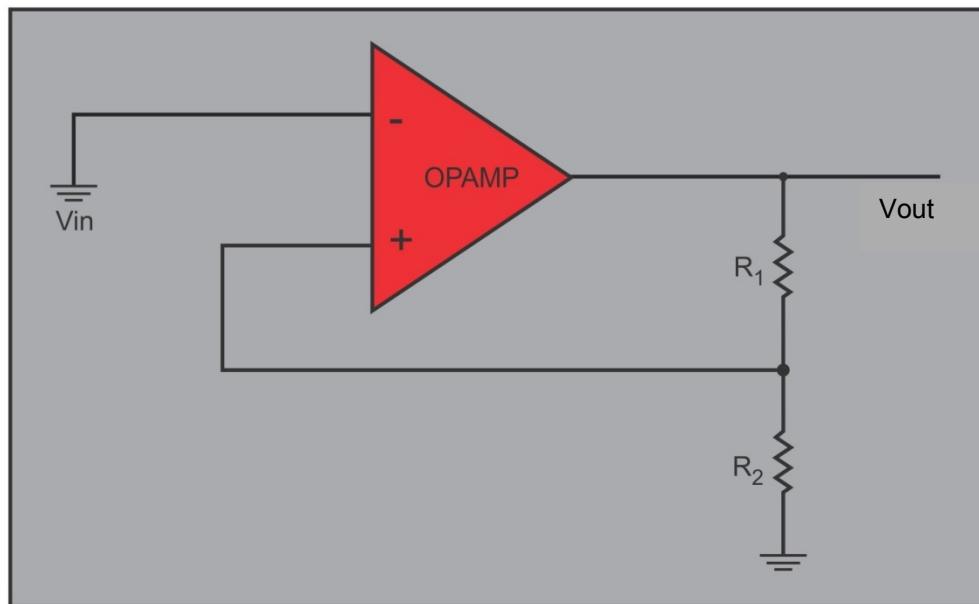


Fig 5.12 Schmitt Trigger

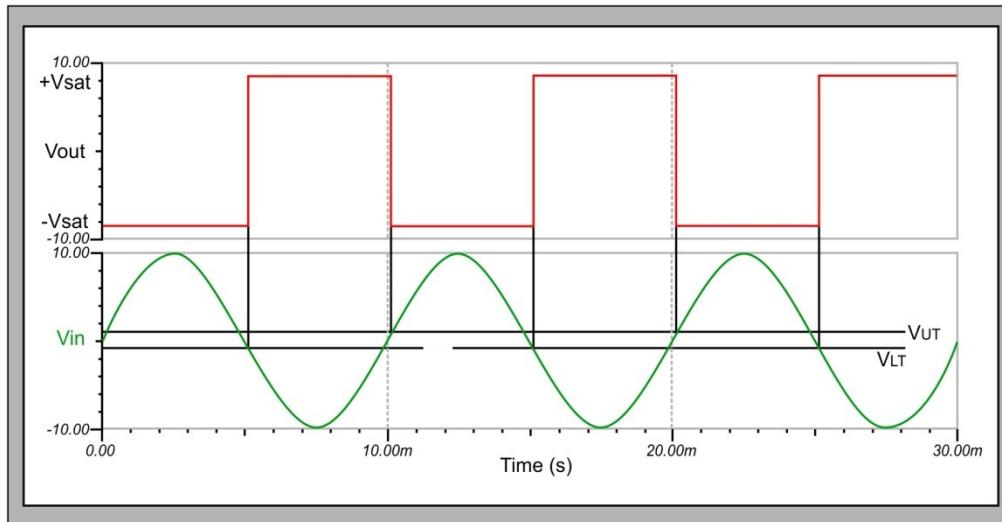


Fig 5.13 Input and Output Waveforms of Schmitt Trigger

The circuit of a typical Schmitt trigger is as shown in the figure 5.12. The input voltage, V_{in} , is applied to the inverting input terminal and a part of the output voltage is connected as feedback to the non-inverting input terminal, through a potential divider network.

The input voltage V_{in} triggers the output voltage V_{out} to change from one saturation level to the other, every time when the input voltage exceeds a certain predefined voltage levels. These voltage levels are called as upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}).

The input and output waveforms of the Schmitt trigger circuit are shown in the figure 5.13. It can be seen that, as long as the input voltage V_{in} is less than upper threshold voltage V_{UT} , the output voltage is saturated at its positive extreme $+V_{sat}$. When the input voltage goes beyond V_{UT} , the output immediately switches to its negative saturation level $-V_{sat}$.

The upper and lower trigger points that is the threshold voltages can be mathematically obtained by using the relation,

$$V_{UT} = [R_2 \cdot (+V_{sat})] / (R_1 + R_2) \text{ and } V_{LT} = R_2 \cdot (-V_{sat}) / (R_1 + R_2)$$

$$\text{If } R_2 / (R_1 + R_2) = \beta, \text{ then } V_{UT} = \beta (+V_{sat}) \text{ and } V_{LT} = \beta (-V_{sat})$$

Above given equations portrays that, by choosing appropriate values of resistor R_1 & R_2 , the upper and lower threshold levels can be adjusted and controlled.

5.7 Voltage Limiter Circuit Using Op-amp

Current limiting is the practice in electrical or electronic circuits of imposing an upper limit on the current that may be delivered to a load with the purpose of protecting the circuit generating or transmitting the current from harmful effects due to a short-circuit or similar problem in the load.

Thus, to maintain the op-amp's output voltage swing between these ranges, other components like zener diodes are added to the circuit. Such circuits with specified output swing are called voltage limiters. Some of the most commonly used voltage limiter circuits are shown in figure 5.14.

A Zener diode behaves like an ideal diode, till the voltage reaches a certain value known as the breakdown voltage. But for higher voltages, it allows current to flow in the reverse direction.

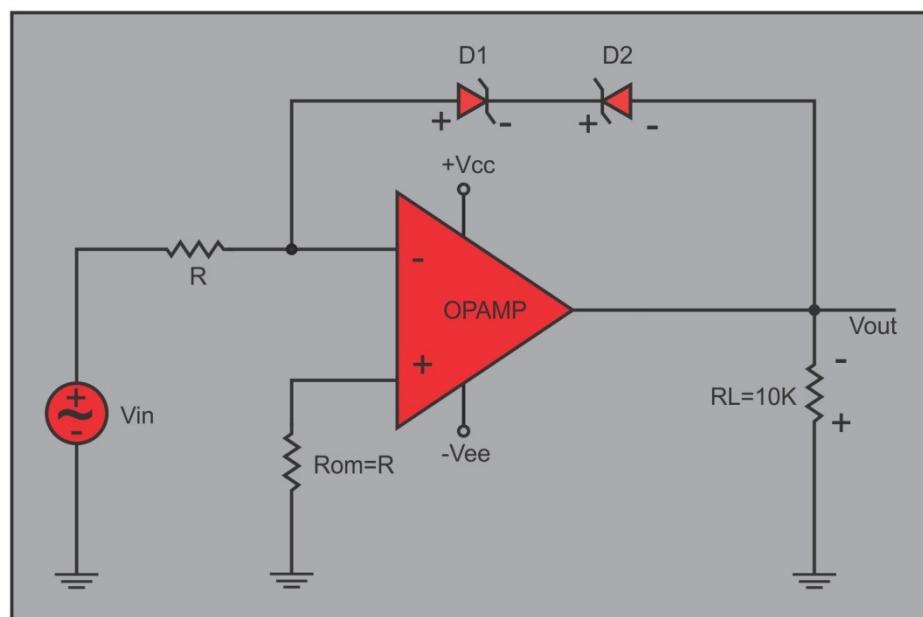


Fig 5.14 Voltage limiter using op-amp

There are two zener diodes that are connected in the feedback path of the op-amp circuit. The voltage limit between the positive and negative values of the output voltage, V_0 is kept in this design. As shown in figure 5.15, the voltage V_{in} increases from zero to positive voltage, the value of V_0 increases in the negative direction. This goes until the diode D1 becomes forward biased and in D2 avalanche breakdown takes place.

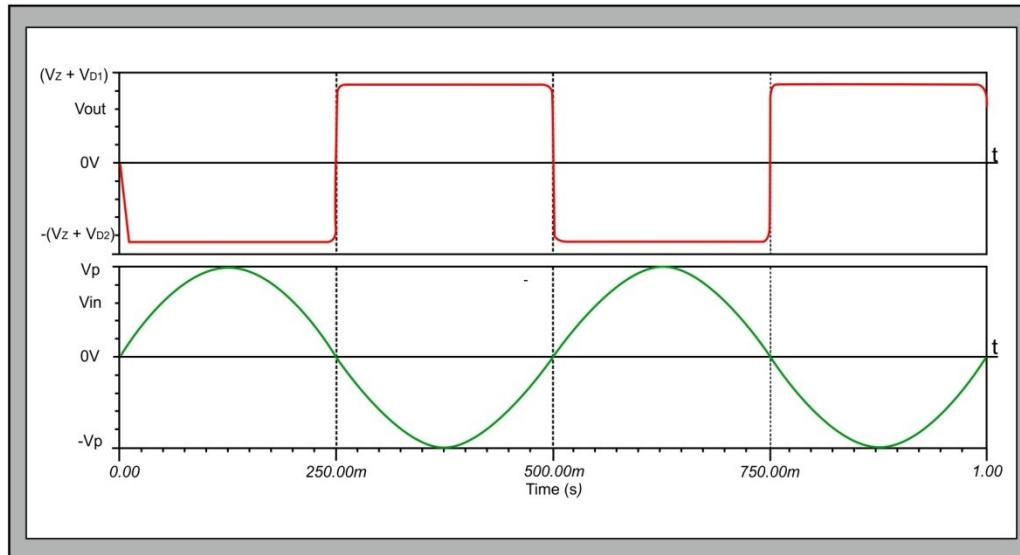


Fig 5.15 Voltage limiter waveforms

At this condition, $V_0 = V_z + V_{D1}$

V_z – Zener Voltage & V_{D1} – Voltage drop across D1 = 0.7V

If V_0 increases from 0 to negative voltage, V_0 increases positively until diode D2 is forward biased and D1 goes into avalanche condition.

At this condition, $V_0 = V_z + V_{D2}$

V_z – Zener Voltage & V_{D2} – Voltage drop across D2 = 0.7V

Thus the limit of output voltage swing is between $+ (V_z + 0.7)$ and $- (V_z + 0.7)$.

In the figure 5.16, R_{om} is used to reduce the offset problems. V_{in} will appear across resistor R, since the $V_1 = V_2 = 0V$ (virtual ground).

The fig (5.16) shows a combination of zener diode and rectifier diodes. This circuit is used to bring the level of swing of V_0 to a positive direction. When V_{in} ranges from 0 to positive voltage, D2 is reverse biased and thus $V_0 = -V_{sat}$.

When V_{in} ranges from 0 to negative voltage, D2 is forward biased and D1 goes into avalanche condition.

Thus $V_0 = V_z + V_{D2}$

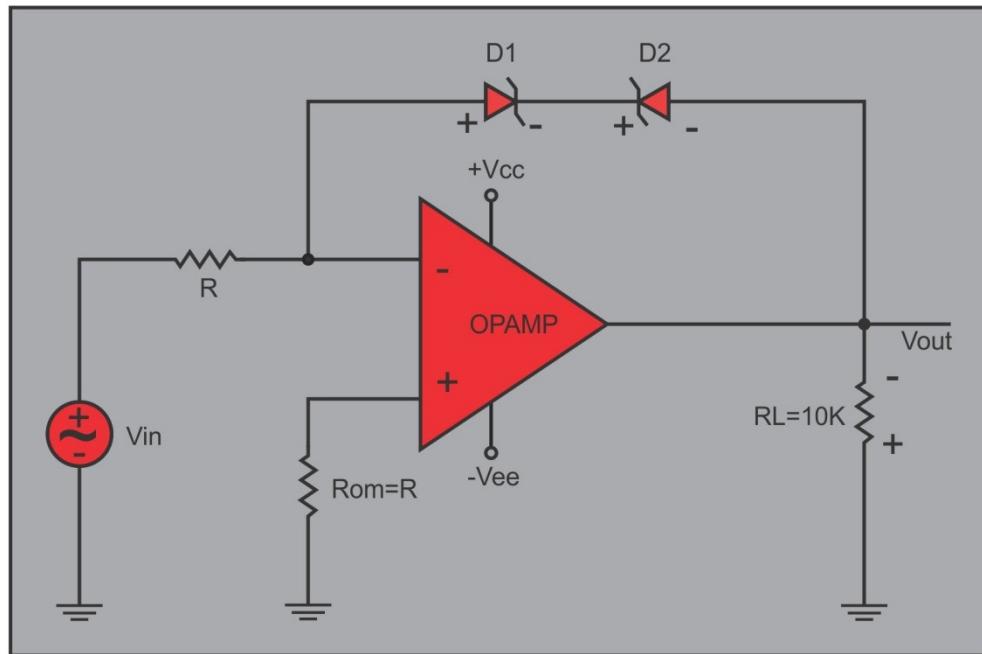


Fig 5.16 Voltage limiter circuit with two zener diodes

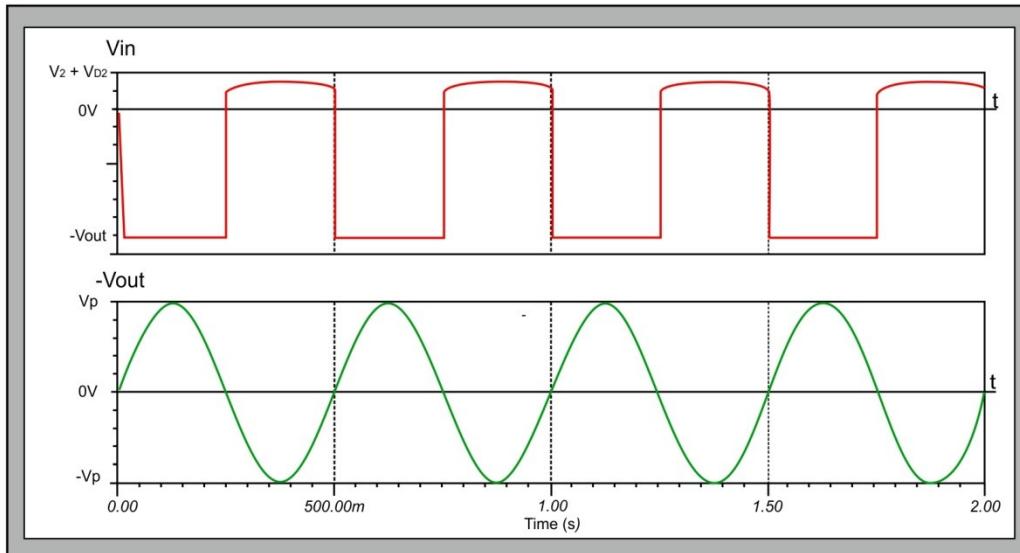


Fig 5.17 Output waveforms of voltage limiter circuit

Figure 5.18 shows the use of a single zener diode in the feedback path of an op-amp. This enables the output to be limited between $+V_Z$ and $-V_D$.

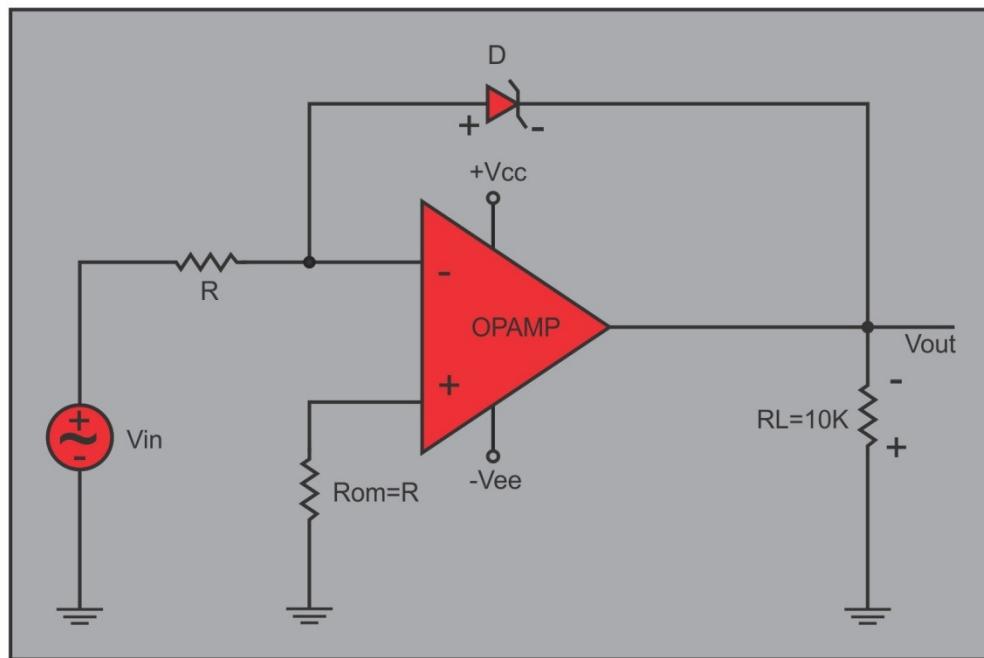


Fig 5.18 Voltage limiter circuit with one zener diode

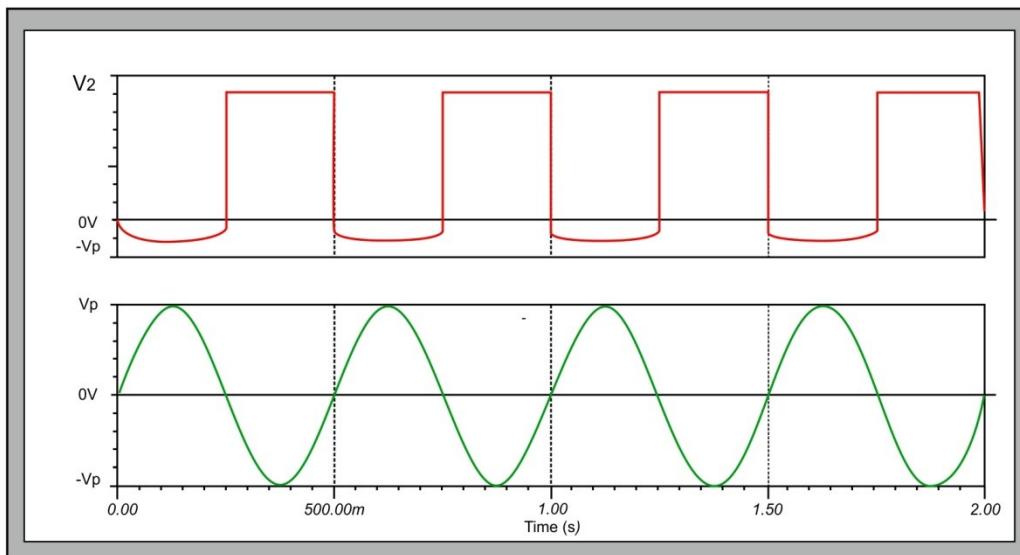


Fig 5.19 Voltage limiter waveforms

5.8 Clippers and Clampers

Wave shaping circuits such as Clipper and Clamper are widely used in analog television receivers and FM transmitters. The variable frequency interference can be removed by using the clamping method in television receivers, and in FM transmitters. The typical application of diode clipper is for the protection of transistor from transients, as a freewheeling diode connected in parallel across the inductive load. Clampers can be used for removing the distortions. Clampers can be used as voltage doublers or voltage multipliers.

In op-amp clipper circuits, a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform. In op-amp clamper circuits, a predetermined dc level is intensively inserted in the output volt. Because of this, the clamper is sometimes called a dc inverter.

5.8.1 Positive Clipper

Positive clipper is a circuit that removes positive parts of the input signal (Figure 5.20). The level of clipping is determined by the reference voltage V_{ref} , which should be lesser than the input range of the op-amp ($V_{ref} < V_{in}$). During the positive half cycle of the input, the diode D1 conducts until V_{in} equals to V_{ref} . This happens because when $V_{in} < V_{ref}$, the output volts V_0 of the op-amp becomes negative with respect to the device D1 into conduction when D1 conducts it closes feedback loop and op-amp operates as a voltage follower (i.e.) Output V_0 follows input until $V_{in} = V_{ref}$. When $V_{in} > V_{ref}$, then the V_0 becomes positive to derive D1 into off condition. This opens the feedback loop and op-amp operates in open loop configuration. The op-amp alternates between open loop and closed loop operation as the D1 is turned off and on respectively. The output waveforms are shown in Figure 5.21.

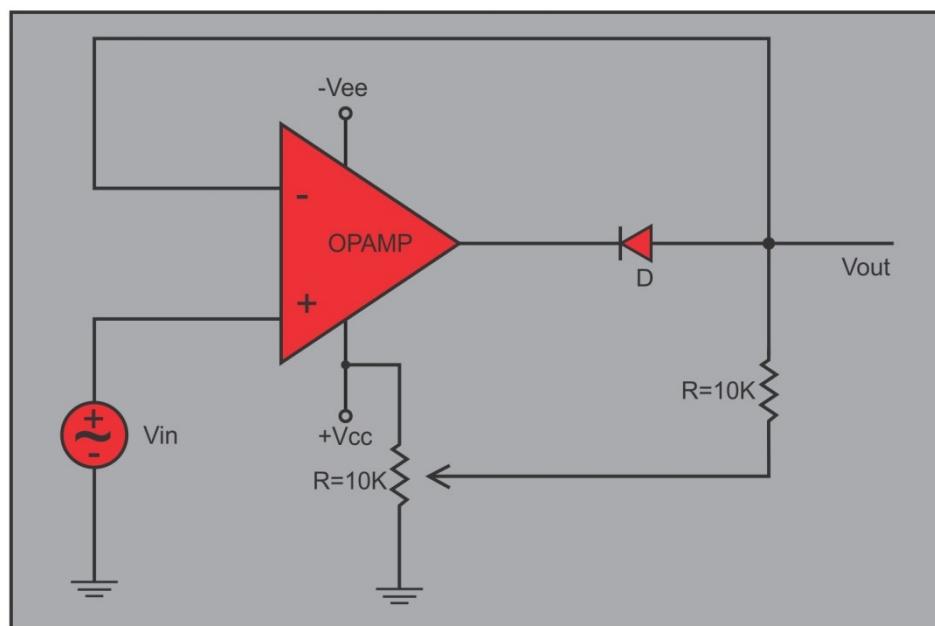


Fig 5.20 Positive clipper

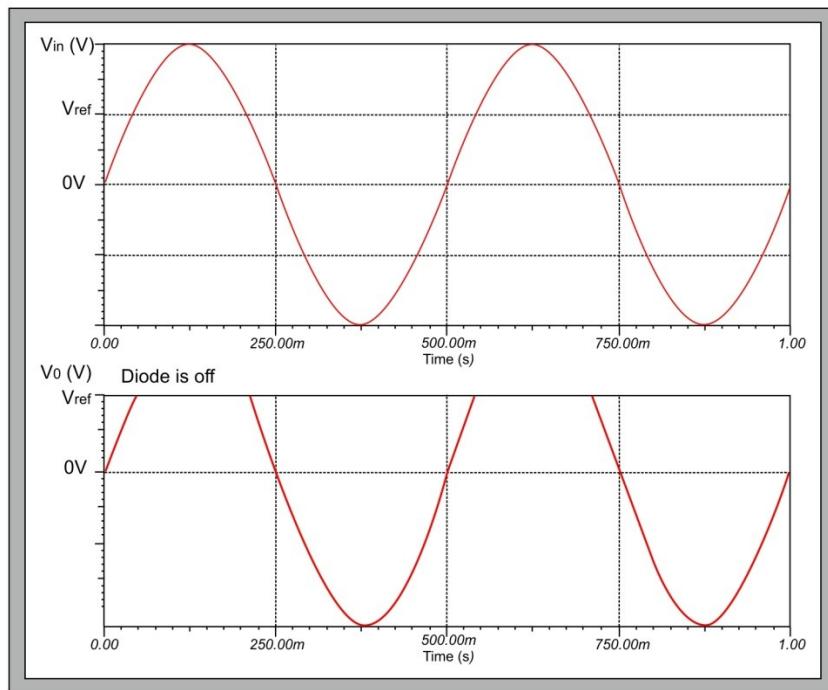


Fig 5.21 Output waveforms of positive clipper

5.8.2 Negative Clipper

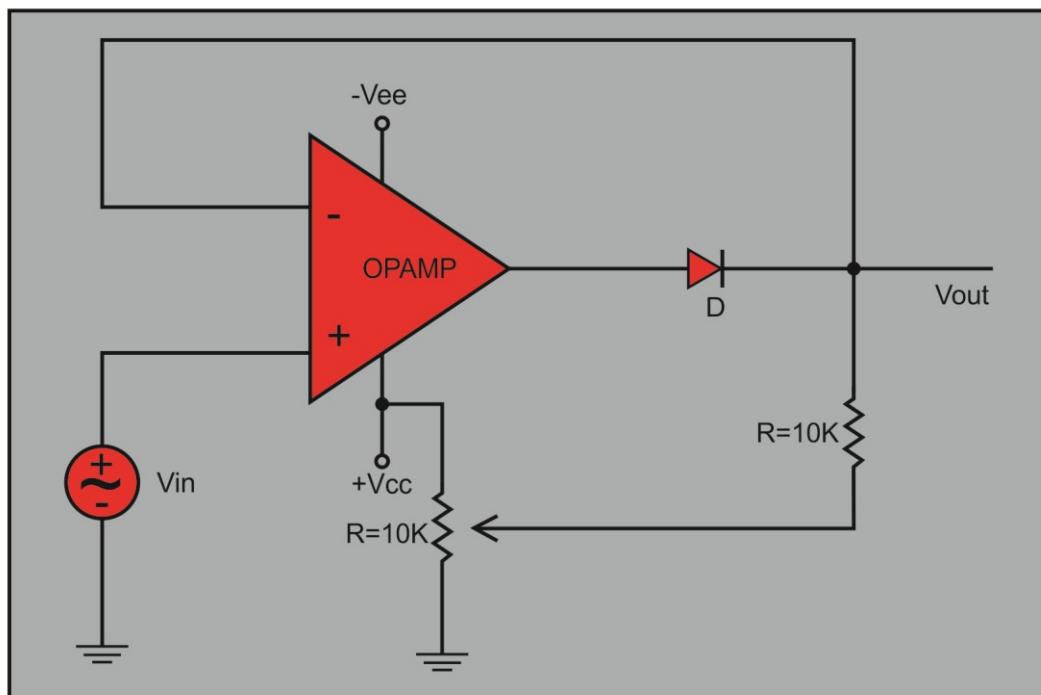


Fig 5.22 Negative clipper circuit

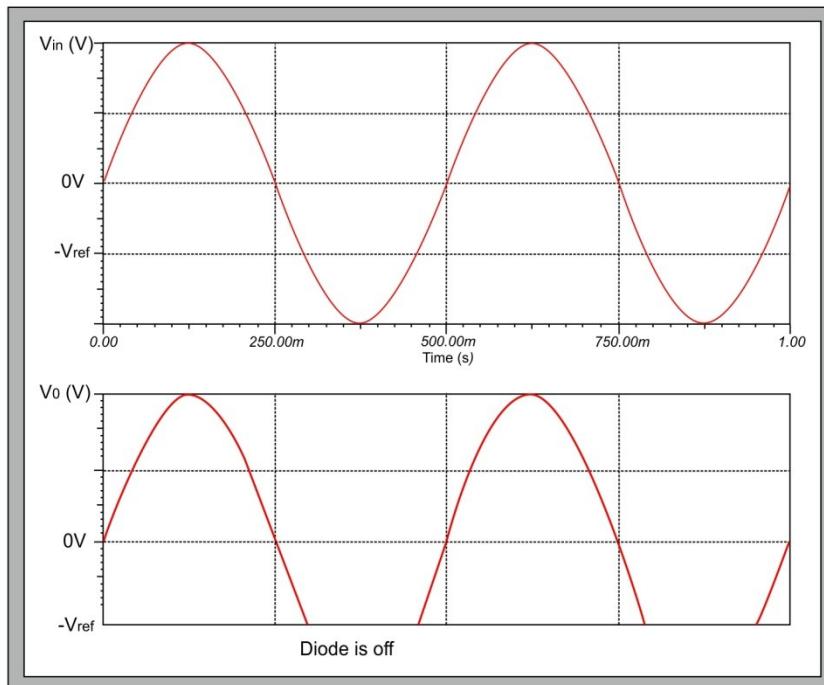


Fig 5.23 output waveforms of negative clipper

The positive clipper is converted into a negative clipper (Figure 5.22) by simply reversing diode D1 and changing the polarity of V_{ref} voltage. The negative clipper clips off the negative parts of the input signal below the reference voltage. Diode D1 conducts when V_{in} is greater than or equal to V_{ref} and therefore during this period o/p volt V_0 follows the i/p volt V_{in} . The negative portion of the output volt below $-V_{ref}$ is clipped off because (D1 is off) V_{in} is less than or equal to V_{ref} . If $-V_{ref}$ is changed to $-V_{ref}$ by connecting the potentiometer R_p to the $+V_{cc}$, the V_0 below $+V_{ref}$ will be clipped off. The diode D1 must be on for $V_{in} > V_{ref}$ and off for V_{in} .

5.8.3 Positive and Negative Clampers

In clamper circuits, a predetermined dc level is added to the output voltage. The output is clamped to a desired dc level. If the clamped dc level is positive, the clamper is called as positive clamper. If the clamped dc level is negative, the clamper is called as negative clamper.

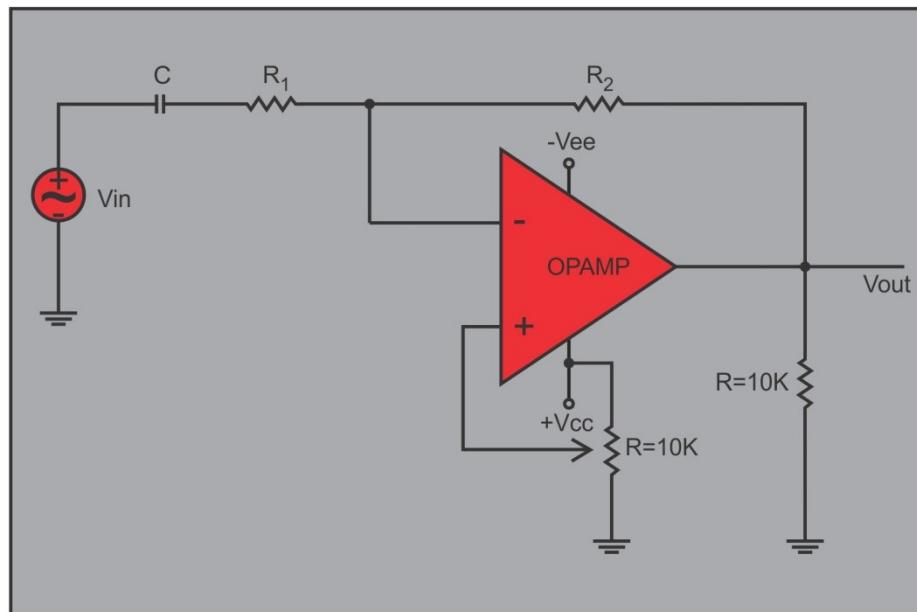


Fig 5.24 Positive clamper circuit

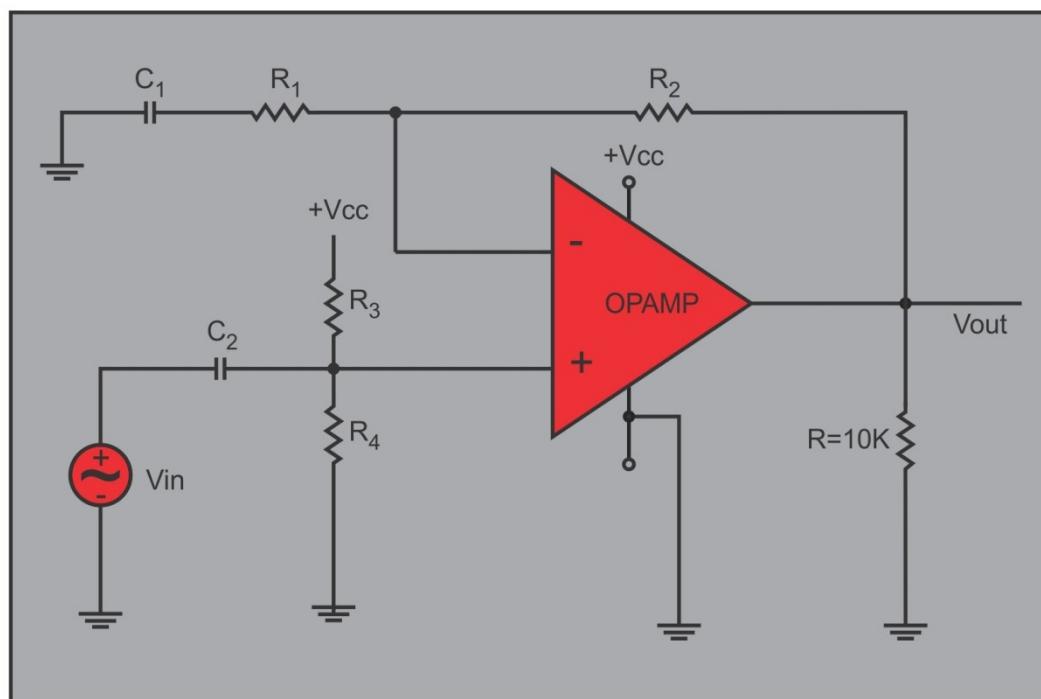


Fig 5.25 Negative clamper circuit

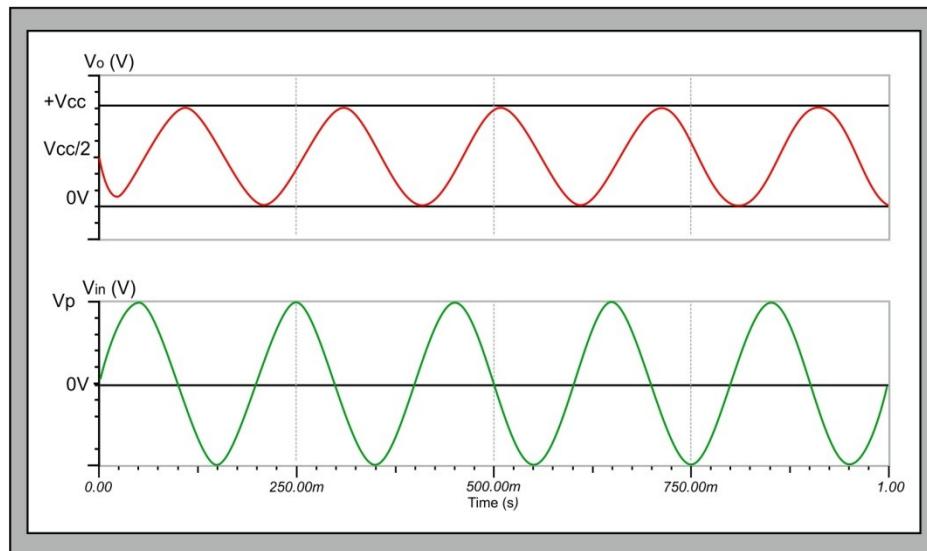


Fig 5.26 Positive clamper output waveform

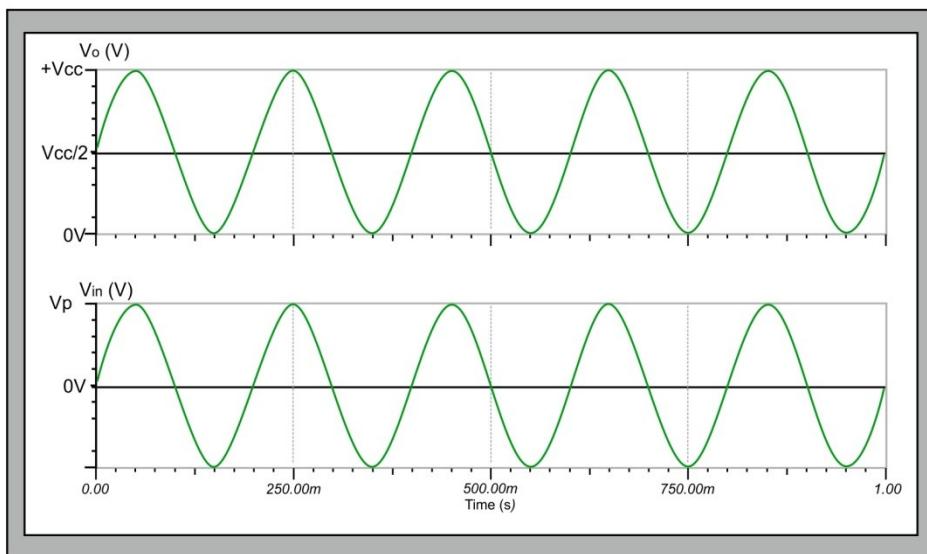


Fig 5.27 Negative clamper output waveform

5.9 Absolute value circuit:

Operational amplifiers can improve the performance of a wide variety of signal processing circuits. In rectifier circuits, the voltage drop that occurs with an ordinary semiconductor rectifier can be eliminated to give a precision rectification. The figure 5.28 given below is the precision full wave rectifier. It consists of following sections: Precision half-wave rectifier & Inverting summing amplifier.

The input voltage V_{IN} is applied to one terminal of the summing amplifier along with resistor R_3 and to the input of the precision rectifier. The output of precision rectifier is applied to another terminal of summing amplifier. The precision half-wave rectifier circuit uses an inverting amplifier configuration.

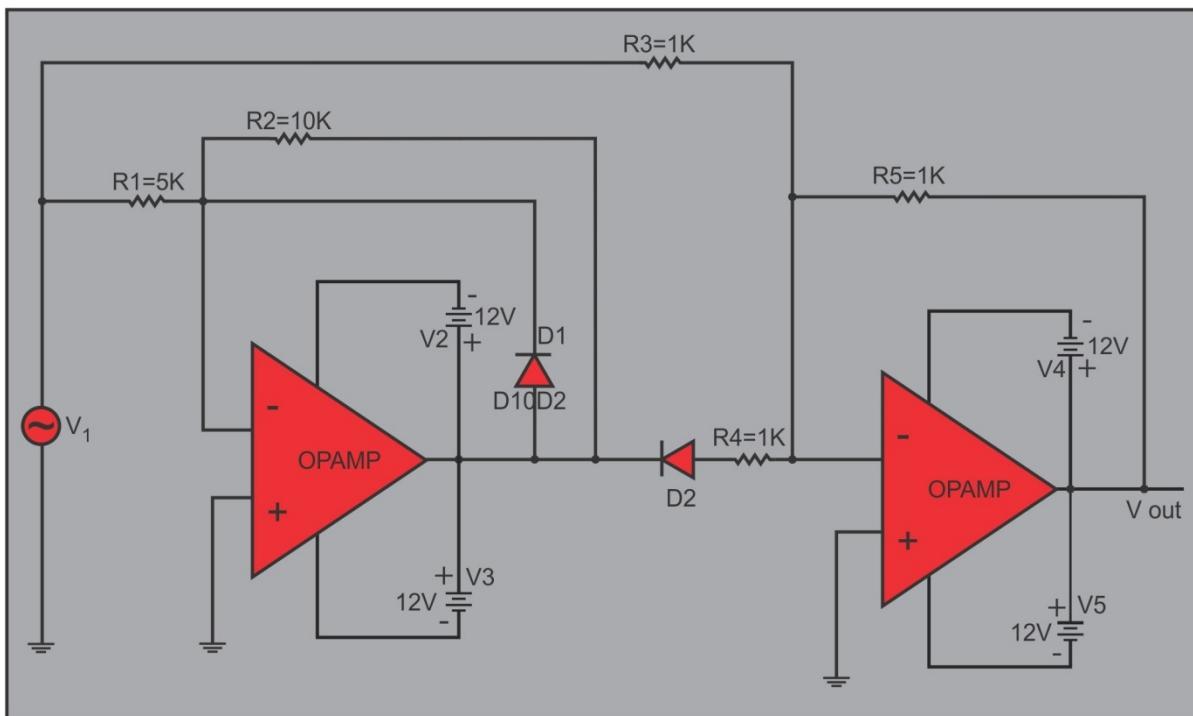


Fig 5.28 Absolute Value Circuit

When the input signal V_{in} is positive, Op-Amp output terminal is negative, Diode D1 is reverse biased and D2 Diode is forward biased, the circuit is

$V_b = - (R_2/R_1) * V_{in}$. In the circuit, R_1 and R_2 have been chosen such that $R_2 = 2R_1$. So the voltage at $V_b = -2V_{in}$. Thus during the positive half cycle of the rectified voltage V_b is applied to terminal B of the inverting summing amplifier is $-2V_{in}$.

The voltage at terminal A is $V_a = +V_{in}$. The output from the summing circuit with $R_3=R_4=R_5$ is $V_o = -(V_a+V_b)$. Hence $V_o = -(V_{in} - 2V_{in}) = +V_{in}$. So during the negative half cycle of the input, the Op-Amp output terminal goes positive, causing D2 to be reverse biased. This tends to pull the Op-Amp inverting terminal in a positive direction. But, such a move would cause the Op-Amp output to go negative. So, the output settles at the voltage close to ground level. That is $V_b=0$ and $V_a = -V_{in}$. Totally the V_o will be $V_o = -(-V_{in}+0) = +V_{in}$.

It is seen that the output is a full wave rectified version of the input voltage. A precision full-wave rectifier is also known as absolute value circuit. This means the circuit output is the absolute value of the input voltage regardless of polarity.

5.9.1 Op-amp absolute value amplifier

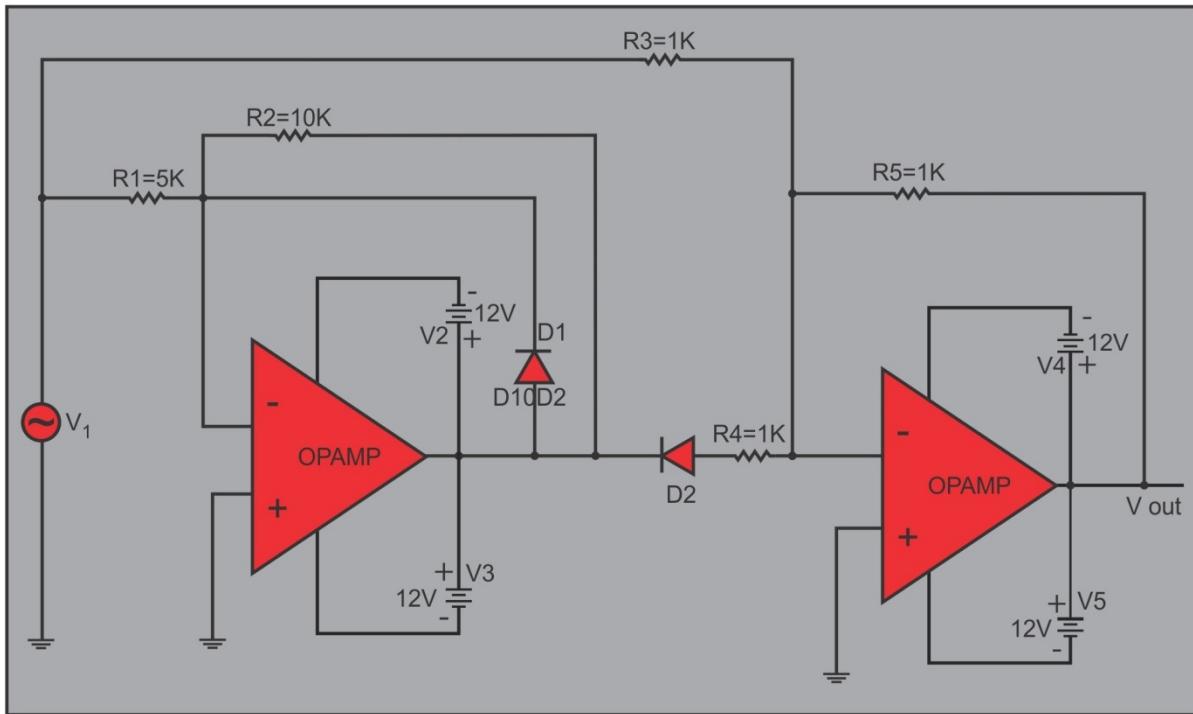


Fig 5.29 Op-amp absolute value amplifier

In order to analyze the given circuit, analysis has to be separated.

- $V_{IN} > 0$.

The inverting input of Op-amp1 is on higher potential, and then the non-inverting input which is on the ground level, if input voltage is positive. Equivalent circuit is given in fig (5.30).

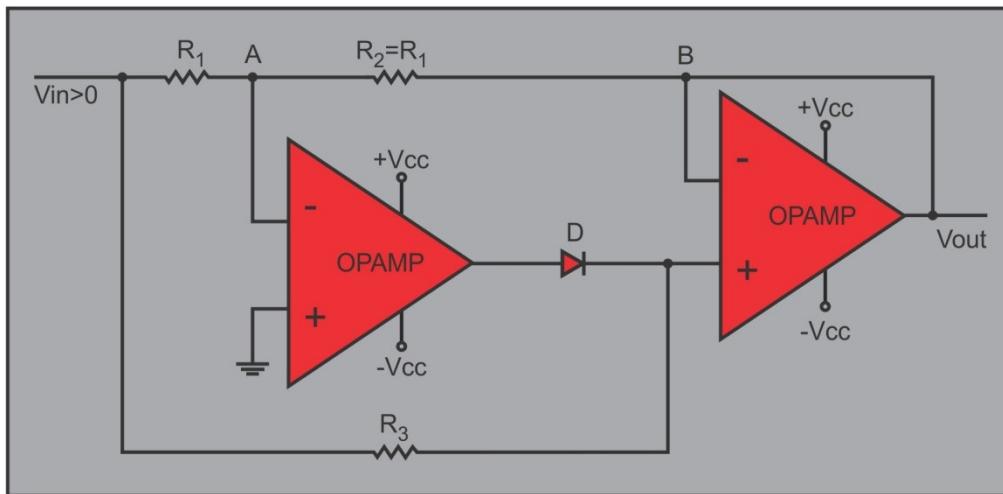


Fig 5.30 Op-amp absolute value amplifier if $V_{IN} > 0$

The non-inverting input of OPAMP₂ is connected via R₃ to V_{IN}. Inverting input is also connected to V_{IN} via 2R₁. Both inputs are at the same potential, OPAMP₂ operates in amplifying mode, and inverting input is shortly connected to the output. If V_{IN}>0, V_{OUT}=V_{IN}.

- **V_{IN}<0**

If input voltage is negative, inverting input of OPAMP₁ is on lower potential than the non-inverting input which is on the ground level. Equivalent circuit is given in figure 5.31.

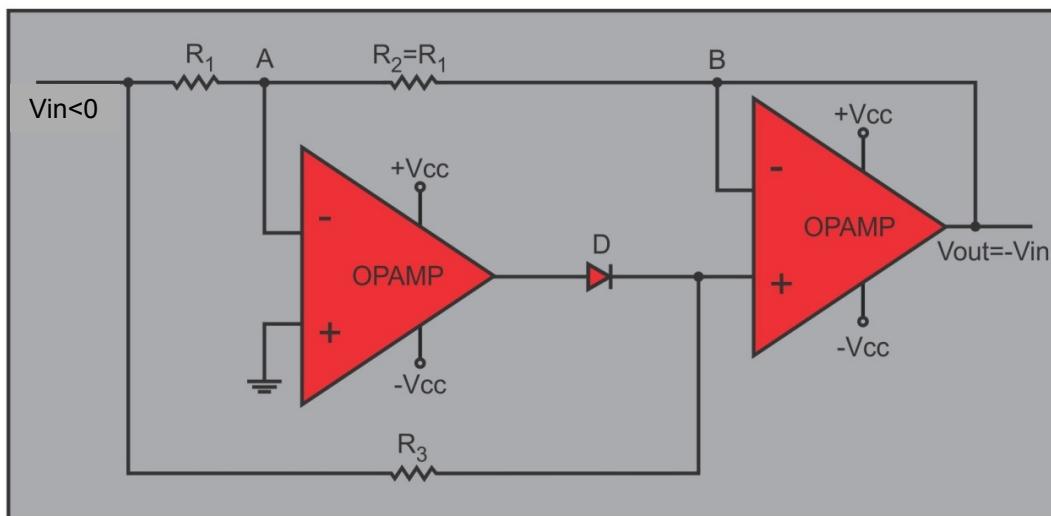


Fig 5.31 Op-amp absolute value amplifier if V_{in}<0

The inverting input of OPAMP₁ is on the virtual ground, i.e. on potential of zero volts. Current through R₁ flows from point A i.e.; zero volts to input terminal i.e.; negative voltage. Current through R₂ is with the same magnitude and since R₁=R₂, potential of point B is positive and equal to -V_{IN}. Non-inverting input is on the same positive potential of -V_{IN}. Inverting input of Op-amp₂ is shortly connected to output, so output is now in -V_{IN}.

If $V_{in} > 0$, $V_{out} = -V_{in}$

$$V_{out} = \begin{cases} V_{in}, & V_{in} > 0 \\ -V_{in}, & V_{in} > 0 \end{cases}$$

$$V_{out} = |V_{in}|$$

5.10 Op-Amp Peak Detector

A circuit which detects and holds the most positive value attained by the input signal prior to the time when the switch is closed is called Peak detector. The op amp peak detector is as shown in figure 5.32 below.

Peak detectors can operate at frequencies much higher than those for which there are ADCs, since its only semiconductors are the op amps and diode, both of which are available into the tens of GHz. Due to its virtues, this design is still used as the core of the RF peak-power measurement function, either using discrete components, as a single-purpose IC/module, or as part of a larger IC.

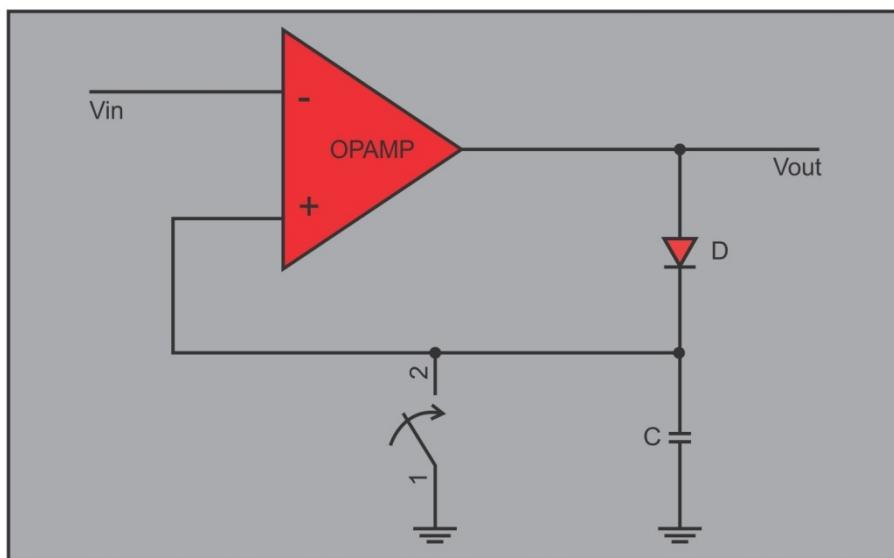


Fig 5.32 Op-amp peak detector

The operation can be explained as follows, assume the switch is open and if

a) $V_{out} < V_{in}$ the op amp output V' is positive so that the diode conducts and the capacitor charges to the input value. At that instant it forms a voltage follower circuit.

b) When $V_{out} > V_{in}$, op amp output V' is negative and the diode becomes reverse biased.

Thus the capacitor charges to the most positive value of input.

Hence the operation of opamp peak detector can be summarized as follows

- $V_{out} < V_{in}$; D ON and C charges to peak value of input,
- $V_{out} > V_{in}$; D OFF and C holds the peak value of input

5.11 Sample and Hold Circuit Using Op-Amp

A circuit which samples an input signal and holds onto its last sampled value until the input is sampled again is called a sample and hold circuit.

Sample and hold circuits are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process. Sample and hold circuits are used in linear systems. In addition, sample and hold circuits are often used when multiple samples need to be measured at the same time. These circuits are commonly used in analog to digital converters, communication circuits, PWM circuits etc. The circuit shown in figure 5.33 is of a sample and hold circuit based on op-amp, n-channel MOSFET and few passive components.

In the circuit MOSFET works as a switch while opamp is wired as a voltage follower. The signal to be sampled (V_{IN}) is applied to the drain of MOSFET while the sample and hold control voltage (V_s) is applied to the source of the MOSFET. The source pin of the MOSFET is connected to the non inverting input of the opamp through the resistor R_3 . Resistor R_2 serves as the load resistor while preset R_1 is used for adjusting the offset voltage.

During the positive half cycle of the V_s , the MOSFET is ON which acts like a closed switch and the capacitor C_1 is charged by the V_{IN} and the same voltage (V_{IN}) appears at the output of the opamp. Since the input impedance of the opamp is too high the voltage V_{IN} is retained and it appears at the output of the opamp.

The time periods of the Vs during which the voltage across the capacitor (Vc) is equal to Vin are called sample periods (Ts) and the time periods of Vs during which the voltage across the capacitor C1 (Vc) is held constant are called hold periods (Th). The input and output wave forms of the circuit are given in figure 5.34.

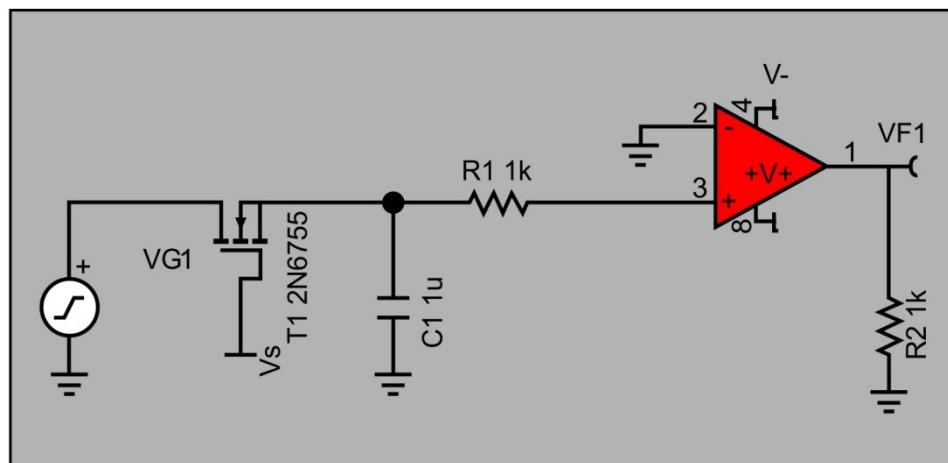


Fig 5.33 Sample and Hold circuit using op-amp

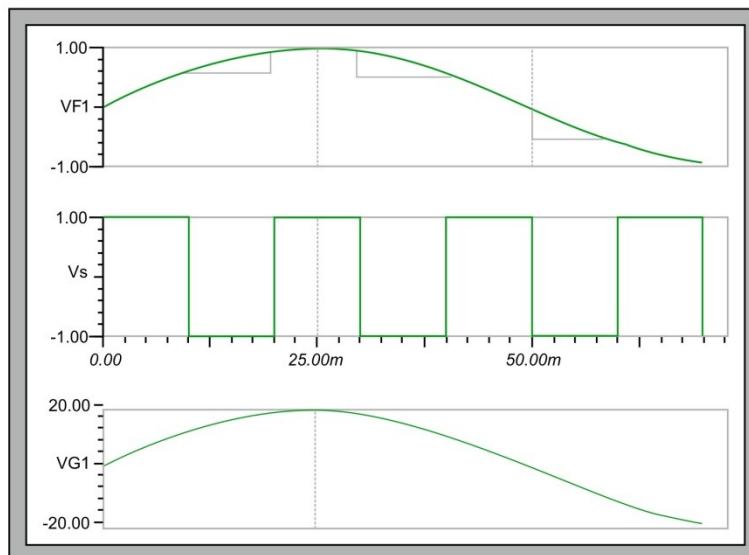


Fig 5.34 Input and output waveforms - Sample and hold circuit

5.12 Precision Rectifiers

The precision rectifier, also known as a super diode, is a configuration circuit obtained with an operational amplifier in order to have a circuit which behaves like an ideal diode and rectifier. It is useful for high-precision signal processing.

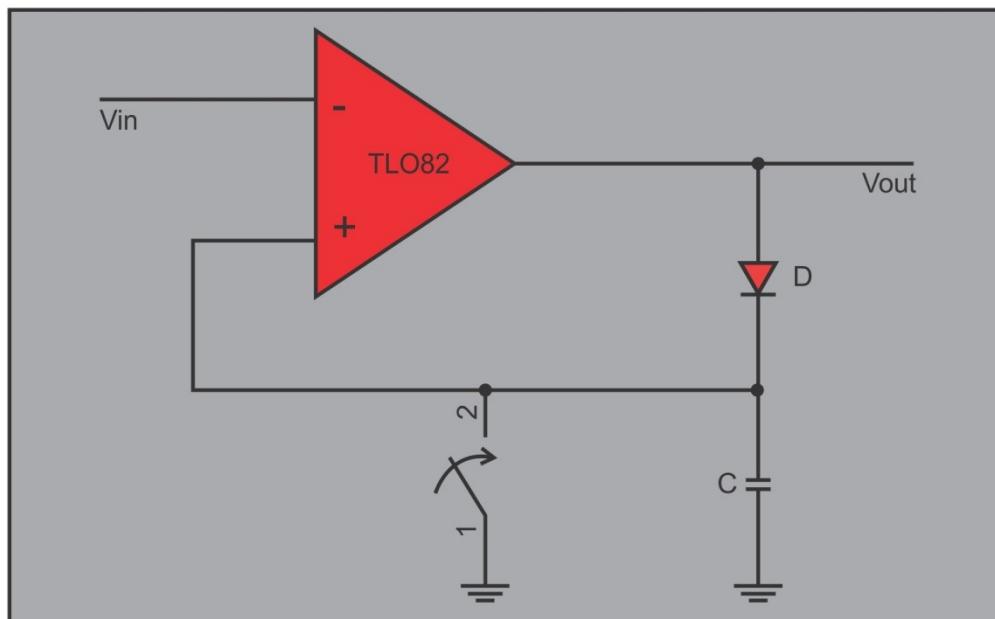


Fig 5.35 Precision Rectifier

5.12.1 A Simple Precision Rectifier Circuit

The basic circuit implementing such a feature is shown in figure 5.35, where R_L can be any load. When the input voltage is negative, there is a negative voltage on the diode, so it works like an open circuit, no current flows through the load, and the output voltage is zero.

When the input is positive, it is amplified by the operational amplifier which switches the diode on. Current flows through the load and, because of the feedback, the output voltage is equal to the input voltage. The actual threshold of the super diode is very close to zero, but is not zero. It equals the actual threshold of the diode, divided by the gain of the operational amplifier. When the input becomes (even little) negative, the operational amplifier runs open loop, as there is no feedback signal through the diode. With a typical high open loop gain operational amplifier, the output saturates. The input then becomes positive again, the op-amp has to get out of the saturated state before positive amplification can take place. This change generates some ringing and takes some time, greatly reducing the frequency response of the circuit.

5.13 Voltage-to-current signal conversion

In electronics, transconductance is the mathematical ratio of current change to the voltage change ($\Delta I / \Delta V$), and it is measured in the unit of Siemens, the same unit is also used to express conductance. The transconductance ratio is fixed by the value of the 250Ω resistor, giving a linear current-out/voltage-in relationship in this circuit.

5.13.1 Voltage to current converter

In Figure 5.36, a voltage to current converter in which load resistor R_L is floating (not connected to ground). The input voltage is applied to the non-inverting input terminal and the feedback voltage across R operates the inverting input terminal in the device. As the feedback voltage across R depends on the

output current i_L and is in series with the input difference voltage v_d , this circuit is also called a current series negative feedback amplifier.

Writing the voltage equation for the input loop:

$$V_{in} = V_d + V_f$$

But $v_d \gg$ since A is very large, therefore,

$$V_{in} = V_f, V_{in} = R i_{in}, i_{in} = V_{in}/R$$

and since input current is zero,

$$i_L = i_{in} = V_{in}/R$$

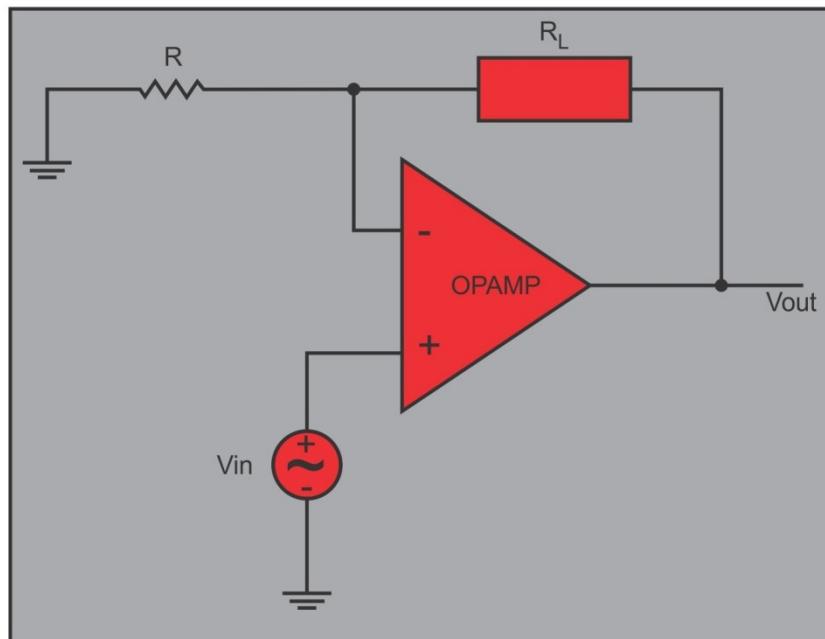


Fig 5.36 Voltage to current converter

The value of load resistance is neglected. Therefore, the output current is independent of the load resistance. The input voltage is converted into current. Thus the load current is supplied by the source.

5.14 Current to Voltage converter

Voltage signals are relatively easy to produce directly from transducer devices, whereas accurate current signals are not. A current to voltage converter is an op amp circuit which accepts an input current and gives an output voltage that is proportional to the input current

Current-to-voltage converters are used with sensors that have a current response that is more linear than the voltage response. In electronics, a transimpedance amplifier (TIA) is a current-to-voltage converter, most often implemented using an operational amplifier. One example of such an application is using the photodiode sensor to measure light intensity.

Generally, a transimpedance amplifier, (TIA) is a current-to-voltage converter; implemented using an op-amp. Current-to-voltage converters are used with sensors that have a current as the response that is more linear than that of the voltage response. The transimpedance amplifier presents low impedance to the photodiode and isolates it from the output voltage of the operational amplifier. In its simplest form a transimpedance amplifier has just a large valued feedback resistor, R_f . The gain of the amplifier is set by the resistor mentioned above and because the amplifier is in an inverting configuration and has a value of

$-R_f$. There are several different configurations of transimpedance amplifiers, each suited to a particular application.

In the circuit shown in figure 5.37, the photodiode is connected between ground and the inverting input of the OpAmp. The other input of the OpAmp is also connected to ground terminal. This provides a low impedance load for the photodiode, which keeps the photodiode voltage low with respect to the attained voltage. The photodiode is operating in photovoltaic mode that has no external bias. The feedback of the OpAmp keeps the photodiode current equal to the feedback current through R_f . The input offset voltage due to the photodiode is very low in this self-biased photovoltaic mode of this device.

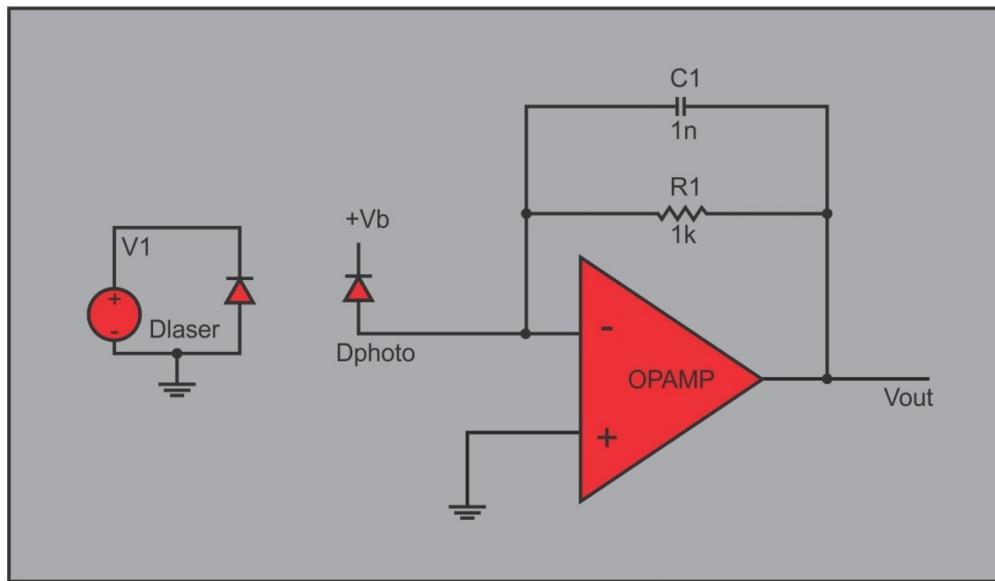


Fig.5.37 Inverting Transimpedance amplifier (TIA) with a reverse biased photodiode

$$-I_p = \frac{V_{out}}{R_f}$$

$$R_f = \frac{V_{out}}{I_p}$$

The above equation is the low frequency gain and DCof a transimpedance amplifier. If the gain is high any input offset voltage at the non-inverting input terminal of the opamp will result in an output DC offset voltage. An input bias current on the inverting terminal of the operating amplifier will similarly result in an output offset voltage.

In figure 5.37, an inverting amplifier with the photodiode driven by a laser diode is operating in the photoconductive mode is shown below. A positive voltage at the cathode of the photodiode applied as a reverse bias voltage. This reverse bias increases with the width of the depletion region and lowers the junction capacitance, improving the high frequency performance of the amplifier. The photoconductive configuration of a transimpedance photodiode amplifier is used in the situation where fast switching speed is required but high gain is not required. The feedback capacitor in the diagram, C_f is usually required to improve stability.

5.15 Summary

Operational amplifiers in the open loop configuration operate in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. The above applications are dealt in this chapter.

Operational amplifiers are used in some advanced applications like Amplitude modulation and frequency shift keying in Communication systems. Also they are used in various types of Voltage regulator circuits and frequency divider circuits. The next chapter will be dealt with all these applications.

Points to Remember:

- A Comparator is an open loop op-amp with analog inputs and a digital output.
- Reduced output voltage levels can be obtained by using back-to-back zener diodes at the output.
- Zero Crossing detector is a comparator with $V_{ref}=0$.
- Schmitt trigger is a comparator with positive feedback.
- In Schmitt trigger, the input voltage triggers the output every time it exceeds certain voltage levels called upper threshold and lower threshold voltage.
- A Monostable multivibrator is used to generate pulses of desired duration.
- An Astable multivibrator is a non-linear circuit designed using op-amp which generates square waves without any external triggering
- Circuits which offer a specified output swing are called voltage limiters. To keep the op-amp's output voltage swing between these ranges, zener diodes are added onto the circuit.
- In op-amp clipper circuits uses a rectifier diode to clip off a certain portion of the input signal to obtain a desired o/p waveform.
- In an op-amp clamper circuits, a predetermined dc level is inserted in the output volt.
- A circuit which samples an input signal and holds onto its last sampled value until the input is sampled again is called sample and hold circuit.
- The precision rectifier, which is known as a super diode, is a configuration obtained with an op-amp in order to have a circuit which behaves like an ideal diode and rectifier.
- Transconductance amplifier is a Voltage-to-current converter, implemented using an operational amplifier.

In electronics, a transimpedance amplifier, is a current-to-voltage converter, implemented using an operational amplifier.

5.16 Review Questions

1. What do you mean by a comparator?

Comparator is an open-loop op-amplifier which compares the input voltage at other one terminal to a reference voltage at other terminal and produce a voltage at their output terminal.

2. What do you mean by a zero-crossing detector?

Zero-detector is a comparator in which a zero reference is applied at their non-inverting terminal. Zero-crossing detector switches their output from one state to another state if the input voltage crosses the zero point.

3. What do mean by a Schmitt trigger?

Schmitt trigger is a type of comparator which uses positive feedback. Schmitt trigger convert an sinusoidal signal to a square wave signal.

4. How many types of Schmitt trigger used?

There are two types Schmitt trigger are used.

- Inverting Schmitt trigger.
- Non-inverting Schmitt trigger.

5. What do you mean by threshold voltage of Schmitt trigger?

The input voltage of Schmitt trigger for which the Schmitt trigger changes their output is called threshold voltage.

6. What do you mean by hysteresis of Schmitt trigger?

Hysteresis is the voltage difference between turn-on and turn-off voltage of comparator.

7. Explain the main effect of a hysteresis?

The main effect of hysteresis are-

- It improves the noise immunity.
- It reduces the response time.
- It reduces the false triggering.
- When hysteresis increases then sensitivity reduce.

8. What do you mean by a voltage to frequency converter?

A device which convert an analog voltage into a pulse signal which frequency is proportional to the applied input voltage.

9. What is the function of frequency to voltage converter?

A device which convert the frequency of the i/p signal into a proportional o/p voltage.

10. What are main applications of frequency to voltage converter?

The main applications of these are follows-

- It is used to control the speed of motor.
- It is used for rotational measurement
- It is used for digital to analog conversion.

*Review Questions***Additional Review Questions:**

- 1) What is the difference between comparator & Schmitt trigger?
- 2) What is a comparator?
- 3) What is Voltage limiting & why it is needed?
- 4) What is the difference between Clippers & Clampers?
- 5) What is Sample & hold Circuit? Why it is needed?
- 6) What is the basic difference between comparator & Schmitt trigger?
- 7) What is a Multivibrator circuit?
- 8) What is Astable multivibrator
- 9) What are Precision Rectifiers
- 10) What is the function of sample and hold circuit

5.17 Exercises:

Example 1:

An operational amplifier is to be used with positive feedback to produce a Schmitt trigger circuit. If resistor, $R_1 = 10\text{k}\Omega$ and resistor, $R_2 = 90\text{k}\Omega$, what will be the values of the upper and lower switching points of the reference voltage and the width of the hysteresis if the op-amp is connected to a dual $\pm 10\text{V}$ power supply.

Given: $R_1 = 10\text{k}\Omega$, $R_2 = 90\text{k}\Omega$. Power supply $+V_{CC} = 10\text{V}$ and $-V_{CC} = 10\text{V}$.

Feedback Fraction:

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{10\text{k}\Omega}{10\text{k}\Omega + 90\text{k}\Omega} = 0.1$$

Upper Voltage Trip Point, V_{UTP}

$$UTP = \left(\frac{R_1}{R_1 + R_2} \right) \times (V_{CC}) = +\beta V_{CC}$$

$$\therefore UTP = 0.1 \times (+10) = +1.0\text{ V}$$

Lower Voltage Trip Point, V_{LTP}

$$LTP = \left(\frac{R_1}{R_1 + R_2} \right) \times (-V_{CC}) = -\beta V_{CC}$$

$$\therefore LTP = 0.1 \times (-10) = -1.0\text{ V}$$

Hysteresis width:

$$V_{(HYS)} = UTP - LTP$$

$$V_{(HYS)} = +\beta V_{CC} - (-\beta V_{CC}) = 1.0\text{V} - (-1.0\text{V}) = 2.0\text{V}$$

$$Also: V_{(HYS)} = \beta V_{CC} - (-\beta V_{CC})$$

Then the reference voltage V_{REF} , switches between $+1\text{V}$ and -1V as the output saturates from one level to the other. Hopefully we can see from this simple example that the width of this hysteresis, 2 volts in total,

can be made larger or smaller simply by adjusting the voltage divider ratio of the feedback resistors R_1 and R_2 .

Example 2:

An op-amp multivibrator circuit is constructed using the following components.

$R_1 = 35\text{k}\Omega$, $R_2 = 30\text{k}\Omega$, $R = 50\text{k}\Omega$ and $C = 0.01\mu\text{F}$. Calculate the circuits frequency of oscillation.

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{30\text{k}\Omega}{35\text{k}\Omega + 30\text{k}\Omega} = 0.462$$

$$T = 2RC \ln\left(\frac{1 + \beta}{1 - \beta}\right) = 2RC \ln\left(\frac{1 + 0.462}{1 - 0.462}\right)$$

$$T = 2 \times (50\Omega \times 0.01\mu\text{F}) \times \ln(2.717)$$

$$\therefore T = 0.001 \times 1 = 0.001\text{Sec or } 1\text{mS}$$

$$\therefore f = \frac{1}{T} = \frac{1}{0.001} = 1,000\text{ Hz or } 1\text{ kHz}$$

Then the frequency of oscillation is calculated as 1kHz. When $\beta = 0.462$, this frequency can be calculated directly as: $f = 1/2RC$. Also when the two feedback resistors are the same, that is $R_1 = R_2$, the feedback fraction is equal to 3 and the frequency of oscillation becomes: $f = 1/2.2RC$.

We can take this op-amp multivibrator circuit one step further by replacing one of the feedback resistors with a potentiometer to produce a variable frequency op-amp multivibrator as shown.

Advanced Applications of Operational Amplifiers

The earlier chapters focused on building a basic understanding of operational amplifiers and their applications in amplifiers, oscillators, active filters etc. With this background in mind, this last chapter will cover the use of operational amplifiers in advanced applications including amplitude modulation and frequency shift keying circuits; design frequency dividers, automatic gain and voltage controllers using op-amps.

In this chapter, readers will also understand the working of various voltage regulators and be equipped to design fixed and adjustable voltage regulators.

Topic	Page
6.1 Introduction	212
6.2 Series Voltage Regulation	214
6.3 Shunt Voltage Regulation.....	218
6.5 Switching Regulators	222
6.6 Dual Power supply.....	227
6.7 Characteristics of standard regulator ICs – TPS40200, TPS40210.....	227
6.8 Phase Locked Loops	229
6.9 AGC/ AVC using op-AMP and analog multipliers:.....	242
6.10 Amplitude modulation using analog multiplier	245
6.11 Summary:	246
6.12 Review Questions.....	247
6.13 Exercises	248

6.1 Introduction

Operational amplifiers have several advanced applications. We discuss voltage regulators and power supplies followed by phase locked loops and their applications in communication engineering. We also present basic switching regulator and characteristics of standard regulator ICs.

6.1.1 Need for Voltage Regulators

Unregulated voltage supplied by the electricity company fluctuates greatly depending on various factors including condition of local power grid, the time of the day and the number of devices that are turned ON and OFF. These factors cause the voltage to swing from very low value to a significantly high value. Any electrical equipment directly connected an unregulated supply voltage suffers from one or many of the following issues (not limited to):

- Performance Degradation
- Reduced lifespan
- Hard drive failure
- Memory reboots

Voltage regulators compensate for this problem by raising or lowering the in- coming voltage in order to put out a steady supply voltage

Why can't we use a simple voltage divider for regulating voltages?

Consider a simple voltage divider equation:

$$V_{out} = V_{in} \cdot \frac{R_2}{R_1 + R_2} - i_{out} \cdot R_1 || R_2 \quad (6.1)$$

It is obvious from eq. 1, that the output voltage depends on the input voltage V_{in} and the output current i_{out} . With variable and low impedance load being quite common, a voltage divider circuit cannot provide fixed voltage to such loads. However, we will see, as we progress in this chapter, that a voltage regulator will, within its limits, maintain the output voltage irrespective of variations in input voltage and load current.

6.1.2 Voltage Regulation

An ideal voltage regulator provides a constant output voltage irrespective of variations in input (line) voltage or load current demand. In other words, a voltage regulator provides constant DC output voltage independent of the input voltage, output load current and temperature [1]. The input voltage to a regulator can be from one of the following:

- Filtered output of a rectifier, derived from ac voltage
- Battery, in case of portable systems

Thus, the heart of any regulated power supply is a voltage regulator that provides a constant voltage reference.

As mentioned before, the function of a regulator is to provide constant reference voltage under varying input voltages and or load conditions. Thus, the performance of a voltage regulator can be measured in terms of the following:

Line Regulation: It is a measure of the ability of a regulator circuit to maintain a prescribed voltage level under varying input voltages. Line regulation is also referred to as input or supply regulation.

$$\text{Line Regulation} = \frac{\Delta V_o}{\Delta V_{in}} \quad (6.2)$$

Note: Line Regulation is also specified as change in output voltage per volt divided by change in input voltage.

Load Regulation: It is a measure of the ability of a regulator circuit to maintain a prescribed output voltage level, under varying load conditions.

$$\text{Load Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \quad (6.3)$$

In eq.3, V_{NL} and V_{FL} refer to the output voltage with no **load** and the output voltage with full load respectively. It is worth noting that eq.3, considers the variations in load alone, while keeping the input voltage and temperature constant (typically 25 degree).

Can load regulation be specified differently?

Load regulation is also specified in terms of equivalent output resistance of a power supply R_{out} . In such circumstances, the Thevenin voltage corresponds to voltage with no load, R_{out} corresponds to the Thevenin resistance and R_L is the load connected.

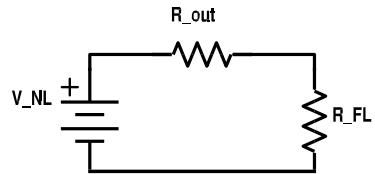


Figure 1: Thevenin Equivalent Of Power Supply with load

$$V_{FL} = V_{NL} - \frac{R_{FL}}{R_{out} + R_{FL}} \quad (6.4)$$

Substituting eq.4 in eq.3 and rearranging terms, we get the load regulation in terms of the equivalent output resistance, as

$$\text{Load Reg In.} = \frac{R_{out}}{R_{FL}} \times 100\% \quad (6.5)$$

Thermal Coefficient: It is the regulator's ability to maintain the pre-scribed output voltage level under temperature variations. Denoted by TC (V_o), it is expressed mathematically as

$$TC(V_o) = \frac{\Delta V_o}{\Delta T} \text{ measured in V/oC} \quad (6.6)$$

Are voltage stabilizers and regulators the same?

- Voltage Stabilizer: Reduces variations in voltage of the supply to some other apparatus. Corrects for input voltage changes only, but not for changes in load.
- Voltage Regulator: Maintains output voltage takes into account both input supply and load variations.

Voltage regulators are categorized as linear regulators and switching regulators. Linear regulators are further classified as series regulator and shunt regulators.

6.2 Series Voltage Regulation

A simple series voltage regulator can be constructed using a zener diode. However, we based linear regulator.

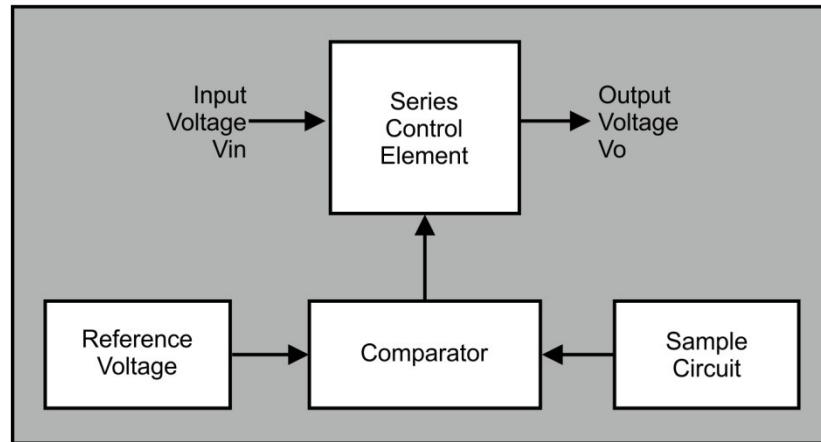


Fig 6.1 Linear Regulator (Series Regulation)

Fig 6.1 gives the block level details of a linear, series type voltage regulator. The control element is in series with the load between input and output. The sample circuit senses change in the output voltage. The error control circuit compares the sample voltage with the reference voltage, causing the control element to compensate so as to maintain a constant output voltage. The error voltage is typically the change from quiescent bias voltage.

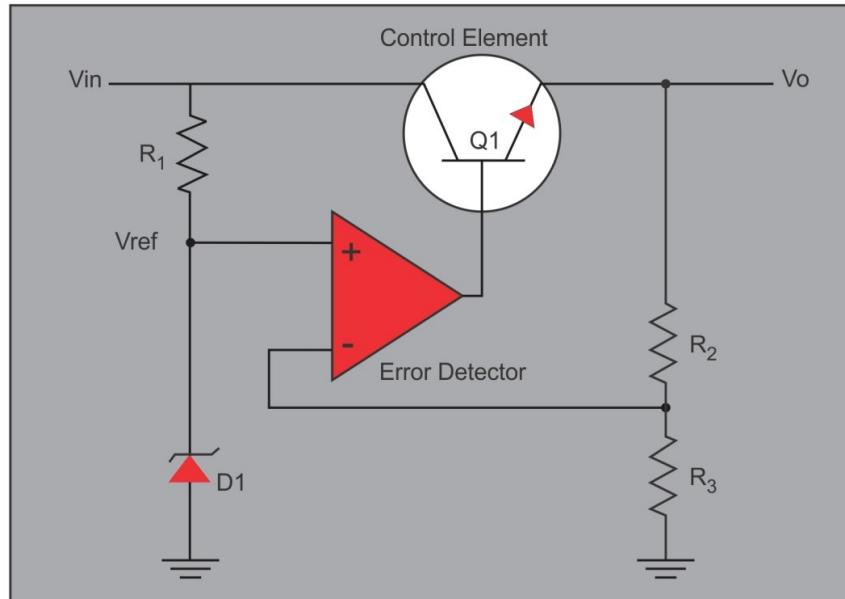


Fig 6.2 Linear Regulator (Series Type)

Fig 6.2, illustrates an Op-amp based series regulator. Comparing this circuit with the block diagram given in Fig 6.1, we establish the following:

- Series Control Element - *npn* transistor Q1
- Comparator - Op - Amp (Error Detector)
- Reference Voltage - Provided by the reverse biased zener diode D1
- Sample Circuit - R_2 and R_3 voltage divider circuit

Having established the similarity between the block diagram and the circuit, we now discuss the working of this series regulator. This, we do in two phases:

Phase - 1: Output voltage tries to decrease as result of decrease in input voltage or change in load current (R_L decreases)

- Voltage across the resistive divider, R_2 and R_3 decreases proportionally.
- This reduced voltage is directly applied to the inverting terminal of the op-amp.
- The non-inverting terminal of the op-amp is held at a constant voltage (fixed reference) by the reverse biased zener diode D1.
- A voltage difference between the op-amp input terminals develops.
- This difference voltage is amplified, causing the op-amp output voltage to increase.
- This increase in output voltage of the op-amp, applied to the base of Q1 causes the emitter voltage to increase. The emitter voltage is nothing but the output voltage of the regulator, V_o .
- V_o increases until the voltage at the inverting input terminal of the op-amp equals the reference voltage provided by the zener diode D1.
- This, in turn, compensates for the attempted decrease in the output voltage, thus keeping the output voltage, almost a constant.

Phase - 2: Output voltage attempts to increase as a result of increase in supply voltage or change in load current (R_L increases)

- With increase in V_{in} or R_L , V_o attempts to increase.
- The voltage applied to the inverting terminal of the op-amp increases.
- The op-amp is connected as a non-inverting amplifier with reference voltage, being the input at the non-inverting terminal.
- The sampling circuit, formed by the resistive divider, R_2 and R_3 act as the feedback resistors, providing the negative feedback, for the non-inverting amplifier.
- The base voltage applied to Q1 attempts to decrease.
- This leads to reduction in emitter voltage V_o .

In this case, the decrease in base voltage compensates for an attempted increase in V_o by decreasing the emitter voltage of Q1.

Observe the following [1]

When the output voltage attempts to increase, we noted that the op-amp acts as a non-inverting amplifier, with the resistive divider providing the negative feedback and the input at the non-inverting terminal being the reference voltage provided by zener diode $D1$. In this case,

$$V_o = (1 + R_2/R_3) V_{REF} \quad (6.7)$$

Thus we note that the output voltage is independent of the input voltage and the load connected. The output voltage depends only on the reference voltage provided by the zener diode and the feedback ratio R_2/R_3 , thus achieving regulation. This works only when the input voltage and load currents are well within the limits specified.

Having seen the working of the regulator circuit, we now try to answer some critical questions concerned with load failure.

- **What happens when there is a load failure?** - It is not uncommon for the supply to be accidentally short-circuited, due to load failure. An output short-circuit current tends to damage the regulating circuitry, as the pass transistor attempts to increase the short-circuit voltage by increasing the output current, *very quickly* beyond the allowable limits.
- **How do we avoid problems due to load failure?** - To avoid this, we modify the regulator, incorporating the over-current sensing circuit, which remains inactive in normal operation, but becomes active when the current exceeds a preset value.
- **What does the modified regulator circuit look like?** - A small modification to the circuit given in fig. 3 will help in overcoming problems due to excessive amount of load current being drawn.

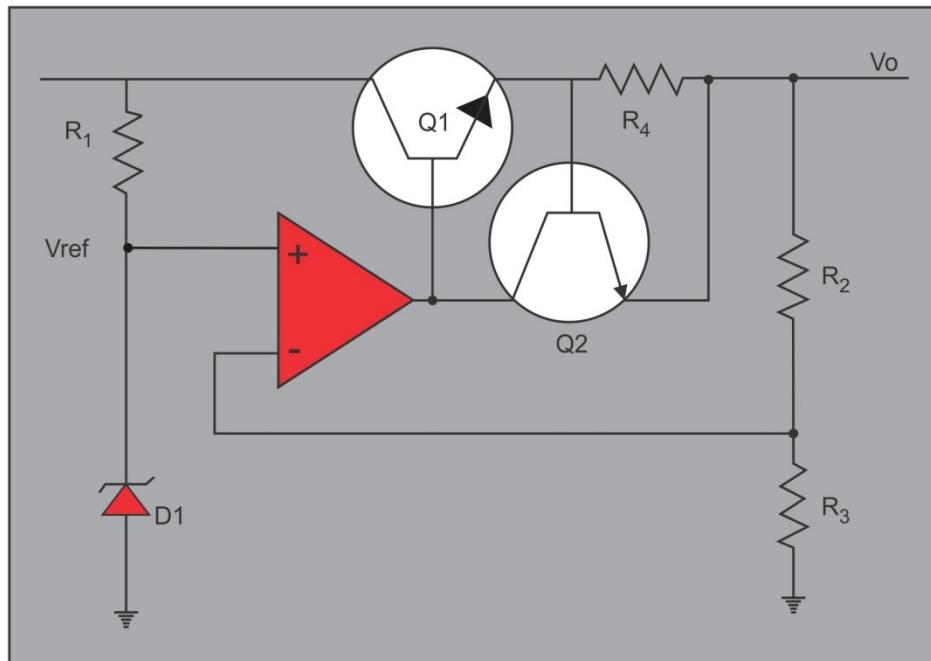


Fig 6.3 Constant Current Regulator

- **How does the circuit work?** - The current from the pass transistor Q1, emitter is passed through R_4 , a small current-sensing resistor placed in series with the load. The emitter junction of transistor Q2 monitors the voltage drop across R_4 . When the voltage drop is large enough, Q2 turns ON, diverting the current from pass transistor base and thereby limiting the emitter current of Q1.
- **What is the constraint on maximum current permitted?** - The constraint is the allowable dissipation in the pass transistor Q1. The maximum dissipation for Q1 occurs with maximum rated load current and the *minimum* rated output voltage.
- **What is the maximum load current?** - As V_{BE} of Q2 cannot exceed 0.7V, the voltage drop across R_4 is held to this value and hence the load current is limited to

$$I_L(\max) = \frac{0.7}{R} \quad (6.8)$$

Thus, we see that the load current is restricted to a maximum constant value, as determined by eq. 6.8

- **If the load current is restricted to a maximum value, what do we do in high-current regulators?** - Fold-back current limiting is employed in high-current regulators.
- **How does a regulator employing fold-back current limiting work?**
The output current under overload condition drops to a value well below the peak load current capability and prevents excessive dissipation.
- **How is the regulator circuit modified to employ fold-back current limiting?**

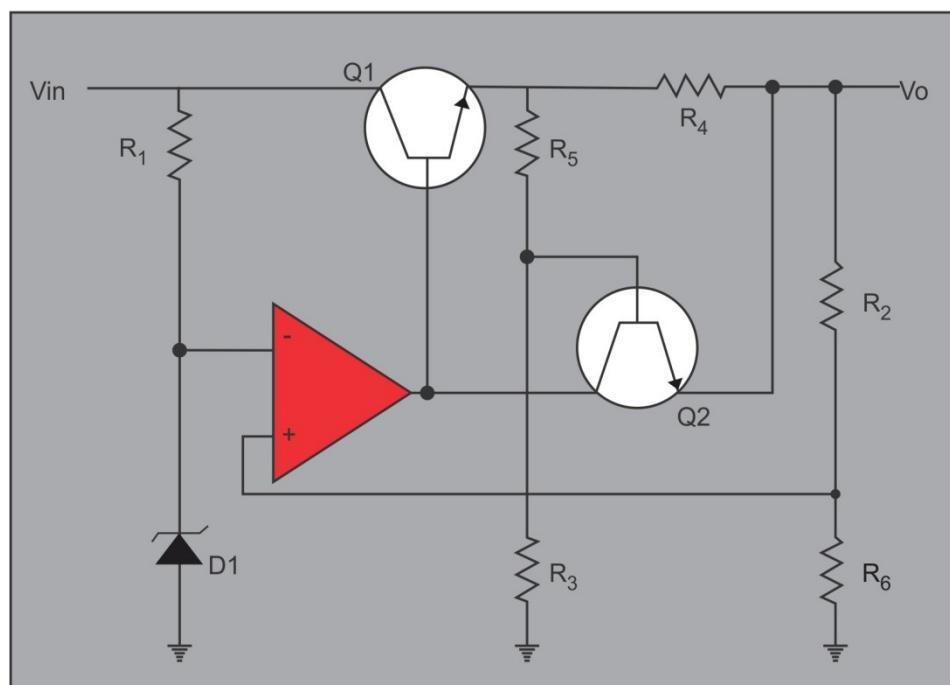


Fig 6.4 Regulator with fold-back current limiting

Fig 6.4 shows a series regulator employed with fold-back current limiting. The working of the circuit is as follows:

- R_5, R_6 divider senses the voltage at the emitter of Q1.

- When the load current increases to its maximum value the voltage across R_4 becomes large enough to turn on Q_2 .
- This action provides the current limiting.
- In case the load becomes smaller, the voltage driving Q_2 ON, becomes less, thus leading to drop in load current.
- When the load resistance is returned to its rated value, the circuit resumes normal voltage regulation.

6.3 Shunt Voltage Regulation

A shunt voltage regulator regulates the output voltage by shunting current away from the load. The block diagram of the same is given in Fig 6.5

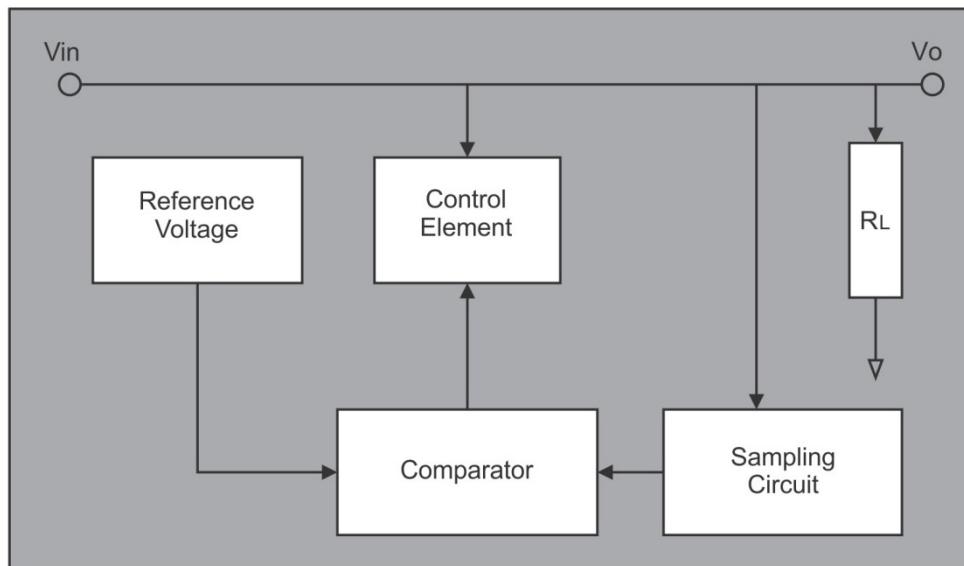


Fig 6.5 Linear Voltage Regulator - Shunt type

We note from Fig 6.5 that the current to the load is provided by the unregulated power supply. The control element draws some current to maintain the regulated output voltage across the load. If the load voltage changes due to change in load, the sampling circuit gives feedback signal to the comparator circuit. Comparator provides the necessary control signal to vary the amount of current shunted away from the load.

If the output voltage attempts to increase, the sample circuit provides a feedback to the comparator, which in turn provides a control signal to draw increased shunt current, providing less load current, thereby keeping the regulated voltage from increasing.

Observe the following

In series voltage regulator, the control element is in series with the load, as illustrated in fig.2. We see that in shunt voltage regulator, the control element is in shunt with the load, as in fig. 6.

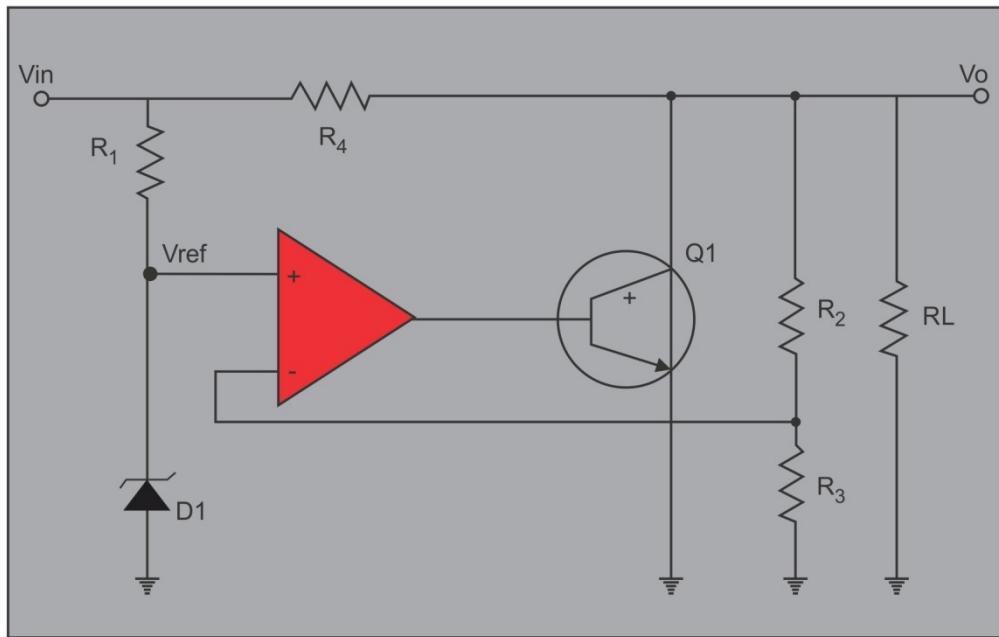


Fig 6.6 Shunt type voltage regulator

The feedback voltage provided by the resistive divider is compared with the zener reference voltage, as in Fig 6.6. The comparator provides the control drive current to the shunt element Q1. The current through R4 is thus controlled to drop a voltage across R4 to maintain the output voltage. 6.4 Switching Regulation

Switching regulator circuit is known for its efficient power transfer to the load. A switching regulator passes voltage to the load in the form of pulses, which are then filtered, providing a smooth dc voltage.

In series and shunt regulators, the control elements conduct all the time, with amount of conduction varying depending on the variations in output voltage or current.

The control element in switching regulator operates as a switch. This has a direct effect on the power dissipation, in the sense that the transistor is not always conducting. As a result, the switching regulators can provide higher load currents at low voltage.

There are three types of switching regulators - step down, step-up and in-verting. The following discussion will throw more light on each of these types.

6.4.1 Step-down type

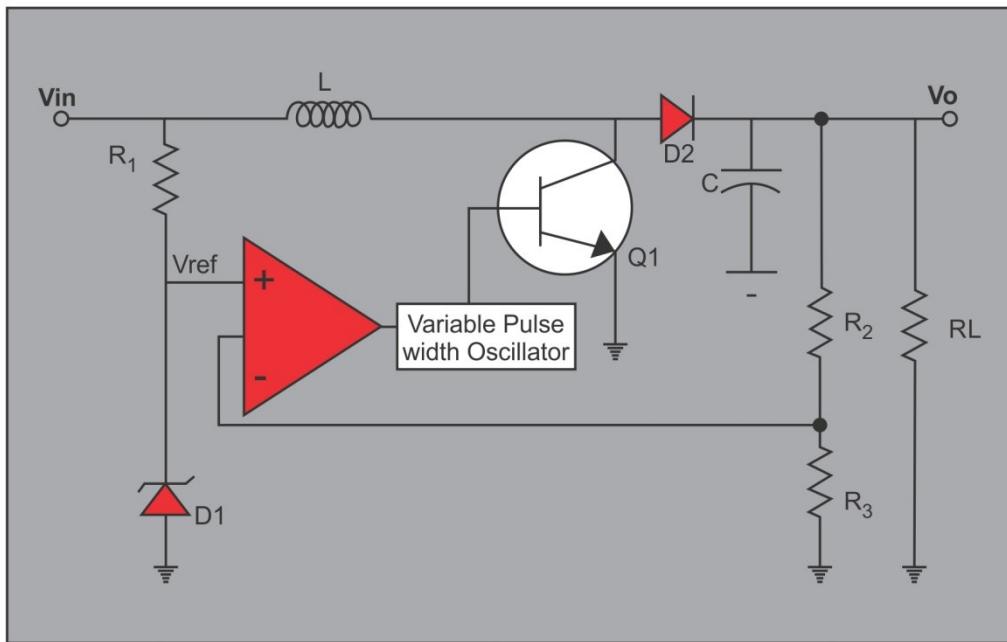


Fig 6.7 Step-down type shunt voltage regulator

As the name suggests, this configuration is characterized by an output voltage which is always less than the input voltage. Q1 switches the input voltage at a duty cycle determined by the regulator's load requirement. Q1 is either saturated (ON) or cutoff (OFF) and hence there is less power dissipated in the control element.

The output voltage fluctuations caused by charging and discharging of the capacitor are smoothed by the inductor. Also, the output voltage can be varied by adjusting the ON time and OFF time. In other words, the output voltage can be varied by varying the duty cycle.

Observe the following

- When V_o attempts to decrease, the ON time of Q1 is increased.
- Increase in ON time of Q1 results in additional charge on the capacitor C.
- This compensates the attempted decrease in V_o .
- When V_o attempts to increase, the ON time of Q1 is decreased.
- This causes the capacitor C to discharge enough, compensating the attempted increase.

6.4.2 Step-up type

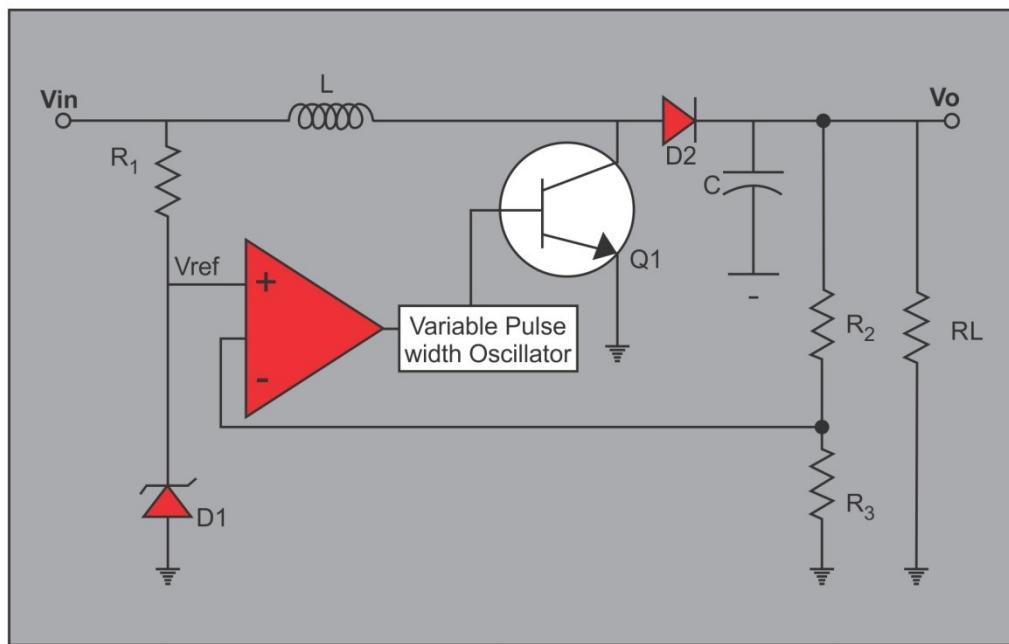


Fig 6.8 Step-up type shunt voltage regulator

Control element Q1 in the circuit, shown in Fig 6.8 acts as a switch to ground in this configuration. Let us now discuss the working of this circuit in two phases, as before.

Q1 ON:

- When Q1 turns ON, V_{in} volts is induced across the inductor.
- During the ON time of Q1, diode D2 is reverse biased. The inductor voltage decreases as long as Q1 is ON.
- In this interval when Q1 is ON, the capacitor discharges through the load.

Q1 OFF:

- When Q1 turns OFF, the polarity of the inductor voltage reverses and adds to the input voltage V_{in} .
- D1 is forward biased.
- Capacitor C charges.

Note: The output voltage is equal to the capacitor voltage. This can be larger than V_{in} and the capacitor charges to a voltage which is the sum of input voltage V_{in} and the voltage across the inductor, L.

Observe the following

- When V_o attempts to decrease, the ON time of Q1 increases.
- Increase in ON time of Q1, results in increase in the amount those capacitor C charges to.
- This compensates the attempted decrease in V_o .
- When V_o attempts to increase, the ON time of Q1 decreases.
- This causes the capacitor C to charge to a lower value.
- In either case, the output voltage V_o is held at a constant level as a result of this regulating action.

As mentioned before, the voltage regulation is achieved as a result of varying the ON time of the control element Q1.

6.5 Switching Regulators

Linear regulators are typically used in low powered devices. They work by taking difference between the input and output voltages and burn it up as waste heat. Linear regulators have very low efficiency ranging from 14% to 40% [7]. This also requires the use of bulky and expensive heatsinks. To overcome this, we employ switching regulators. These work by taking small chunks of energy from the input to the output. This task is accomplished by using an electrical switch and a controller which determine the rate of transfer of energy to the output and hence the name, switching regulator. They typically have an efficiency of 85%. With the efficiency of switching voltage regulators less dependent on the input source, they can power useful loads from higher voltage sources. Switching regulators also allow generation of multiple output voltages of different polarities from a single input voltage. They find wide applications in portable phones, video game platforms and for personal computers. The four most commonly used switching regulators are [4]:

- Buck converter - a voltage steps down, current step up converter
- Boost converter - a DC-to-DC power converter with an output voltage greater than its input voltage
- Buck-Boost converter - a switched mode power supply that combines the principles of buck and boost converter in a single circuit.
- Flyback converter - a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation.

We discuss these switching regulators in this section.

6.5.1 Buck Regulator

The most commonly used switching regulator is the buck converter. Buck converter is used to down-convert an input DC voltage to a lower DC voltage output of the same polarity. The DC input can be a rectified AC or a DC supply. The buck configuration is used in SMPS circuits in which the output DC voltage is lower than the input DC voltage.

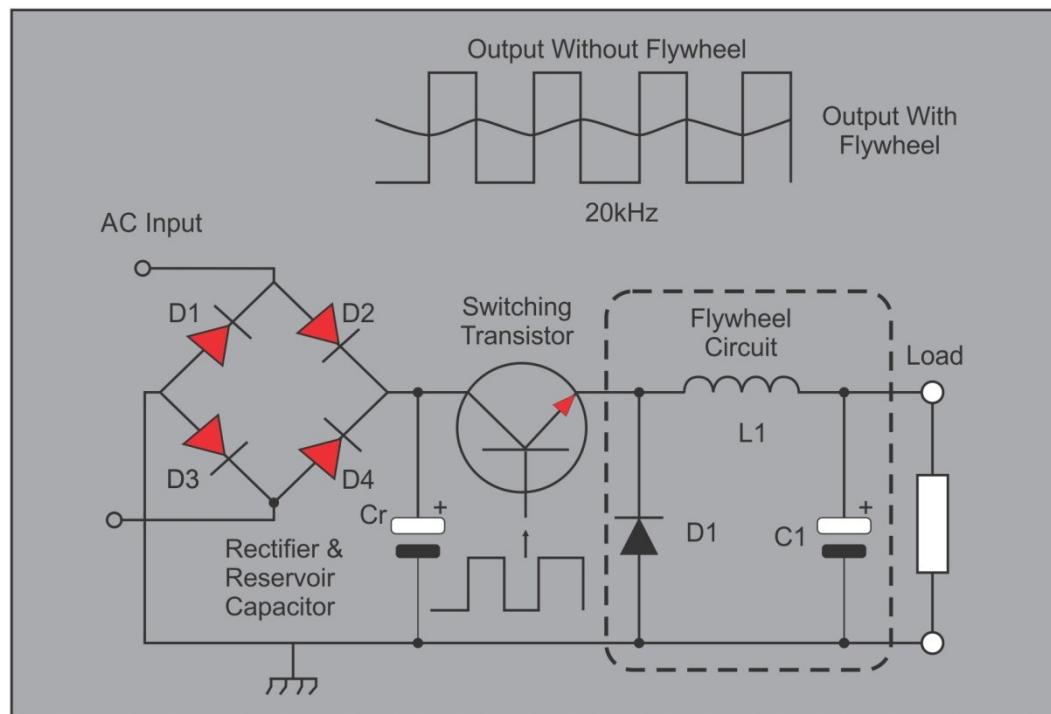


Fig 6.9 Buck Regulator

The buck converter, shown in Fig 6.9 uses a transistor switch to alternately connect and disconnect the input voltage to an inductor.

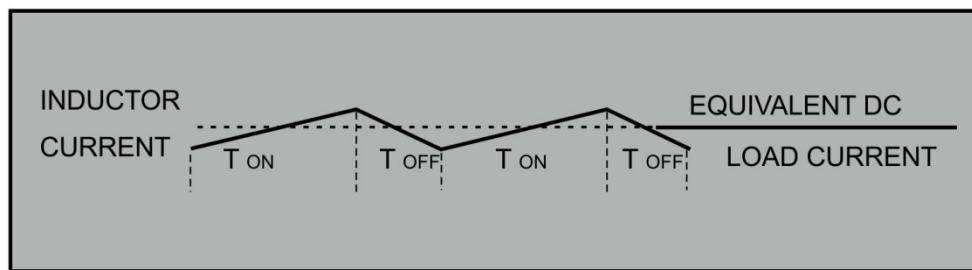


Fig 6.10 Current through the inductor in a buck regulator

When the switch is turned ON, the input voltage is connected to the inductor, causing the current through inductor to increase. This current flows through both the load and the output capacitor charges during this time. When the switch is turned off, the input voltage applied to the inductor is cutoff. As the current in the inductor cannot change instantly, the voltage across the inductor will adjust to hold the current constant. However, the input end of the inductor is forced negative in voltage, by the decreasing current, eventually making the diode turn ON. The inductor current then flows through the load and back through the diode.

During the OFF time, the capacitor discharges into the load, contributing to the current supplied to the load, the total load current being the sum of inductor and capacitor current. The DC load current from the regulated output is the average value of the inductor current.

The current through the inductor is given in Fig 6.10. The current through the inductor increases when the switch is ON and decreases when the switch is OFF. The peak to peak difference in the inductor current waveform is called the inductor ripple current.

6.5.2 Boost Regulator

The boost regulator, shown in Fig 6.11 takes in a DC input voltage and produces an output voltage which is higher than the input and of the same polarity.

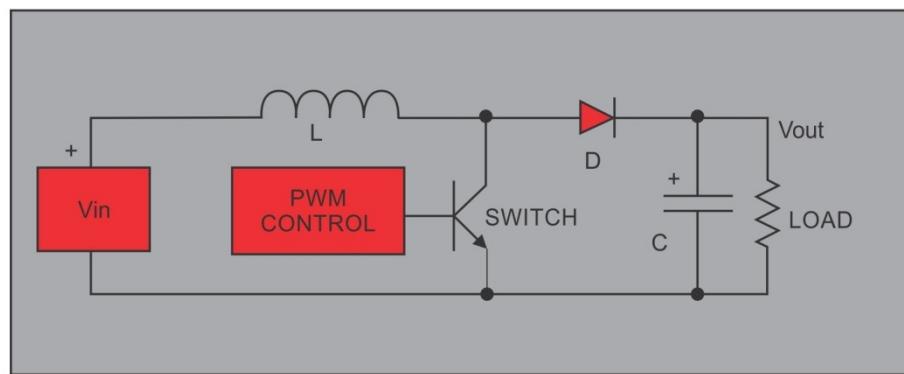


Fig 6.11 Boost Regulator

When the switch is ON, the input voltage is forced across the inductor, making the current through the inductor rise. When the switch is OFF, the inductor current decreases, making the switch end of the inductor swing positive, forward biasing the diode, allowing the capacitor to charge to a voltage higher than the input voltage. Note that when the switch is ON, the load current is supplied by the capacitor. One of the important design considerations for boost regulator is that the output load current and the switch current are not equal. Also, the maximum available load current is always less than the current rating of the switching transistor. Since the output voltage of the boost regulator is higher than the input voltage, the output current must be lower than the input current.

6.5.3 Buck-Boost Regulator

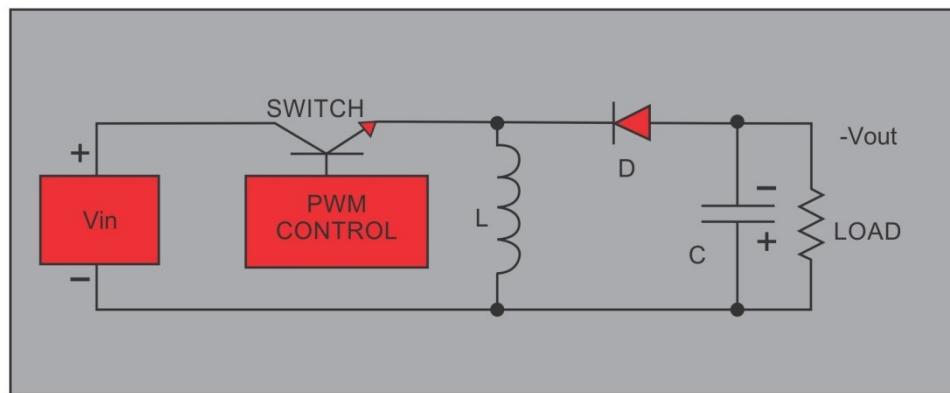


Fig 6.12 Buck-Boost Regulator

The buck-boost regulator, in Fig 6.12 is an inverting regulator that takes a DC input voltage and produces a DC output voltage, opposite in polarity to the input. The negative input voltage can be larger or smaller than the input voltage.

When the switch is ON, the input voltage causes a current to flow through the inductor. During this time, the discharging capacitor acts as the only source of load current. This also requires that the charge lost from the output capacitor during the ON time of the switch be replenished during the OFF time.

When the switch turns OFF, the decreasing current in the inductor causes the voltage at the diode end of the inductor to swing negative, causing the diode to turn ON. This allows the inductor current to supply both output capacitor and the load. Note that the load current is supplied by the inductor when the switch is ON and by the capacitor when the switch is OFF. During ON period, the circuit behaves as a buck regulator and in OFF period, it behaves as a boost regulator.

6.5.4 Flyback Regulator

The most versatile among all the regulator topologies, the Flyback regulator in Fig 6.13 offers flexibility to create one or more output voltages, some of which may be opposite in polarity. These regulators are quite popular in battery powered systems, where a single voltage must be converted to multiple system voltages with very high power conversion efficiency.

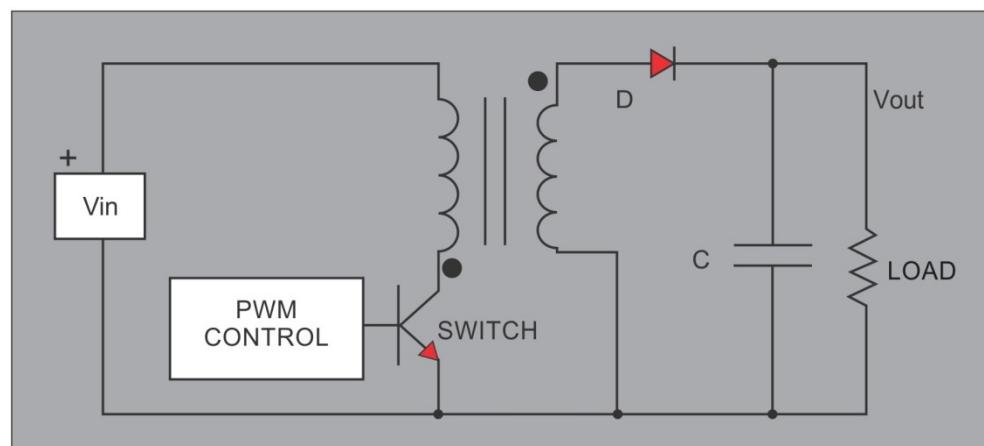


Fig 6.13 Flyback Regulator

The important feature of the Flyback regulator is the transformer phasing indicated by the dots on primary and secondary windings. When the switch is ON, the input voltage is forced across the primary, causing current to flow through it. The voltage induced in the secondary is of the same polarity (more negative, as in the primary). The diode is reverse biased and is turned OFF. Thus there is no current flow in the secondary winding when the switch is ON. The load current is thus supplied by the output capacitor. When the switch turns OFF, the decreasing current flow in the primary causes voltage at the dot end to swing positive. Simultaneously, the primary voltage is redirected to the secondary with the same polarity. This causes the diode to turn ON allowing current to flow through both the load and the output capacitor. The output capacitor charges for this period.

Generating multiple voltages using Flyback regulator

As mentioned earlier, the biggest advantage of a flyback regulator is its ability to provide multiple outputs, as shown in Fig 6.14

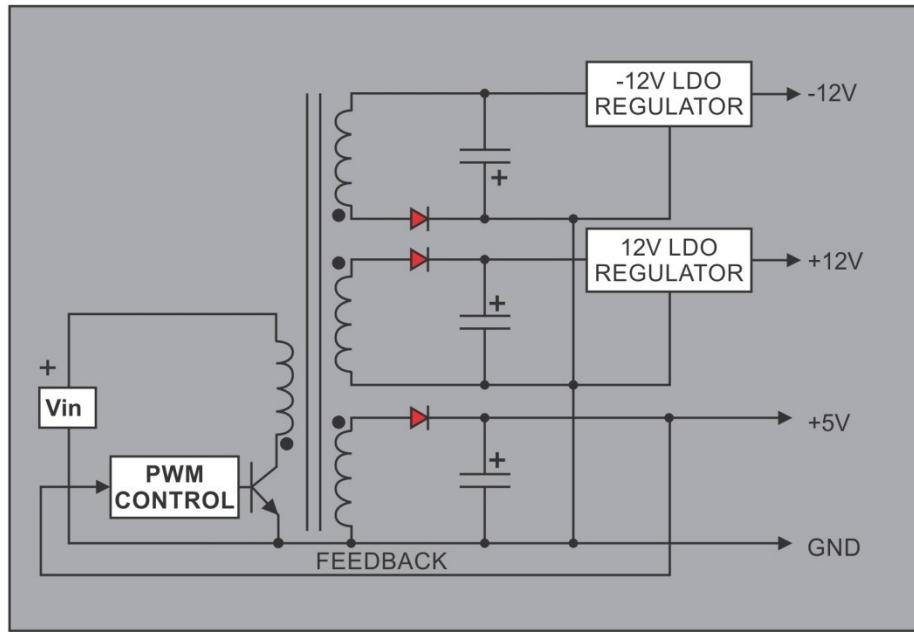


Fig 6.14 Multiple output Flyback regulator

One of the outputs, typically the highest current output is selected to provide a pulse width modulated feedback to the control loop, thus making this output directly regulated.

The other secondary windings are indirectly regulated as their pulse width follows the regulated winding. The load regulation on the unregulated secondary is typically around 5 - 10%, but adequate for many applications.

6.6 Dual Power supply

Dual voltage power supply architectures are becoming common place in high performance microprocessor and digital signal processor (DSP) systems. A Dual power supply provides positive polarity, negative polarity and ground potential. Some Op Amps need dual power source that is +Vcc and -Vcc (Positive and Negative polarity). In Texas Instruments there are a wide variety of voltage regulators which provide dual output power supply.

The TPS54340 can be used to convert a positive input voltage to a split rail positive and negative output voltage by using a coupled inductor. Ideal applications are amplifiers requiring a split rail positive and negative voltage power supply

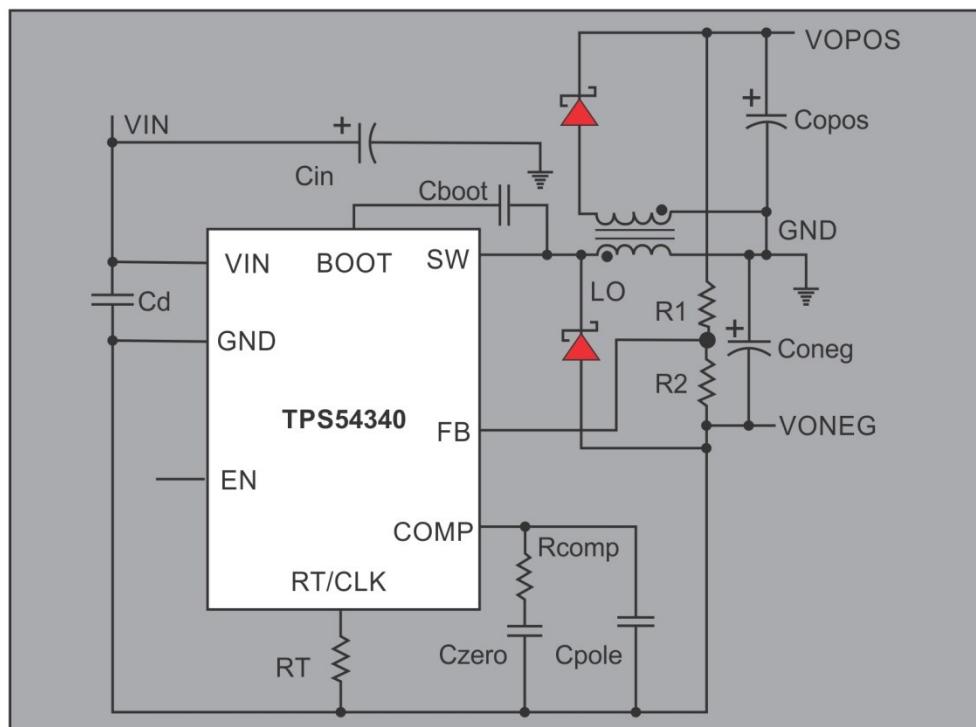


Fig 6.15 TPS54340 Split Rail Power Supply

6.7 Characteristics of standard regulator ICs – TPS40200, TPS40210

- TPS40200:** The TPS40200 is a flexible nonsynchronous controller with a built-in 200-mA driver for P-channel FETs. The circuit operates with inputs up to 52 V, with a power-saving feature that turns off driver current once the external FET has been fully turned on. This feature extends the flexibility of the device, allowing it to operate with an input voltage up to 52 V, without dissipating excessive power. The circuit operates with voltage-mode feedback and has feed-forward input-voltage compensation that responds instantly to input-voltage change. The integral 700- mV reference is trimmed to 2%, providing the means to accurately control low voltages. Clock frequency, soft start and over current limit are each easily programmed by a single, external component. The part has under voltage lockout, and can be easily synchronized to other controllers or a system clock to satisfy sequencing and/or noise-reduction requirements.

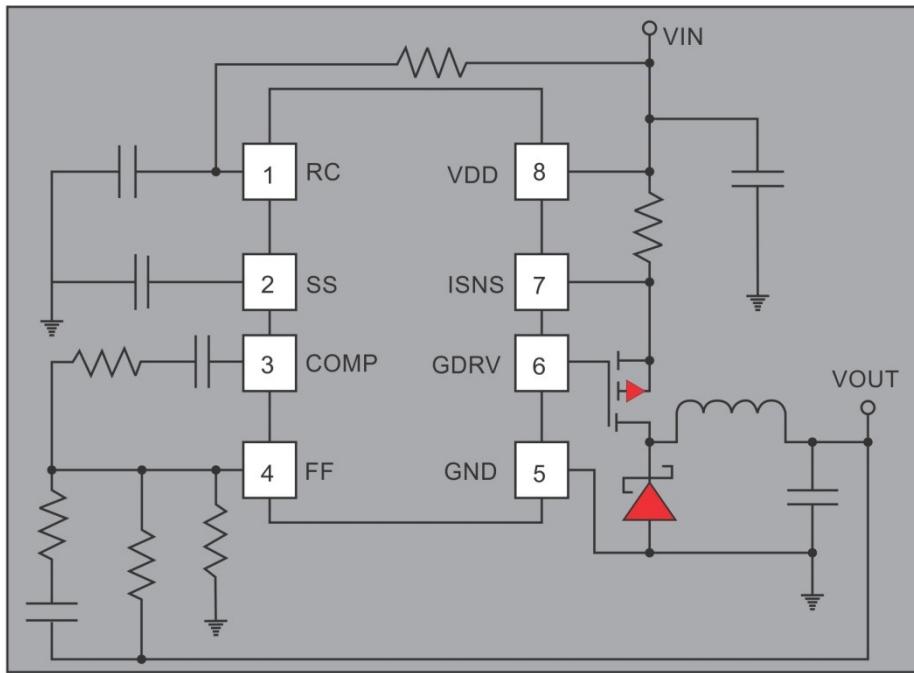


Fig 6.16 Schematic of TPS40200

Following are the features of TPS40200,

- Input Voltage Range 5.5 V to 52 V
- Output Voltage (700 mV to 87% VIN)
- 200-mA Internal P-Channel FET Driver
- Voltage Feed-Forward Compensation
- Under voltage Lockout Temperature Range
- Programmable Fixed-Frequency (35 kHz to 500 kHz) Operation
- Programmable Short-Circuit Protection
- Hiccup Over current Fault Recovery
- Programmable Closed-Loop Soft Start
- 700-mV 1% Reference Voltage with design

Application:

- Automotive Controls
 - Automotive Power Supplies
 - Distributed Power Systems
- b) TPS40210: TPS40210 is a wide-input voltage nonsynchronous boost controller. This is suitable for topologies which require a grounded source N-channel FET including boost, flyback, SEPIC and various LED Driver applications. The device features include programmable soft-start, overcurrent protection with automatic retry and programmable oscillator frequency. Current mode control provides improved transient response and simplified loop compensation. The main difference between the two parts is the reference voltage to which the error amplifier regulates the FB pin.

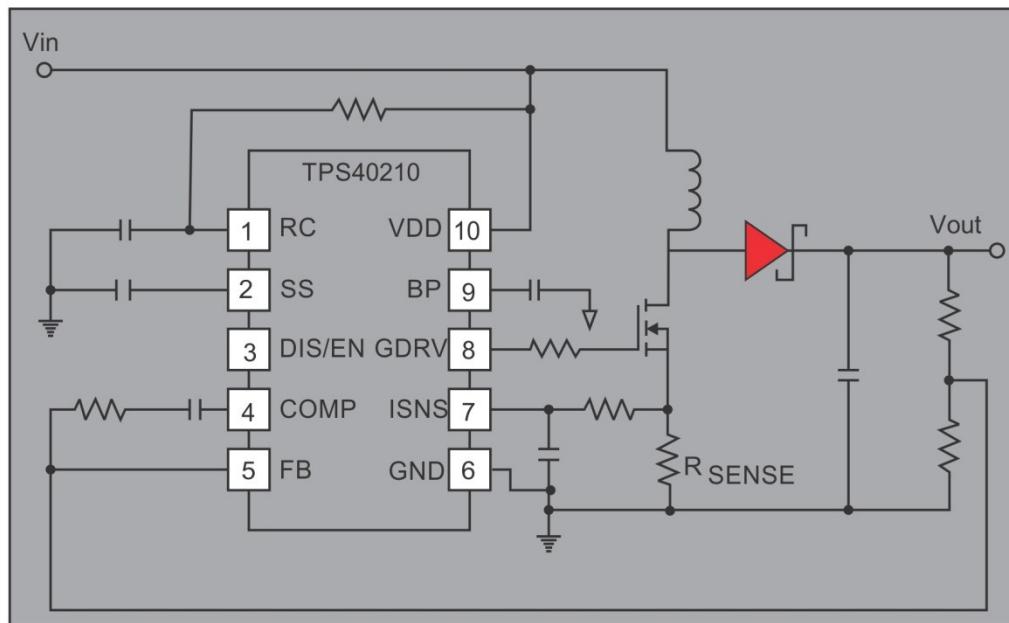


Fig 6.17: Schematic of TPS40210

Following are the features of TPS40210:

- For Boost, Flyback, SEPIC, LED Drive Apps
- Wide Input Operating Voltage: 4.5 V to 52 V
- Adjustable Oscillator Frequency
- Fixed Frequency Current Mode Control
- Internal Slope Compensation
- Integrated Low-Side Driver
- Programmable Closed-Loop Soft-Start
- Over current Protection
- External Synchronization Capable
- Low Current Disable Function

Applications:

- LED Lighting
- Industrial Control Systems
- Battery Powered Systems

6.8 Phase Locked Loops

Phase locked loops (PLL) are frequency control systems with feedback. The output of the PLL is such that its phase is related to that of the input signal. PLLs have a wide variety of applications including frequency modulation (FM), tracking filters, FM demodulators, frequency shift keying (FSK) decoders for demodulation of carrier frequencies, clock recovery circuits and so on. While each of the application mentioned above requires different characteristics, the basic circuit concept used is the same for all. In the following sections, we see the details of PLL and their applications.

6.8.1 How does PLL work?

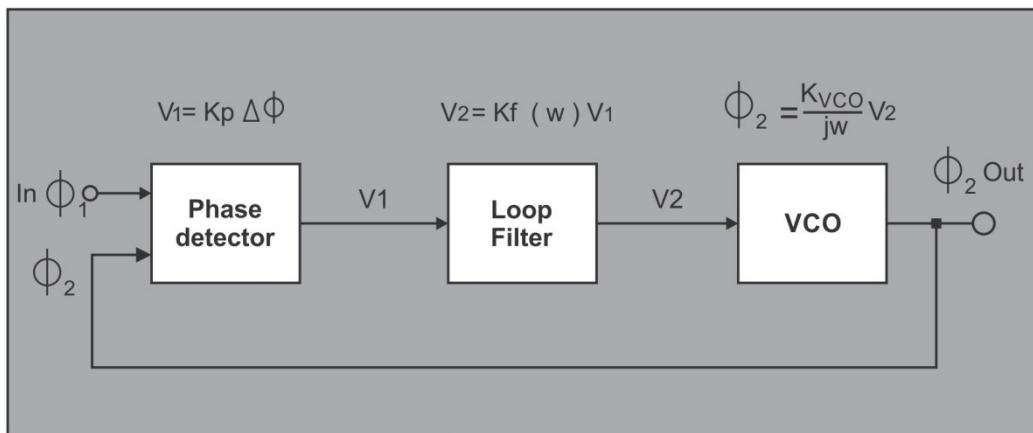


Fig 6.18: Block diagram of PLL

Fig 6.18 gives the block diagram of a phase locked loop [6]. We see that the PLL consists of a phase detector, a loop filter and a voltage controlled oscillator.(VCO). Before we get into the details of working of a PLL, we look at what the name signifies. In the context of a PLL, the term phase refers to the relative phase difference between input signal and the phase of the voltage controlled oscillator's output. Whenever the VCO's output phase is in constant relation with that of the input signal, we say that the phase of output signal is locked with that of the input. The loop in PLL refers to the presence of a feedback loop which is used for synchronizing the oscillator frequency with that of the input signal.

In other words, a PLL is a phase comparator that produces a control signal to adjust the frequency of the local oscillator in such a way that it matches the frequency of the input signal. As a result, the oscillator output is basically a locally produced copy of the input signal.

The phase detector compares the phases of its input signals and generates an output V_1 proportional to the phase difference between its input signals, $\Delta\phi$. The constant of proportionality, K_p , is measured in volts per radian. The output of the phase detector typically is in the form of pulses, which are passed through a low pass filter. Let $V_1(\omega)$ be the frequency domain representation of V_1 and let $K_f(\omega)$ be the low pass filter transfer function. $V_1(\omega)$ is multiplied by $K_f(\omega)$ to generate the control voltage $V_2(\omega)$. This voltage is applied to VCO. The division by $j\omega$ indicates that the signal is integrated in time domain and turns the frequency output into phase output. The polarities must be arranged such that if ϕ_2 lags ϕ_1 , the VCO increases frequency slightly, indicating that the feedback must be negative. The output of the VCO is fed back to the phase detector and the feedback is closed.

Phase Detectors

The phase detectors can be classified into digital and analog ones, based on the nature of the input signal and the VCO output. The other classification is Type I and Type II, depending on whether the phase difference is constant or zero. These are discussed in the subsequent paragraphs.

Digital Phase Detector

The simplest digital phase detector is an *exclusive - OR* gate, give in Fig 6.19 These are called Type - I detectors, which give a high output when the signals are anti phase (more specifically, opposite sign) and a low output when the signals are in phase (same polarity). If the two signals are of different frequencies, then the output will be a train of pulses owing to the continuous change in phase relation. The pulses fed as input to the VCO cause a change in the oscillating frequency, subsequently making the VCO output frequency equal to the input frequency. However, this may not result in same phase, but leads to a constant phase difference, as found in Fig 6.20

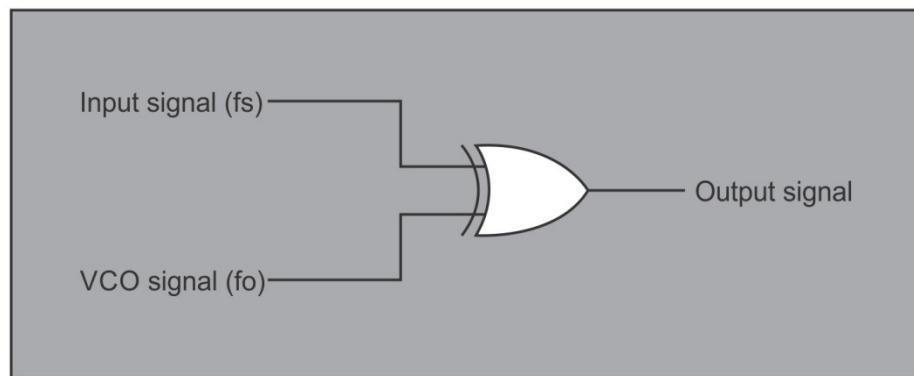


Fig 6.19 Digital Phase Detector

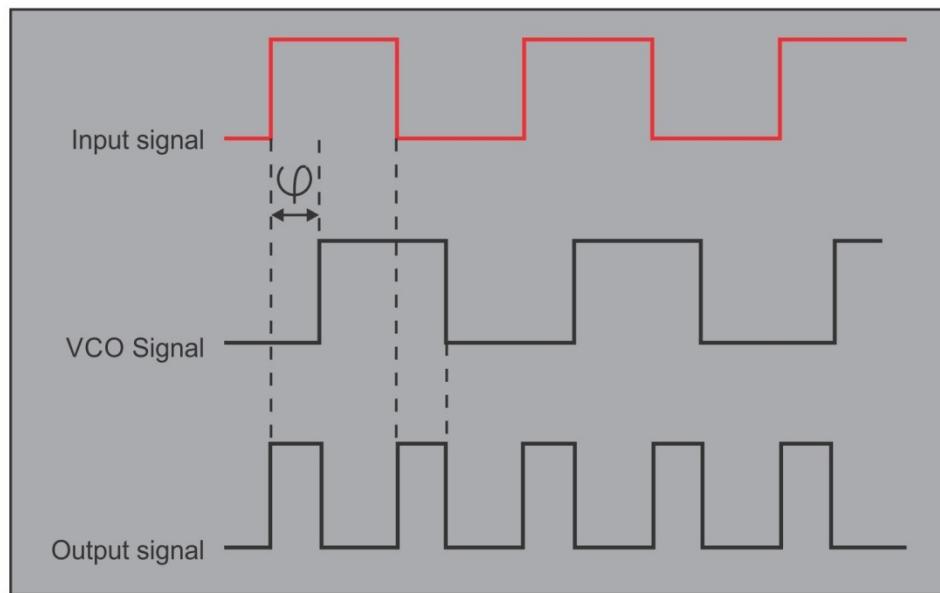


Fig 6.20 Digital Phase Detector Response

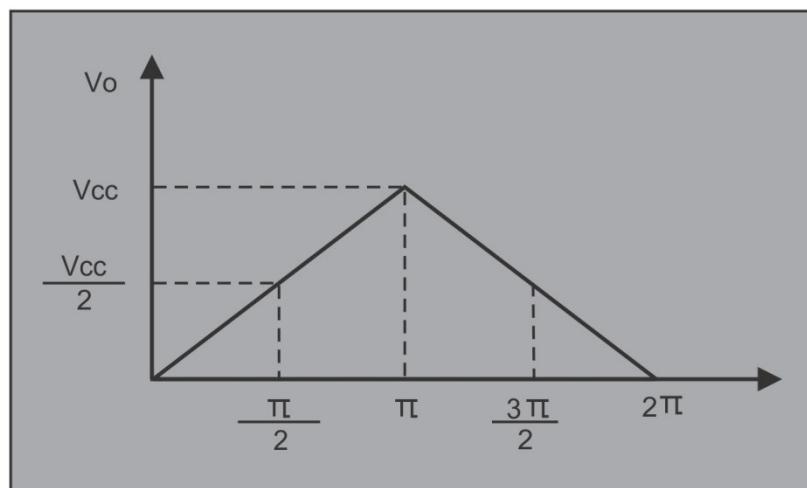


Fig 6.21 Variation of dc output voltage with phase difference

Fig 6.21 illustrates the variation of dc output voltage with the phase difference ϕ . It can be seen clearly that when the phase difference is 180° , the dc output voltage of the phase detector is maximum, the reason being the output of the gate remains high throughout. Note that the output dc voltage depends on the input's duty cycle. This makes it more convenient to use digital phase detectors when the waveforms of the input signal and the output signal are square waves with 50% duty cycle.

Analog Phase Detector

The simplest analog phase detector is an electronic switch controlled by the VCO output. This is shown in Fig 6.22. The electronic switch is opened and closed by the VCO output, which is normally a square wave. At a rate determined by the VCO frequency, the input signal is chopped off.

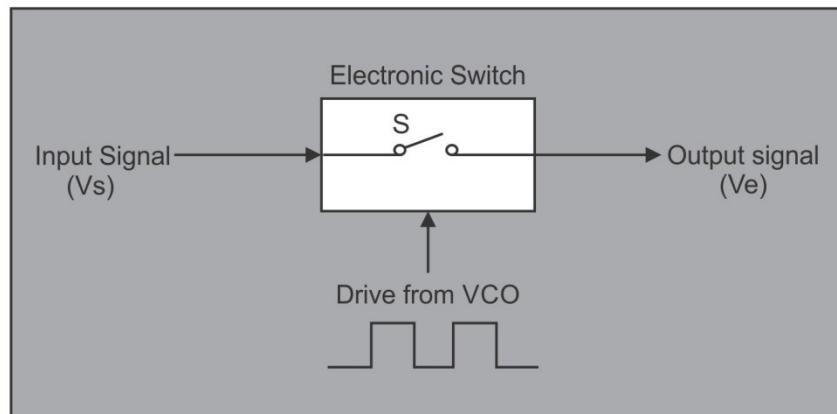


Fig 6.22 Analog Phase Detector

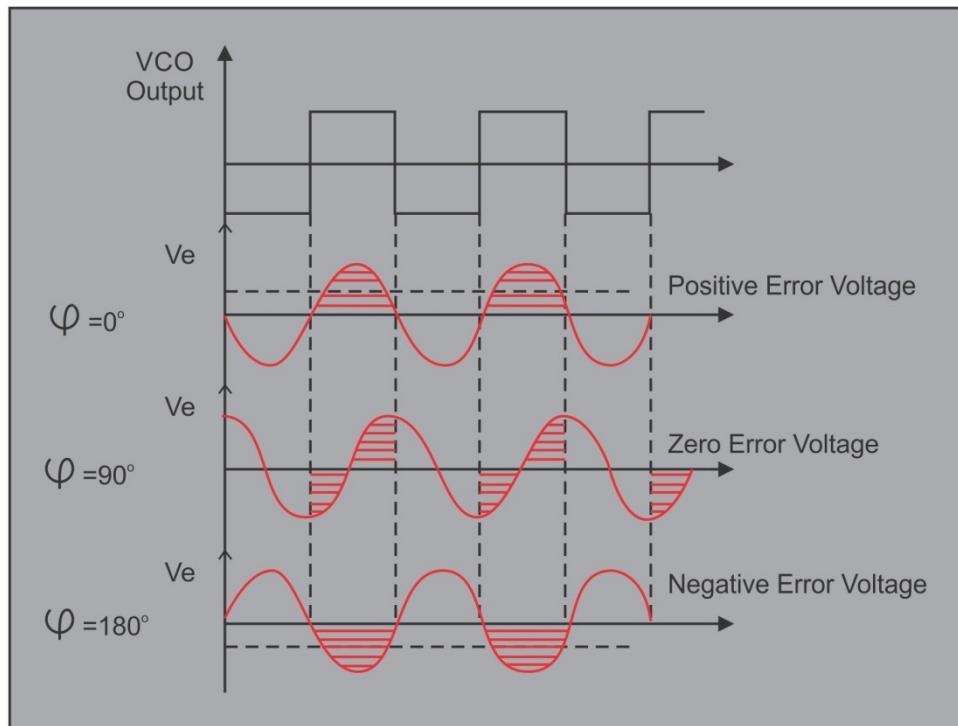


Fig 6.23 Analog Phase Detector Response

Fig 6.23 gives the response of an analog phase detector. The input signal is assumed to be in phase with the VCO output. Observe that the output waveform of the analog phase detector is always half sinusoids. These phase detectors are also referred to as half wave detectors as the phase information of only one half of the input waveform is detected and subsequently averaged out. The phase comparator's output is then low pass filtered, basically yielding the error signal which is the average value of the output, denoted by the dotted line. In case of digital phase detector, we claimed that if the phase difference is 180° , then the output dc voltage is maximum. However in the case of analog phase detector, we see that the error voltage is the average value of the output waveform, as shown in dotted lines in Fig 6.23

The main feature of analog PLL is that the error voltage is zero when the phase shift is between the two signals is 90° . Thus to achieve perfect locked condition, the VCO output should be 90° out of phase, with respect to the input signal.

Type II phase detectors use sequential logic machine that compares the delay between edges of the input with that of the VCO output. When the input signal leads in phase, the output signal will consist of positive pulses and the width of the pulses will be equal to the difference. When the input signal lags, the pulses are negative. These pulses are then integrated using the loop filter, the average value of which will then control the VCO.

The difference between Type I and Type II detectors is that while in Type I detector, the phases will be brought to a fixed difference, a Type II detector brings the phase into coincidence.

Having discussed the working and description of PLL, we turn our attention to some of the terms associated with PLL. First, we look at the three different states in which a PLL operates. The three states are free running state, capture state and locked state. These three states are defined as follows:

- **Free running state:** The PLL is said to be in free running state when there is no input applied to it. This implies that in free running state, the outputs of the phase detector and the low pass filter are zero. The voltage controlled oscillator operates at its natural or free running frequency, f_{osc} , as determined by the components of VCO.
- **Capture state:** The PLL enters capture state when an input frequency is applied to it. Upon applying the input frequency, the VCO frequency begins to change continuously till it equals the input.
- **Locked State:** Once the VCO frequency equals the input frequency, the PLL is said to be in phase locked mode. In this state, the phase error between the input signal and the VCO's output signal is zero or constant. In case the phase error increases, a control mechanism acts on the VCO in such a way to reduce the phase error and subsequently minimize the same.

A system in which the phase of the output signal is locked to the phase of the input signal or the reference signal is called a **phase locked loop**.

PLLs are associated with two frequency ranges, as illustrated in Fig 6.24; namely the lock range and the capture range.

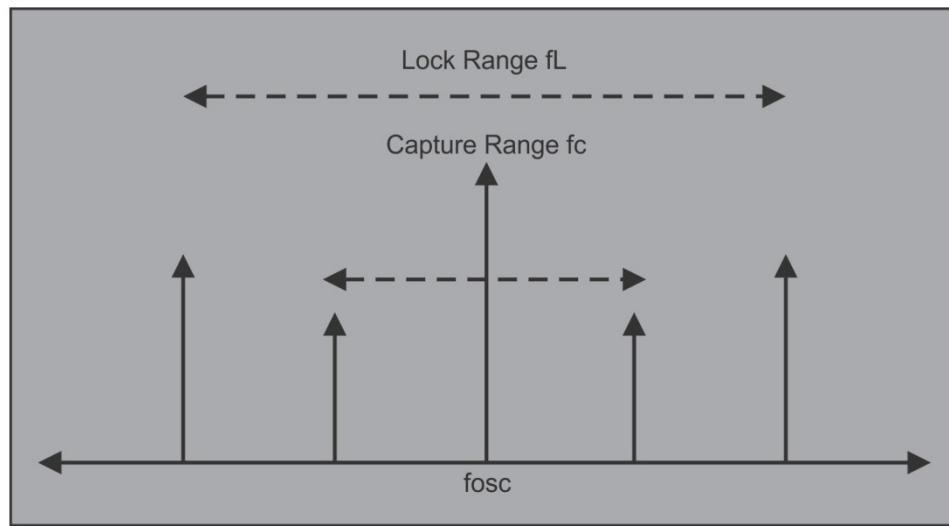


Fig 6.24 PLL Spectrum

- **Lock Range (f_L):** The range of frequencies over which the PLL tracks the input frequency and remains locked is called as lock range. It is the range above and below the PLL free running frequency.
- **Capture Range (f_c):** The frequency range in which the loop acquires the phase lock is called capture range.

The process of capture is typically the transient state in which the VCO control voltage is trying to acquire a value in order to make stable phase relations. Locking will happen only if the control range of the VCO includes the input frequency. If the control range is proper, then employing Type II detector would eventually lead to lock. This may not be the case with Type I detector, especially when the signal and VCO free-running frequencies are far apart. The reason is that the filtered output of the detector will not be sufficient enough to raise the VCO control voltage to the required amount and therefore there will not be any capture at all. Once the loop is locked, it will follow the whole range of the VCO. Typically, the capture range can never be greater than the lock range.

6.8.2 Transfer Characteristics of PLL

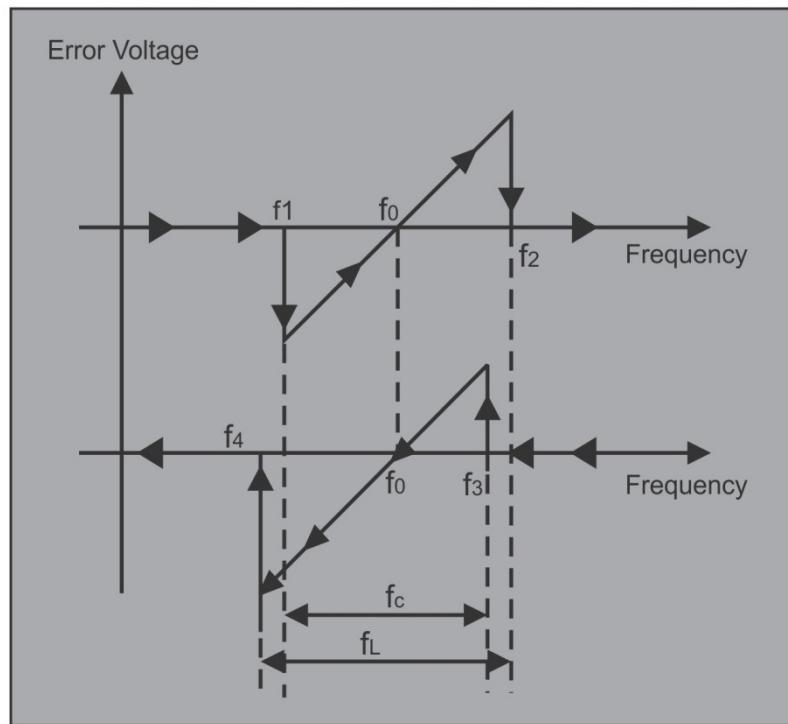


Fig 6.25 Transfer characteristics of PLL

Fig 6.25 illustrates the transfer characteristics of a PLL. Initially, the signal frequency is gradually increased, as illustrated in the upper portion of fig.26. Note that the PLL is not locked because the signal frequency and the VCO frequency are the same. At some frequency f_1 , the lower edge of the capture range, the PLL is locked. After f_1 , the PLL remains locked. At f_1 , a sudden negative jump of error voltage is observed, which shifts the VCO frequency f_0 . Increasing the signal frequency further keeps the loop in locked condition. At frequency f_2 , the upper edge of the lock range, the PLL comes out of locked condition. Beyond f_2 , the error voltage drops to zero, thus making the VCO operate at its free running frequency. We now look at the lower portion of the fig.26. This corresponds to the input frequency gradually decreased. As the frequency is decreased, the loop is captured at frequency f_3 , the upper edge of capture range and removed at the upper edge frequency of lock range, f_4 . From the Fig 6.25, we see that the frequency range between f_3 and f_1 is called the capture range and the range of frequencies between f_4 and f_2 is called the lock range.

6.8.3 CD4046B Monolithic PLL

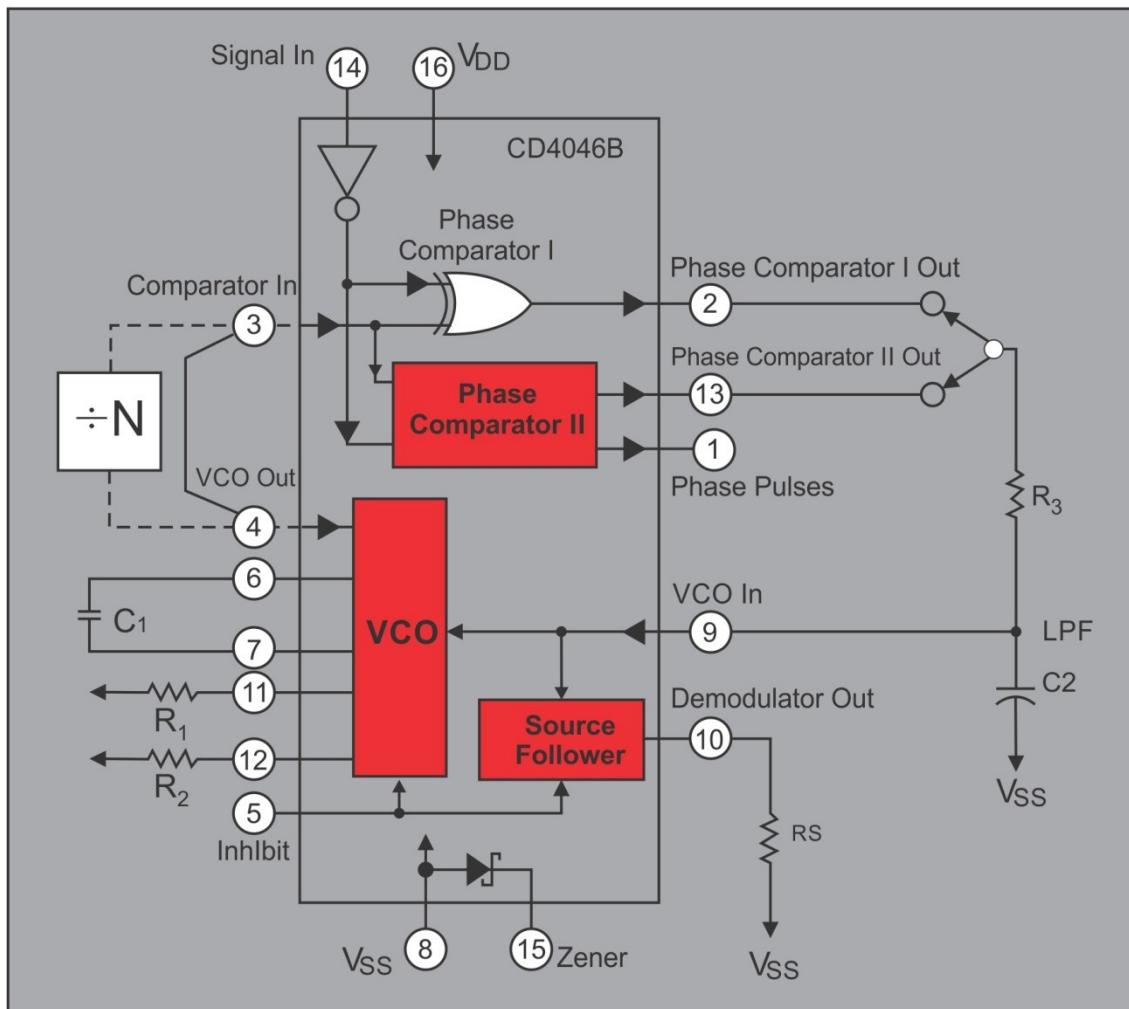


Fig 6.26 CD4046B Monolithic PLL

In this section, we look at a monolithic IC which contains all the parts necessary to make a PLL. We focus on CD4046B from Texas Instruments, which is widely used in applications such as FSK demodulation, frequency multiplication, frequency synthesis and many more. NE565 is another commonly used monolithic bipolar PLL.

The monolithic form low-power-consumption CD4046B is particularly desirable for use in portable battery-powered equipments. It typically consumes $600\mu\text{W}$ of power at 10kHz , which is 160 times lesser than that required by similar monolithic bipolar PLLs. CD4046B is available as 16-lead ceramic dual-in-line packages, 16-lead dual-in-line plastic packages, 16-lead small outline packages and in chip form.

Fig 6.26 shows the block diagram of monolithic IC CD4046B. The block diagram shows that CD4046B consists of a linear VCO, two different phase comparators having a common signal-input amplifier and a common comparator input. The zener diode gives voltage supply regulation, if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low pass filter is implemented externally to facilitate configuration changes from application to application.

Phase Comparators:

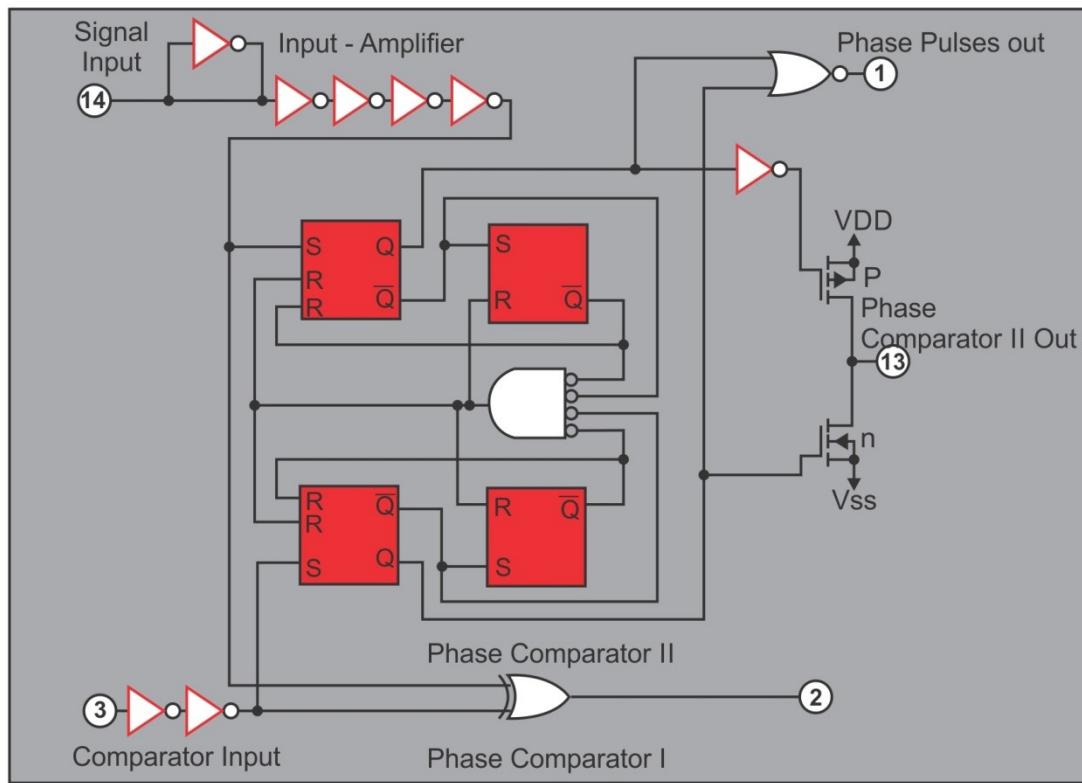


Fig 6.27 CD4046B Phase Comparator

The CD4046B design employs digital comparators, as illustrated in Fig 6.27 driven by common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. With signal swing well within CMOS logic levels, the phase comparator signal input, at terminal 14, can be directly coupled. For smaller input signal swings, the signal must be capacitive coupled to the self-biasing amplifier at the signal input to ensure an overdriven digital signal into the phase comparators.

Phase comparator I is an exclusive-OR network. As mentioned earlier, to maximize the lock range, the signal - and comparator - input frequencies must have a 50% duty cycle. When there is no signal input or only noise as input signal, this phase comparator has an average output voltage of $V_{DD}/2$. The low pass filter, at the output of phase comparator I provides the averaged voltage to the VCO input, making the VCO oscillate at f_0 , the center frequency of the oscillator. The LPF characteristics determine the capture range of PLL and thus the capture range can be made as large as the lock range. Phase comparator I enables a PLL system to remain in lock despite high amounts of noise in the signal input.

Phase comparator II is a type II phase detector that employs edge-controlled digital memory network. It consists of four flip-flops, control gating and 3-state output circuit comprising p- and n- drivers having a common output node, as can be seen in fig. 24. The p-MOS and n-MOS drivers, when ON, pull the output signal to either VDD or down to VSS respectively.

If the input signal frequency is higher than the comparator input frequency, the p-MOS output driver is maintained ON continuously.

If the input signal frequency is lower than the comparator input frequency, the n-MOS output driver is maintained ON continuously.

If the two frequencies are same, but the input signal lags the comparator input in phase, then n-MOS output driver is maintained ON for a time corresponding to the phase difference.

If the two frequencies are same, but the input signal leads the comparator input in phase, then p-MOS output driver is maintained ON for a time corresponding to the phase difference.

Subsequently, the capacitor voltage of the low pass filter is adjusted till the two signals are equal in both phase and frequency. It may be recalled that type II phase detectors have the same frequency and have no phase difference. At this operating point both p-MOS and n-MOS drivers are OFF. The phase comparator output becomes open circuit and holds the voltage on capacitor of the LPF constant.

The PLL lock range for this type of phase comparator is equal to the capture range, irrespective of the low pass filter.

Voltage Controlled Oscillator

Fig 6.28 gives the details of the VCO employed in CD4046B PLL. Observe that the VCO input uses n-MOS, which has practically infinite input resistance, thereby allowing more freedom in selecting the low pass filter components. This also prevents the VCO input from loading the filter or modifying the characteristics of the filter.

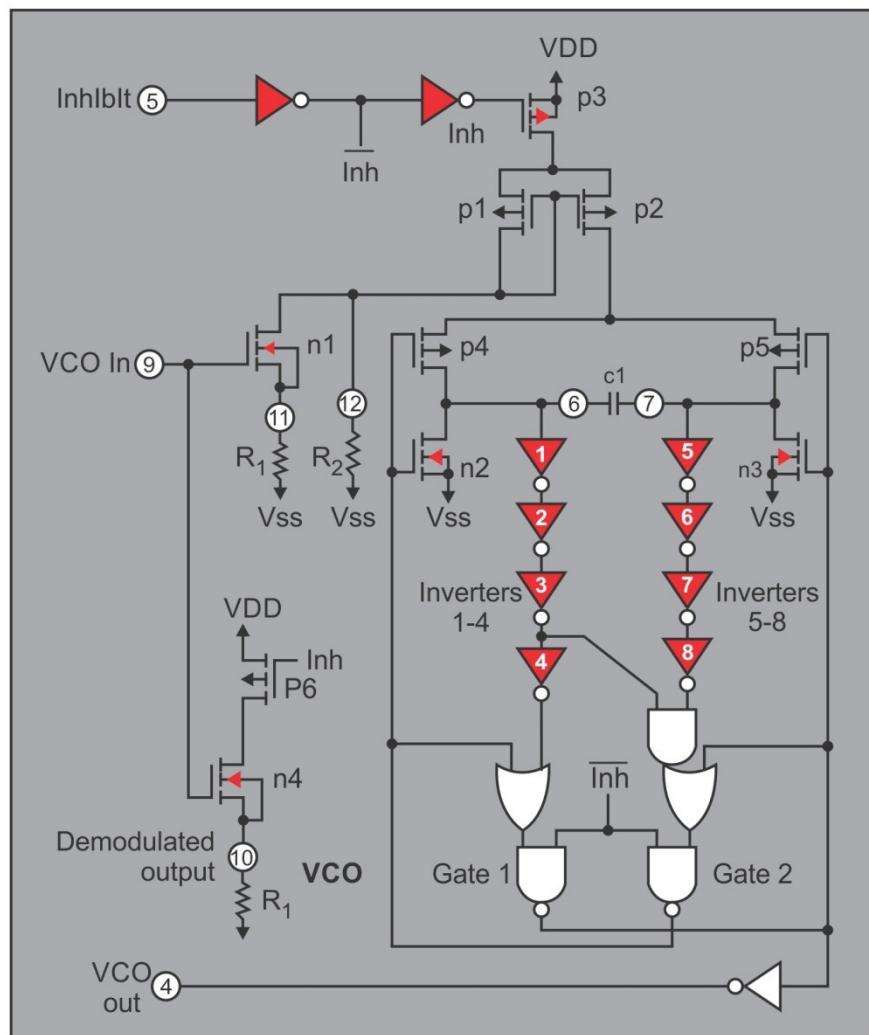


Fig 6.28 CD4046B Voltage Controlled Oscillator

The VCO operates as follows: when the inhibit input is low, p3 is turned full on, effectively connecting the sources of p1 and p2 to VDD, and gates 1 and 2 are permitted to function as NOR-gate flip-flops. n1 and external resistor R1 form a source-follower configuration. As long as the resistance of R1 is at least an order of magnitude greater than the on resistance of n1 (greater than 10 kΩ), current through R1 is linearly dependent on the VCO input voltage. This current flows through p1, which, together with p2, forms a current-mirror network. External resistor R2 adds an additional constant current through p1; this current offsets the VCO operating frequency for VCO input signals of 0 volts.

In the current-mirror network, the current of p2 is effectively equal to the current through p1, independent of the drain voltage at p2. (This condition is true, provided p2 is maintained in saturation. In the circuit in fig.26, p2 is saturated under all possible operating conditions and modes.) The set/reset flip-flop composed of gates 1 and 2 turns on either p4 and n3 or p5 and n2. One side of external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by p2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The charged side of the capacitor now is pulled to ground.

The other side of the capacitor goes negative and discharges rapidly through the drain diode of the off n device. Subsequently, a new half cycle starts. Because inverters 1 and 5 have the same transfer points, the VCO has a 50% duty cycle.

- Shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage.
- Maintain low power dissipation through the use of high impedance devices at inverters 1 and 5 (slow-input waveforms)
- Provide four inverter delays before removal of the set/reset flip-flop triggering pulse to ensure proper switching action.

In order not to load the LPF, a source-follower output of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (RS) of 10 kΩ, or more, should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off the VCO and source follower to minimize standby power consumption.

6.8.4 Frequency Shift Keying - Modulation and Demodulation

Frequency shift keying (FSK) is the most common digital modulation technique in the high-frequency radio spectrum and has applications in telephone circuits. The binary states are represented by analog waveforms of two different frequencies. While logic 0 is represented by a signal of low frequency, logic 1 is represented using a signal of higher frequency. FSK is a modulation scheme used to send and receive digital information between digital equipments. Data transmission is carried out by shifting the frequency of a continuous carrier in a binary manner to one or the other of two discrete frequencies. The high frequency corresponding to logic 1 is called MARK frequency, while the low frequency corresponding to logic 0 is called the SPACE frequency. Fig.30 shows the relation between data and transmitted signal. The binary data frequency modulates the carrier signal to produce the FSK signal whose frequency characteristic is as illustrated in Fig 6.30

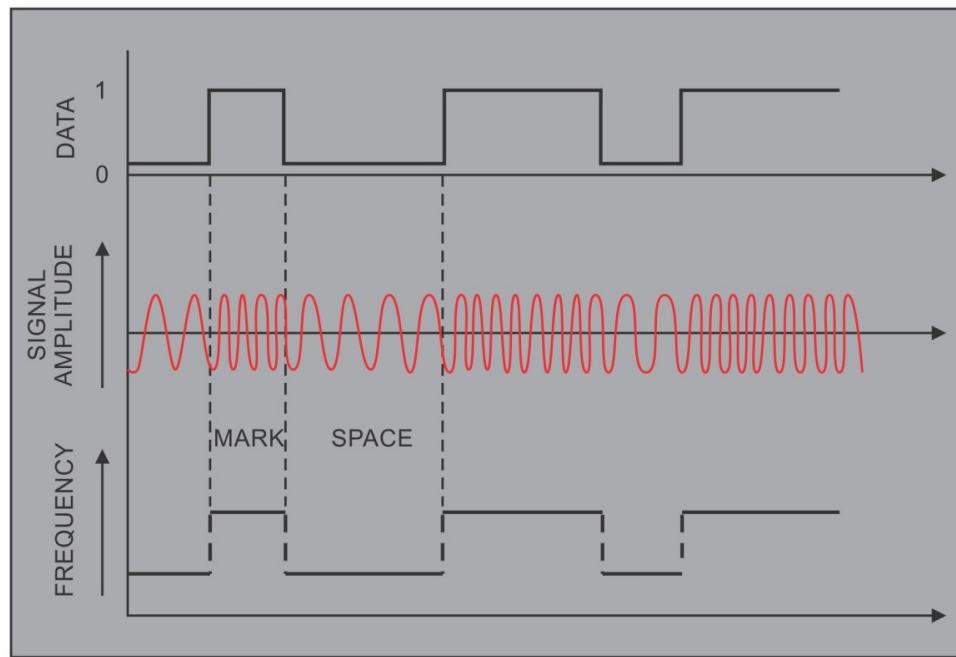


Fig 6.29 FSK Modulation

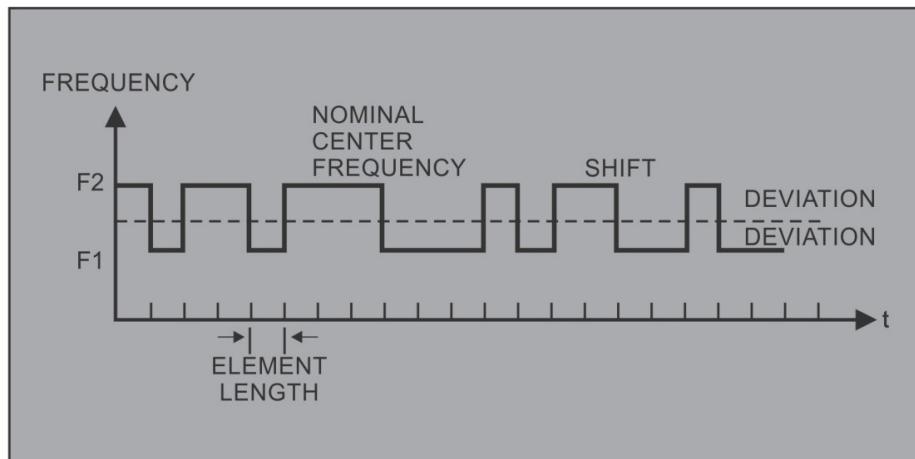


Fig 6.30 FSK Parameters

Fig 6.30 illustrates the various parameters associated with an FSK signal.

The minimum duration of a mark or space condition is called the *element length*. Typical values for element length are between 5 and 22 milliseconds. The alternate way of specifying element length is in terms of the keying speed. The keying speed in bauds is equal to the inverse of the element length in seconds.

Frequency measures of the FSK signal are stated in terms of shift and center frequency. The shift is the frequency difference between the mark and space frequencies. The nominal center frequency is the average of mark and space frequencies. The other term occasionally associated with FM is deviation, which is defined as the absolute value of the difference between the center frequency and mark or space frequency. The deviation is also equal to half of the shift.

6.8.5 IMPLEMENTATION OF FSK Modulation and Demodulation using PLL

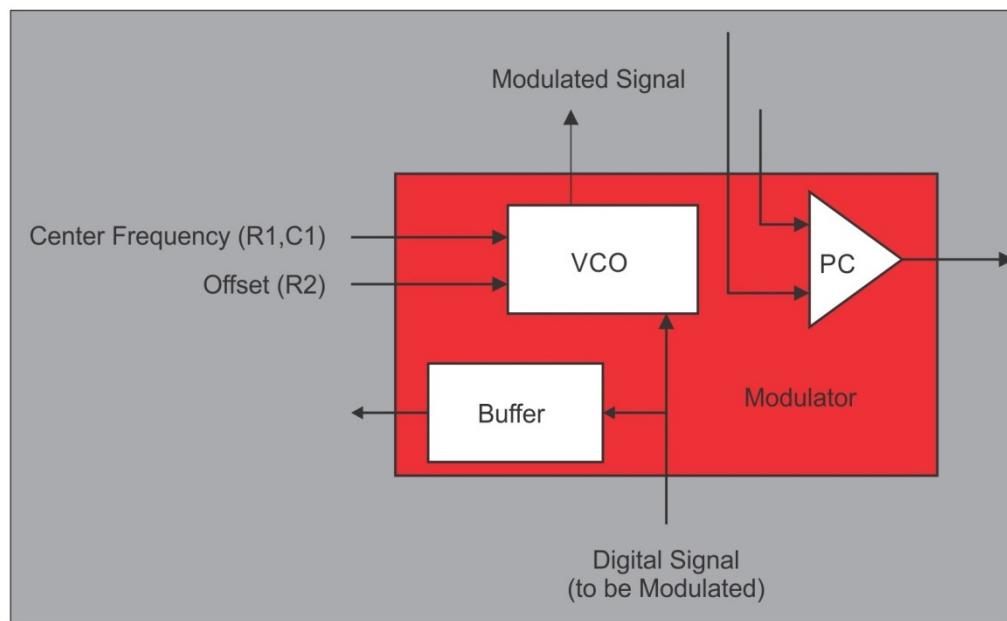


Fig 6.31 PLL as FSK modulator

The circuit in Fig 6.31 illustrates the application of PLL for FSK Modulation. The modulator uses only VCO for FSK modulation. $R1$ and $C1$ determine the frequency range of the VCO and center frequency of operation depends upon VCO input, which is a digital input signal level for a modulator. Hence, high and low voltage levels of the digital input determine actual output frequencies and separation between them. An optional low pass filter is included to minimize noise at VCO input pin. However, the 3-dB cutoff frequency of this filter should be 10 times or higher than the maximum bit rate of the modulating signal.

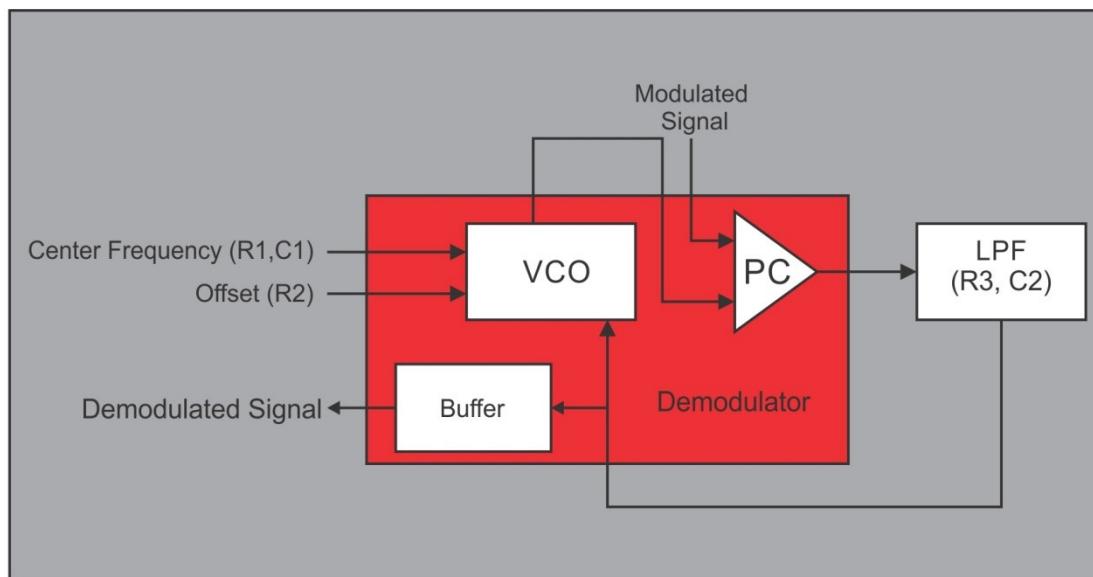


Fig 6.32 PLL as FSK demodulator

In a practical circuit, frequency separation depends on the bandwidth availability of the transmission media. Hence, by choosing an appropriate offset frequency and voltage levels of the VCO/N signal, expected modulation can be achieved.

The FSK demodulator, shown in Fig 6.32, operates in closed-loop mode with phase comparator and an external loop filter. The same value of $R1$, $C1$, as used in modulator should be used in demodulator circuit. While using the phase comparator I, the capture range depends on the low pass filter ($R3$, $C2$) characteristics and can be made as large as the lock range. For the phase comparator II, recollect that capture range is equal to lock range and is independent of the low pass filter.

The phase comparator produces an output proportional to the phase difference between the input FSK signal and the VCO output frequency. The output is then passed on through a low pass filter, producing an average error voltage which is applied to the VCO. This error voltage produces a change in the VCO frequency making it move closer to the FSK input frequency. Once the input frequency and the VCO frequency are equal, the PLL is locked to the input frequency and the error voltage indicates the data level.

6.9 Automatic Gain Controller (AGC)/Automatic Volume Control (AVC) using op-AMP and analog multipliers:

Automatic Gain Controller (AGC) is a type of AC voltage regulator. It is popularly called automatic volume control system (AVC) or in another application, it is also termed as amplitude stabilization of oscillators.

In a gain control system, the output remains constant. So we need an AC stabilization scheme. Hence before seeing the working of AGC, what comes into picture is the multiplier. Multiplier is nothing but an amplifier whose gain can be controlled. A multiplier is the ideal block into which this control system can be incorporated. If V_i is applied as input sinusoidal signal and V_c is the control voltage and we are asked to maintain the output constant, then output of the multiplier will be multiplication of both sine wave and control signal. As the output must remain constant, if V_{pi} decreases, V_c should increase so that V_{pi} into V_c remains a constant and output is $V_{pi} \cdot \sin \omega t$ into V_c by $10(V_R)$.

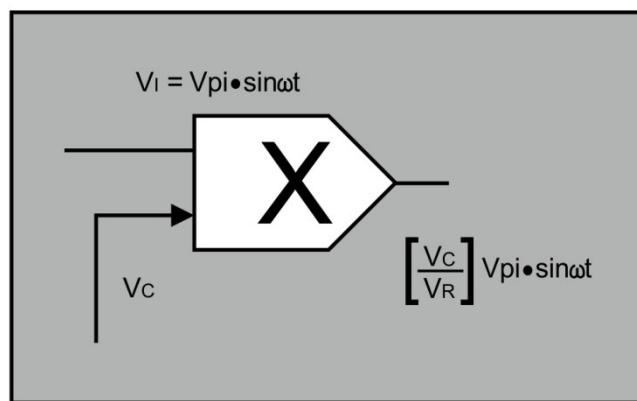


Fig 6.33 Analog Multiplier

This is the automatic gain control scheme or automatic volume control scheme. What it needs is an amplifier whose gain is controlled by means of a voltage or current; and these amplifiers should be working at a single frequency or a narrow band frequency.

Texas Instruments MPY634 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy. An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.

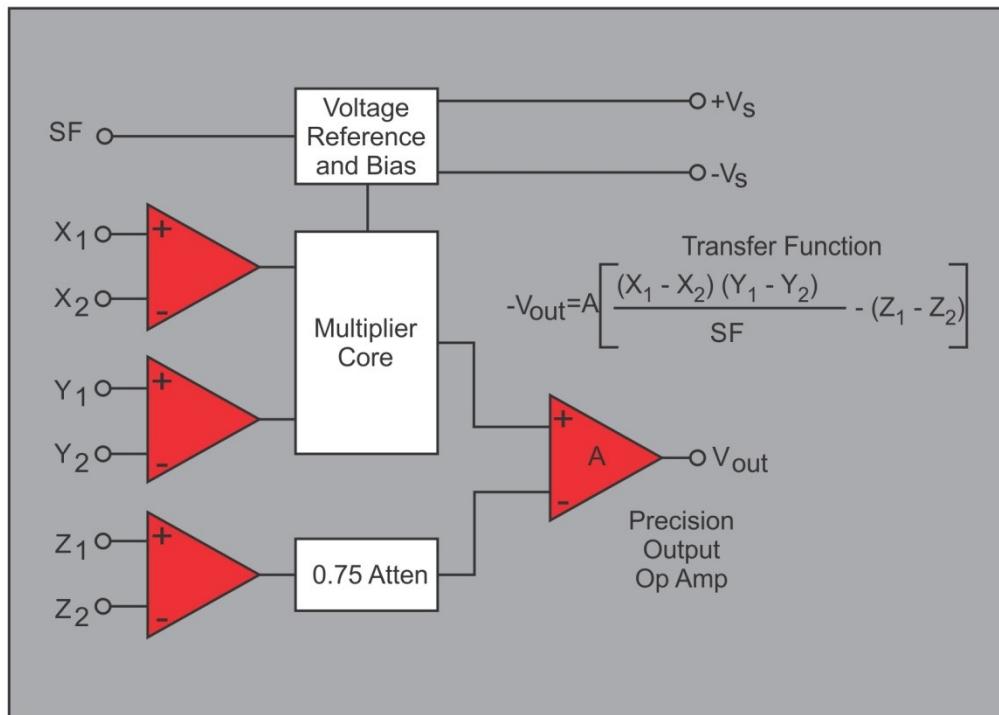


Fig 6.34 MPY634 Analog Multiplier

AGC, AVC are all applied to receivers. For example, we use a microphone in an environment where the level of the audio source is unknown. The Automatic Gain Control (AGC) circuit addresses this situation by compensation for significant variations in level from a microphone's input. It maintains a fixed level during recording or playback. The following scenarios showcase the real world benefits of the AGC circuit:

Scenario 1: An user talks too loudly or too close to the microphone. This causes a clipped voice signal at the output of the microphone preamplifier.

Without AGC: The user at the receiving end hears a clipped signal. This clipped signal sounds distorted. Further, it may damage the receiving-end transducer or may cause hearing loss.

With AGC: The AGC automatically lowers the microphone preamplifier gain. This prevents voice signal clipping. The resulting undistorted, unclipped voice signal is then presented to the user on the receiving end.

Scenario 2: A user talks too softly or too far away from the microphone.

Without AGC: The resultant low-level voice signal may not be heard clearly or at all by the user at the receiving end.

With AGC: The AGC will automatically increase the gain of the microphone preamplifier to a level that is heard clearly by the user at the receiving end. As shown in the scenarios above, the AGC operates by automatically adjusting the gain of the microphone preamplifier to maintain a pre-defined target level at the amplifier's output. The AGC loop is shown in Figure.

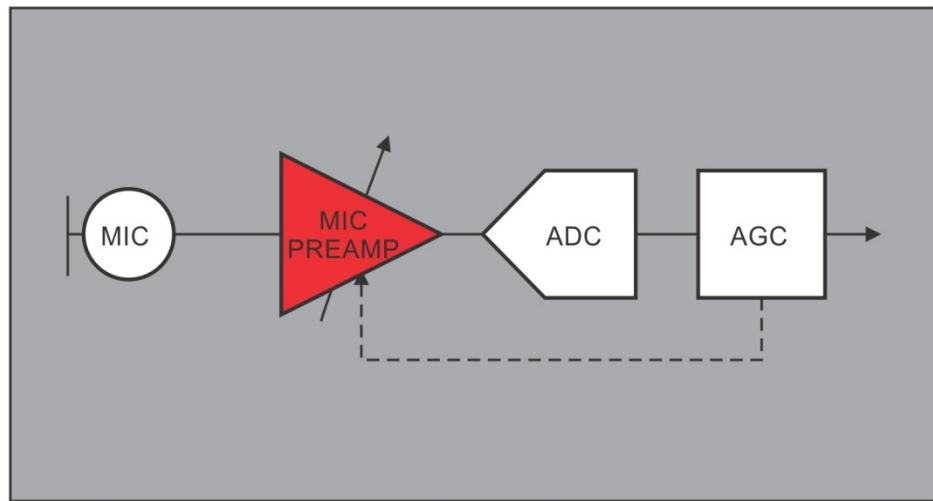


Fig 6.35 AGC LOOP

AGC system involves basically an amplifier with gain control, filter and voltage reference. In the signal chain of an electronic system, the output of the sensor can vary depending on the strength of the input. To adapt to wide variations in the magnitude of the input, we can design an amplifier whose gain can be adjusted dynamically. This is possible when the input signal has a narrow bandwidth and the control system is called Automatic Gain Control or AGC. Since we may wish to maintain the output voltage of the amplifier at a constant level, we also use the term Automatic Volume Control (AVC). Figure shows an AGC circuit. The typical I/O characteristics of AGC/AVC circuit are shown in Fig. As shown in Figure, the output value of the system remains constant at $\sqrt{2V_R V_{ref}}$ beyond input voltage $V_{pi} = \sqrt{2V_R V_{ref}}$

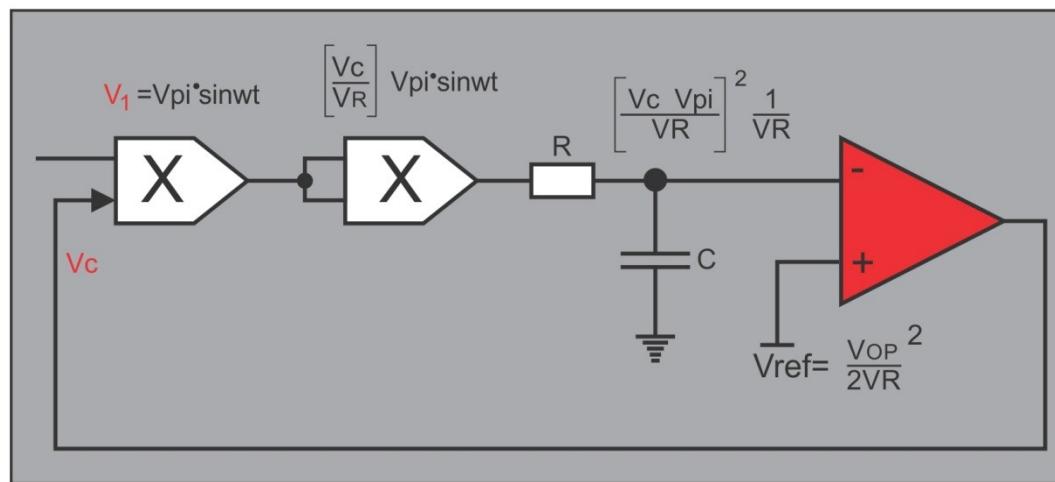


Fig 6.36 Automatic Gain Control (AGC)/Automatic Volume Control (AVC)

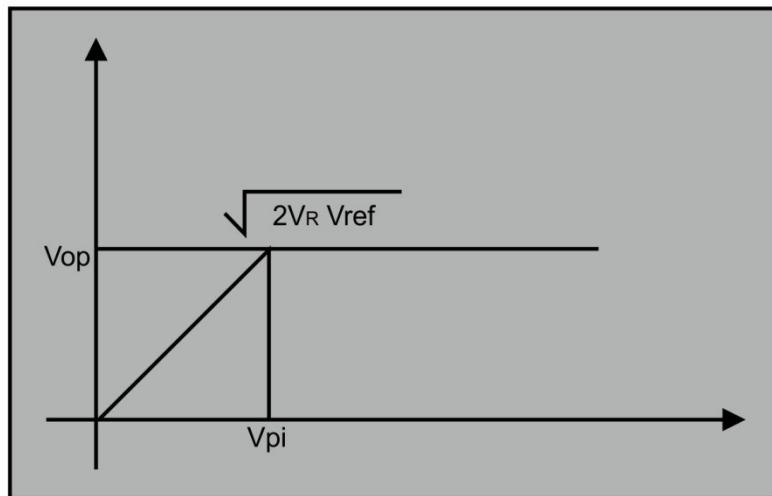


Fig 6.37 Input-Output Characteristics of AGC/AVC

6.10 Amplitude modulation using analog multiplier

For signal processing applications, a multiplier can be used. In this section, we represent an example to illustrate the use of a multiplier to make an amplitude modulator. Amplitude modulation is a technique which uses a low-frequency signal to control the amplitude of a high frequency signal.

One input is the high-frequency or carrier signal, and the other input is the modulating signal. A typical broadcast AM signal includes the carrier as well as the sidebands in the transmission.

To get such a double sideband transmitted carrier signal (DSB-TC) we must bias or offset the modulating signal by a value equal to the carrier's peak voltage.

The MPY634 is a wide bandwidth, high accuracy, four quadrants analog multiplier. The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies.

The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

The figure shows how MPY634 can be used in amplitude modulation application. The connection for AM modulator is shown in figure. Y1 and Z2 must be connected together and that connection is where the carrier is applied.

The low frequency modulating signal is applied to the X1 input. By injecting the input carrier signal into the output through connection to the Z2 input, conventional amplitude modulation is achieved. Amplification can be achieved by use of the SF pin, or Z attenuator (at the expense of bandwidth)

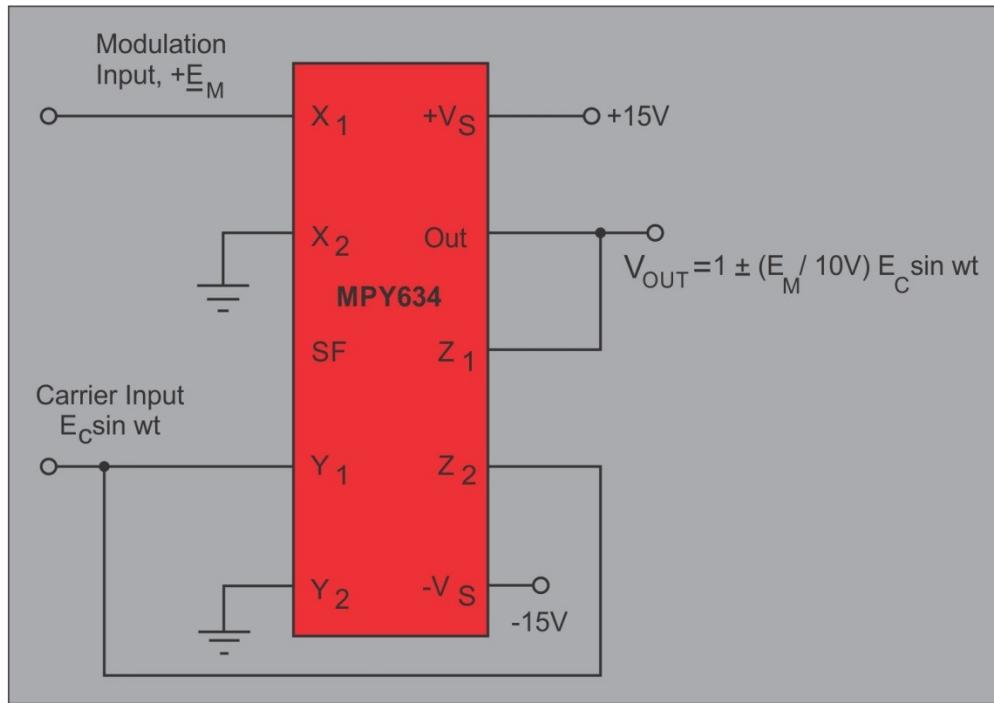


Fig 6.38 MPY634 Amplitude modulation setup

6.11 Summary:

- A voltage regulator is designed to automatically maintain a constant voltage level. An ideal voltage regulator provides a constant output voltage irrespective of variations in input (line) voltage or load current demand.
- Voltage regulators are categorized as linear regulators and switching regulators. Linear regulators are further classified as series regulator and shunt regulators.
- Switching regulator circuit is known for its efficient power transfer to the load. A switching regulator passes voltage to the load in the form of pulses, which are then filtered, providing a smooth dc voltage.
- Linear regulators have very low efficiency, requires the use of bulky and expensive heatsinks. To overcome this, we employ switching regulators. These work by taking small chunks of energy from the input to the output.
- The four most commonly used switching regulators are Buck converter, Boost converter, Buck-Boost converter, Fly back converter
- Buck converter is a voltage step down, current step up converter, and Boost converter is a DC-to-DC power converter with an output voltage greater than its input voltage
- In Buck-Boost converter a switched mode power supply combines the principles of buck and boost converter in a single circuit.
- Flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation.
- Phase locked loops (PLL) are frequency control systems with feedback. The output of the PLL is such that its phase is related to that of the input signal. PLLs and a wide variety of applications including frequency modulation (FM), tracking filters, FM demodulators, frequency shift keying (FSK) decoders for demodulation of carrier frequencies, clock recovery circuits and so on.
- PLLs are associated with two frequency ranges, namely the lock range and the capture range.

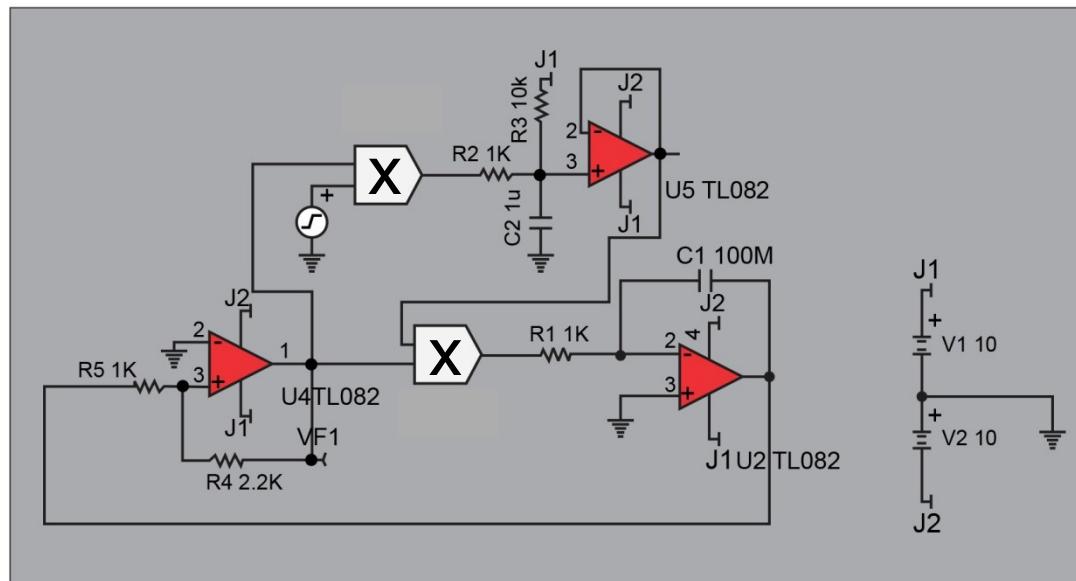
- Automatic Gain Controller (AGC) is a type of A C voltage regulator. It is popularly called automatic volume control system (AVC) or in another application, it is also termed as amplitude stabilization of oscillators. AGC system involves basically an amplifier with gain control, filter and voltage reference.

6.12 Review Questions

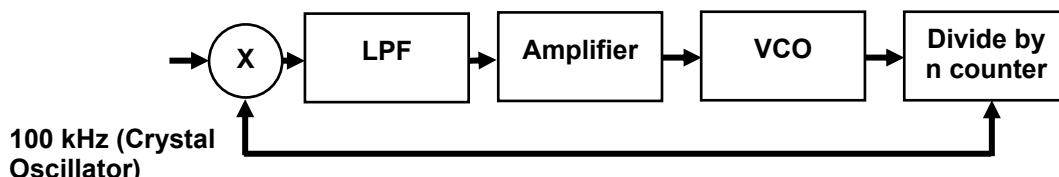
1. Explain the function of voltage regulators. List the different types of voltage regulator.
2. What are the advantages and disadvantages of switching voltage regulators in comparison with series voltage regulators?
3. With the help of the diagram explain the discrete components of series voltage regulator circuit and explain its operation.
4. Distinguish between a linearly regulated power supply and a switched mode power supply with reference to their principle of operation, advantages and disadvantages.
5. Briefly describe the procedure for designing the flyback DC to DC converter operating from a input voltage V_{in} and required to deliver output power of P_o to the load.
6. Give the reason for the following:
 - a. Why can the boost regulator not produce voltage less than the input voltage?
 - b. Why Flyback converter is not suitable for delivering high level of power to the load?
 - c. Why do we need to connect power converters in series or parallel?
7. With the help of basic configurations, briefly describe the operational principle of following switching regulators circuits:
 - a. Buck Regulator
 - b. Boost Regulator
 - c. Buck -Boost Regulator
8. Write a short note on standard switching regulator TPS40200 and TPS40210, explaining its characteristics, features and application field.
9. Explain the working of Phase Locked using block diagram. Also describe the different states in which PLL works.
10. Draw and explain the transfer characteristics of PLL.
11. How can we design Automatic Gain Controller using op-AMP and analog multipliers? Explain in detail.
12. How implementation of fsk modulation and demodulation can be done using pll.

6.13 Exercises

1. Determine the free running frequency of Phase Locked Loop, shown in Figure. Determine the lock ranges when the input is a square wave of amplitude 0.5 V.



2. Design a frequency synthesizer to generate a waveform of 1MHz frequency from a 100 kHz crystal as shown in Figure:



3. Design a DC-DC converter using a switching frequency of 10 kHz and 100 kHz using available reference voltage, for an output voltage of 5V.
4. How a PMOS switch can be used to achieve Class-D operations for the DC-DC converter system we studied. Show the block diagram. You may need diode in your system-Why?

Dr S Rajaram, BE, ME, PhD, Post Doc.

**About the author's educational qualifications**

Rajaram was born in Mamsapuram near Rajapalayam in the year 1973. He received a Bachelor's degree in Electronics and Communication Engineering in 1994 from the Thiagarajar College of Engineering, Madurai and a Master's degree with Distinction in Microwave and Optical Engineering from Alagappa Chettiar College of Engineering and Technology, Karaikudi in 1996. Dr S Rajaram holds a PhD degree in VLSI Design from Madurai Kamaraj University. He completed his Post Doctoral Research in 3D wireless system at Georgia Institute of Technology, Atlanta, USA during 2010-2011.

Current service details

Since 1998, he has been with Thiagarajar College of Engineering, Madurai. Currently he holds the post of Associate Professor in the department of Electronics and Communication Engineering, Thiagarajar College of Engineering.

Any extras such as specializations, papers published, programs conducted etc

He is a former Member of Academic Council of Thiagarajar College of Engineering and Member of Board of Studies for several educational Institutions. His fields of interest are VLSI Design and Wireless Communication. He is one among the Senior Resource persons in Thiagarajar College of Engineering for conducting faculty development programs. Under his guidance ten research scholars have already obtained PhD degrees in the area of Applications of VLSI Design for wireless Communication systems. He has published around 170 Papers in reputed Journal and Conferences. He was the recipient of Young Scientist Fellowship from TNSCST, BOYSCAST Fellowship from DST and Cambridge International certificate for Teachers and Trainers.

Other qualifications and ex-officio posts held

Dr. S Rajaram is also the principal investigator for several projects funded by AICTE, DST and DRDO. He has established several Research Centres at Thiagarajar College of Engineering such Altera VLSI Design Centre, ASIC Tools Laboratory and TIFAC Core in wireless Technologies in collaboration with Industries and Government Agencies.

He is a senior member of the Institute of Electrical and Electronics Engineers (IEEE, USA), Life member of Indian Society of Technical Education, and member of VLSI society of India. He has visited USA for Post doctoral research work and conferences.

Dr A Kandaswamy, BE (Hons), MSc (Engg), PhD**About the author's educational qualifications**

Arumugam Kandaswamy was born in Coimbatore in the year 1944. He received a Bachelor's degree with honors in Electrical Engineering in 1969 from the PSG College of Technology, and a Master's degree in Applied Electronics from Madras University, Chennai in 1974. Dr Kandaswamy holds a PhD degree in Electrical and Electronics Engineering from Bharathiar University, Coimbatore.

Current service details

Since 1969, he has been with PSG College of Technology, Coimbatore. He retired from service as Dean of Electrical Sciences and Prof. and Head of Electronics and Communication Engineering in 2005. He is now the Management's representative for ISO implementation.

Any extras such as specializations, papers published, programs conducted etc

He also heads the Department of Biomedical Engineering which offers a 4-year BE program (Biomedical Engineering). He is a former Senate Member of Bharathiar University and Member of Board of Studies for several educational Institutions. His fields of interest are Signal Processing and Image Processing Applications in Medicine. He is one among the Senior Resource persons in PSG College of Technology for conducting faculty development programs. Under his guidance fourteen research scholars have already obtained PhD degrees and eight more are doing research in the area of Applications of Image processing in Medicine.

Other qualifications and ex-officio posts held

Dr. Kandaswamy is also the principal investigator for several projects funded by UGC, DST and AICTE. He has established several Research Centres at PSG College of Technology such as Virtual Instrumentation, (National Instruments, USA), VLSI Design Centre (Govt. of India) and National MEMS Design Centre (Govt. of India) in collaboration with Industries and Government Agencies.

He is a member of the Institute of Electrical and Electronics Engineers (USA), Fellow of Institution of Engineers (India), and Life member of Biomedical Engineering Society of India, Indian Society of Technical Education, Computer Society of India, System Society of India and Life member of Advanced Computing and Communications Society. He has visited several countries such as USA, France, Germany, Switzerland, Malaysia and Singapore for conferences and to give special lectures.

M Alagappan M.Sc., M.Phil, M.Tech, (Ph.D)**About the Author's Educational Qualifications**

M Alagappan has completed his Master of Science in Applied Electronics and Master of Philosophy in Electronics from Bharathiar University, Coimbatore. He has also completed his Master of Technology in Nanotechnology and currently pursuing his Doctoral Research on Biosensors from Anna University, Chennai.

Current Service Details

He has been working as Assistant Professor (Selection Grade) in the Department of Electronics and Communication Engineering, PSG College of Technology, Coimbatore since August 2015. He has continued his services in the Department of Biomedical Engineering as Assistant Professor (Senior Grade) with the same institution from June 2009 to July 2015. Before turning to Lectureship position, he worked as Project Scientist in Product Development Centre at PSG College of Technology during August 2006 – May 2009. Further, he had served as Senior Lecturer in the Department of Electronics, S.N.R. Sons College, Coimbatore between August 1998 and July 2006.

Any Extras such as Specializations, Papers Published, Programs Conducted etc

He has guided one M.Phil dissertation and several projects in the area of Electronics, MEMS and Nanotechnology to Under Graduate and Post Graduate students. He has been a consultant to few industries in India and testing their products to meet the industrial standards. He has published many papers in National and International Journals and Conferences. He has also acted as a resource person and delivered lots of technical lectures to the industries and academia in India. Further, he has conducted several training programmes to the industrial personnel and to the academicians that helped several individuals to perform better in industries and a few became successful entrepreneurs. He has shown his organizational skills by conducting an International / National Conferences, Several Faculty Development Programmes, Workshops, Seminars and Entrepreneurship Awareness Camps and provided opportunities to the experts to share their views on the new trends in his field.

Other Qualifications and Ex-officio Posts Held

He is the investigator of few projects funded by UGC. He has associated with several professional bodies such as the International Association of Computer Science and Information Technology (IACSIT), International Association of Engineers (IAENG), Institute of Smart Structures and Systems (ISSS), Biomedical Engineering Society of India (BESI) and Indian Red Cross Society (IRCS). He has also visited several Central Government Research Laboratories, Industries and Non-Government Organizations and interacted with Scientists and Several Industrialists. He utilized the knowledge gained from these endeavors to the benefit of students. He has associated himself with the societal activities by organizing several Blood Donation Camps, Youth Development Programmes including Health Awareness Programmes, First Aid training, Women Safety, etc. for the benefit of students and society. He has also received accolades for his prominent achievement in his field and his significant contribution for the betterment of contemporary society.

Dr. Arulalan Rajan, BE, ME, Ph.D.



About the author's educational qualifications

Dr. Arulalan Rajan holds a PhD from the Indian Institute of Science. He did his BE from University of Madras, following it up with ME in VLSI System from Regional Engineering College, Trichy. His research interests include Number Theory and Applications, Sequences Patterns and Processing, Signal Processing and Architectures.

Current service details

He is currently in the faculty of Dept. of Electronics and Communication Engineering at the National Institute of Technology Karnataka, Surathkal. He teaches courses on Linear Integrated Circuits, Digital Signal Processing Architectures, Cryptography and Linear Algebra and Applications.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), evaluation modules, and samples (<http://www.ti.com/sc/docs/samptersms.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated