In this report, I have selected the following processors as representatives of the 1960s, 1990s, and 2020s:

1. **Processor from the 1960s: IBM System/360 Model 91**

I have chosen IBM System/360 Model 91 as a typical processor from the 1960s because it was a pioneering mainframe computer introduced by IBM in 1966, which marked a significant milestone in the history of computing. It was one of the first processors to use microcode, a technique that allowed the processor's instruction set to be modified by software.

**Technical Design:**

**Year of release:** 1966

**Manufacturing technology:** Discrete transistors

**Clock frequency:** Fixed clock frequency of 10 MHz

**Overall architecture:** Single processor with a 32-bit word length and 64-bit double-word length

**Cache design**: No cache

**Number of operations per cycle**: Single scalar

Source:

<http://www.columbia.edu/cu/computinghistory/36091.html>

1. **Processor from the 1990s: Intel Pentium Pro**

I have chosen Intel Pentium Pro as a typical processor from the 1990s because it was a high-performance processor designed for servers and workstations, and it represented a major leap in processor architecture with its out-of-order execution and speculative execution capabilities.

**Technical Design:**

**Year of release**: 1995

**Manufacturing technology**: 0.6 µm CMOS process

**Clock frequency**: Variable clock frequency, ranging from 150 MHz to 200 MHz

**Overall architecture**: Single processor with dual instruction pipelines and out-of-order execution

**Cache design**: 8 KB instruction cache, 8 KB data cache, and a larger second-level cache with capacities of 256 KB to 1 MB

**Number of operations per cycle**: Superscalar with multiple instructions executed in parallel.

Source:

<https://ark.intel.com/content/www/us/en/ark/products/49951/intel-pentium-pro-processor-200-mhz-1m-cache-66-mhz-fsb.html>

<https://en.wikipedia.org/wiki/Pentium_Pro>

**Processor from the 2020s: Apple M1 chip**

I have selected the Apple M1 chip as a representative processor from the 2020s due to its significant historical significance as the first high-performance computer chip to utilize ARM architecture instead of the traditional x86 architecture typically found in CPUs. The Apple M1 chip not only marks a milestone in the adoption of ARM architecture beyond just smartphone SoCs, but also demonstrates the potential of ARM architecture in delivering high-performance computing, particularly in laptops. In comparison to x86 chips, the Apple M1 chip stands out for its higher energy efficiency, making it a noteworthy choice for representing the processor landscape of the 2020s.

**Technical Design:**

**Year of release:** 2020

**Manufacturing technology:** cutting-edge 5 nm process technology, should be CMOS.

**Clock frequency:** Different cores in different modes may have different variable clock frequencies. For the high-performance Firestorm cores, range is from 2.1 GHz to 3.2 GHz, while energy efficient Icestorm cores is from 0.6GHz to 2.05GHz.

**Overall architecture:** Apple M1 chips is a system-on-chip (SoC) design that integrates multiple components, including a high-performance CPU, a high-performance GPU, an image signal processor (ISP), a neural engine for machine learning task, and other specialized hardware accelerators. It is an 8-cores ARM-based architecture.

**Cache design:** The Apple M1 chip has a unified memory architecture with a shared memory pool for CPU, GPU, and other components. The four high-performance cores of 192KB of instruction cache, 128KB of data cache, and shared 12MB L2 cache. And also with four-efficiency cores with 128KB of instruction cache, 64KB of data cache, and shared 4MB L2 cache.

**Number of operations per cycle**: superscalar with multiple instructions per cycle, like 8 instructions per cycle to its high-performance Firestorm cores and 4 instructions per cycle to its energy efficient Icestorm cores.

Source:

<https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/>

<https://en.wikipedia.org/wiki/Apple_M1>

**Comparison and Evolution of Processor Technologies:**

Over the years, the manufacturing technology evolved from discrete transistor in 1960s to the 0.6 µm CMOS process at 1990s and then to the 5 nm process technology at 2020s. We can see the manufacturing technology is more advanced, keep the transistor be smaller and having a higher density of the transistor inside the chips.

While for the clock frequency, it has steadily increased, IBM 360 Mode 91 in 1960s having only a fixed clock frequency of 10MHz, to the Intel Pentium Pro in 1990s, having a variable clock frequency of 150MHz to 200MHz, and at 2020s, the Apple M1 chips having variable clock with 0.6-3.2GHz. This shows that in past 60 years, the clock frequency is keep rising and making it be variable. However, for the resent years, the power wall has limited the ability to increase clock frequency of a single core due to the excessive heat generated. Although extreme cooling methods like liquid nitrogen can push clock up to 8812.85 MHz, reference: ( <https://www.youtube.com/watch?v=2wKzvC--McM> ),the energy efficiency becomes extremely low. As a result, the modern processor is making use of multi-core instead. like the M1 chips is an 8-cores processor, and I think the core number of it will be keep increasing in the future.

While for the architecture, in the 1960s and 1990s the IBM and Intel processor, they are using system360/architecture and the x86 architecture, both are the CISC (Complex Instruction Set Computing) architecture. While for the Apple M1 chips, it instead using the RAM architecture, which is the RISC (Reduced Instruction Set Computing) architecture. Although RISC processor are not widely use in most of the laptop/desktop processor now, but it is very widely use in the mobile phone and the server as it’s higher efficiency of power. So, I think, for the future, the RISC architecture may become more popular.

For the cache design, we can see the tread is using more and more cache now. For the 1960s, it is no cache design, for the 1990s, it already using 8KB for L1 cache and using up to 1MB L2 cache, while for now, using a larger, unified cache. This is for bridge the speed gap between the processor and the main memory. I think in the future, we will still be using the cache to enhance the speed, and the cache should be larger, with more layers and more utilize of the unified cache for the content shared by different cores.

For the Number of operations per cycle, at 1960s, the IBM 360 using the single scalar, while the Pentium pro start using the superscalar in its single core to do the instructions parallel and at M1 chips, it do the superscalar in each of its core. As doing the multiple instructions on the same time, we are possible to make our processor having the CPI lower than 1 and make it as small as it can. I think for the future, the superscalar will be continued and making it utilize in multi-cores processor.