TN0054
Technical note

PwSSO packages, an effective solution for power dissipation and miniaturization

Introduction

This document provides information on the PwSSO, MO-271 JEDEC registered power IC surface mount package family.

Following the success of the PowerSO – MO-166 packages, and in reply to the increasing demand for effective power dissipation and miniaturization in power applications, STMicroelectronics has developed the PwSSO package family for the automotive, industrial and audio markets.

The PwSSO (PowerSSO) is derived from the well known SO16 wide body package.

The main packages of the family are:

- PwSSO24 - 24 leads at 0.8 mm pitch
- PwSSO36 - 36 leads at 0.5 mm pitch

Both packages have been in mass production since 2005.

This document provides mechanical, thermal, electrical and reliability data for these packages and also suggests guidelines for their assembly on printed circuit boards.

Figure 1. PowerSSO24 package

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1 Market demands - higher performance and smaller packages

The electronics industry is increasingly demanding higher performance and smaller size. This challenge must be addressed, not only for consumer applications, but also for professional markets such as automotive and telecom.

During the 90's, after the consolidation of surface mounting technology in the assembly of signal modules, STMicroelectronics introduced the PowerSO-20 and PowerSO-36 packages (MO166 JEDEC registered).

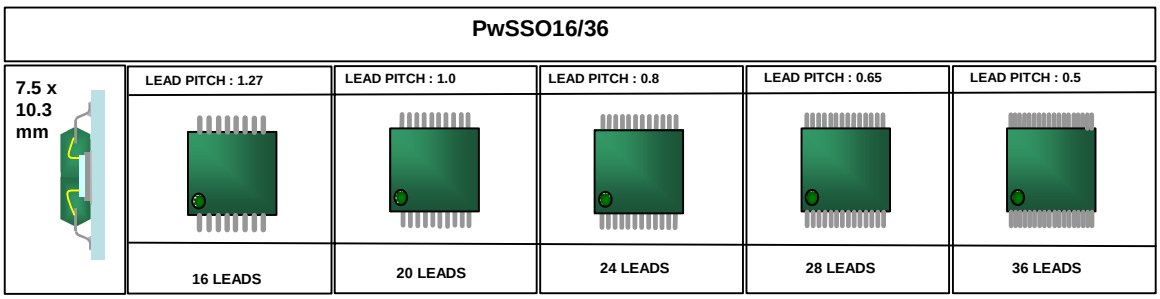
Today the PowerSO packages are still very successful but for some applications such as audio power amplifiers, printer linear drivers, power supply for desktop microprocessors, automotive body electronics and power train and safety systems, the market is demanding smaller package solutions.

To reply to this demand STMicroelectronics has developed the PwSSO (JEDEC MO-271) family of packages using the well established concept of "variable pitch in a fixed body" with 1.27 mm, 1.0 mm, 0.8 mm, 0.65 mm and 0.5 mm pitches (see *Figure 2*), with a range of 16 to 36 leads.

The PwSSO packages have the same body as the SO 16W (7.5 x 10.3 mm), but the key new feature is an exposed pad for enhanced thermal dissipation.

This document looks at the two main packages of the family, PwSSO24 and PwSSO36.

Figure 2. PwSSO family (JEDEC MO-271)



2 Mechanical data

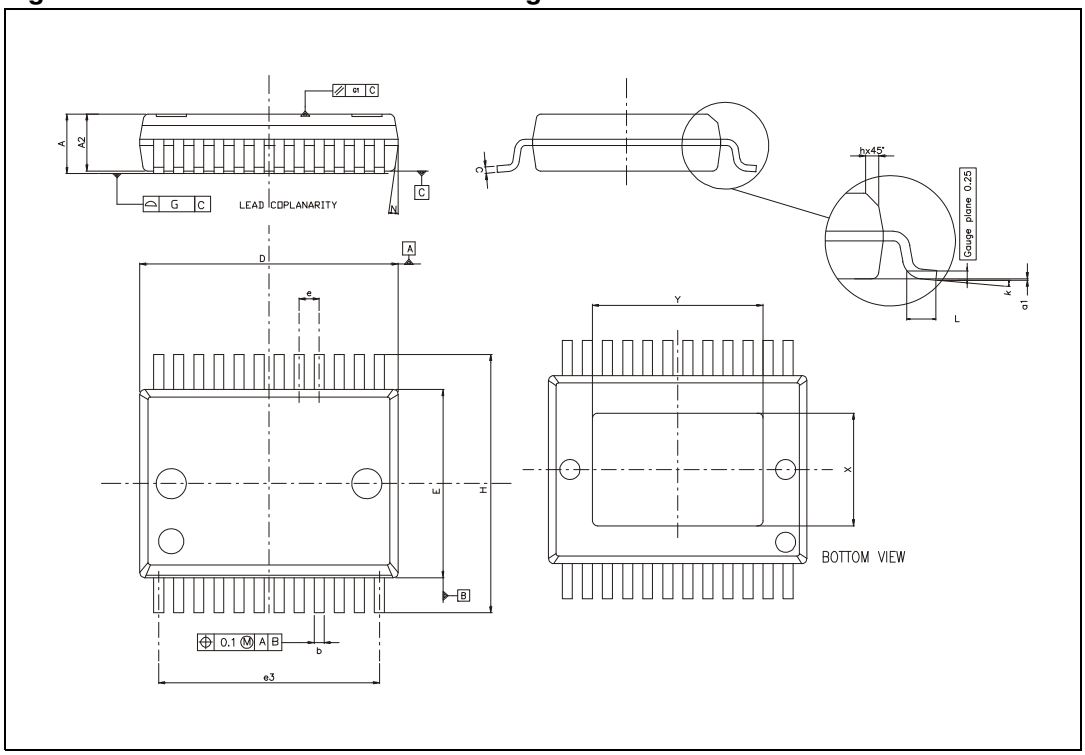
2.1 PwSSO24 mechanical data

Table 1. PwSSO24 mechanical data(1) (2)

Reference dimension	Data book mm		
	Typ	Min	Max
A	-	2.15	2.47
A2	-	2.15	2.40
a1	-	0	0.075
b	-	0.33	0.51
c	-	0.23	0.32
D(3)	-	10.10	10.50
E(3)	-	7.4	7.6
e	0.8	-	-
e3	8.8	-	-
G	-	-	0.1
G1	-	-	0.06
H	-	10.1	10.5
h	-	-	0.4
k	5 deg	-	-
L	-	0.55	0.85
N	-	-	10 deg
X	-	4.1	4.7
Y	-	6.5	7.1
Variation for small window leadframe option			
Y	-	4.9	5.5

1. No inward intrusion allowed on the leads
2. Flash or bleeds on exposed die pad must not exceed 0.5 mm per side
3. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions must not exceed 0.15 mm per side.

Figure 3. PwSSO24 mechanical drawing



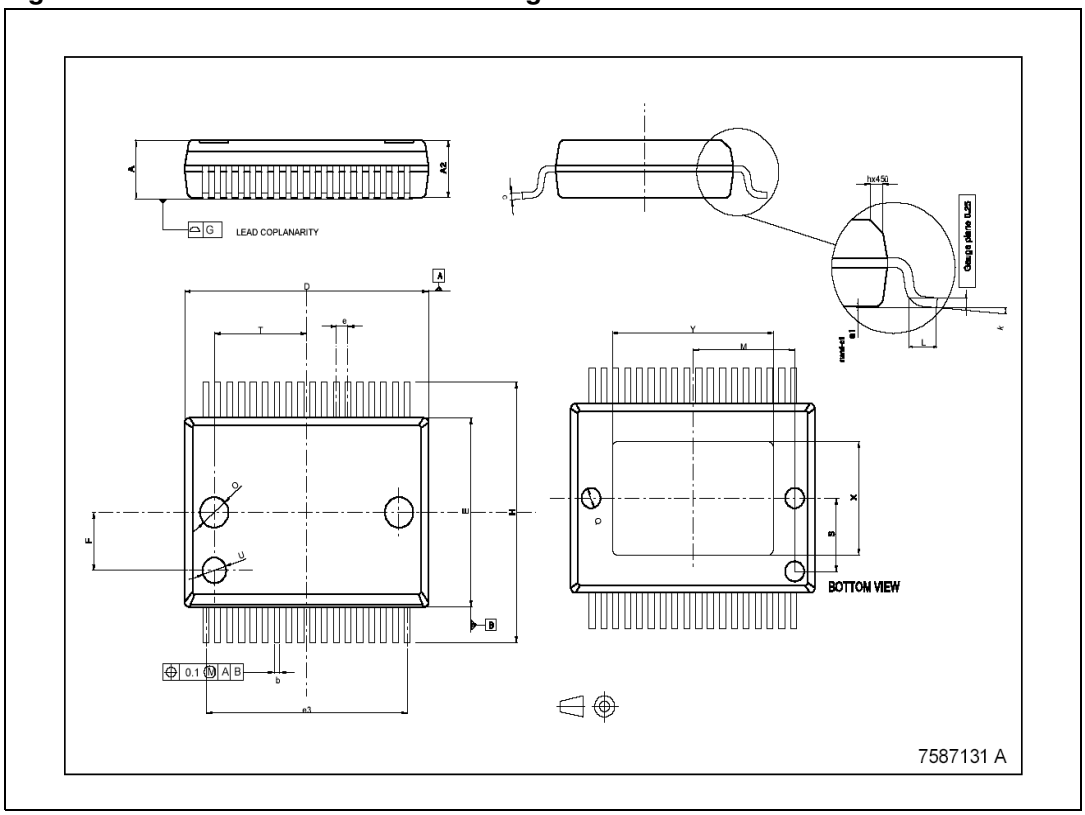
2.2 PwSSO36 mechanical data

Table 2. PwSSO36 mechanical data(1) (2)

Reference dimension		Data book mm		
		Typ	Min	Max
A		-	2.15	2.47
A2		-	2.15	2.40
a1		-	0	0.075
b		-	0.18	0.36
c		-	0.23	0.32
D(3)		-	10.10	10.50
E(3)		-	7.4	7.6
e		0.5	-	-
e3		8.5	-	-
F		2.3	-	-
G		-	-	0.075
G1		-	-	0.06
H		-	10.1	10.5
h		-	-	0.4
L		-	0.55	0.85
M		4.3	-	-
N		-	-	10 deg
O		1.2	-	-
Q		0.8	-	-
S		2.9	-	-
T		3.65	-	-
U		1.0	-	-
Variation A	X	-	4.1	4.7
	Y	-	6.5	7.1
Variation B	X	-	4.1	4.7
	Y	-	4.9	5.5
Variation C	X	-	4.3	5.2
	Y	-	6.9	7.5

1. No inward intrusion allowed on the leads.
2. Flash or bleeds on exposed die pad must not exceed 0.5 mm per side.
3. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions must not exceed 0.15 mm per side.

Figure 4. PwSSO36 mechanical drawing



3 PwSSO structure and characteristics

The main structural feature of the PwSSO24 and PwSSO36 is the exposed copper pad onto which the silicon chip is soldered. The exposed copper pad provides a low thermal resistance path from the chip to the external heatsink, which in turn allows the possibility of a reliable exposed pad solution using proprietary depress and deep downset technology.

3.1 Enhanced thermal solution

The PwSSO24/36 exposed pad size is optimized for a good compromise between size and thermal performance. As a result the junction to case thermal resistance is similar to Rth(j-c) of the PwSO20/36 (about 1°C/W), while thermal impedance is below 8°C/W for up to 1 second. Therefore, at this pulse duration, the power dissipation range is still very attractive for many applications (up to 7 W with allowed deltaTj of 50°C).

See *Section 4* for more details of the thermal design.

Note: Remember the importance of the die attach process, typical of power IC packages, which uses a high melting temperature (300°C) tin based alloy.

3.2 High current capability

Different frame designs can be developed providing flexible options (*Figure 5* and *Figure 6*).

If required, two or more leads can be short circuited, as shown in *Figure 5*, and multiple Cu wire bonding implemented (as shown in *Figure 7*), to give a high current capability. Currents up to 80A can be managed provided that the silicon bond pad structure can support 3 mils of Cu wire bonding.

Figure 5. Leads short circuited, option 1

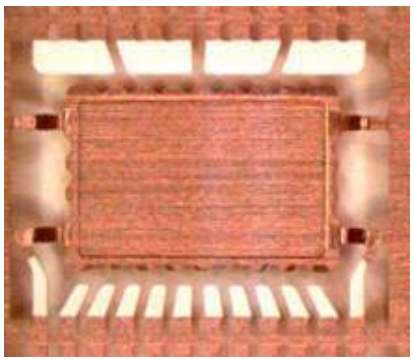


Figure 6. Multiple Cu wire bonding, option 2

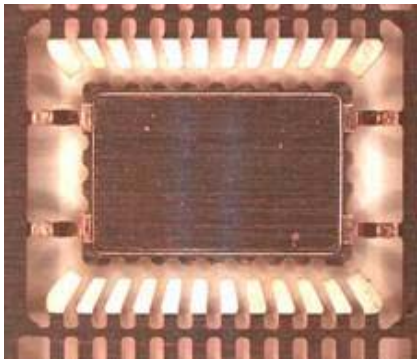
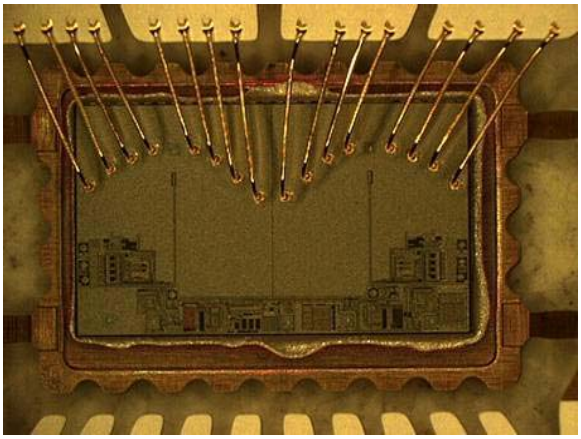


Figure 7. Multiple wires and short circuited leads for high current capability



4 Thermal designs

The thermal characteristics of the PwSSO24/36 packages make them suitable for a wide range of applications in the medium to high power range (1-7 W in “slug-down” configuration).

This section considers a number of typical applications, taking into account the major role played by the temperature increase Tj-Ta required in the different applications. Delta Tj can be as low as 25-30°C in extreme conditions such as automotive or as high as 100°C in some other systems.

Unless otherwise stated, a ΔTj of 50°C and a maximum device temperature of 150°C are assumed in all the examples used in this document.

4.1 Junction-to-case thermal resistance

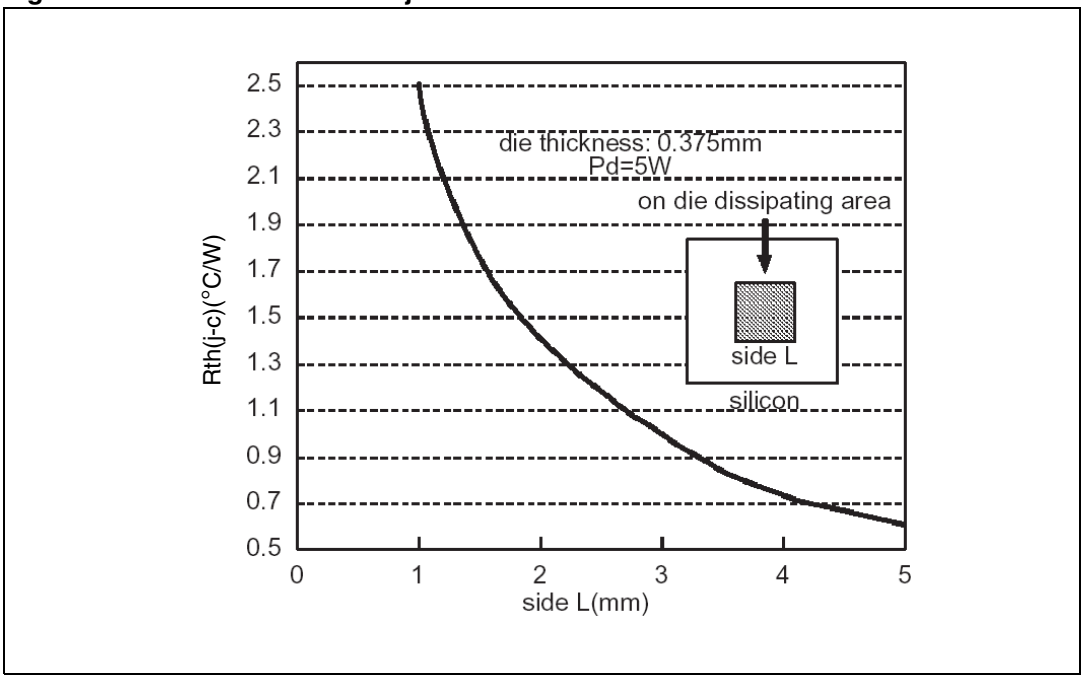
The main feature of the PwSSO packages is the optimization of junction-to-case thermal resistance, from the junction to the external surface of the exposed pad.

Unlike standard SO packages, which use epoxy die attach and thin lead frames, the PwSSO’s take advantage of power package technology, with exposed copper pads and tin based alloy die soldering, which minimizes the junction-to-case thermal resistance Rth(j-c).

Figure 8 shows how Rth(j-c) is affected by the die size, assuming that the power source is uniformly distributed on the die.

For real applications, Rth(j-c) ranges from 2°C/W for small dice to 0.5°C/W for the maximum PwSSO die size of 30mm^2.

Figure 8. Thermal resistance junction-to-case



4.2 Junction-to-ambient thermal resistance

Thermal performance can dramatically change depending on the structure and configuration of the PCB.

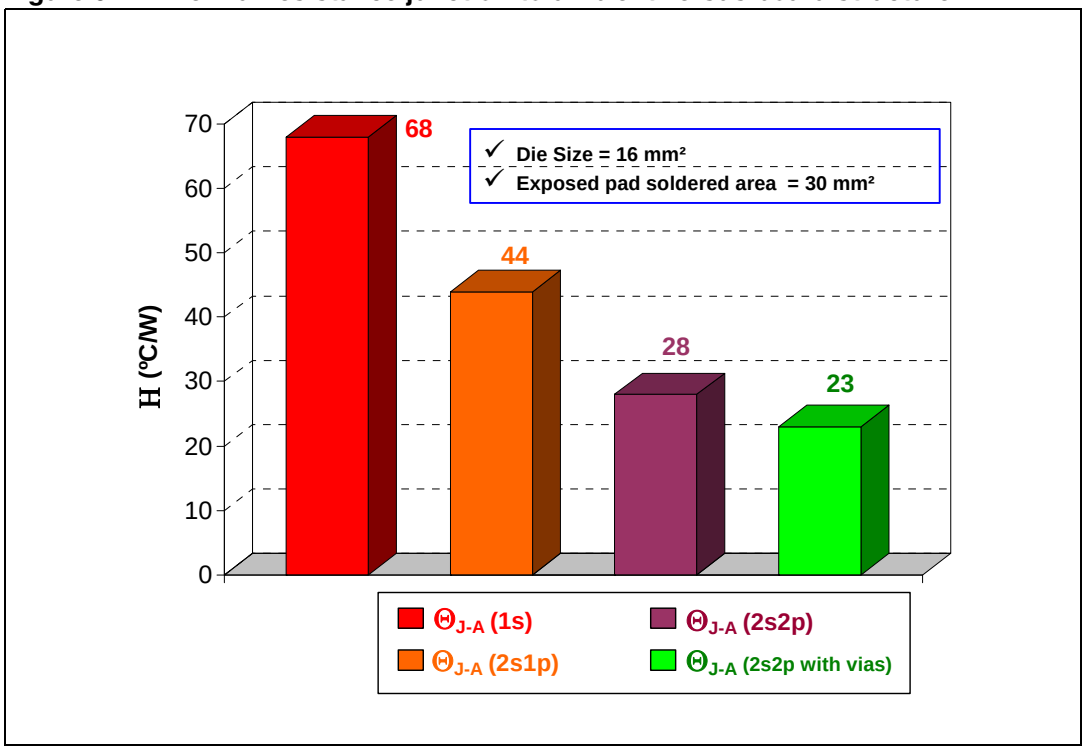
One simple way to improve the thermal efficiency is to add dissipating elements on the PCB surface but this has the drawback of increasing the PCB area which increase the size of the device.

In applications using multi-layer boards with ground layers, the efficiency increases due to the heat spreading effect of the ground layers. If via holes are used, a more direct thermal path is obtained from the exposed pad to the ground layers.

Figure 9 shows that the junction-to-ambient thermal resistance of PwSSO packages can be reduced to 20-23 °C/W if the package is soldered onto a “2s2p” multi-layer board with thermal vias, allowing power dissipation of up to 2.5W.

Refer to *Section 5* for soldering guidelines including suggestions on which high performance PCB footprint should be used.

Figure 9. Thermal resistance junction-to-ambient versus board structure

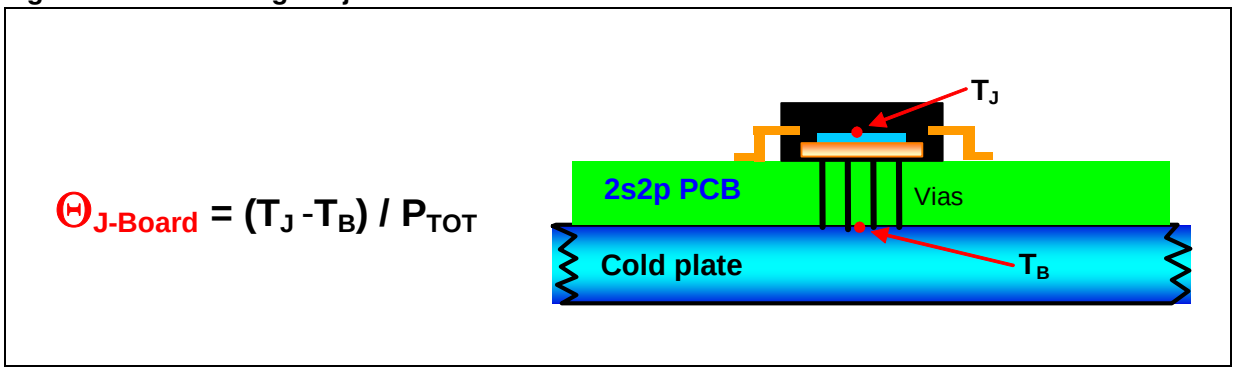


4.3 Junction-to-board (board on heat sink) thermal resistance

In some applications such as automotive, the bottom side of the PCB is put in contact with a metal plate (external heat sink) to improve the thermal dissipation of the module.

The final value of the thermal resistance is calculated by adding the resistance of via holes and the resistance of the plate to the ambient. *Figure 10* shows the schematic for measuring the junction-to-board thermal resistance.

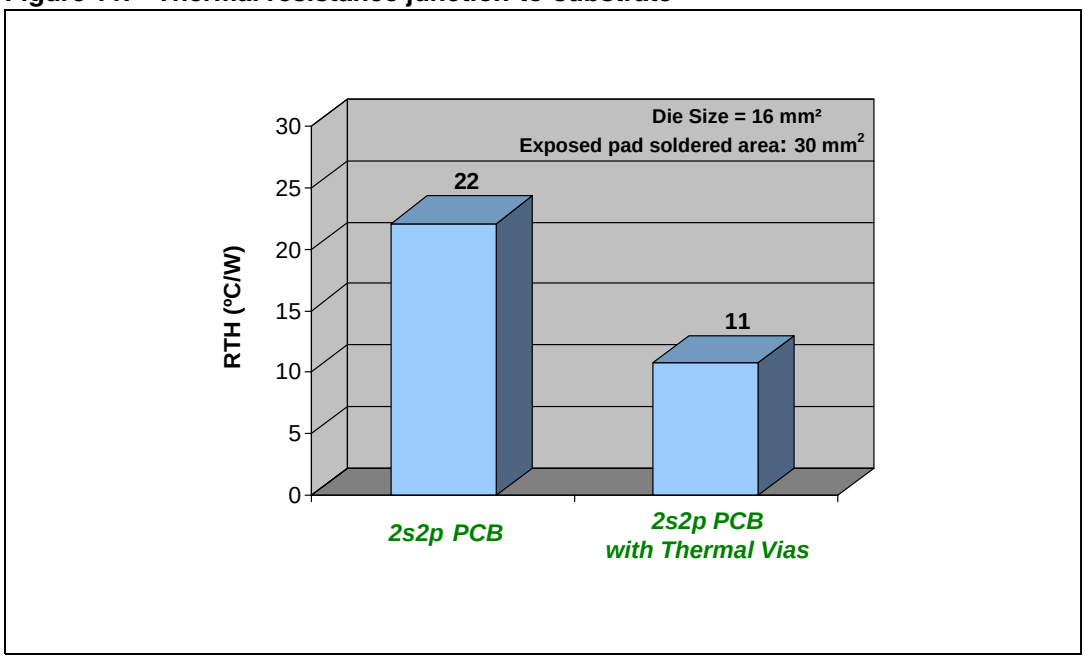
Figure 10. Measuring the junction-to-board thermal resistance



The junction-to-board thermal resistance of PwSSO packages can reach around 11°C/W if the package is soldered onto a “2s2p” multi-layer board with thermal vias (see *Figure 11*).

This means that, with a typical resistance of 2°C/W given by the metal plate, the final thermal resistance is around 13°C/W, allowing a power dissipation of up to 4 watts in steady state.

Figure 11. Thermal resistance junction-to-substrate



4.4 High power dissipation management (10-15 watts)

To be able to achieve an Rth(j-a) of a few °C/W, high power applications must have large (in terms of area and thickness) external heat sinks in close contact with the power device.

This is not a simple requirement when considering cost effectiveness using standard surface mount technology and a simple PCB substrate. However, PCB based surface mount technology is pushing the industry to explore several solutions to improve thermal efficiency.

Rather than a proven solution, the following section should be considered as a preliminary attempt to explore the capabilities of existing surface mount processes and materials, with the objective of increasing heat dissipation at a low cost.

”Slug-up” package and external heat sink

Figure 13 shows a PwSSO36 in “reverse” or “slug-up” configuration. A power dissipation of up to 15W can be achieved by mounting an external heat sink directly on the package’s exposed pad.

A large variety of assembly solutions exist which take advantage of the metal box housing the board.

STMicroelectronics offers a slug-up option for the PwSSO packages, which has been qualified for audio amplifier applications since 2005. However some important automotive customers are now exploring this package option.

For high reliability markets such as automotive, the major concerns are related to the critical assembly of a large heat sink onto a small package. Vibrations and thermal excursions can generate undesirable mechanical stress, which can damaging the package leads or the integrity of the contact between the slug and heat sink.

Tolerances for all the dimensions related to the package height, the heat sink and their surface planarity must be properly controlled to minimize the stress. The thermal and mechanical efficiency can be improved by placing thermal compliant materials like grease and rubber in between the package and the external heat sink (*Figure 12*).

Caution: To minimize the risk of stress on both the package and housed silicon, the force must not exceed 800 N when applying the external heat sink.

Figure 12. Slug-up mounting

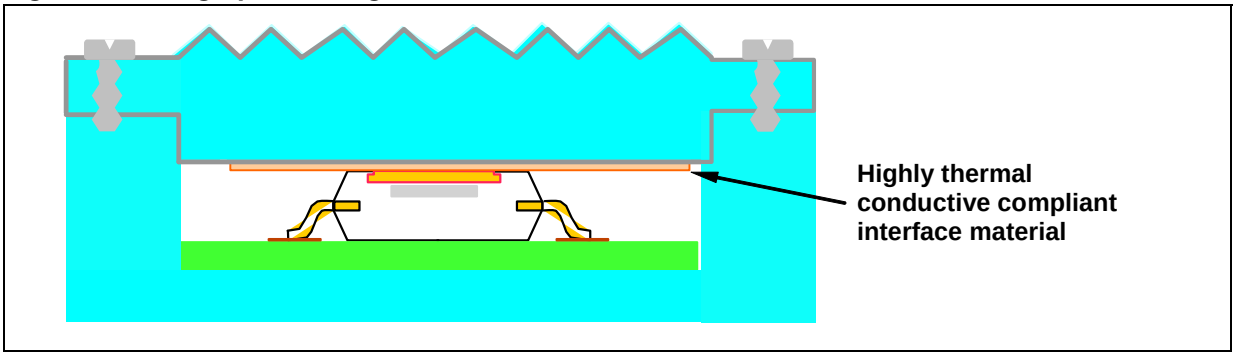
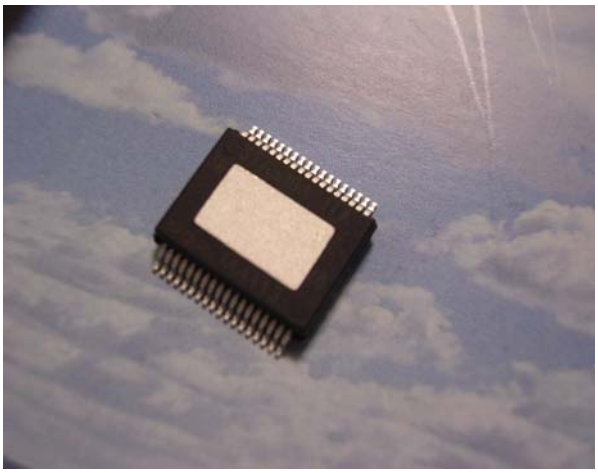


Figure 13. PwSSO36 slug-up



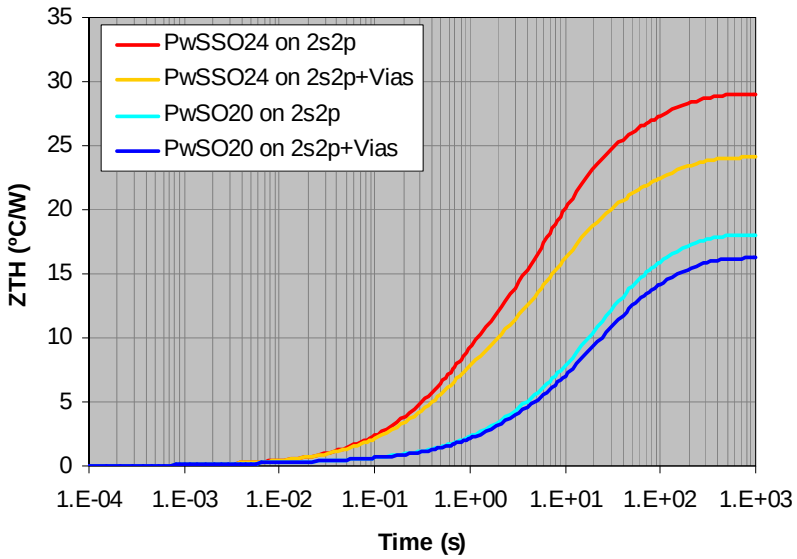
4.5 Thermal impedance

The advantage of the PwSSO over other power packages such as PowerSO20/36 or Multiwatt, is the exposed pad which has the same thickness as the lead frame (10 mils) rather than an integrated thick copper slug.

Nevertheless, the thermal impedance can reach 7 °C/W for a 1 second pulse duration, giving a power dissipation of 7W, which is still a good value for a wide range of applications.

Figure 14 shows a detailed comparison between a PwSSO24 and PowerSO20.

Figure 14. PwSSO vs PowerSO thermal impedance comparison



5 PCB footprint and board mounting guidelines

As explained in *Section 4.2*, thermal vias on PCBs help to enhance the thermal performance of the system.

The PCB soldering pad must be well designed and the soldering process well controlled to make sure that the thermal advantage of vias is not lost.

Figure 15 shows a suggested high performance PCB soldering footprint in which only the selected area of the exposed pad is soldered to ensure a correct out gassing during the reflow operation.

Depending on the PCB assembly capability, an alternative design with thermal vias placed outside the exposed pad area can be also considered. This avoids any risk of uncontrolled solder leakage inside the vias which could cause a package buoyancy effect.

Reflow profile and peak temperature have a strong influence on the formation of voids. Therefore users must follow the reflow profile recommendations of the solder paste supplier, since the reflow profile is specific to the requirements of the flux formulation.

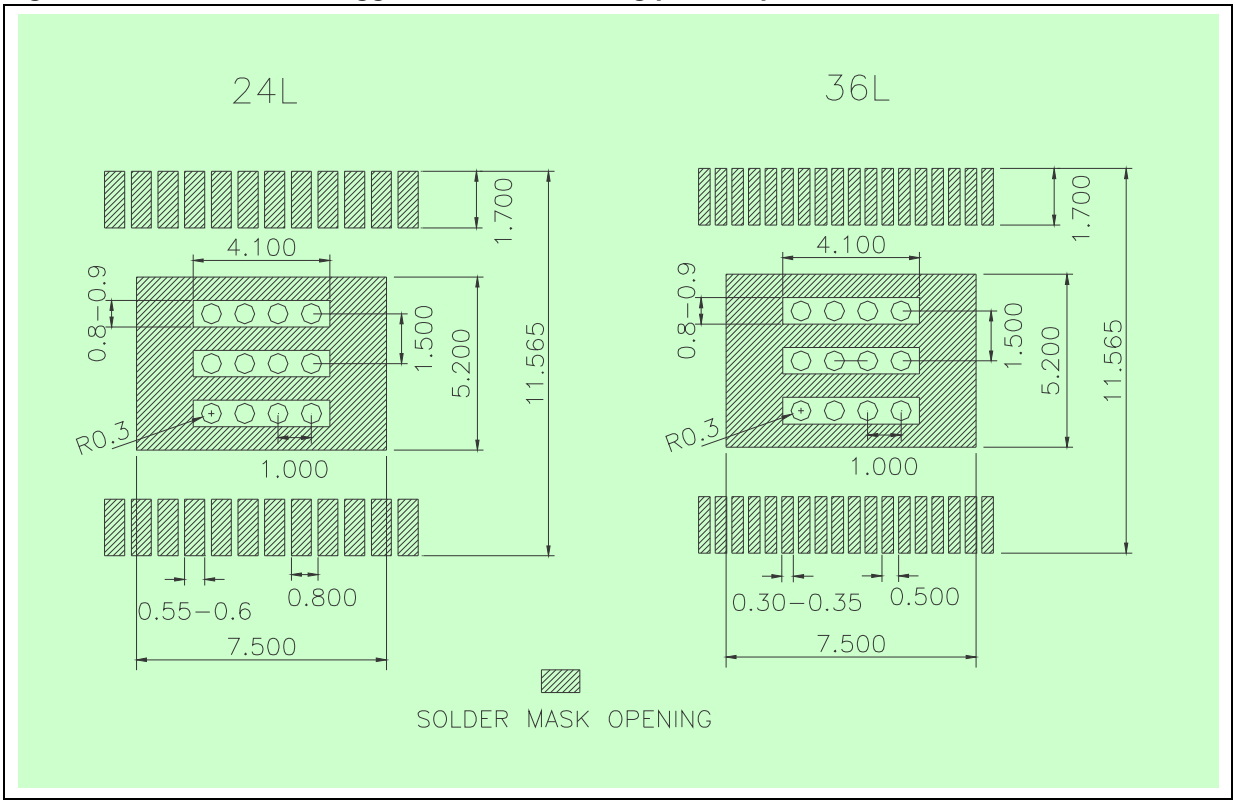
It is important to include post print and post reflow inspection, especially during process development. The volume of paste printed should be measured by either 2D or 3D techniques. The paste volume should be around 80 to 90% of the stencil aperture volume to indicate a good paste release. Stencil thickness should be 0.125 mm SMD (solder mask defined).

After reflow, inspect the mounted package with transmission x-rays for the presence of voids, solder balling, or other defects.

Although STMicroelectronics does not recommend a specific reflow profile, the temperature must not exceed the maximum temperature the package is qualified for, according to the moisture sensitivity level. PwSSO packages are classified as MSL3 with peak temperature of 260 °C.

Refer to the criteria shown in IPC-JEDEC document J-STD-020 for reflow classification and conditions.

Figure 15. PwSSO24/36 suggested PCB soldering pad footprint



Note: STMicroelectronics is not responsible for any PCB related issues. The footprint shown in Figure 15 is a suggestion which might not be in line with the customer/PCB supplier design rules.

6 Electrical modeling

As data transfer rates, gate counts and circuit density continue to grow, the electrical performance of a package plays an increasingly important role on the overall system performance.

State of the art simulation techniques were used to model the electrical inductance of the PwSSO36 package for a specific audio amplifier (*Figure 16*) operating at 1GHz and 50MHz. 30 µm gold and 50 µm copper wires were selected for the simulation.

At 1GHz, self inductance of the leads can vary from 2.8 to 6.1nH, depending on lead length and the type of connected wire, while lead to lead (mutual) inductance is in the range of 1.2 to 2.2nH.

For low frequencies (50MHz), self inductance ranges from 3.4 to 7nH, while mutual inductance is about 2nH.

Figure 17 shows the T-shaped cell used for the simulation model.

Figure 16. PwSSO36 3D view of modeled application

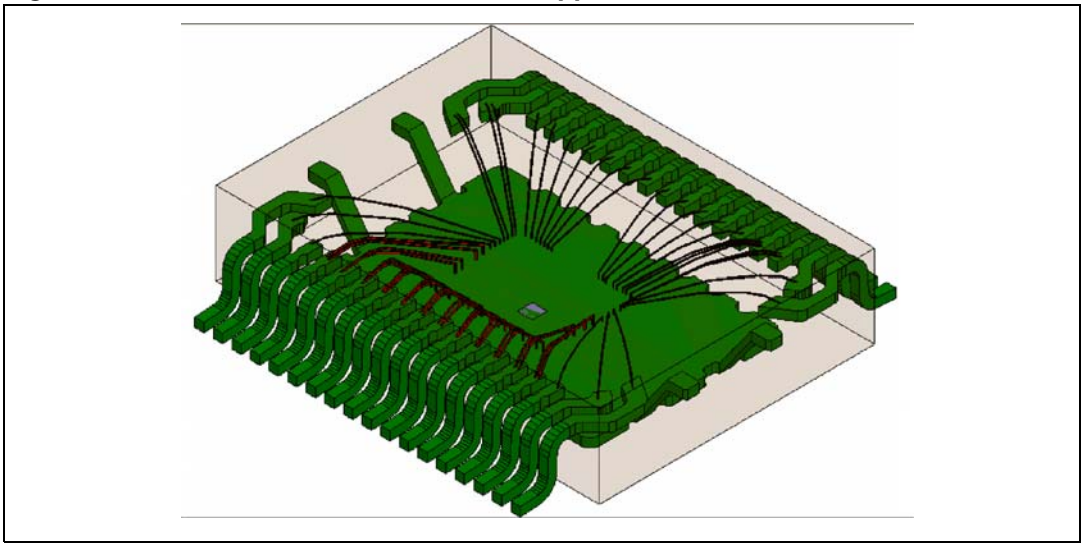
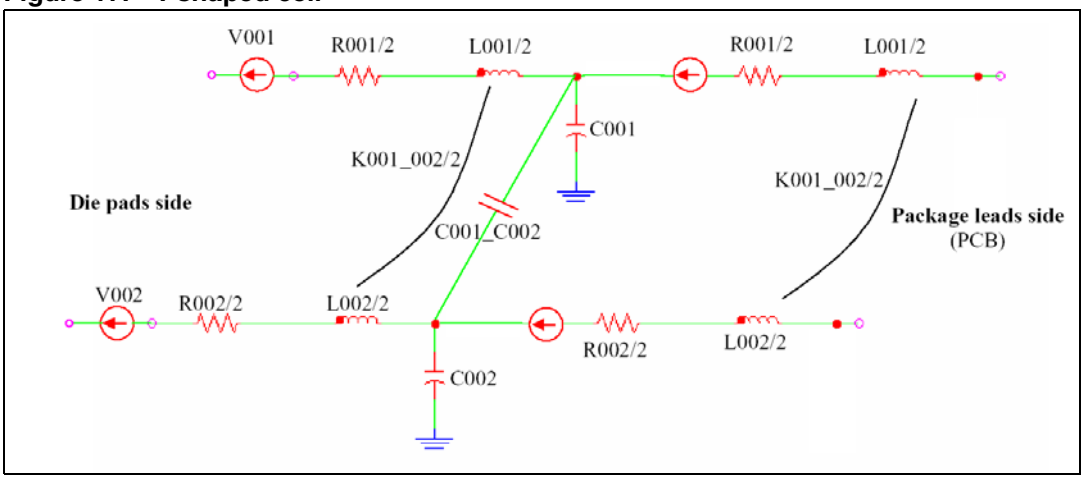


Figure 17. T-shaped cell



7 Reliability data

The information presented in this section shows that PwSSO24 and 36 are able to work reliably in severe environments, such as automotive, where the reliability target is <<1 ppm failure rate.

To evaluate the reliability of the PwSSO packages a complete qualification program was conducted on the PwSSO24 for a specific automotive application and the PwSSO36 for an audio amplifier test vehicle for both slug-down and slug-up options.

A list of main tests, their features and purpose is given in *Table 3*.

Table 3. Reliability tests description

Test	Features	Purpose
High temperature reverse bias (HTRB)	Reverse biased device at elevated temperature	To detect surface defects like poor passivation and contamination
Operating life test (OLT)	Device submitted to application conditions	To put in evidence thermomechanical stress induced by internal power dissipation
Thermal humidity bias (THB)	Biased in presence of steam	Metal corrosion detection
Power temperature cycling	Passive plus active thermal cycling	To check die attach and wire bond integrity
Pressure pot test (PPT)	High temperature and pressure with saturated steam	Electrochemical and galvanic corrosion
Solderability test (ST)	Verifies tinning process	Detects poor solder joints
Environmental sequence (ES)	Thermal cycling combined with pressure pot	To study corrosion mechanism after thermal cycling stress
Surface mount (SM)	Simulation of soldering process in the presence of humidity	To point out the package resistance to the stress due to surface mounting in presence of humidity
Resistance to slovens (RS)	Mil-Std-883 Meth. 2015	To verify the permanency of the marking

Table 4 reports the qualification results of the PwSSO24 with an automotive device.

All the package and die oriented tests were successfully. The test conditions and acceptance criteria are the same as those for standard power packages and follow **AEC-Q100** criteria.

Table 4. PwSSO24 reliability tests results

Test	Test description	AEC Q100 SS	ST test conditions	ST SS	Results fail/SS	Generic data
HTOL	High temperature operative live	77 x 3 lots	TA = 125°C Bias = 28 V Time = 1000 hours	77	0/77	0/231
HTB	High temperature bake	77 x 1 lots	TA = 150°C Time = 1000 hours	77	0/77	0/231
PC	Preconditioning before THB, TC	All devices to be subjected to THB, TC	Drying 24 h @ 125°C store 192 h @ TA = 30°C RH = 60% IR 3 time @ 260°C	154	0/281	
THB	Temperature humidity bias	77 x 3 lots	TA = 85°C Bias = 28 V Time = 1000 hours	77	0/77	0/240
AC	Autoclave	77 x 3 lots	TA = 121°C -PA = 2 ATM Bias = 28 V Time = 1000 hours	77	0/77	0/240
TC	Temperature cycling	77 x 3 lots	TA = –65°C to 150°C 1 hour/cycle Time = 1000 cycles	77	0/77	0/250
EV	External visual	All devices submitted for testing			0/600	
PD	Physical dimensions	30 x 1 lot		30	0/30	
LI	Lead integrity	45 leads from min. of 5 devices x 1 lot		5	0/5	
BPS	Bond pull strength	30 bonds from a min. of 5 devices x 1 lot		5	0/5	
BS	Bond shear	30 bonds from a min. of 5 devices x 1 lot		5	0/5	
ESD	Electrostatic discharge	Min. 3/V level/model x 1 lot		*		
LU	Latch-up	6 x 1 lot		*		
SD	Solderability	15 x 3 lots		45	0/45	
ELFR	Early life failure rate	800 x 3 lots	Time = 48h TA = 125°C Bias = 28V	*		0/140000
GL	Gate leakage	6 x 1 lot	Time = 720 sec – E-field = ±400V–TA = 155°C	6	0/6	
ED	Electrical distributions	30 x 3 lots		*		

Table 5 reports the qualification results of the PwSSO36 with an audio amplifier device.

Table 5. PwSSO36 reliability tests results

Test	Conditions	Sample size	Duration	Failure
HTOL(1)	Vs=32V, Tj=150°C, Load=8Ω	15 x 3 lots	1000h	0
HTRB(2)	Vs=40V, Tj=150°C, standby	20 x 3 lots	500h	0
HTS(2) (3) (7)	Ta=175°C, unbiased	50 x 3 lots	500h	0
PC(2) (4)	Bake: 24h @ 125°C	All the part submitted to THB, AC and TC	-	0
THB(2) (5)	Vs=40V, Ta=85°C, RH=85%, standby	20 x 3 lots	1000h	0
TC(2) (6) (7)	Ta=–50°C/+150°C	50 x 3 lots	1000h	0
AC(2) (7)	Ta=121°C, P=2atm	50 x 3 lots	168h	0

1. Parts assembled in PwSS036 slug-down.
2. Parts assembled in PwSS036 slug-up.
3. The test was continued to 2000 hours on a reduced sample size. No failures were detected.
4. No die-delamination was observed at SAM analysis before and after the stress test.
5. The test was continued to 2000 hours. No failures were detected.
6. The test was continued to 2000 cycles on a reduced sample size. No failures were detected.
7. No defects were detected after DPA

8 Environmentally friendly packages

The electronics industry started converting to lead-free processes in 2004-2005 but although consumer electronics are now completely converted to lead-free, high reliability sectors require strenuous qualification tests and verifications before the conversion can be implemented.

For example, automotive electronics modules are still exempted from RoHS lead-free legislation, although most manufacturers in this sector are seriously investigating Pb-free processes to help vehicle manufacturers meet the End of Life Vehicles (ELV) mandate.

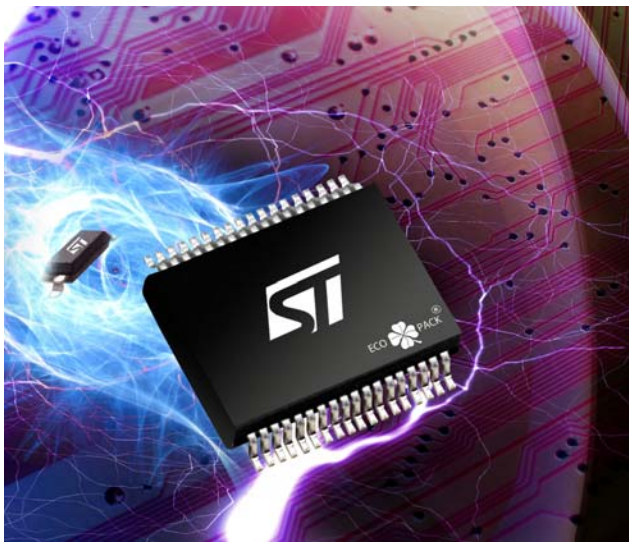
To meet environmental requirements, STMicroelectronics offers most of their devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

The PwSSO24/36 are ECOPACK (RoHS compliant) due to the pure-tin finishing of the terminals. In addition to RoHS compliancy, the environmental characteristics of the packages are reinforced by using a halogen-free (Br/Sb) mold compound.

As well as being environmentally friendly, the choice of a halogen-free mold compound increases the high temperature life-time (up to 175 °C) by a factor of 10 compare to similar packages based on Br/Sb2O3.

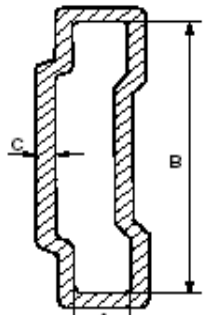
Figure 18. PwSSO36 ECOPACK package



9 Packing information

The PwSSO packages can be shipped in either tube or tape & reel form. *Figure 19* and *Figure 20* show the packing information.

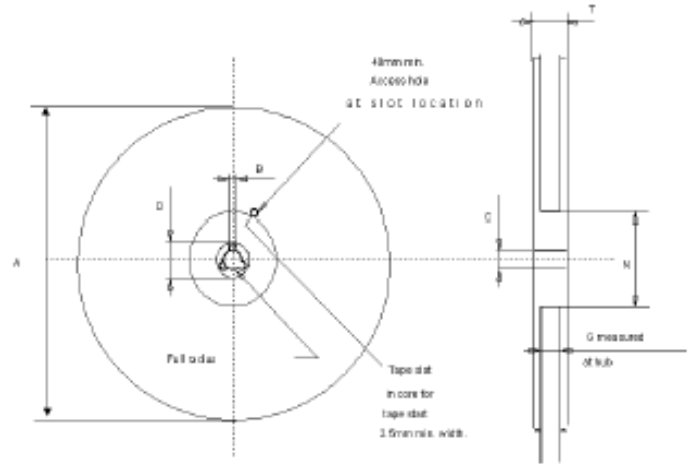
Figure 19. PwSSO24/36 tube packing (no suffix in part number)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 20. PwSSO24/36 tape and reel packing (suffix "TR")



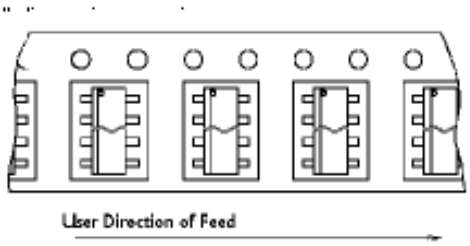
REEL DIMENSIONS

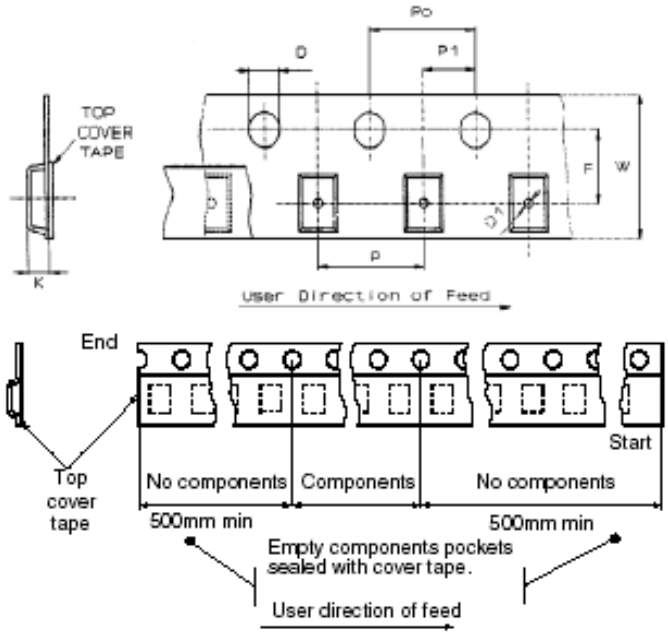
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (±0.1)	4
Component Spacing	P	12
Hole Diameter	D (±0.05)	1.55
Hole Diameter	D1 (min)	1.5
Hole Position	F (±0.1)	11.5
Compartment Depth	K (max)	2.85
Hole Spacing	P1 (±0.1)	2





10 Conclusion

STMicroelectronics designed and developed the PwSSO (JEDEC MO-271) packages to satisfy market demands for surface mount assembly and the reduction in size of power modules.

The main advantages of PwSSO24/36 are:

1. Good thermal characteristics and high power density through reduced package footprint and height (they can house a die size of up to 30 mm^2).
2. Versatility - a wide variety of intelligent power products with a wide range of options can be managed due to the different mounting options offered by the package.
3. High reliability - the correct choice of materials and particular design features ensure that the PwSSO24/36 pass the severe tests required by the automotive market.

11 Revision history

Table 6. Document revision history

Date	Revision	Changes
19-Oct-2007	1	Initial release.