PEX 8624-AA RDK
Hardware Reference Manual

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PREFACE

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ABOUT THIS MANUAL

This document describes the PLX PEX 8624-AA RDK, a Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes complete schematics and bill of materials.

Note: This Hardware Reference Manual is specific to the PEX 8624 RDK. In the event of a discrepancy between this Hardware Reference Manual and the PEX 8624 Data Book, please be sure to follow the instructions and guidelines as stated in the PEX 8624 Data Book when designing your systems.

REVISION HISTORY

Date	Version	Comments
1/2/2008	0.81	Hardware Reference Manual initial release.
1/18/2008	0.82	Added SHP configuration, updated the BOM and schematics.
2/8/2008	0.83	Updated Table 2-4 and schematics.
4/11/2008	1.0	Updated BOM and Schematics.
5/3/2010	1.1	Updated BOM and Schematics for the replacement On Semi CAT25080LI-G EEPROM. Added note to follower Data Book in the case of a discrepancy with Hardware Reference Manual in “About This Manual” section.

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TABLES

1. General Information

The PLX PEX 8624-AA RDK is a Rapid Development Kit based on the PEX 8624, a 24-lane, 6-port PCI Express Gen 2 switch. The PEX 8624-AA RDK provides a complete hardware and software development platform that facilitates getting designs up and running quickly, lowering risk and reducing time-to-market. This RDK allows the upstream port of the PEX 8624 to be directly plugged into a system board's x8 or x16 PCI Express connector, or plugged into an x4/x1 PCI Express connector by using card edge adapters.

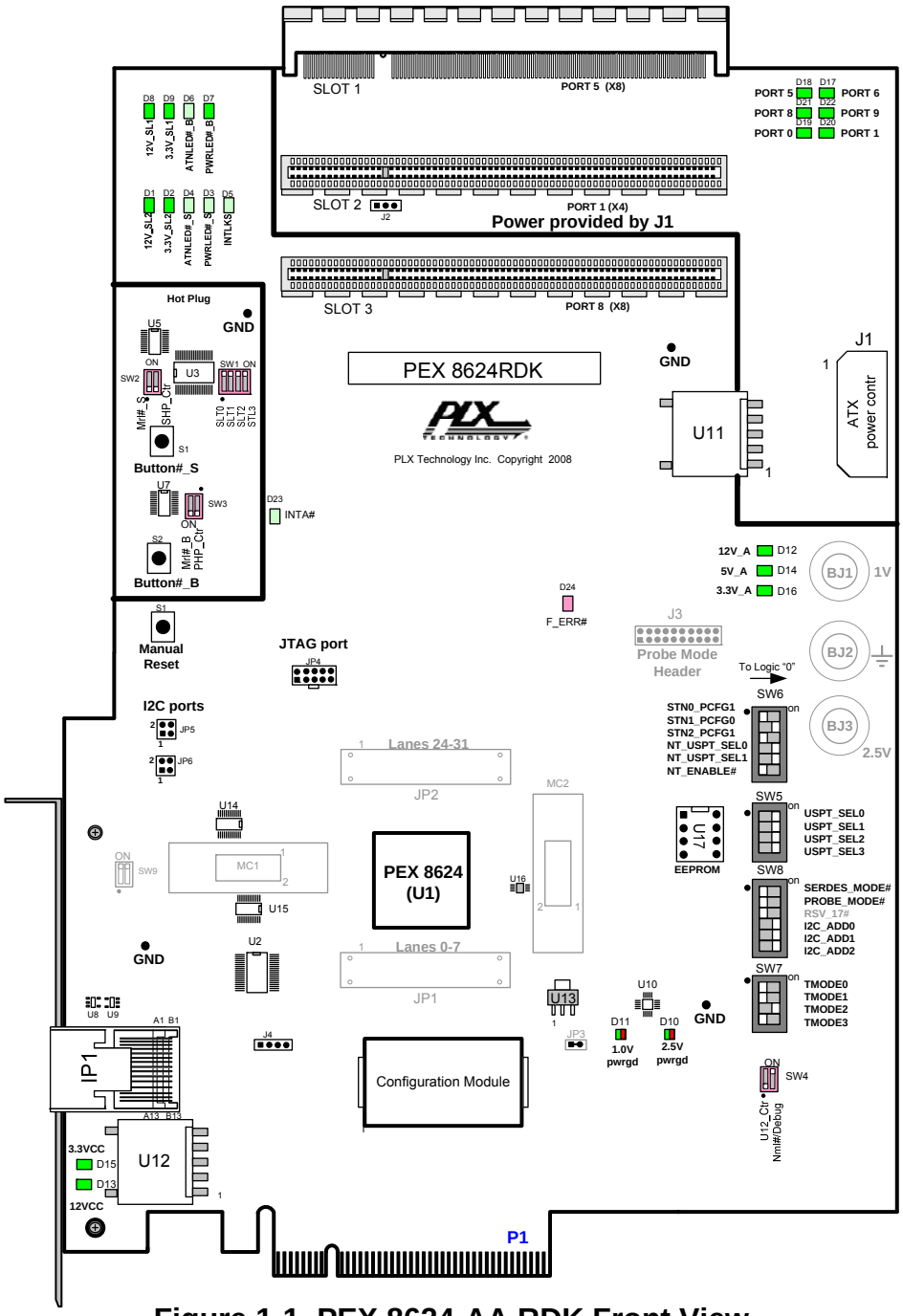

Figure 1-1. PEX 8624-AA RDK Front View

1.1 PEX 8624 Features

- 24-lane, 6-port PCI Express Gen 2 switch with integrated on-chip SerDes
- 240 GT/s aggregate bandwidth (5.0GT/s/Lane x 24 Lanes x 2 (full duplex))
- 19mm^2 324-ball Flip-Chip Plastic Ball Grid Array (FCBGA) package
- Typical Power – 3.01 W
- Cut-Thru packet latency of less than 150ns (x8 to x8)
- Low power SerDes (under 90mW per lane)
- Fully non-blocking switch architecture
- Flexible port configuration
    - Ports configurable as x8 or x4, with auto link-width negotiation to x2 and x1
- Flexible device configuration
    - Configurable via serial EEPROM, I^{2}C, hardware strapping, or by the host
- Maximum packet payload size of 2,048 bytes
- Designate any Port as the *Upstream Port* (Port 0 is recommended)
- Dynamic Buffer Pool Architecture
- Read Pacing (allows user to throttle Read requests from Downstream Ports to allow for more efficient performance)
- Dual casting (enhances performance by sending date from one ingress port to two egress ports)
- Dynamic speed (2.5 GT/s or 5.0 GT/s) negotiation
- Dynamic link-width negotiation (automatically negotiates down to optimal link-width based on traffic density)
- Lane and polarity reversal
- Non-Transparent Bridging support
    - Enables Dual-Host, Dual-Fabric, Host-Failover applications
- Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 **(**with Vaux not supported)
- Conventional PCI-compatible Device Power Management states – D0 and D3hot
- Active State Power Management
- Quality of Service (QoS)
    - One Virtual Channels (VC0) and Eight Traffic classes (TC)
    - Round-Robin and Weighted Round-Robin Port arbitration
- Reliability, Availability, Serviceability (RAS) features
    - PCI Express Standard Hot-Plug Controller for three Ports, include optional usage models for Manually operated Retention Latch, by way of MRL Sensor and Attention Button support
    - Electromechanical Interlock supported with Power Enable output
    - Baseline and Advanced Error Reporting capability
    - Performance Monitoring
        - Per-Port Payload and Header Counters
        - Per-traffic type (write, Read, Completion) Counters
    - JTAG AC/DC boundary scan
    - 6-port link status indicators (PEX_PORT_GOOD[9,8,6,5,1,0]#)
    - 14 GPIO and/or Serial Hot-Plug PERST# pins
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- Compliant to the following specifications:
    - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
    - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
    - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
    - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
    - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
    - *PCI Express Card Electromechanical (CEM) Specification, Revision 2.0*
    - *PCI ExpressCard CEM r2.0)*
    - *PCI Express Mini Card Electromechanical (CEM) Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
    - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990 (IEEE Standard 1149.1-1990)*

- *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
- *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
- *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
- *The I2C-Bus Specification, Version 2.1 (I2C Bus v2.1)*

1.2 PEX 8624-AA RDK Features

- PLX PEX 8624 PCI Express switch in a 324-ball Flip-Chip Plastic BGA package
- Form factor based on PCI Express Card Electromechanical (CEM) Specification 2.0
- Ships with default configuration of three x8 Ports
  - All PEX 8624 lane/port configurations supported with breakout boards and configuration modules
- Non-Transparent Bridging support
- Two x8 Gen 2 Midbus probe footprints for one upstream and one downstream port PCI Express signal probing
- On-board PCI Express RefClk buffer which supports Spread Spectrum Clocking
- Parallel Hot-Plug and Serial Hot-Plug circuits
- Socketable Serial EEPROM (2.5V)
- Two standard 2x2 headers provides the I^2C interface to an I^2C master
- DIP switches for port configuration, upstream port or NT port select and I^2C address settings
- Manual push-button PERST# capability
- Up to six Lane Status indicator LEDs for visual inspection of link speed and status
- Voltage level monitoring circuit for 1.0V and 2.5V power to the PEX 8624

2. PEX 8624-AA RDK Hardware Architecture

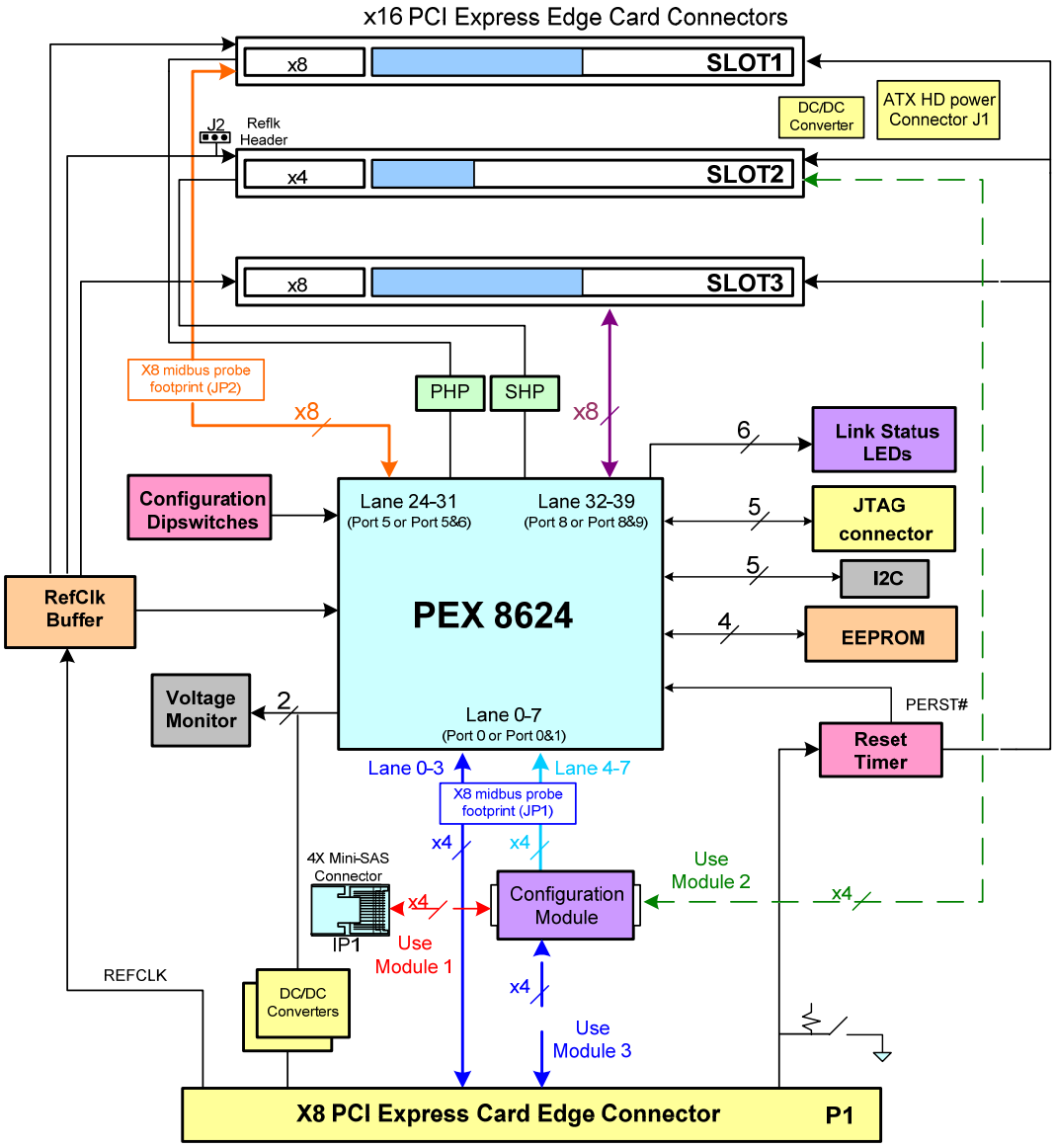

Figure 2-1. PEX 8624-AA RDK Hardware Architecture

2.1.1 PEX 8624 PCI Express Gen 2 Switch

The PEX 8624 is a 24-lane, 6-port PCI Express Gen 2 (5.0GT/s) switch. It is designed with three stations, with each station housing eight lanes. Station 0 contains lanes 0 thru 7, Station 1 contains lanes 24 thru 31, and Station 2 contains lanes 32 thru 39. Each station can be configured as one x8 port or two x4 ports. Each port can then auto-negotiate its link-width down to x2 or x1.

2.2 PEX 8624-AA RDK PCI Express Interfaces

The PEX 8624-AA RDK is designed around the PEX 8624, a 6-port, 24-lane Gen 2 switch, and is based on the form factor specified in the PCI Express CEM 2.0 Specification. The PEX 8624-AA RDK offers five PCI Express (PCIe) interfaces: a x8 PCI Express Card Edge connector (P1), three x16 PCI Express Edge Card connectors (SLOT 1, SLOT 2, & SLOT 3), and a 4X Mini-SAS connector (IP1).

Although the three PCIe slots (SLOT 1-3) have a x16 link-width form factors, the slots themselves are configured as x8 for SLOTs 1 & 3, and x4 for SLOT 2 as shown in Figure 2-1 above. Using a x8-to-x4x4 Breakout Board, the x8 slots (SLOTs 1 & 3) can be broken out into two x4 slots, creating two x4 ports from a x8 slot.

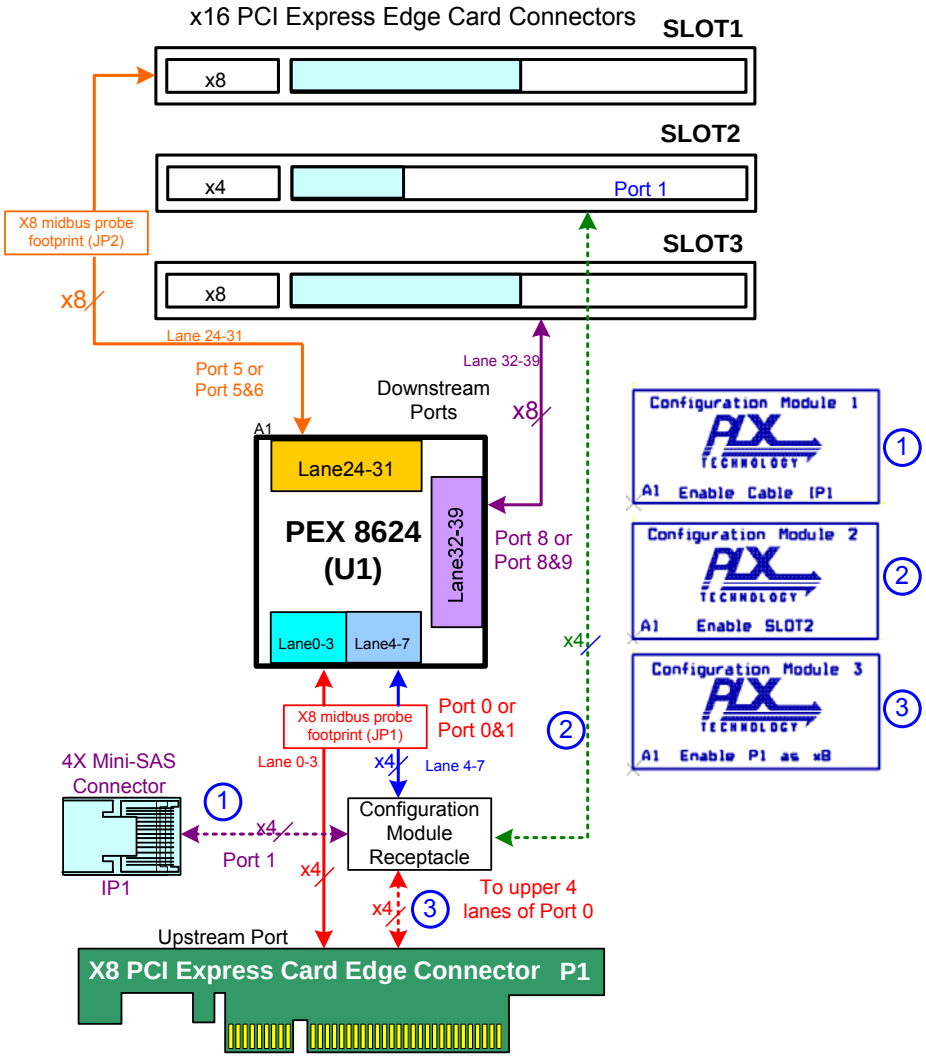

Figure 2-2. PCI Express up to 5GT/s Gen 2 Connections

2.2.1 Configuration Modules and Receptacle CM1

Configuration Module Receptacle CM1 is a 200-pin high-speed Mezzanine Connector. It is soldered on the PCB of PEX 8624-AA RDK. It directly connects to lane 4 to lane 7 of the PEX 8624, lane 4 to lane 7 of PCI Express card edge connector P1, lane 0 to lane 3 of PCI Express Edge Card Connector SLOT 2, and lane 0 to lane 3 of 4x mini-SAS connector IP1.

One of three configuration modules (see Figure 2-2) can be plugged into the Configuration Module Receptacle (CM1) of the PEX 8624-AA RDK. Which Configuration Module is used determines how lanes 4-7 of the PEX 8624 are routed:

1) Configuration Module 1 (marked “Enable Cable IP1”) routes lanes 4-7 to the 4X Mini-SAS Connector.
2) Configuration Module 2 (marked “Enable SLOT 2” routes lanes 4-7 to PCIe SLOT 2.
3) Configuration Module 3 (marked “Enable P1 as x8”) routes lanes 4-7 to the x8 PCIe Card Edge Connector to enable P1 as a x8 Port.

Figure 2-2 shows the RDK PCI Express Gen 2 connections and the top view of the three configuration modules. By default, PEX 8624-AA RDKs are shipped to customers with Configuration Module 3, enabling three x8 ports. To achieve other configurations, a combination of x8-to-x4x4 Breakout Boards and/or Configuration Modules 1 or 2 will be required.

2.2.2 PCI Express Card Edge Connector P1

Card Edge Connector P1 can directly plug into a x8 or x16 PCI Express slot. Lanes 0-3 of PEX 8624's Port 0 is connected to this connector through a x8 midbus probe footprint (JP1). PEX 8624's lanes 4-7 also passes through the x8 midbus probe footprint (JP1) and connects to the CM1 receptacle. When Configuration Module 3 is plugged into the CM1 receptacle, the PEX 8624's lanes 4-7 are routed to Connector P1 and become the upper four lanes of Port 0's x8 link. By default, the PEX 8624-AA RDK sets this port to be the upstream port. Connector P1 also provides 12V and 3.3V power, along with PERST# and REFCLK_P/N to the RDK.

2.2.3 PCI Express Edge Card Connector SLOT 1

Connector SLOT 1 is a straddle-mount, x16 PCI Express connector. Cards plugging into this slot will be in-line with the RDK. Eight lanes, lanes 24-31, from the PEX 8624 are connected to this connector. The default configuration of the PEX 8624-AA RDK sets the x8 link, Port 5, at this connector to be a downstream port. With a x8-to-x4x4 breakout board plugged into the connector, the x8 link at port 5 can be split into two x4 links, Port 5 and Port 6. Power is provided to this connector from the ATX hard disk power connector J1 through the power MOSFETs which are controlled by the Parallel Hot-Plug Controller (PHPC) of PEX 8624 (see Section 2.5.1 for details).

2.2.4 PCI Express Edge Card Connector SLOT 2

Connector SLOT 2 is a vertical-mount through-hole x16 PCI Express connector. Cards plugging into this slot will be perpendicular to the RDK. When Configuration Module 2 is plugged into the CM1 receptacle, lanes 4-7 from the PEX 8624 pass the midbus probe footprint JP1 and CM1 and connects to Lane 0 to lane 3 of this connector. Depending on the port configuration, port 1 at connector SLOT 2 can be a downstream port, upstream port or an NT port. Power is provided to this connector from the ATX hard disk power connector J1 through the power MOSFETs which are controlled by the Serial Hot-Plug Controller of the PEX 8624 (see Section 2.5.2 for details).

2.2.5 PCI Express Edge Card Connector SLOT 3

Connector SLOT 3 is a vertical-mount through-hole x16 PCI Express connector. Cards plugging into this slot will be perpendicular to the RDK. Eight lanes, lanes 32-39, from PEX 8624 are connected to this connector. The default configuration of the PEX 8624-AA RDK sets the x8 link, Port 8, at this connector to be a downstream port. With a x8-to-x4x4 breakout board plugged into this connector, the x8 link can be split into two x4 links, Port 8 and Port 9. Power is provided to this connector from the PCI Express card edge connector P1.

2.2.6 4X Mini-SAS Connector IP1

PEX 8624 only supports Non-Transparent (NT) mode on Port 0 or Port 1 of Station 0. The 4X mini-SAS connector IP1 provides the simplified connections for the customers to connect the PEX 8624-AA RDK to two PC motherboards. When the Configuration Module 1 is plugged into the CM1 receptacle, lanes 4-7 from the PEX 8624 pass the midbus probe footprint JP1 and CM1 and connects to the 4X mini-SAS connector IP1. Depending on the port configuration, Port 1 at connector IP1 can be set as a downstream port, upstream port or an NT port. Figure 2-3 shows a set up using PEX 8624-AA RDK's NT function. Either Motherboard A or B can be connected to an upstream port or NT port of the PEX 8624.

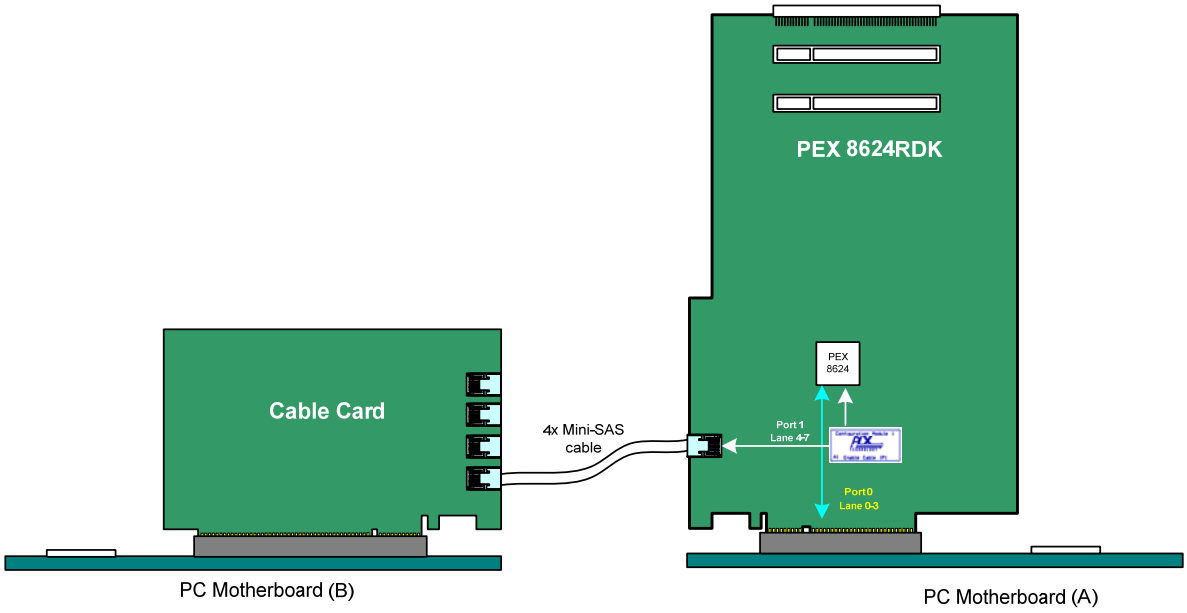

Figure 2-3. Use mini-SAS Connector for NT Function Setup

2.3 Reference Clock Circuitry

The PEX 8624-AA RDK reference clock circuitry contains a one-to-four differential clock fan out buffer (U2) from SpectraLinear (CY28400-2). The clock fan out buffer supports four 100 MHz PCI Express reference clocks with the option for constant frequency and spread spectrum outputs. When the RDK is plugged into a PCI Express slot of a PC motherboard, the differential reference clock input to the fan out buffer is taken from the PCI Express card-edge connector (P1), and the differential clock outputs are distributed to the PEX 8624 reference clock input (PEX_REFCLKP/PEX_REFCLKN), downstream slot connectors (SLOT 1, SLOT 2 and SLOT 3), and the reference clock header J2. The 3-pin reference clock header (J2) provides a reference clock input which is to be used in conjunction with the midbus probe(s). The reference clock outputs from the fan out buffer (U2) to SLOT1 and SLOT 2 are controlled by the parallel Hot-Plug circuit and the Serial Hot-Plug circuit respectively. (See Figure 2-4 and Section 2.5 for details)

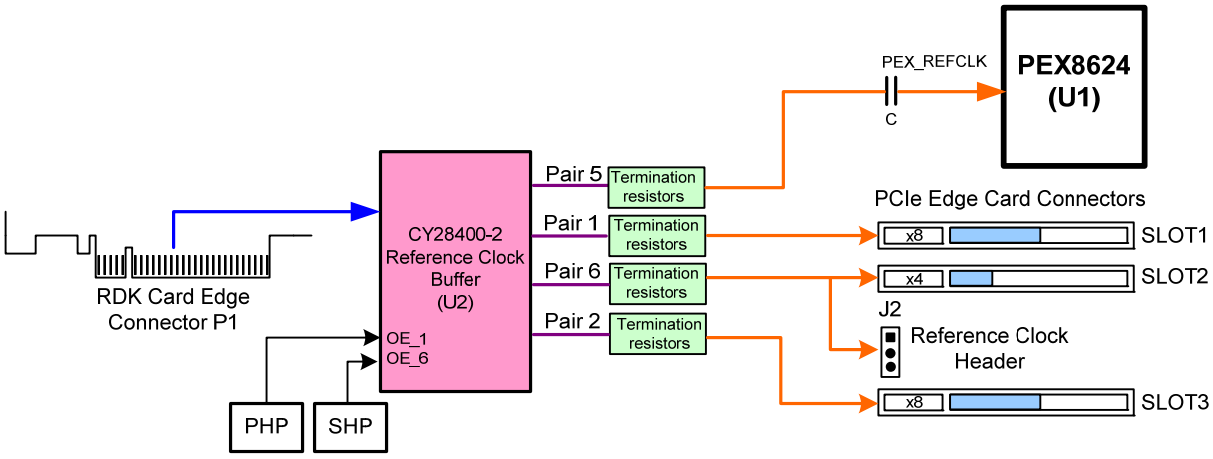

Figure 2-4. PEX 8624-AA RDK Reference Clock Circuit

2.4 Reset Circuitry

The PEX 8624-AA RDK reset circuitry includes a MAX6420 adjustable reset timer (U9), a Fairchild 2-input AND gate NC7S08 (U8) and manual reset push-button switch (S1). The reset timer accepts PERST# from the card edge (P1) and from S1 (logical-OR via U8). The MAX6420 has the capability of adjusting the reset timeout period by changing the value of C70 (0.001μF ≈ 3ms). (See Figure 2-5 for details)

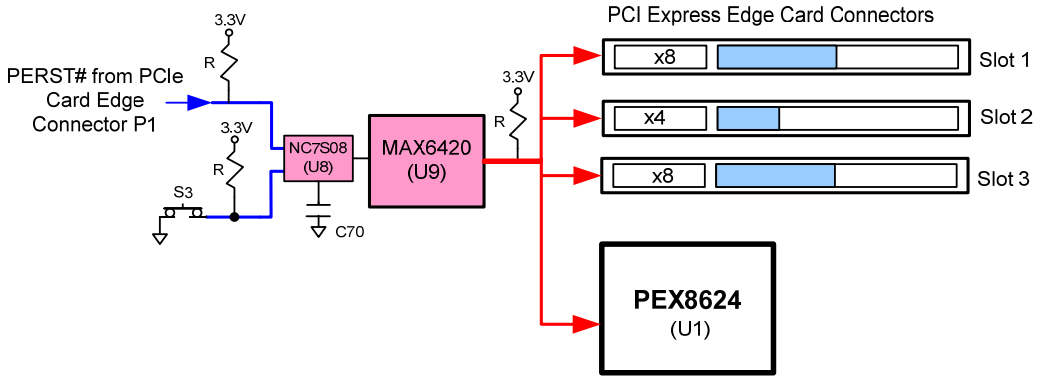

Figure 2-5. PEX 8624-AA RDK Reset Circuit

2.5 Hot-Plug Circuits

PEX 8624 provides on-chip Parallel Hot-Plug controllers to downstream ports 1, 5 and 9. The remaining downstream ports are also Hot-Plug capable through the use of the I2C bus and external I/O expander devices. The PEX 8624-AA RDK implements Hot-Plug control circuitry for SLOT 1 and SLOT 2. SLOT 1 uses the on-chip parallel Hot-Plug controller while SLOT 2 uses the Serial Hot-Plug control capability through the I2C and I/O expander. Note that additional device configuration should be required when using the Serial Hot-Plug capability. (See Section 2.5.2 and PEX 8624-AA Data Book for details)

2.5.1 Parallel Hot-Plug Controller Circuit

PEX 8624-AA RDK uses the Parallel Hot-Plug controller on Port 5 for PCI Express connector SLOT 1. The parallel hot-plug controller consists of five input elements (HP_BUTTON_B#, HP_MRL_B#, HP_PRSNT_B#, HP_PWR_GOOD_B, HP_PWRFLT_B#) and five output elements (HP_ATNLED_B#, HP_CLKEN_B#, HP_PERST_B#, HP_PWREN_B, HP_PWRLED_B#).

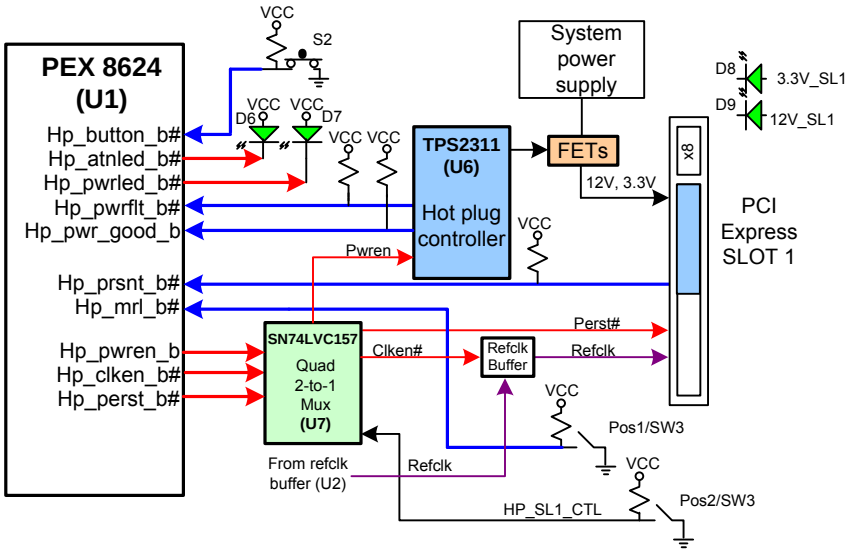

Figure 2-6. PEX 8624-AA RDK PHP Circuits

Figure 2-6 shows the parallel hot-plug circuit. It includes a low cost TI dual hot–swap power controller TPS2311 (U6), a quad 2-to-1 multiplexer SN74LVC157 (U7), two International Rectifier power MOSFET IRF7470 (Q3 and Q4), LEDs, manual switch, dipswitch and resistors. The manual switch (S1) connects to the HP_BUTTON_B# input of the PEX 8624. It is used to generate the active low Hot-Plug attention button signal to the parallel hot-plug controller. LEDs D6 and D7 represent the HP_ATNLED_B# (the attention LED) and HP_PWRLED_B# (power LED) respectively on the parallel hot-plug controller. The PRSNT2# signal from SLOT 1 connects to the HP_PRSNT_B# signal on the parallel hot-plug controller. This signal is used to detect when a PCI Express adapter card is plugged into the connector SLOT 1. SW3 (position 1) is used to emulate the manually operated retention latch sensor input HP_MRL_B# to the parallel hot-plug controller. When set to “ON” position, the internal state machine of the parallel hot-plug controller is enabled. SW3 (position 2) is used to enable the power and clock to SLOT 1. When set to the “ON” position, the active low signal HP_SL1_CTL on the multiplexer (U7) will select HP_PWREN_B# to enable the hot-swap power controller (U6), HP_CLKEN_B# to enable the RefClk output to connector SLOT 1, and the reset signal HP_PERST_B# to connector SLOT 1. Inversely when set to the “OFF” position (SW3 position 2), the active high signal HP_SL1_CTL will bypass the Hot-Plug control outputs from the parallel hot-plug controller and select another set of outputs to enable the hot-swap power controller (U6), and enable the RefClk output and PERST# to connector SLOT 1.

When enabled, the hot-swap power controller (U6) monitors the 12V and 3.3V voltage supplies to SLOT 1. When current levels exceed 5A, HP_PWRFLT# becomes active. Similarly, HP_PWR_GOOD_B becomes active when lower than normal current levels are detected. PWRGD1 and PWRGD2 implement pull-up with external resistor.

Two additional LEDs, D8 and D9, are used to indicate 3.3V and 12V power at the connector SLOT 1.

2.5.2 Serial Hot-Plug Controller Circuits

PEX 8624-AA RDK also implements the serial hot-plug controller circuitry to PCI Express SLOT 2. By default, the RDK is configured to bypass the serial hot-plug controller. In order to configure port 1 at PCI Express SLOT 2 as a Serial Hot-Plug port with the port 0 is still a x4 upstream port, use the EEPROM to write 2’b00 to the bit [14:13] of station 0’s Parallel Hop-Plug capable configuration register at offset 1E0h.

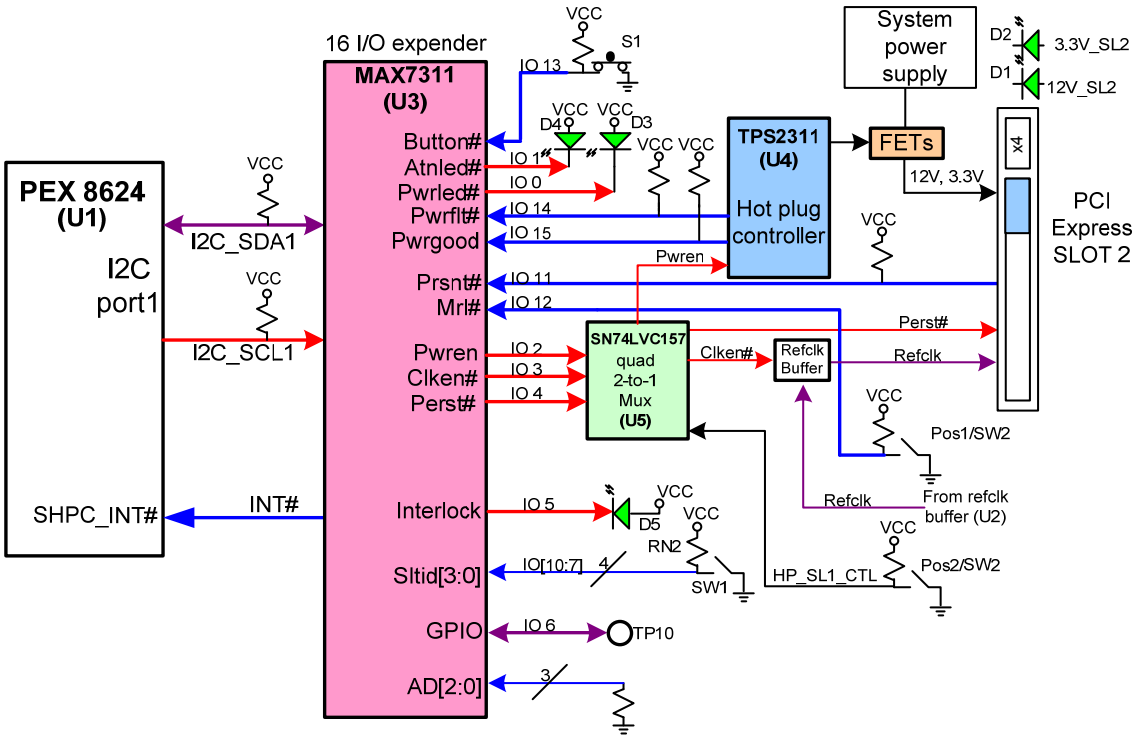

Figure 2-7. PEX 8624-AA RDK SERIAL HOT-PLUG Circuits

The serial hot-plug controller consists of an I/O expander (MAX 7311 (U3)), a dual hot–swap power controller (TPS2311 (U4)), a quad 2-to-1 multiplexer (SN74LVC157 (U5)), two power MOSFET IRF7470 (Q1 and Q2), LEDs, manual switch, dipswitches and resistors. The PEX 8624 master I^2C interface is designed for the specific control use of the serial hot-plug controller. The master I^2C interface connected to the I/O expander and the interrupt output from the I/O expander connects to the SERIAL HOT-PLUGC_INT# of the PEX 8624. When power is applied to the PEX 8624, the master I^2C interface will scan the bus and attempts to detect the presence of the I/O expander. If an I/O expander is detected, the I^2C master will program it as a "remote parallel hot-plug controller" and assign an available serial hot-plug port to the I/O expander. (see Section 2.5.1, Figure 2-6 and Figure 2-7 for details).

The RDK also provides dipswitches for setting the SLTID [3:0], a test point for access the GPIO pin, and three pull-down resistors to set AD [2:0] of the I/O expander U3. The LEDs D1 and D2 are 12V and 3.3V power indicators when power reaches PCI Express connector SLOT 2.

2.6 Serial EEPROM

The PEX 8624-AA RDK contains an 8-pin DIP socket for a serial EEPROM (U17). The board is populated with a blank On Semi CAT25080LI-G 32-Kbit device. The CAT25080LI-G device can directly interface to the PEX8624. When programmed correctly, the serial EEPROM can be used to change the default configuration of the PEX 8624. A blank EEPROM results in the default register values set in the PEX 8624. Please refer to the Software Development Kit (SDK) documentation for additional information on how to program the serial EEPROM.

2.7 I^2C Interface

The PEX 8624 implements an I^2C slave interface (I^2C port 0), which allows an external I^2C master to read and write device registers through an out-of-band mechanism. The PEX 8624 I^2C interface is accessible via a 7-bit address, at data rates from 100 Kbps up to 3.4 Mbps. The RDK provides two cascaded 2x2, 0.1" pitch headers (JP5 and JP6), which interface to the PEX 8624's I^2C port. That allows for cascading multiple RDKs together using standard ribbon cable, and/or connecting to an I^2C master such as the Total Phase Aardvark I^2C controller. (See Section 3.6 for pin assignment of JP5 and JP6.)

2.8 Power Distribution

The PEX 8624-AA RDK has two sources of DC power. The first source is the card edge connector (P1). The x8 connector provides up to 2.1A at 12V and 3.0A at 3.3V from the PCI Express edge card connector it plugs in. The power from P1 is intended to power the PEX 8624, PCI Express connector SLOT 2, and the on-board electronic components. The dc/dc converter U12 converts 12V from the Card Edge connector to 1.0VCC to support the SerDes and core power of the PEX 8624. The LDO U13 converts 3.3V to 2.5VCC to support the I/O power of the PEX 8624.

The second source of power includes an ATX HD power connector J1, and a 5V to 3.3V step down dc/dc converter U11. Through controlled power MOSFETS, connector J1 provides 12VCC up to 5A to each of PCI Express Edge Card Connectors SLOT 1 and SLOT 2. The J1 also provides enough 5V power for the dc/dc converter U11 to generate 3.3VCC up to 3A for each of SLOT 1 and SLOT 2 (See Figure 2-8 for details).

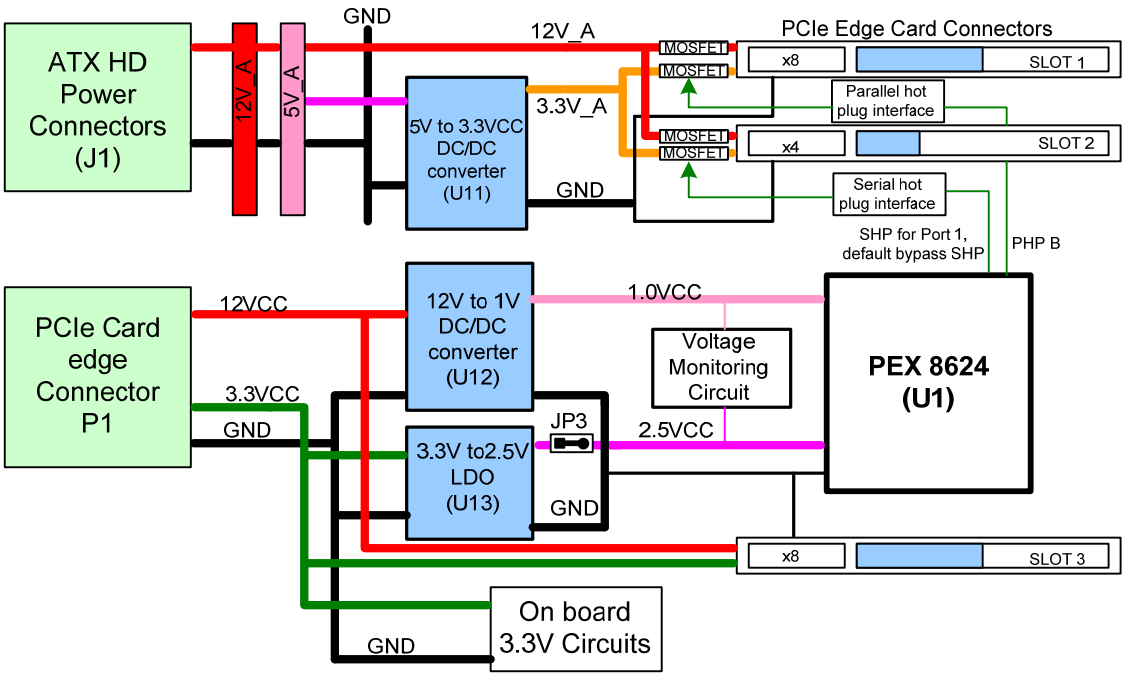

Figure 2-8. PEX 8624-AA RDK Power Subsystem

2.9 LED Indicators

The PEX 8624-AA RDK provides a number of LED indicators including power-on indication, PEX 8624 port link status indication, Hot-Plug LED indication, fatal error indication, event/error indication, and voltage level monitoring indications. Table 2-1 provides a quick explanation of the various board indicators.

Table 2-1. PEX 8624-AA RDK LED Indicator descriptions

Indicator Type	Locations	LED Functions
Slot Power LED/green color	D1	On: 12V at PCI Express connectors SLOT 2
	D2	On: 3.3V at PCI Express connectors SLOT 2
Slot Power LED/green color	D8	On: 12V at PCI Express connectors SLOT 1
	D9	On: 3.3V at PCI Express connectors SLOT 1
SERIAL HOT-PLUG LED/green color	D3	On: HP power LED output active at port 1
	D4	On: HP Attention LED output active at port 1

Indicator Type	Locations	LED Functions
	D5	On: HP interlock output active at port 1
PHP Attention LED/green color	D6	On: HP Attention LED output active at port 5
	D7	On: HP power LED output active at port 5
Slot Power LED/green color	D8	On: 12V at PCI Express connectors SLOT 1
	D9	On: 3.3V at PCI Express connectors SLOT 1
Voltage level monitoring / bi-color LED	D10	Monitor 2.5V to PEX 8624 (see Table 2-3 for details)
	D11	Monitor 1V to PEX 8624 (see Table 2-3 for details)
Slot 1-2 Power LED/green color	D12	On: 12V at ATX HD power connector J1
	D14	On: 5V at ATX HD power connector J1
	D16	On: 3.3V at dc/dc converter U11 output
Board Power LED/green color	D13	On: 12V at edge card connector P1
	D15	On: 3.3V at edge card connector P1
PEX 8624 Port Link Status LED (driven by PEX_PORT_GOOD pins) /green color	D19	Port 0 speed and link activity (see Table 2-2 for details)
	D20	Port 1 speed and link activity (see Table 2-2 for details)
	D18	Port 5 speed and link activity (see Table 2-2 for details)
	D17	Port 6 speed and link activity (see Table 2-2 for details)
	D21	Port 8 speed and link activity (see Table 2-2 for details)
	D22	Port 9 speed and link activity (see Table 2-2 for details)
INTA# of PEX 8624/green color	D23	On: event/error occurs
FATAL_ERR#/red color	D24	On: error(s) occurs (see PEX 8624-AA Data Book)

2.9.1 Port Link Status Indication (D17 – D22)

The PEX 8624-AA RDK provides up to six green color link status LEDs, D17 to D22, to indicate its port 0, 1, 5, 6, 8 and 9 link states. LED on, off, and three blinking patterns cover all five states of port link status. (See Table 2-2 for details)

Table 2-2. Port Link Status LED Functions

Port Link State	LED Pattern
Link down	off
Link up, 5Gbps, all lanes are up	on
Link up, 5Gbps, reduced lanes are up	Blinking: 0.5 second on, 0.5 second off
Link up, 2.5Gbps, all lanes are up	Blinking: 1.5 second on, 0.5 second off
Link up, 2.5Gbps, reduced lanes are up	Blinking: 0.5 second on, 1.5 second off

2.9.2 Fatal Error Indication (D24)

The PEX 8624 provides an output status pin (FATAL_ERR#) which reports the event of a PCI Express fatal error condition. The RDK connects this output to a red LED (D24) which is lit when a fatal error condition is detected. Examples of fatal error conditions are data link layer protocol errors, receiver overflow and malformed TLPs. The PCI Express Base specification provides a complete listing of fatal error conditions. The PEX 8624-AA Data Book also provides additional details on the assertion of FATAL_ERR#.

2.9.3 PEX_INTA Interrupt Indication (D23)

The PEX 8624 provides an output status pin (PEX_INTA#) for signaling various programmable events. The RDK connects this output to a green LED (D23) for this interrupt output. Please refer to the PEX 8624-AA Data Book for additional information on the programmable events for PEX_INTA#.

2.9.4 PEX 8624 Voltage Level Monitoring (D10 – D11)

The PEX 8624-AA RDK provides voltage level monitoring circuit to monitor the 1 volt and 2.5 volt power to the PEX 8624. The circuit contains an Intersil multiple voltage supervisory ISL6132, two bi-color LEDs, D10 and D11, and various value resistors. When the 1 volt or 2.5 volt is within the +/- 10% range the green LED will turn on. Otherwise the red LED will be on. (See Table 2-3 for details)

Table 2-3. Voltage Level Monitoring LED Functions

LED	Green LED on/ Red LED off	Green LED off/Red LED on
D8	1 volt to PEX 8624 within +/- 10% range	1 volt to PEX 8624 out of +/- 10% range
D9	2.5 volt to PEX 8624 within +/- 10% range	2.5 volt to PEX 8624 out of +/- 10% range

2.10 GPIO Pins

The PEX 8624 has fourteen GPIO pins. All GPIO pins are connected to mictor connectors (MC1 and MC2) to be used by external applications.

2.11 Reserved Pins

The PEX 8624 has 9 STRAP_RESERVED pins. They are factory use only and should be set to know logic states. Table 2-4 shows the list of these reserved pins and their connections in the RDK.

Table 2-4. Strap_Reserved Pin Connections

Name	Pin Location	Connections on PEX 8624-AA RDK
STRAP_RESERVED0	J4	Pull-down with a 1K ohm resistor
STRAP_RESERVED1	P2	Pull-down with a 1K ohm resistor
STRAP_RESERVED2	K5	Pull-up with a 4.7K ohm resistor
STRAP_RESERVED3	E2	Pull-down with a 1K ohm resistor
STRAP_RESERVED4	V12	Pull-down with a 1K ohm resistor
STRAP_RESERVED7	F3	Pull-up with a 4.7K ohm resistor
STRAP_RESERVED8	E12	Pull-down with a 1K ohm resistor
STRAP_RESERVED16	T13	Pull-down with a zero ohm resistor
STRAP_RESERVED17#	D18	Set DIP switch to OFF (logic ‘HIGH’)

3. On-Board Connectors, Switches, and Jumpers

3.1 DIP Switches

The PEX 8624-AA RDK contains nine user controllable DIP switches (SW1-SW9) for selecting the slot ID for the serial hot-plug, enable/disable Hot-Plug signals, enable/bypass the serial hot-plug and parallel hot-plug, upstream port select, port configuration, NT upstream port select, I^2C address settings and test mode settings. The dipswitches are presented following the orientations shown in Figure 3-1.

3.1.1 Slot ID Selection (SW1)

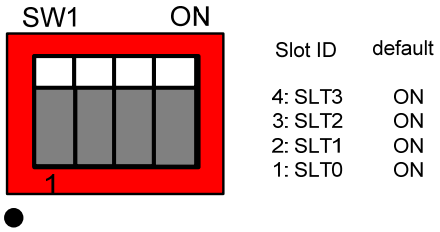

Figure 3-1. Switch SW1 Default Settings

Switch SW1 is used to set the slot ID for the PCI Express SLOT 2. Users can select one of 16 combinations.

3.1.2 Serial Hot-Plug Signal and Control (SW2)

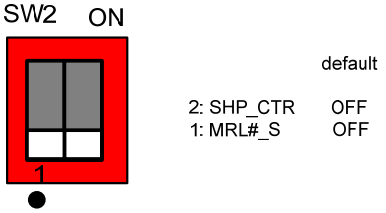

Figure 3-2. Switch SW2 Default Settings

Table 3-1. Switch SW2 Description

SW2 Functional Description	Switch Position Settings
Enable/bypass SERIAL HOT-PLUG outputs to generate power, RefClk and PERST#, to connector SLOT 2	Position 2 ON: enable SERIAL HOT-PLUG outputs to generate power, RefClk and PERST# to SLOT 2 OFF: bypass SERIAL HOT-PLUG and still provide power, RefClk and PERST# to SLOT 2
Enable/disable MRL#_S at Serial Hot-Plug	Position 1 ON: enable MRL#_S OFF: disable MRL#_S

3.1.3 Parallel Hot-Plug Signal and Control (SW3)

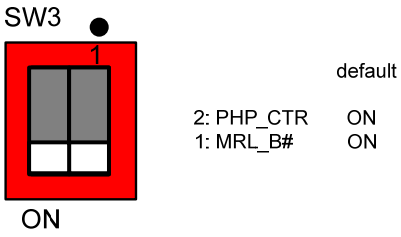

Figure 3-3. Switch SW3 Default Settings

Table 3-2. Switch SW3 Description

SW2 Functional Description	Switch Position Settings
Enable/bypass PHP outputs to generate power, RefClk and PERST#, to connector SLOT 1	Position 2 ON: enable SERIAL HOT-PLUG outputs to generate power, RefClk and PERST# to SLOT 1 OFF: bypass SERIAL HOT-PLUG and still provide power, RefClk and PERST# to SLOT 1
Enable/disable HP_MRL_B# at Parallel Hot-Plug	Position 1 ON: enable HP_MRL_B# OFF: disable HP_MRL_B#

3.1.4 DC/DC Converter and Mode Controls (SW4)

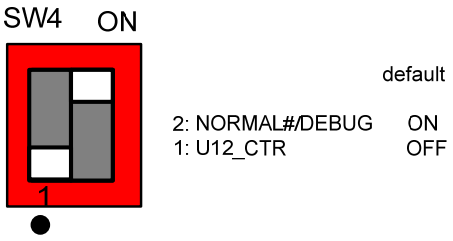

Figure 3-4. Switch SW4 Default Settings

Switch SW4 is for PLX internal test only. Changing the settings for SW4 is not recommended.

3.1.5 Upstream Port Select (SW5)

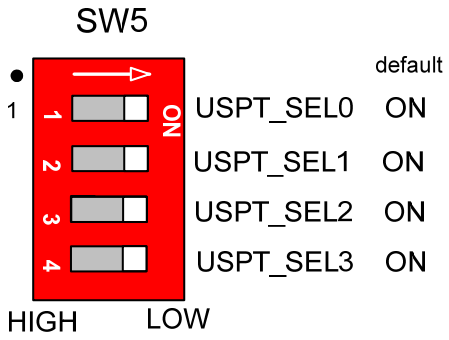

Figure 3-5. Switch SW5 Default Settings

Table 3-3. Switch SW5 Description

SW5 Functional Description	Switch Position Settings
Strap Upstream Port Select	1: USPT_SEL0 2: USPT_SEL1 3: USPT_SEL2 3: USPT_SEL3

UPSTREAM PORT	USPT_SEL[3:0]
0	ON,ON,ON,ON
1	ON,ON,ON,OFF
5	ON,OFF,ON,OFF
6	ON,OFF,OFF,ON
8	OFF,ON,ON,ON
9	OFF,ON,ON,OFF

3.1.6 Port Configuration and NT Upstream Port Select (SW6)

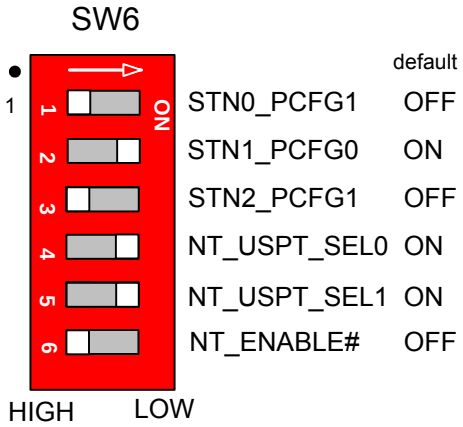

Figure 3-6. Switch SW6 Default Settings

Table 3-4. Switch SW6 Description

<table>
<tr><th>SW5 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>Strap Port Configuration
& NT Upstream Port Select</td><td>1: STN0_PCFG1
2: STN1_PCFG0
3: STN2_PCFG1
4: NT_USPT_SEL0
5: NT_USPT_SEL1
6: NT_ENABLE#
a. Strap Port Configuration
<table>
<tr><th>Strap Pin Name</th><th>Setting</th><th>Port Configurations</th></tr>
<tr><td rowspan="2">STN0_PCFG1</td><td>ON</td><td>X4X4</td></tr>
<tr><td>OFF</td><td>X8</td></tr>
<tr><td rowspan="2">STN1_PCFG0</td><td>ON</td><td>X8</td></tr>
<tr><td>OFF</td><td>X4X4</td></tr>
<tr><td rowspan="2">STN2_PCFG1</td><td>ON</td><td>X4X4</td></tr>
<tr><td>OFF</td><td>X8</td></tr>
</table>
b. NT Upstream Port Select
When NT Port Enable (NT_ENABLE# :ON), NT port select are:
<table>
<tr><th>Strap Pin Name</th><th>Setting</th><th>NT Port</th></tr>
<tr><td rowspan="2">NT_USPT_SEL[1:0]</td><td>ON, ON</td><td>Port 0</td></tr>
<tr><td>ON, OFF</td><td>Port 1</td></tr>
</table></td></tr>
</table>

3.1.7 Test Mode Select (SW7)

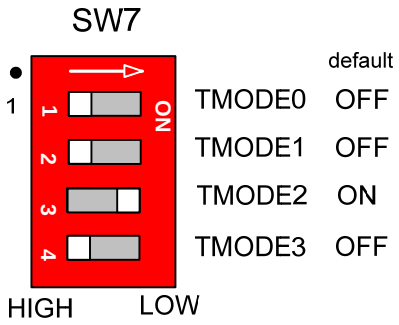

Figure 3-7. Switch SW7 Default Settings

Table 3-5. Switch SW7 Description

<table>
<tr><th>SW7 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>Strap Test Mode Select</td><td>1: TMODE0
2: TMODE1
3: TMODE2
3: TMODE3
<table>
<tr><th>TMODE[3:0]</th><th>Description of Functions</th></tr>
<tr><td>OFF,OFF,OFF,OFF</td><td>All PEX_PORT_GOOD pins became GPIO pins</td></tr>
<tr><td>OFF, ON,OFF,OFF</td><td>All PEX_PORT_GOOD pins are used for port link status outputs</td></tr>
<tr><td>OFF,OFF,ON,ON</td><td rowspan="2">PEX_PORT_GOOD and GOIP pins are programmed for different functions
(see the PEX 8624-AA Data Book for details)</td></tr>
<tr><td>OFF,OFF,ON,OFF</td></tr>
</table></td></tr>
</table>

3.1.8 I²C Address and Other Mode Select (SW8)

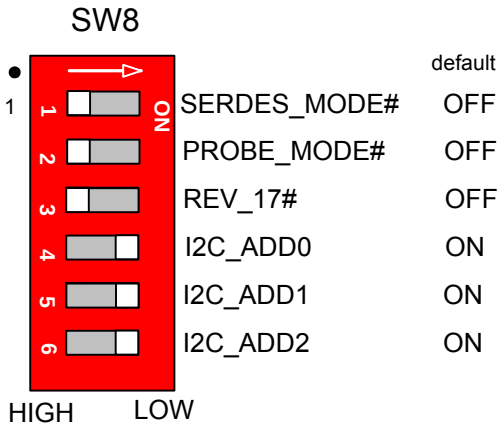

Figure 3-8. Switch SW8 Default Settings

Table 3-6. Switch SW8 Description

SW8 Functional Description	Switch Position Settings
Other Mode Settings a. SERDES_MODE# relates to STRAP_SERDES_MODE_EN# pin b. PROBE_MODE# relates to STRAP_PROBE_MODE# pin c. REV_17# relates to STRAP_RESERVED17# pin	1: SERSES_MODE# ON: For PLX use only OFF: For normal operation 2: PROBE_MODE# ON: For PLX use only OFF: For normal operation 3: REV_17# ON: For PLX use only OFF: For normal operation

<table>
<tr><th>SW8 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>PEX 8624 I²C Address bits[2:0].
Default setting is 000b.</td><td>4: I2C_ADDR[0]
5: I2C_ADDR[1]
6: I2C_ADDR[2]
<table><tr><th>I2C_ADD[2:0]</th><th>PEX 8624 I²C Slave Address</th></tr><tr><td>ON,ON,ON</td><td>68h</td></tr><tr><td>ON,ON,OFF</td><td>69h</td></tr><tr><td>ON,OFF,ON</td><td>6Ah</td></tr><tr><td>ON,OFF,OFF</td><td>6Bh</td></tr><tr><td>OFF,ON,ON</td><td>6Ch</td></tr><tr><td>OFF,ON,OFF</td><td>6Dh</td></tr><tr><td>OFF,OFF,ON</td><td>6Eh</td></tr><tr><td>OFF,OFF,OFF</td><td>6Fh</td></tr></table></td></tr>
</table>

3.2 Push-Button Switches

3.2.1 Manual Reset# (S1)

The PEX 8624-AA RDK provides a manual switch (S1) for manual PERST# capability. Note that manual PERST# will only apply warm reset to the PEX 8624 as well as SLOT 1 to SLOT 3.

3.2.2 Serial Hot-Plug Controller Attention Button (S2)

The PEX 8624-AA RDK provides a manual switch S2 for the attention button to the serial hot-plug circuit. When pushed and released, the switch generates an active low pulse to the Attention Button Input of the serial hot-plug controller.

3.2.3 Parallel Hot-Plug Controller Attention Button (S3)

The PEX 8624-AA RDK provides a manual switch S3 for attention button to the parallel hot-plug circuit. When pushed and released, the switch generates an active low pulse to the Attention Button Input of parallel hot-plug controller.

3.3 Midbus probe footprints (JP1 – JP2)

The PEX 8624-AA RDK provides two strategically placed midbus probe footprints. Each footprint provides 16 channels and each can support eight PCI Express lanes. The midbus footprints are based on Agilent's Soft Touch Midbus Probe, as shown in Figure 3-9, and can be used with Agilent, LeCroy as well as Tektronix retention mechanism. Table 3-7 below shows the signal names of x8 PCI Express midbus probe footprint and Table 3-8 shows the PCI Express lanes of the PEX 8624 and their midbus probe footprints.

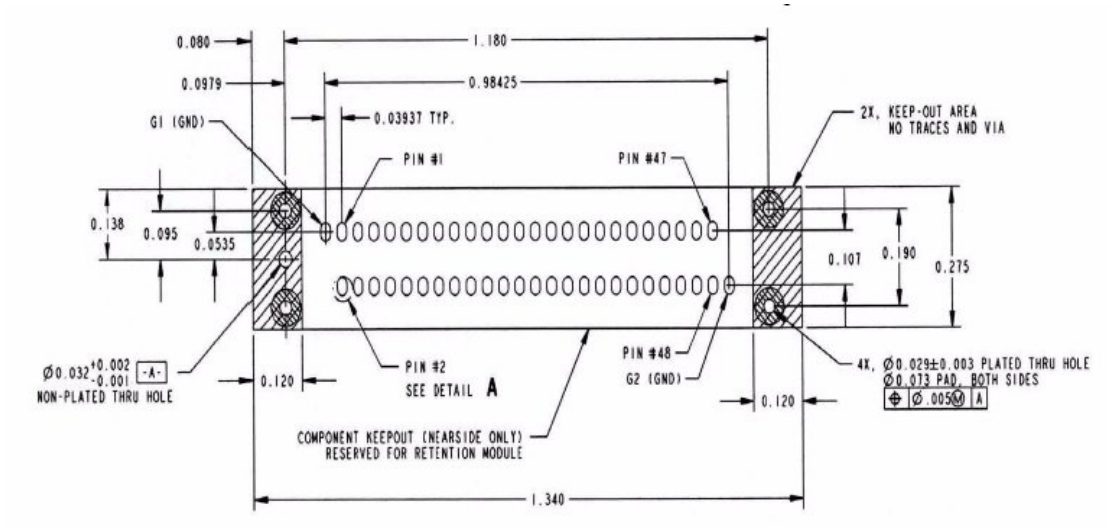

Figure 3-9. Midbus 2.0 footprint Dimensions, pin numbering and specification
(Copied from Agilent's document)

Table 3-7. Signal Names of x8 PCI Express Midbus probe footprint

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p-Upstream
4	C0p-Downstream	3	C0n-Upstream
6	C0n-Downstream	5	GND
8	GND	7	C1p-Upstream
10	C1p-Downstream	9	C1n-Upstream
12	C1n-Downstream	11	GND
14	GND	13	C2p-Upstream
16	C2p-Downstream	15	C2n-Upstream
18	C2n-Downstream	17	GND
20	GND	19	C3p-Upstream
22	C3p-Downstream	21	C3n-Upstream
24	C3n-Downstream	23	GND
26	GND	25	C4p-Upstream
28	C4p-Downstream	27	C4n-Upstream
30	C4n-Downstream	29	GND
32	GND	31	C5p-Upstream
34	C5p-Downstream	33	C5n-Upstream
36	C5n-Downstream	35	GND
38	GND	37	C6p-Upstream
40	C6p-Downstream	39	C6n-Upstream
42	C6n-Downstream	41	GND

Pin #	Signal Name	Pin #	Signal Name
44	GND	43	C7p-Upstream
46	C7p-Downstream	45	C7n-Upstream
48	C7n-Downstream	47	
G2	GND		

Table 3-8. Midbus probe footprints VS. Lanes of PEX 8624

Midbus Probe Footprint	Lanes of PEX 8624
JP1	Lane 0 – Lane 7
JP2	Lane 24 – Lane 31

3.4 2.5V Header (JP3)

This 2-pin header provides the mechanism for 2.5 volt measurement, which is for PLX use only. For regular RDKs, no header will be assembled and instead a wire will be used to connect pin 1-2 of JP7.

3.5 JTAG Header (JP4)

The 2x5 header JP4 provides a direct connection to the PEX 8624 JTAG interface. The 10-pin connector is designed to allow a direct interface to 3rd party JTAG controllers, such as the Corelis USB-1149.1/E controller. The pin assignment for the JTAG header (JP4) is listed at Table 3-9.

Table 3-9. Pin assignment of JP4

Pin Number	Signal Name
1	JTAG_TRST
3	JTAG_TDI
5	JTAG_TDO
7	JTAG_TMS
9	JTAG_TCK
2,4,6,8,10	GND

3.6 I²C Port (JP5 – JP6)

(See Section 2.7 for details)

Table 3-10. Pin assignment of JP5 and JP6

Pin Number	Signal Name
1	I2C_SCL
2	GND
3	I2C_SDA
4	NC

3.7 ATX HD Power Connector (J1)

(See Section 2.8 for details)

Table 3-11. Pin assignment of J1

Pin Number	Signal Name
1	+12VDC
2	COM (GND)
3	COM (GND)
4	+5VCC

3.8 Reference Clock Header (J2)

(See Section 2.3 for details)

Table 3-12. Pin assignment of J2

Pin Number	Signal Name
1	RefClkp (+)
2	GND
3	RefClkn (-)

3.9 Probe Mode Input Header (J3)

This is for PLX use only.

Table 3-13. Pin assignment of J3

Pin Number	Signal Name In Schematics
1	GND
2	DB_SEL0_I
3	PWRFLT_B#_I
4	DB_SEL1_I
5	MRL_B#_I
6	PRSNT_B#_I
7	BUTTON_B#_I
8	GND
9	MRL_C#_I
10	BUTTON_C#_I
11	PWRFLT_C#_I
12	PRSNT_C#_I
13	GND
14	PWRGD_A_I
15	PWRGD_B_I
16	MRL_A#_I
17	BUTTON_A#_I
18	PWRFLT_A#_I
19	PRSMT_A#_I
20	GND

3.10 PLX Use Header (J4)

This is for PLX use only.

Table 3-14. Pin assignment of J4

Pin Number	Signal Name In Schematics
1	SPARE2_O
2	SPARE1_IO
3	STRAP_RESERVED16
4	GND

4. Bill of Materials/ Schematics

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
SURFACE MOUNT COMPONENTS							
1	1	PLX	PEX8624-AA50BC F	IC, PCI Express Gen2 switch, 24 lane and up to 6 ports	SMT 324-pin BGA,19x19mm, 1mm pitch	U1	
2	1	SpectraLinear	CY28400OXC-2	IC, 100MHz Differential Clock Buffer	SMT, 28-pin SSOP	U2	408-855-0555, fax:408-855-0550
3	1	Maxim	MAX7311AUG	IC, 2 wire interface 16-bit IO port expander with interupt and hot isertion protection	SMT, 24-pin TSSOP	U3	
4	2	TI	TPS2311IPW	IC, Dual-power Hot Plug Controller, active high enable,	SMT, 20-lead TSSOP	U4, U6	
5	2	TI	SN74LVC157APW	IC, quadruple 2-line to 1-line data selectors/multiplexers	SMT, 16-pin TSSOP	U5,U7	Mouser: pn: 595-SN74lvc157APW
6	1	Fairchild	NC7S08M5X	IC, Tiny Logic 2-input AND gate	SMT, 5-pin SOT-23	U8	
7	1	Maxim	MAX6420UK29-T	IC, Reset controller, Adj. reset timeout	SMT, SOT23-5	U9	
8	1	Intersil	ISL6132IR	IC, multiple voltage supervisory	SMT, 4mmx4mm QFN package	U10	
9	2	Belfuse	S7AH-08E1A0	IC, Non-iso DC/DC converter, 4.5-14V-to-0.8/3.63V @ 8A	SMT, 7-pin	U11-U12	-
10	1	Micrel	MIC37100-2.5BS	IC, LDO linear regulator, output: 2.5V@1A	SMT, SOT-223	U13	
11	2	TI	SN74CBTLV3245APWR	IC, low voltage 8-bit FET bus switch, 3.3V	SMT,20-pin TSSOP	U14-U15	Mouser: pn: 595-SNCBTLV3245APWR

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
12	1	TI	SN74CB3T3306 DCTR	IC, low voltage 2-bit FET bus switch, 3.3V	SMT, 8-pin SSOP	U16	Mouser pn: 595-SN74CB3T3306DCTR
13	3	ITTCANON	TDA02H0SK1	Dip Switch, 2-pos, half pitch	SMT, dual in line	SW2-SW4	CKN1362-ND
14	1	ITTCANON	TDA04H0SK1	Dip Switch, 4-pos, half pitch,	SMT, dual in line	SW1	CKN1364-ND
15	2	ITTCANON	SDA04H1SKD	Dip Switch, 4-pos, 1mm pitch	SMT, dual in line	SW5,SW7	CKN1288-ND
16	2	ITTCANON	SDA06H1SKD	Dip Switch, 6-pos, 1mm pitch	SMT, dual in line	SW6,SW8	CKN1290-ND
17	1	FCI	84517-101LF	Connector, MEG-Array receptacle, 10x20 pos, 4mm	SMT,200 pos, 1.27mm pitch	CM1	
18	4	International Rectifier	IRF7470	IC, N-Channel MOSFET	SMT, 8-pin, SO-8	Q1-Q4	
19	21	Chicago Miniature Lamp	CMDA5CG7D1Z	LED, green, Vf=2.1V, 20mA,	SMT 0805	D1-D9,D12-D23	
20	2	Chicago Miniature	CMD15-22SRUGC	LED, bi-color LED, green-red	SMT, 4-pins	D10-D11	
21	1	Chicago Miniature Lamp	CMDA5DR7D1Z	LED, red, Vf=1.7V, 20mA,	SMT 0805	D24	
22	1	Molex	MOL75783-0036	Connector, right angle with shell 0.8mm pitch for mini-SAS,4x 26 CKT internal cable,	shell TH, SMT 26-pin connector	IP1	
23	1	Adex	CONN-PCIEXP-16X-SM	PCI Express x16 straddle-mount connector	SMT, 164-pin	SLOT1	
24	3	Omron	B3S1002	Switch, Push Button	SMT	S1-S3	
30	1	Kemet	C0603C102J5RACTU	Cap. Ceramic, 0.001uF, X7R, 50V 5%	SMT, 0603	C70	399-1083-2-ND
31	5	Kemet	C0603C103J5RAC	Cap, Ceramic, 0.01uF,50V 5%	SMT, 0603	C58-C60,C89-C90,	

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
32	2	Muurata	GRM033R60J223KE01D	Cap. Ceramic 0.022uF 6.3V X5R 10%	SMT 0201	C95-C96	490-3169-1-ND
33	2	Murata	GRM033R60J333KE01D	Cap. Ceramic 0.033uF 6.3V X5R 10%	SMT 0201	C97-C98	490-3170-1-ND
34	1	Murata	GRM033R71C102KD01D	Cap, Ceramic 0.001uF,16V X7R, 10%	SMT 0201	C99	490-1261-1-ND
35	5	Murata	GRM033R61A103KA01D	Cap, Ceramic, 0.01uF,X5R,10V 10%	SMT, 0201	C93-C94,C107-C109	490-3166-1-ND
36	5	Panasonic	ECJ-ZEB1A104M	Cap, Ceramic, 0.1uF, X5R, 10V, 20%	SMT, 0201	C100-C102,C110-C111	PCC2424CT-ND
37	54	Kemet	C0402C104K4RACTU	Cap. Ceramic, 0.1uF, X7R, 16V, 10%	SMT, 0402	C1-C8,C15-C46, C49-C56, C85-C88,C91-C92	
38	7	AVX	0603YC104KAT2A	Cap, Ceramic, 0.1uF, X7R, 16V, 10%	SMT, 0603	C62-C64,C66-68, C71	
39	8	AVX	0603YD105KAT2A	Cap, Ceramic, 1uF, X5R, 16V, 10%	SMT. 0603	C65,C69,C73,C75,C77,C79 ,C82,C83,	
40	12	AVX	1206YD106KAT2A	Cap, Ceramic, 10uF,X5R, 16V, 10%	SMT, 1206	C57,C61,C78,C81,C84, C103-C106, C112-C114	
41	10	AVX Corporation	TAJB226K020R	Cap. Tantalum, 22uF, 20V 20%	SMT, B-case	C9-C14,C47-C48,C72,C74,	
60	1	CTS	742C083102J	Chip Res. Array, 1K ohm, 5%, 4R isolated	SMT	RN4	
61	7	CTS	742C083472J	Chip Res. Array, 4.7K ohm, 5%, 4R isolated	SMT	RN1-RN3, RN5-RN8	
62	4	TTelectronics	LRF2512-LF-R020-F	Res. 2W, 0.02 ohm 1%	SMT, 2512	R32,R35,R41,R44	
63	1	Panasonic	ERJ-3GEYJ4R7V	Res. 1/10W, 4.7 ohm 5%	SMT, 0603	R4	

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
64	4	Panasonic	ERJ-3GEY0R00V	Res. 1/10W, zero ohm 5%	SMT, 0603	R56,R58,R86,R89	
65	8	Panasonic	ERJ-2GEJ330X	Res. 1/16W, 33 ohm 5%	SMT 0402	R7-R8,R11-R12,R15-R16, R19-R20,	
66	8	Panasonic	ERJ-2RKF49R9X	Res. 1/16W, 49.9 ohm 1%	SMT 0402	R9-R10,R13-R14,R17-R18, R21-R22,	
67	16	Panasonic	ERJ-6GEYJ151V	Res. 1/18W, 150 ohm 5%	SMT 0805	R26-R27,R31,R51, R53-R54, R79-R85, R98,R121-R122,	
68	1	Panasonic	ERJ-6GEYJ361V	Res. 1/8W, 360 ohm, 5%	SMT, 0805	R78	
69	1	Panasonic	ERJ-3EKF4750V	Res. 1/16W, 475 ohm 1%	SMT 0603	R6	
70	13	Panasonic	ERJ-3GEYJ102V	Res. 1/10W, 1 K ohm, 5%	SMT, 0603	R23-R25,R38, R47, R103-R104,R106-R107, R125-R126, R127-R128,	P1.0KGCT-ND
71	4	Panasonic	ERJ-6GEYJ122V	Res. 1/8W, 1.2K ohm, 5%	SMT 0805	R30,R50,R76-R77	
72	4	Panasonic	ERJ-3EKF2001V	Res. 1/10W, 2.0K ohm, 1%	SMT, 0603	R33-R34,R42-R43,	
73	32	Panasonic	ERJ-3GEYJ472V	Res. 1/10W, 4.7K ohm, 5%	SMT, 0603	R1-R3,R5,R29, R36-R37,R39-R40,R45-R46, R48-R49,R52, R66-R67,R72,R87-R88, R102,R105,R111-R116, R119-R120,R123,R129-R130	
74	1	Panasonic	ERJ-3GEYJ512V	Res. 1/10W, 5.1K ohm, 5%	SMT, 0603	R59	P5.1KGCT-ND
75	3	Panasonic	ERJ-3GEYJ103V	Res. 1/10W, 10K ohm, 5%	SMT 0603	R55,R117-R118	
76	1	Panasonic	ERJ-3GEYJ513V	Res. 1/10W, 51K ohm 5%	SMT, 0603	R57	
77	2	Yageo America	90C6031A1242FKHFT	Res. 1/10W, 12.4K ohm, 1%	SMT, 0603	R91,R94	
78	2	Yageo America	90C6031A1372FKHFT	Res. 1/10W, 13.7K ohm, 1%	SMT, 0603	R92,R96	

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
79	2	Yageo America	90C6031A2002 FKHFT	Res. 1/10W, 20K ohm, 1%	SMT, 0603	R90,R95	
80	2	Yageo America	9C06031A1003 FKHFT	Res. 1/10W,100K ohm, 1%	SMT, 0603	R93,R97	311-100KHCT-ND
81	1	Yageo America	9C06031A4640 FKHFT	Res. 1/10W, 464 ohm, 1%	SMT, 0603	R64	311-464HTR-ND
82	1	Yageo America	9C06031A1181 FKHFT	Res. 1/10W, 1.18K ohm, 1%	SMT, 0603	R61	311-1.18KHTR-ND
83	1	Yageo America	9C06031A2321 FKHFT	Res. 1/10W, 2.32K ohm, 1%	SMT, 0603	R65	311-2.32KHTR-ND
84	1	Yageo America	9C06031A3091 FKHFT	Res. 1/10W, 3.09K ohm, 1%	SMT, 0603	R60	311-3.09KHTR-ND
85	1	Yageo America	9C06031A5761 FKHFT	Res. 1/10W, 5.76K ohm, 1%	SMT, 0603	R62	311-5.769KHTR-ND
86	1	Yageo America	9C06031A7321 FKHFT	Res. 1/10W,7.32K ohm, 1%	SMT, 0603	R63	311-5.769KHTR-ND
87	1	Yageo America	9C06031A1301 FKHFT	Res. 1/10W,1.30K ohm, 1%	SMT, 0603	R74	311-1.30KHTR-ND
88	1	Yageo America	9C06031A3742 FKHFT	Res. 1/10W,37.4K ohm, 1%	SMT, 0603	R75	311-37.4KHCT-ND
89	3	Panasonic	9C06031A1431 FKHFT	Res. 1/16W, 1.43K ohm 1%	SMT, 0603	R108-R110	311-1.43KHCT-ND
90	1	Panasonic	ERJ-3GEYJ510V	Res. 1/10W, 51 ohm 5%	SMT, 0603	R28	P51GCT-ND
91	1	Panasonic	ERJ-3GEYJ150V	Res. 1/10W, 15 ohm 5%	SMT 0603	R124	P15GCT-ND
92	4	Panasonic	ERJ-6GEYJ391V	Res. 1/18W, 390 ohm 5%	SMT 0805	R68-R71	P391ACT-ND
THROUGH-HOLE COMPONENTS							

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
101	1	AMP	103240-5	Header, 2x5, 100mil pitch	2x5 th	JP4	A26528-05-ND
102	2	AMP	103240-2	Header, 2x2, 100 mil pitch	2x2 th	JP5-JP6	A26528-02-ND
103	1	Molex	53113-0410	Connector, 4-pin right angle	6 hole, PCB mount	J1	
104	1	AMP	103185-4	Header, 1x4, 100 mil pitch	1x4 th	J4	A26513-04-ND
105	2	Molex	87715-3302	Connector, PCI Express edge card connector, x16	164 pin, 4 row. TH	SLOT2-SLO3	
106	2	Vishay	94SP187X0020 FBP	Cap, solid aluminum, 180uF, 20V	F case	C76,C80	
107	1	Samtec	ICA-308-S-TT	Socket, 8-pin DIP, 300 mil,	8-pin DIP	U17	
MANUALLY INSERTED COMPONENTS							
200	1	On Semi	CAT25080LI-G	IC, 8Kb SPI serial EEPROM, 1.8-5.5V, up to 10MHz, 8-pin DIP	8-pin DIP	U17	
201	1	Keystone Electronics	9203	PCI bracket w/ two tabs			
202	1	Building Fasteners	PMSSS 440 0025 PH	Phillips Panhead screw, 4-40 thread, 0.25"			
203	1	The Olander Company Inc	FWN-4-312-032	Nylon washer,	#4x.312O.D.x.032THK	between the PCB and the tap of the PCI bracket	Phone: 800-538-1500, fax:800-355-6515
MISCELLANEOUS COMPONENTS							
300	1	TBD	TBD	PCB (90-0080-100-A)			
301	1	PLX	91-0096-000-A	Configuration Module #3, x8 to card edge connector P1	SMT, Plug	Plug to receptacle CM1 of PEX 8624RDK	
PARTS SHOULD NOT BE ASSEMBLED							

Item Number	Quantity	Manufacturer	Manufacturer's Part Number	Description	Package Type	Component Designator(s)	Distributor Part Number
13	0	ITTCANON	TDA02H0SK1	Dip Switch, 2-pos, half pitch	SMT, dual in line	SW9	
25	0	AMP	767054-1	Connector, 38-pin Mictor connector, vertical	SMT vertical	MC1-MC2	
73	0	Panasonic	ERJ-3GEYJ472V	Res. 1/10W, 4.7K ohm, 5%	SMT, 0603	R100,R101	
90	0	TBD			SMT 0603	R73,R99	
100	0	AMP/Tyco	103185-2	Header, 1x2 100 mil pitch	1x2 th	JP3	
108	0	Samtec	TMS-103-02-S-S	Header, micro terminal strip, 100mil	3-p through hole	J2	
109	0	AMP	1-103240-0	Header, 2x10, 100 mil pitch	2x10 th	J3	
110	0	Concord Electronics	09-9127-1-0210	Banana panel jack, black, insulated	through hole	BJ2	
111	0	Concord Electronics	09-9127-1-0212	Banana panel jack, red, insulated	through hole	BJ1,BJ3	
112	0	AMP/Tyco	382811-6	Jumper shunt, for 0.1" hdr.	2-pin	JP3(1-2)	

Customer Name	**PLX**	**PLX Part #**	**91-0080-102-B**
Product Name	**PEX8624RDK**	**Date**	**March 26, 2010**

REVISON HISTORY		
Revision	Date	Description
0	9/28/2007	First Released
1	1/2/2008	Changed R119&R120 to pull-up and C65&C69 to 1uF
2	1/8/2008	Modified Tx/Rx signals to IP1,changed package symbol for U3, added R129 and R130 at I2C master pins, and J2 to SLOT 2.
3	1/30/2008	Changed R1&R2 to pull-up to 3.3VCC. Renamed some net name on Page8.
4	3/26/2010	Changed U17 to SPI serial EEPROM

PEX8624RDK

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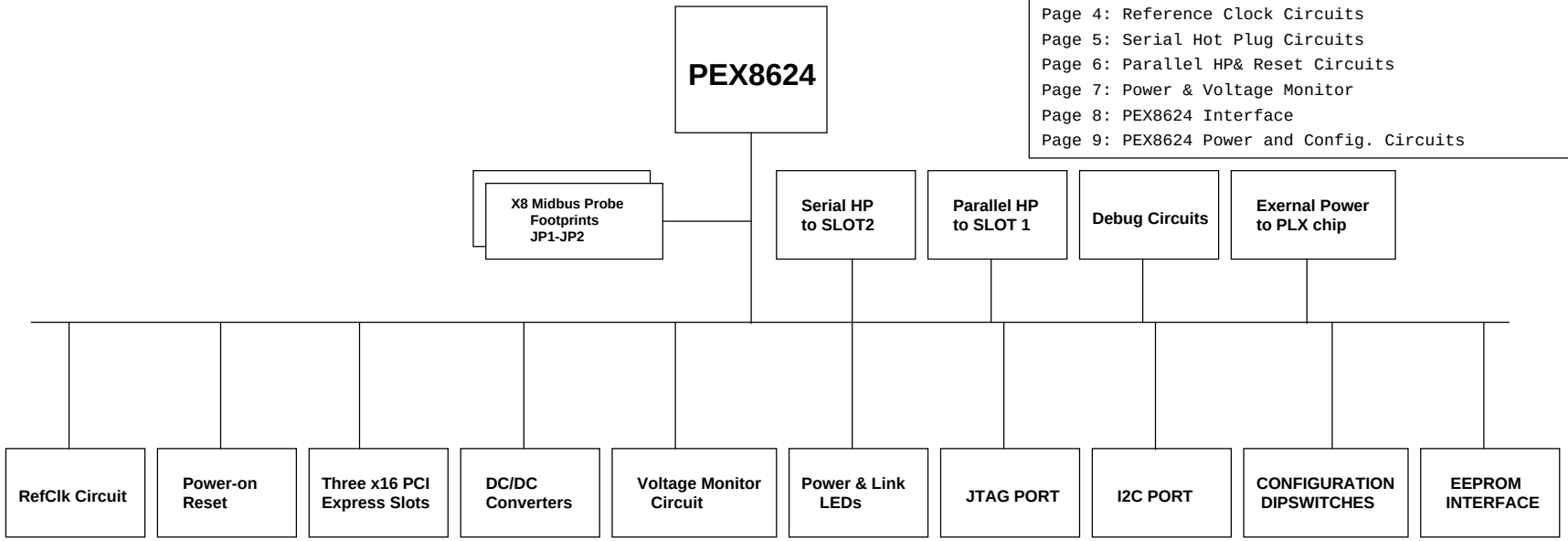

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Title: BLOCK DIAGRAM

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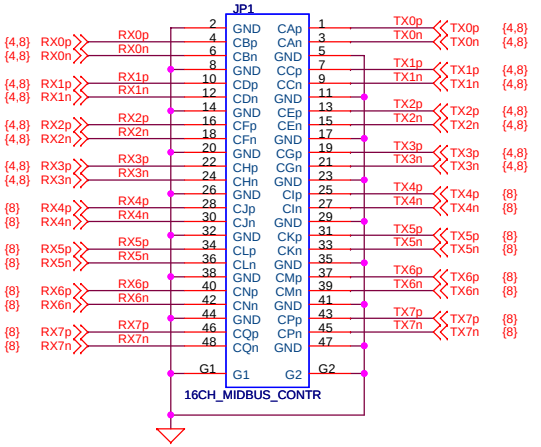
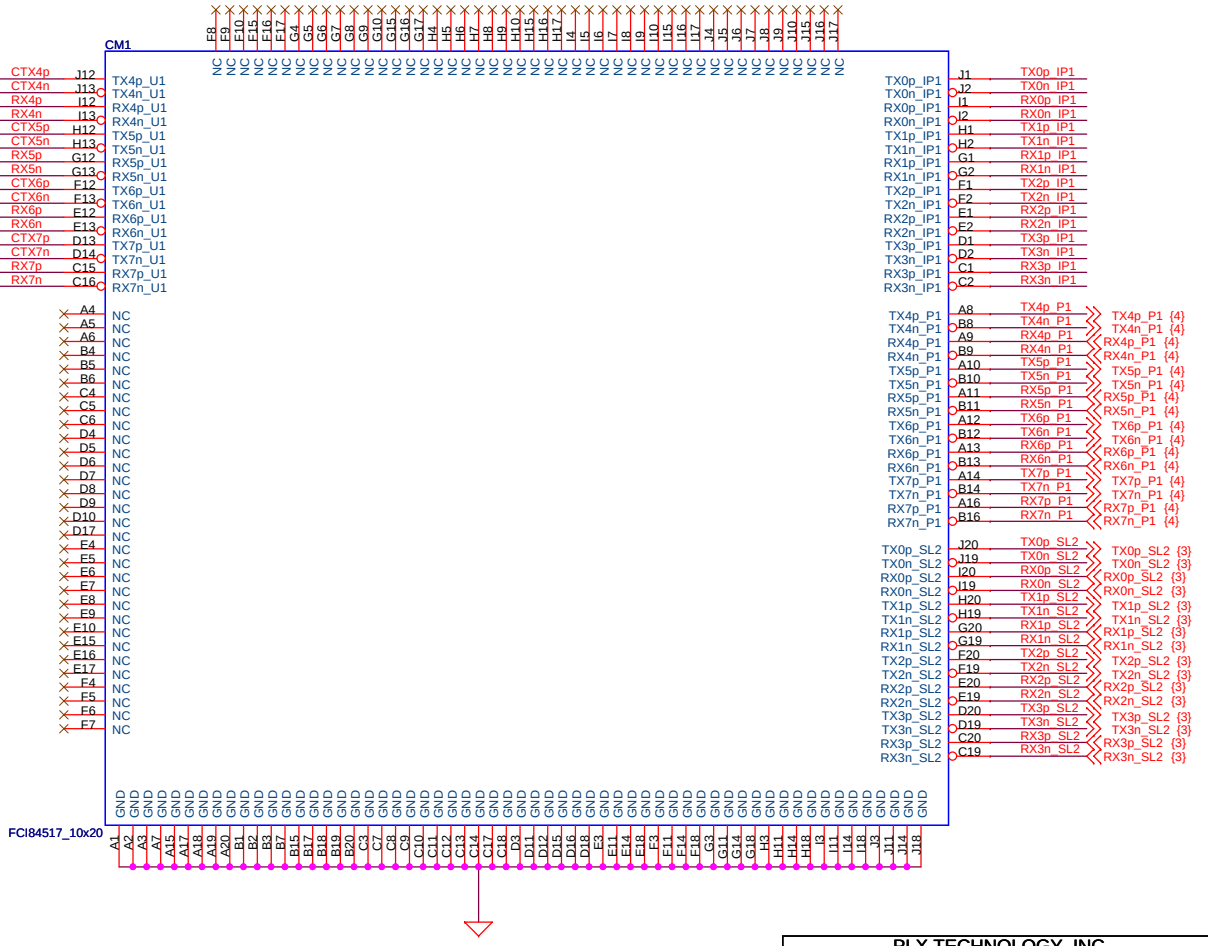
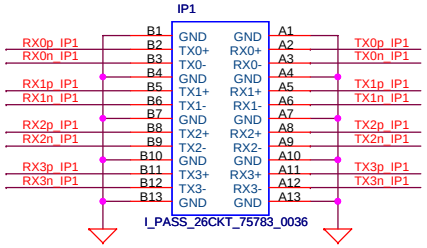
x8 MIDBUS PROBE FOOTPRINT FOR THE UPSTREAM PORT



CONFIGURATION MODULE RECEPTACLE



MINI SAS CONNECTOR



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Title: CM RECEPTACLE & MINI-SAS CNTR.		
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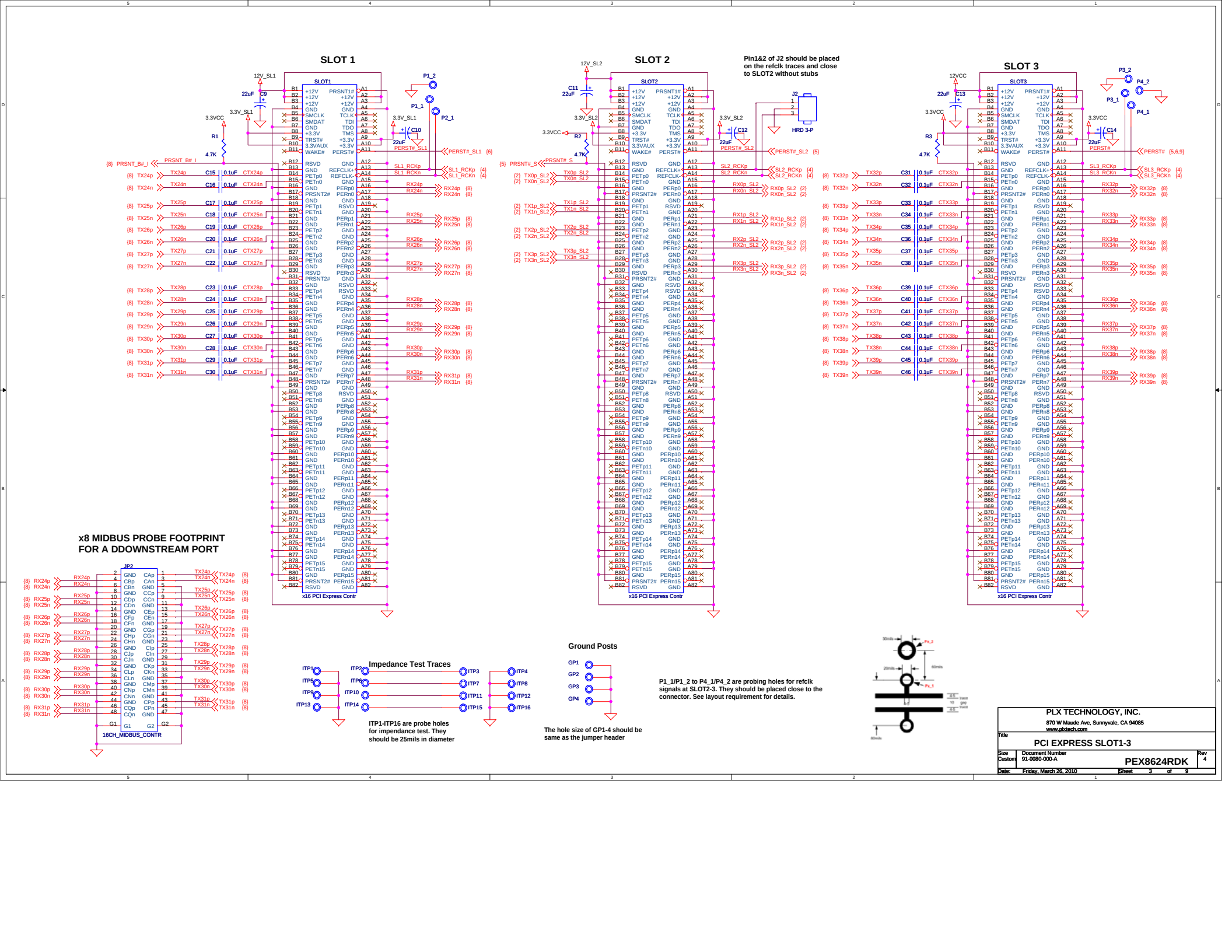
SLOT 1
SLOT 2
SLOT 3
Pin1&2 of J2 should be placed on the refclk traces and close to SLOT2 without stubs
x8 MIDBUS PROBE FOOTPRINT FOR A DDOWNSTREAM PORT
Impedance Test Traces
ITP1-ITP16 are probe holes for impendance test. They should be 25mils in diameter
Ground Posts
GP1
GP2
GP3
GP4
The hole size of GP1-4 should be same as the jumper header
P1_1/P1_2 to P4_1/P4_2 are probing holes for refclk signals at SLOT2-3. They should be placed close to the connector. See layout requirement for details.
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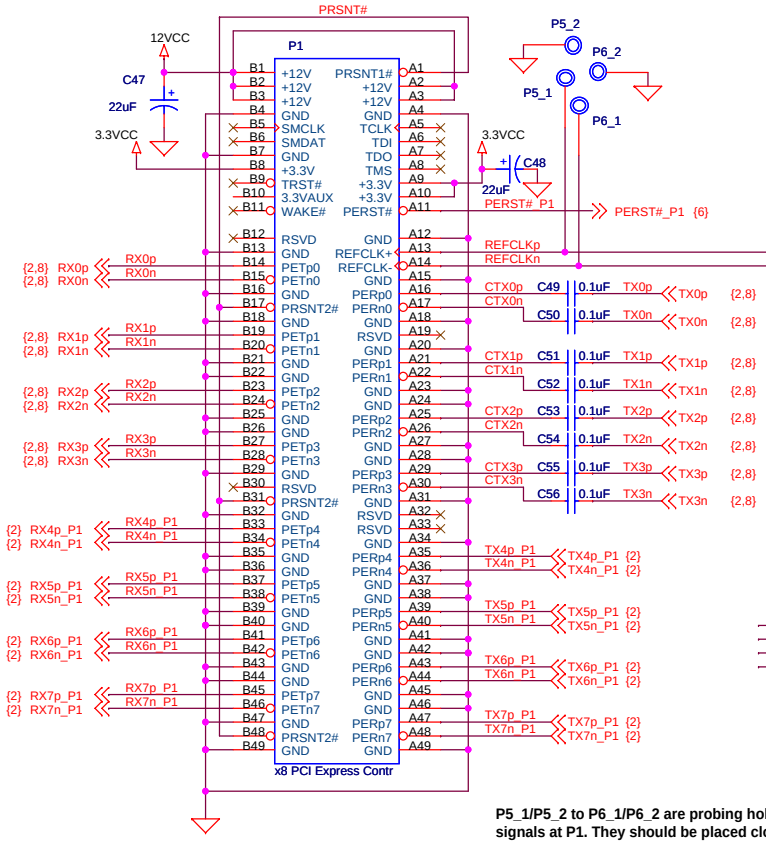
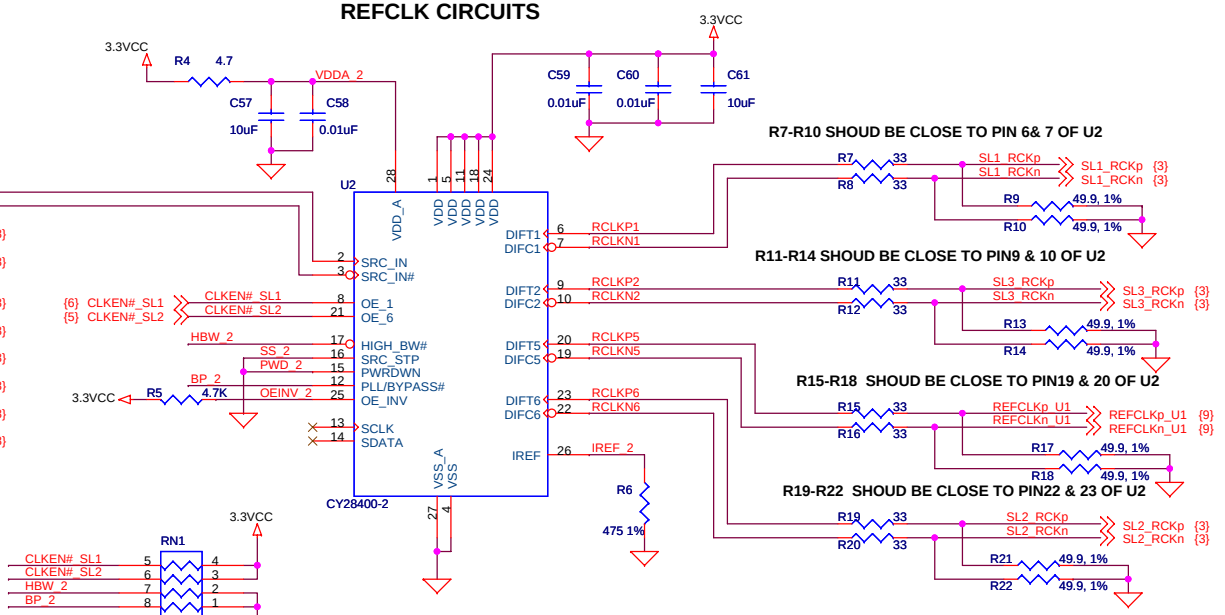
PCI EXPRESS SLOT1-3
PEX8624RDK
Friday, March 26, 2010

PCIE MALE CONNECTOR



REFCLK CIRCUITS



P5_1/P5_2 to P6_1/P6_2 are probing holes for refclk signals at P1. They should be placed close to the connector. See layout requirement on page 3 for details.

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Title: REFERENCE CLOCK CIRCUITS		
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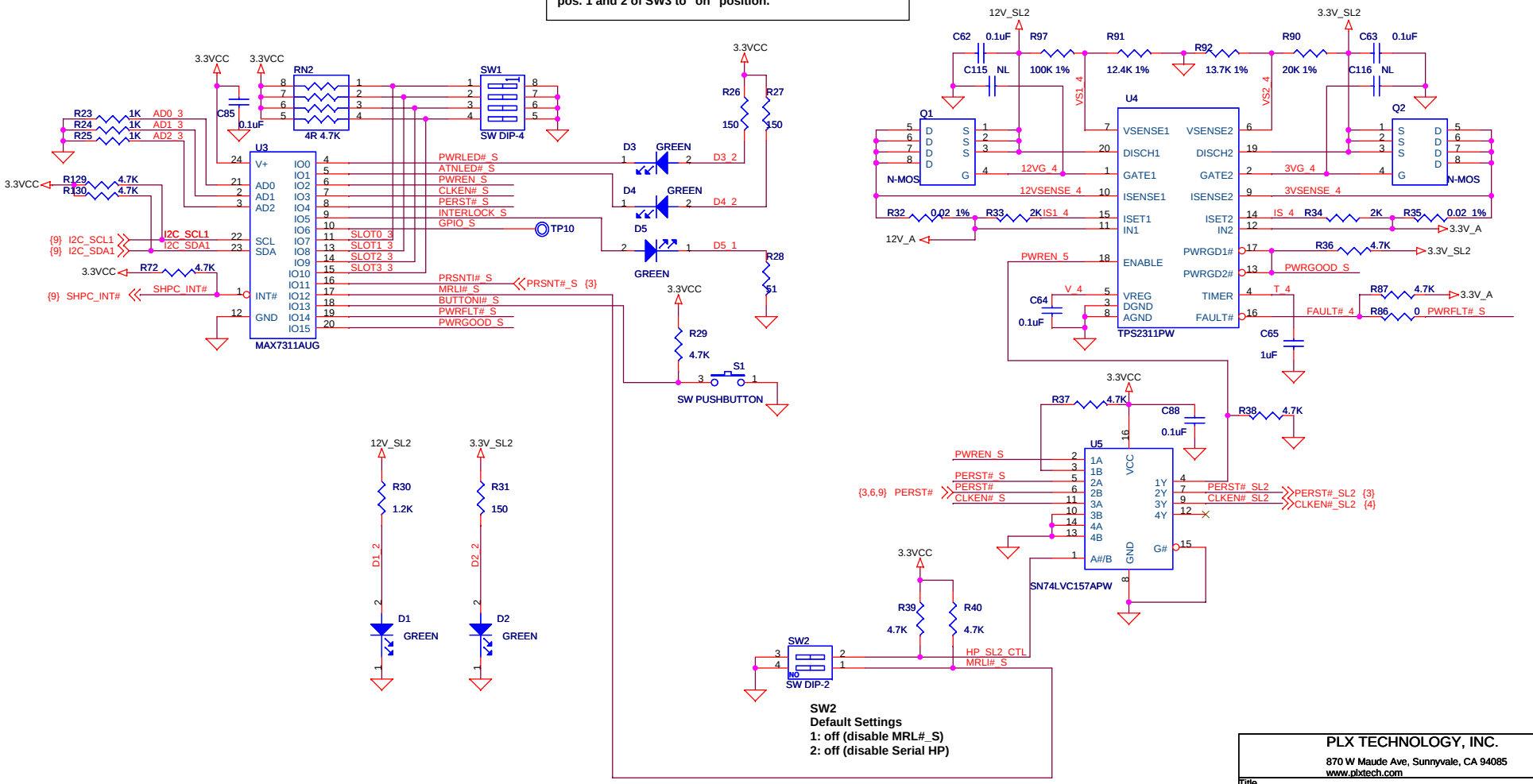
SERIAL HOT PLUG CIRCUIT FOR PORT 1 AT SLOT 2

To demonstrate the serial hot plug function of PEX 8624 requires the chip to boot with EEPROM and sets both pos. 1 and 2 of SW3 to "on" position.



SW2
Default Settings
1: off (disable MRL#_S)
2: off (disable Serial HP)

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Title: **SERIAL HOT PLUG CIRCUITS**

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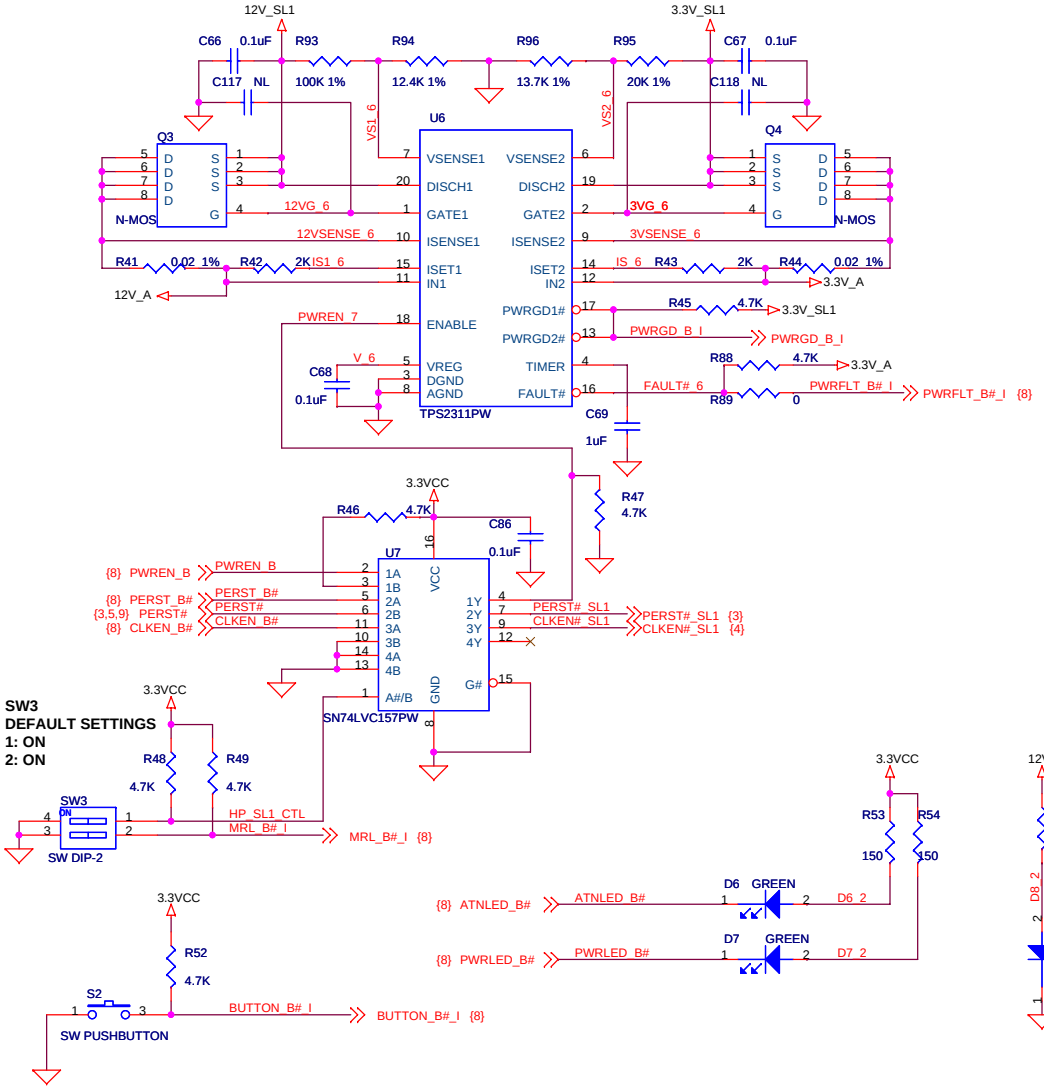
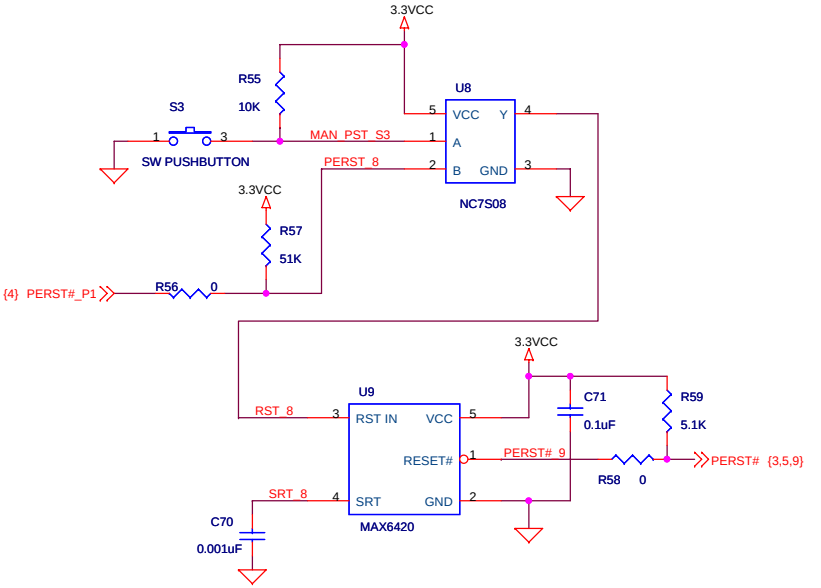
PARALLEL HOT PLUG CIRCUIT FOR SLOT 1



RESET CIRCUIT



C70 IS USED TO SET THE RESET TIMEOUT PERIOD FOR U9. A VALUE OF 0.001UF RESULTS IS APPROXIMATELY 3MS. SEE MANUFACTURER DATASHEET FOR DETAILS.

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Title: PARALLEL HP & RESET CIRCUIT		
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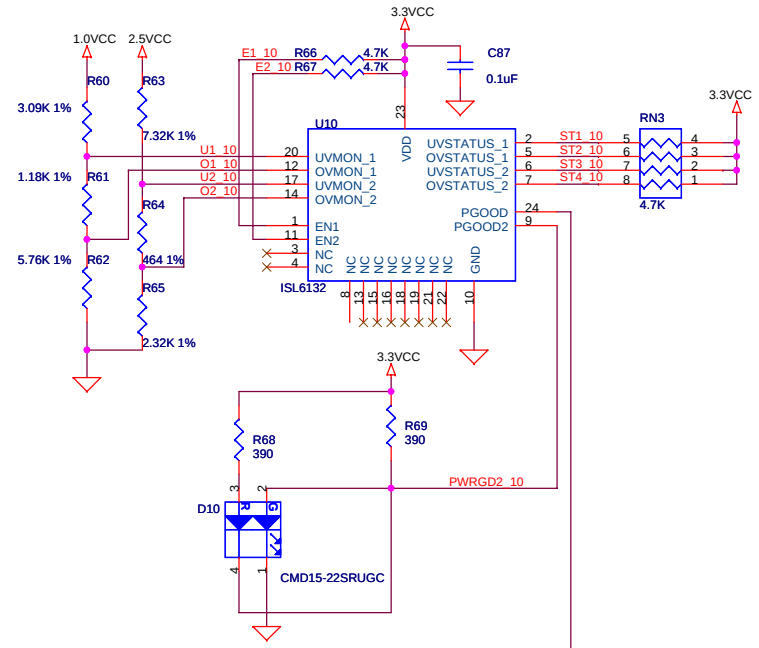
POWER FOR SLOT 1 & SLOT 2

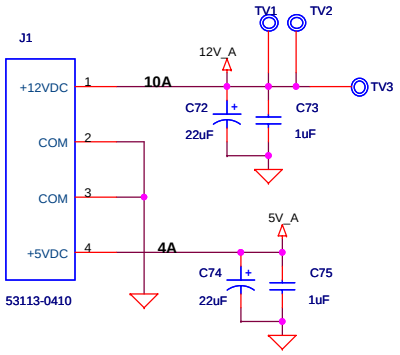
PEX8624 VOLTAGE MONITOR CIRCUIT



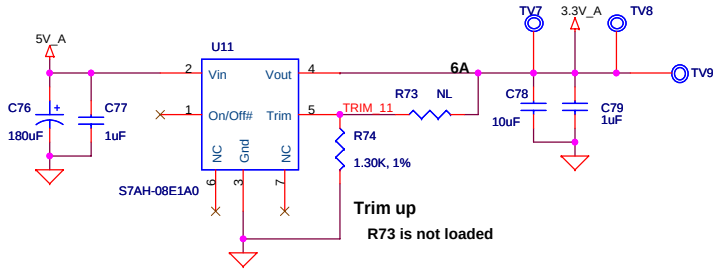
D10 is green: 2.5VCC is within the 10% range
D10 is red: 2.5VCC is out of range

D11 is green: 1.0VCC is within the 10% range
D11 is red: 1.0VCC is out of range

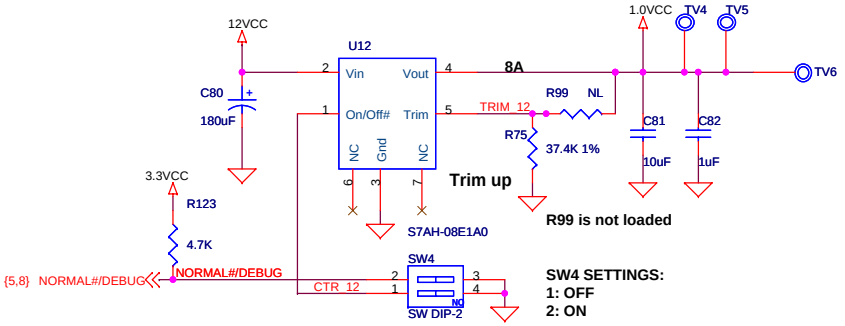
ATX HD POWER CONNECTOR



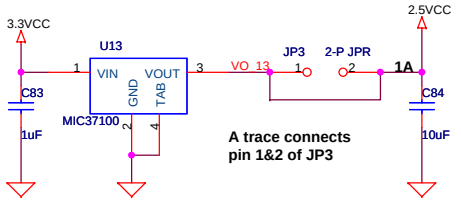
5V-TO-3.3V DC/DC CONVERTER



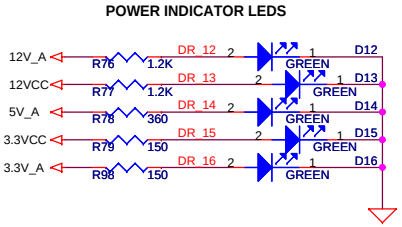
12V-TO-1.0V DC/DC CONVERTER

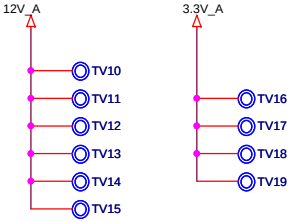


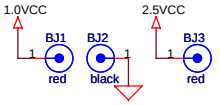
3.3V-TO-2.5V LDO



POWER INDICATOR LEDS







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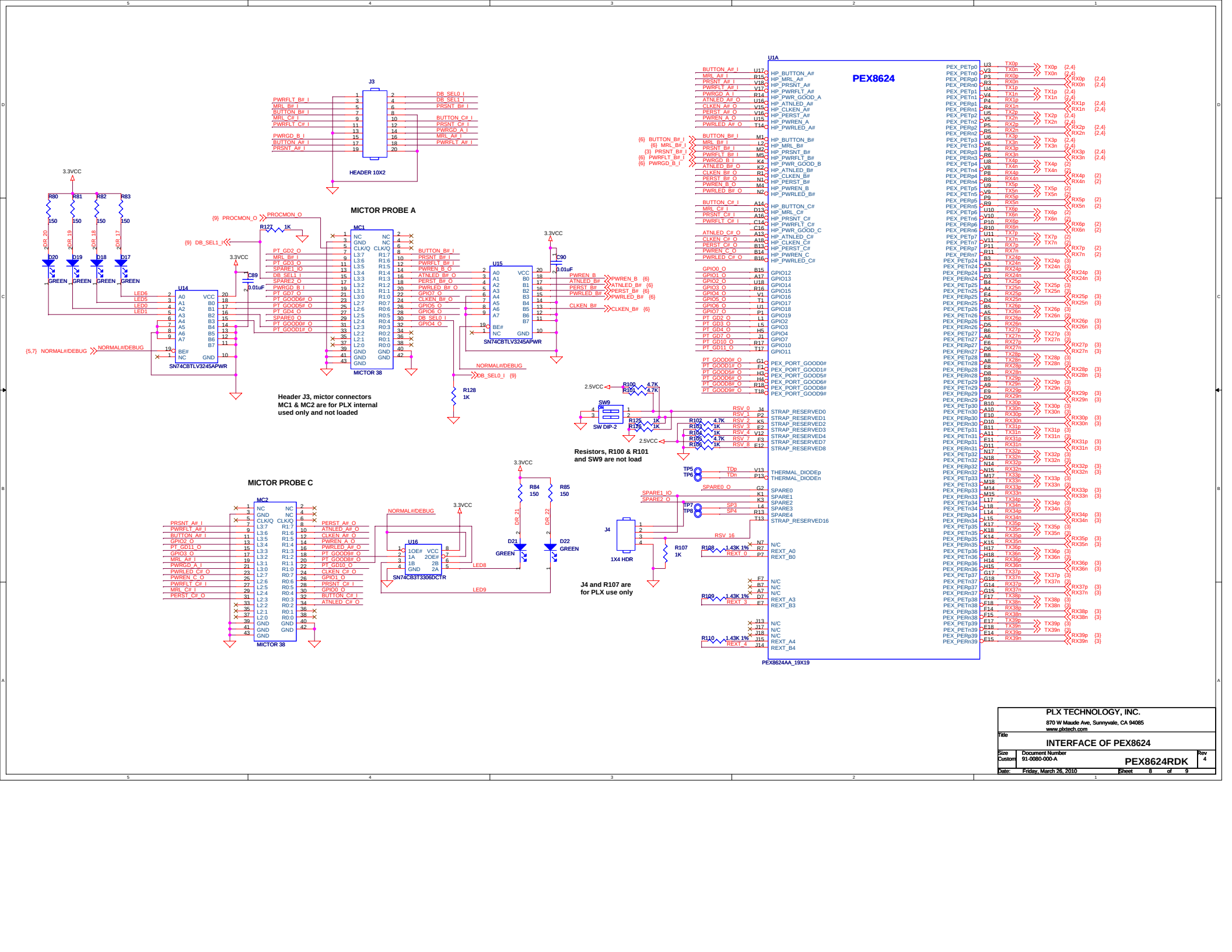

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Title: INTERFACE OF PEX8624

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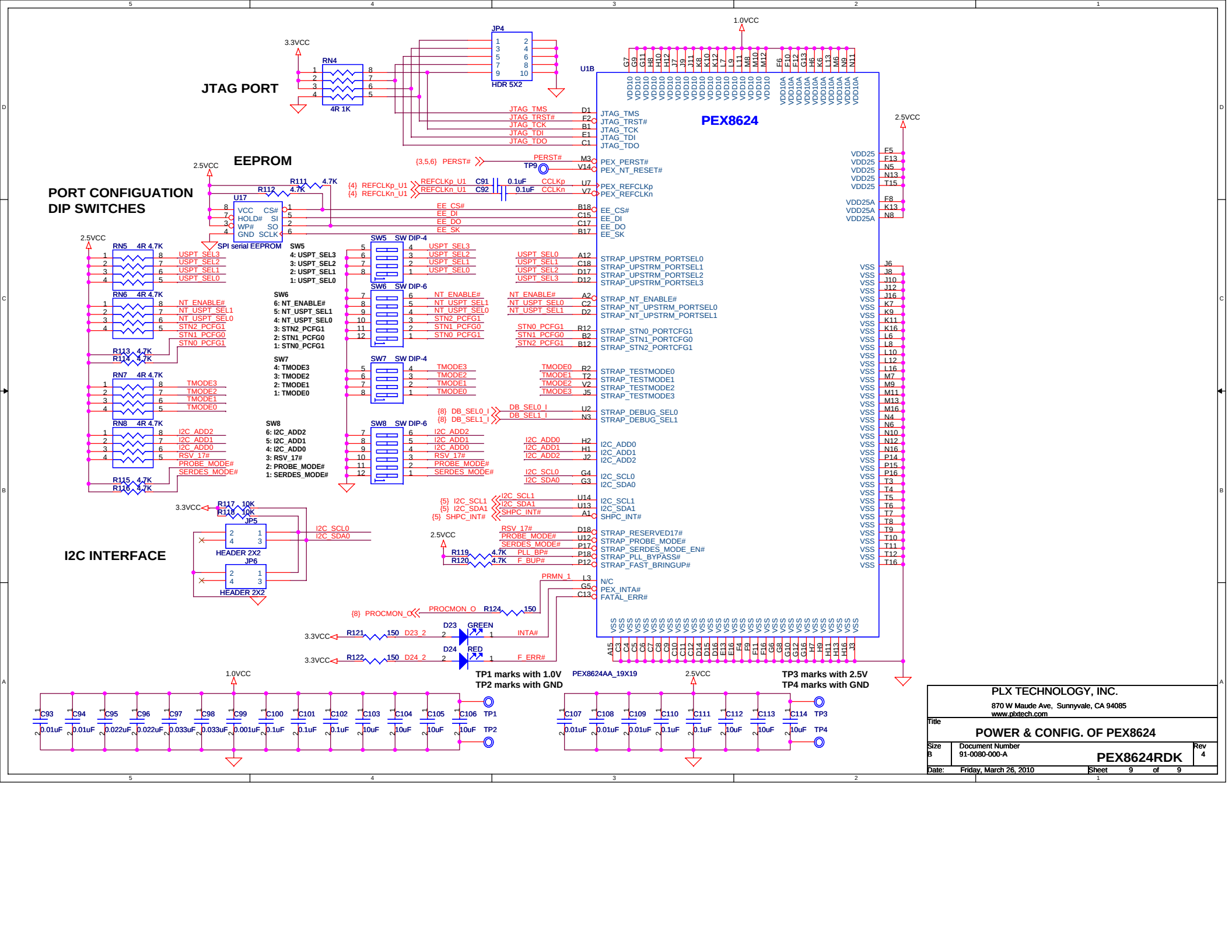

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Title: POWER & CONFIG. OF PEX8624

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