PEX 8608BA-AIC4U1D RDK

Hardware Reference Manual

Version 1.3

August 2010

Website: www.plxtech.com

Technical Support: www.plxtech.com/support

Order Number: 8608-RDK-HRM-1.3

August 6, 2010

PREFACE

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ABOUT THIS MANUAL

This document describes the PLX PEX 8608BA-AIC4U1D RDK, a Rapid Development Kit, from a hardware perspective. The contents of this document provide an accurate description of all aspects of this RDK board including a description of the major features and components, and details regarding the layout of the printed circuit board such as PCB mechanical outline, PCB stack-up, and component placement. This manual also includes complete schematics and bill of materials.

This Hardware Reference Manual is specific to the PEX 8608BA-AIC4U1D RDK. In the event of a discrepancy between this Hardware Reference Manual and the PEX 8608 Data Book, please be sure to follow the instructions and guidelines as stated in the PEX 8608 Data Book when designing your systems.

REVISION HISTORY

Date	Version	Comments
October 2008	1.0	Hardware Reference Manual initial release.
December 2008	1.1	Updated Schematics.
November 2009	1.2	Updated schematics and other miscellaneous edits
August 2010	1.3	Updated 2.7.3 to reflect support for SSC isolation

REFERENCES

- PLX Technology, Inc., www.plxtech.com
  - *PEX 8608 Data Book, Version 1.0*
- PLX Technology, Inc., www.plxtech.com
  - *PEX 8608 Quick Start Hardware Design Guide, Version 1.0*
- Agilent Technologies, www.agilent.com
  - *Agilent Soft Touch Midbus Probe User's Guide*
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
  - *PCI Express External Cabling Specification, Version 1.0*
  - *PCI Express CEM, Version 2.0*
  - *PCI Express Base Specification, Version 2.0*

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1. System Architecture

The PEX 8608BA-AIC4U1D RDK is a PLX Rapid Development Kit intended primarily for use by PLX customers for silicon evaluation and design reference of the PEX 8608. The form factor is based on the PCI Express Card Electromechanical specification. The board is designed to work by plugging into a PCI Express compliant motherboard via a x4 PCIe card edge connector. Two Configuration Modules are used at two locations to provide the hardwire routing flexibility needed to support the required port configurations that are used on this board. The PEX 8608BA-AIC4U1D RDK board supports Non-Transparent operation through a PCIe cable. Probe mode is available through two MICTOR connectors and one 2x10 pin header. Figure 1 below shows board layout and placement of major components for the PEX 8608BA-AIC4U1D RDK board.

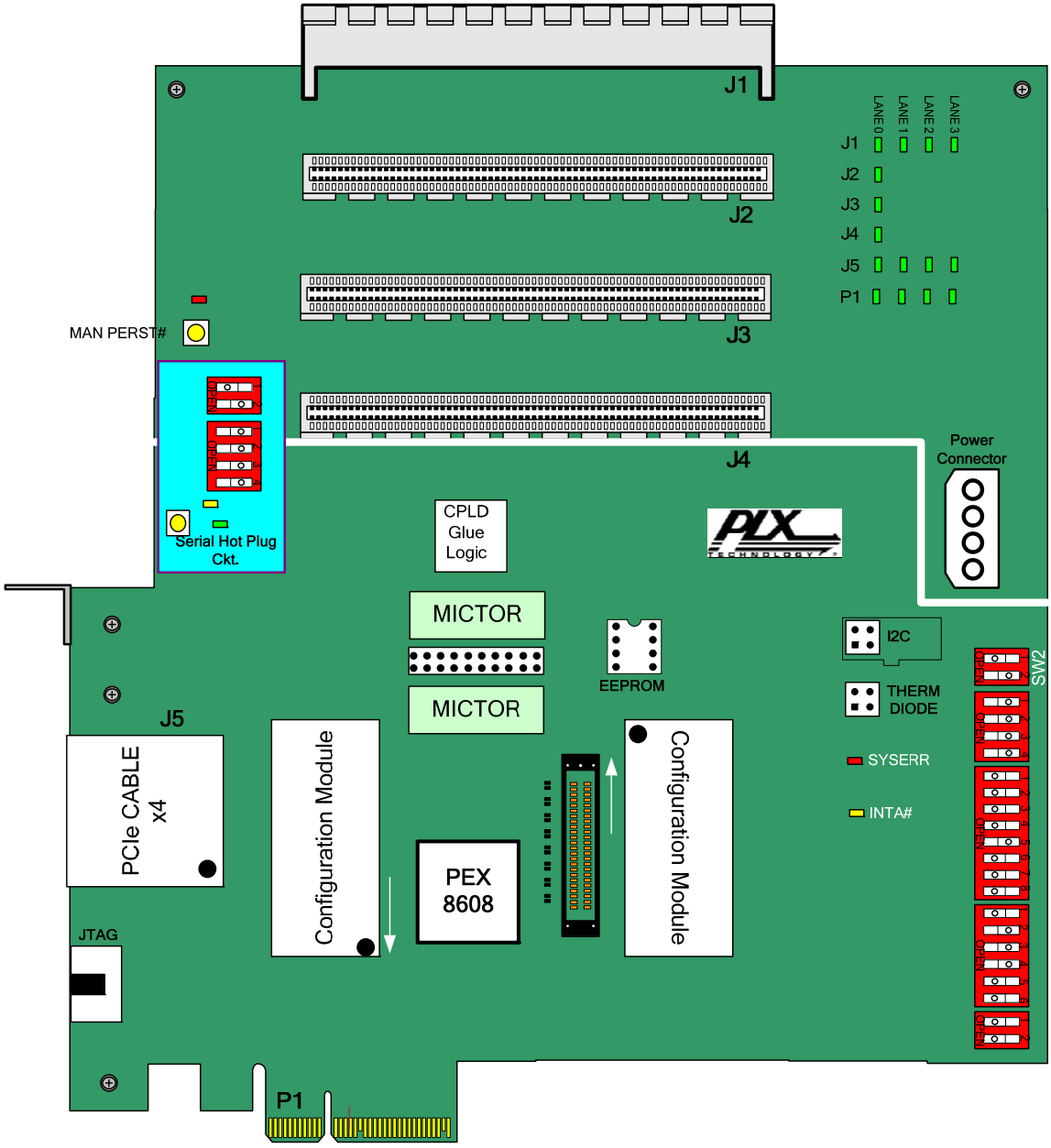


Figure 1. Component Placement for PEX 8608BA-AIC4U1D RDK

2. Hardware Architecture

2.1 PCI Express Port Configurations

The PEX 8608BA-AIC4U1D RDK supports the PEX 8608 device: an 8-lane, 8-port, non-blocking PCI Express switch, which can support both transparent and Non-Transparent modes of operation. Section 2.1.1, below, describes the port configurations that the PEX 8608BA-AIC4U1D RDK supports, and how these configurations are set-up.

The PEX 8608 device lane numbering is shown in Figure 2 below.

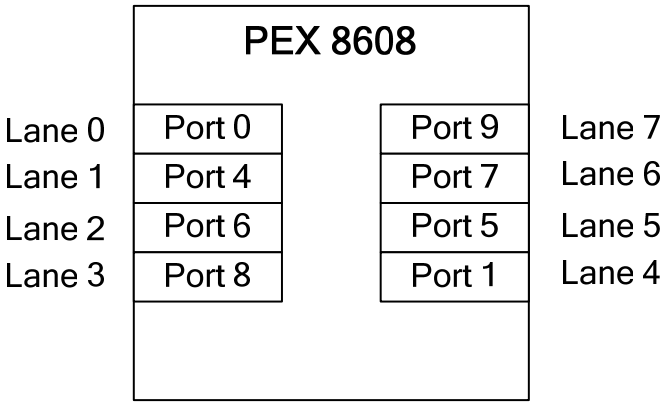


Figure 2. PEX 8608 Lane Numbering

Lanes 0 through 3 pass through an Agilent soft touch midbus probe footprint in order to monitor PCIe traffic. Refer to the *Agilent Soft Touch Midbus Probe User's Guide* for further details of the headers. Lane 0 is wired directly to card edge connector P1. Lanes 1 through 3 are routed to P1 or J2, J3, J4 by the Configuration Module on the right. Lanes 4 through 7 are routed to J1 or J5 by the Configuration Module on the left.

2.1.1 PEX 8608 AIC RDK Port Configurations

The PEX 8608BA-AIC4U1D RDK is designed to support the port configurations shown in Table 1 below.

Table 1. PEX 8608BA-AIC4U1D RDK Configurations Supported

Config	P1	J1	J2	J3	J4	J5
All x1	x1 – Port 0	x1x1x1x1 – Ports 1, 5, 7, 9	x1 – Port 4	x1 – Port 6	x1 – Port 8	
x4x1x1x1x1 **Default Configuration**	x4 – Port 0	x1x1x1x1 – Ports 1, 5, 7, 9				
x4x4	x4 – Port 0	x4 – Port 1				
x4-Cable x4	x4 – Port 0					x4 – Port 1

Table 2 below describes how the PEX 8608BA-AIC4U1D RDK is hardwire configured to support these four configuration modes, and points to the appropriate Figure showing how the routing occurs.

Table 2. PEX 8608BA-AIC4U1D RDK Hardware Configurations

Config	Left Config Module Used	Right Config Module Used	Number of Breakout Boards	SW2 Settings	Routing Figure
All x1	-0107	-0108	1	LL	Figure 3
x4x1x1x1x1 **Default Configuration**	-0107	-0107	1	LH	Figure 4
x4x4	-0107	-0107	0	HL	Figure 5
x4-Cable x4	-0108	-0107	0	HL	Figure 6

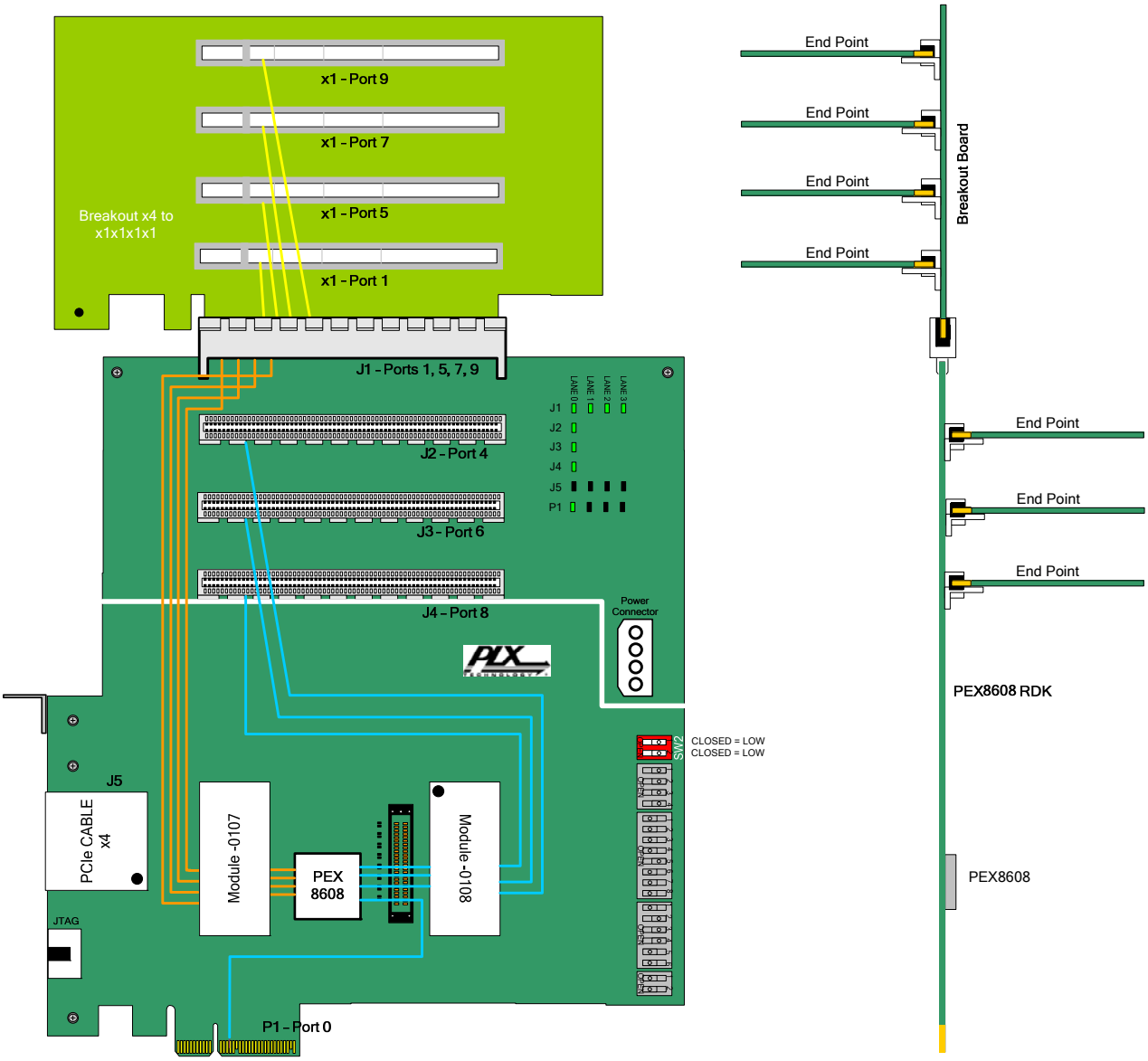


Figure 3. PEX 8608BA-AIC4U1D RDK – All x1 Configuration

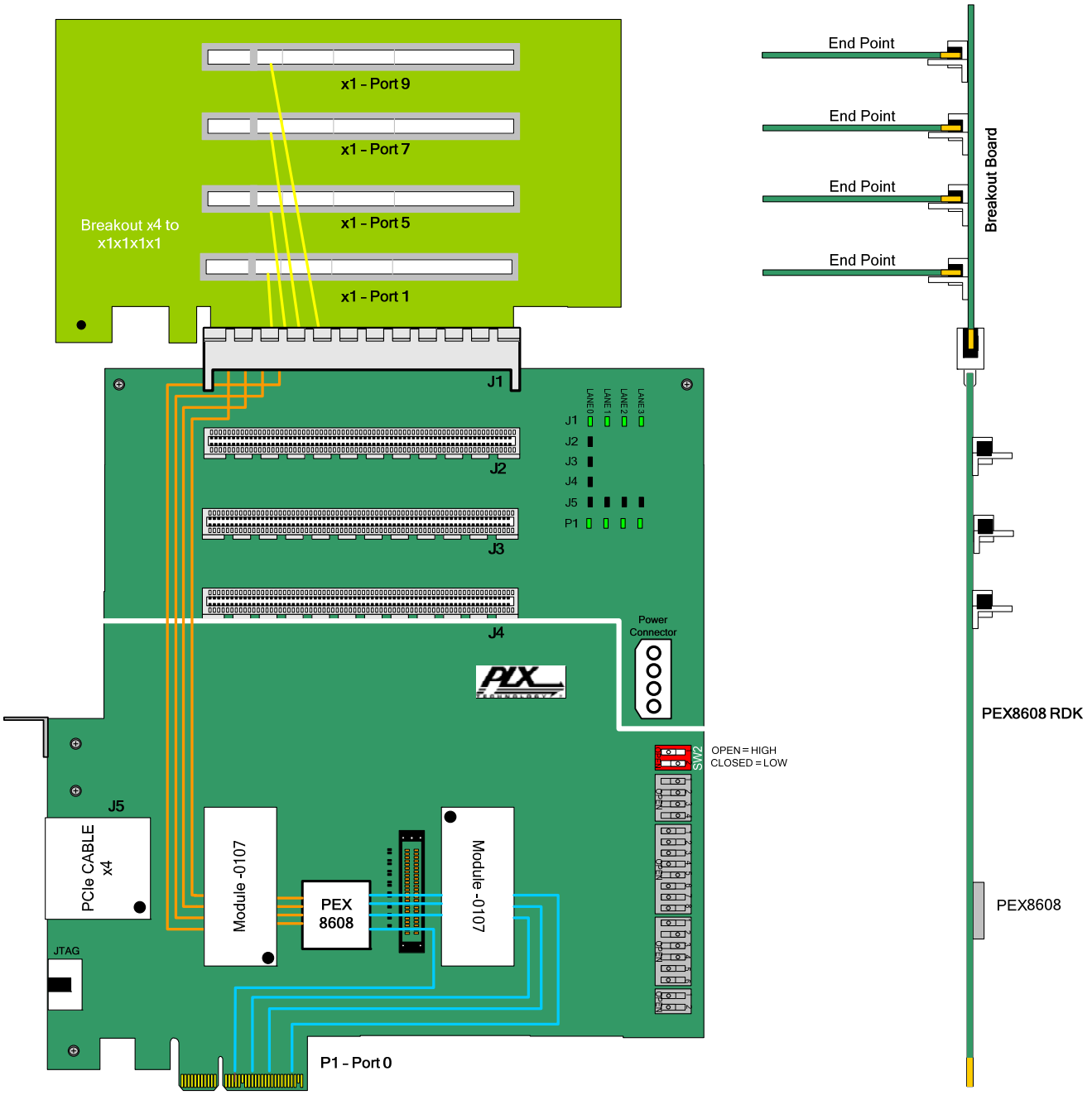


Figure 4. PEX 8608BA-AIC4U1D RDK – x4x1x1x1x1 Configuration

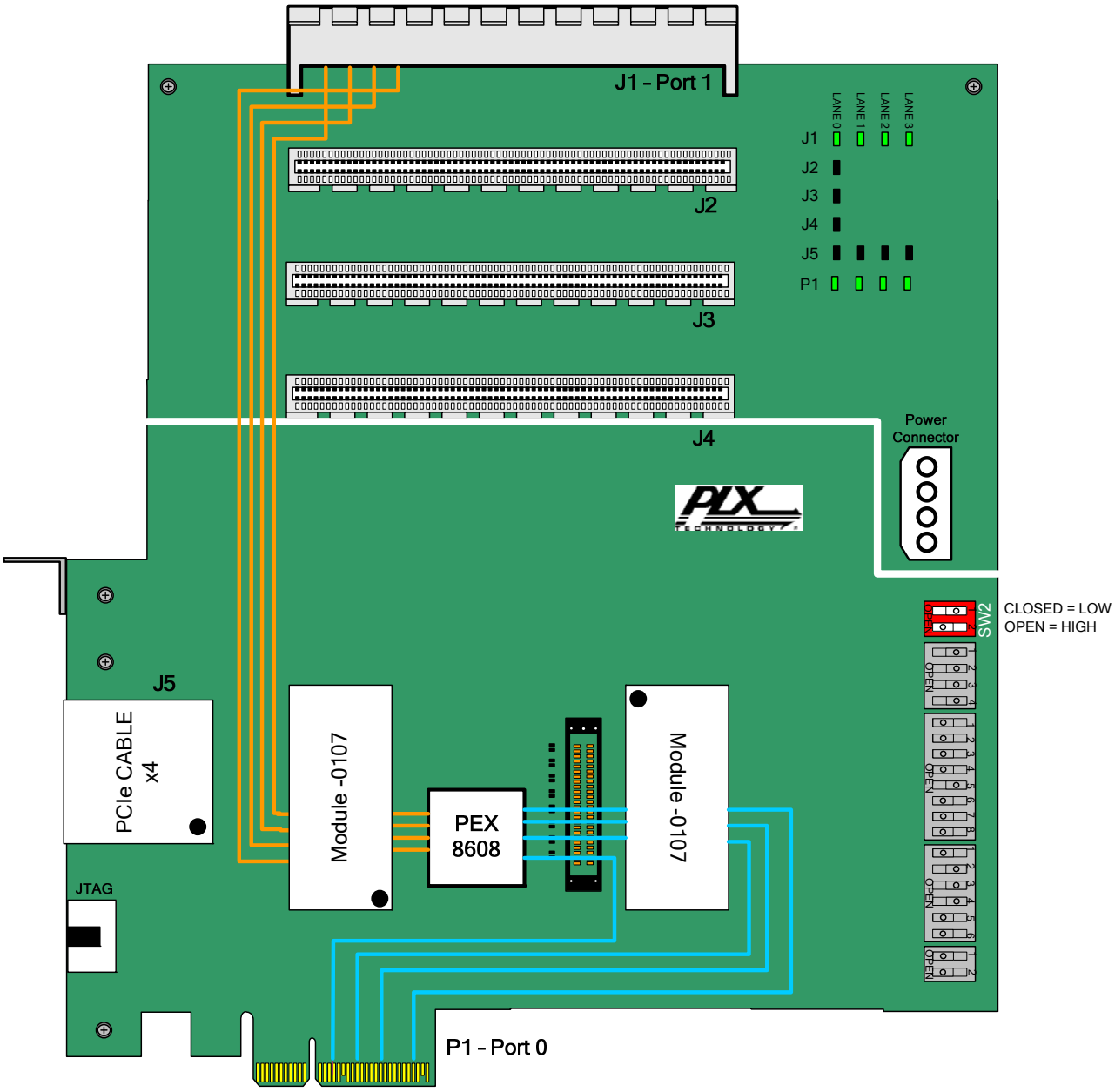


Figure 5. PEX 8608BA-AIC4U1D RDK x4x4 Configuration

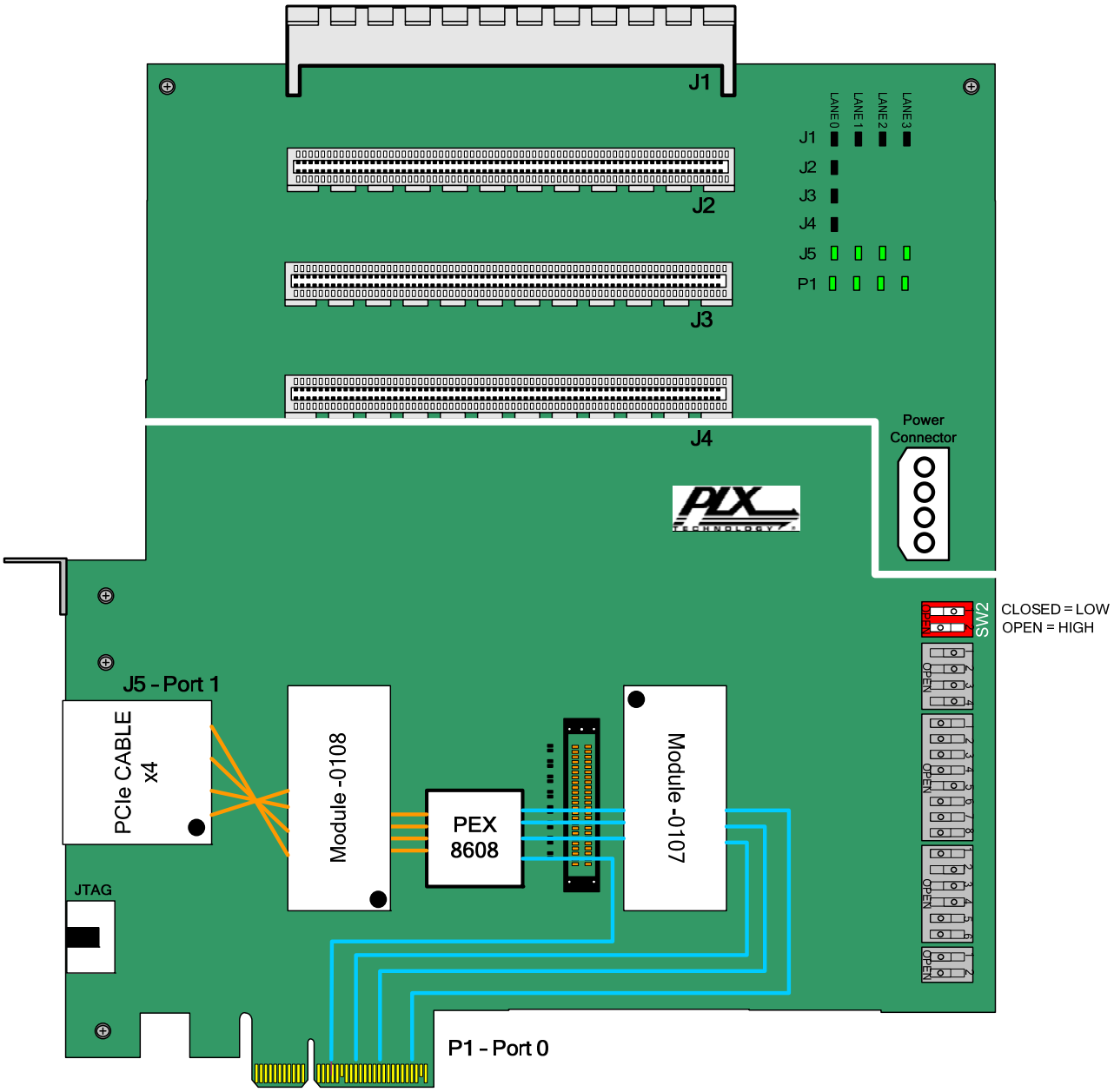


Figure 6. PEX 8608BA-AIC4U1D RDK x4 – Cable x4 Configuration

2.1.2 Configuration Modules

Two Configuration Modules are used on the board. The configuration modules consist of a 10x20 ball board-to-board high-speed connector, with one half of the connector mounted on the PEX 8608BA-AIC4U1D RDK, and the other half mounted on a small 4-layer PCB that performs the re-mapping. There are no other components. Two configuration modules are required. A 3-pin interface on the modules communicates their function to the board. The default configuration of the PEX 8608BA-AIC4U1D Rapid Development Kit provides two -0107 configuration modules. Additional modules can be purchased separately.

2.1.3 x4-to-x1x1x1x1 Breakout Board

The x4-to-x1x1x1x1 Breakout Board is a board that takes four lanes from its male card edge connector and routes each lane to its own female slot connector. PCIe REFCLK from the male card edge connector goes to a 1:4 fan-out buffer, which is driven to each of the female slot connectors. PERST#, 3.3VAUX, and WAKE# are passed from the card edge connector to each of the female slot connectors.

2.2 PCI Express Cable Support

The PEX 8608BA-AIC4U1D RDK is meant to demonstrate PCI Express cable usage. The cable connection, J5, is hardware configurable so that it can act as a downstream port. The board adheres to the downstream subsystem requirements as outlined in the *PCI Express External Cabling Specification Rev 1.0* for a x4 cable, with the following exceptions: none of the optional features are implemented, and CREFCLK is not dual 50 ohm terminated to ground. This means that only the lanes, and CPRSNT#, are implemented. Other side-band signals, such as CREFCLK and CPERST#, are not. The PCI Express cable connection can be used to demonstrate Non-Transparent operation to an NT host PC, see Section 2.3 for further details.

2.3 Non-Transparent Operation

The PEX 8608BA-AIC4U1D RDK board is capable of routing Lanes 4 through 7 to a x4 PCI Express cable connector, J5. This, in conjunction with a cable adapter board kit, permits connection to a second computer to demonstrate Non-Transparent (NT) operation. The cable adapter board kit can be purchased separately, part name: ***x4 PCI Express Cable Kit***. There is a specific power-up sequence that must be followed. The host PC must be powered-up before the NT host PC. If the host PC is running spread-spectrum clocking, then SSC isolation must be enabled. The NT host PC cannot be running spread-spectrum clocking. If it is, then a second PEX 8608BA-AIC4U1D RDK with SSC isolation enabled must be used in place of the cable adapter board in the NT host PC to provide clock isolation. The PEX_NT_RESET signal from the PEX 8608 device is brought out to a test point via.

Note: Please refer to the PEX8608 Errata document for updates on the SSC isolation function.

2.4 PCI Express Hot-Plug Circuitry

The PEX 8608 device supports Hot-Plug through a serial Hot-Plug interface brought out through I^2C port 1. Only slot connector J1 supports Hot-Plug. The PEX 8608BA-AIC4U1D RDK supports Hot-Plug to connector J1 via an IO expander IC. The I^2C address for the IO expander is set to 000b by way of pull-down resistors. The two power rails to this slot (3.3VDC and 12VDC) are current limited to 5 amps. Hot-Plug control of this slot can be disabled by setting switch SW10-1 to CLOSED (LOW), so that this slot is always on. The MRL# signal is simulated by switch SW10-2. Switch block SW8 sends the Hot-Plug port address to the PEX 8608 device. The INTERLOCK signal from the PEX 8608 device is brought out to a test point via.

2.5 Reference Clock Circuitry

The PEX 8608BA-AIC4U1D has circuitry to support SSC isolation. Refer to the *PEX 8608BA Quick Start Hardware Design Guide* for details on how spread-spectrum clock isolation is implemented in the PEX 8608 device.

The RefClk from the host PC is brought onto the board via card edge connector P1. This clock is assumed to be spread-spectrum. This clock drives a 1:3 clock fan-out buffer. One of these fan-out clocks goes to the PEX 8608 device's PEX REFCLK input. A second fan-out clock is routed to a 3-pin header associated with using the midbus soft-touch probe. The third fan-out clock goes to a 2:1 mux. The other input to this mux is from an onboard constant frequency clock generator. The output from this mux drives a 1:4 clock fan-out buffer, such as SpectraLinear's CY28400-2 device. The outputs from this fan-out buffer drive the downstream connectors. From the 1:4 fan-out buffer, one of these clocks is routed to connector J1 and can be enabled/disabled by the serial hot-plug circuit. If the hot-plug control is disabled, this clock is always enabled. The other three clocks are routed to connectors J2, J3, and J4, and are always enabled. A second onboard constant frequency clock generator drives the PEX REFCLK CFC input to the PEX 8608 device. Refer to Figure 7 below.

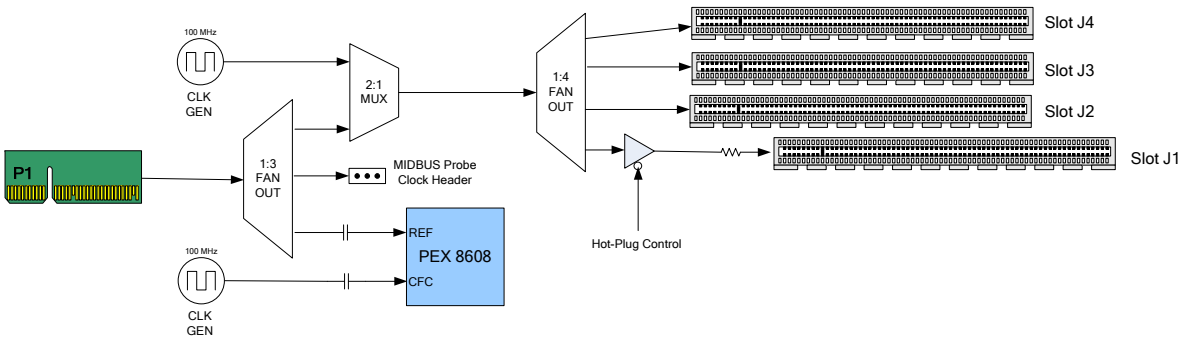


Figure 7. PEX 8608BA-AIC4U1D RDK Reference Clock Block Diagram

The clock into the PEX 8608 device's PEX REFCLK input drives all SerDes when SSC ISOLATION is disabled. In this case the downstream slots must also be driven by this clock. When SSC ISOLATION is disabled, the on-board circuitry turns off the CFC clock into the 2:1 mux, and sets the 2:1 mux to pass the RefClk from P1 to the downstream connectors by way of the 1:4 fan-out buffer.

When using SSC ISOLATION, the clock into the PEX 8608 device's PEX REFCLK input only drives the SerDes for Port 0. In this case Port 0 CAN ONLY BE x4, and Port 0 must be an upstream port or an NT port. The clock into the PEX 8608 device's PEX REFCLK CFC input drives the remaining SerDes. The downstream slots must also be driven by this constant frequency clock. When SSC ISOLATION is enabled, the on-board circuitry turns off the SSC from the 1:3 fan-out buffer into the 2:1 mux, and sets the 2:1 mux to pass the CFC from the on-board generator to the downstream connectors by way of the 1:4 fan-out buffer.

2.6 Lane Status Indicator LEDs

The status of each PCIe lane can be monitored by a bank of green LEDs driven by the PEX 8608 device's lane status balls. This bank of indicators are grouped in the upper right corner of the RDK board. Blinking indicates Gen 1 speeds, solid indicates Gen 2 speeds. Refer to Figure 8 below.

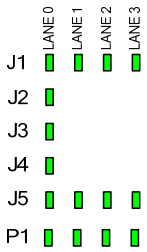


Figure 8. PEX 8608BA-AIC4U1D RDK Lane Status LEDs

2.7 Switches and Jumpers

The PEX 8608 has a number of strap pins which provide the capability to perform various types of hardware initialization without the use of software. Some strap pins are brought out to DIP switches, including the PORT_CFG strap pins. *When the DIP switch is CLOSED, the value is LOW. When the switch is OPEN, the value is HIGH.* Other strap pins that are not used in typical situations are strapped using pull-up/pull-down resistors. Strap pins I2C_ADDR[2:0] are pulled low, and STRAP_TESTMODE[3:0] are pulled high through resistors.

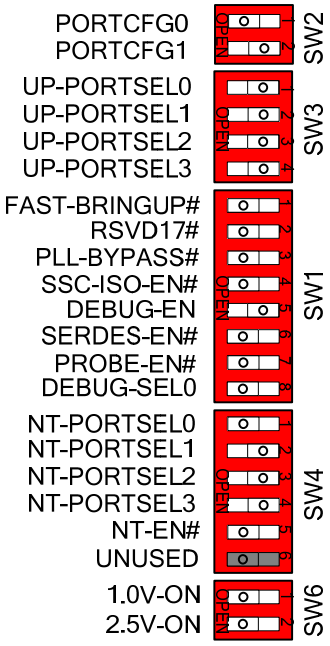


Figure 9. Hardware Strap Configuration Switches

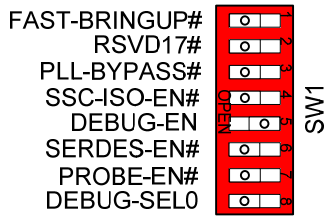
2.7.1 SW2 – Port Configuration

PORTCFG[1:0]	Port Configuration	Default RDK
LL	All x1	-
LH	x4 and 4 x1	*Yes*
HL	x4x4	-
All Others	*Reserved*	-

2.7.2 SW3 – Upstream Port Select

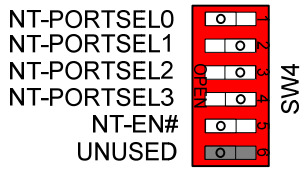
Default is Port 0. Upstream port and NT port cannot be the same port.

2.7.3 SW1 – Functional Strapping Selection



FAST-BRINGUP#	*Factory Test Only.* Keep HIGH(OPEN)
RSVD17#	*Factory Test Only.* Keep HIGH(OPEN)
PLL-BYPASS#	*Factory Test Only.* Keep HIGH(OPEN)
SSC-ISO-EN#	Default is HIGH(OPEN). LOW(CLOSED) Enables spread-spectrum clocking isolation. Refer to section 2.5 for details.
DEBUG-EN	Default is LOW(CLOSED). HIGH(OPEN) isolates the debug signals from on-board circuitry (Lane Status LEDs, etc.) so they only go to the debug headers. Refer to section 2.10 for details.
SERDES-EN#	Default is HIGH(OPEN). LOW(CLOSED) Enables SerDes debug mode. If Enabled, DEBUG-EN needs to be HIGH(OPEN).
PROBE-EN#	Default is HIGH(OPEN). LOW(CLOSED) Enables Probe debug mode. If Enabled, DEBUG-EN needs to be HIGH(OPEN).
DEBUG-SEL0	*Factory Test Only.* Keep HIGH(OPEN)

2.7.4 SW4 – Non-Transparent Port Select



Default is NT Port 1, with Non-Transparent disabled. Upstream port and NT port cannot be the same port. Location 6 on Switch SW4 is unused.

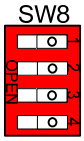
2.7.5 SW6 – On-Board Voltage Generation Enable

Default is all HIGH(OPEN). When LOW(CLOSED), these switches turn off the on-board voltage generation for the PEX 8608 device in order to use external voltage supplies to the PEX 8608 device for voltage margining and current measurement tests.

2.7.6 SW10 – Hot Plug Control

SHP EN	Default is HIGH(OPEN). When HIGH(OPEN) the PEX 8608 controls the Hot-Plug slot. When LOW(CLOSED) the Hot-Plug slot is always turned on.
MRL#	Default is LOW(CLOSED). This switch mimics the Manual Retention Lever signal.

2.7.7 SW8 – Hot Plug Slot Address



Default is all LOW(CLOSED). These switches transmit the Hot-Plug slot address back to the PEX 8608 device.

2.7.8 JP11 – 3.3 Vaux Jumper

Default position is NOT installed. The PEX 8608BA-AIC4U1D is meant to support WAKE functionality. Therefore, 3.3 Vaux is routed from card edge connector P1 to the downstream slot connectors. However, some slots that the PEX 8608BA-AIC4U1D is plugged into may not support 3.3 Vaux, and some add-in cards require 3.3 Vaux. In this case this jumper is installed to route 3.3 VDC from the card edge connector P1 to 3.3 Vaux of the downstream slot connectors.

2.8 Power Circuitry

The PEX 8608BA-AIC4U1D RDK is an add-in board. Power to the on-board circuitry is derived from PCIe card edge connector P1. Power to the PCIe slot connectors J1, J2, J3 and J4 is from hard disk drive connector P2. A 4-pin, straight mount, HDD power connector is used.

Dedicated power rails supply the 1.0VDC and 2.5VDC voltages to the PEX 8608 device only. This permits accurate current draw measurements when operating in various port configurations and traffic levels. Test points are available to attach external power supplies to provide the 1.0VDC (TP1 for 1.0VDC, TP2 for GND) and 2.5VDC (TP3 for 2.5VDC, TP4 for GND). This permits current draw measurements and voltage margining of the PEX 8608 device voltages. When using external supplies, onboard voltage generators need to be disabled by switch SW6. Bi-color red/green LED indicators are used to indicate when 1.0VDC is within 5%, and 2.5VDC is within 10%.

Power to PCIe slot J1 can be controlled by the Hot-Plug circuit.

2.9 Reset Circuit

The PEX 8608BA-AIC4U1D RDK accepts a PERST# from the host PC via card edge connector P1. This signal is OR'd with a manual reset circuit. The manual reset circuit consists of a pushbutton (SW7, upper left corner) that feeds into a reset timer. The reset timer monitors its power rail and reset input. If the reset input is low or the supply rail is out of range, the reset output is held. Once both conditions no longer exist, the reset output will de-assert after a programmable reset timeout period (capacitor adjustable, default value 128 msec). The OR'd reset signal goes to the PEX 8608 device's PEX_PERST# input pin, and the downstream slots' PERST# connector pins. PERST# to Slot J1 can be controlled by the PEX 8608 device's Hot-Plug interface.

2.10 Debug Mode Interface

The PEX 8608BA-AIC4U1D RDK supports the use of probe mode and SerDes debug mode through two MICTOR connectors and one 2x10 pin header. The MICTORs are high-speed connectors that deliver probe mode signals from the PEX 8608 device. The 2x10 pin header delivers selection signals to the PEX 8608 device. Probe mode signals are multiplexed onto other package balls that, in normal operation, deliver low speed signals for things like lane status. Table 3 provides a description of the signal mapping of the debug signals to the debug mode headers.

*Note: Inputs are marked in **blue**, outputs are marked in **red.***

Table 3. Signal Mapping of the Debug Signals

Ball Name	Probe Mode	SerDes Debug Mode	Connection
STRAP_NT_UPSTRM_PORTSEL2	stn_sel		JP8-pin23, SW4-pin3
STRAP_DEBUG_SEL0	mod_sel3	In_sel3	JP7-pin19, JP8-pin7, SW1-pin8
STRAP_UPCFG_TIMER_EN#	mod_sel2	rcvr_dat18	JP7-pin17, JP8-pin9, SW5-pin5
STRAP_SMBUS_EN#	mod_sel1	In2_add1	JP7-pin15, JP8-pin11, SW5-pin4
STRAP_SPARE0#	mod_sel0	In2_add0	JP7-pin11, JP8-pin13, SW5-pin1
I2C_ADDR2	port_sel3	In_sel0	JP7-pin3, JP8-pin21, R125-pin1
GPIO30	port_sel2	In_sel2	JP7-pin5, JP8-pin19
GPIO29	port_sel1	In_sel1	JP7-pin7, JP8-pin17
STRAP_NT_UPSTRM_PORTSEL3	port_sel0		JP7-pin9, JP8-pin15
GPIO3	outA_sel3	rx_status0	JP7-pin14, JP8-pin14
GPIO2	outA_sel2		JP7-pin16, JP8-pin12
GPIO1	outA_sel1		JP7-pin18, JP8-pin10
GPIO0	outA_sel0		JP7-pin20, JP8-pin8
I2C_ADDR1	outB_sel3		JP7-pin4, JP8-pin22, R123-pin1
I2C_ADDR0	outB_sel2		JP7-pin6, JP8-pin20, R84-pin1
GPIO5	outB_sel1	rx_status2	JP7-pin10, JP8-pin18
GPIO4	outB_sel0	rx_status1	JP7-pin12, JP8-pin16
STRAP_SPARE1#	ext_trig_in	rcvr_polarity	JP7-pin2, JP8-pin24
GPIO15	prb_outA9	rcvr_dat9	JP8-pin38
GPIO14	prb_outA8	rcvr_dat8	JP8-pin36
GPIO13	prb_outA7	rcvr_dat7	JP8-pin34
GPIO12	prb_outA6	rcvr_dat6	JP8-pin32
GPIO11	prb_outA5	rcvr_dat5	JP8-pin30
GPIO10	prb_outA4	rcvr_dat4	JP8-pin28
GPIO9	prb_outA3	rcvr_dat3	JP8-pin26
GPIO8	prb_outA2	rcvr_dat2	JP8-pin31
GPIO7	prb_outA1	rcvr_dat1	JP8-pin29
GPIO6	prb_outA0	rcvr_dat0	JP8-pin27
GPIO16	prb_outB8	xmit_dat8	JP9-pin7
PEX_LANE_GOOD7#	prb_outB7	xmit_dat7	JP9-pin22
PEX_LANE_GOOD6#	prb_outB6	xmit_dat6	JP9-pin20
PEX_LANE_GOOD5#	prb_outB5	xmit_dat5	JP9_pin18
PEX_LANE_GOOD4#	prb_outB4	xmit_dat4	JP9_pin16
PEX_LANE_GOOD3#	prb_outB3	xmit_dat3	JP9-pin14
PEX_LANE_GOOD2#	prb_outB2	xmit_dat2	JP9-pin12
PEX_LANE_GOOD1#	prb_outB1	xmit_dat01	JP9-pin10
PEX_LANE_GOOD0#	prb_outB0	xmit_dat0	JP9-pin8
N/C on ball N1	sclk/2	rclk/2	JP8-pin5
STRAP_NT_P2P_EN#	trig_out	trig_out	JP8-pin37

Due to signal integrity concerns, the debug mode interface is placed near, and directly attached to, the PEX 8608 device. A CPLD provides isolation between the PEX 8608 device and the onboard circuitry that these signals would drive when the PEX 8608 device is in normal operation. When in debug mode, the CPLD will block these signals from being propagated by setting switch SW1-5 (DEBUG-EN) to OPEN (HIGH). Please contact PLX when using the Debug Mode Interface.

2.11 Serial EEPROM Interface

The PEX 8608BA-AIC4U1D RDK provides a socketed Serial EEPROM. The contents of the serial EEPROM can be used to initialize the PEX 8608 device after power-on reset. PLX's Software Development Kit (SDK) can be used to read from or write to the EEPROM.

2.12 JTAG Interface

The PEX 8608BA-AIC4U1D RDK has a dedicated JTAG header (JP2) to the PEX 8608 device. The header provides connections for TDI, TDO, TMS, TCK, TRST# and GND. This connector is right angle and accessible through the bulkhead bracket.

2.13 I^2C Interface

The PEX 8608 device provides a two-wire I^2C compatible slave mode interface with three bit addressing. Through this out-of-band channel, the users can read, write, and configure the PEX 8608 device internal registers, run internal output probe mode, monitor error counters, and monitor status using PLX's Software Development Kit (SDK). There is no "standard" I^2C header pin arrangement; therefore, I^2C header type and pin assignments are somewhat arbitrary. A 2x2 pin header is used with a silkscreen outline to represent how an Aardvark controller would connect. See Figure 10, below. The upper 4 bits of the 7-bit I^2C address have a default value of 0111. The lower 3 bits of the 7-bit I^2C address are determined by external pull-up/pull-down resistors. The default I^2C address provided by the 8608BA-AIC4U1D RDK is 38h.

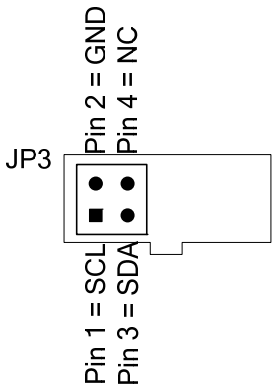


Figure 10: I^2C Interface Footprints

2.14 FATAL_ERR#, INTA#, PEX_NT_RESET#

The PEX 8608 device has a number of chip-specific side band signals that are intended for various uses. The FATAL_ERR# output (legacy SERR# equivalent) is used to indicate that the PEX 8608 device detected a fatal unrecoverable error. The INTA# output is used to be compatible with PCI. The PEX_NT_RESET# output is used to indicate an in-band Reset from an NT host. These three signals are brought out to test point vias, so that a customer can access these pins. The FATAL_ERR# signal also drives a red LED indicator. The INTA# signal also drives a yellow LED indicator.

3. Board Layout Information

3.1 Trace Routing Design Rules

3.1.1 Trace Width/Spacing Rules

There should be at least a 20-mil gap from the outer edge of one pair to the outer edge of another pair. PCI Express pairs are routed on the outer layers as much as possible, other signal traces are routed on outer and inner layers. The differential pairs are routed as loosely coupled pairs, 6 mil width, with 42.5 ohm single ended impedance, 85 ohm differential impedance.

3.1.2 Trace Length Matching Rules

The two traces of a differential pair are length matched within 5-mil. Because the pairs are loosely coupled, only the total length of the two halves need to be closely matched. We don't need to match each segment on a given layer for pairs that route on multiple layers. Differential pairs that form a common link should be matched pair-to-pair within 3-inches.

3.1.3 Trace Length Restrictions

Differential pairs being routed from the PEX 8608 device to the slot connectors should not exceed 8-inches in length.

3.2 PCB Stack-up

The PEX 8608BA-AIC4U1D RDK board is an 8 layer, 62-mil thick PCB. Refer to Figure 11, below.

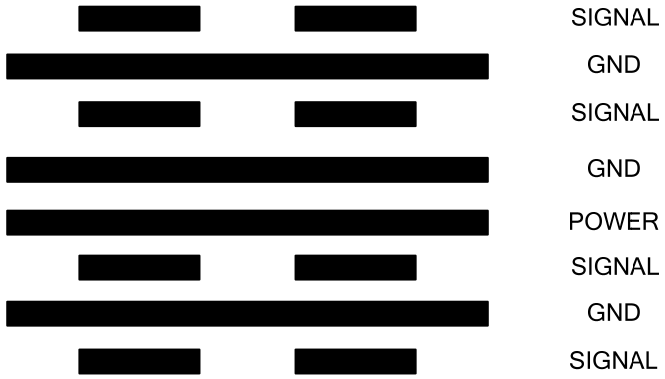


Figure 11: PEX 8608BA-AIC4U1D RDK Stack-up

This stack up includes 2 outer routing layers for much of the differential signaling, 2 inner layer signal planes for low speed or static single-ended signals and additional differential signaling, 3 ground planes adjacent to these to provide controlled impedance of the differential signals, and a split power plane to deliver the required voltages. Plane capacitance decoupling of the powers occurs between layers 4 and 5.

4. Bill of Materials / Schematics

Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
SURFACE MOUNT COMPONENTS									
1	47	Kemet	C0402C104K8P ACTU	CAP .10UF 10V CERAMIC X5R 0402	SMT, 0402	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C61, C62, C63, C64, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C104, C110, C111, C115, C116, C121, C127, C132, C135, C141, C143, C144, C145, C146	Digi-Key	399-3027-1-ND	0.1uF
2	10	AVX	TAJC226K020R	CAP TANTALUM 22UF 20V 10% SMD	EIA size C	C33, C34, C35, C36, C37, C38, C39, C40, C50, C81	Digi-Key	478-1711-1-ND	22uF
3	10	Kemet	C0603C105K8P ACTU	CAP CERAMIC 1.0UF 10V X5R 0603	SMT, 0603	C41, C42, C43, C44, C57, C58, C59, C60, C120, C142	Digi-Key	399-3118-1-ND	1uF
4	26	Panasonic	ECJ-ZEB1E102K	CAP 1000PF 25V CERAMIC X7R 0201	SMT, 0201	C45, C46, C47, C48, C49, C51, C52, C53, C54, C55, C56, C65, C66, C67, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80	Digi-Key	PCC2130CT-ND	1000pF
5	4	Panasonic	ECJ-3YB1C106M	CAP 10UF 16V CERAMIC X5R 1206 LOVOLT FOOTPRINT	SMT, 1206, LoVolt	C100, C108, C128, C140	Digi-Key	PCC2227CT-ND	10uF
6	2	Kemet	C0603C105K8P ACTU	CAP CERAMIC 1.0UF 10V X5R 0603, 2 VIA	SMT, 0603, 2via	C101, C109	Digi-Key	399-3118-1-ND	1uF
7	2	Kemet	C1206C226K9P ACTU	CAP 22UF 6.3V CER X5R SMD 1206 LOVOLT FOOTPRINT	SMT, 1206, LoVolt	C102, C103	Digi-Key	399-3229-1-ND	22uF
8	2	Panasonic	ECJ-1VB1H473K	CAP .047UF 50V CERAMIC X7R 0603	SMT, 0603	C105, C114	Digi-Key	PCC2286CT-ND	0.047uF
9	2	Panasonic	ECJ-0EB1E102K	CAP 1000PF 25V CERAMIC 0402 SMD	SMT, 0402	C122, C147	Digi-Key	PCC102BQCT-ND	1000pF
10	12	Panasonic	ECJ-0EB1C103K	CAP 10000PF 16V CERAMIC 0402 SMD	SMT, 0402	C123, C124, C125, C126, C129, C130, C133, C134, C136, C137, C138, C139	Digi-Key	PCC103BQCT-ND	0.01uF
11	4	Kemet	C0603C180J5G ACTU	CAP CERAMIC 18PF 50V NP0 0603	SMT, 0603	C148, C149, C150, C151	Digi-Key	399-1052-1-ND	18pF
12	16	Lumex	SML-LXT0805GW-TR	LED THIN 565NM GRN DIFF 0805 SMD	SMT, 0805	DS1, DS2, DS3, DS4, DS9, DS10, DS11, DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20, DS35	Digi-Key	67-1553-1-ND	Green
13	2	Lumex	SML-LXT0805YW-TR	LED THIN 585NM YEL DIFF 0805 SMD	SMT, 0805	DS30, DS36	Digi-Key	67-1554-1-ND	Yellow
14	2	Lumex	SML-LXT0805SRW-TR	LED THIN660NM SUPRED DIFF0805SMD	SMT, 0805	DS31, DS34	Digi-Key	67-1555-1-ND	Red
15	2	CML Innovative Technologies	CMD15-22SRUGC/TR8	LED, RED/GREEN HI BRT S TYPE SMD, If=20mA		DS32, DS33	Digi-Key	L6221115CT-ND	LED_BI

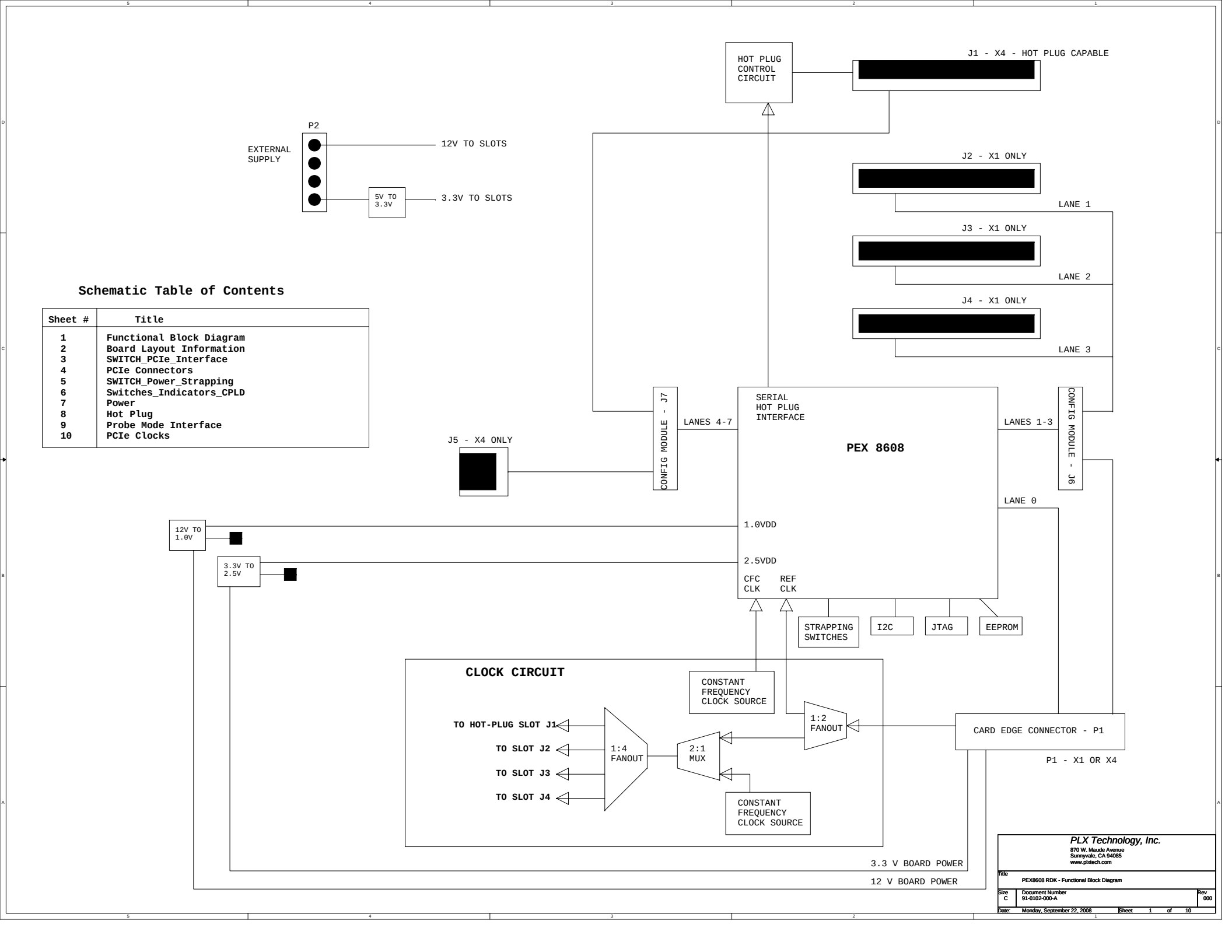
Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
16	2	Amp	767054-1	CONN, 38-pin MICTOR, RECPT, STRAIGHT	MICTOR38	JP8, JP9			MICTOR 38 RECEPT
17	1	Molex	87767-0123	PCI Express x16 straddle-mount connector	SMT, 164-pin	J1			PCI_EXP_X16_STRADDLE_MNT_CONN
18	1	Molex	75586-0011	Connector, Right-angle receptacle, PCIe x4 Cable	SMT, PCIe x4 Cable	J5	Mouser	538-75586-0011	PCIe x4 Cable
19	2	FCI	84517-101LF	Header, BGA, 10x20, recept, Pb Free	84517	J7, J6			84517-101
20	2	International Rectifier	IRF7470	MOSFET, N-CHAN, 10A, Rds=13 mohm	SO8	Q1, Q2			IRF7470
21	4	ON Semiconductor	MMBT3904LT1	NPN, GPSS, MMBT3904, SOT23		Q3, Q4, Q5, Q6			MMBT3904LT1
22	6	CTS Resistor Products	742-083-512-J	RESNET, MF, 5.1 KOHM NIL 5%, ISOLATED	742-CTS-RN-8	RN1, RN2, RN4, RN5, RN7, RN8	Digi-Key	742C083512JCT-ND	5.1K
23	2	Panasonic	ERJ-3EKF1431V	RES 1.43K OHM 1/10W 1% 0603 SMD	SMT, 0603	R1, R2	Digi-Key	P1.43KHCT-ND	1.43K
24	21	Yageo	9C06031A0R00JLHFT	RES 0.0 OHM 1/10W 5% 0603 SMD	SMT, 0603	R5, R6, R8, R9, R10, R15, R77, R97, R98, R99, R106, R108, R112, R177, R179, R135, R140, R142, R159, R164, R167	Digi-Key	311-0.0GCT-ND	0
25	4	Panasonic	ERJ-3GEYJ102V	RES 1.0K OHM 1/10W 5% 0603 SMD	SMT, 0603	R7, R16, R17, R18	Digi-Key	P1.0KGCT-ND	1K
26	43	Panasonic	ERJ-3GEYJ512V	RES 5.1K OHM 1/10W 5% 0603 SMD	SMT, 0603	R11, R12, R13, R14, R21, R48, R60, R66, R67, R75, R76, R85, R86, R103, R104, R105, R107, R109, R110, R113, R118, R124, R127, R128, R131, R138, R139, R144, R145, R158, R161, R163, R168, R170, R178, R180, R22, R23, R24, R25, R84, R123, R125	Digi-Key	P5.1KGCT-ND	5.1K
27	1	Panasonic	ERJ-3GEYJ152V	RES, Shunt Select Footprint, 0603	SMT, 0603-2	R19	Digi-Key	P1.5KGCT-ND	1.5K
28	3	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD	SMT, 0603	R20, R30, R31	Digi-Key	P10KGCT-ND	10K
29	4	Panasonic	ERJ-3EKF2261V	RES 2.26K OHM 1/10W 1% 0603 SMD	SMT, 0603	R26, R27, R28, R29	Digi-Key	P2.26KHCT-ND	2.26K
30	22	Panasonic	ERJ-3GEYJ391V	RES 390 OHM 1/10W 5% 0603 SMD	SMT, 0603	R32, R33, R34, R35, R40, R41, R42, R44, R45, R46, R47, R49, R50, R51, R52, R63, R64, R71, R72, R82, R83, R120	Digi-Key	P390GCT-ND	390
31	3	Panasonic	ERJ-3GEYJ151V	RES 150 OHM 1/10W 5% 0603 SMD	SMT, 0603	R53, R94, R95	Digi-Key	P150GCT-ND	150
32	1	Panasonic	ERJ-3GEYJ333V	RES 33K OHM 1/10W 5% 0603 SMD	SMT, 0603	R65	Digi-Key	P33KGCT-ND	33K
33	1	Panasonic	ERJ-3GEYJ273V	RES 27K OHM 1/10W 5% 0603 SMD	SMT, 0603	R68	Digi-Key	P27KGCT-ND	27K
34	1	Panasonic	ERJ-3EKF4001V	RES 4.00K OHM 1/10W 1% 0603 SMD	SMT, 0603	R69	Digi-Key	P4.00KHCT-ND	4.00K

Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
35	2	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/10W 1% 0603 SMD	SMT, 0603	R70, R79	Digi-Key	P1.00KHCT-ND	1.00K
36	1	Panasonic	ERJ-3EKF6811V	RES 6.81K OHM 1/10W 1% 0603 SMD	SMT, 0603	R73	Digi-Key	P6.81KHCT-ND	6.81K
37	1	Panasonic	ERJ-3EKF1432V	RES 14.3K OHM 1/10W 1% 0603 SMD	SMT, 0603	R74	Digi-Key	P14.3KHCT-ND	14.3K
38	1	Panasonic	ERJ-3EKF1501V	RES 1.50K OHM 1/10W 1% 0603 SMD	SMT, 0603	R78	Digi-Key	P1.50KHCT-ND	1.50K
39	1	Panasonic	ERJ-3EKF1212V	RES 12.1K OHM 1/10W 1% 0603 SMD	SMT, 0603	R80	Digi-Key	P12.1KHCT-ND	12.1K
40	1	Panasonic	ERJ-3EKF4531V	RES 4.53K OHM 1/10W 1% 0603 SMD	SMT, 0603	R81	Digi-Key	P4.53KHCT-ND	4.53K
41	1	Panasonic	ERJ-3GEYJ132V	RES 1.3K OHM 1/10W 5% 0603 SMD	SMT, 0603	R87	Digi-Key	P1.3KGCT-ND	1.3K
42	1	Panasonic	ERJ-3EKF2802V	RES 28.0K OHM 1/10W 1% 0603 SMD	SMT, 0603	R88	Digi-Key	P28.0KHCT-ND	28.0K
43	1	Panasonic	ERJ-3EKF4991V	RES 4.99K OHM 1/10W 1% 0603 SMD	SMT, 0603	R89	Digi-Key	P4.99KHCT-ND	4.99K
44	2	Panasonic	ERJ-3GEYJ330V	RES, CF, 33 OHM, 1/16W, 5%, 0603 SMD	SMT, 0603	R90, R93	Digi-Key	P33GCT-ND	33
45	2	Panasonic	ERJ-3EKF3481V	RES 3.48K OHM 1/10W 1% 0603 SMD	SMT, 0603	R91, R92	Digi-Key	P3.48KHCT-ND	3.48K
46	2	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD	SMT, 0603	R96, R101	Digi-Key	P2.00KHCT-ND	2.00K
47	2	TTelectronics	LR2512-01-R020-F	Res. 2W, 0.02 ohm 1%	SMT, 2512	R100, R102	Mouser	66-LR2512-01-R040-F	0.02
48	1	Panasonic	ERJ-3GEYJ152V	RES 1.5K OHM 1/10W 5% 0603 SMD	SMT, 0603	R111	Digi-Key	P1.5KGCT-ND	1.5K
49	3	Yageo	9C08052A0R00JLHFT	RES 0.0 OHM 1/8W 5% 0805 SMD	SMT, 0805	R114, R149, DS21	Digi-Key	311-0.0ACT-ND	0
50	18	Panasonic	ERJ-1GEF49R9C	RES 49.9 OHM 1/20W 1% 0201 SMD	SMT, 0201	R115, R116, R119, R121, R136, R137, R146, R147, R152, R153, R156, R157, R166, R169, R174, R175, R176, R181	Digi-Key	P49.9ABCT-ND	49.9
51	2	Panasonic	ERJ-3GEYJ272V	RES 2.7K OHM 1/10W 5% 0603 SMD	SMT, 0603	R117, R122	Digi-Key	P2.7KGCT-ND	2.7K
52	2	Panasonic	ERJ-2RKF4750X	RES 475 OHM 1/16W 1% 0402 SMD	SMT, 0402	R129, R182	Digi-Key	P475LCT-ND	475
53	14	Panasonic	ERJ-1GEF33R2C	RES 33.2 OHM 1/20W 1% 0201 SMD	SMT, 0201	R130, R132, R133, R134, R141, R143, R150, R151, R154, R155, R160, R162, R172, R173	Digi-Key	P33.2ABCT-ND	33.2
54	2	Panasonic	ERJ-3EKF4750V	RES 475 OHM 1/16W 1% 0603 SMD	SMT, 0603	R148, R171	Digi-Key	P475HCT-ND	475
55	4	Panasonic	ERJ-2RKF33R2X	RES 33.2 OHM 1/16W 1% 0402 SMD	SMT, 0402	R185, R186, R189, R190	Digi-Key	P33.2LCT-ND	33.2
56	2	Omron	B3S-1002	SWITCH TACT 6MM SMD MOM 230GF		SW7, SW9	Digi-Key	SW416-ND	B3S-1002
57	1	PLX Technology	PEX8608-AA50BCG	IC, PCI Express Switch, Gen 2, 8 Lane		U1			PEX 8608

Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
58	1	Maxim	MAX6658	IC, Temperature Sensor, SMBus-Compatible, SO8	SO8	U3			MAX6658
59	1	Lattice	LCMXO256C-3TN100C	IC, CPLD	TQFP100	U4			LCMXO256C-3TN100C
60	2	Belfuse	S7AH-08E1A00	IC, Non-iso DC/DC converter, 12V-to-1V @ 8A	SMT, 7-pin Belfuse	U5, U10			S7AH-08E1A00
61	1	Maxim	MAX8556ETE	IC, V-REG, 4 A, ADJ, Enable, POK	Thin QFN16	U6			MAX8556
62	1	Intersil	ISL6132IR	IC, MULTI-VOLTAGE SUPERVISOR	L24.4x4	U7			ISL6132
63	1	Maxim	MAX6412UK29-T	IC, Reset controller, 2.9V threshold, Adj. reset timeout	SOT23-5	U8			MAX6412
64	1	Fairchild	NC7SZ08P5X	IC, AND Gate, Tpd=15nsec, 24mA	SC70-5	U9			NC7SZ08
65	1	TI	TPS2311IPW	IC, DUAL HOT SWAP CONTROLLER	TSSOP20	U11			TPS2311
66	1	Maxim	MAX7311AUG	IC, 2-WIRE, 16-BIT IO EXPANDER	TSSOP24	U12			MAX7311AUG
67	2	SpectraLinear	CY28400OXC-2	IC, 1:4 100MHz Differential Clock Fanout	SSOP28	U16, U18			CY28400-2
68	1	Maxim	MAX4906	IC, Bus Switch, Dual SPDT, Ron=4 ohm typ, BW=1.0 GHz, Con=4pF typ	uDFN10	U17			MAX4906
69	2	Fairchild	NC7SZ04P5X	IC, NOT GATE	SC70-5	U19, U22			NC7SZ04P5X
70	2	On Semiconductor	NB3N3002D	IC, Crystal-to-HCSL Clock Generator, OE	TSSOP16	U23, U24			NB3N3002
THROUGH-HOLE COMPONENTS									
100	4	Vishay	94SP187X0016EBP	CAP, Oscon, 180uF, 16V	E case	C98, C99, C106, C107			180uF
101	1	Tyco Electronics Amp	5103310-1	CONN HEADER LOPRO R/A 10POS 15AU	0.1" 2x5 RA	JP2	Digi-Key	A33179-ND	JTAG Header
102	2	3M	929710-10-02	CONN HEADER .100 DUAL STR 4POS	0.1" 2x2	JP3, JP4	Digi-Key	929710-10-02-ND	HEADER 2X2
103	1	3M	929400-01-36	HEADER, Lattice Programming, 1x8 VERTICAL, .1in THRU-HOLE	0.1" 1x8	JP6	Digi-Key	929400-01-36-ND	Lattice JTAG
104	1	3M	929710-10-10	CONN HEADER LOPRO STR 20POS 15AU	0.1" 2x10	JP7	Digi-Key	929710-10-10-ND	PRB MODE INPUT HEADER
105	1	3M	929400-01-36	HEADER, 1x2 VERTICAL, .1in THRU-HOLE	SIP-2	JP11	Digi-Key	929400-01-36-ND	JUMPER
106	3	Molex	87715-3302	PCI Express x16 Through-hole connector	TH, 164-pin	J2, J3, J4			PCI_EXP_X16_FEMALE_CONN

Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
107	1	Molex	74540-0400	Guide house, for 4x link PCIe external cable connector	TH, PCIe x4 Cable	J5	Mouser	538-74540-0400	
108	1	Molex	15-24-4449	Header, HD 4-pin, straight		P2	Arrow		IDE4_HEADER
109	1	Grayhill	76SB08T	SWITCH 8POS DIP EXT ROCK UNSEALD	DIP16	SW1	Digi-Key	GH7177-ND	SW DIP-8
110	2	Grayhill	76SB04T	SWITCH 4POS DIP EXT ROCK UNSEALD	DIP8	SW3, SW8	Digi-Key	GH7170-ND	SW DIP-4
111	1	Grayhill	76SB06T	SWITCH DIP EXT RCKR UNSEALD 6POS	DIP12	SW4	Digi-Key	GH7174-ND	SW DIP-6
112	3	Grayhill	76SB02T	SWITCH DIP EXT ROCKER 2POS TH	DIP4	SW2, SW6, SW10	Digi-Key	GH7115-ND	SW DIP-2
113	1	Mill-Max	210-93-308-41-001000	Socket, EEPROM, DIP8, Thru-hole	DIP8	U2	Digi-Key	ED60000-ND	AT25128A
114	2	Citizen	HC49US25.000 MABJ-UB	CRYSTAL 25.000 MHZ HC49/US	2-pin thru-hole	Y1, Y2			25MHz
115	4	Components Corporation	TP-101-10-T	Test Point Post		TP1, TP2, TP3, TP4			TP-101-10-T
MANUALLY INSERTED COMPONENTS									
200	1	Atmel	AT25128A-10PI-2.7	IC SRL EE 128K 2.7V 8DIP	DIP-8	U2	Digi-Key	AT25128A-10PI-2.7-ND	AT25128A
201	2	PLX Technology	91-0107-000-A	CONFIGURATION MODULE, A3-to-B3		J6, J7			0107
202	1	Amp	881545-2	SHUNT LP W/HANDLE 2 POS 30AU		JP11	Digi-Key	A26242-ND	
MISCELLANEOUS COMPONENTS									
300	1	Keystone Electronics	9203	Modified PCI bracket			Mouser	534-9203	
301	1	Building Fasteners	PMSSS 440 0025 PH	Phillips Panhead screw, 4-40 thread, 0.25"			Digi-Key	H703-ND	
302	1	PLX Technology	90-0102-000-A	PCIe 8 LANE SWITCH RDK PCB, GEN2, Rev 000					
303	1	PLX Technology	91-0106-000-A	PCIe x4 to 4x1 Breakout Board					
PARTS SHOULD NOT BE ASSEMBLED									
	1	Agilent	E5387-68701	Header, Midbus LAI Probe Shroud	PCIe MIDBUS	JP1			Midbus LAI
	1	Yageo	9C06031A0R00JLHFT	RES 0.0 OHM 1/10W 5% 0603 SMD	SMT, 0603	R165	Digi-Key	311-0.0GCT-ND	NL
	4	Panasonic	ERJ-2RKF33R2X	RES 33.2 OHM 1/16W 1% 0402 SMD	SMT, 0402	R183, R184, R187, R188	Digi-Key	P33.2LCT-ND	NL
	2	Maxim	DS4100H+	IC, HCSL Oscillator, 100 MHz	LCCC10	U20, U21			DS4100H
	2	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402	SMT, 0402	C112, C113	Digi-Key	399-3027-1-ND	0.1uF
	1	Samtec	TMS-103-02-S-S	HEADER, RefClk, 3-pin, 0.05"	TMS-103-02-S-S	JP10			TMS-103-02-S-S

Item #	Qty	Man.	Man. Part #	Description	Package Type	Reference	Disti	Distributor Part #	Part
SECOND SOURCE / ALTERNATIVE PARTS									
	2	On Semiconductor	NB3N5573D	IC, Crystal-to-HCSL Clock Generator, OE, Dual	TSSOP16	U23, U24			NB3N5573
	1	Maxim	MAX8557ETE	IC, V-REG, 4 A, ADJ, Enable, POR	Thin QFN16	U6			MAX8557


HOT PLUG CONTROL CIRCUIT
J1 - X4 - HOT PLUG CAPABLE
P2
EXTERNAL SUPPLY
12V TO SLOTS
5V TO 3.3V
3.3V TO SLOTS
J2 - X1 ONLY
LANE 1
J3 - X1 ONLY
LANE 2
J4 - X1 ONLY
LANE 3
Schematic Table of Contents
Sheet # Title
1 Functional Block Diagram
2 Board Layout Information
3 SWITCH_PCIe_Interface
4 PCIe Connectors
5 SWITCH_Power_Strapping
6 Switches_Indicators_CPLD
7 Power
8 Hot Plug
9 Probe Mode Interface
10 PCIe Clocks
CONFIG MODULE - J7
LANES 4-7
SERIAL HOT PLUG INTERFACE
PEX 8608
LANES 1-3
CONFIG MODULE - J6
J5 - X4 ONLY
LANE 0
12V TO 1.0V
1.0VDD
3.3V TO 2.5V
2.5VDD
CFC CLK
REF CLK
STRAPPING SWITCHES
I2C
JTAG
EEPROM
CLOCK CIRCUIT
CONSTANT FREQUENCY CLOCK SOURCE
1:2 FANOUT
CARD EDGE CONNECTOR - P1
P1 - X1 OR X4
TO HOT-PLUG SLOT J1
TO SLOT J2
TO SLOT J3
TO SLOT J4
1:4 FANOUT
2:1 MUX
CONSTANT FREQUENCY CLOCK SOURCE
3.3 V BOARD POWER
12 V BOARD POWER
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Title
PEX8608 RDK - Functional Block Diagram
Size C
Document Number 91-0102-000-A
Rev 000
Date: Monday, September 22, 2008
Sheet 1 of 10

Board Thickness	= 63 mils

LAYER STACKUP

L1, SIGNAL 1		
	PREPREG, Er=4.0, 3.5 mils	
L2, GND		
	LAMINATE, Er=4.0, 5.0 mils	
L3, SIGNAL 2		
	PREPREG, Er=4.0, 4.5 mils	
L4, GND		
	LAMINATE, Er=4.0, 28.0 mils	
L5, POWER		
	PREPREG, Er=4.0, 4.5 mi/	
L6, SIGNAL 3		
	LAMINATE, Er=4.0, 5.0 mils	
L7, GND		
	PREPREG, Er=4.0, 3.5 mils	
L8, SIGNAL 4		

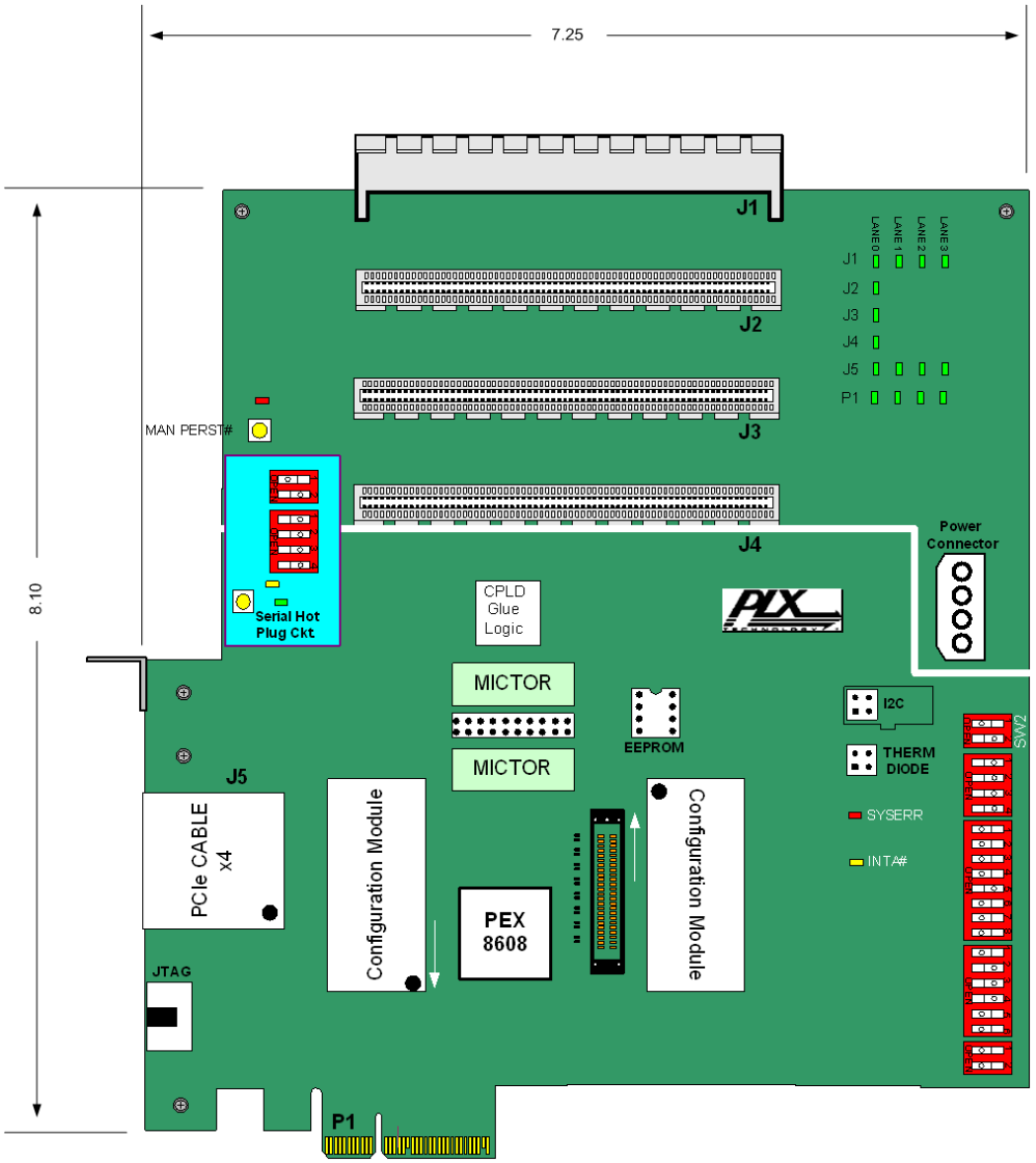
OUTER TRACES

WIDTH = 6.0 mils
Cu = 1.50 oz
DIFF Trace Zo = 85 ohm

INNER TRACES

WIDTH = 6.0 mils
Cu = 0.50 oz
DIFF Trace Zo = 85 ohm

NL = No Load



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Title	PEX8608 RDK - Board Layout Information	
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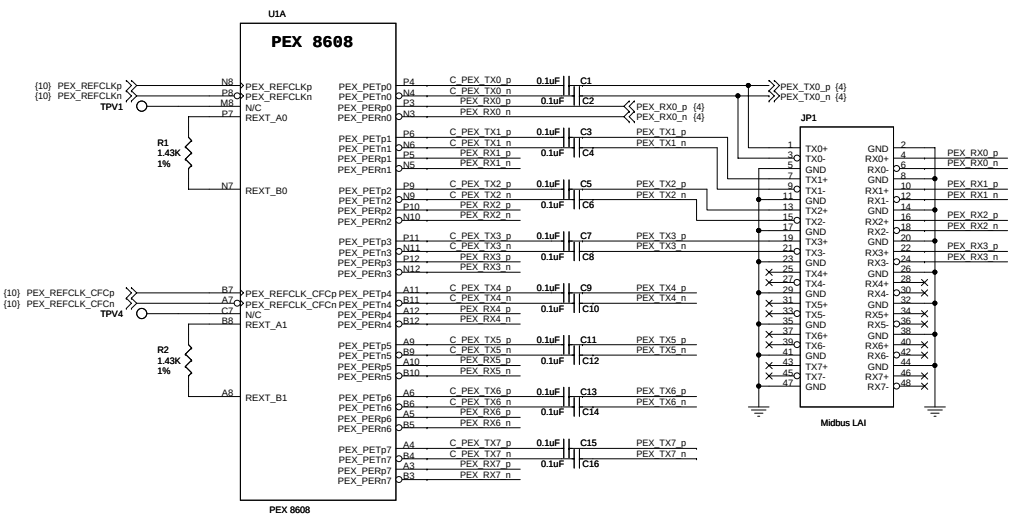
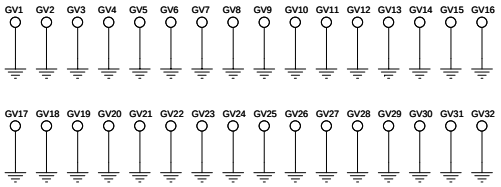
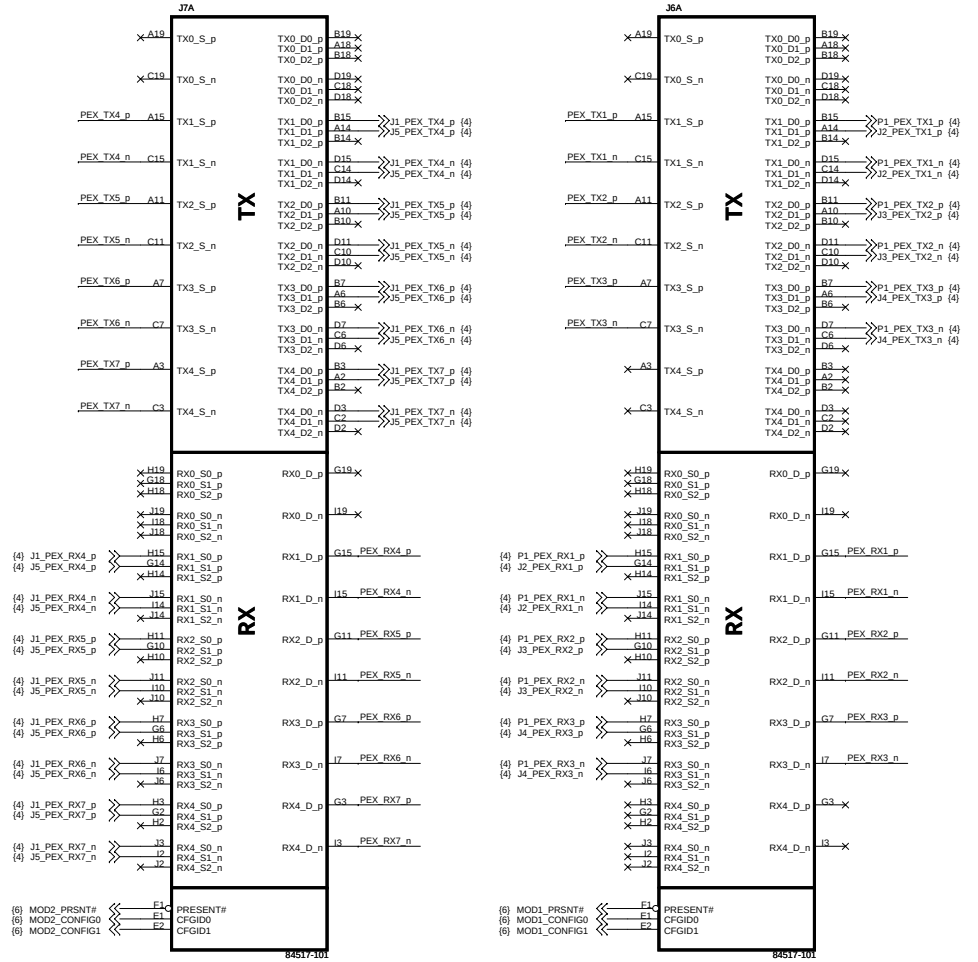
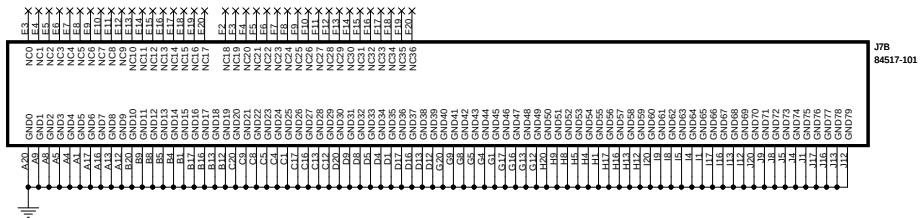
Date: Monday, September 22, 2008	Sheet 2 of 10	

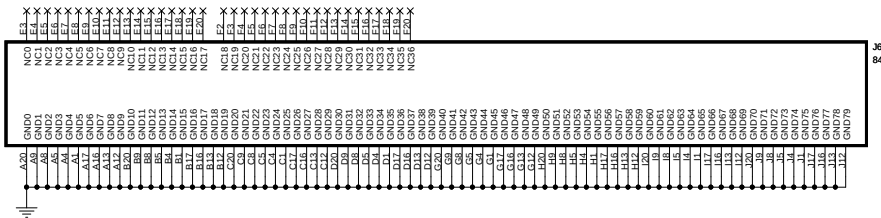


STITCHING VIAS WHERE NEEDED









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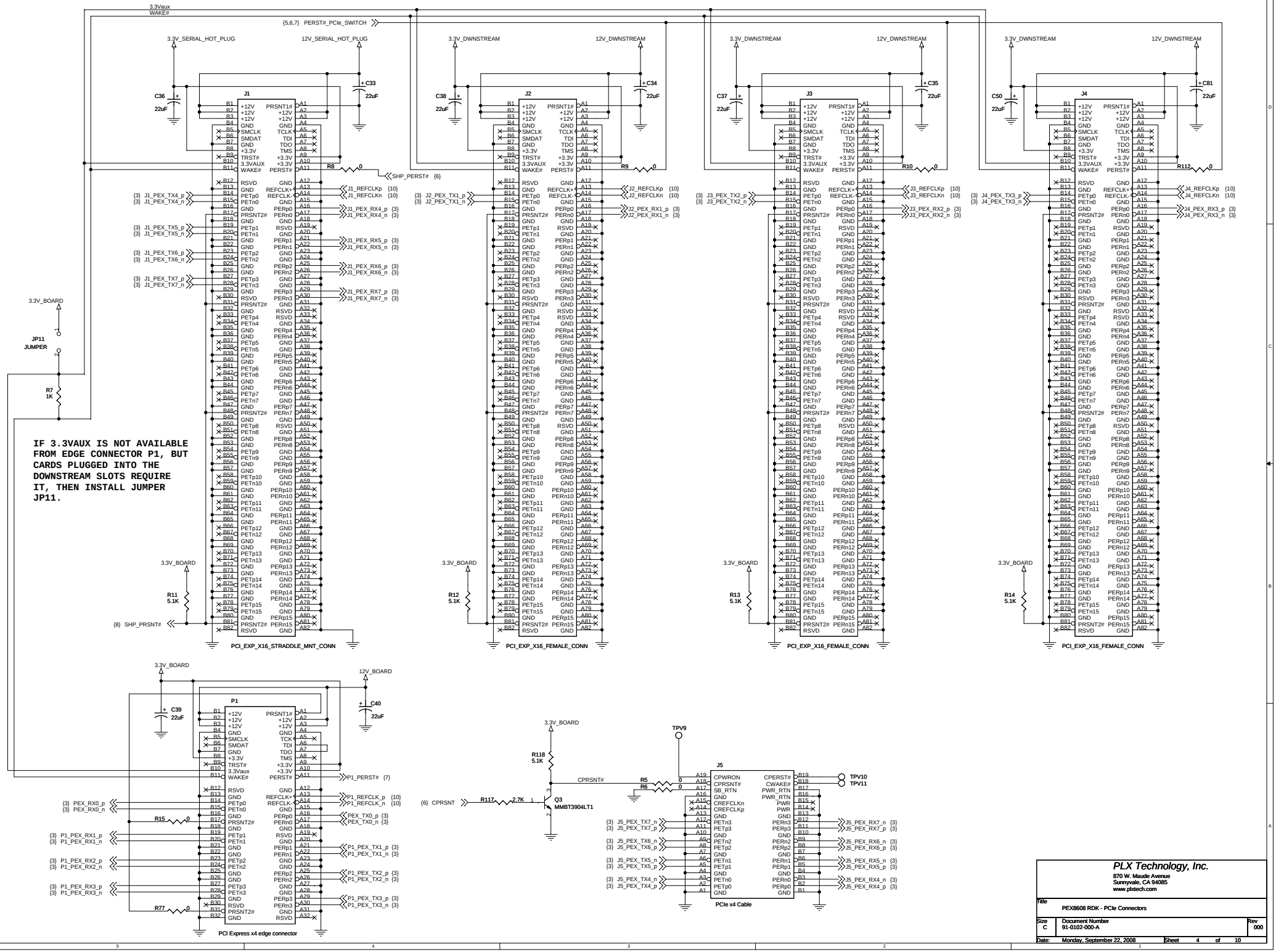
Title PEX8608 RDK - PCIe INTERFACE		
Size C	**Document Number** 91-0102-000-A	**Rev** 000
Date: Saturday, December 13, 2008	**Sheet** 3 of 10	


3.3Vaux
WAKE#
{5,6,7} PERST#_PCIe_SWITCH
3.3V_SERIAL_HOT_PLUG
12V_SERIAL_HOT_PLUG
3.3V_DWNSTREAM
12V_DWNSTREAM
C36
C38
C37
C50
C33
C34
C35
C81
22uF
J1
J2
J3
J4
PCI_EXP_X16_STRADDLE_MNT_CONN
PCI_EXP_X16_FEMALE_CONN
3.3V_BOARD
JP11
JUMPER
R7
1K
R8
R9
R10
R112
SHP_PERST# {6}
{8} SHP_PRSNT#
R11
5.1K
R12
5.1K
R13
5.1K
R14
5.1K
IF 3.3VAUX IS NOT AVAILABLE FROM EDGE CONNECTOR P1, BUT CARDS PLUGGED INTO THE DOWNSTREAM SLOTS REQUIRE IT, THEN INSTALL JUMPER JP11.
12V_BOARD
C39
C40
P1
PCI Express x4 edge connector
P1_PERST# {7}
R15
R77
R118
5.1K
Q3
MMBT3904LT1
CPRSNT#
R117
2.7K
R5
R6
TPV9
TPV10
TPV11
J5
PCIe x4 Cable
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Title
PEX8608 RDK - PCIe Connectors
Size C
Document Number 91-0102-000-A
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Date: Monday, September 22, 2008
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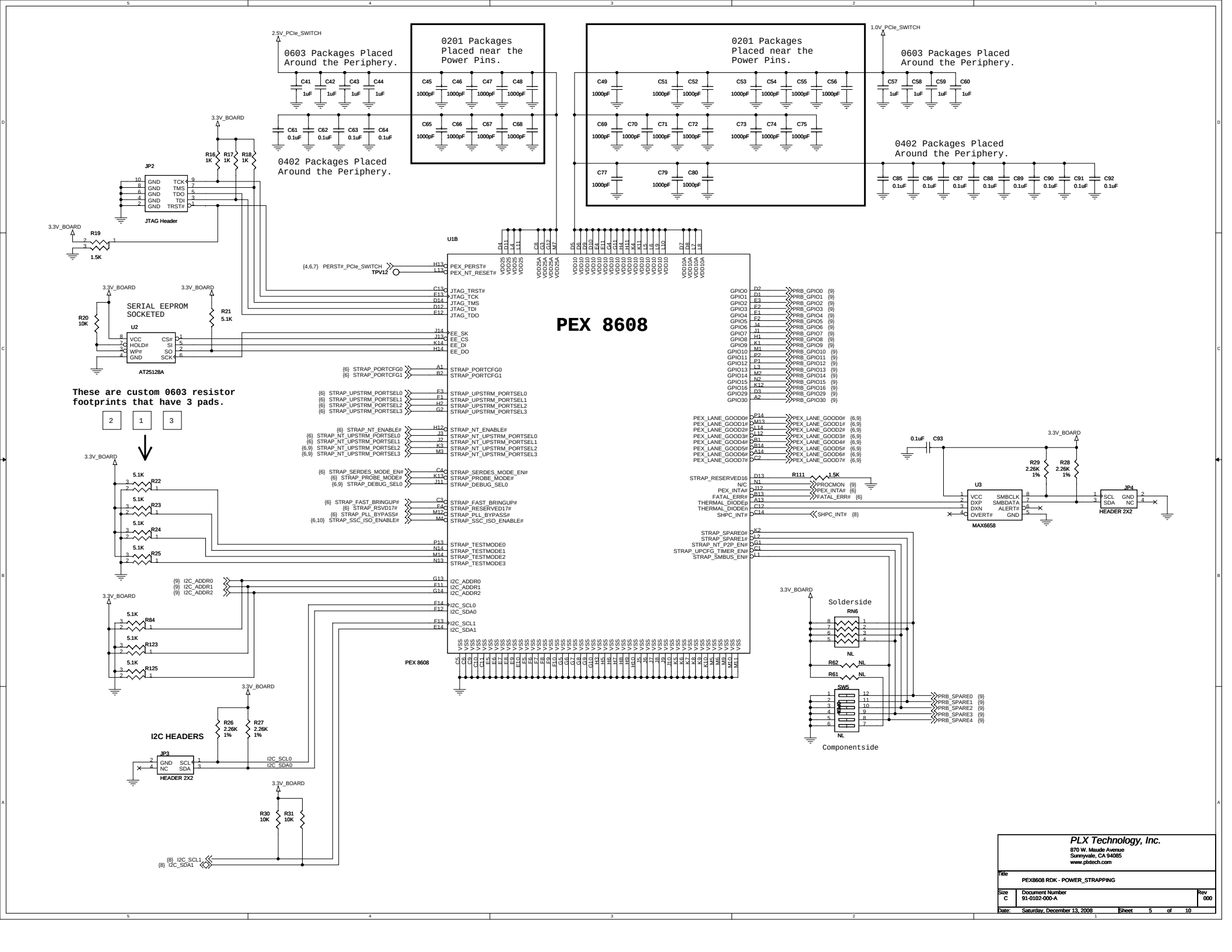

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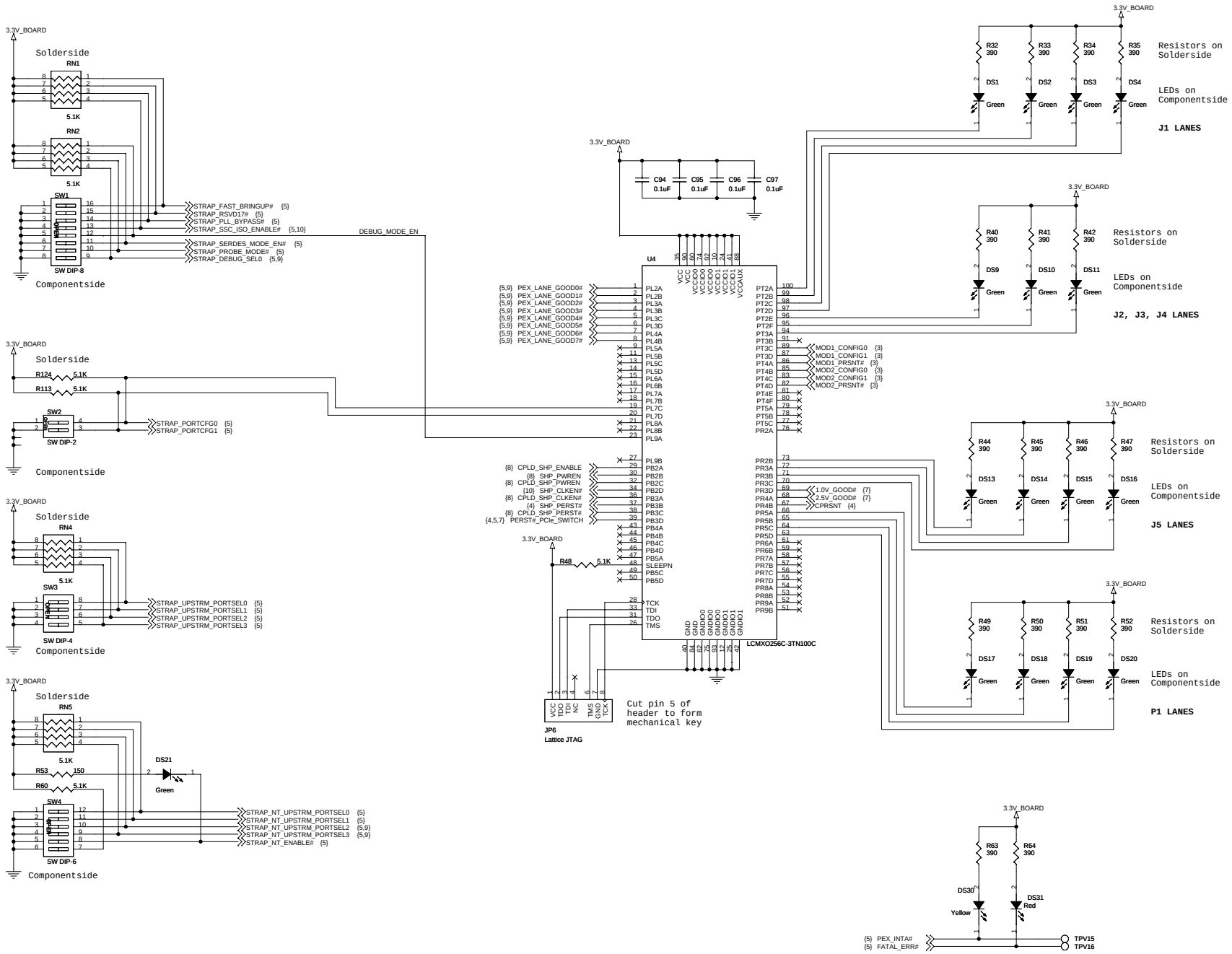
870 W. Maude Avenue Sunnyvale, CA 94085 www.plxtech.com		
Title: PEX8608 RDK - POWER_STRAPPING		
Size: C	Document Number: 91-0102-000-A	Rev: 000
Date: Saturday, December 13, 2008	Sheet 5 of 10	



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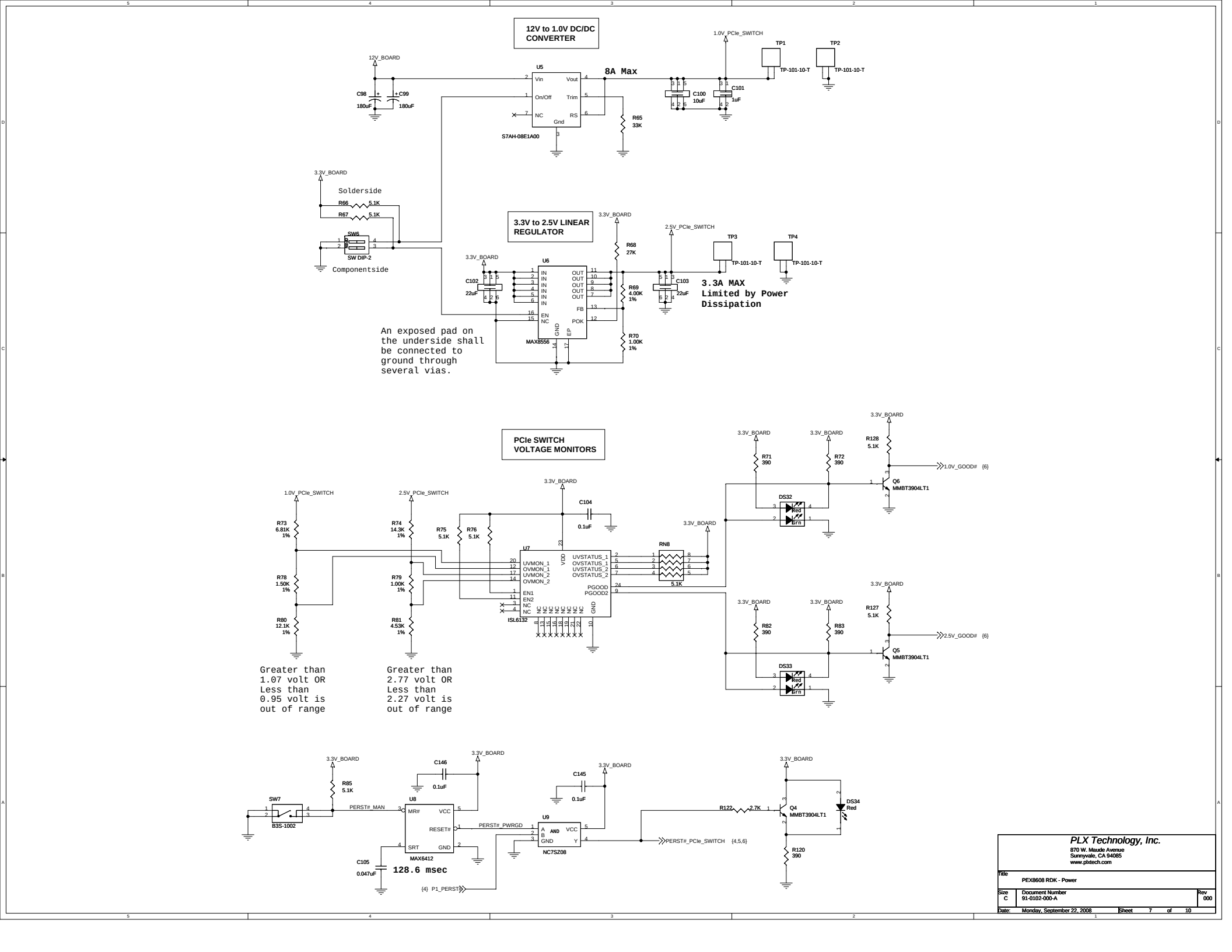
Title: PEX8608 RDK - Switches / Indicators/CPLD		
Size: C	Document Number: 91-0102-000-A	Rev: 000
Date: Monday, September 22, 2008	Sheet 6 of 10	



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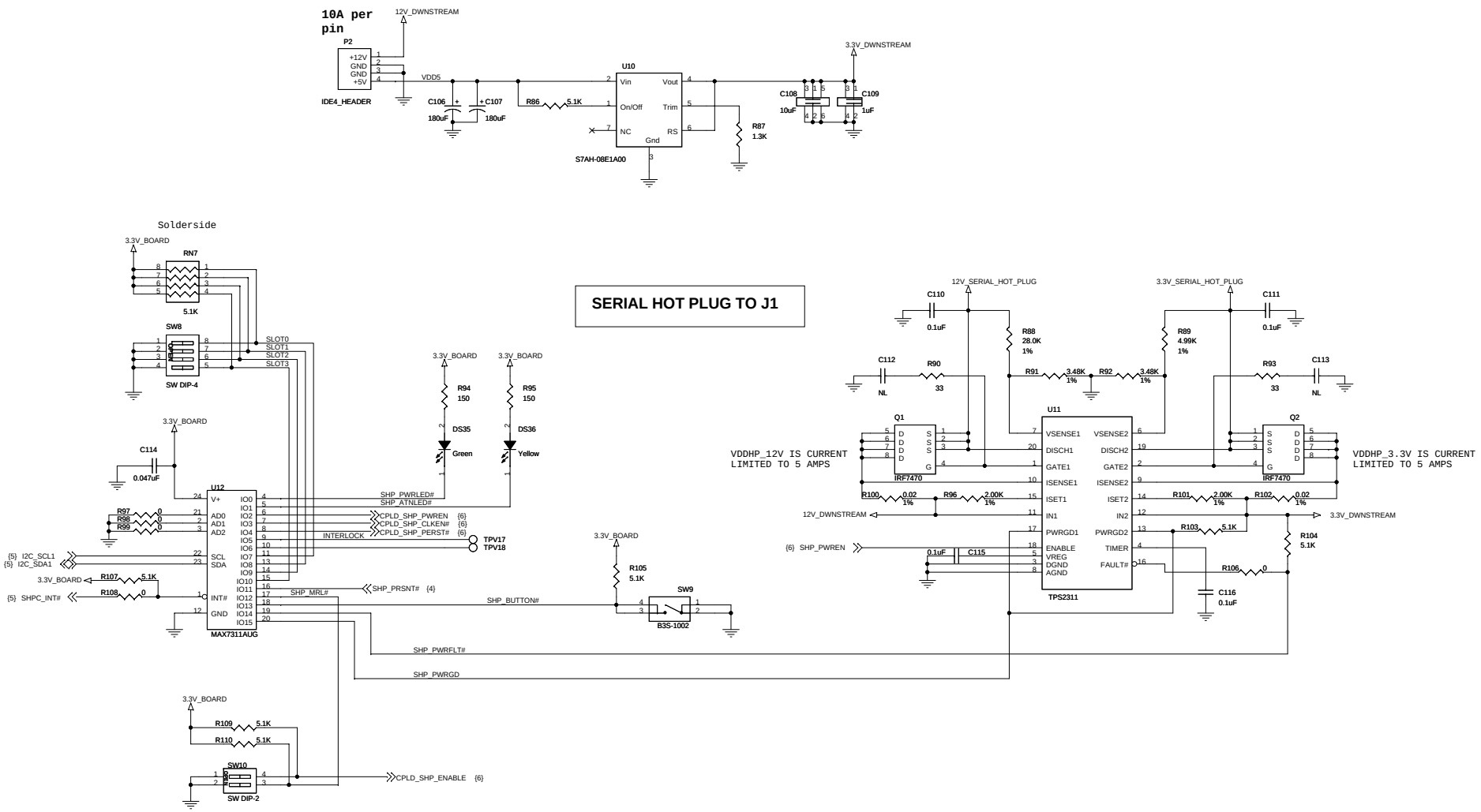
Title	PEX8608 RDK - Power
Size C	Document Number 91-0102-000-A, Rev 000
Date: Monday, September 22, 2008	Sheet 7 of 10



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Title: PEX8608 RDK - Hot Plug		
Size: C	Document Number: 91-0102-000-A	Rev: 000
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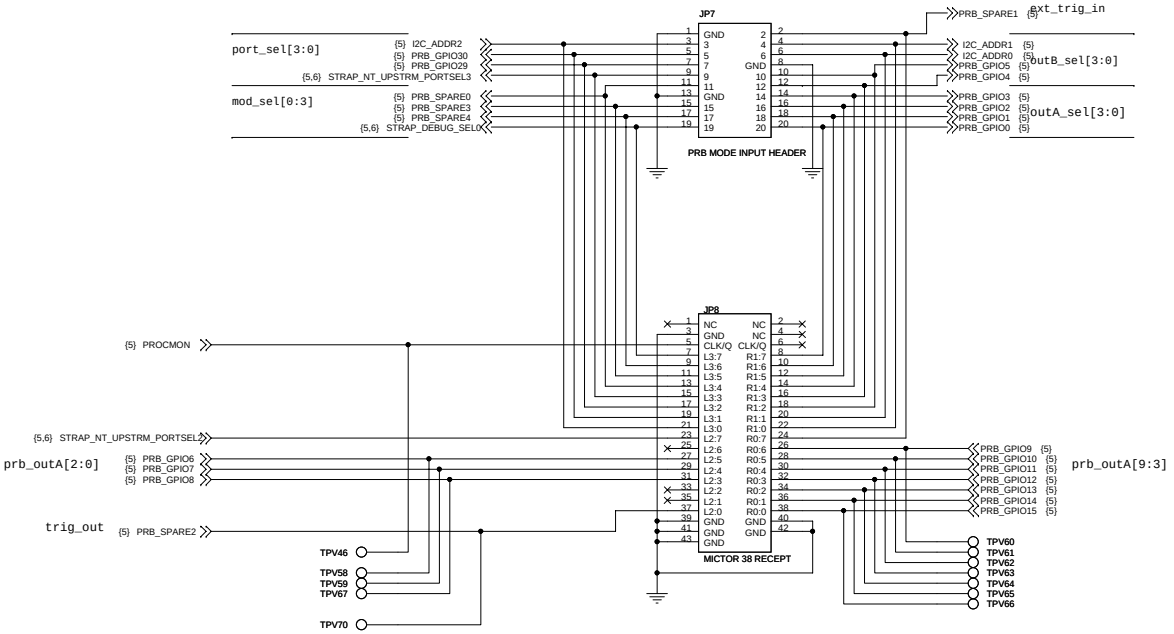
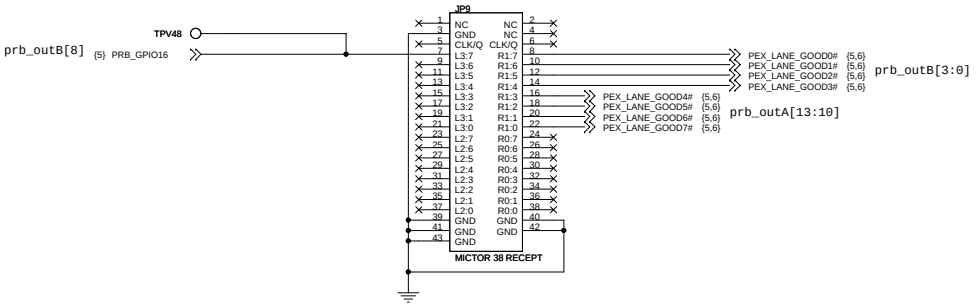
PROBE MODE INPUTS



PROBE MODE OUTPUTS



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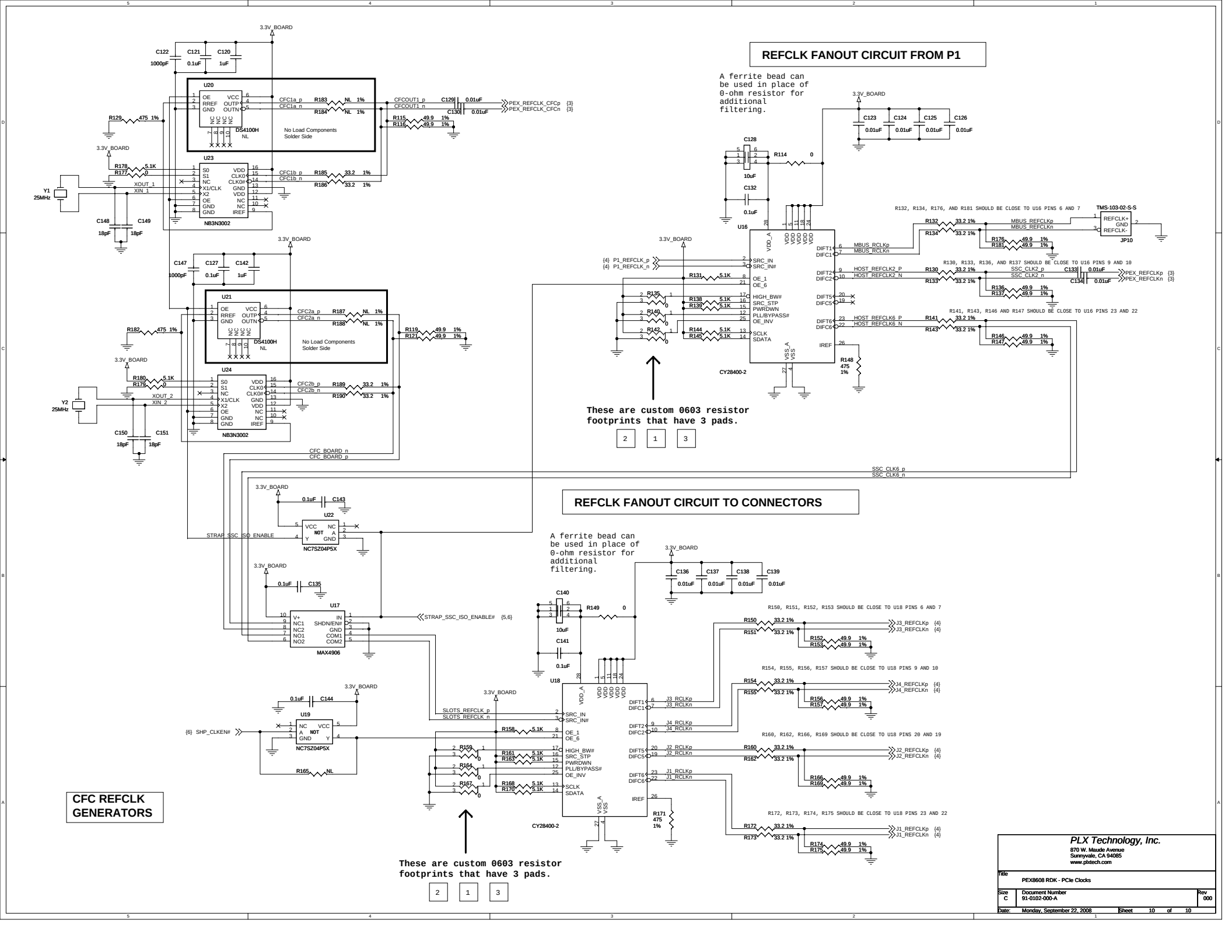
Title	PEX8608 RDK - Probe Mode Interface	
Size: C	Document Number: 91-0102-000-A	Rev: 000
Date: Monday, September 22, 2008	Sheet 9 of 10	


REFCLK FANOUT CIRCUIT FROM P1
REFCLK FANOUT CIRCUIT TO CONNECTORS
CFC REFCLK GENERATORS
A ferrite bead can be used in place of 0-ohm resistor for additional filtering.
No Load Components Solder Side
These are custom 0603 resistor footprints that have 3 pads.
R132, R134, R176, AND R181 SHOULD BE CLOSE TO U16 PINS 6 AND 7
R130, R133, R136, AND R137 SHOULD BE CLOSE TO U16 PINS 9 AND 10
R141, R143, R146 AND R147 SHOULD BE CLOSE TO U16 PINS 23 AND 22
R150, R151, R152, R153 SHOULD BE CLOSE TO U18 PINS 6 AND 7
R154, R155, R156, R157 SHOULD BE CLOSE TO U18 PINS 9 AND 10
R160, R162, R166, R169 SHOULD BE CLOSE TO U18 PINS 20 AND 19
R172, R173, R174, R175 SHOULD BE CLOSE TO U18 PINS 23 AND 22
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PEX8608 RDK - PCIe Clocks
Document Number 91-0102-000-A
Rev 000
Monday, September 22, 2008
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