RaggedStone2 User Manual

Issue – 1.02

Kit Contents

You should receive the following items with you Raggedstone2 development kit:

1 - Raggedstone2 Board
2 - 4 Digit, 7 Segment LED display (usually fitted)
3 – PCI mounting bracket (usually fitted)
3 – Prog2 (parallel port) or Prog3 (USB) programming cable

Contents

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR RAGGEDSTONE2 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

Trademarks

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Raggedstone2 is a trademark of Enterpoint Ltd.

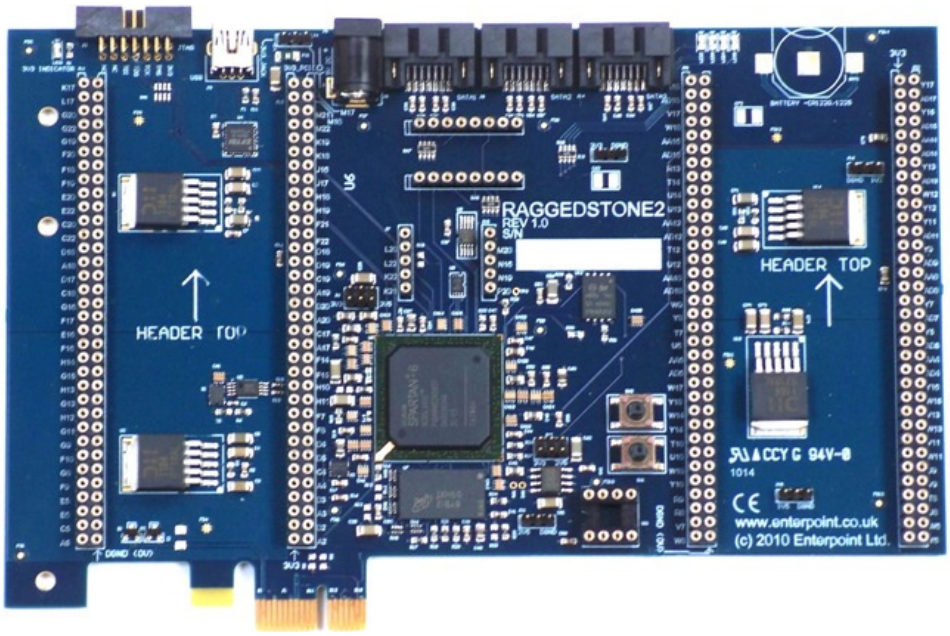


Figure 1 – Raggedstone2 Board.

Introduction

Welcome to your Raggedstone2 board. Raggedstone2 is X1 PCIe development board based on a single Xilinx™ Spartan™-6 FPGA. This product has been designed as a migration product for users of our highly popular Raggedstone1 board with a high degree of feature and mechanical compatibility.

The aim of this manual is to assist in using the main features of Raggedstone2. It is aimed as a basic manual and may not cover in sufficient depth some of the advanced features of this product. Our support team can be contacted on support@enterpoint.co.uk for information beyond the scope of this manual.

Raggedstone2 is initially offered in a single variant based on an XC6SLX45T-4FGG484C Spartan™-6. We will offer options subject to demand including bigger, faster and industrial grade FPGAs. Please ask our board sales team boardsales@enterpoint.co.uk to quote for any specific requirements.

As with all of our products we can offer OEM customers semi custom, or full custom, derivative designs based on this product. Please ask our board sales team boardsales@enterpoint.co.uk to quote for custom derivative products.

In addition Raggedstone2 is supported by our wide range of add-on modules. Some examples of these include:

ADC 7927 MODULE
LED DOT MATRIX MODULE
BUTTONS/SWITCHES/SATA/MEMORY MODULE
RS232 AND RS485 HEADER MODULES
DP83816 ETHERNET MODULE
SD CARD MODULE
DDR2 MODULE
IDE/5V TOLERANT CPLD MODULE
USB MODULE
D/A CONVERTER MODULE
ADV70202 MODULE

We can also offer custom DIL Header modules should you require a function not covered by our current range of modules. Typical turn around for this service is 4-8 weeks depending upon quantity ordered and availability of components.

Raggedstone2 Main Features

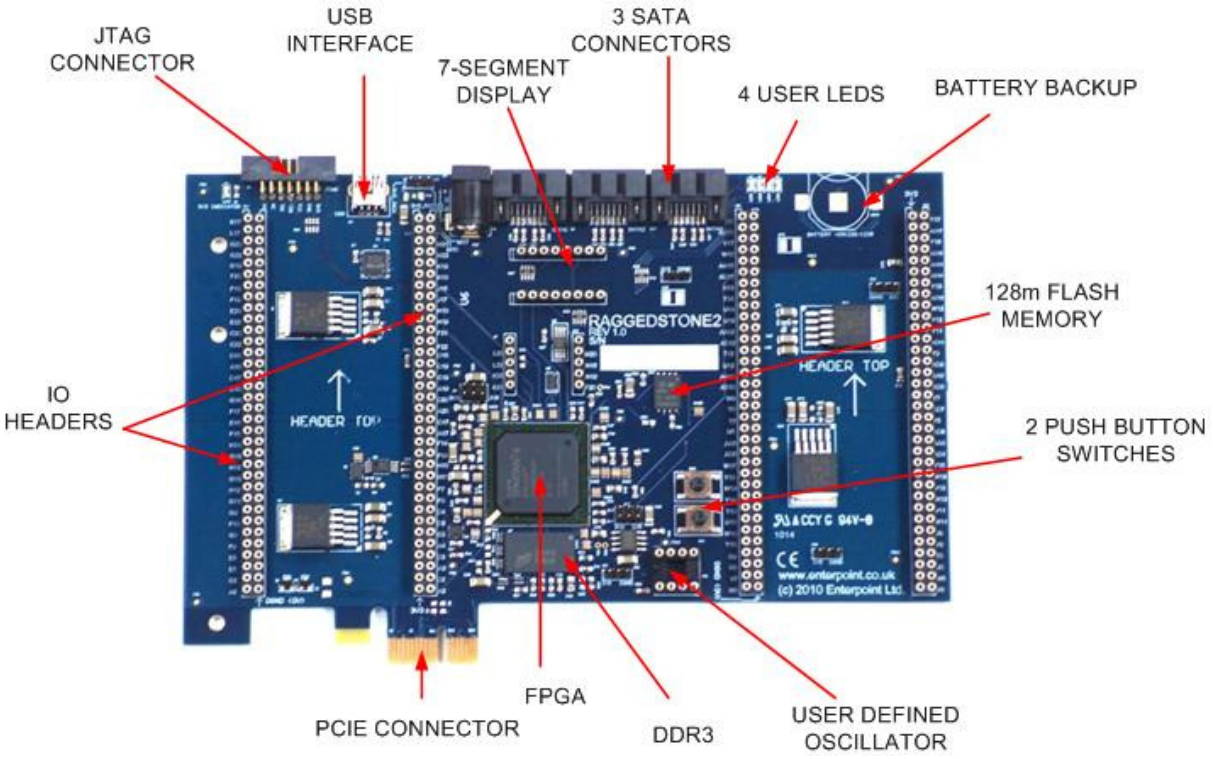


Figure 2 – Raggedstone2 MAIN FEATURES.

Getting Started

Your Raggedstone2 will be supplied with a default setting of jumpers fitted.

(1) Please read the entire user manual.

(2) Fit the LED 7 segment display into its connector if needed.

(3) Check the bank voltage jumper selections are set as required by your application.

(4) Check that power selection header J4 has a jumper fitted as appropriate for PC hosting or stand alone bench operation.

(5) Fit an oscillator into the DIL socket if needed.

(6) Either plug the Raggedstone2 board into a un-poweredPCIe host connector or alternatively plug in a 5V power supply into the 2.1mm Jack socket.

(7) Switch on you host system with PCIe connector or switch on your 5V power supply.

Selecting the FPGA Bank voltages.

The main User I/O pins of the Spartan™-6 on Raggedstone2 are divided into 2 banks. The left hand side header pins are routed to BANK1 of the FPGA, the Right hand side headers are routed to BANK2. The IO voltages are usually set to either 3.3V or 2.5V using jumpers on the 6-pin headers J6 for BANK1 and J12 for BANK2. Alternatively a user-generated Bank IO voltage could be introduced on pin 2 of J6 or J12. There is a DGND (0V) reference on pin 5 of J6 and J12 for this purpose. If you choose to use this option please refer to the Spartan™-6 user guide from www.Xilinx.com to check the allowed IO voltage range for the FPGA.

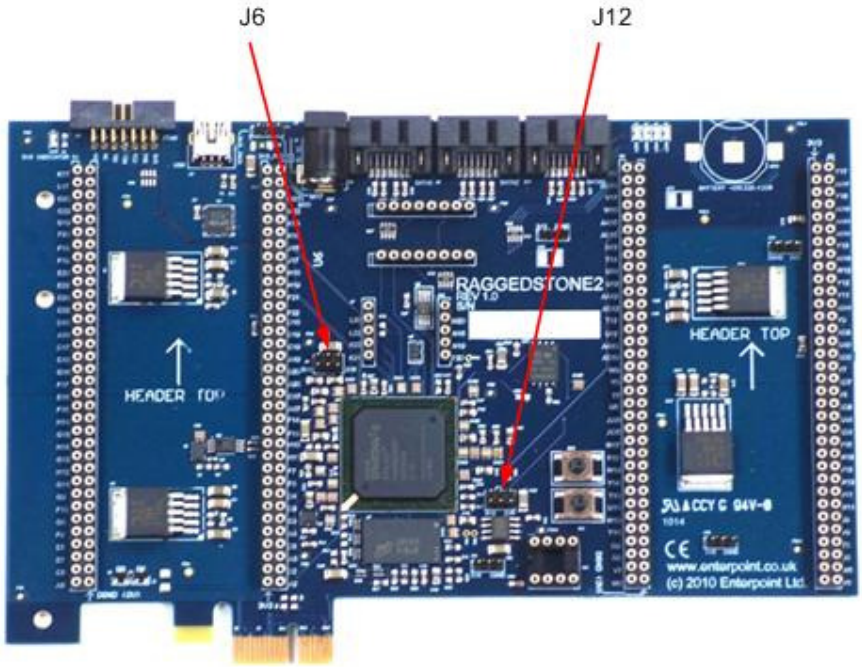


Figure 4 – Raggedstone2 VCCO SUPPLY FEATURES.

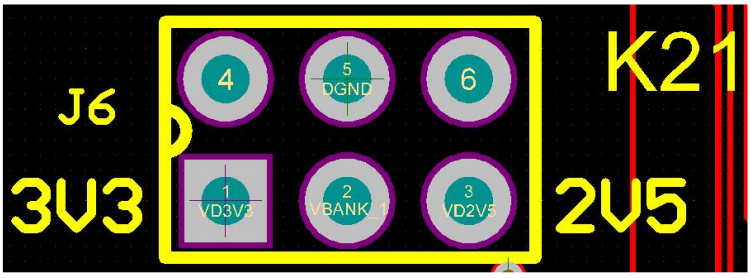


Figure 4a – Pin allocation of J6 (J12 is identical)

Programming Raggedstone2

The programming of the FPGA and SPI Flash on Raggedstone2 is achieved using a JTAG connection. Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx™ ISE™ software although other alternatives do exist. Our Prog2 (parallel port) or Prog3 (USB) programming cables are normally supplied with this board unless your ware buying OEM versions where cables are not supplied.

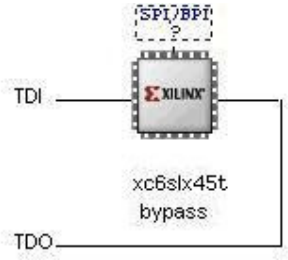
There is a single JTAG chain on Raggedstone2. The JTAG chain allows the programming of the Spartan™-6 and the SPI Flash device.

The JTAG connector has a layout as follows:

Top edge of board

GND	GND	GND	GND	GND	GND	GND
NC	NC	TDI	TDO	TCK	TMS	3V3

Using the ISE IMPACT tool the boundary scan the JTAG chain appears like this:



Programming the FPGA directly.

Direct JTAG programming of the Spartan™-6 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).

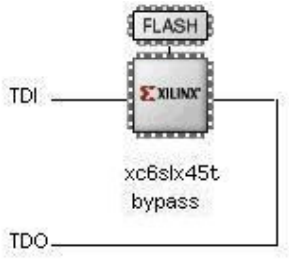
Bit files are usually used for direct JTAG programming and these are generated by the Xilinx™ ISE™ tool chain. This powerful set of tools is available from Xilinx™. The free ISE™ Webpack™ version will support XC6SLX45T and XC6SLX75T based versions of Raggedstone2. Versions of Raggedstone2 using XC6SLX100 and XC6SLX150 will need a paid license version of ISE™ to build, and program, the internal FPGA design.

Once you have built the design in ISE™ click on program device to open the Impact™ part of the ISE™ toolset. Once you have selected boundary scan mode and Initialised the chain you should see FPGA portrayed as shown above. Right click the icon representing the Spartan™-6 FPGA and choose ‘Assign New Configuration File’. Navigate to your .bit file and choose ‘OPEN’. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Spartan™-6 FPGA and choose ‘Program’. On the next dialogue box ensure that the ‘Verify’ box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Spartan™-6 will program. This process is very quick and is typically a few seconds.

Programming the SPI flash memory using Boundary Scan

Once the SPI Flash memory has been programmed, the Spartan™-6 device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE IMPACT's Prom File Formatter mode.

Right click on the icon representing the Spartan™-6 and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. Data width should be set to 1.The flash memory should appear as shown below.



Right click on the icon representing the flash memory and choose 'Program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase before programming' are chosen. Otherwise all defaults can be accepted. The programming operation will take some time. This time depends on which programming cable you use and it's setup but typically expect this to take 3 to 4 minutes.

Field Updating the SPI flash via USB Serial Interface or Other Interface

It is possible to update the Raggedstone2 via it's FT232 USB, or other, interface if a basic build supporting a field updating mode has been previously loaded into the Raggedstone2. It is also possible to Multiboot the Spartan™-6 FPGA with bitstream loaded dependent on a switch or other stimulus. These advanced topics are not covered in this manual and are only mentioned here for completeness. We are hoping to provide further information on this in our TechiTips section of our Engineering Website.

Bitstream Encryption

Raggedstone2 can support bitstream encryption on versions of the board with XC6SLX75T, XC6SLX100T or XC6SLX150T FPGAs fitted. **XC6SLX45T versions of the product do not support bitstream encryption.**

Raggedstone Features

Power Inputs and Pick-ups

Raggedstone2 can be powered either from the PCIe edge connector or from a single 5V power supply input via the 2.1mmDC jack socket.

The 5V DC jack input to Raggedstone2 is initially regulated down to 3.3V by an AP1184 regulator. The resultant 3.3V is fed to power selection header.J4 located between the USB connector and 5V Jack. Fitting a jumper between Pin1 and Pin2 selects the 5V DC Jack feed derived 3.3V. Fitting the jumper between Pins 2 and 3 selects the PCIe 3.3V input.

The 3.3V output of J4 then acts as the main 3.3V for the board and also the main power feed to the regulators for 1.2V, 1.5V and 2.5V. A pair of low current control voltage rails are also produced by diode ORs of 12V (PCIe) and 5V (Jack) for use at the main regulators.

On Raggedstone2 there are 2 sets of 34 header pins with 3.3V and DGND (0V) available on each side of the board for users to access power for their own add-on circuitry. These pins are arranged on a 0.1inch grid to enable users to plug in their own strip-board designs or even custom add-on PCBs.

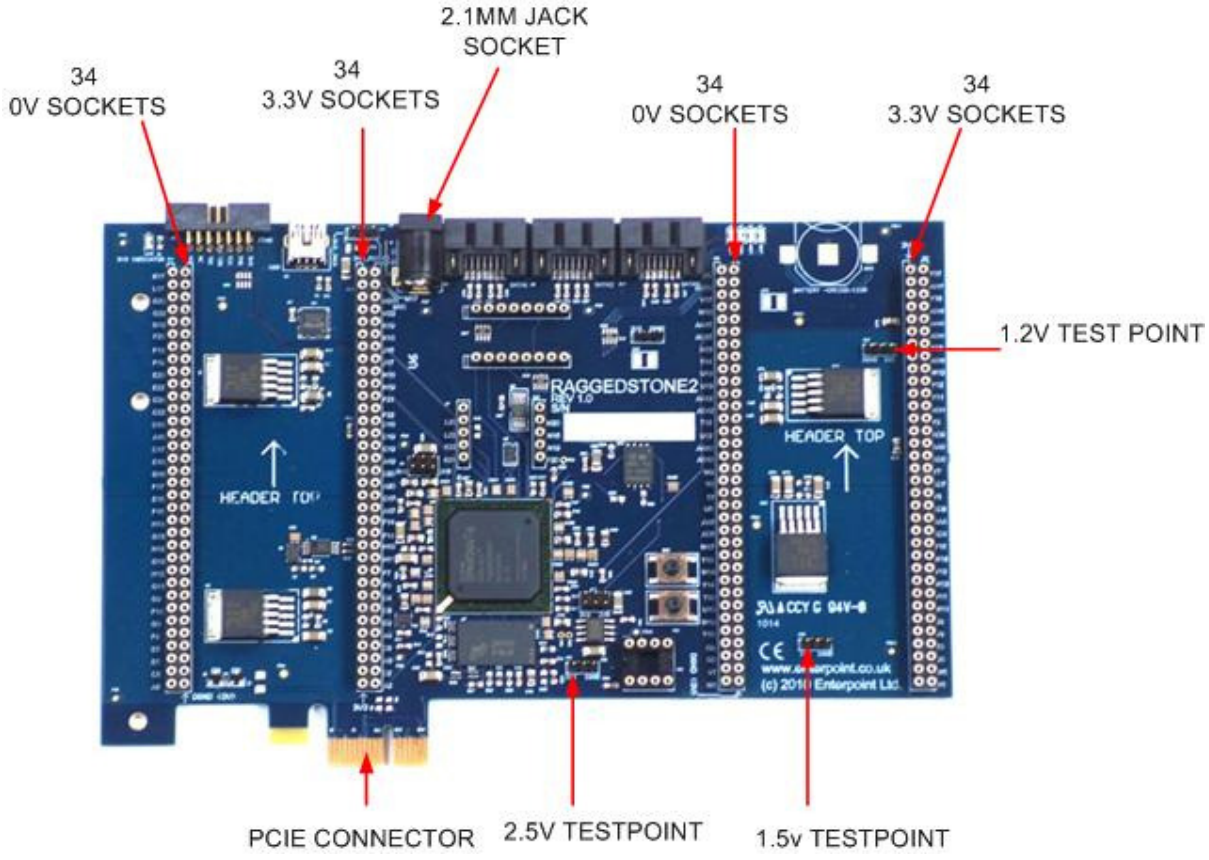


Figure 3 – Raggedstone2 Power Supply Features

WARNING – THE REGULATORS, AND SURROUNDING PCB, MAY BECOME HOT WHILST IN NORMAL OPERATION.

Power Regulators

Raggedstone2 has a power backbone based on four AP1184 linear regulators. These regulators are each capable of delivering 4 amps. The structure of the regulator circuit limits the maximum power drawn from the supply and minimises losses by regulating the 5V or 12v PCIe supply to 3.3V, which is then used to supply the 1.2V, 1.5V and 2.5V regulators. The maximum current that can be delivered into Raggedstone2 has also been limited by a resettable fuse to a maximum current to 1.1A at 3.3V through to the board. This limit should be considered when adding user circuitry onto the header pins.

If more current is drawn the resettable fuse will cut the supply to the board, if this happens the power supply must be switched off and time given for the fuse to reset, which occurs when the fuse has cooled and reconnected its internal contacts. This typically takes 1-2 seconds.

A fifth regulator (LP2996) provides a 0.75V reference for the DDR3 memory device.

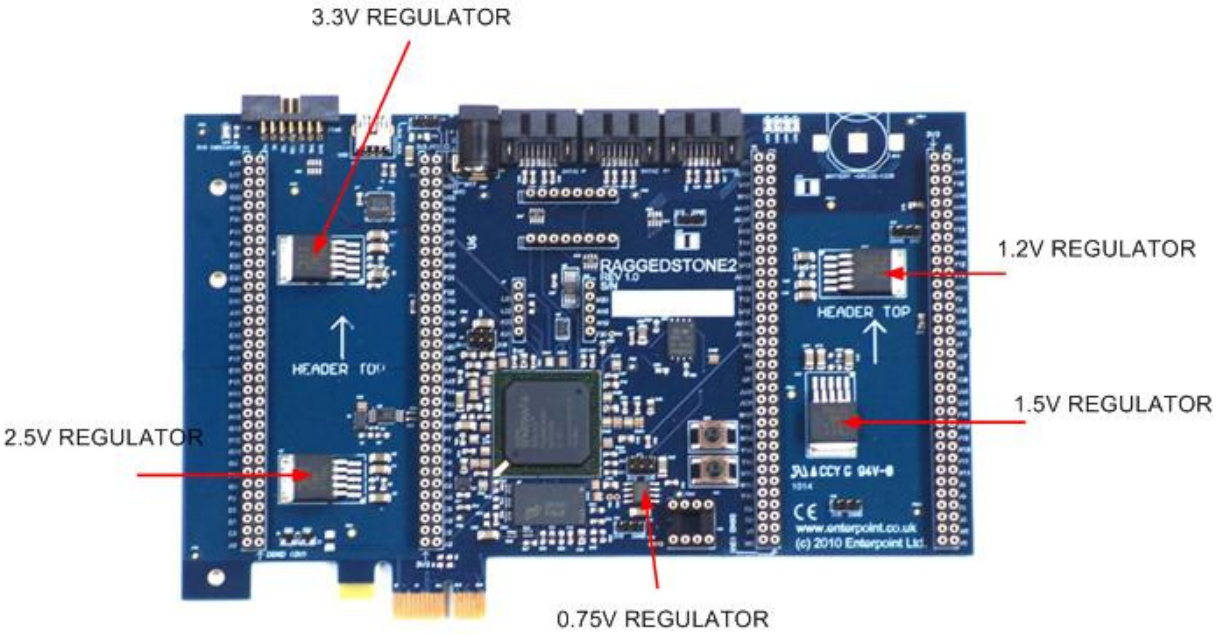


Figure 6 – Raggedstone2 POWER REGULATION.

DIL Headers

The DIL Headers provide a simple mechanical and electrical interface for add-on modules. The connectors on this header are on a 0.1inch, 2.54mm, pitch and allow either custom modules or strip board to be fitted. The headers have a row of permanent positive power sockets (3.3V) to the left of JL2 and JR2 and a row of permanent GND (DGND (0V)) sockets to the right of the JL1 and JR1.

Voltages outside the range 0V to 3.3V must not be applied to the DIL headers. The Spartan™-6 has an absolute maximum IO input voltage of 4.1V. The connections between the DIL the headers and the FPGA are shown below:

LEFT DIL HEADER				RIGHT DIL HEADER			
JL1		JL2		JR1		JR2	
K17	DGND	3.3V	M17	AA18	DGND	3.3V	Y17
L17	DGND	3.3V	M18	AB18	DGND	3.3V	AB17
G20	DGND	3.3V	M21	V17	DGND	3.3V	Y15
G22	DGND	3.3V	M22	W18	DGND	3.3V	AB15
G19	DGND	3.3V	K19	AA16	DGND	3.3V	AA14
F20	DGND	3.3V	K18	AB16	DGND	3.3V	AB14
F18	DGND	3.3V	J16	R13	DGND	3.3V	Y13
F19	DGND	3.3V	J17	T14	DGND	3.3V	AB13
E20	DGND	3.3V	H18	U14	DGND	3.3V	W12
E22	DGND	3.3V	H19	U13	DGND	3.3V	Y12
C20	DGND	3.3V	F21	AA12	DGND	3.3V	Y11
C22	DGND	3.3V	F22	AB12	DGND	3.3V	AB11
B18	DGND	3.3V	D18	T12	DGND	3.3V	Y9
A18	DGND	3.3V	D19	U12	DGND	3.3V	AB9
D17	DGND	3.3V	C19	AA10	DGND	3.3V	AA8
C18	DGND	3.3V	A19	AB10	DGND	3.3V	AB8
G16	DGND	3.3V	B20	W9	DGND	3.3V	T7
F17	DGND	3.3V	A20	Y8	DGND	3.3V	U6
E16	DGND	3.3V	C17	Y7	DGND	3.3V	Y5
F16	DGND	3.3V	A17	AB7	DGND	3.3V	AB5
H14	DGND	3.3V	F14	AA6	DGND	3.3V	AA4
G15	DGND	3.3V	F15	AB6	DGND	3.3V	AB4
H13	DGND	3.3V	H10	W17	DGND	3.3V	Y16
G13	DGND	3.3V	H11	Y18	DGND	3.3V	W15
H12	DGND	3.3V	F7	W14	DGND	3.3V	V13
G11	DGND	3.3V	F8	Y14	DGND	3.3V	W13
G9	DGND	3.3V	D4	T10	DGND	3.3V	V11
F10	DGND	3.3V	D5	U10	DGND	3.3V	W11
G8	DGND	3.3V	C4	W10	DGND	3.3V	U9
F9	DGND	3.3V	A4	Y10	DGND	3.3V	V9
E5	DGND	3.3V	B3	R9	DGND	3.3V	T8
E6	DGND	3.3V	A3	R8	DGND	3.3V	U8
C5	DGND	3.3V	B2	V7	DGND	3.3V	W6
A5	DGND	3.3V	A2	W8	DGND	3.3V	Y6

The signals on the DIL headers are arranged in LVDS pairs and routed such that the trace lengths approximately match and skew is minimised within pair. Adjacent LVDS_P and LVDS_N form the matched pair at the DIL Header and the Spartan™-6 FPGA. For example K17 and L17 form one pair.
All LVDS pairs can be used as general inputs/outputs from the Spartan6.

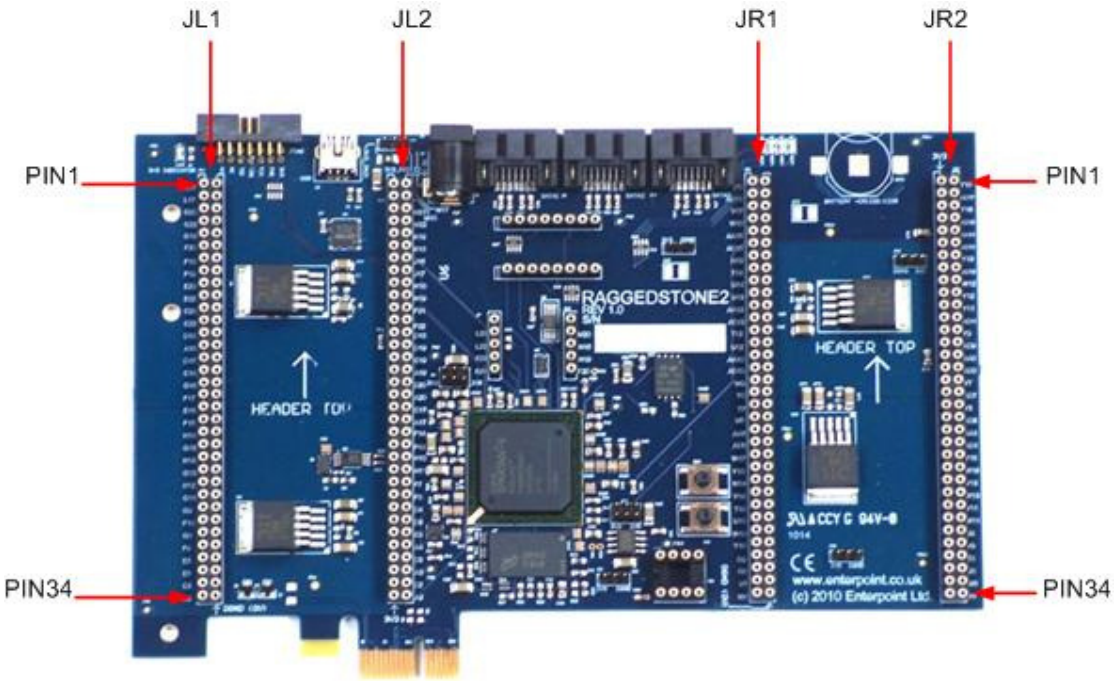


Figure 7 – Raggedstone2 DIL Headers

SIL Headers

There are 4 SIP headers on Raggedstone2. They are arranged as 2 pairs. J7 and J10 form the Clock Module header and have 5 pins each. The two 8-pin SIL headers are usually used to support the LTC-C4627JR 4-digit 7-segment display (U6), however the 7 segment display can be removed to make these pins available to the user. Voltages outside the range 0V to 3.3V must not be applied to the SIL headers. The Spartan™-6 has a maximum IO input voltage of 4.1V.

1. CLOCKMODULE HEADER

These header pins are designed to allow the Enterpoint Clock module to be fitted. This module is fitted with an ICS8442 700MHZ, Crystal Oscillator-To-Differential Lvds Frequency Synthesizer device. If this module is not fitted the header pins are available to the user.

J10 has a permanent positive power pin (3V3) at the top position. J7 has a Gnd (DGND (0V)) connection at the top position. The connections to the FPGA (BANK1) are shown below:

J7			J10	
PIN1	DGND		PIN1	3.3V
PIN2	L20		PIN2	M20
PIN3	L22		PIN3	N16
PIN4	K22		PIN4	N19
PIN5	K21		PIN5	P20

The connections to J7 are LVDS pairs connecting to Global Clock inputs on the FPGA. On J10 connections to N19 and P20 are an LVDS pair and Global Clock inputs. The Connections to M20 and N16 are to general purpose IO pins.

The horizontal distance between J7 and J10 is 0.6inch (15.25mm).

2. 7-SEGMENT DISPLAY HEADER

The two 8-pin headers which form the 7-segment display holder U6 have 14 connections to the FPGA. Of these 14 connections 8 have series 470ohm resistors, which are normally used as current-limiting resistors for the 7 segment display.This should be taken into account if this header is used for other purposes. The connections between U6 and the FPGA are shown below:

PIN16 N20	PIN15 P19	PIN 14 R19	PIN13 R20	PIN12 T20	PIN11 V20	PIN10 N/C	PIN9 N/C
PIN1 N22	PIN2 T22	PIN3 V19	PIN4 P16	PIN5 U20	PIN6 U19	PIN7 V21	PIN8 AB19

It should be noted that AB19 is on BANK2, All the other connections are on BANK1.

The vertical distance between the upper and lower pins of U6 is 0.4inch (10.2mm).

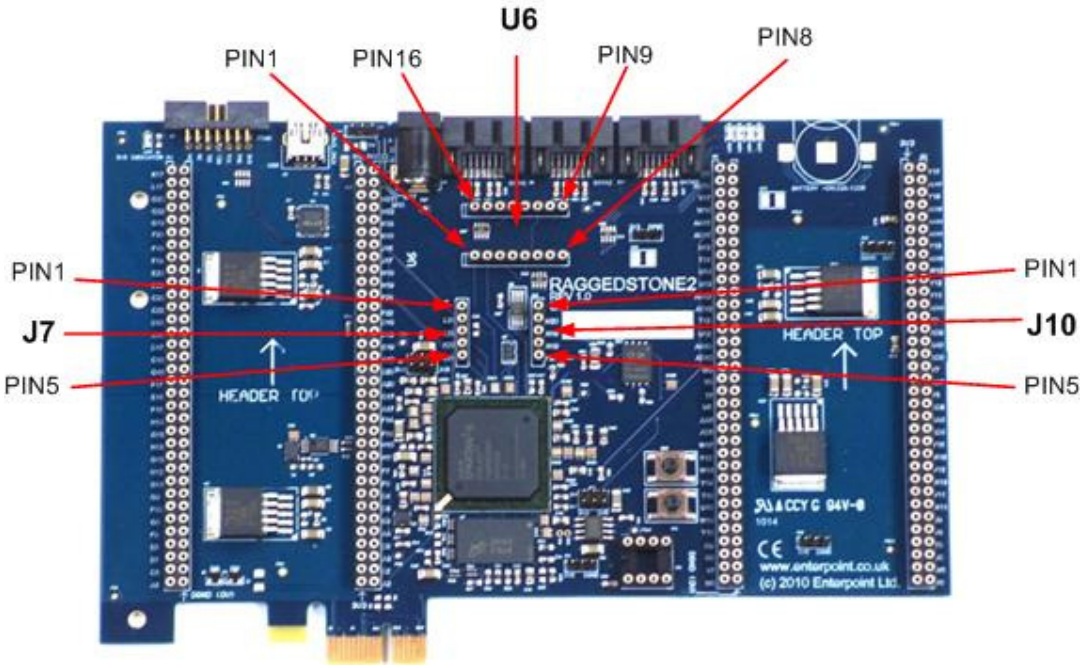


Figure 8 – Raggedstone2 SIL Headers

FPGA

Raggedstone2 supports Spartan™-6 devices in the FGG484 package. Raggedstone2 is normally available with the XC6SLX45T-4FGG484C fitted, which has 43,661 logic cells. Should you have an application that needs bigger devices, industrial or faster speed grades please contact sales for a quote at boardsales@enterpoint.co.uk

Oscillator

The oscillator socket on Raggedstone2 supports 3.3V, 8-pin DIL outline, oscillator crystals. The on board clock signal is routed directly through to the FPGA (pin **M19**) which is a Global Clock input to the FPGA.

The Spartan™-6 has Digital Clock Multipliers (DCMs) to produce multiples, divisions and phases of clock signals. Please consult the Spartan™-6 datasheet available from the Xilinx™ website at http://www.Xilinx.com if multiple clock signals are required.

LEDs

On Raggedstone2 there are 5 LEDS. LED1 is situated on the top left corner of the board and isindicates the presence of the 3.3V power rail. It is not available for other uses. LEDs 2 to 5, which are situated the top of the board between the rightmost SATA connectors and the Battery holder, are user LEDs and are connected to the FPGA as indicated below:

LED2	LED3	LED4	LED5
W22	W20	Y22	Y21

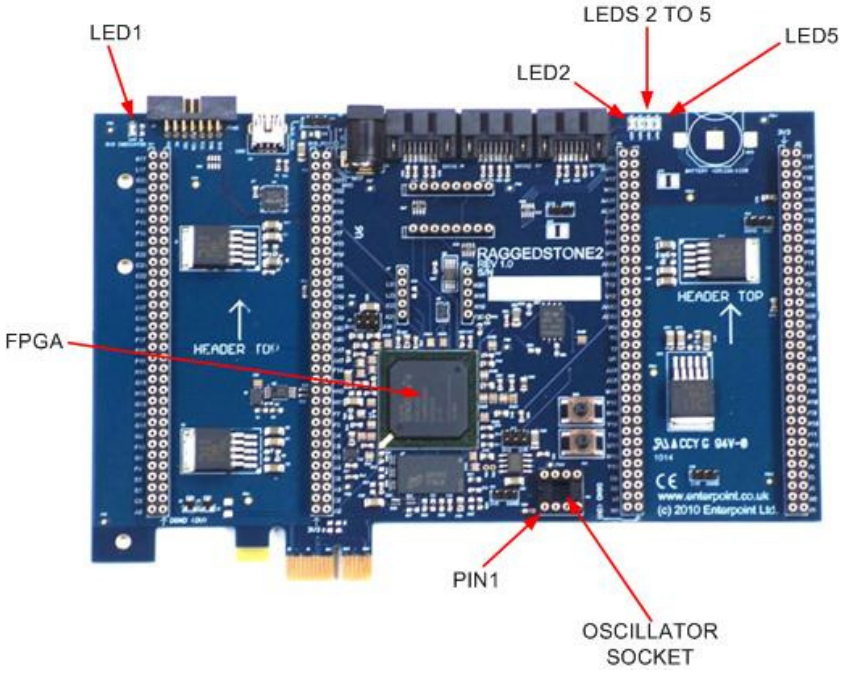
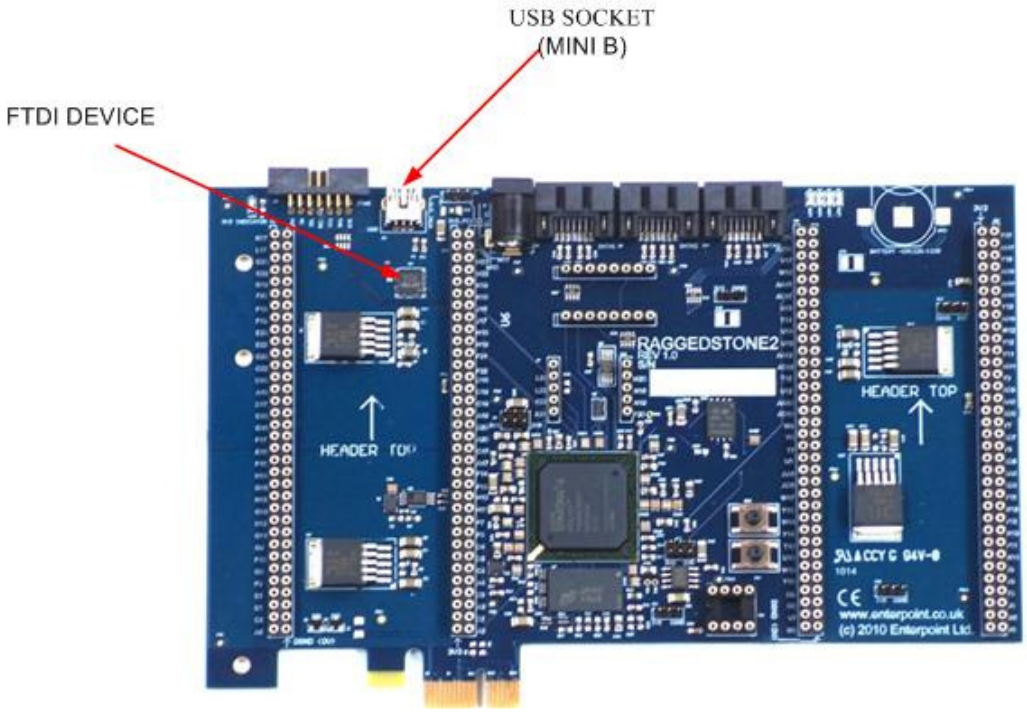


Figure 8 – Raggedstone2 FPGA, Oscillator socket and LEDs

USB



The USB interface on the Raggedstone2 is achieved using an FT232R USB to serial UART interface. The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed the Raggedstone2 USB port should be detected as a serial port. Alternative data optimised drivers are also available from FTDI.

The FT232R is connected to the Spartan™-6 and provided a simple UART, or other converter, is implemented then the data sent over the USB serial port can be used either as control and/or data information. This allows a host computer to act in a number of ways including system control and data storage functions.The connections between the USB device and the FPGA are shown below:

FT232R	FPGA PIN
CTS#	L19
DCD#	K20
DSR#	J19
RI#	J22
RTS#	H20
DTR#	H22
TXD	H21
RXD	J20

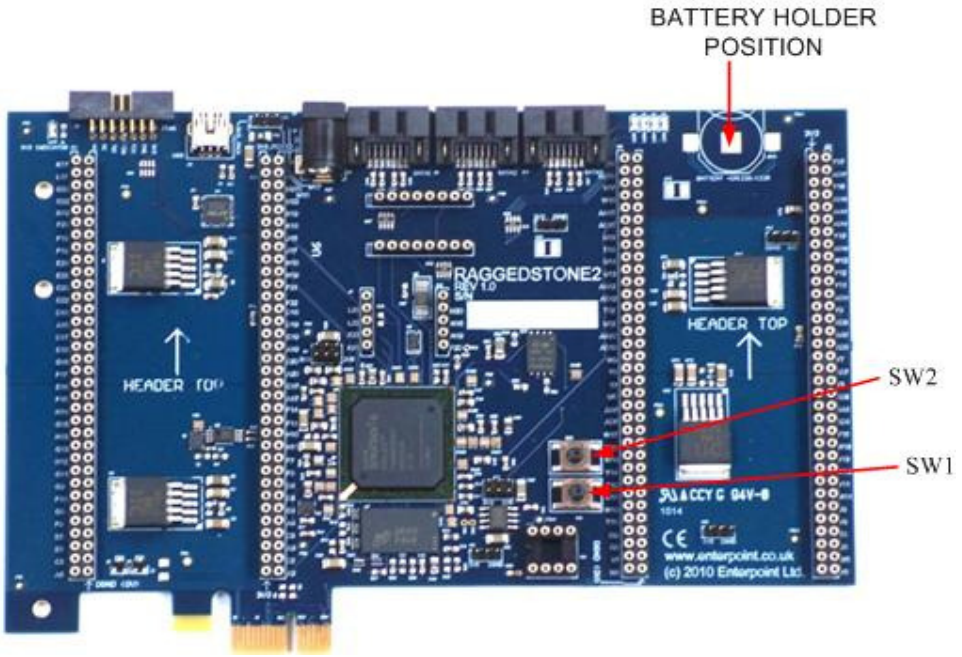
Push Button Switches

Raggedstone2 has two tactile push-button switches. To use these switches it is necessary to set the IO pins connected to the switches to have a pull up resistor setting in the constraints file. Any switch pressed, or made, will then give a LOW signal at the FPGA otherwise a HIGH is seen. The two push button switches are connected to the following IO pins.

SWITCH 1	SWITCH 2
R7	W4

Battery Backup

The Raggedstone2 has a battery holder which is available to provide battery backup to the FPGA. It is connected to the Spartan™-6 on pin T16. The battery holder accepts a 3V Lithium battery size CR1220 or equivalent.



DDR3

Raggedstone2 has a 1GBIT DDR3 Micron MT41J64M16LA device as standard. This device is organised as 8 Meg x 16 x 8 banks. This device is supported by the hard core memory controller that is in the Spartan™-6 FPGA. To add this core to your design the COREGEN tool, part of the ISE suite, will generate implementation templates in VHDL or Verilog for the configuration that you want to use. More details on the memory controller can be found in the user guide http://www.Xilinx.com/support/documentation/user_guides/ug388.pdf.

For OEM applications we can fit bigger DDR3 parts subject to limitations of the memory controller.

The DDR3 has 12 address lines and 16 data lines to address all the available memory, which can be accessed at speeds of 1.87ns. More details of the DDR3 can be found in http://download.micron.com/pdf/datasheets/dram/ddr3/1Gb_DDR3_SDRAM.pdf.
The DDR3 site has the following connections to the FPGA:

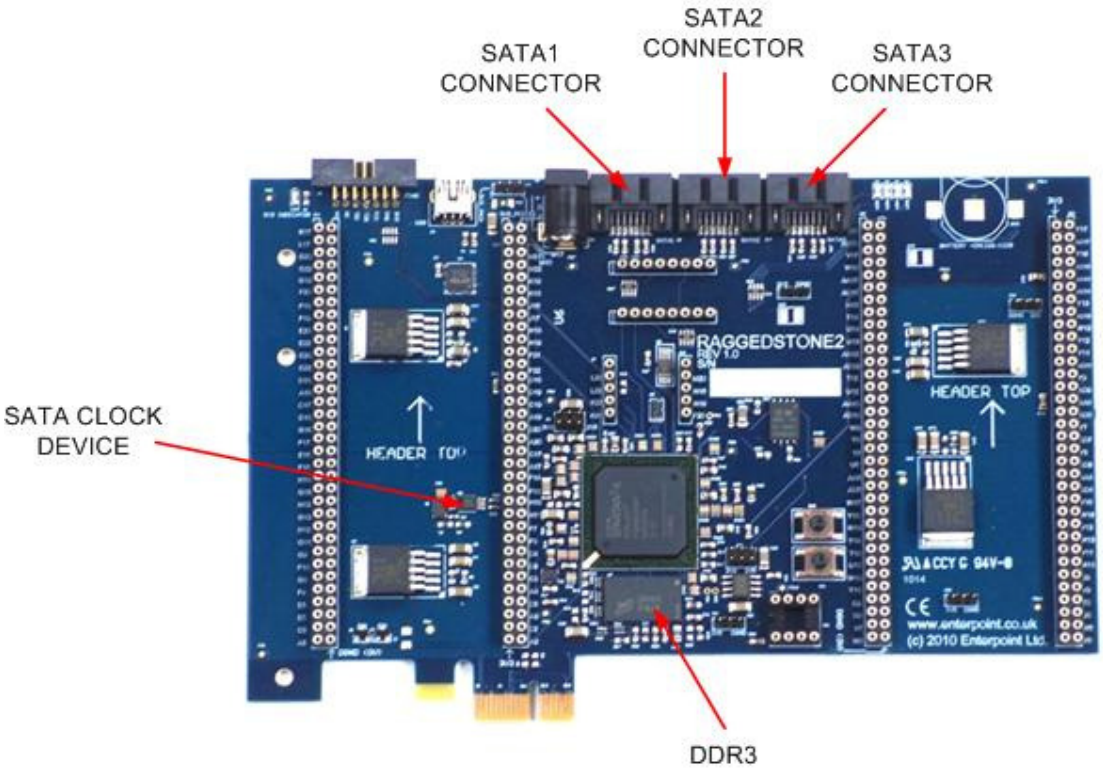
DDR3 FUNCTION	FPGA PIN	DDR3 FUNCTION	FPGA PIN
DDR_A0	K2	DDR_DQ3	P1
DDR_A1	K1	DDR_DQ4	L3
DDR_A2	K5	DDR_DQ5	L1
DDR_A3	M6	DDR_DQ6	M2
DDR_A4	H3	DDR_DQ7	M1
DDR_A5	M3	DDR_DQ8	T2
DDR_A6	L4	DDR_DQ9	T1
DDR_A7	K6	DDR_DQ10	U3
DDR_A8	G3	DDR_DQ11	U1
DDR_A9	G1	DDR_DQ12	W3
DDR_A10	J4	DDR_DQ13	W1
DDR_A11	E1	DDR_DQ14	Y2
DDR_A12	F1	DDR_DQ15	Y1
DDR_A13	J6	DDR_LDM	N4
DDR_A14	H5	DDR_LDQS	N3
DDR_A15	D1	DDR_LDQS_N	N1
DDR_BA0	J3	DDR_UDM	P3
DDR_BA1	J1	DDR_UDQS	V2
DDR_BA2	H1	DDR_UDQS_N	V1
DDR_CS_N	P4	DDR_ODT	L6
DDR_RAS_N	M5	DDR_CAS_N	M4
DDR_WE_N	H2	DDR_RESET_N	E3
DDR_DQ0	R3	DDR_CKE	F2
DDR_DQ1	R1	DDR_CLK_N	K3
DDR_DQ2	P2	DDR_CLK	K4

The signals shown shaded in yellow are terminated using suitable arrangements of resistors.

SATA

Raggedstone2 has 3 SATA connectors which are connected to the MGT interface of the Spartan6. An ICS844071 is used to generate the SATA Clock. The connections between the SATA Clock, the SATA connectors and the FPGA are shown below (omitting series capacitors):

Sata1 ConnectorJ8 pin	FPGA PIN	Sata2 Connector J9 Pin	FPGA PIN	Sata3 Connector J14 Pin	FPGA PIN
J8 PIN 2	D9	J9 PIN 2	D13	J14 PIN 2	C15
J8 PIN 3	C9	J9 PIN 3	C13	J14 PIN 3	D15
J8 PIN 5	A8	J9 PIN 5	A14	J14 PIN 5	A16
J8 PIN 6	B8	J9 PIN 6	B14	J14 PIN 6	B16
CLOCK+	C11	CLOCK+	A12	CLOCK+	E12
CLOCK-	D11	CLOCK-	B12	CLOCK-	F12



PCIe Edge Connector

The Raggedstone2 has a x1 PCIe Interface. The pin out of the Spartan™-6 FPGA has been chosen such that the PCI interface follows the pinout for the Xilinx™ Spartan™-6 hard core for PCIe which can be generated automatically by the Xilinx™ Core Generator.

The connections between the PCIe connector and the FPGA are shown below.

SIGNAL NAME	PCIE CONNECTOR PIN	FPGA PIN
PCIE_CLK_P	A13	A10
PCIE_CLK_N	A14	B10
PCIE_TX_P	A16	B6
PCIE_TX_N	A17	A6
PCIE_RX_P	B14	D7
PCIE_RX_N	B15	C7
PCIE_PRESENT#1	A1	P5
PCIE_PRESENT#2	B17	P5

Serial EEPROM

Raggedstone2 has a 16K Two-Wire Atmel AT24C16BY6 EEPROM device which uses a simple Parallel address and single serial data line and clock. There is also a write protect line which can be used to electronically safeguard the information contained in the device

The EEPROM has 3 address lines which are permanently connected to DGND. It can run at speeds up to 400 kHz. This serial memory has 2048 words of 8 bits and employs a byte or page programming system. The connections between the EEPROM and the FPGA are shown below:

EEPROM SIGNAL	FPGA PIN
SDA	P22
SCL	P21
WP	R22

SPI Flash Memory

The M25P128 SPI flash memory device configures the FPGA when it is powered providing a suitable bitstream is programmed into the device. The M25P128 has a capacity of 128Mbits with a single configuration bitstream for Raggedstone2 taking between 3.6Mbits (LX16) and 11.4Mbits (LX45). Any remaining space can be used for alternative configurations or code and data storage.

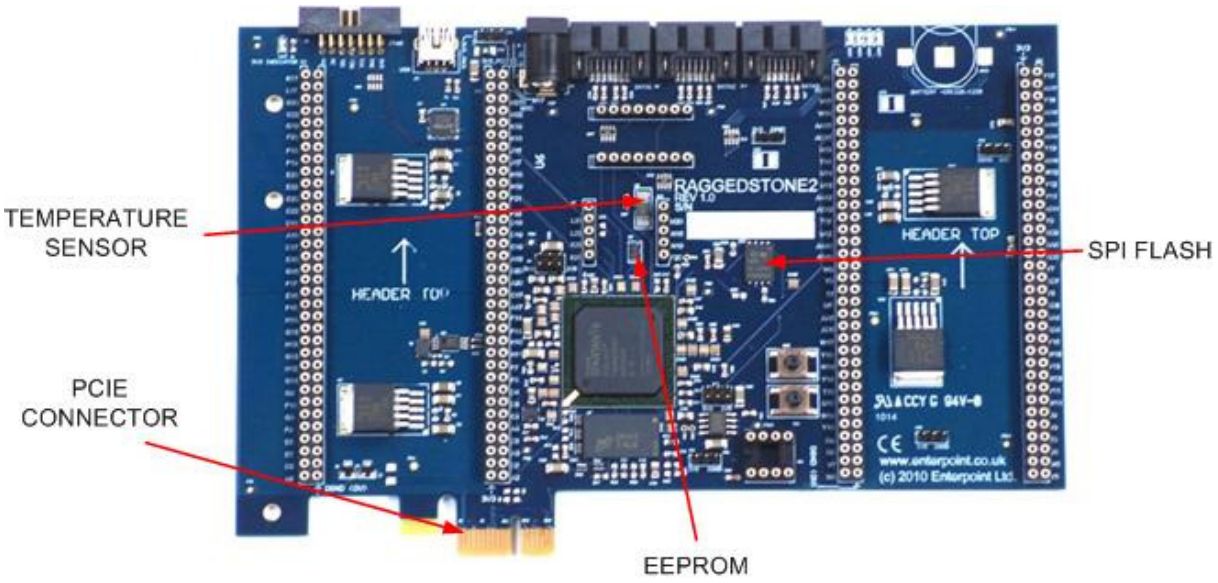
The HOLD pin of this memory device is permanently connected to 3.3V. After configuration the SPI Flash can be accessed via the following pins of the FPGA:

M25P128 FUNCTION	FPGA PIN
CCLK	Y20
MOSI	AB20
WRITE	D3
DIN	AA20
CSO_B	AA3

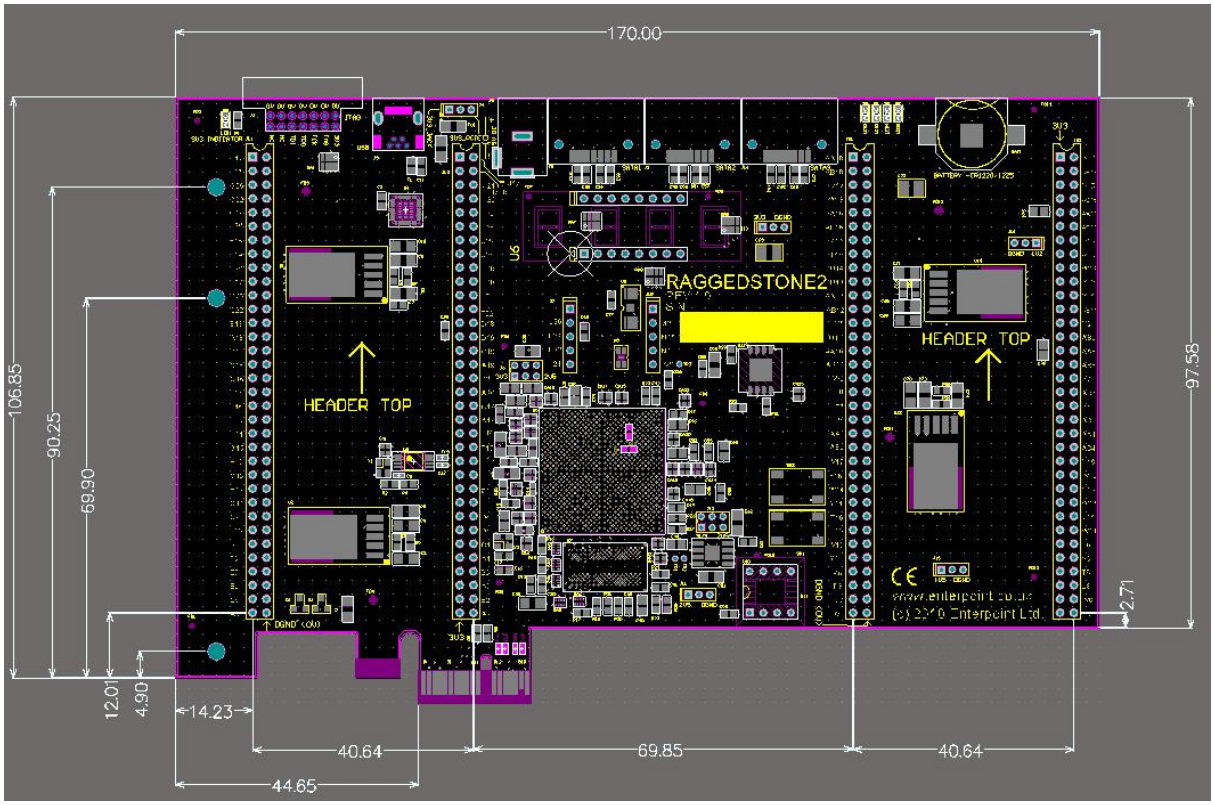
Temperature Sensor

There is a temperature sensor (type LM75C) on Raggedstone2 which has a 2-wire serial interface and an output which behaves as an over-temperature warning. The connections to the FPGA are shown below:

SIGNAL	FPGA PIN
SDA	T21
SCL	U22
OVER-TEMPERATURE	V22



Mechanical information



All dimensions are shown in millimetres. If you need any further mechanical information please contact us. Contact information is shown on page 26 of this manual.

Medical and Safety Critical Use

Raggedstone2 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Raggedstone2 board, or its design, when it is used in any medical or safety critical application.

Warranty

Raggedstone2 comes with a 90 return to base warranty. Do not attempt to solder connections to the Raggedstone2. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the Raggedstone2 board.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Raggedstone2 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Raggedstone2 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - +44 (0) 121 288 3945
Email - support@enterpoint.co.uk