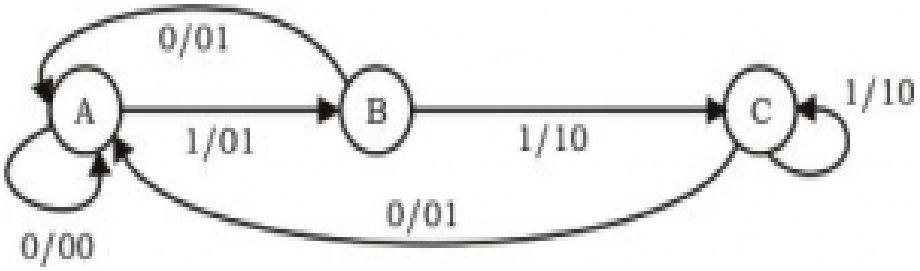
# ELL201 – Tutorial Sheet 3

1. A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. What is the minimum number of flip-flops required to implement this FSM?

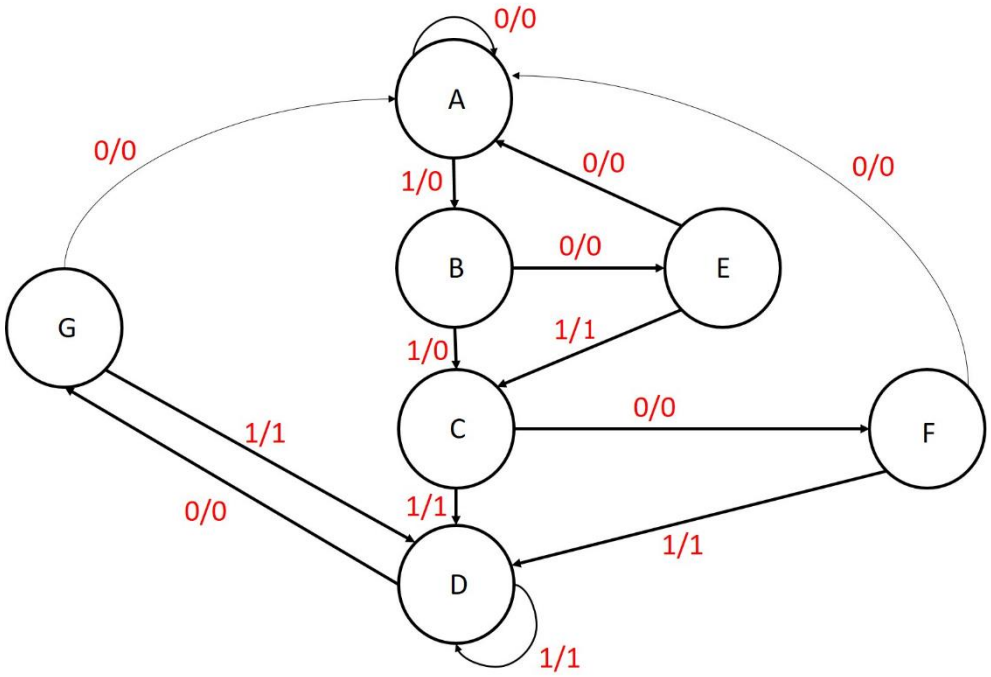
2. Design a Moore FSM that has output 'p' only if it receives a string of '01' on the serial input. Otherwise, the output will be 'q'. Convert the FSM to Mealy type.

3. Design a Mealy FSM that prints '1' when a string of 'aa' or 'bb' comes in the serial input line. Convert the FSM to Moore type.

4. The Finite state machine described by the following state diagram with A as starting state, where an arc label is x / y and x stands for 1-bit input and y stands for 2- bit output. Identify the function of the FSM.




5. Consider the following Mealy machine. Apply state reduction and answer the questions that follow.




i. What is the number of states after reduction?

ii. Mention any one pair of states that are equivalent.

iii. Convert the reduced state machine from a Mealy Machine to a Moore Machine - How many states does it have?

iv. During the above conversion from Mealy to Moore, mention any one state which undergoes a split into two states.

v. Consider the FSM's initial state to be State D, and the Serial Input to the FSM be 11001101, what will be the output observed (8-bit)?