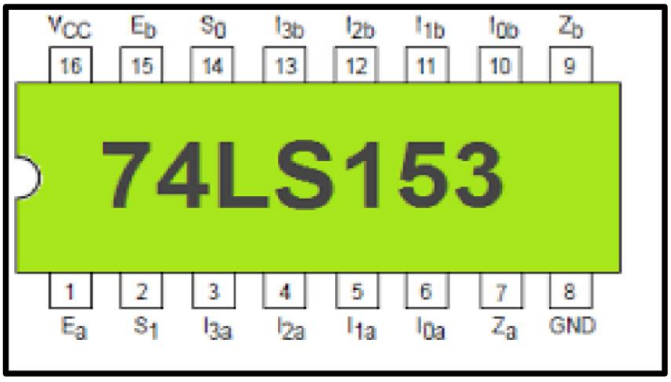
Indian Institute of Technology Delhi
ELL201/ELP201: Digital Electronics Laboratory
2020-21, Semester II
Experiment 3: Exercise with Multiplexers

The function, **F = ∑(0,1,2,5,6,8,9,11,13,14,15)** needs to be realized.

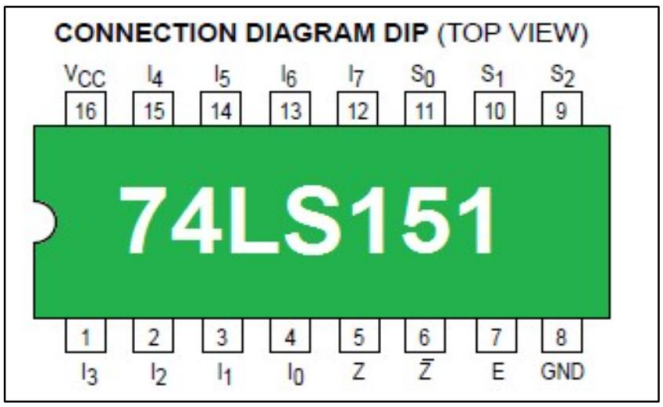
- Realize the function F using one 8 to 1 multiplexer (74151), and minimum additional gates.

- Realize the same function F using two 4 to 1 multiplexers (74153), and minimum additional gates.

Pin Diagram for MUX ICs 74151 & 74153



E_a = Enable Active low
E_b = Enable Active low
Z_a,Z_b = outputs
I_{0a}, I_{1a}, I_{2a} ,I_{3a} = input lines for mux A
I_{0b}, I_{1b}, I_{2b} ,I_{3b} = input lines for mux B
S_0, S_1 = Select lines



Z = Output
$\overline{Z}$ = Compliment of Z
E = Enable Active low
I_0, I_1..... I_7 = input lines
S_0, S_1 & S_2 = Select lines