

Simulation analysis

2025-07-19

Experiments

- Variants
 - Linear Leios, `linear`
 - Linear Leios with tx references, `linear-with-tx-references`
 - Stracciatella, `full-without-ibs`
- 100 tx/s for first 900 seconds
- Simulation ends at 1200th second
- 1400 B/tx

<https://github.com/input-output-hk/ouroboros-leios/tree/bwbush/ll3/analysis/sims/2025w29b>

`sim-cli @ 631d24a3`

100 tx/s with 1400 B/tx

Variant	Stage length	Max EB size	Demand [tx/s]	Demand [MB/s]	Demand [Mb/s]	Time to full EB [s]	Transaction size [B/tx]
<fct>	<fct>	<fct>	<dbl>	<dbl>	<dbl>	<dbl>	<dbl>
full-without-ibs	5 slot/stage	5.0 MB/EB	99.65889	0.1395224	1.11618	35.83653	1400
full-without-ibs	5 slot/stage	10.0 MB/EB	99.65889	0.1395224	1.11618	71.67306	1400
full-without-ibs	5 slot/stage	20.0 MB/EB	99.65889	0.1395224	1.11618	143.34611	1400
full-without-ibs	8 slot/stage	5.0 MB/EB	99.65889	0.1395224	1.11618	35.83653	1400
full-without-ibs	8 slot/stage	10.0 MB/EB	99.65889	0.1395224	1.11618	71.67306	1400
full-without-ibs	8 slot/stage	20.0 MB/EB	99.65889	0.1395224	1.11618	143.34611	1400
linear	5 slot/stage	5.0 MB/EB	99.65889	0.1395224	1.11618	35.83653	1400
linear	5 slot/stage	10.0 MB/EB	99.65889	0.1395224	1.11618	71.67306	1400
linear	5 slot/stage	20.0 MB/EB	99.65889	0.1395224	1.11618	143.34611	1400
linear	8 slot/stage	5.0 MB/EB	99.65889	0.1395224	1.11618	35.83653	1400
linear	8 slot/stage	10.0 MB/EB	99.65889	0.1395224	1.11618	71.67306	1400
linear	8 slot/stage	20.0 MB/EB	99.65889	0.1395224	1.11618	143.34611	1400
linear-with-tx-references	5 slot/stage	5.0 MB/EB	99.65889	0.1395224	1.11618	35.83653	1400
linear-with-tx-references	5 slot/stage	10.0 MB/EB	99.65889	0.1395224	1.11618	71.67306	1400
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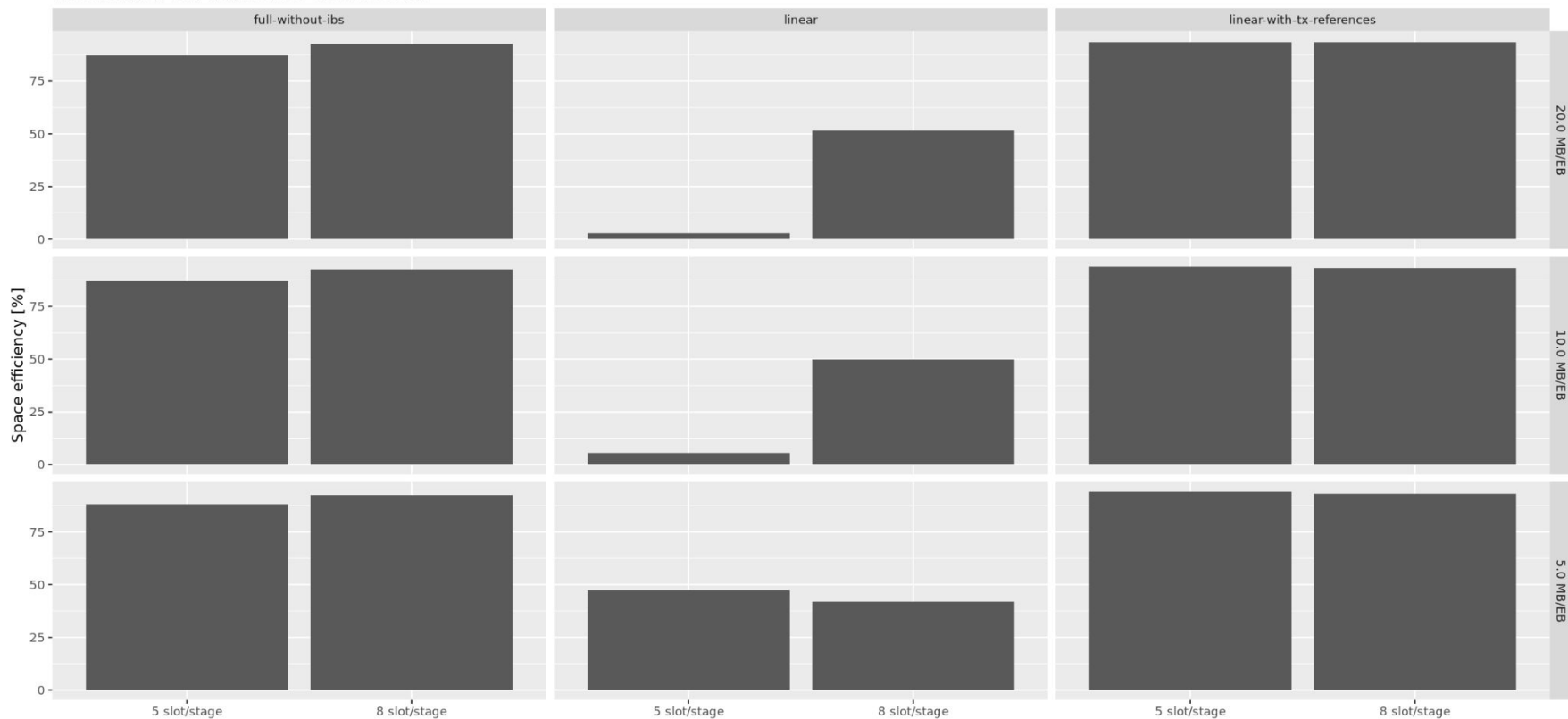
Efficiency

Variant	Stage length	Max EB size	Space efficiency [%]	Time to reach EB [s]	Time to reach ledger [s]
<fct>	<fct>	<fct>	<dbl>	<dbl>	<dbl>
full-without-ibs	5 slot/stage	5.0 MB/EB	88.019663	5.948086	56.87735
full-without-ibs	5 slot/stage	10.0 MB/EB	87.145579	5.901681	57.00624
full-without-ibs	5 slot/stage	20.0 MB/EB	87.140163	5.901895	56.98086
full-without-ibs	8 slot/stage	5.0 MB/EB	92.630722	8.259793	69.21801
full-without-ibs	8 slot/stage	10.0 MB/EB	92.639798	8.161247	68.99397
full-without-ibs	8 slot/stage	20.0 MB/EB	92.689345	8.156960	69.11355
linear	5 slot/stage	5.0 MB/EB	47.263229	43.759517	76.27580
linear	5 slot/stage	10.0 MB/EB	5.412314	133.379196	47.19447
linear	5 slot/stage	20.0 MB/EB	2.808371	110.316553	47.18600
linear	8 slot/stage	5.0 MB/EB	42.014002	112.196650	159.23294
linear	8 slot/stage	10.0 MB/EB	49.915335	19.189494	63.71906
linear	8 slot/stage	20.0 MB/EB	51.593285	17.715550	62.31809
linear-with-tx-references	5 slot/stage	5.0 MB/EB	93.970815	50.349183	89.45720
linear-with-tx-references	5 slot/stage	10.0 MB/EB	93.988888	21.697992	61.40164
linear-with-tx-references	5 slot/stage	20.0 MB/EB	93.488622	21.509128	62.86204
linear-with-tx-references	8 slot/stage	5.0 MB/EB	93.111219	107.221641	149.21241
linear-with-tx-references	8 slot/stage	10.0 MB/EB	93.358883	22.127230	64.90414
linear-with-tx-references	8 slot/stage	20.0 MB/EB	93.459876	20.527595	63.61299

Spatial efficiency

Spatial efficiency (size of txs on ledger / size of non-tx persisted data)

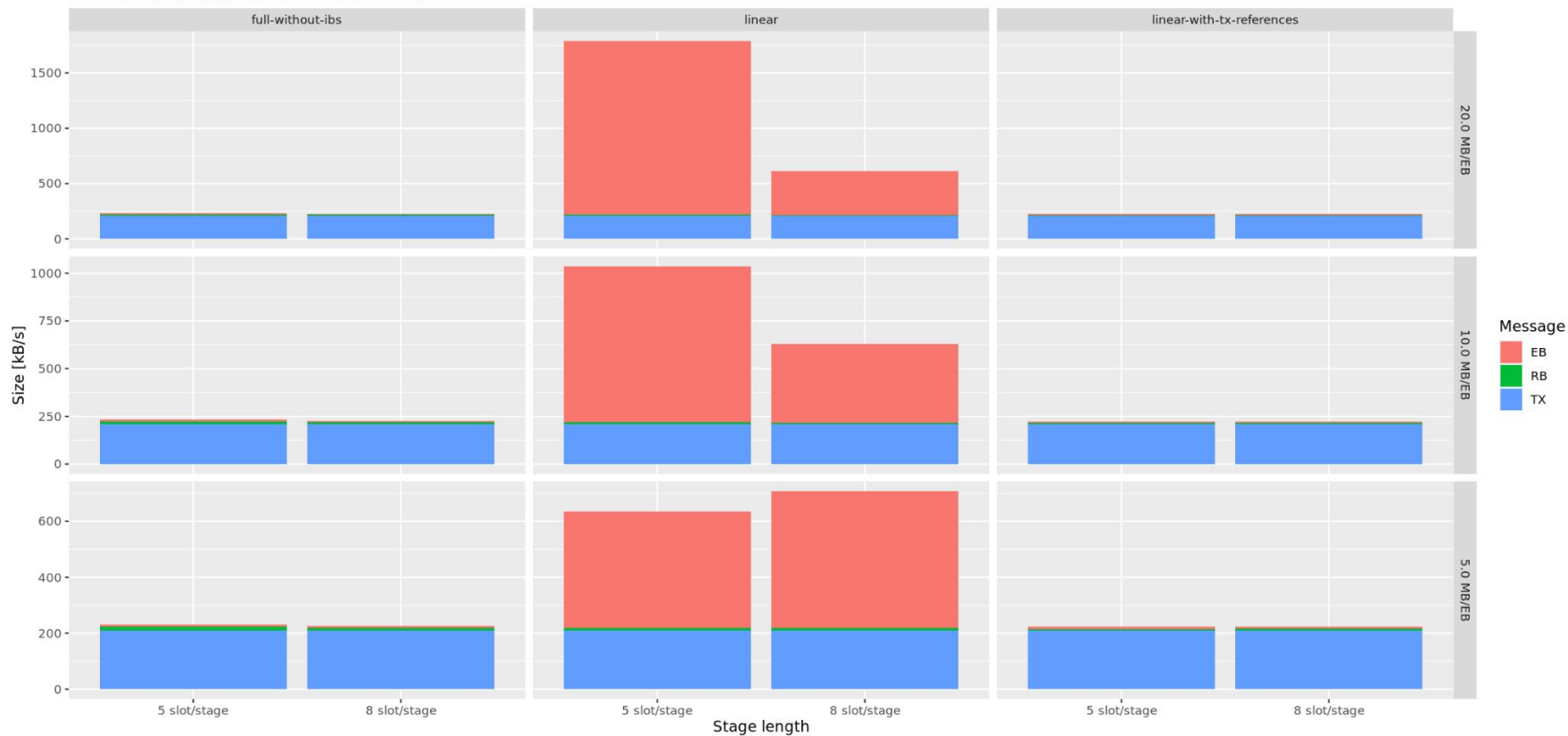
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Data volume

Size of diffused data

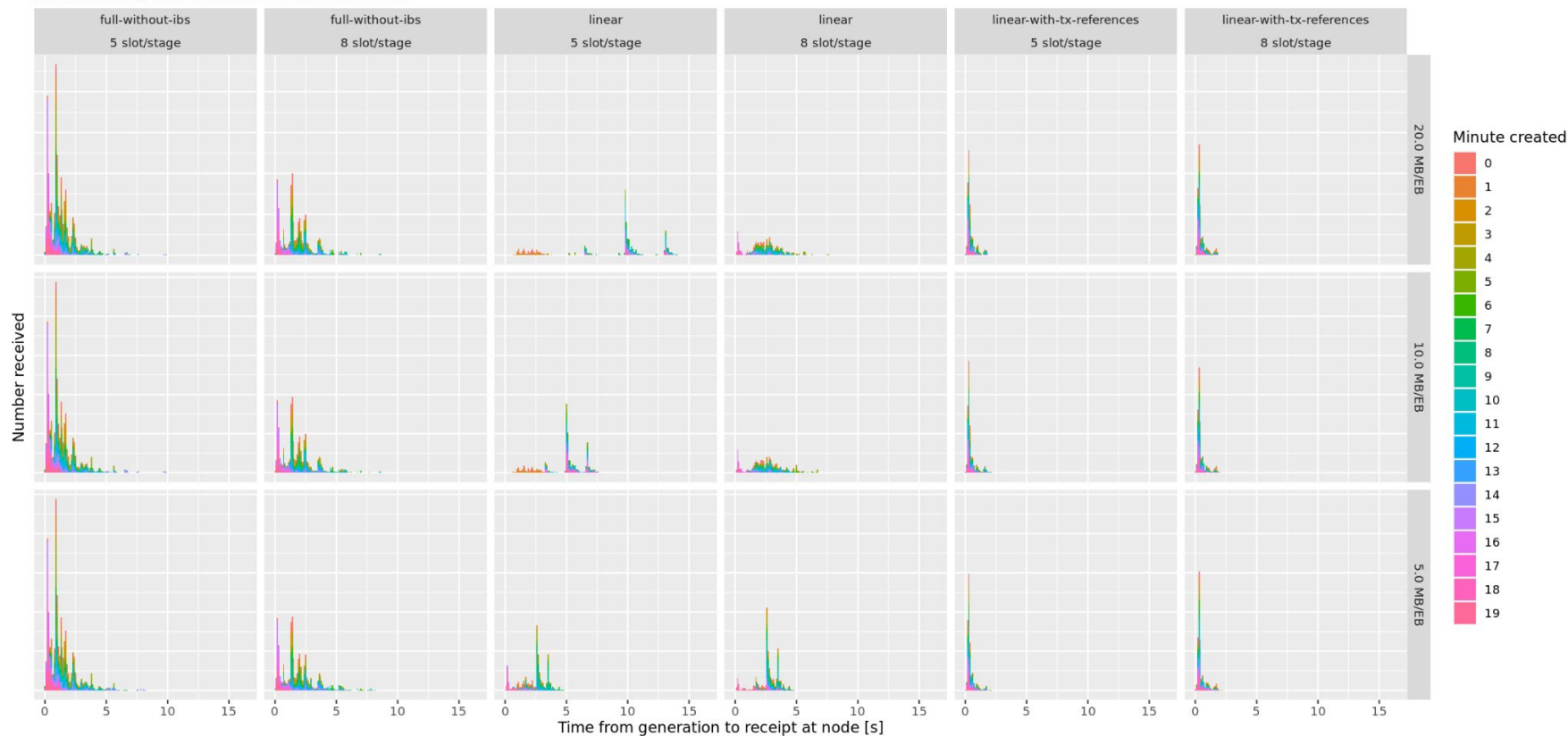
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



EB diffusion

Arrival delay for EB

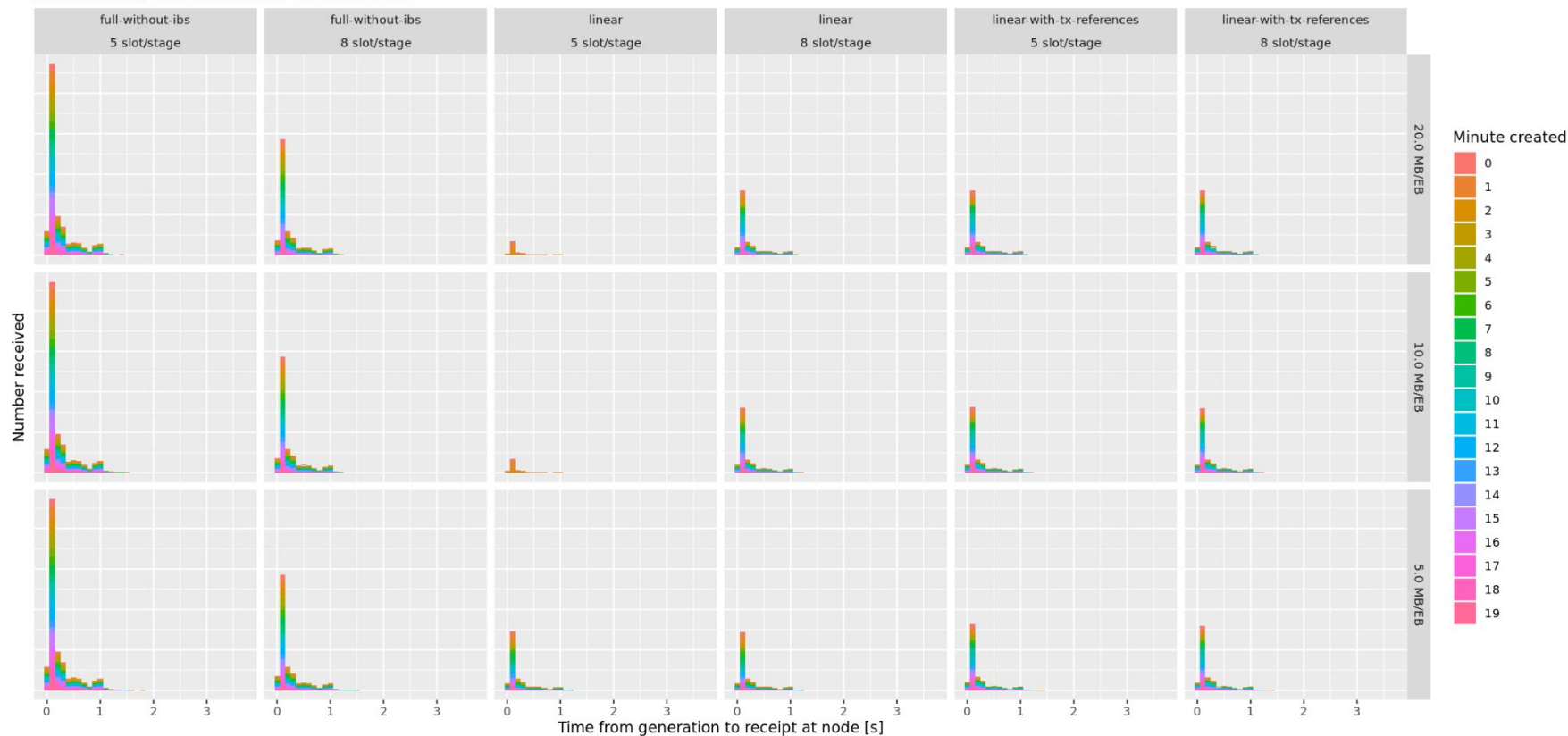
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Vote diffusion

Arrival delay for VT

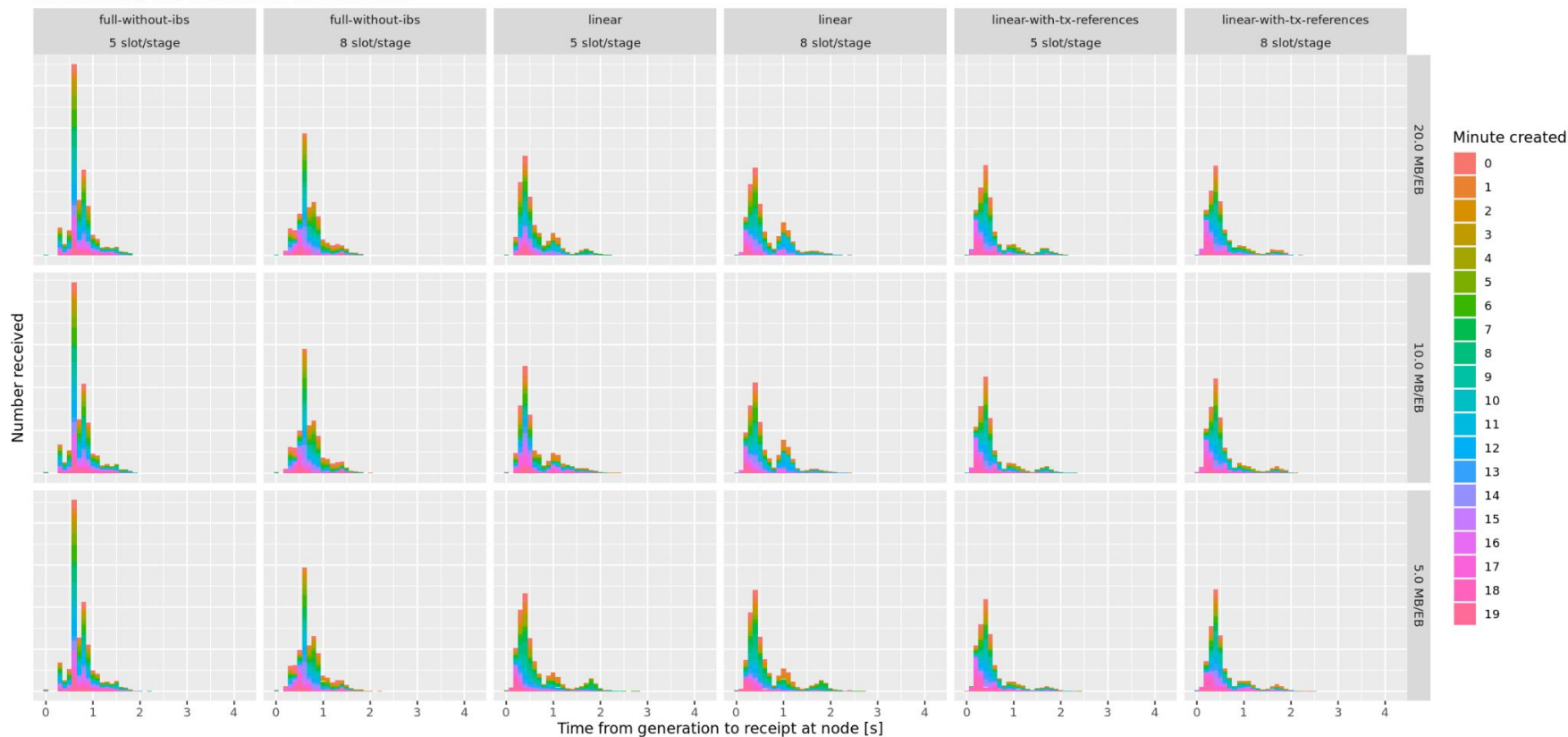
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



RB diffusion

Arrival delay for RB

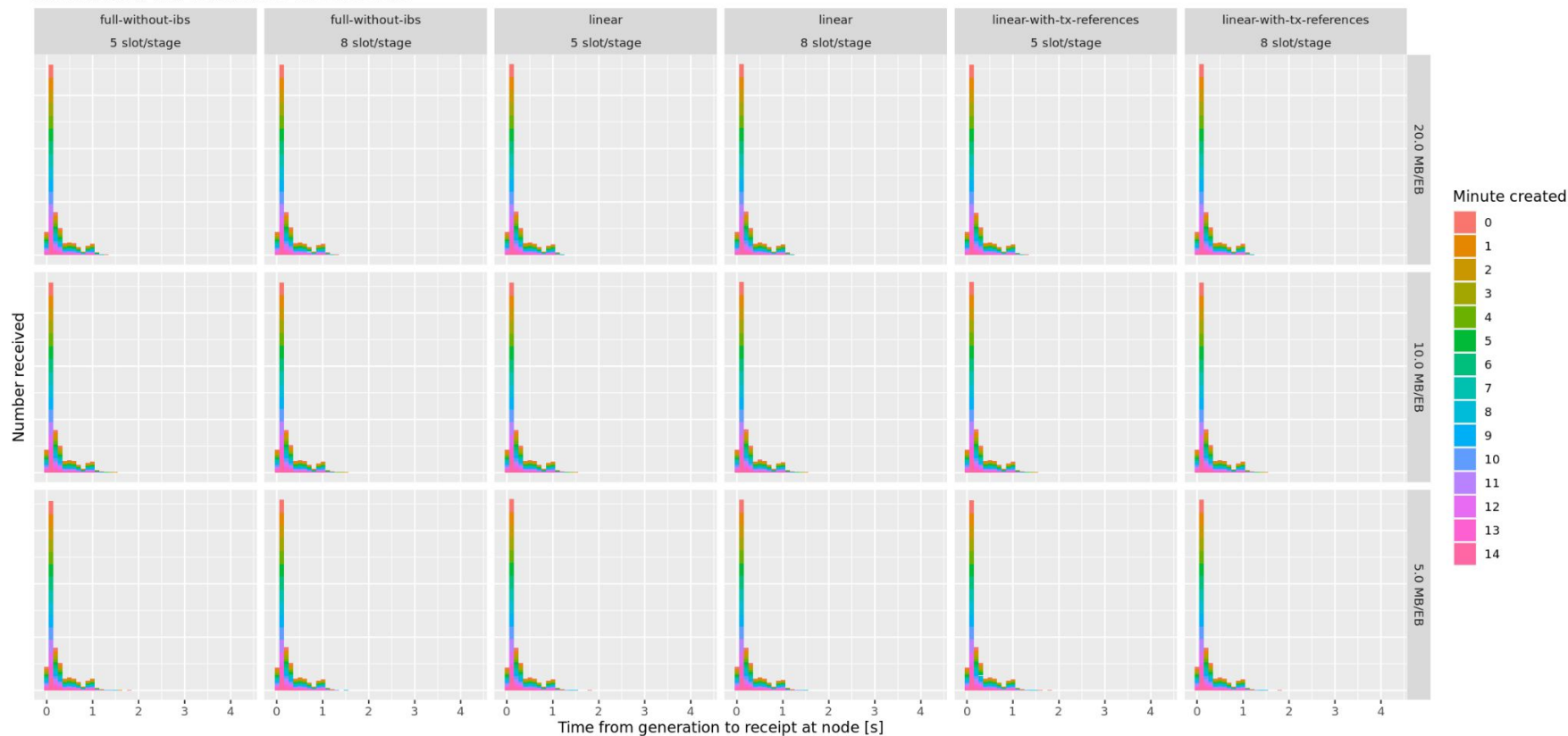
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



TX diffusion

Arrival delay for TX

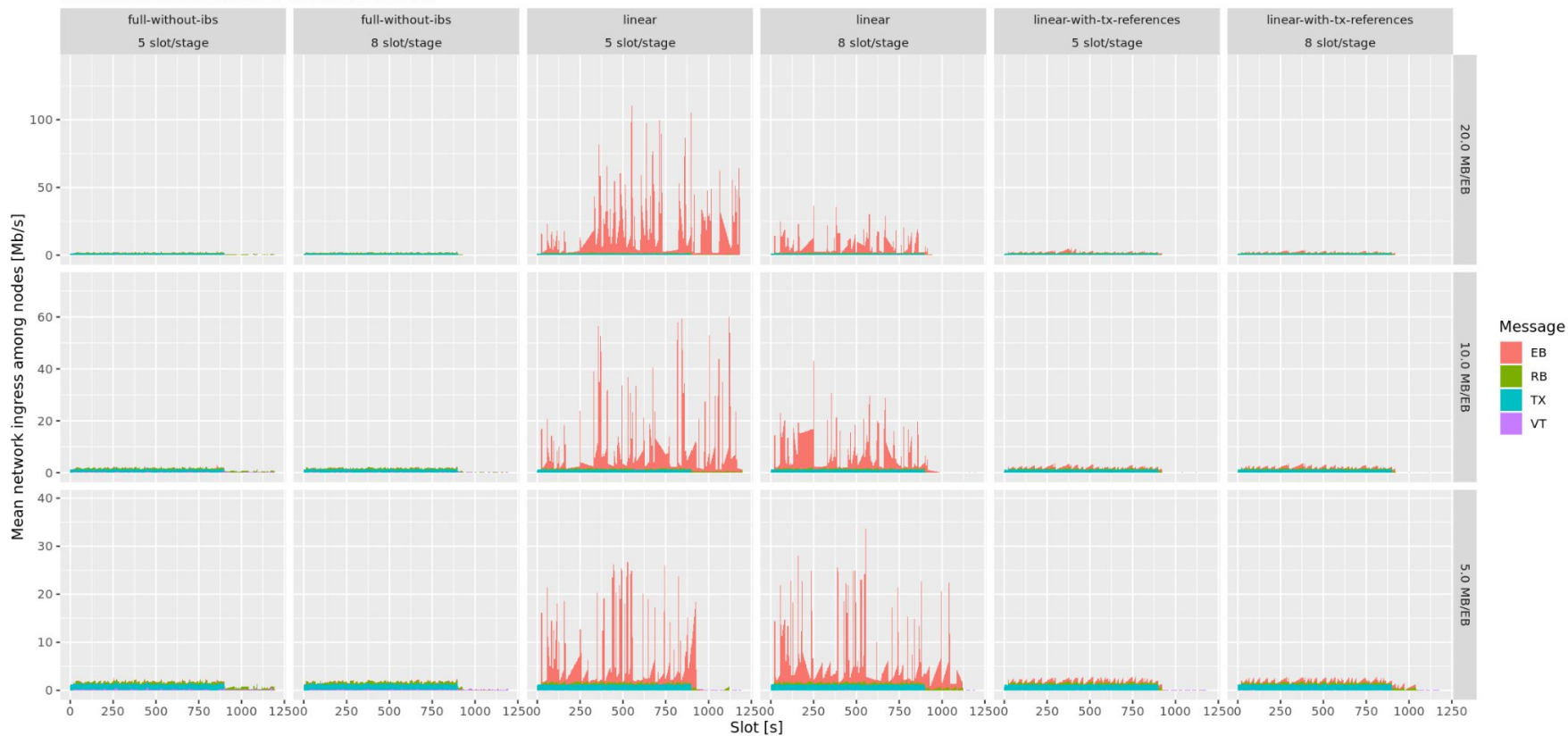
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Network (mean)

Mean nodal ingress

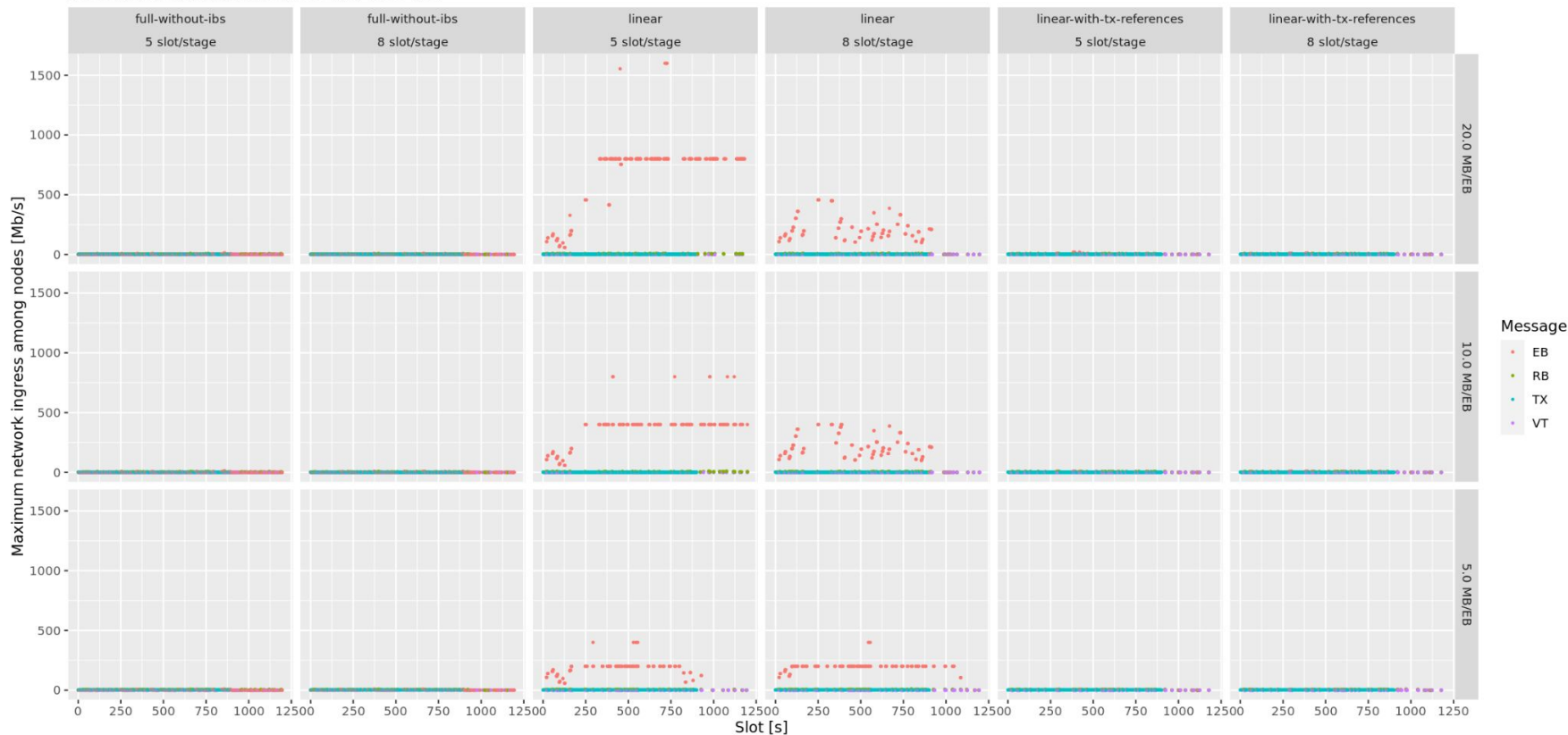
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Network (1-second peak)

Peak nodal ingress

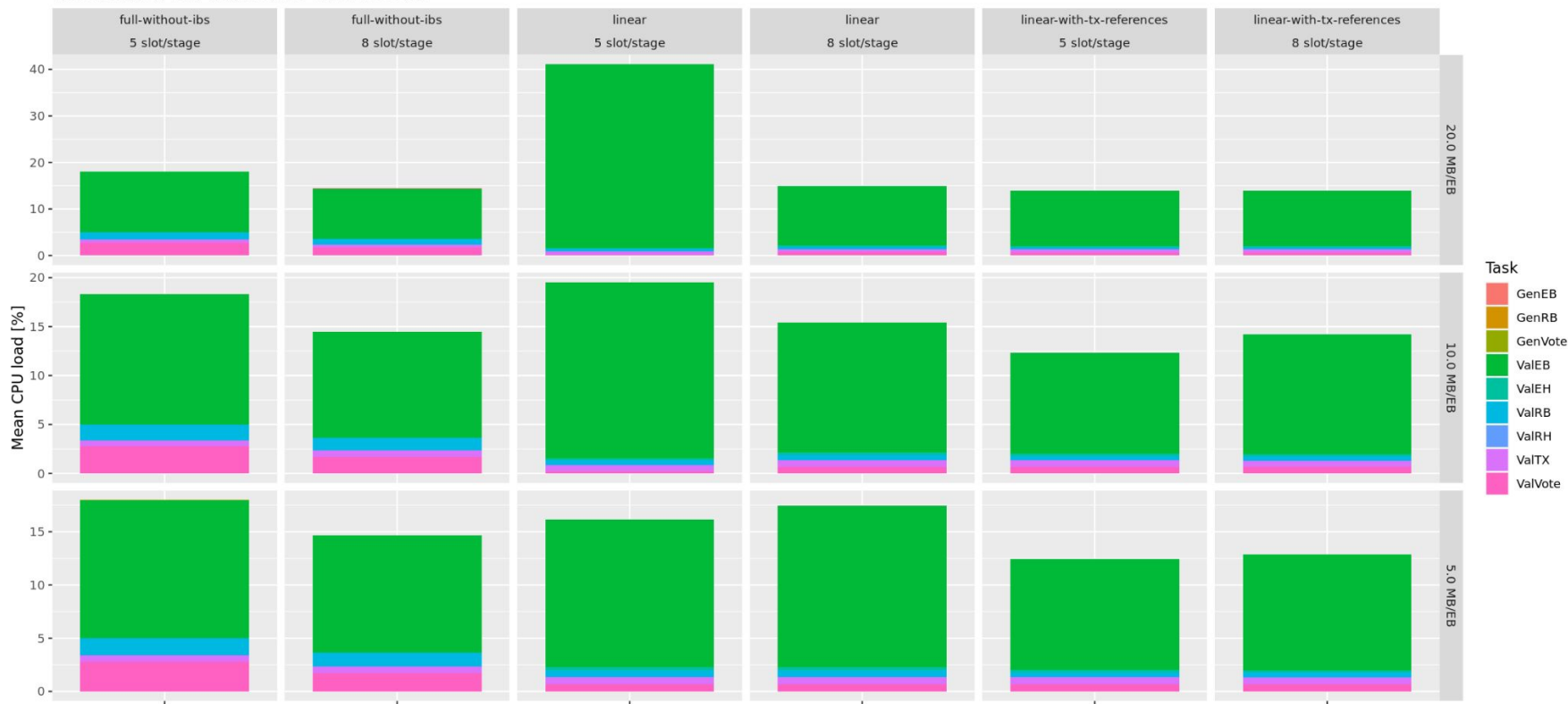
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



CPU (mean)

Mean CPU load among all nodes

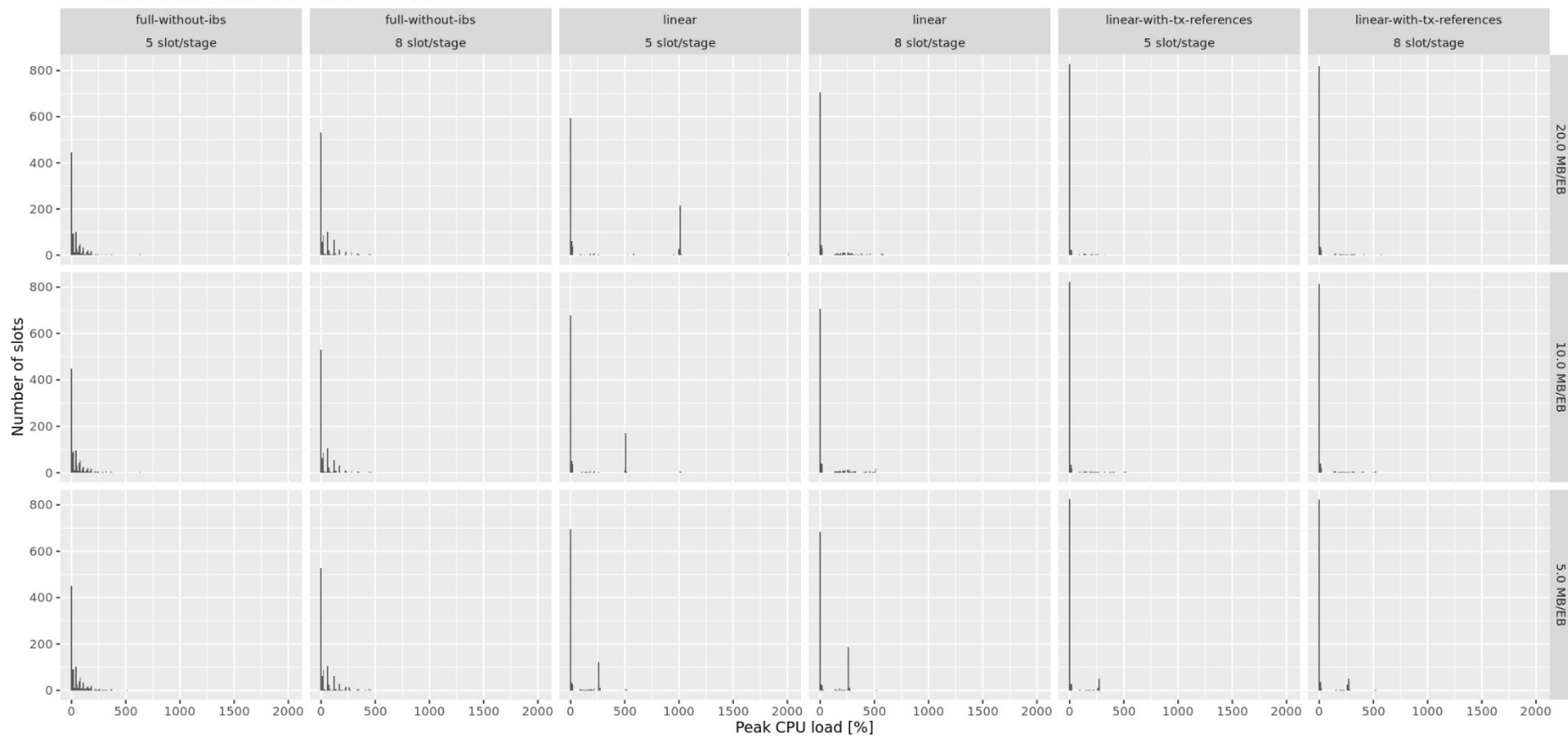
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



CPU (1-second peak)

Peak CPU load among all nodes

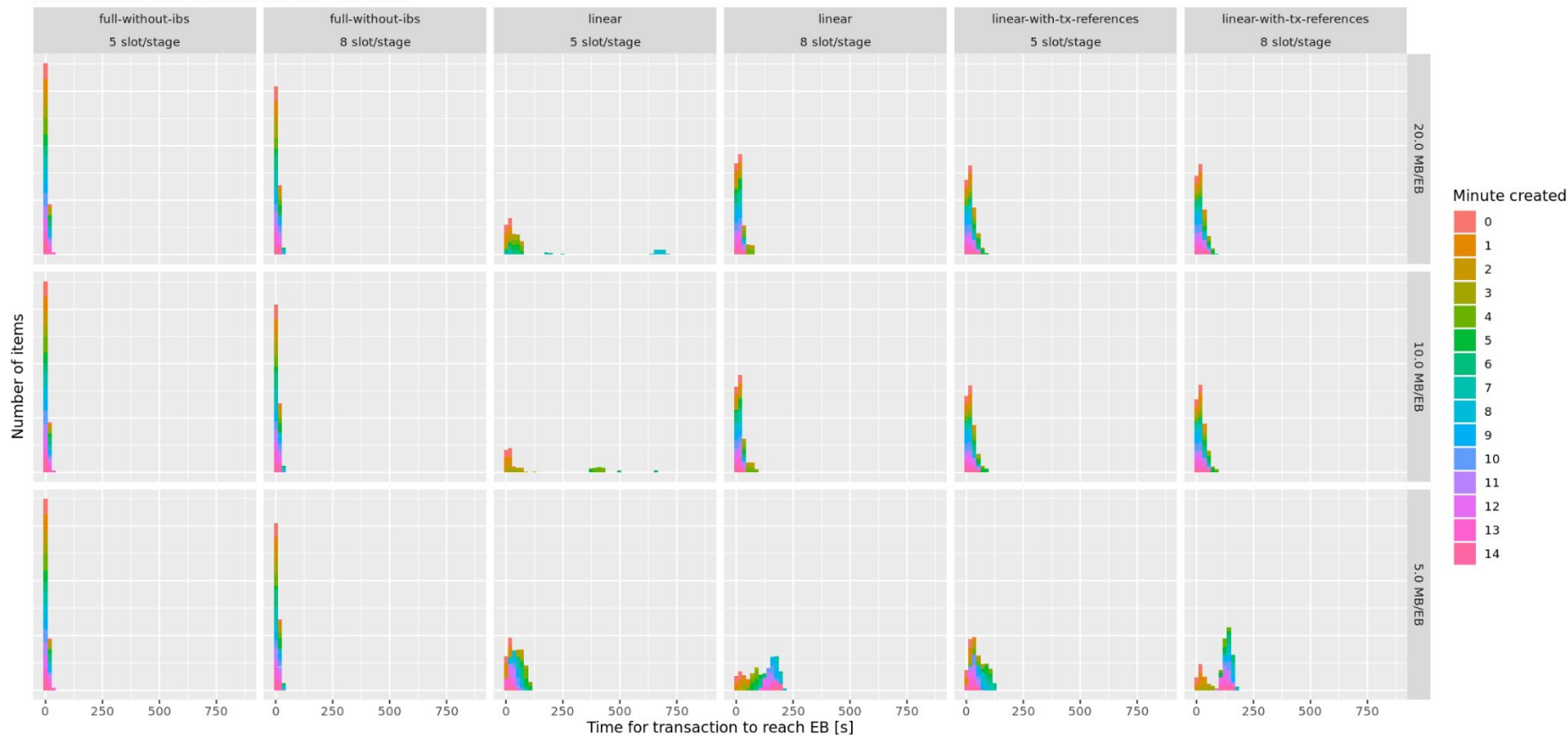
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Mempool to EB

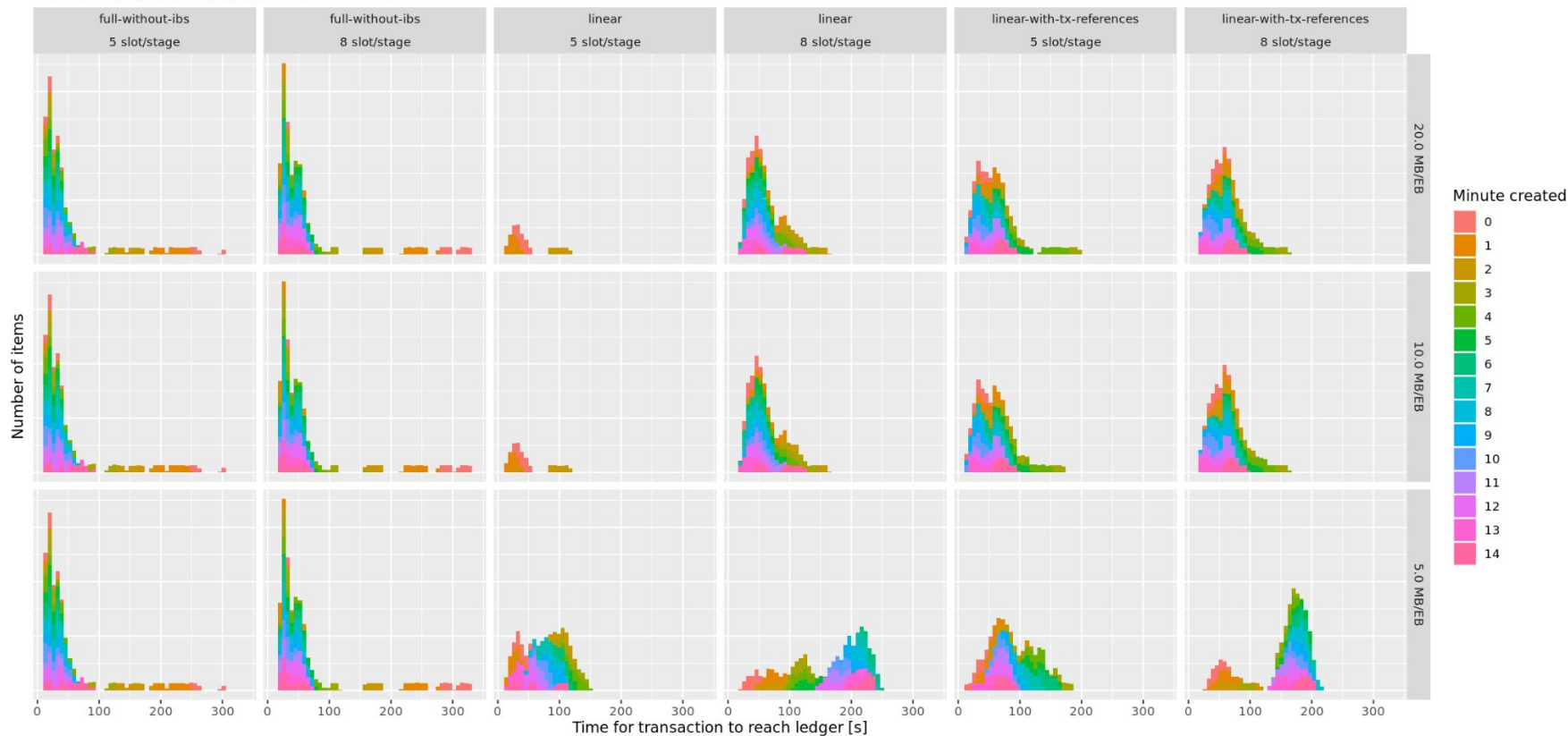
Time for transaction to reach an EB

Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Mempool to RB (certified)

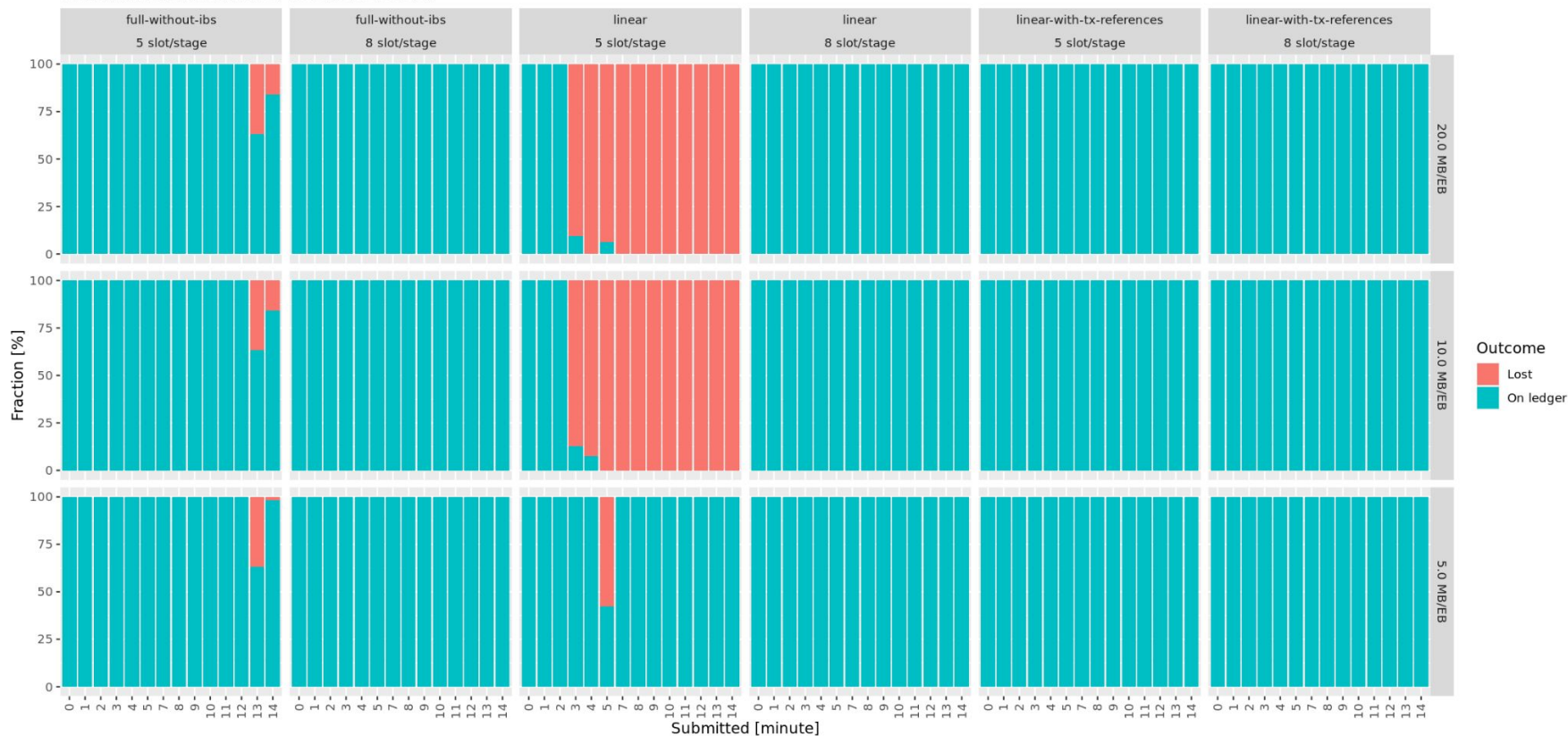
Time for transaction to reach the ledger
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Transactions reaching ledger in under 300 slots

Transactions reaching the ledger

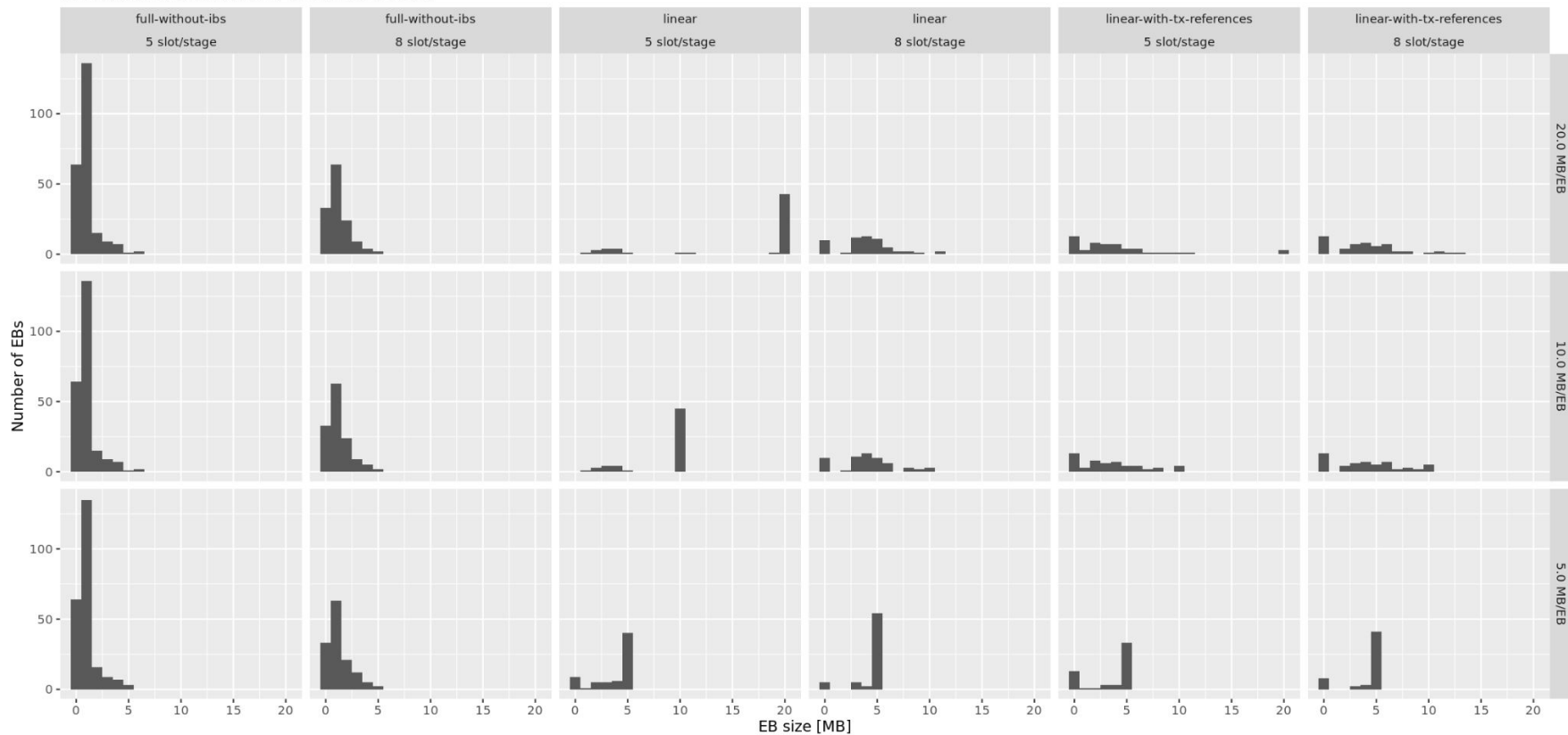
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



EB size distribution

Size of transactions in EBs

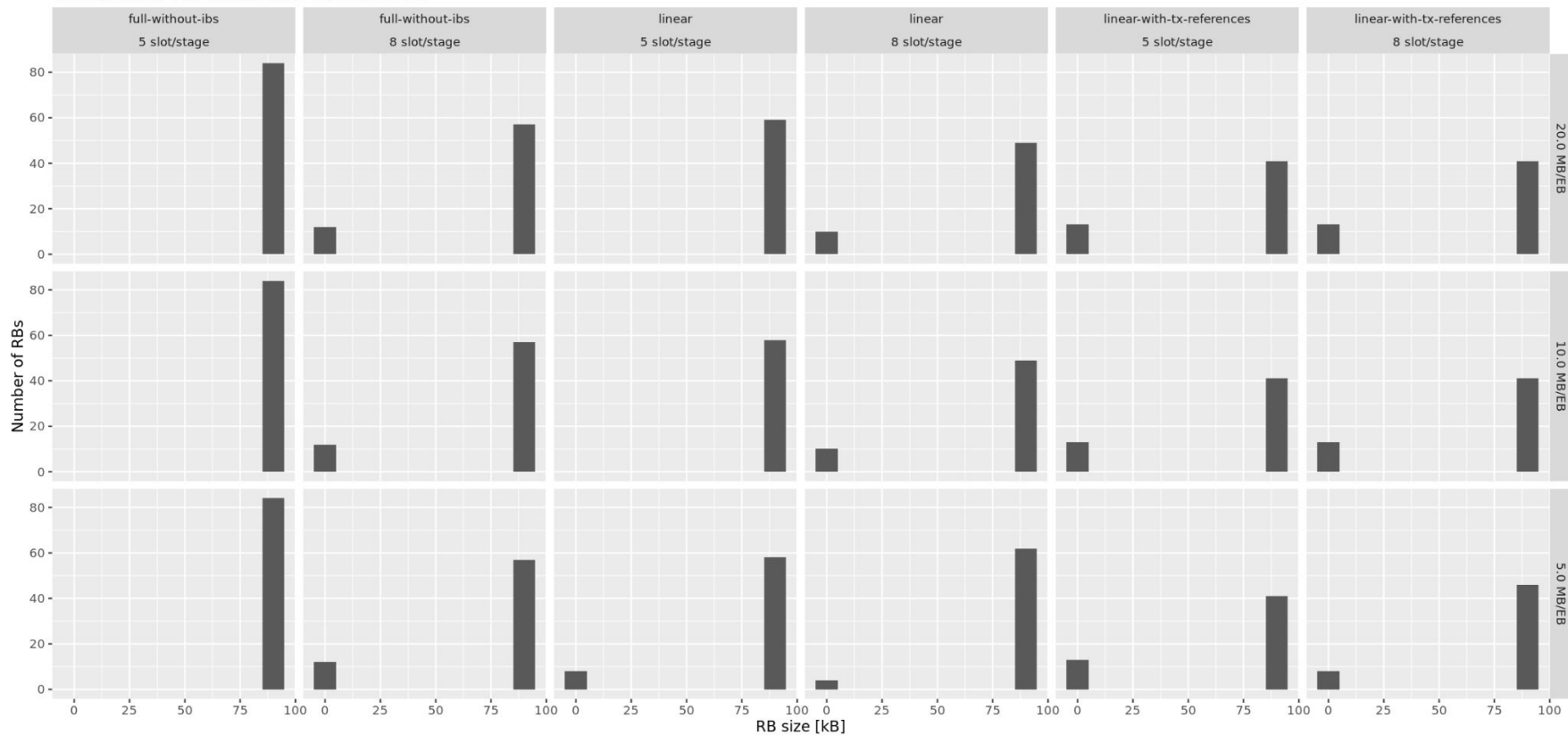
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



RB size distribution

Size of transactions in RBs

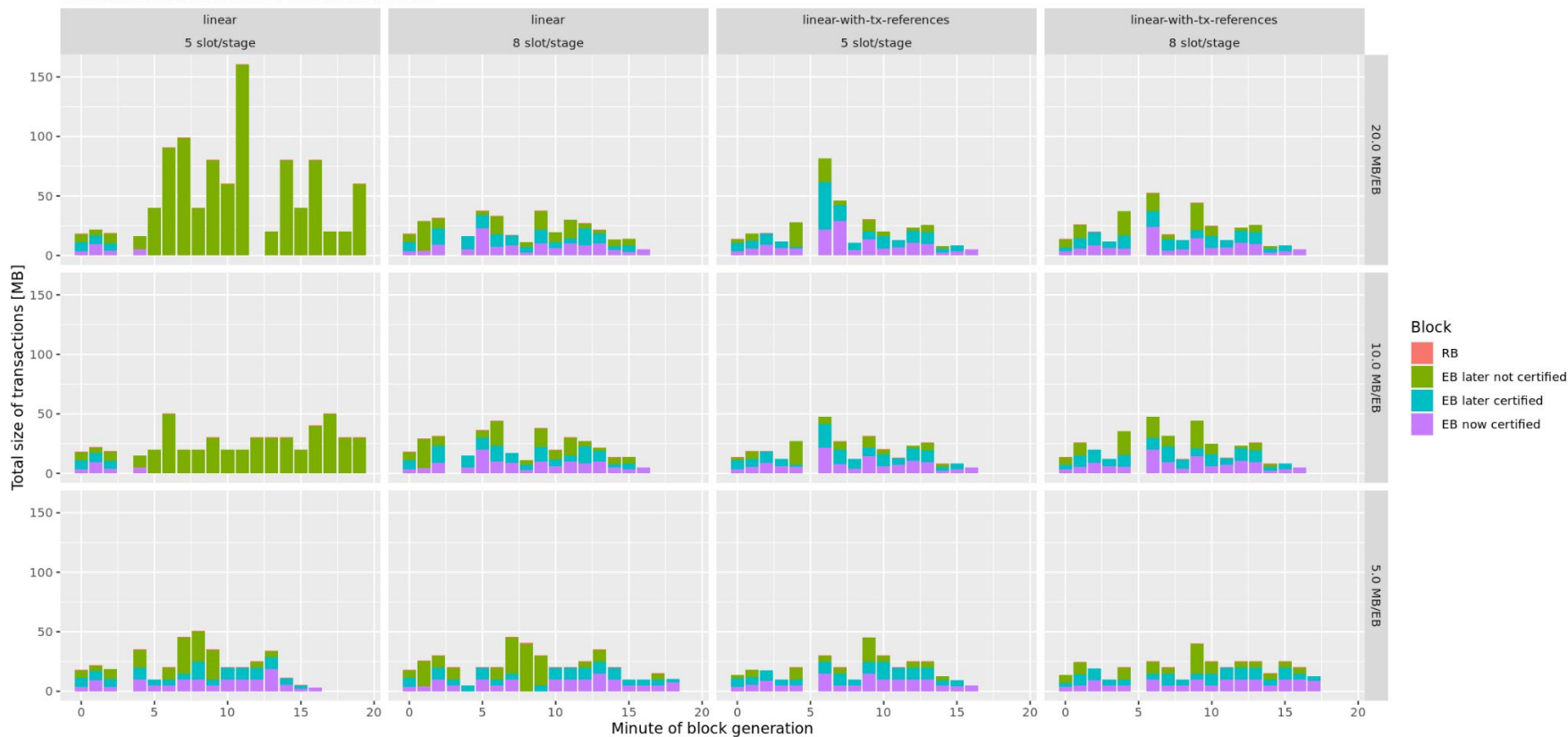
Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Disposition of blocks

Disposition of transactions in blocks

Rust simulator, mini-mainnet, 100 tx/s, 1400 B/tx



Findings

1. 5 slot/stage is too short for Linear Leios at 100 tx/s.
2. Including transactions in EBs (instead of references) results in congestion and delays at 100 tx/s.
3. 10 MB/EB is sufficient for 100 tx/s but 5 MB/EB is not.
4. EB-sortition unluckiness in Stracciatella can lengthen the transaction lifecycle, but this could be remedied by increasing the EB production rate.
5. CPU and network usage peak high when transactions are included in EBs.
6. *Caveat:* this conclusion may change when better transaction validation times are used in the simulator configuration.