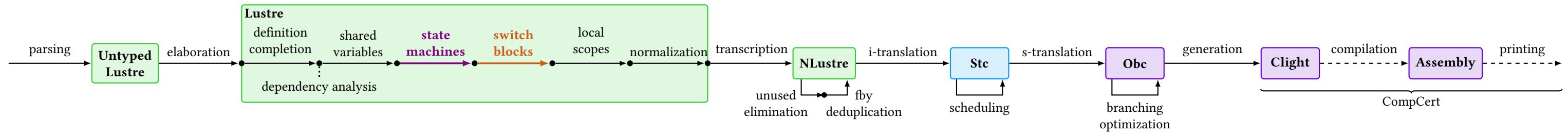


Verified Compilation of Synchronous Dataflow with State Machines

Timothy Bourke, Basile Pesin, Marc Pouzet

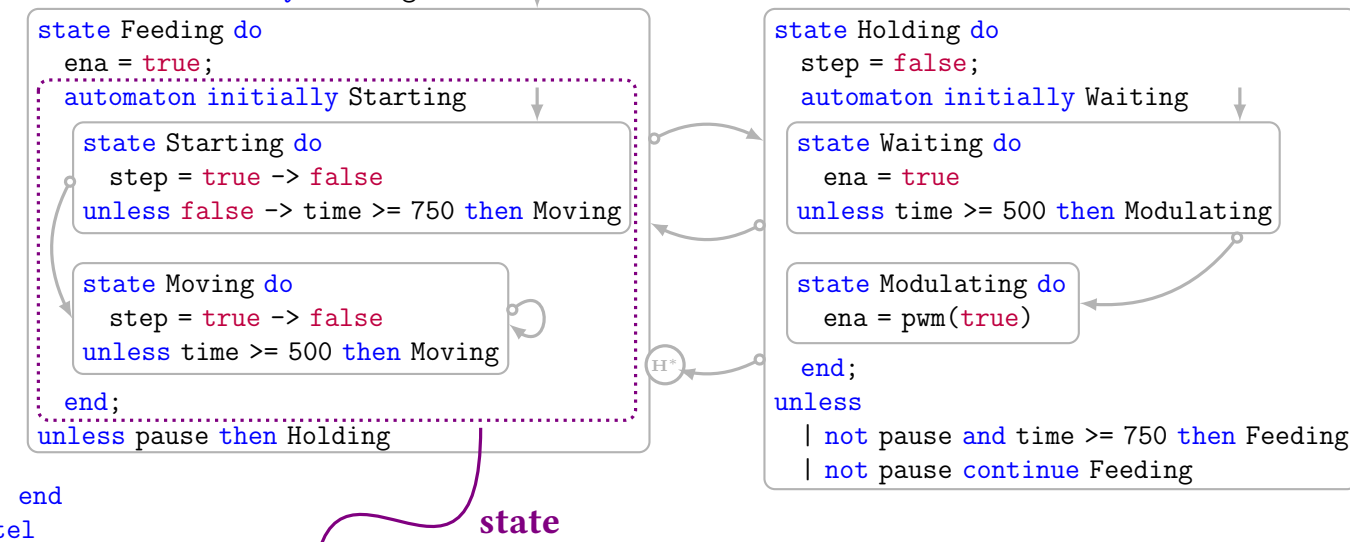
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EMSOFT — September 2023



```
node feed_pause(pause : bool) returns (ena, step : bool)
var time : int;
let
  reset
    time = count_up(50)
  every (false fby step);
```

automaton initially Feeding



state machines

```
(pst, pres) = (Starting, false) fby (st, res);
```

```
switch pst
| Starting do
  reset
    (st, res) =
      if false → time ≥ 750
      then (Moving, true)
      else (Starting, false)
  every pres
  | Moving do ...
end;
```

switch blocks

```
switch st
| Starting do
  reset
    step = true → false
  every res
  | Moving do ...
end
```

```
resS = res when (st=Starting);
reset
  stepS = true when (st=Starting) → false when (st=Starting)
every resS;
step = merge st (Starting => stepS) (Moving => stepM);
```

back-end to imperative code

RELATIONAL DATAFLOW SEMANTICS

$$\text{VARIABLE} \frac{H(x) = s}{G, H \vdash x \Downarrow [s]}$$

$$\text{EQUATION} \frac{\forall i, H(xs_i) \equiv vss_i \quad G, H \vdash es \Downarrow vss}{G, H \vdash xs = es}$$

$$\text{NODE} \frac{G(f) = \text{node } f(x_1, \dots, x_n) \text{ returns } (y_1, \dots, y_m) \text{ blk} \quad \forall i, H(x_i) \equiv xss_i \quad \forall j, H(y_j) \equiv yss_j \quad G, H \vdash \text{blk}}{G \vdash f(xss) \Downarrow yss}$$

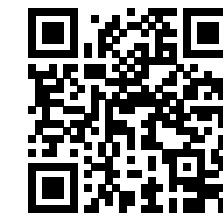
$$\text{SWITCH} \frac{G, H \vdash e \Downarrow [vs] \quad \forall i, G, (\text{when}^{C_i} vs H) \vdash \text{blks}_i}{G, H \vdash \text{switch } e [C_i \text{ do } \text{blks}_i]^i \text{ end}}$$

An operator per construct:

- **automaton** \mapsto select
- **switch** \mapsto when
- **reset** \mapsto mask
- **last** \mapsto fby

COMPILER CORRECTNESS IN COQ

Theorem behavior_asm:

$$\forall D \ G \ Gp \ P \ \text{main ins outs}, \\ \text{elab_declarations } D = \text{OK} (\text{exist_ } G \ Gp) \rightarrow \\ \text{compile } D \ \text{main} = \text{OK } P \rightarrow \\ \text{sem_node } G \ \text{main} (\text{pStr ins}) (\text{pStr outs}) \rightarrow \\ \text{wt_ins } G \ \text{main ins} \rightarrow \\ \text{wc_ins } G \ \text{main ins} \rightarrow \\ \exists T, \text{program_behaves } (\text{Asm.semantics } P) (\text{Reacts } T) \\ \wedge \text{bisim_IO } G \ \text{main ins outs } T.$$


<https://velus.inria.fr>

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PERFORMANCES: WCET ON ARMV7-A

	Vélus	Hept+CC	Hept+gcc	Hept+gcc
stepper-motor	930	1185 (+27%)	610 (-34%)	535 (-42%)
chrono	505	970 (+92%)	570 (+12%)	570 (+12%)
cruisecontrol	1405	1745 (+24%)	960 (-31%)	895 (-36%)
heater	2415	3125 (+29%)	730 (-69%)	515 (-78%)
buttons	1015	1430 (+40%)	625 (-38%)	625 (-38%)
stopwatch	1305	1970 (+50%)	1290 (-1%)	1290 (-1%)