

Retraction

Retracted: A Fault-Tolerant Structure for Nano-Power Communication Based on the Multidimensional Crossbar Switch Network

International Transactions on Electrical Energy Systems

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This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

- (1) Discrepancies in scope
- (2) Discrepancies in the description of the research reported
- (3) Discrepancies between the availability of data and the research described
- (4) Inappropriate citations
- (5) Incoherent, meaningless and/or irrelevant content included in the article
- (6) Peer-review manipulation

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

References

- [1] J. Luo and B. Liao, "A Fault-Tolerant Structure for Nano-Power Communication Based on the Multidimensional Crossbar Switch Network," *International Transactions on Electrical Energy Systems*, vol. 2022, Article ID 4783847, 8 pages, 2022.

Research Article

A Fault-Tolerant Structure for Nano-Power Communication Based on the Multidimensional Crossbar Switch Network

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In order to realize fault tolerance and further reduce the transmission delay, a fault-tolerant structure design method for nano-power communication based on a multidimensional crossbar switch network is proposed. The TSV router is designed as a double crossbar structure, namely the master crossbar (MasterCrossbar) and the slave crossbar (SlaveCrossbar). Each input port of the TSV router is divided into two supports. The port connected to the master crossbar has no input buffer, and the port connected to the slave crossbar has an input buffer. Master crossbar is the first choice for data transmission, and slave crossbar is selected when it is busy to reduce the transmission delay of data packets and reduce power consumption. Dual crossbar switches can also realize the fault tolerance of crossbar switches. The experimental results show that the author's fault-tolerant scheme, without incorporating the double crossbar switch, still has a much smaller transmission delay than the reference because the author realizes fault tolerance for defective TSVs by adding bidirectional TSVs to replace faulty TSVs. Therefore, when there is a TSV failure, the reference transmission delay increases with the number of failures, but the author's design allows packets to be transmitted in the network without being affected; the author's bidirectional TSV fault-tolerant design is combined with the double crossbar design. After that, the transmission delay is smaller than the original, and the maximum transmission delay is about 40% faster than the reference. The authors' design is superior and improves the reliability of the 3DNoC system.

1. Introduction

3DNoC is a multilayer wafer (die) interconnection through through-hole via (TSV) and uses the network structure to interconnect the interconnection of resource nodes. Common 3DNoC topology structures include 3DMesh, 3DToms, 3D stacked Mesh, and others, among them, and the structure widely studied by many scholars is 3DMeshtW. The traditional 3DMesh structure is a regular 3D network structure formed by stacking regular 2DNoCs up and down, and each layer realizes interlayer power communication through TSV. At present, most of the research on 3DNoC is based on this regular 3DMesh topology [1].

However, in today's industrial design, it is usually necessary to place modules that implement different functions on different layers of a 3D chip, for example, the CPU core is placed on the top layer, RAM and ROM are placed on

the middle layer, and communication modules are placed on the bottom layer. Due to the huge difference in the area and function of the devices in each layer, it is difficult for such a design to achieve the same layout of network nodes on each layer; it is possible to have a network structure with $n * n$ on a certain layer and a network structure with $m * m$ ($m \neq n$) on the upper layer, and as a result, some routing nodes have upward or downward channels, that is, TSVs are connected, while some nodes do not have vertical channels [2]. Such a structure makes it difficult to use traditional 3D routing algorithms to achieve the purpose of transmitting data packets.

Today, the chip manufacturing process has entered a level below 65 nanometers, the process is becoming more and more complex, and the manufacturing difficulty is becoming more and more difficult. The size of TSV is only about 10 microns, and the current TSV manufacturing

technology is not mature enough, the manufacturing cost is high, and it is easy to cause voids, fractures, misalignment, and so on in the manufacturing process, resulting in TSV failure. The yield of TSVs has become one of the decisive factors affecting the yield of the entire chip, and when the number of TSVs reaches a certain order of magnitude, the yield of chips will decline exponentially. The data show that for a silicon chip manufactured by using 65 nm CMOS process technology, 46%–65% of the cost overhead is used in the processing of TSV. Therefore, under the premise of ensuring chip communication, the number of TSVs should be as small as possible [3].

2. Literature Review

The fusion of 3D technology and NoC technology brings new opportunities for the development of integrated circuit technology and at the same time brings new challenges. One of them is TSV failure due to physical defects, which affects 3DNoC yield. In order to solve the yield problem of 3D chips, TSV fault tolerance research has gradually been reported in recent years, arousing the attention of researchers at home and abroad. Guennoc, T. et al. first proposed a circuit model for vertical channels and then proposed a fault-tolerant technology for TSV redundancy, which improved the yield from 66% to 98% [4]. Xiao, Y. et al. proposed a fault-tolerant approach based on multichannel, which can improve reliability and throughput at the same time [5]. Afterward, researchers aimed at the process differences and scales of different chips, and many TSV fault tolerance mechanisms are designed to meet the performance requirements of the chip. Zhang, X. et al. proposed that when the TSV failure rate is too high, using serial power communication and signal remapping, remap the communication channel to the fault-free channel, thereby ensuring the smoothness of the vertical channel which is shown in Figure 1 as a communication method based on the binary molecular communication model [6]. Some domestic universities and research institutes have designed circuits including TSV fault self-detection function and fault-tolerant function and also proposed several redundant circuits based on chain structure, high yield can be guaranteed when the number of TSVs is small, and the number of redundant TSVs can be optimized to the greatest extent; Gao, H. et al. proposed a bidirectional redundant fault-tolerant design, which enables redundant channel clusters to dynamically configure direction and interconnection with low latency and high throughput [7]. Zhang, Y. et al. proposed a fault-tolerant routing algorithm based on local fault blocks, which uses extended local reliability information to guide fault-tolerant routing of 3D mesh/torus networks and classifies fault-free nodes within each plane, which greatly improves the system's performance. Computing power and system performance [8]. Chakrabarti, A. et al. proposed a deadlock-free three-dimensional dynamic routing algorithm, based on the traditional 2D NoC parity-turn model, the 3D routing

space is divided into 8 quadrants, and the corresponding routing strategy is determined for each elephant limit so as to avoid deadlock [9]. Yang, S. et al. proposed a fault-tolerant routing algorithm based on cache reuse of faulty links, the algorithm adds 4 self-transmitting channels to each power communication node and adopts a transparent transmission mechanism based on cache reuse, by multiplexing the normal buffers and channels at both ends of the faulty link to transparently transmit the data packets on the faulty channel, and the probability of using the optimal output port for the data packets is improved [10]. Wang, H. et al. proposed a virtual channel-free fault-tolerant routing algorithm for node failures in 3DmeshNoC, which is based on 3D defense areas. The 3D defense area can provide the location information of the faulty body, and according to the location information of the faulty body provided by the defense area, the algorithm can find the fault location in advance and change the forwarding port so as to achieve fault tolerance and avoid introducing deadlock [11].

In 3DNoC, if two sets of unidirectional TSVs connecting adjacent routers fail, data cannot be transmitted through this channel. In order to achieve fault tolerance and further reduce transmission delay and power consumption, the author designs the TSV router in 3DNoC as a double crossbar switch structure, and each input port is divided into two subports without input buffer (buffer) and with input buffer; it is connected with the two-stage crossbar MasterCrossbar and SlaveCrossbar, respectively. Compared with reference, experiments show that by organically combining the improved redundant TSV fault-tolerant design and the design of double crossbar switches, the average delay of the network can be reduced, the area overhead of the buffer in the chip is reduced, the power consumption is reduced, and the system reliability is improved.

3. Research Methods

3.1. Overview of Crossbar Fault Tolerance. In the structure of the 3DNoC router, the crossbar is the core component, and under the cooperative operation of the arbiter and the control module, it can process data from different input ports and select the corresponding output port to output. If the crossbar fails, it will greatly affect the performance of the router power. Therefore, the fault tolerance of the crossbar switch needs to be considered [12].

There is a fault-tolerant scheme that adds a bypass mechanism to bypass the faulty crossbar, and in this scheme, if the crossbar fails, data are transferred through the bypass. Alternatively, between each input and output port on either side of the crossbar, an error detection module for cyclic redundancy check (CRC) is added, and if a data error is detected, the data will be discarded or retransmitted. All unidirectional TSVs in 3DNoC are configured as bidirectional TSVs, which have certain fault tolerance; however, when the unidirectional TSVs between adjacent TSV routers all fail, fault tolerance cannot be achieved.

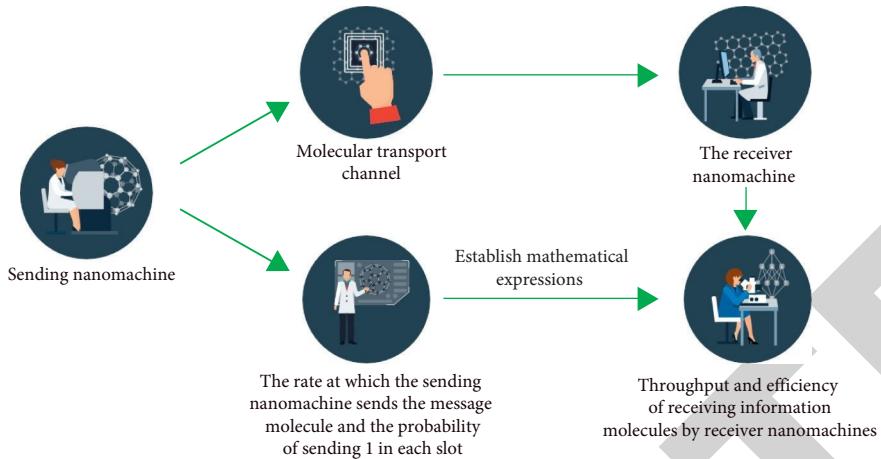


FIGURE 1: A communication method based on the binary molecular communication model.

In addition, the delay and power consumption problems faced in 2DNoC are also problems that 3DNoC hopes to solve. Its delay and power consumption are mainly distributed among the link, crossbar, and input buffer. The power consumption of the input buffer accounts for 46% of the total power consumption [13]. Some researchers reduce the input buffer or remove the buffer, but this will reduce the performance of the network [14].

The author modified the fault-tolerant design of redundant bidirectional TSVs, reducing the original two subinput buffers, and at the same time, combining with the design of the double crossbar switch of the router, the TSV router in the 3DNoC architecture is designed as a double crossbar switch architecture, which can reduce power consumption and delay while realizing fault tolerance.

3.2. Bidirectional TSV Fault Tolerant Architecture. The author has 3DNoC communication architecture, where every four 2D routers share a TSV router. When data packets require interlayer communication, the XYZ routing algorithm is used. First, the data packet is routed on the same plane to reach the cluster corresponding to the cluster where the destination node is located, and then the data packet is transmitted to the TSV router for transmission along the Z direction through TSV.

The author's bidirectional TSV fault-tolerant design structure is shown in Figure 2, which is perfected and modified on the basis of redundant bidirectional TSV fault-tolerant design. The structure design reduces the buffer area and at the same time removes the package assembly module in the original design so that the overall design is more concise and the area cost is smaller. Because the buffer is the component that occupies the largest area and consumes the largest power consumption in the entire router, reducing the use of the buffer can save resources to a large extent. If you want the structure to transmit two flits at the same time to achieve high-speed data transmission, you can perform flit-level acceleration processing on the data packets, such as using

the flit-level acceleration mechanism of the virtual channel, combined with the control module of the bi-directional link, in order to realize the flit-level acceleration high-speed transmission [15].

3.3. TSV Router Architecture

3.3.1. Design and Fault Tolerance of Double Crossbar. In order to further reduce the transmission delay of the network, realize the fault tolerance of the crossbar switch, and improve the performance of the whole 3DNoC system, the author designs the TSV router power in 3DNoC as double crossbar switch architecture.

In the cluster-based 3DNoC architecture, which commonly used TSV routers without virtual channels, each TSV router has 6 input and output ports, namely east-north (EN), west-north (WN), east-south (ES), west-south (WS), up (UP), and down (DW). These six ports are, respectively, responsible for the power communication with the four 2D routers in different directions in the same cluster and the TSV routers in the upper and lower adjacent layers. In order to prevent out-of-order crosstalk of data packets during transmission, the author's data packets are only designed in the format of a data flit.

In 3DNoC, data packet transmission must go through the crossbar switch, and the data packet can transmit data smoothly only after being assigned to the crossbar switch. When there are multiple data packets requesting transmission, the data packets that cannot be allocated by the crossbar switch and cannot be transmitted in time will be buffered in the input buffer and wait, as well as packets cannot be transmitted until the crossbar arbiter responds and assigns the crossbar. If there are many data packets communicated in the network and the network load is large, the data packets buffered in the input buffer will become more and more arriving, and the transmission delay will also increase with the increase of the waiting time of the data packets, which will seriously affect the network performance of 3DNoC. In order to reduce the transmission delay, the author redesigned the architecture of the TSV router in

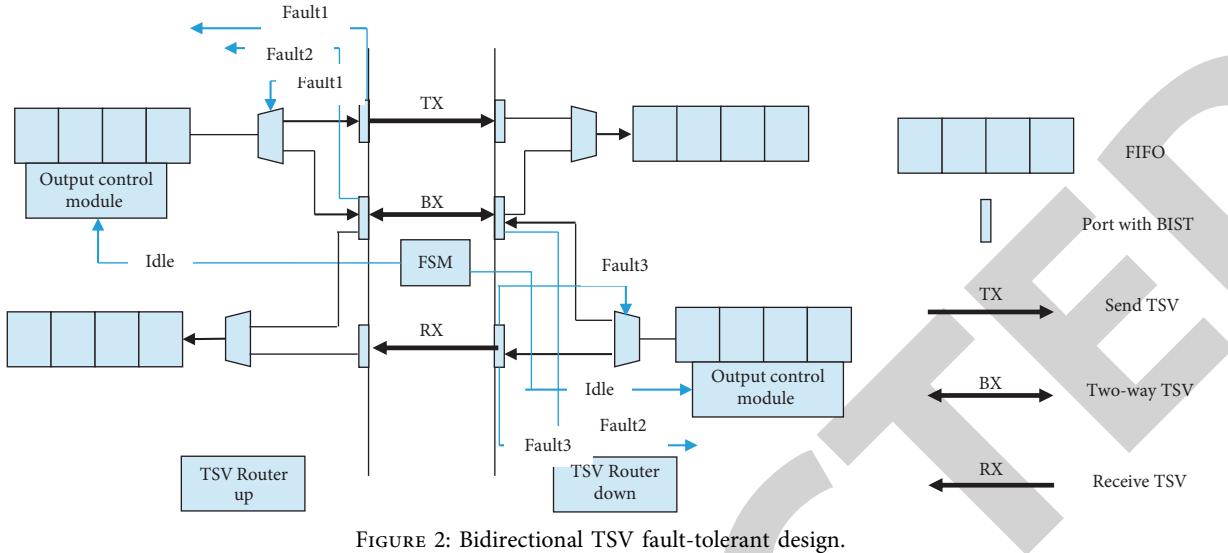


FIGURE 2: Bidirectional TSV fault-tolerant design.

3DNoC by using the architecture of the dual crossbar router in 2DNoC proposed in [16].

The designed crossbar consists of a master crossbar and a slave crossbar. Each input port of the TSV router is divided into two subports by a data distributor (Demultiplexer, DMUX), which are respectively connected to the master crossbar and the slave crossbar. There is no input buffer on the path connected to the master crossbar, and there is an input buffer on the path connected to the slave crossbar; each output port is set with a data selector (Multiplexer, MUX) connected to the master crossbar and the slave crossbar, respectively [17].

The master crossbar has higher priority than the slave crossbar. As long as there is data input from the port of the TSV router, the master crossbar is preferentially selected for transmission; only when the master crossbar is occupied, the slave crossbar is selected for transmission, and the data passing through this path must pass through the input buffer cache [18]. If there is a new data request for transmission at this time, as long as the master crossbar is idle, the master crossbar is preferred; otherwise, it must be cached in the buffer and then transmitted through the slave crossbar.

When data packets are transmitted through the master crossbar path, there is no need to buffer the data, the data can be transmitted directly through the link, and the delay and power consumption of the link are much smaller than that of the buffer; this is the main reason why the author designed the TSV router power as a dual crossbar. On the other hand, the design of the double crossbar switch also has the function of fault tolerance. In the traditional design, there is only one crossbar switch, if a hardware failure occurs in this crossbar switch, the entire TSV router cannot complete the routing and forwarding of data packets, and the entire router will be scrapped, resulting in a great waste of resources. In the author's dual crossbar TSV router, the original crossbar has been replaced by the current two crossbars, the master

crossbar and the slave crossbar, which can help each other and complement each other [19].

Define 1Mfault to represent the fault condition of MasterCrossbar,

$$M_{\text{fault}} = \begin{cases} 0, & \text{No trouble,} \\ 1, & \text{failure.} \end{cases} \quad (1)$$

Define 2Sfault to represent the fault condition of Slave Crossbar,

$$S_{\text{fault}} = \begin{cases} 0, & \text{No trouble,} \\ 1, & \text{failure.} \end{cases} \quad (2)$$

The fault-tolerant mechanism of double crossbar switches detects whether the master and slave crossbars are faulty at the same time through BIST and feeds back the detected M_{fault} and S_{fault} signal values to the crossbar arbiter (SA). After receiving the feedback signal from the BIST, the SA knows whether the crossbar switch of the router is faulty according to the value of the feedback signal and then allocates the crossbar switch according to the fault condition. If $M_{\text{fault}} = 0$ and $S_{\text{fault}} = 0$, then a single data packet preferentially selects the master crossbar of the router to transmit data and only selects the slave crossbar for transmission when the master crossbar is occupied; if multiple data packets are requested at the same time, the master crossbar and slave crossbar can be used to transmit data at the same time under the principle of two-level crossbar priority.

If one of the feedback signals has a value of 1, which indicates that one of the double crossbars is faulty, the data packet can only select the crossbar whose fault signal value is 0 in the router for transmission [20]. There are two cases for this, which are as follows:

- (1) When $M_{\text{fault}} = 1$ and $S_{\text{fault}} = 0$, the master crossbar is faulty, and the data packet can only select the slave crossbar to transmit data.
- (2) When $M_{\text{fault}} = 0$, $S_{\text{fault}} = 1$, the slave crossbar is faulty, and the data packet can only select the master crossbar to transmit data.

Therefore, the structure of the double crossbar switch can realize fault tolerance. In the event of a failure of one of the two crossbar switches, data can be passed through the other faultless crossbar switch without being blocked.

If the main crossbar fails, our original intention of reducing power consumption and delay will not be realized, but data can still be transmitted through the slave crossbar and become a traditional router transmission. If the slave crossbar fails, the data packets can still be transmitted through the master crossbar, but the master crossbar does not have an input buffer, which reduces power consumption and delay and also reduces the throughput of the system, as well as the performance of 3DNoC will decrease accordingly. It is clear that although in the double crossbar design, there is a failure in the system performance which will be affected; however, another one can be used to achieve fault tolerance so that data can be transmitted smoothly. Moreover, the TSV router can still work, and the whole router will not be disabled due to the failure of the crossbar switch, thus saving router resources.

3.3.2. TSV Router Pipeline Segment. In the 3DNoC architecture designed by the author, all 2D routers adopt the four-stage pipeline shown in Figure 3(a). (a) The figure shows the 4-stage basic pipeline of a TSV router without virtual channels. When the data packet arrives at the TSV router, it is first buffered in the buffer, that is, the write buffer (BufferWrite, BW); then, through routing calculation (routing computation, RC), the routing information of the data packet is obtained; after determining the next-hop address of the data packet, the cross switch allocation (switch allocation, SA) is performed; the cross switch determines which port to output the data packet from according to the result of route calculation and cross switch allocation, that is, the cross switch transmission (Switch Transmission, ST); after going through four basic pipelines, the data packets are transmitted through the link (link transmission) and routed to the next-hop TSV router. This is a traditional router pipeline that does not use virtual channels.

The design of the TSV router adopts the forward routing strategy to further reduce the pipeline segment, and after the TSV router adopts the design of the double crossbar switch, the master crossbar switch and the slave crossbar switch can transmit data packets at the same time, so SA and ST can be in the same segment of the pipeline [21]. Moreover, the data packets passing through the main crossbar switch do not need to be written to the buffer BW. Therefore, the pipeline can be reduced by two stages at most, as shown in Figure 3(b), which is the optimal delay. If the data packet is transmitted from the crossbar switch, it is necessary to increase the BW pipeline after the RC, and the overall

pipeline segment is only reduced by one segment, as shown in Figure 3(c). Since the pipeline segment of each data packet is reduced, the transmission delay of the whole network of 3DNoC is also reduced [22].

4. Results Analysis

The experimental tool for network simulation analysis uses OPNET simulation software to build a $4 \times 4 \times 3$ 3DmeshNoC model. In the process model modeled by OPNET, the router-related routing algorithm is set well, and the author's experimental communication still adopts a convincing random power communication mode. In the simulation experiment, under different packet injection rates, comparing the network performance between the author's proposed scheme and the communication architecture proposed in the literature, the transmission delay of data packets in the network is used as a technical indicator.

Before completing the experiment, first introduce two nouns: the Manhattan distance and the hop count.

- (1) Manhattan distance refers to the subtraction of the corresponding X, Y, and Z coordinates of two resource nodes in the 3DNoC network, and the sum of their absolute values is taken; this sum is the Manhattan distance. For example, the coordinates of the source node are (X_s, Y_s, Z_s) , and the coordinates of the destination node are (X_d, Y_d, Z_d) , which is the Manhattan distance between the source node and the destination node as follows:

$$\text{diff} = |X_s - X_d| + |Y_s - Y_d| + |Z_s - Z_d|. \quad (3)$$

- (2) Hop count refers to the sum of the number of routers separated by the source node and the destination node in the X and Y directions.

The delay of data packet transmission is mainly affected by the location and routing algorithm of the source resource node and destination resource node in 3DNoC. If the Manhattan distance between two resource nodes is far away, the number of routing hops will increase when they communicate between them, and the transmission delay will increase with it [23]; on the contrary, the number of hops will be very small, and the delay will be very small. The power communication between resource nodes is completed according to the corresponding routing algorithm; if the efficiency of the routing algorithm is relatively low, the short Manhattan distance needs to be detoured to reach it, and the transmission delay will increase [24, 25].

The author's experimental results are shown in Figures 4–7, and the results show that when the author's fault-tolerant scheme is not combined with the double crossbar switch, the transmission delay is still much less than that of the literature because the author realizes fault tolerance for the faulty TSV by adding a bidirectional TSV to replace the faulty TSV. Therefore, when there is a TSV failure, the transmission delay increases with the increase in the number of failures, but the author's design can make the data packets transmitted in the network without being affected.

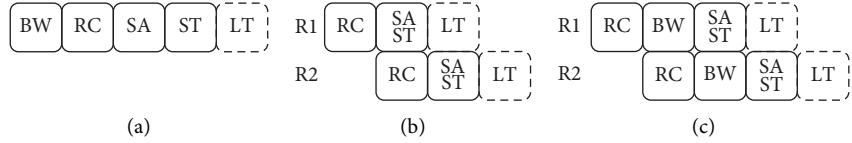


FIGURE 3: Router pipeline segment. (a) No virtual channel. (b) The main crossbar switch. (c) From the crossbar.

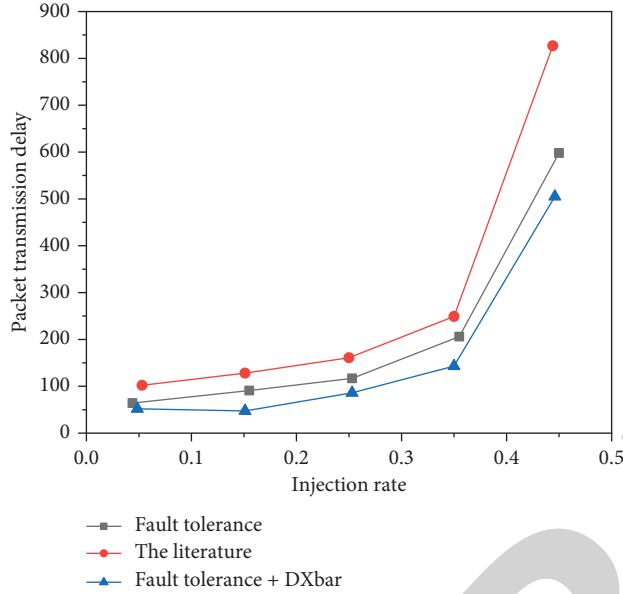


FIGURE 4: Comparison of packet transmission delays when there is no number of faulty TSVs.

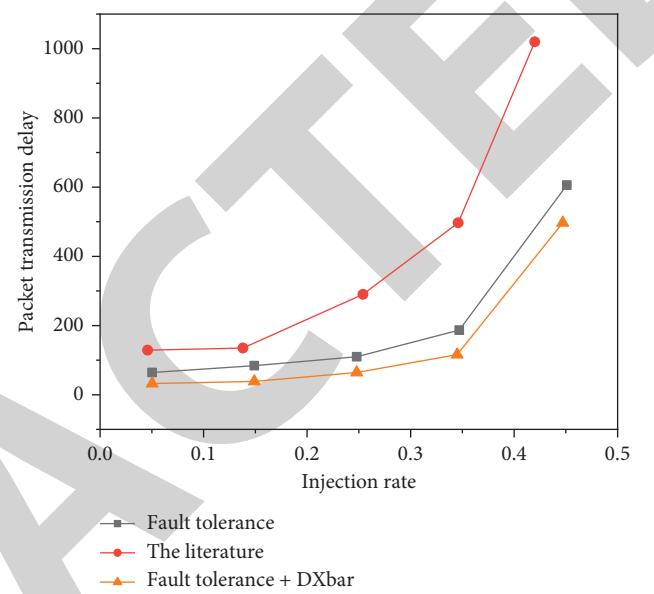


FIGURE 6: Comparison of packet transmission delay with two groups of faulty TSVs.

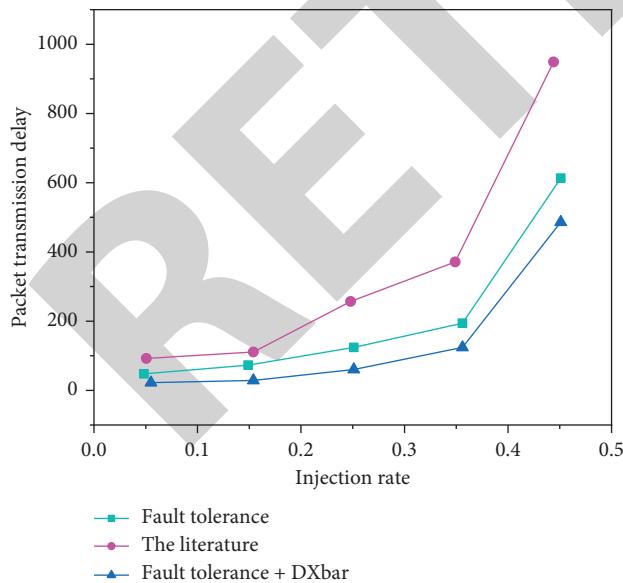


FIGURE 5: Comparison of packet transmission delays when a group of faulty TSVs is counted.

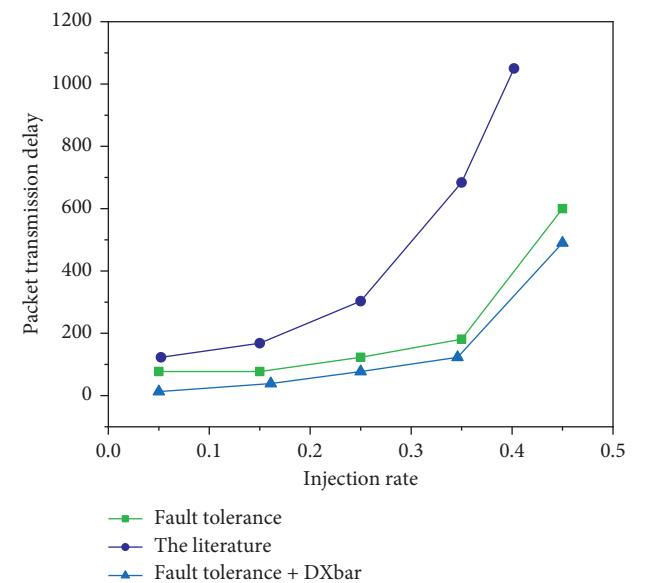


FIGURE 7: Comparison of packet transmission delays with three groups of faulty TSVs.

5. Conclusion

In order to ensure the reliability of the 3DNoC architecture, realize fault tolerance, and reduce the transmission delay of data packets, the author proposes that on the basis of the redundant bidirectional TSV design, the TSV router is designed as a double crossbar switch architecture, which realizes the fault tolerance of the original TSV and further reduces the network delay and power consumption. Moreover, the author adopts the design of double crossbar switches, which can be fault-tolerant to the crossbar switches, and the failure of any crossbar switch will not affect the transmission of data packets. The experimental results show that the author's design scheme is superior and improves the reliability of the 3DNoC system.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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