

Adwait Jog

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RESEARCH INTERESTS

My research interests lie in all aspects of computer architecture and systems, especially in memory systems and scheduling techniques for GPUs and CPU-GPU architectures.

EDUCATION

Pennsylvania State University, University Park, PA *Fall 2009 - Summer 2015*
Ph.D. in Computer Science and Engineering, GPA: 3.84/4
Advisors: Chita Das and Mahmut Kandemir

National Institute of Technology (NIT), Rourkela, India *Fall 2005 - Spring 2009*
Bachelor of Technology (*Hons.*) in Electronics and Instrumentation Engineering
Among Top 5 students in the University, Top 2 in the Department, GPA: 9.49/10

PROFESSIONAL EXPERIENCE

- **College of William and Mary** **Fall 2015 – Present**
Assistant Professor (tenure-track)
Williamsburg, VA
 - Leading a new computer architecture research group.
 - Teaching courses related to computer architecture.
- **Pennsylvania State University, Research Assistant** **Fall 2009 – Summer 2015**
Advisor: Prof. Chita Das, High Performance Computing Lab (HPCL) **University Park, PA**
 - Proposed techniques for efficient execution of multiple applications on next generation GPUs.
 - Proposed criticality-aware memory system for GPUs.
 - Proposed a coordinated scheduling and prefetching mechanism to improve GPU performance.
 - Proposed warp scheduling policies to mitigate contention in GPU memory system.
 - Traded-off non-volatility of STT-RAM for lower write latency and energy.
- **NVIDIA Research, Graduate Research Intern** **Summer 2013**
Manager: Steve Keckler **Santa Clara, CA**
Mentors: Evgeny Bolotin, Zvika Guz, Mike Parker
Researched on efficient execution of multiple contexts/applications on next generation GPUs. The results of this work are published in GPGPU 2014 (co-located with ASPLOS 2014).
- **Intel Labs, Graduate Research Intern** **Summer 2012**
Managers: Srihari Makineni, Ravi Iyer **Hillsboro, OR**
Mentors: Xiaowei Jiang, Li Zhao
Implemented and evaluated micro-architecture techniques for Intel's ultra-low power core (*Siskiyou*). This infrastructure is released to universities to perform research on energy-efficient architectures.
- **Intel Corp., Graduate Technical Intern** **Summer 2011**
Manager: Sridhar Lakshmanmoorthy **Hillsboro, OR**
Mentor: Ramadass Nagarajan
Performed detailed studies and proposed techniques for designing a QoS aware interconnect fabric for the Intel's next generation heterogeneous SoCs.

AWARDS and HONORS

- Outstanding Graduate Research Assistant Award, CSE, Penn State, 2014
- NVIDIA Graduate Fellowship 2013, Finalist
- Best Paper Nomination, PACT 2013 (One of the four papers nominated for the Best Paper Award)
- Student Travel Grants for attending ASPLOS (2014, 2013), ISCA (2015, 2013), MICRO 2014
- College of Engineering Fellowship, Penn State University, 2009
- Summer Research Fellowship, School of Computing, National University of Singapore (NUS), 2008
- Summer Research Fellowship, Indian Academy of Sciences (IAS), 2007
- Undergraduate Scholarship for being in Top 1% in All India Engineering Entrance Exam, 2005

PUBLICATIONS (Total Citations: 303, h-index: 6, as of Oct 2015)

(Google scholar: <https://scholar.google.com/citations?hl=en&user=9RgqL8gAAAAJ>)

[MEMSYS 2015] Adwait Jog, Onur Kayiran, Tuba Kesten, Ashutosh Pattnaik, Evgeny Bolotin, Niladri Chatterjee, Stephen W. Keckler, Mahmut T. Kandemir, Chita R. Das, *Anatomy of GPU Memory System for Multi-Application Execution*, In the Proceedings of 1st International Symposium on Memory Systems (MEMSYS), Washington, DC, Oct 2015

[Ph.D. Thesis 2015] Adwait Jog, *Design and Analysis of Scheduling Techniques for Throughput Processors*, Ph.D. Thesis, The Pennsylvania State University, University Park, PA, 2015

[ISCA 2015] Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Abhishek Bhowmick, Rachata Ausavarungnirun, Onur Mutlu, Chita Das, Mahmut Kandemir, Todd Mowry, *A Case for Core-Assisted Bottleneck Acceleration in GPUs: Enabling Efficient Data Compression*, In the Proceedings of 42nd International Symposium on Computer Architecture (ISCA), Portland, OR, June, 2015 **Acceptance rate: 58/305 \approx 19.1%, Citations (as per Google Scholar): 4**

[MICRO 2014] Onur Kayiran, Nachiappan CN, Adwait Jog, Rachata Ausavarungnirun, Mahmut Kandemir, Gabriel Loh, Onur Mutlu, Chita Das, *Managing GPU Concurrency in Heterogeneous CPU-GPU Architectures*, In the Proceedings of 47th International Symposium on Micro Architecture (MICRO), Cambridge, UK, Dec 2014 **Acceptance rate: 53/273 \approx 19.4%, Citations (as per Google Scholar): 12**

[PACT 2014] Wei Ding, Mahmut Kandemir, Diana Guttman, Adwait Jog, Chita Das, Praveen Yedlapalli, *Trading Cache Hit Rate for Memory Performance*, In the Proceedings of 23rd International Conference on Parallel Architectures and Compilation Techniques (PACT), Edmonton, Canada, August, 2014 **Acceptance rate: 37/144 \approx 25.7%, Citations (as per Google Scholar): 0**

[GPGPU 2014] Adwait Jog, Evgeny Bolotin, Zvika Guz, Mike Parker, Steve Keckler, Mahmut Kandemir, Chita Das, *Application-aware Memory System for Fair and Efficient Execution of Concurrent GPGPU Applications*, In the Proceedings of General-Purpose Computation on Graphics Processing Unit (GPGPU-7), co-located with ASPLOS, Salt Lake City, UT, USA, March, 2014 **Acceptance rate: 12/27 \approx 44.4%, Citations (as per Google Scholar): 11**

[PACT 2013, Best Paper Nominee] Onur Kayiran, Adwait Jog, Mahmut Kandemir, Chita Das, *Neither More Nor Less: Optimizing Thread-Level Parallelism for GPGPUs*, In the Proceedings of 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT), Edinburgh, Scotland, September, 2013 **Acceptance rate: 36/208 \approx 17.3%, Citations (as per Google Scholar): 60**

[ISCA 2013] Adwait Jog, Onur Kayiran, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *Orchestrated Scheduling and Prefetching for GPGPUs*, In the Proceedings of 40th International Symposium on Computer Architecture (ISCA), Tel Aviv, Israel, June, 2013 **Acceptance rate: 56/288 \approx 19.4%, Citations (as per Google Scholar): 58**

[ASPLOS 2013] **Adwait Jog**, Onur Kayiran, Nachiappan CN, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance*, In the Proceedings of 18th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, USA, March, 2013 *Acceptance rate: 44/191 \approx 23.0%, Citations (as per Google Scholar): 79*

[DAC 2012] **Adwait Jog**, Asit Mishra, Cong Xu, Yuan Xie, Vijaykrishnan Narayanan, Ravi Iyer, Chita Das, *Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs*, In the Proceedings of 49th Design Automation Conference (DAC), San Francisco, USA, June 2012 *Acceptance rate: 168/741 \approx 23%, Citations (as per Google Scholar): 79*

PATENTS

[US Patent] Evgeny Bolotin, Zvika Guz, **Adwait Jog**, Stephen W. Keckler, Mike Parker, Approach to Adaptive Allocation of Shared Resources in Computer Systems, United States Patent Application US20150163324 A1

TEACHING EXPERIENCE

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| • Instructor , CS780, GPU Architectures | Spring 2016 |
| • Instructor , CS780, Topics in Computer Architecture | Fall 2015 |
| • Co-Instructor , CMPEN 331, Computer Organization and Design | Fall 2014 |
| • Co-Instructor , CMPEN 331, Computer Organization and Design | Spring 2014 |
| • Teaching Assistant , CMPEN 431, Introduction to Computer Architecture | Spring 2010 |
| • Teaching Assistant , CMPEN 471, Logic Design of Digital Systems | Fall 2009 |

TALKS AND POSTER SESSIONS

- Anatomy of GPU Memory System for Multi-Application Execution,
 - MEMSYS 2015, Washington, DC, Oct 2015
- The Future of Parallel Computing with GPUs
 - The College of William and Mary, Feb 2015
 - University of Utah, Mar 2015
 - Temple University, Mar 2015
 - AMD Research, Mar 2015
 - UC Riverside, Apr 2015
 - Intel Labs, Apr 2015
- Application-aware Memory System for Fair and Efficient Execution of Concurrent GPU Applications,
 - GPGPU-7 Workshop (co-located with ASPLOS 2014), Salt Lake City, UT, March 2014
 - Intern Talk, NVIDIA Research, Santa Clara, CA, Sept 2013
- Mitigating and Masking the Limitations of GPU Memory Systems,
 - Intern Talk, NVIDIA Research, Santa Clara, CA, June 2013
- Orchestrated Scheduling and Prefetching for GPGPUs,
 - ISCA 2013, Tel Aviv, Israel, June 2013
- OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance,
 - ASPLOS 2013, Houston, TX, March 2013
- Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs,
 - DAC 2012, San Francisco, CA, June 2012
 - Poster presentation at IUCRC NEXYS Workshop, Pittsburgh, PA

PROFESSIONAL SERVICE AND MEMBERSHIPS

- Program Committee Member and Invited Reviewer, ICPP 2016
- Program Committee Member and Invited Reviewer, GPGPU9
- Co-organizer of the 1st Warp Scheduling Championship to be held with MICRO 2015
- Proceedings and Submission Chair, ANCS 2015
- Invited Reviewer (Journals):
 - ACM Transactions on Architecture and Code Optimization (TACO)
 - ACM Transactions on Parallel Computing (TOPC)
 - IEEE Transactions on Computers (TC)
 - ACM Transactions on Embedded Computing (TECS)
 - ACM Transactions on Design Automation of Electronic Systems (TODAES)
 - IEEE Journal on Computer Architecture Letters (CAL)
- Invited External Reviewer (Conferences): DAC 2013, HPCA 2013, MICRO 2012, and ICCD (2014, 2013)
- Member of ACM, IEEE, ACM SIGARCH

SKILLS AND SOFTWARE

- C, Perl/Bash Scripting, GPGPU-Sim, M5, R, MATLAB, GDB

GRADUATE COURSEWORK

Operating System Design	Topics in Computer Architecture	Performance Evaluation
Algorithm Design & Analysis	Computer Networks	Computer Vision
VLSI Digital Circuit	Programming Language Concepts	Applied Statistics
Multiprocessor Architecture	Compiler Construction	Computer Hardware Design
Data Structures & Algorithms	Regression Methods	Bioinformatics