BRAJESH KUMAR PATRO

CONTACT:9740867293, brajeshkp7@gmail.com

Verification and Emulation Engineer, 6+Years of Experience

PROFESSIONAL SYNOPSIS:

- About 7+ years of experience in Verification and Test benches in System Verilog and UVM and emulation.Lastly worked with harman connected services with intel client for the emulation with verification project.
- Knowledge of emulation model build with zebu and veloce emulator.
- Knowledge of **AHB,AXI5,Ethernet, APB,SPI, I2C protocol**.
- Knowledge of Code Coverage and Functional Coverage.
- Experience in SOC (communication Protocols) projects like **SPI, I2C .**
- Knowledge on ARC Processor and SOC verification concepts .
- Proficient in shell scripting .My work involves writing shell scripts to run multiple test case at a time to speed up the process, writing shell scripts to optimize gate level simulation .Updated makefile as 3 folds at run times as per the requirement.

Tools used: ncsim,xcelium,questasim,Verdi,Zebu,Veloce.simvision,imc,Xilinx vivado design suite, Verdi,Visualizer,Zebu,Veloce,bcompare, vmanager

Languages used :Verilog,System Verilog,UVM,C,Python and shell scripting

PROJECTS:

Harman project and experience :

Project :Emulation build of LTM and LCD (Harman(client-Intel) June 2023 -Aug 2024)

Woked in emulation build of lcd ,ltm and sm7 build projects where I created model build for two ips and understood the model build flow and involved in debugging work.

- **Responsibilities:**
- Waveform capture and debug using Verdi tool
- Python scripts developed for fetching the information from tracker log file.
- Building emulation model for ltm and lcd project.(Zebu and veloce for model build creation)
- Automation using python script to reduce the manual work

Project : UX IP verification(Sevitech,UST (Client-intel) May 2022 to may 2023)

UX quad is a form of serdes architecture .UX quad is a hard macro inside HSSI subsystem.It includes 4 instances of serdes phy hard ip,clockrx hard ip and various additional module

Responsibilities:

- Test case coding for different versions of transceiver serdes for different blocks like deterministic latency ,pma arbiter ,cpi sequencer,fluxtop.
- Coding Testbench components including reference model and checkers.Verification closure using Functional coverage & code coverage as closing criteria.
- Found bugs and reported to design team for pll block bug.

Cientra project and experience:

Project : LTS(Long tail support) for four SOCs and Camera module in Fillmore and Lemans SOC:(Apri l2021-September 2021- Cientra-client-Qualcomm):

Role:

1. Setting up development view and running with RTL sanity and VECTOR mode regression. (LTS)
2. Creation of smoke list for further regression analysis (LTS).
3. Creating config files for RadagastAU soc and running in latest baseline
4. Running separate test by creating development view which includes frequency plan and nominal tests. (Camera)
5. Debuging build failures (Camera)
6. Making toggle coverage 100 %(Camera)
7. Creating non tile and tile-based development view (Camera)

Key challenges:

1. 100 %Toggle coverage for Fillmore soc. (Camera)
2. Fixing file mismatch from one to another server. (LTS)

Achievements:

1. Fillmore soc was ready for tape out after reaching critical milestone of 100 % toggle coverage.

Memory Controller Functional Verification using System Verilog.(NXP client)

- Responsibilities:
- Testplan development
- Developing testbench architecture
- Coding Testbench components including reference model and checkers
- Verification closure using Functional coverage & code coverage as closing criteria.

Sevitech project and experience :

- **ADCQ subsystem verification: (Client :STmicroelctronics,Sevitech Ust) (January 2020-march 2021) Responsibilities:**
  - Understood the ADCQ subsystem Specification and devised a test plan.
  - Made class based verification environment in UVM.
  - Test case development and coverage models development.

  GLS(Gate level simulation july 2019-december 2020(UST sevitech)Responsibilities:
  - Testbench cleanup and fixing the RTL and Gate level TB mismatches
  - Correcting the checkers
  - Debugging the multi million gates design.
  - Simulating the test case for GLS with SDF.

Key Challenges and Identified Issues:

- Non-resetable flops, Dual port memories (simultaneously access), Huge delay in pre SDF and reset timing bugs etc.
- Debugging on optimized netlist.

- The dump size is very huge and debugging and tracing the signals requires much more time.
- Implemented on latest simulation environment reducing the simulation time 3 days to 1 day with optimized netlist.
- Got all memories initialized and also corrected internal probing in the checkers.
- Identified zero delay glitches causing simulation go wrong in the Riviera environment , causing simulation failure and data mismatch.

Incise projects and experience:

SOC verification: I2C peripheral subsystem (august 2018-May 2019)

- Developed C test cases to verify the BUS and Interrupts.
- Verify connectivity between I2C and processor.

SOC verification: SPI peripheral subsystem(August 2018 to December 2019) (CoreEL technology training project, Sandeepani school of Vlsi design)Responsibilities:

- Verify connectivity between SPI, processor.
- Understood booting process and Interrupt handling.
- Found bug while handling interrupt

SOC Verification of GMAC Ethernet (Sandeepani school of Vlsi design)Responsibilities:

- Verify the connectivity between processor and GMAC1 instance with c level test cases.

AMBA APB Bus Protocol Verification using UVM(Jan2018-Mar2018)(Sandeepani school of Vlsi design)

Description: The AMBA APB protocol is targeted at low-performance, suitable for low-frequency system designs.

Responsibilities:

- Made class based Verification environment in UVM .
- Developed test cases and assertion models.

AMBA AHB Bus Protocol Verification using UVM(Oct 2017-Dec 2017)(Sandeepani school of Vlsi design)

Description:The AMBA AHB protocol is targeted at high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed data transfer.

Responsibilities:

- To verify AHB protocol features Burst transfer, aligned address,pipelined operations and verify AHB Slave.
- Understand specifications and create test plan.
- Test case for verifying the design.

Asynchronous FIFO: (Jan 2017-Sep 2017 Sandeepani school of Vlsi design) Design of an Asynchronous First-In-First Out memory queue with control logic that performs management of the read and write pointers, generation of status flags like almost empty and almost full, and optional handshake signals for interfacing with the user logic.

Round Robin Arbiter: (July 2016-Dec 2016)(Sandeepani school of vlsi design)
Round Robin Arbiter: The aim of this project was to develop a Round Robin Arbiter to help schedule the processes/requests of four entities cyclically in a given priority order so as to ensure execution of all the requests in a cycle. The major blocks of this design are the Acknowledgement Register Block, Priority Logic, Feedback Logic and Output Logic. The priority assigned to the four entities is user defined and can be varied according to the requirements.

Software Tools: QuestaSim & Vivado. Hardware: Xilinx Zedboard

Research fellow, Indian Institute of Technology, Bhubaneswar(April 2015 to March 2016 in design innovation centre ,IIT bhuabaneswar)
Worked as project fellow in IIT Bhubaneswar (School of mechanical sciences) in a technical project of MHRD (Govt of India) under the guidance of Prof Dr Satyanarayana Panigrahi (Ph.D., IISC, Bengaluru). o Project titled "A vehicle mounted surveillance system for tracking and monitoring the vehicle positions and its surroundings ". o In the above project a Raspberry pi model B+ and various other processors like Arduino, were used for certain testing purposes. o Knowledge in python language while working with Raspberry Pi computer was required.

EDUCATIONAL QUALIFICATION

- **B.Tech.** in ETC From SILICON INSTITUTE OF TECHNOLOGY (B.P.T.U) in 2013 with 63.5%.