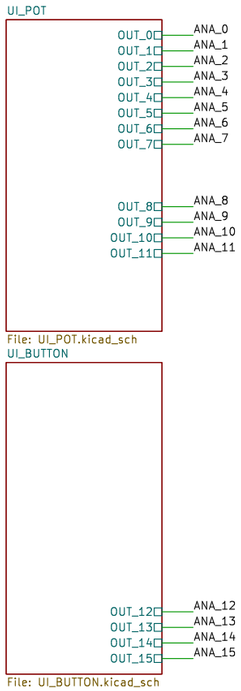
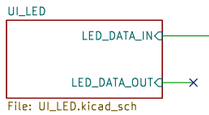
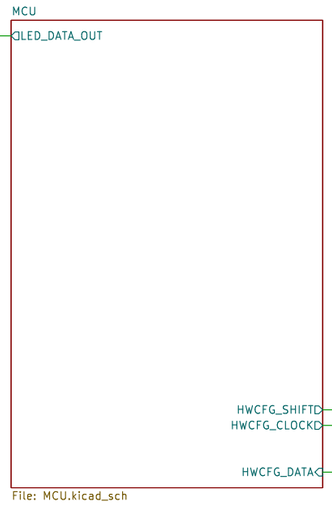
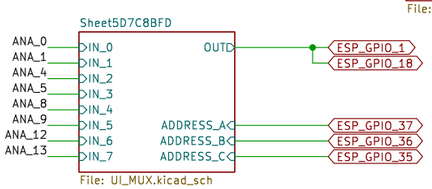
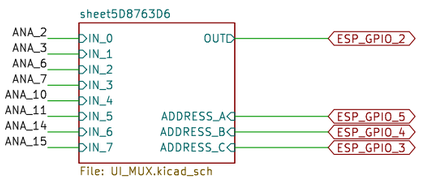










Common Sheets:
500 GRID
600 USB_POWER
700 MCU

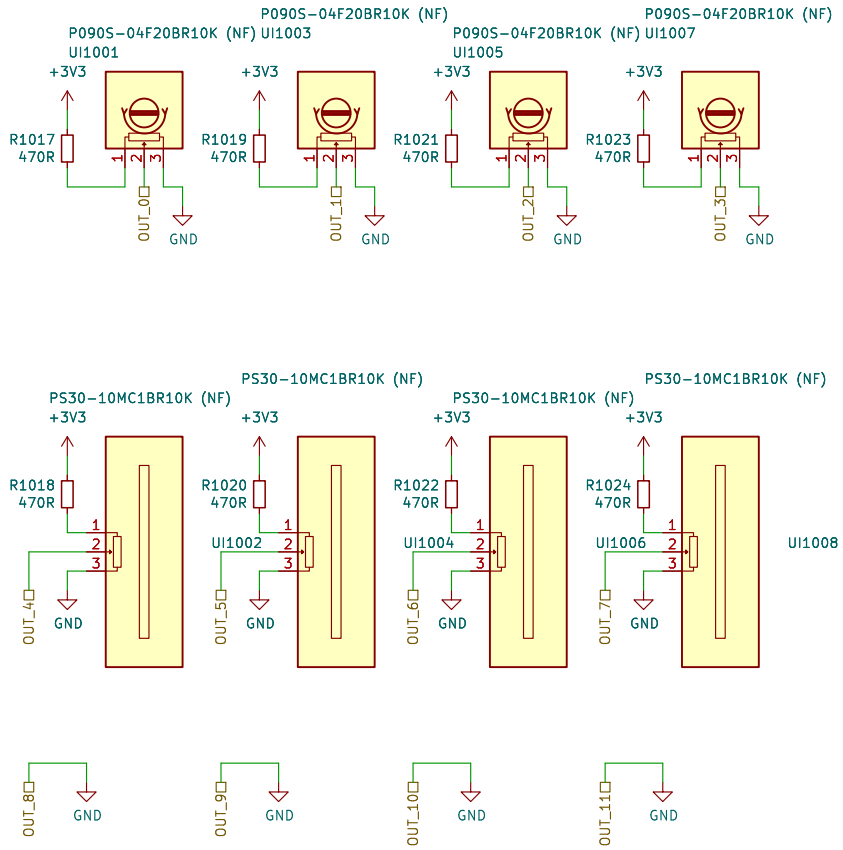
Module Specific:
800 HWCFG
900 LED
1000 UI

Sheet: /
File: PCBA-PBF4.kicad_sch

Title:

Size: A3 | Date: | **Rev:**
KiCad E.D.A. 8.0.4 | Id: 1/10

1000



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Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 2/10

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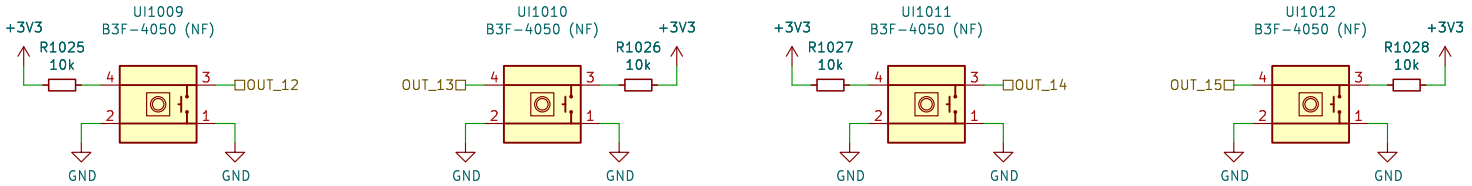
Simulation:

http://tinyurl.com/y229mty4



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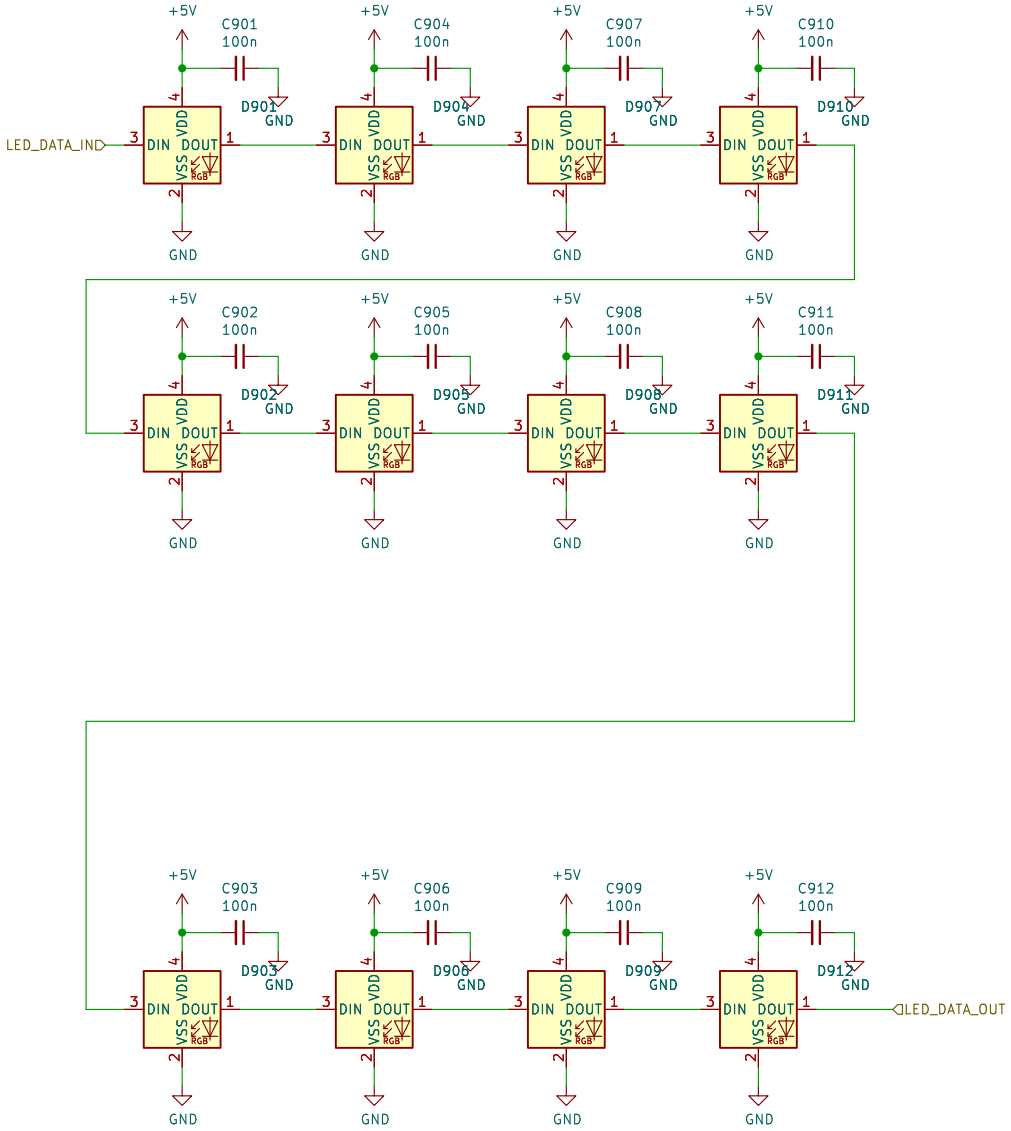
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 3/10

900



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Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 4/10

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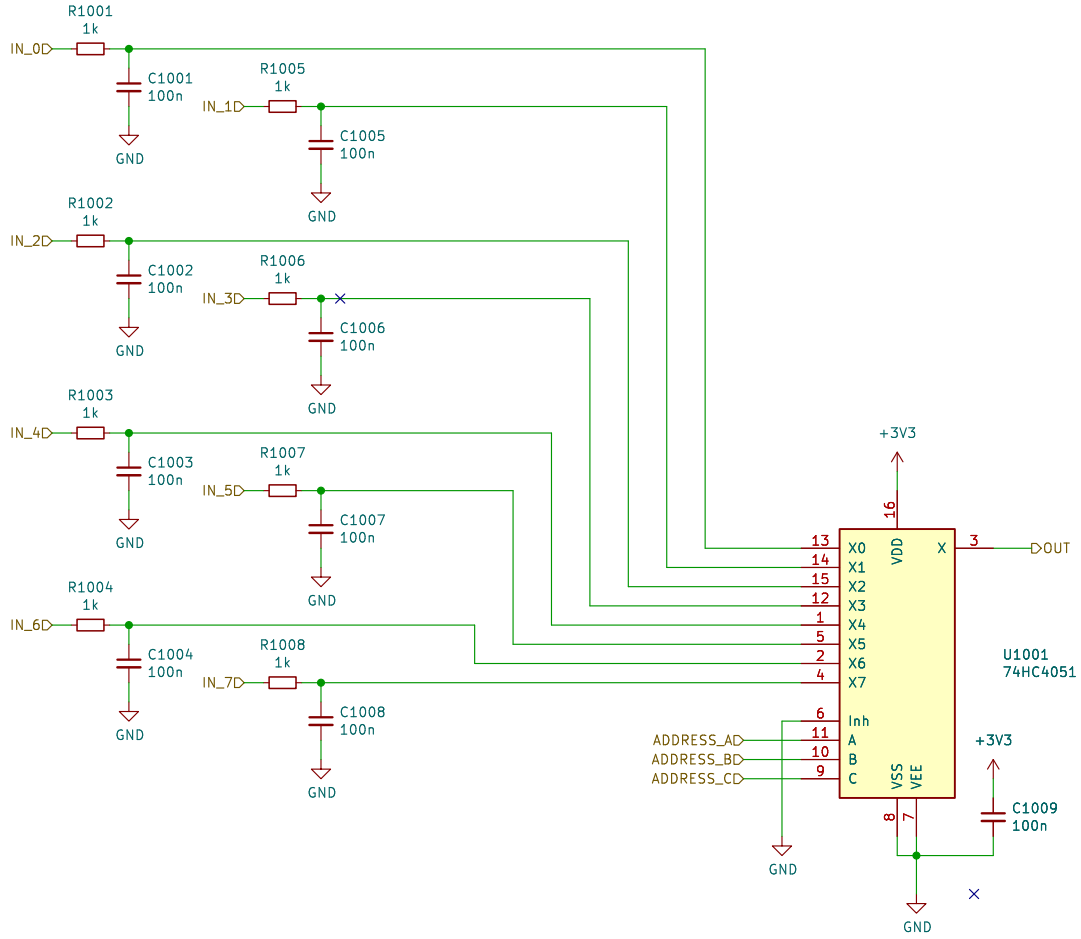

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Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 5/10

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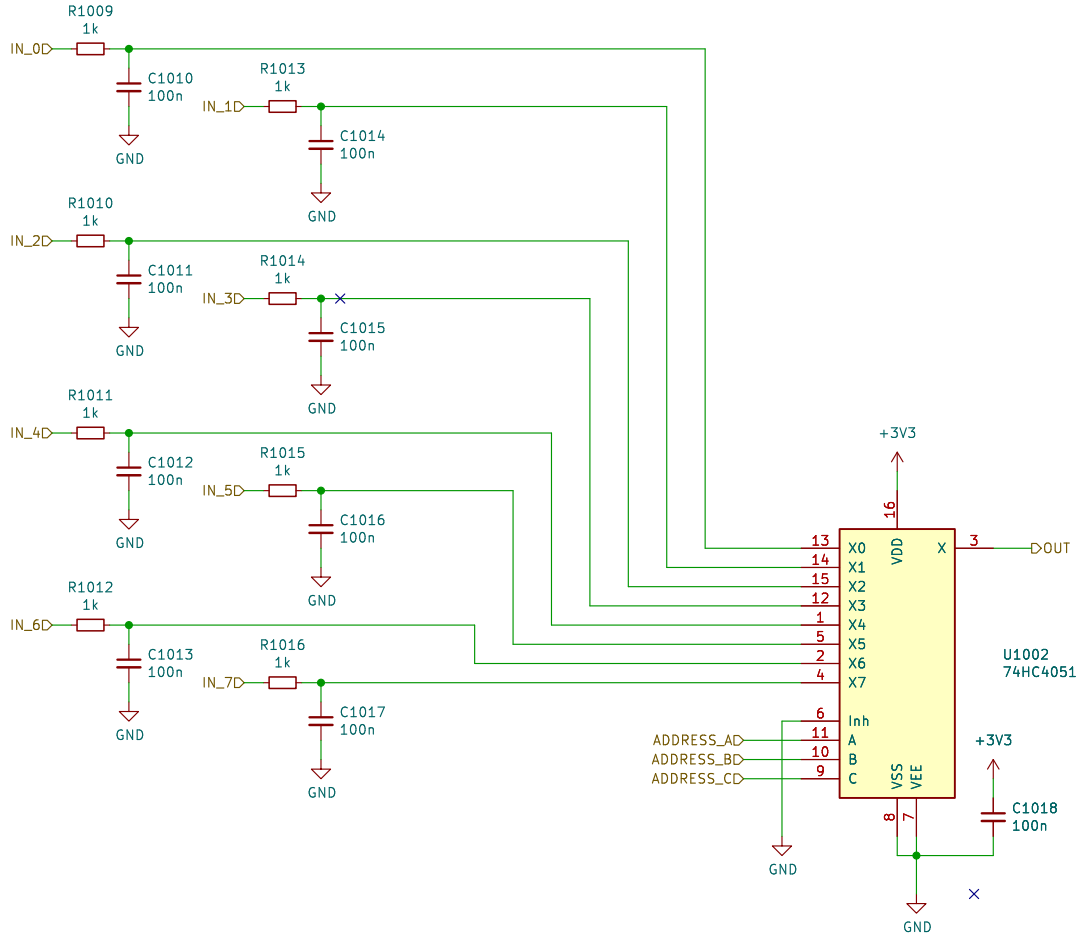

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Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 6/10

700

Sheet60F06FE1
USB_DP
USB_DN
USB_DATA_P
USB_DATA_N
File: USB_POWER.kicad_sch

+3V3
GZ2012D601TF
L702
PWR_FLAG
C743 10u
C746 1u
C747 100n
C749 100n
C751 100n
C752 100n
C753 10n
C754 1u
VDD_SPI
GND

J701
C5137195
U.FL-R-SMT-1(80)
L701 1n8
C739 3p9
C742 1p8
ESP_LNA

1.8nH LQG15HS1N8S02D
3.9pF GJM1555C1H3R9WB01D
1.8pF GJM1555C1H1R8BB01D

ESP32-S3
ESP_RESET
ESP_LNA
USB_DN
USB_DP
SPIHD
SPIWP
SPICS0
SPICLK
SPIQ
SPID
40MHz Y701
C748 10p
C750 10p
TCK
TDO
TDI
TMS
U0TXD
U0RXD
ESP_BOOT0
ESP_GPIO_1
ESP_GPIO_2
ESP_GPIO_3
ESP_GPIO_4
ESP_GPIO_5
RP_SPIO_RX
RP_SPIO_CS
RP_SPIO_TX
RP_SPIO_SCK
HWCFG_SHIFT
HWCFG_CLOCK
HWCFG_DATA
RP_SWDIO
RP_SWCLK
RP_CLK
ESP_GPIO_16
RP_INTERRUPT
ESP_GPIO_18
LED_DATA_OUT
ESP_GPIO_33
ESP_GPIO_34
ESP_GPIO_35
ESP_GPIO_36
ESP_GPIO_37
MAP_MODE
ESP_GPIO_45
ESP_GPIO_46
ESP_GPIO_47
ESP_GPIO_48
U704

LCSC:
TXM40M0004322HBCEO00T
S3240000091040JY

ESP_GPIO_47 TP706 TestPoint
ESP_GPIO_48 TP707 TestPoint
ESP_GPIO_34 TP708 TestPoint
ESP_GPIO_33 TP709 TestPoint
TP710 TestPoint

Programming Interface
RP_UART0_TX
RP_UART0_RX
U0TXD
U0RXD
1k R733
TMS
TCK
TDO
TDI
Conn_02x05_Odd_Even
J702

Mapmode switch
This pusbutton is acessible through the housing, activates USB bootloader.
R701 5k1
100n C757
R736 1k
SW701 C255807
MAP_MODE
Internal Pull-up

R735 5k1
SW702 C2905169
ESP_RESET
C758 1u

SW703 C2905169
ESP_BOOT0

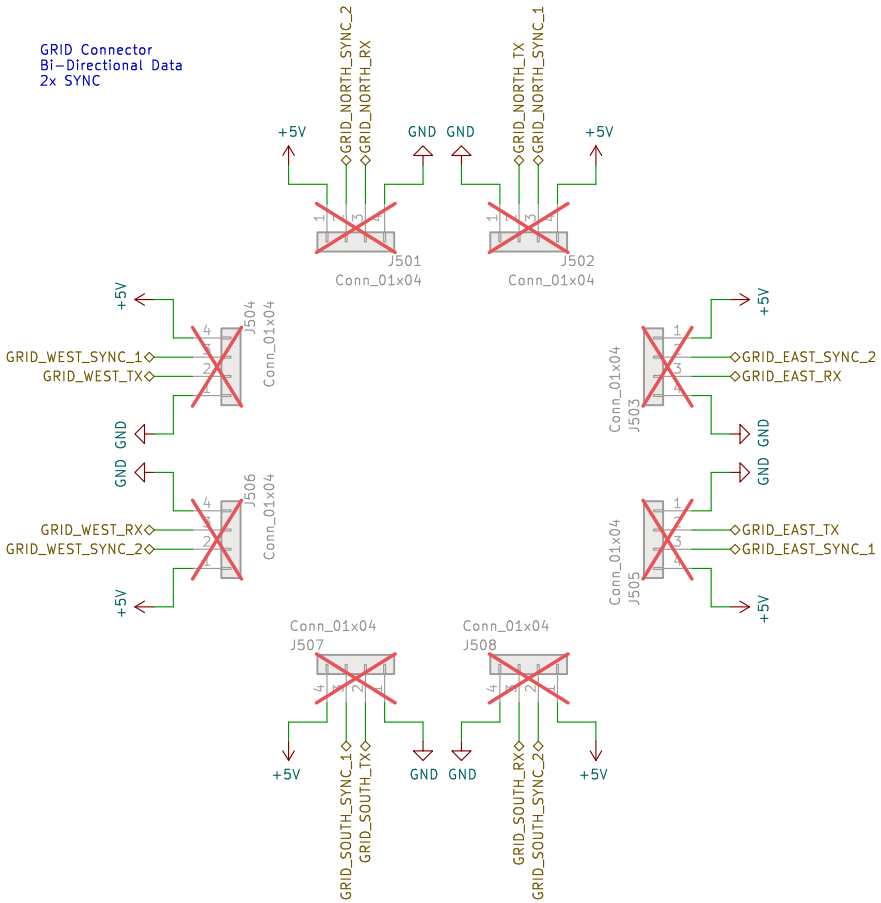
+1V1
+3V3
C731 100n
C732 100n
C733 1u
C734 1u
C735 100n
C736 100n
C737 100n
C738 100n
C740 100n
C741 100n
C744 100n
C745 100n
R729 5k1
RP_RUN
U703
RP2040
RUN
USB_DP
USB_DM
QSPI_SS
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
QSPI_SCLK
XIN
XOUT
SWCLK
SWD
TESTEN
VREG_VOUT
DVDD
IOVDD
USB_VDD
ADC_AVDD
VREG_IN
RP_UART0_TX
RP_UART0_RX
GRID_SOUTH_TX
GRID_WEST_RX
GRID_SYNC_2
GRID_WEST_TX
GRID_NORTH_RX
GRID_EAST_TX
GRID_SOUTH_RX
TP701 TestPoint
TP702 TestPoint
TP703 TestPoint
TP704 TestPoint
TP705 TestPoint
RP_SPIO_RX
RP_SPIO_CS
RP_SPIO_SCK
RP_SPIO_TX
RP_INTERRUPT
GRID_NORTH_TX
GRID_EAST_RX
GRID_SYNC_1

GRID Connector
Connector arrays for the interface boards on all four sides of the module.
sheet5D85C9EA
GRID_SYNC_1
GRID_WEST_TX
GRID_WEST_RX
GRID_SYNC_2
GRID_WEST_SYNC_1
GRID_WEST_TX
GRID_WEST_RX
GRID_WEST_SYNC_2
GRID_SOUTH_TX
GRID_SOUTH_RX
GRID_SOUTH_SYNC_1
GRID_SOUTH_TX
GRID_SOUTH_RX
GRID_SOUTH_SYNC_2
GRID_EAST_TX
GRID_EAST_RX
GRID_EAST_SYNC_1
GRID_EAST_TX
GRID_EAST_RX
GRID_EAST_SYNC_2
GRID_NORTH_TX
GRID_NORTH_RX
GRID_NORTH_SYNC_1
GRID_NORTH_TX
GRID_NORTH_RX
GRID_NORTH_SYNC_2
File: GRID.kicad_sch

J799
Conn_01x02

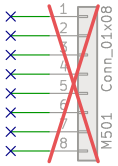
QSPI Flash memory
This memory can be accessed throgh the QSPI interface of the MCU. Can be used for configuration, static data or program execution.
R734 5k1
U705
W25Q64JVSSIQ
SPICS0
SPICLK
SPID
SPIQ
SPIWP
SPIHD
C755 1u
C756 100n

Sheet: /MCU/
File: MCU.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. 8.0.4
Id: 7/10



500

Board Mounting Pattern

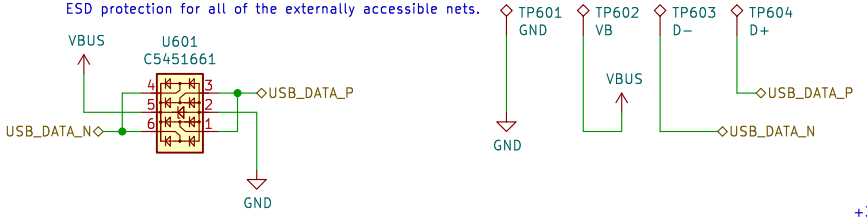


Sheet: /MCU/sheet5D85C9EA/ File: GRID.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 8/10

600

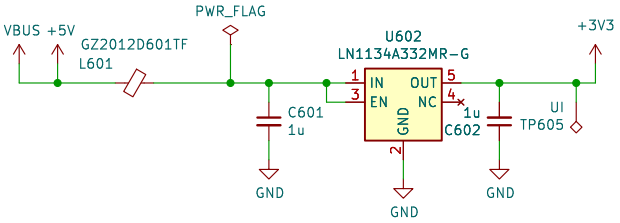
ESD Diodes

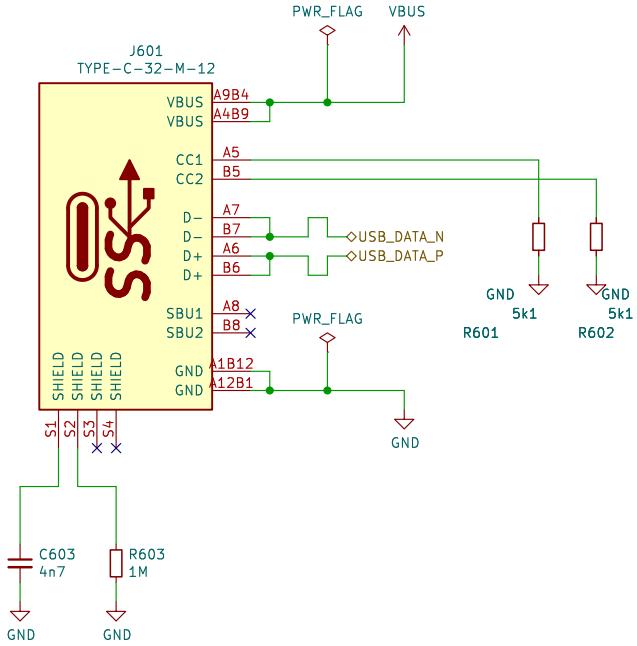
ESD protection for all of the externally accessible nets.



+3V3 LDO Regulators

Regulators for generating independent power rails for the microcontroller and the user interface.





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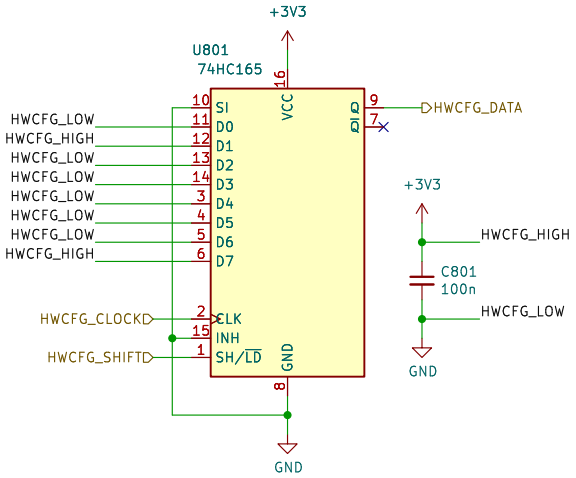
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 9/10

800



Board Identification

Grid firmware can identify the hardware and the board revision thorugh a 3 wire serial interface using one or more shift register as read only memory. The content of the memory is defined by pulling the inputs high or low through pcb traces or solderable configuration jumpers.

4b'Model + 4b'Revision + nb'Reserved (Multiple shift registers)

D0: MODEL (LSB)
D1: MODEL
D2: MODEL
D3: MODEL (MSB)
D4: REVISION (LSB)
D5: REVISION
D6: REVISION
D7: REVISION (MSB)

Model Codes (D3-D0):

Po16 0000
Bo16 0001
PBF4 0010
EN16 0011
...

Revision Codes (D7-D4):

RevA 0000
RevB 0001
RevC 0010
RevD 0011
...

Sheet: /HWCFG/		
File: HWCFG.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 10/10