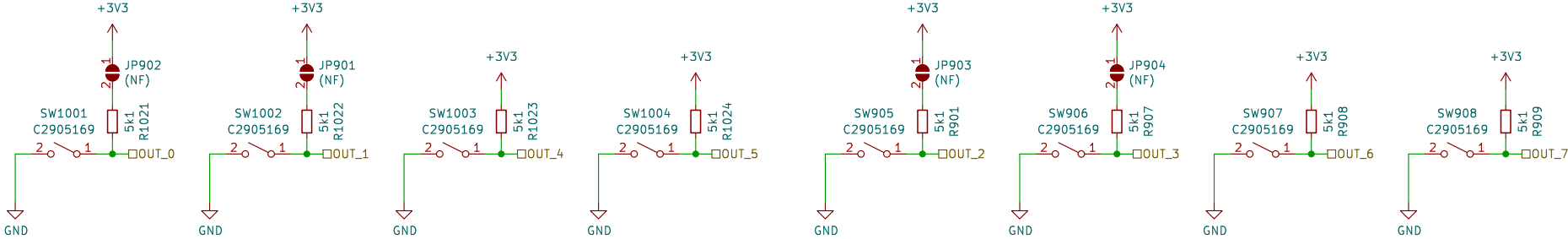
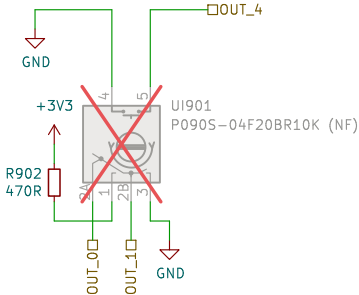


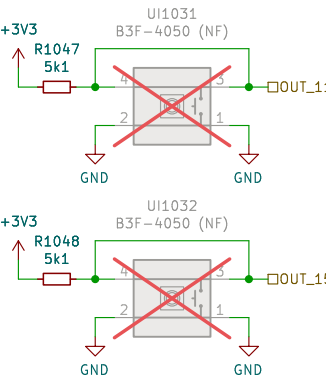
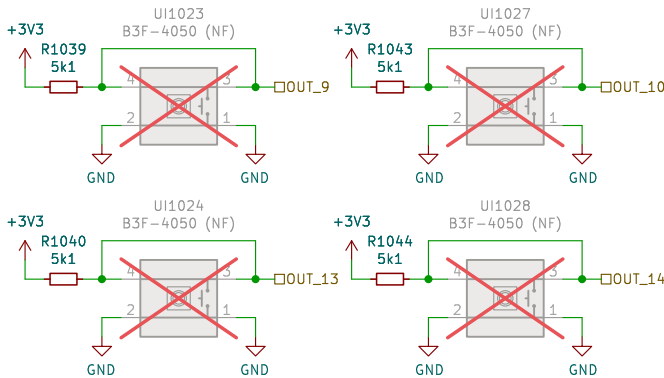
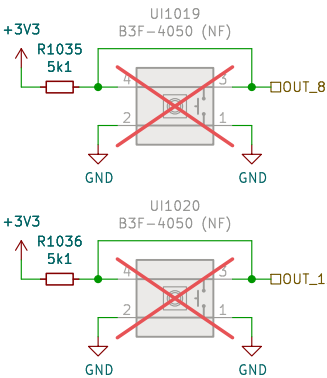
1000



Sheet: /UI_POT_BTN/ File: UI_POT_BTN.kicad_sch		
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Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.3		Id: 2/11

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Simulation:  
<http://tinyurl.com/y229mty4>



Sheet: /UI_BUTTON/ File: UI_BUTTON.kicad_sch		
Title:		
Size: A4	Date:	Rev:
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# 900



Sheet: /UI\_LED/  
File: UI\_LED.kicad\_sch

**Title:**

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**Rev:**

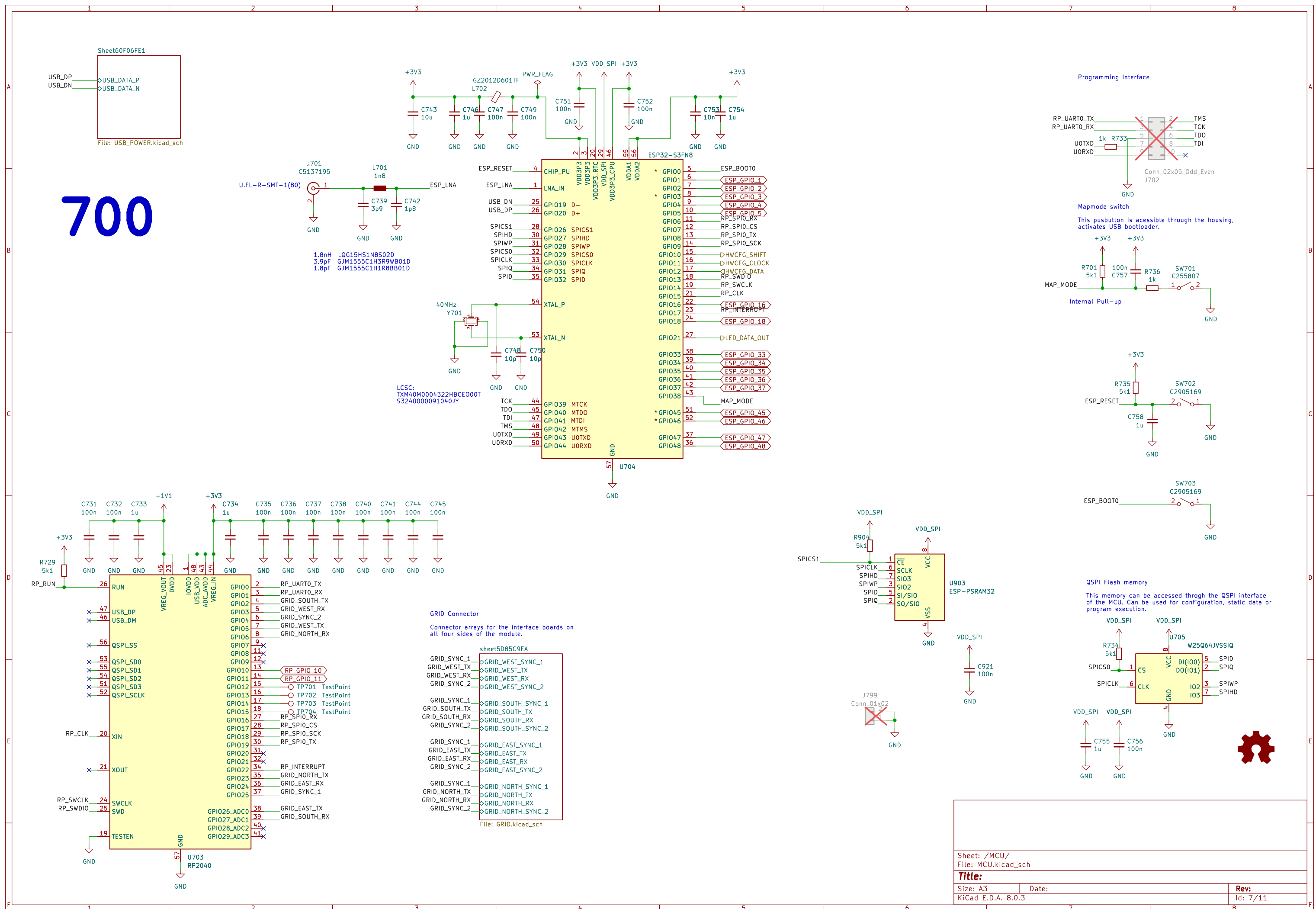
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500

GRID Connector  
Bi-Directional Data  
2x SYNC

Board Mounting Pattern



Sheet: /MCU/sheet5D85C9EA/ File: GRID.kicad_sch		
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**600**

**ESD Diodes**  
ESD protection for all of the externally accessible nets.

**+3V3 LDO Regulators**  
Regulators for generating independent power rails for the microcontroller and the user interface.

The schematic shows the power management circuit for the 600 board. It includes a USB Type-C connector (J601) with pins for VBUS, CC1, CC2, D-, D+, SBU1, SBU2, and SHIELD. The VBUS line is connected to a USB Type-C symbol and a USB Type-A symbol. The CC1 and CC2 pins are connected to a USB Type-C symbol. The D- and D+ pins are connected to USB\_DATA\_N and USB\_DATA\_P. The SBU1 and SBU2 pins are connected to PWR\_FLAG. The SHIELD pins are connected to GND. The circuit also includes a USB Type-A connector (J602) with pins for VBUS, D-, D+, and GND. The VBUS line is connected to a USB Type-A symbol and a USB Type-B symbol. The D- and D+ pins are connected to USB\_DATA\_N and USB\_DATA\_P. The circuit includes several components: U601 (C5451661) ESD diodes, U602 (LN1134A332MR-G) LDO regulator, C601 (1uF) capacitor, C602 (1uF) capacitor, C603 (4n7) capacitor, R601 (5k1) resistor, R602 (5k1) resistor, R603 (1M) resistor, and TP601 through TP605 test points. The power rails are labeled: VBUS, +5V, +3V3, and PWR\_FLAG. The ground is labeled GND.

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**800**

The schematic shows a 74HC165 shift register (U801) used for board identification. It has two input screens, LEFT SCREEN and RIGHT SCREEN, each with a jumper (JP801, JP802) and a pull-up resistor (R801, R802, 5k1) connected to +3V3. The shift register's clock inputs (CLK, INH, SH/LD) are connected to HWCFG\_CLOCKD, HWCFG\_SHIFTD, and GND respectively. Its data inputs (D0-D7) are connected to HWCFG\_LOW and HWCFG\_HIGH. The output (Q) is connected to HWCFG\_DATA. A capacitor C801 (100nF) is connected between HWCFG\_HIGH and HWCFG\_LOW.

**Board Identification**

Grid firmware can identify the hardware and the board revision through a 3 wire serial interface using one or more shift register as read only memory. The content of the memory is defined by pulling the inputs high or low through pcb traces or solderable configuration jumpers.

4b'Model + 4b'Revision + nb'Reserved (Multiple shift registers)

D0: MODEL (LSB)  
D1: MODEL  
D2: MODEL  
D3: MODEL (MSB)  
D4: REVISION (LSB)  
D5: REVISION  
D6: REVISION  
D7: REVISION (MSB)

**Model Codes (D3–D0):**

Po16 0000  
Bo16 0001  
PBF4 0010  
EN16 0011  
...

**Revision Codes (D7–D4):**

RevA 0000  
RevB 0001  
RevC 0010  
RevD 0011  
...

Grid firmware can identify the hardware and the board revision through a 3 wire serial interface using one or more shift register as read only memory. The content of the memory is defined by pulling the inputs high or low through pcb traces or solderable configuration jumpers.

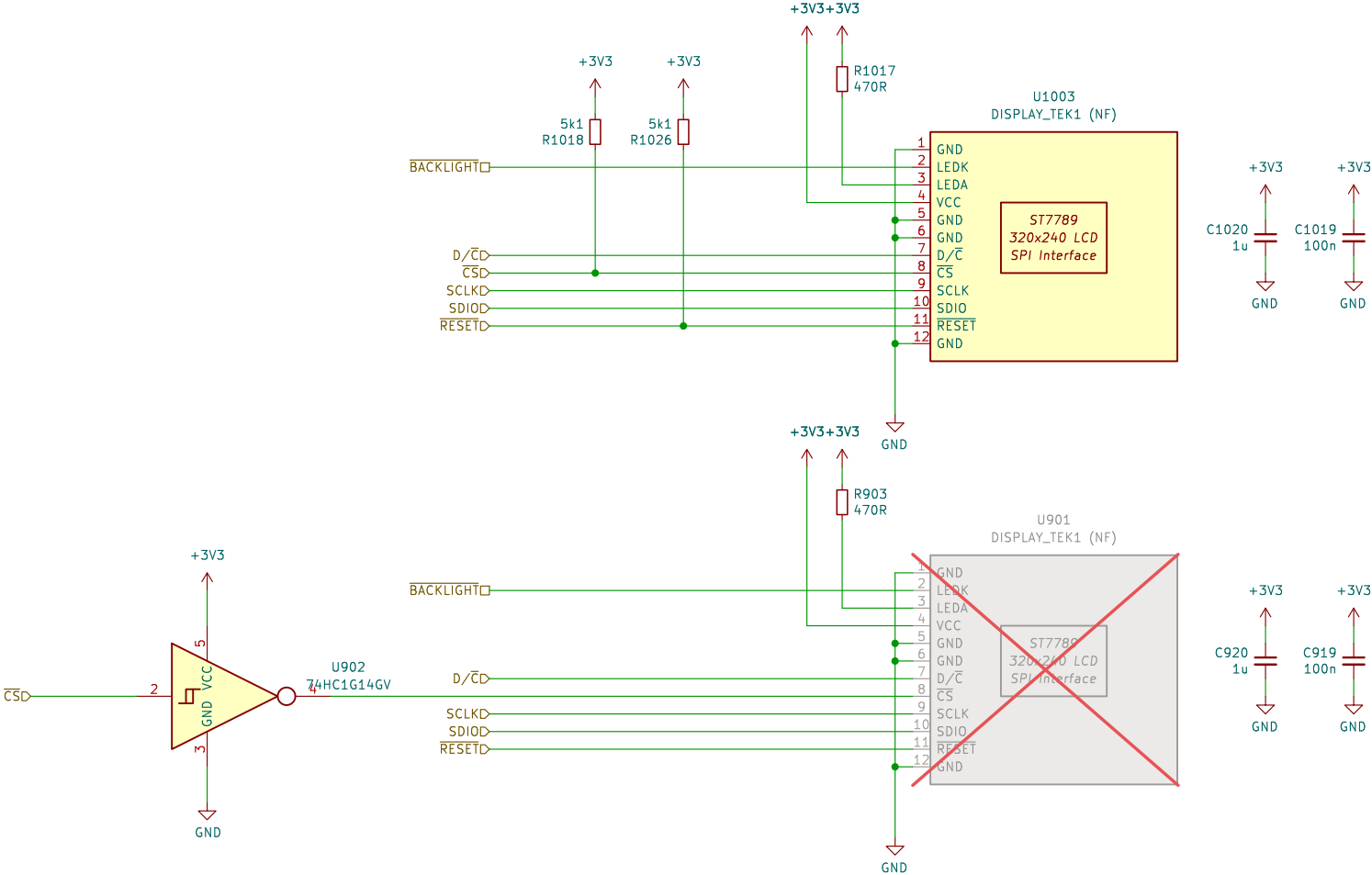
D0: MODEL (LSB)  
D1: MODEL  
D2: MODEL  
D3: MODEL (MSB)  
D4: REVISION (LSB)  
D5: REVISION  
D6: REVISION  
D7: REVISION (MSB)

Po16	0000
Bo16	0001
PBF4	0010
EN16	0011
...	

```
RevA 0000
RevB 0001
RevC 0010
RevD 0011
...
```

Sheet: /HWCFG/ File: HWCFG.kicad_sch	
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Sheet: /UI\_DISPLAY/  
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Date:

KiCad E.D.A. 8.0.3

**Rev:**

Id: 11/11