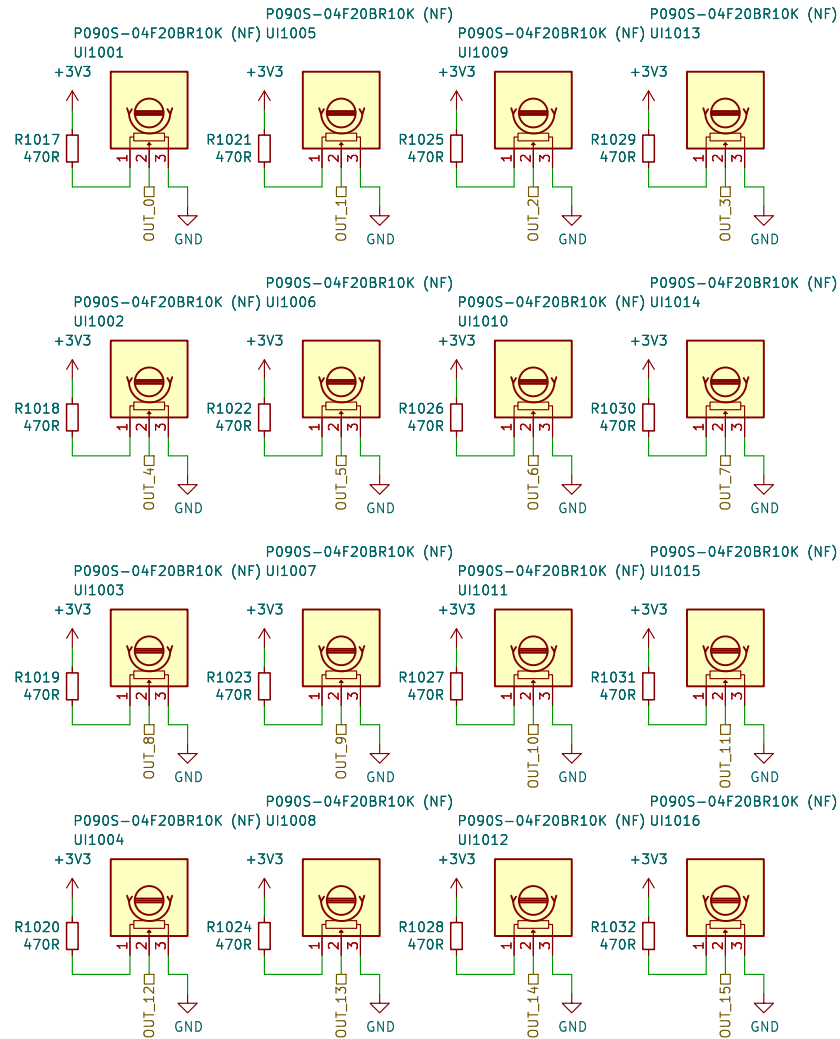


1000



Sheet: /UI_POT/
File: UI_POT.kicad_sch

Title:

Size: A4
KiCad E.D.A. kicad-cli 7.0.11+1

Date:

Rev:
Id: 2/10

1000

Simulation:
<http://tinyurl.com/y229mty4>



Sheet: /UI_BUTTON/
File: UI_BUTTON.kicad_sch

Title:

Size: A4
KiCad E.D.A. kicad-cli 7.0.11+1

Date:

Rev:

Id: 3/10

900



Sheet: /UI_LED/
File: UI_LED.kicad_sch

Title:

Size: A4
KiCad E.D.A. kicad-cli 7.0.11+1

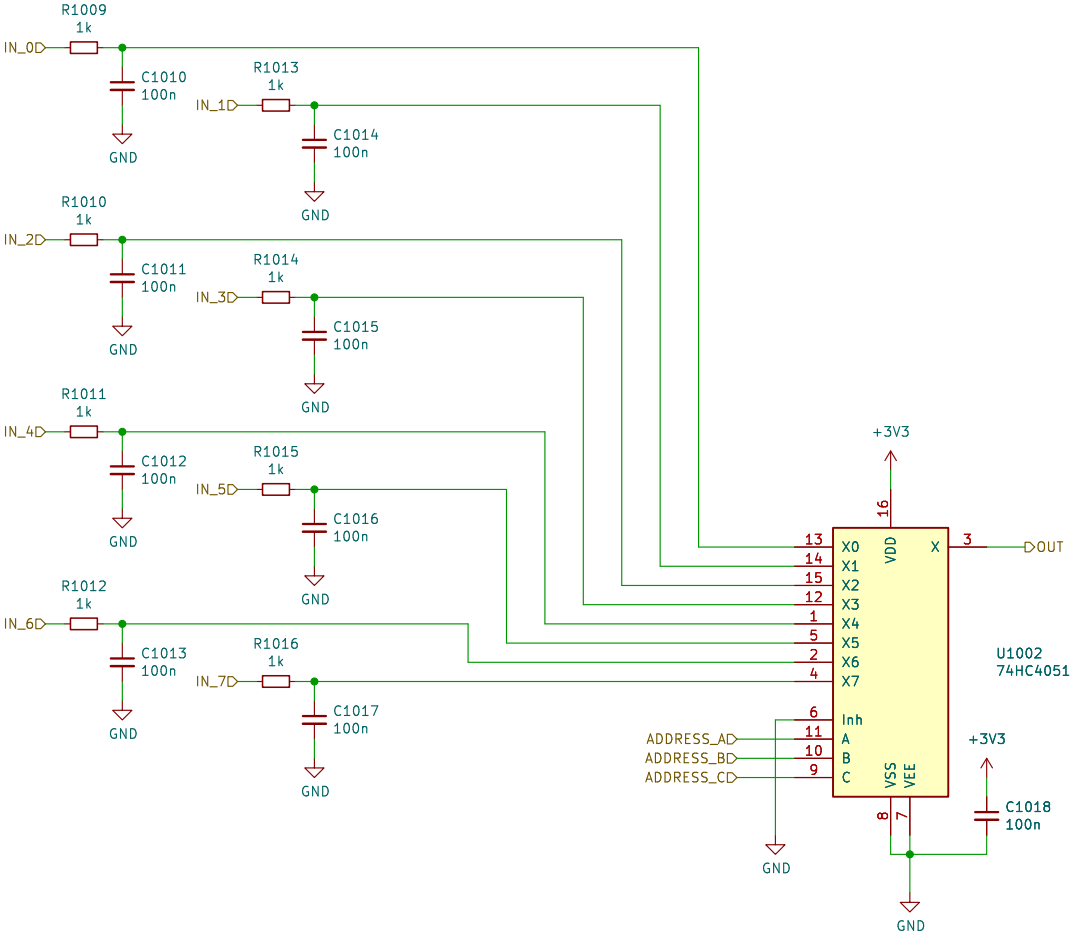
Date:

Rev:
Id: 4/10

1000



1000





500

GRID Connector
Bi-Directional Data
2x SYNC



Board Mounting Pattern



| | | |
|--|-------|----------|
| Sheet: /MCU/sheet5D85C9EA/ File: GRID.kicad_sch | | |
| Title: | | |
| Size: A4 | Date: | Rev: |
| KiCad E.D.A. kicad-cli 7.0.11+1 | | Id: 8/10 |

600

ESD Diodes

ESD protection for all of the externally accessible nets.



+3V3 LDO Regulators

Regulators for generating independent power rails for the microcontroller and the user interface.



Sheet: /MCU/Sheet60F06FE1/
File: USB_POWER.kicad_sch

Title:

Size: A4

Date:

KiCad E.D.A. kicad-cli 7.0.11+1

Rev:

Id: 9/10

The schematic shows a 74HC165 shift register (U801) used for board identification. The clock input (CLK, pin 2) is connected to HWCFG_CLOCKD. The inhibit input (INH, pin 15) is connected to HWCFG_SHIFTD. The serial input (SI, pin 10) is pulled up to +3V3 by resistor R801 (5k1) through jumper JP801 (NF), which is labeled "OPEN IF BU16". The parallel inputs D0-D7 are connected to HWCFG_LOW (pins 11, 12, 13, 14, 3, 4, 5, 6) and HWCFG_HIGH (pin 1). The output Q (pin 9) is connected to HWCFG_DATA through jumper JP701 (NF), which is labeled "CLOSED IF PB44". Resistor R702 (5k1) pulls down the signal at JP701. Power pins VCC (pin 16) and GND (pin 8) are also shown.

800

Board Identification

Grid firmware can identify the hardware and the board revision thorough a 3 wire serial interface using one or more shift register as read only memory. The content of the memory is defined by pulling the inputs high or low through pcb traces or solderable configuration jumpers.

4b'Model + 4b'Revision + nb'Reserved (Multiple shift registers)

D0: MODEL (LSB)
 D1: MODEL
 D2: MODEL
 D3: MODEL (MSB)
 D4: REVISION (LSB)
 D5: REVISION
 D6: REVISION
 D7: REVISION (MSB)

Model Codes (D3–D0):

```
Po16 0000
Bo16 0001
PBF4 0010
EN16 0011
...
```

Revision Codes (D7–D4):

```
RevA 0000
RevB 0001
RevC 0010
RevD 0011
...
```

| | | |
|---|--------------------|-----------|
| | | |
| Sheet: /HWCFG/ File: HWCFG.kicad_sch | | |
| Title: | | |
| Size: A4 | Date: | Rev: |
| KiCad E.D.A. | kicad-cli 7.0.11+1 | Id: 10/10 |

Grid firmware can identify the hardware and the board revision through a 3 wire serial interface using one or more shift register as read only memory. The content of the memory is defined by pulling the inputs high or low through pcb traces or solderable configuration jumpers.

D0: MODEL (LSB)
D1: MODEL
D2: MODEL
D3: MODEL (MSB)
D4: REVISION (LSB)
D5: REVISION
D6: REVISION
D7: REVISION (MSB)

| | |
|------|------|
| Po16 | 0000 |
| Bo16 | 0001 |
| PBF4 | 0010 |
| EN16 | 0011 |
| ... | |

```
RevA 0000
RevB 0001
RevC 0010
RevD 0011
...
```

| | |
|---|-----------|
| | |
| Sheet: /HWCFG/ File: HWCFG.kicad_sch | |
| Title: | |
| Size: A4 | Date: |
| KiCad E.D.A. kicad-cli 7.0.11+1 | Id: 10/10 |