

## Experiment 1: Differential Pair Current-Voltage Characteristics

- Construct either an nMOS or pMOS differential pair from Fig. 7.1.
- Set the bias voltage  $V_b$  so the bias current is just at or slightly below threshold
- Set  $V_2$  to a value sufficiently far away from the appropriate power supply rail so the bias transistor is saturated.
- With full power supply across the diff pair, measure each of the output currents,  $I_1$  and  $I_2$ , and the common-source node voltage  $V$ , as you sweep  $V_1$  from a few tenths of a volt below  $V_2$  to a few tenths of a volt above  $V_2$ .
  - Repeat this process for at least two more values of  $V_2$  are still keep the bias transistor saturated.
  - Include LTspice schematic(s) (**FIG 1**)
- Include a single plot showing  $I_1$ ,  $I_2$ ,  $I_1 - I_2$ , and  $I_1 + I_2$ , as function of  $V_1 - V_2$  for all three values of  $V_2$  you used (twelve curves on the same plot that will be practically indistinguishable) (**FIG 2**)
  - Q: Do the current voltage characteristics change significantly as  $V_2$  changes?
- Include a plot showing the common source node voltage  $V$ , as function of  $V_1 - V_2$  for all three values of  $V_2$  (**FIG 3**)
  - Q: How does the value of  $V$  change as  $V_1$  goes from below  $V_2$  to above it?
- For each of the three values of  $V_2$  you used, fit a straight line to the plot of  $I_1 - I_2$  as function of  $V_1 - V_2$  around the region where  $V_1 \approx V_2$  ( $V_1 - V_2 \approx 0$ ) (**FIG 4**) (might be 3 separate plots need to check with Brad)
  - The slope should be  $\approx$  equal to the incremental differential-mode transconductance gain of the diff pair (look at lab for eq.)
  - Does the value of the diff-mode  $g_m$  change significantly as  $V_2$  changes?
- Set bias voltage  $V_b$  so the bias current is above threshold. For 1 value of  $V_2$  that is far enough away from the power supply rail to keep the bias transistor saturated, perform the same measurements as before. (Might want to increase the range you sweep  $V_1 - V_2$  slightly. (**FIG 5 FIG 6 FIG 7**)
  - Q: how does the behavior of the circuit change as the bias current changes from weak or moderate inversion to strong inversion?