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Information technology - Serial Attached SCSI - 3 (SAS-3)

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American National Standard
for Information Technology

Serial Attached SCSI - 3 (SAS-3)

Secretariat
Information Technology Industry Council

Approved mm.dd.yy

American National Standards Institute, Inc.

ABSTRACT

This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer - 2 (SPL-2) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 3 (SAS-3) and beyond. Prior to this standard, the protocol layer was included with the physical layer. This standard is intended to be used in conjunction with SCSI and ATA command set standards.

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Revision Information

R.0 Revision SAS3r00 (08 November 2011)

First release of SAS-3. The project proposal was 10-117r1.
Incorporated these:

a) this revision contains the physical contents of the SAS-2.1 standard;
b) 11-093r2 SAS-3 MultiLink connector (Alvin Cox, Seagate);
c) 11-100r0 Link Rate Long-Term Specs (Mark Seidel, Intel); and
d) 11=221r8 SAS-3 Electrical Spec (Kevin Witt, Maxim).

R.1 Revision SAS3r01 (23 April 2012)

Incorporated these:

a) 12-160r1 SCRAMBLED_0 pattern length for WDP (Mathieu Gagnon, PMC-Sierra); and
b) 12-015r5 Active Cable Electrical Characteristics (Gourgen Oganessyan, Intersel).

R.2 Revision SAS3r02 (17 July 2012)

Incorporated these:

a) 12-226r1 SAS-3 12 Gbps transmitter requirement updates (Alvin Cox , Seagate);
b) 12-249r2 SAS-3 Tranmitter coefficient ranges (Mathieu Gagnon, PMC Sierra);
c) 12-252r1 SAS-3 Compliance and measurement points (Mathieu Gagnon, PMC Sierra);
d) 12-253r1 SAS-3 Reference transmitter (Mathieu Gagnon, PMC Sierra); and
e) update reference of SPL to SPL-2 in figure 1.

R.2a Revision SAS3r02 (26 July 2012)

Incorporated these:

a) Added editors notes to indicated format changes of lists and tables; and
b) Corrected the v_{HL} measurement interval from 20T to 80T.

R.3 Revision SAS3r03 (18 October 2012)

Incorporated these:

a) 12-242r6 SAS-3 Transmitter device compliance [Gagnon, PMC Sierra];
b) 12-243r6 SAS-3 TxRx connection compliance [Gagnon, PMC Sierra];
c) 12-244r6 SAS-3 Receiver device compliance [Gagnon, PMC Sierra];
d) 12-293r4 SAS PHY: End-to-End Compliance Methodology and Specification [Gagnon, PMC Sierra];
e) 12-298r2 SAS-3 Active Cable Output Amplitude [Oganessyan, Intersel];
f) 12-299r2 SAS-3 addition of SFF-8639 receptacle connector [Cox, Seagate];
g) 12-310r0 SAS-3 Mini SAS HD 4i fanout cable assembly wiring diagrams [Rost, Molex];
h) 12-312r3 SAS-3 Reference TxRx connection segments [Gagnon, PMC Sierra]; and
i) 12-365r2 Transmitter device A.C. coupling requirements for CT [Cox, Seagate].

R.4 Revision SAS3r04 (8 November 2012)

Incorporated these:

a) 12-443r0 SAS-3 Preset +/-1.5 dB [Newman, LSI]
b) 12-444r1 SAS-3 addition of RJ for trained 12 Gbps stressed receiver test [Cox, Seagate]
c) 12-445r0 SAS-3 reference receiver peaking and reference transmitter coefficient limits [Gagnon, PMC Sierra]; and
d) corrections to the incorporation of 12-244r6.

Foreword (This foreword is not part of this standard)

This standard defines the physical layer of the Serial Attached SCSI (SAS) interconnect.

This standard contains five annexes. Annexes A and B are normative and are considered part of this standard. Annexes C through E are informative and are not considered part of this standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, International Committee for Information Technology Standards, Information Technology Institute, 1101 K Street, NW, Suite 610, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by the International Committee for Information Technology Standards (INCITS). Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, INCITS had the following members:

INCITS Technical Committee T10 on SCSI Storage Interfaces, which developed and reviewed this standard, had the following members:

John B. Lohmeyer, Chair Mark S. Evans, Vice-Chair Ralph O. Weber, Secretary

Introduction

This standard defines the Serial Attached SCSI (SAS) interconnect.

The standard is organized as follows:

Clause 1 (Scope) describes the relationship of this standard to the SCSI and ATA families of standards.
Clause 2 (Normative references) provides references to other standards and documents.
Clause 3 (Definitions, symbols, abbreviations, keywords, and conventions) defines terms and conventions used throughout this standard.
Clause 4 (General) describes the SAS physical architecture.
Clause 5 (Physical layer) describes the physical layer. It describes passive interconnect components (connectors, cables, and backplanes), the transmitter device and receiver device electrical characteristics, and out of band (OOB) signals,
Normative Annex A (Jitter tolerance pattern (JTPAT)) describes the jitter tolerance patterns.
Normative Annex B (SASWDP) includes the simulation program used for transmitter device and receiver device compliance.
Informative Annex C (StatEye) includes a simulation program that may be used for TxRx connection compliance.
Informative Annex E (Signal performance measurements) describes signal measurement techniques.
Informative Annex F (Description of the included Touchstone models) provides information about how S-parameter models included with this standard were derived.
Informative Annex G (Mini SAS 4x active cable assembly power supply and voltage detection circuitry) provides a sample circuit diagram for detecting the presence of a Mini SAS 4x active cable assembly.
Informative Annex H (SAS icons) defines the SAS icons.

1 Scope

The SCSI family of standards provides for many different transport protocols that define the rules for exchanging information between different SCSI devices. This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer - 2 (SPL-2) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 3 (SAS-3) and beyond, defining the rules for exchanging information between SCSI devices using a serial interconnect. Other SCSI transport protocol standards define the rules for exchanging information between SCSI devices using other interconnects.

Figure 1 shows the relationship of this standard to the other standards and related projects in the SCSI family of standards.

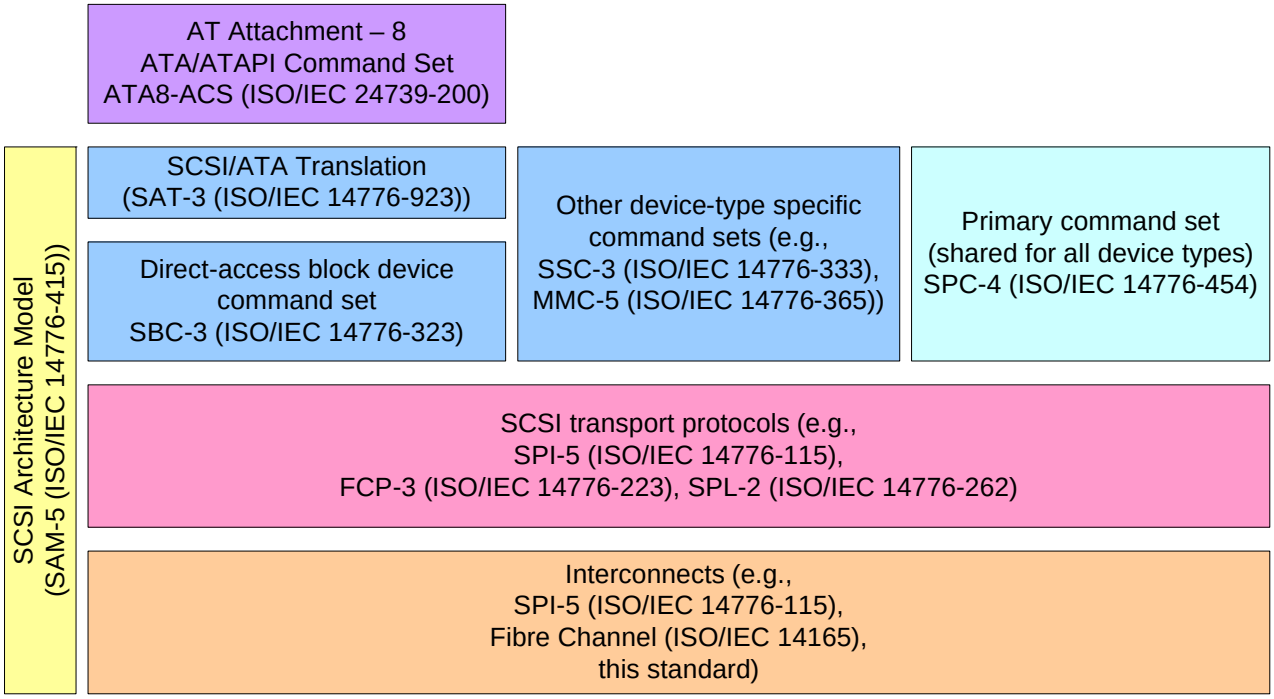

Figure 1 — SCSI document relationships

Figure 2 shows the relationship of this standard to other standards and related projects in the ATA family of standards.

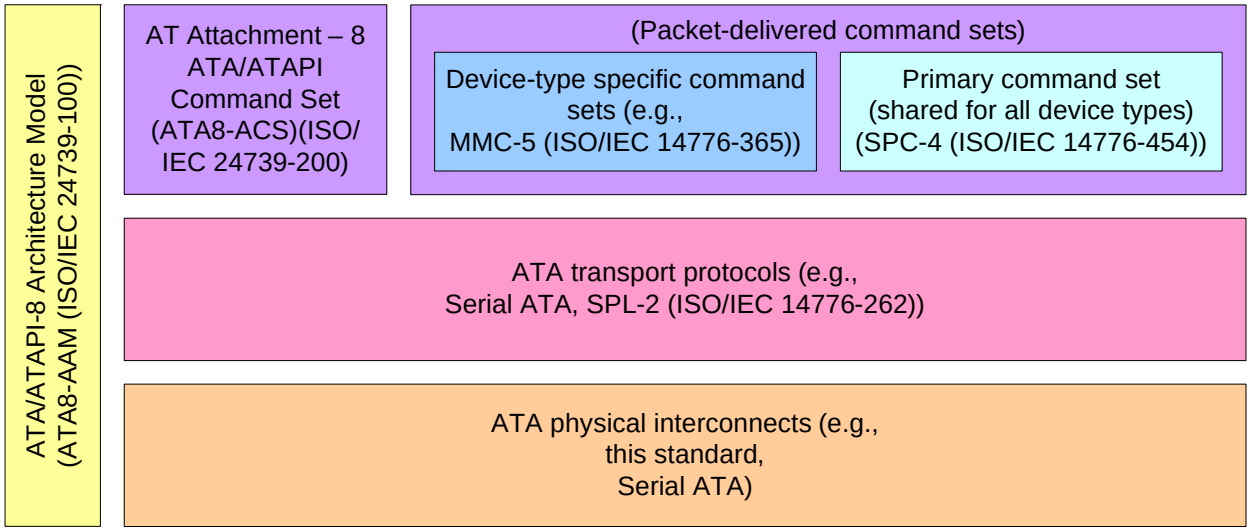

Figure 2 — ATA document relationships

Figure 1 and figure 2 show the general relationship of the documents to one another, and do not imply a relationship such as a hierarchy, protocol stack or system architecture.

These standards specify the interfaces, functions and operations necessary to ensure interoperability between conforming implementations. This standard is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

2 Normative references

2.1 Normative references

Referenced standards and specifications contain provisions that, by reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents may be obtained from ANSI:

a) approved ANSI standards;
b) approved and draft international and regional standards (e.g., ISO, IEC); and
c) approved and draft foreign standards (e.g., JIS and DIN).

For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax) or via the World Wide Web at http://www.ansi.org.

Additional availability contact information is provided below as needed.

Table 1 shows standards bodies and their web sites.

Table 1 — Standards bodies

Abbreviation	Standards body	Web site
ANSI®	American National Standards Institute	http://www.ansi.org
DIN	German Institute for Standardization	http://www.din.de
IEC®	International Electrotechnical Commission	http://www.iec.ch
IEEE®	Institute of Electrical and Electronics Engineers	http://www.ieee.org
INCITS	International Committee for Information Technology Standards	http://www.incits.org
ISO®	International Organization for Standardization	http://www.iso.ch
ITIC	Information Technology Industry Council	http://www.itic.org
JIS	Japanese Industrial Standards Committee	http://www.jisc.co.jp
T10	INCITS T10 SCSI storage interfaces	http://www.t10.org
T11	INCITS T11 Fibre Channel interfaces	http://www.t11.org
T13	INCITS T13 ATA storage interface	http://www.t13.org

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NOTE 2 - ISO is a registered trademark of the International Organization for Standardization.

NOTE 3 - IEC is a registered trademark of the International Electrotechnical Commission.

NOTE 4 - IEEE is a registered trademark of the Institute of Electrical Electronics Engineers, Inc.

2.2 Approved references

At the time of publication, the following referenced standards or technical reports were approved:

ANSI INCITS TR-35-2004, *Methodologies for Jitter and Signal Quality Specification (MJSQ)*. When MJSQ is referenced from this standard, the FC Port terminology used within MJSQ should be substituted with SAS phy terminology.

IEC 60169-15, First edition 1979-01, *Radio-frequency connectors. Part 15: R.F. coaxial connectors with inner diameter of outer conductor 4.13 mm (0.163 in) with screw coupling — Characteristic impedance 50 ohms (Type SMA)*.

ANSI INCITS 451-2008, *Information technology - AT Attachment-8 ATA/ATAPI Architecture Model (ATA8-AAM)*

ANSI INCITS 452-2009, *Information technology - AT Attachment-8 ATA/ATAPI Command Set (ATA8-ACS)*

2.3 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

ISO/IEC 14776-415, *Information technology - SCSI Architecture Model - 5 (SAM-5).*

ISO/IEC 14776-454, *SCSI Primary Commands-4 (SPC-4)* (T10/1731-D)

ISO/IEC 14776-922, *SCSI/ATA Translation-3 (SAT-3)* (T10/2126-D)

ISO/IEC 14776-261, *SAS Protocol Layer-2 (SPL-2)* (T10/2228-D)

NOTE 5 - For more information on the current status of these documents, contact the INCITS Secretariat at 202-737-8888 (phone), 202-638-4922 (fax) or via Email at incits@itic.org. To obtain copies of these documents, contact Global Engineering at 15 Inverness Way, East Englewood, CO 80112-5704 at 303-792-2181 (phone), 800-854-7179 (phone), or 303-792-2192 (fax) or see http://www.incits.org.

ISO 80000-2, *Quantities and units -- Part 2: Mathematical signs and symbols to be used in the natural sciences and technology*.

2.4 Other references

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

Serial ATA Revision 3.1 (SATA). 18 July 2011

NOTE 6 - For more information on Serial ATA international Organization, see www.sata-io.org.

SFF-8086, *Compact Multilane Series: Common Elements*

SFF-8087, *Compact Multilane Series: Unshielded*

SFF-8088, *Compact Multilane Series: Shielded*

SFF-8147, *54mm x 71mm Form Factor w/micro SAS Connector*

SFF-8223, *2.5" Drive Form Factor with Serial Connector*

SFF-8323, *3.5" Drive Form Factor with Serial Connector*

SFF-8436, *QSFP+ Copper and Optical Modules*

SFF-8449, *Mini Multilane Series Management Interface*

SFF-8523, *5.25" Drive Form Factor with Serial Connector*

SFF-8410, *HSS Copper Testing and Performance Requirements*

SFF-8416, *Measurement and Performance Requirements for HPEI Bulk Cable*

SFF-8460, *HSS Backplane Design Guidelines*

SFF-8482, *Unshielded Dual Port Serial Attachment Connector*

SFF-8484, *Multi-Lane Unshielded Serial Attachment Connectors*

SFF-8485, *Serial GPIO (SGPIO) Bus*

SFF-8486, *Serial Attachment Micro Connector*

SFF-8630, *Serial Attachment 12 Gbs 4X Unshielded Connector (Style B)*

SFF-8639, *Multifunction 12 Gb/s 6X Unshielded Connector*

SFF-8643, *Mini Multilane Series: Unshielded HD Integrated Connector*

SFF-8644, *Mini Multilane Series: Shielded HD Integrated Connector*

SFF-8680, *Serial Attachment 12 Gbs 2x Unshielded Connector*

NOTE 7 - For more information on the current status of SFF documents, contact the SFF Committee at 408-867-6630 (phone), or 408-867-2115 (fax). To obtain copies of these documents, contact the SFF Committee at 14426 Black Walnut Court, Saratoga, CA 95070 at 408-867-6630 (phone) or 408-741-1600 (fax) or see http://www.sffcommittee.org.

ASTM Standard B 258-02, 2002, *Standard specification for standard nominal diameters and cross-sectional areas of AWG sizes of solid round wires used as electrical conductors*, ASTM International, West Conshohocken, PA, USA.

NOTE 8 - For more information on ASTM International standards, see www.astm.org.

PANTONE® Color Formula Guide

NOTE 9 - Pantone® and PANTONE MATCHING SYSTEM® are registered trademarks of Pantone, Inc. For more information on Pantone colors, contact Pantone, Inc. (see http://www.pantone.com).

Touchstone® File Format Specification. Revision 1.1. IBIS Open Forum.

NOTE 10 - Touchstone® is a registered trademark of Agilent Corporation. For more information on the Touchstone specification, contact the IBIS Open Forum (see http://www.eigroup.org).

MATLAB® 7 Programming Fundamentals. Release 2008b.

NOTE 11 - MATLAB® is a registered trademark of The MathWorks, Inc. For more information on MATLAB, contact The Mathworks, Inc. (see http://www.mathworks.com).

3 Definitions, symbols, abbreviations, keywords, and conventions

3.1 Definitions

3.1.1 active cable assembly: A cable assembly (see 3.1.9) that requires power for internal circuitry used in the transmission of the signal through the cable assembly.

3.1.2 AT Attachment (ATA): A standard for the internal attachment of storage devices to hosts. See ATA8-AAM.

3.1.3 baud rate: The nominal signaling speed, expressed as the maximum number of times per second that the signal (see 3.1.95) may change the state of the physical link (see 3.1.68). Each state change produces a transition (i.e., signal edge). The baud rate is the reciprocal of the UI (i.e., $f_{baud} = 1 / UI$) (see 3.1.114).

3.1.4 bit error ratio (BER): The number of logical bits output from a receiver circuit that differ from the correct transmitted logical bits, divided by the number of transmitted logical bits. The BER is computed on the raw bit stream before 10b8b decoding. The BER is usually expressed as a coefficient and a power of 10 (e.g., 2 erroneous bits out of 100 000 bits transmitted is expressed as 2 out of 10^5 or 2×10^{-5}). See MJSQ.

3.1.5 bit time: The nominal duration of a signal transmission bit (e.g., $666.\overline{6}$ ps at 1.5 Gbps, $333.\overline{3}$ ps at 3 Gbps, $166.\overline{6}$ ps at 6 Gbps, and $83.\overline{3}$ ps at 12Gbps).

3.1.6 bounded uncorrelated jitter (BUJ): The part of DJ (see 3.1.24) not aligned in time with the signal being measured. Specifically, BUJ excludes ISI (see 3.1.49) and duty cycle distortion. See MJSQ.

3.1.7 burst time: The part of an OOB signal (see 3.1.62) where the OOB burst (see 3.1.58) is transmitted. See 5.11.

3.1.8 byte: A sequence of eight contiguous bits considered as a unit.

3.1.9 cable assembly: Bulk cable with a separable connector at each end plus any retention, backshell, shielding features, or circuitry used for cable management or signal transmission. See 5.5.3.

3.1.10 clock data recovery (CDR): The function provided by the receiver circuit responsible for producing a regular clock signal (i.e., the recovered clock) from the received signal and for aligning the recovered clock to the symbols (i.e., bits) being transmitted with the signal. The CDR uses the recovered clock to recover the bits. See MJSQ.

3.1.11 common SSC transmit clock: An implementation that employs a single transmit clock for multiple transmitter devices and enables or disables SSC (see 5.9.6) on the transmit clock signal to all transmitter devices in common rather than allowing each transmitter device to independently control SSC.

3.1.12 compliance point: An interoperability point where interoperability specifications are met. See 5.3.

3.1.13 compliant jitter tolerance pattern (CJTPAT): A test pattern for jitter testing. See 5.9.3.5 and Annex A.

3.1.14 connector: Electro-mechanical components consisting of a receptacle and a plug that provide a separable interface between two transmission segments. See 5.5.3.

3.1.15 consecutive identical digits (CID): A serial bit stream with repeated data bits of the same binary value.

3.1.16 cumulative distribution function (CDF): The probability that jitter (see 3.1.50) is less than a given value. See MJSQ.

3.1.17 D.C. idle: A differential signal level that is nominally 0 V(P-P), used during the idle time (see 3.1.47) and negation time (see 3.1.57) of an OOB signal (see 3.1.62) when D.C. mode (see 3.1.18) is enabled. See 5.9.4.

3.1.18 D.C. mode: A mode in which D.C. idle (see 3.1.17) is used during the idle time (see 3.1.47) and negation time (see 3.1.57) of an OOB signal (see 3.1.62).

3.1.19 data dependent jitter (DDJ): Jitter (see 3.1.50) that is added when the transmission pattern is changed from a clock-like to a non-clock-like pattern. See MJSQ.

3.1.20 decibel (dB): Ten times the common logarithm (i.e., $\log_{10}$) of the ratio of relative powers.

NOTE 12 - The ratio of powers P_1 and P_2 in dB is $10 \times \log_{10} (P_1 / P_2)$. If $P_1 = V_1^2 / R_1$, $P_2 = V_2^2 / R_2$, and $R_1=R_2$, then this ratio is equivalent to 20 times the common logarithm of the relative voltage ratio (i.e., $dB = 20 \times \log_{10} (V_1 / V_2)$). A ratio of 1 results in a dB value of 0 (e.g., $20 \times \log_{10} (1) = 0$ dB), a ratio greater than 1 results in a positive dB value (e.g., $20 \times \log_{10} (2) = 6$ dB) and a ratio less than 1 results in a negative dB value (e.g., $20 \times \log_{10} (0.5) = -6$ dB).

3.1.21 dB millivolts (dBmV): The decibel ratio of an rms voltage value relative to 1 mV.

NOTE 13 - 20 mV(rms) is equal to $20 \times \log_{10}(20 \text{ mV} / 1 \text{ mV}) = 26$ dBmV. This does not depend on the impedance level.

3.1.22 dB milliwatts (dBm): The decibel ratio of a power value relative to 1 mW.

NOTE 14 - 20 mW is equal to $10 \times \log_{10}(20 \text{ mW} / 1 \text{ mW}) = 13$ dBm. If power is measured with a 50 ohm impedance level, then 20 mW is equivalent to $(0.02 \text{ W} \times 50 \text{ ohm})^{(1/2)} = 1$ V or 60 dBmV. If power is measured with a 25 ohm impedance level (i.e., the reference impedance for common mode measurements), then 20 mW is equivalent to $(0.02 \text{ W} \times 25 \text{ ohm})^{(1/2)} = 0.707$ V or 57 dBmV.

3.1.23 decision feedback equalizer (DFE): A nonlinear equalizer that uses a feedback loop based on previously decoded symbols.

3.1.24 deterministic jitter (DJ): Jitter (see 3.1.50) with non-Gaussian distribution that is bounded in amplitude and has specific causes. See MJSQ.

3.1.25 direct current (D.C.): The non-A.C. component of a signal. In this standard, all frequency components below 100 kHz.

3.1.26 disparity: The difference between the number of ones and zeros in a character. See SPL-2.

3.1.27 dispersion: Signal pulse broadening and distortion from all causes.

3.1.28 duty cycle distortion (DCD): One-half of the difference of the average width of a one and the average width of a zero in a signal waveform eye pattern measurement. See MJSQ.

3.1.29 dword: A sequence of four contiguous bytes or four contiguous characters considered as a unit. See SPL-2.

3.1.30 electromagnetic interference (EMI): Any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment.

3.1.31 enclosure: The box, rack, or set of boxes providing the powering, cooling, mechanical protection, EMI protection, and external electronic interfaces for one or more end device(s) (see 3.1.35) and/or expander device(s) (see SPL-2). The enclosure provides the outermost electromagnetic boundary and acts as an EMI barrier.

3.1.32 enclosure in port: A set of expander phys with subtractive routing attributes using the same external connector (see 5.5.3.4). See SPL-2.

3.1.33 enclosure out port: A set of expander phys with table routing attributes in an expander device that does not support table-to-table attachment using the same external connector (see 5.5.3.4). See SPL-2.

3.1.34 enclosure universal port: A set of expander phys with table routing attributes in an expander device that supports table-to-table attachment using the same external connector (see 5.5.3.4). See SPL-2.

3.1.35 end device: A SAS device or SATA device that is not contained within an expander device (see 3.1.38). See SPL-2.

3.1.36 end-to-end simulation: A simulation performed from a reference transmitter or from a captured signal to the output of a reference receiver.

3.1.37 etch: Printed circuit board copper conductor path.

3.1.38 expander device: A device that is part of a service delivery subsystem (see SAM-5), facilitates communication between SAS devices (see 3.1.88) and SATA devices (see 3.1.91). See SPL-2.

3.1.39 expander phy: A phy in an expander device that interfaces to a service delivery subsystem (see SAM-5).

3.1.40 expander port: An expander device object that interfaces to a service delivery subsystem (see SAM-5) and to SAS ports in other devices. See SPL-2.

3.1.41 external connector: A bulkhead connector (see 3.1.14) that carries signals into and out of an enclosure (see 3.1.31) and exits the enclosure with only minor compromise to the shield effectiveness of the enclosure (e.g., a Mini SAS 4x receptacle or Mini SAS HD receptacle). See 5.5.3.4.

3.1.42 eye contour: The locus of points in a signal level versus time eye diagram where the CDF of 10^{-12} in the actual signal population exists. Comparison of the measured eye contour to the jitter eye mask determines whether a jitter eye mask violation has occurred. See 5.9.3 and MJSQ.

3.1.43 fall time: The time interval for the falling signal edge to transit between specified percentages of the signal amplitude. In this standard, the measurement points are the 80 % and 20 % voltage levels. Also see rise time (see 3.1.87).

3.1.44 fanout cable assembly: A cable assembly with one connector on one end and multiple connectors on the other end. See 5.5.4.1.3.

3.1.45 field: A group of one or more contiguous bits.

3.1.46 golden phase lock loop (golden PLL): A function that conforms to the jitter timing reference frequency response requirements in MJSQ that extracts the jitter timing reference from the data stream under test to be used as the timing reference for the instrument used for measuring the jitter in the signal under test. See MJSQ.

3.1.47 idle time: The part of an OOB signal (see 3.1.62) where OOB idle (see 3.1.17) is being transmitted. See 5.11.

3.1.48 insertion loss: The ratio, usually expressed in dB, of incident power to delivered power. The dB magnitude of S_{12} or S_{21} is the negative of insertion loss in dB. See E.11.

3.1.49 intersymbol interference (ISI): Reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses. Neighboring pulses are pulses that are close enough to have significant energy overlapping the affected pulse and does not imply or exclude adjacent pulses (i.e., many bit times (see 3.1.5)

may separate the pulses, especially in the case of reflections). ISI may result in DDJ and vertical eye closure. Several mechanisms produce ISI (e.g., dispersion, reflections, and circuits that lead to baseline wander). See MJSQ.

3.1.50 jitter: The collection of instantaneous deviations of signal edge times at a defined signal level of the signal from the reference times (e.g., as defined by the jitter timing reference) for those events. See MJSQ.

3.1.51 jitter timing reference: The signal used as the basis for calculating the jitter in the signal under test. See MJSQ.

3.1.52 jitter tolerance: The ability of the receiver device to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal applied to the receiver device compliance point. See MJSQ.

3.1.53 jitter tolerance pattern (JTPAT): A test pattern for jitter testing. See 5.9.3.5 and Annex A.

3.1.54 least mean square (LMS): An algorithm for adaptively adjusting the tap coefficients of a DFE (see 3.1.23) based on the difference between the desired and actual signal.

3.1.55 managed connector category: The category of connectors that support a cable management interface. See 5.5.3.2.

3.1.56 near-end crosstalk (NEXT): Crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the disturbing channel. The terminals of the disturbed channel, at which the near-end crosstalk is present, and the energized terminals of the disturbing channel are usually near each other.

3.1.57 negation time: The part of an OOB signal (see 3.1.62) during which OOB idle (see 3.1.59) is transmitted after the last OOB burst (see 3.1.58). See 5.11.

3.1.58 OOB burst: The transmission of signal transitions or ALIGN3 primitives for a burst time (see 3.1.7). See 5.11.1.

3.1.59 OOB idle: The transmission of D.C. idle (see 3.1.17) when D.C. mode (see 3.1.18) is enabled, or a defined sequence of dwords when optical mode (see 3.1.63) is enabled.

3.1.60 OOB interval: The time basis for burst times (see 3.1.7), idle times (see 3.1.47), negation times (see 3.1.57), and signal times (see 3.1.98) used to create OOB signals (see 3.1.62). See 5.11.1.

3.1.61 OOB sequence: A sequence where two phys exchange OOB signals (see 3.1.62). See SPL-2.

3.1.62 OOB signal: A pattern of idle time (see 3.1.47), burst time (see 3.1.7), and negation time (see 3.1.57) used during the link reset sequence. See 5.11.

3.1.63 optical mode: A mode in which a defined sequence of dwords is used during the idle time (see 3.1.47) and negation time (see 3.1.57) of an OOB signal (see 3.1.62). See 5.11.

3.1.64 passive cable assembly: A cable assembly (see 3.1.9) that does not require external power for internal circuitry used in the transmission of the signal through the cable assembly.

3.1.65 passive TxRx connection: The complete simplex signal path between the transmitter circuit (see 3.1.107) and receiver circuit (see 3.1.74) that does not include powered circuitry used in the transmission of the signal through the TxRx connection (see 3.1.112). See 5.6.1.

3.1.66 phy: A object in a device that is used to interface to other devices (e.g., an expander phy (see 3.1.39) or a SAS phy (see 3.1.89)). See 4.1.

3.1.67 physical interconnect TxRx connection segment (PICS): A TxRx connection segment (see 3.1.113) used to model channel loss between the TDCS (see 3.1.111) and the RDCS.(see 3.1.78) See 5.4.

3.1.68 physical link: Two differential signal pairs, one pair in each direction, that connect two physical phys (see 3.1.70). See 4.1.

3.1.69 physical link rate: A link rate between two physical phys established as a result of speed negotiation between those phys.

3.1.70 power on: Power being applied.

3.1.71 probe point: Physical position in a test load where signal characteristics for compliance points are measured See 5.7.

3.1.72 random jitter (RJ): Jitter (see 3.1.50) that is characterized by a Gaussian distribution and is unbounded. See MJSQ.

3.1.73 rate: Data transfer rate of a physical or logical link (e.g., 1.5 Gbps, 3 Gbps, or 6 Gbps).

3.1.74 receiver circuit: An electronic circuit that converts an analog serial input signal to a logic signal.

3.1.75 receiver circuit TxRx connection segment (RCCS): A TxRx connection segment (see 3.1.113) used to model package loss within the simulated receiver circuit (see 3.1.74).

3.1.76 reference clock: The clock generated by the PLL. This clock is filtered by the JTF (see 5.9.3.2) and aligned with the zero-crossing instants.

3.1.77 receiver device (Rx): The device downstream from a receiver device compliance point (see 3.1.12) containing a portion of the physical link and a receiver circuit (see 3.1.74).

3.1.78 receiver device TxRx connection segment (RDCS): The TxRx connection segment (see 3.1.113) between the simulated receiver circuit (see 3.1.74) and a separable connector.

3.1.79 reference pulse response cursor (peak-to-peak): The cursor that is twice the amplitude of the response to a one-UI-wide positive pulse of the same amplitude and transmitter equalization as the data stream it represents (see 5.8.3), sampled at the reference sampling instant (see 3.1.82).

3.1.80 reference receiver device: A set of parameters defining electrical performance characteristics that provide a set of minimum electrical performance requirements for a receiver device and that are also used in mathematical modeling to determine compliance of a TxRx connection or transmitter device. See 5.9.5.7.3.

3.1.81 reference sampling clock: The reference clock (see 3.1.76) shifted by 0.5 UI (see 3.1.114).

3.1.82 reference sampling instant: The instant at which a reference sampling clock (see 3.1.81) samples the maximum amplitude of the response to a positive pulse generated using the reference sampling clock (see figure 113).

3.1.83 reference transmitter device: A set of parameters defining electrical performance characteristics of a transmitter device that are used in mathematical modeling to determine compliance of a TxRx connection. See 5.9.4.6.5 and 5.9.4.7.3.

3.1.84 reference transmitter test load: A set of S-parameters defining the electrical characteristics of a TxRx connection used as the basis for transmitter device and receiver device performance evaluation through mathematical modeling. See 5.7.5.

3.1.85 reflection coefficient (ρ): The ratio of reflected voltage to incident voltage.

3.1.86 return loss: The ratio, usually expressed in dB, of incident power to reflected power. The dB magnitude of S_{11} or S_{22} is the negative of return loss in dB. See E.11.

3.1.87 rise time: The time interval for the rising signal edge to transit between specified percentages of the signal amplitude. In this standard, the measurement points are the 20 % and 80 % voltage levels. Also see fall time (see 3.1.43).

3.1.88 SAS device: A SAS initiator device (see SPL-2) and/or a SAS target device (see SPL-2).

3.1.89 SAS phy: A phy in a SAS device (see 3.1.88) that interfaces to a service delivery subsystem (see SAM-5).

3.1.90 SAS target device: A device containing SSP, STP, and/or SMP target ports in a SAS domain. See SPL-2.

3.1.91 SATA device: An ATA device (see ATA8-AAM) that contains a SATA device port in an ATA domain. See SPL-2.

3.1.92 SATA phy: A phy in a SATA device (see SPL-2) or SATA port selector (see SPL-2) that interfaces to a service delivery subsystem (see SAM-5). Analogous to a SAS phy (see 3.1.89).

3.1.93 Serial ATA (SATA): The protocol defined by SATA (see 2.4).

3.1.94 Serial Attached SCSI (SAS): The set of protocols defined in SPL-2 and the interconnect defined by this standard.

3.1.95 signal: Detectable transmitted energy that is used to carry information.

3.1.96 signal amplitude: A property of the overall signal (see 3.1.95) that describes the peak or peak-to-peak values of the signal level (see 3.1.97).

3.1.97 signal level: The instantaneous intensity of a signal (see 3.1.95) measured in volts.

3.1.98 signal time: The time of an OOB signal (see 3.1.62), consisting of six burst times (see 3.1.7), six idle times (see 3.1.47), and one negation time (see 3.1.57). See 5.11.

3.1.99 signal tolerance: The ability of the receiver device to recover transmitted bits in an incoming data stream with maximum jitter and minimum amplitude. See MJSQ.

3.1.100 significant crosstalk: Any crosstalk source having a magnitude point of its transfer function in excess of -46 dB in the range of frequencies up to 6 GHz.

3.1.101 sinusoidal jitter (SJ): Single frequency jitter (see 3.1.50) applied during signal tolerance testing. See MJSQ.

3.1.102 spread spectrum clocking (SSC): The technique of modulating the operating frequency of a transmitted signal (i.e., the physical link rate) to reduce the measured peak amplitude of radiated emissions. See SPL-2.

3.1.103 symbol: The smallest unit of data transmission on a physical link (i.e., a bit). A symbol represents a single transition if the maximum transition rate (i.e., a 0101b pattern) is occurring.

3.1.104 total jitter (TJ): Jitter (see 3.1.50) from all sources. See MJSQ.

3.1.105 trained: A physical link rate negotiated with Train-SNW. See SPL-2.

3.1.106 transceiver: A physical entity that contains both a transmitter device (see 3.1.110) and a receiver device (see 3.1.77).

3.1.107 transmitter circuit: An electronic circuit that converts a logic signal to an analog serial output signal.

3.1.108 transmitter circuit TxRx connection segment (TCCS): A TxRx connection segment (see 3.1.113) used to model package loss within the simulated transmitter circuit (see 3.1.107).

3.1.109 transmitter compliance transfer function (TCTF): The mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask. See 5.9.4.1.

3.1.110 transmitter device (Tx): The device upstream from a transmitter device compliance point (see 3.1.12) containing a portion of the physical link and a transmitter circuit (see 3.1.107).

3.1.111 transmitter device TxRx connection segment (TDCS): The TxRx connection segment (see 3.1.113) between the transmitter circuit (see 3.1.107) and a separable connector.

3.1.112 TxRx connection: The complete simplex signal path between the transmitter circuit (see 3.1.107) and receiver circuit (see 3.1.74). See 5.6.1.

3.1.113 TxRx connection segment: That portion of a TxRx connection (see 3.1.112) delimited by separable connectors or changes in the conductive material. See 5.6.1.

3.1.114 unit interval (UI): The normalized, dimensionless, nominal duration of a symbol (see 3.1.103) (e.g., 666.$\overline{6}$ ps at 1.5 Gbps, 333.$\overline{3}$ ps at 3 Gbps, 166.$\overline{6}$ ps at 6 Gbps, and 83.$\overline{3}$ ps at 12 Gbps). The UI is the reciprocal of the baud rate (i.e., UI = 1 / f_{baud}) (see 3.1.3).

3.1.115 unmanaged active connector category: The category of connectors that support power for Mini SAS 4x active external cable assemblies (see 5.5.4.2.2) but do not support cable assemblies with a cable management interface. See 5.5.3.2.

3.1.116 unmanaged passive connector category: The category of connectors that do not support power for Mini SAS 4x active external cable assemblies (see 5.5.4.2.2) and do not support cable assemblies with a cable management interface. See 5.5.3.2.

3.1.117 untrained: A physical link rate not negotiated with Train-SNW. See SPL-2.

3.1.118 usage variable: A SASWDP parameter set to a value that determines if the stressor file is to be added to the simulation. See Annex B.

3.1.119 voltage modulation amplitude (VMA): The difference in electrical voltage of a signal (see 3.1.95) between the stable one level and the stable zero level.

3.1.120 waveform dispersion penalty (WDP): A simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device. See 5.9.4.6.1 and Annex B.

3.2 Symbols and abbreviations

See 2.1 for abbreviations of standards bodies (e.g., ISO). Units and abbreviations used in this standard:

Abbreviation	Meaning
A.C.	alternating current
ATA	AT attachment (see 3.1.1)

Abbreviation	Meaning
ATAPI	AT attachment packet interface
ATA8-AAM	AT Attachment - 8 ATA/ATAPI Architecture Model standard (see 2.3)
ATA8-ACS	AT Attachment - 8 ATA/ATAPI Command Set standard (see 2.3)
AWG	American wire gauge (see ASTM Standard B 258-02 (see 2.4))
BER	bit error ratio (see 3.1.4)
BUJ	bounded uncorrelated jitter (see 3.1.6)
CDF	cumulative distribution function (see 3.1.16)
CDR	clock data recovery (see 3.1.10)
CIC	compliance interconnect channel (see SATA)
CID	consecutive identical digits (see 3.1.15)
CJTPAT	compliant jitter tolerance pattern (see 3.1.13)
CR	inter-enclosure (i.e., cabinet) receiver device compliance point (see 5.3)
CT	inter-enclosure (i.e., cabinet) transmitter device compliance point (see 5.3)
dB	decibel (see 3.1.20)
dBm	decibel milliwatts (see 3.1.22)
dBmV	decibel millivolts (see 3.1.21)
D.C.	direct current (see 3.1.25)
DCD	duty cycle distortion (see 3.1.28)
DDJ	data dependent jitter (see 3.1.19)
DFE	decision feedback equalizer (see 3.1.23)
DJ	deterministic jitter (see 3.1.24)
Dxx.y	data character (see 3.1.19)
e	2.718 28..., the base of the natural (i.e., hyperbolic) system of logarithms
EMI	electromagnetic interference (see 3.1.30)
ESD	electrostatic discharge
G1	generation 1 physical link rate (i.e., 1.5 Gbps)
G2	generation 2 physical link rate (i.e., 3 Gbps)
G3	generation 3 physical link rate (i.e., 6 Gbps)
G4	generation 4 physical link rate (i.e., 12 Gbps)
Gbps	gigabits per second (i.e., 10^9 bits per second)
Gen1i	SATA generation 1 physical link rate (i.e., 1.5 Gbps) (see SATA)
Gen2i	SATA generation 2 physical link rate (i.e., 3 Gbps) (see SATA)
Gen3i	SATA generation 3 physical link rate (i.e., 6 Gbps) (see SATA)
GHz	gigahertz (i.e., 10^9 cycles per second)(i.e., s^{-9})
GPIO	general purpose input/output
HD	high-density
Hz	hertz (i.e., cycles per second)(i.e., s^{-1})
IR	intra-enclosure (i.e., internal) receiver device compliance point (see 5.3)
ISI	intersymbol interference (see 3.1.49)
IT	intra-enclosure (i.e., internal) transmitter device compliance point (see 5.3)
JMD	jitter measurement device

Abbreviation	Meaning
JTF	jitter transfer function (see 5.9.3.2)
JTPAT	jitter tolerance pattern (see 3.1.53)
kHz	kilohertz (i.e., 10^3 cycles per second)(i.e., s^{-3})
LED	light-emitting diode
LMS	least mean square (see 3.1.54)
µA	microampere (i.e., 10^{-6} amperes)
µs	microsecond (i.e., 10^{-6} seconds)
m	meter
mA	milliampere (i.e., 10^{-3} amperes)
MBps	megabytes per second (i.e., 10^6 bytes per second)
MHz	megahertz (i.e., 10^6 cycles per second)(i.e., s^{-6})
ms	millisecond (i.e., 10^{-3} seconds)
mV	millivolt (i.e., 10^{-3} volts)
mW	milliwatt (i.e., 10^{-3} watts)
N/A	not applicable
NEXT	near-end crosstalk (see 3.1.56)
nF	nanofarad (i.e., 10^{-9} farads)
ns	nanosecond (i.e., 10^{-9} seconds)
OOB	out-of-band
OOBI	out-of-band interval (see 3.1.60)
PCB	printed circuit board
PJ	periodic jitter
PLL	phase lock loop
P-P	peak-to-peak
ppm	parts per million (i.e., 10^{-6})
ps	picosecond (i.e., 10^{-12} seconds)
RCCS	receiver circuit TxRx connection segment (see 3.1.75)
RD	running disparity (see SPL-2)
RDCS	receiver device TxRx connection segment (see 3.1.78)
RJ	random jitter (see 3.1.72)
rms	root mean square (i.e., quadratic mean)
Rx	receiver device (see 3.1.77)
RTTL	reference transmitter test load (see 3.1.84)
SAM-5	SCSI Architecture Model - 5 standard (see 2.3)
SAS	Serial Attached SCSI (see 3.1.94)
SATA	Serial ATA (see 3.1.93) or the Serial ATA 3.1 specification (see 2.4)
SCSI	Small Computer System Interface
S_{ij}	S-parameter for port j to port i (see E.11)
S_{CCij}	S-parameter for common-mode to common-mode port j to port i (see E.11)
S_{CDij}	S-parameter for differential to common-mode port j to port i (see E.11)
S_{DCij}	S-parameter for common-mode to differential port j to port i (see E.11)

Abbreviation	Meaning
S_{DDij}	S-parameter for differential to differential port j to port i (see E.11)
SGPIO	serial GPIO (see 2.4)
SJ	sinusoidal jitter (see 3.1.101)
SMA	subminiature version A connector (see 2.2)
SPC-4	SCSI Primary Commands - 4 standard (see 2.3)
SPL-2	SAS Protocol Layer - 2(see 2.3)
SSC	spread spectrum clocking
STP	Serial ATA Tunneled Protocol
s	second (unit of time)
sgn	signum function (i.e., sign function)
TCCS	transmitter circuit TxRx connection segment (see 3.1.108)
TCTF	transmitter compliance transfer function (see 3.1.109)
TDCS	transmitter device TxRx connection segment (see 3.1.111)
TDNA	time domain network analyzer (i.e., TDR/TDT plus analysis software that performs a VNA-style output)
TDR	time domain reflectometer
TDT	time domain transmission
TJ	total jitter (see 3.1.104)
Tx	transmitter device (see 3.1.110)
UI	unit interval (see 3.1.114)
V	volt
VMA	voltage modulation amplitude (see 3.1.119)
VNA	vector network analyzer
W	watt
WDP	waveform dispersion penalty (see 3.1.120)
Δ (Delta)	difference operator
ϕ (phi)	phase
π (pi)	3.141 59... , the ratio of the circumference of a circle to its diameter
ρ (rho)	reflection coefficient (see 3.1.85)
τ (tau)	time constant
^	exclusive logical OR
<	less than
$\leq$	less than or equal to
>	greater than
$\geq$	greater than or equal to
$\pm$	plus or minus
$\times$	multiplication
/	division
|v|	the absolute value (i.e., magnitude) of v
~	approximately equal to
®	registered trademark
$\otimes$	convolution

3.3 Keywords

3.3.1 invalid: A keyword used to describe an illegal or unsupported bit, byte, word, field or code value. Receipt of an invalid bit, byte, word, field or code value shall be reported as an error.

3.3.2 mandatory: A keyword indicating an item that is required to be implemented as defined in this standard.

3.3.3 may: A keyword that indicates flexibility of choice with no implied preference (equivalent to “may or may not”).

3.3.4 may not: Keywords that indicate flexibility of choice with no implied preference (equivalent to “may or may not”).

3.3.5 obsolete: A keyword indicating that an item was defined in prior standards but has been removed from this standard.

3.3.6 optional: A keyword that describes features that are not required to be implemented by this standard. However, if any optional feature defined in this standard is implemented, then it shall be implemented as defined in this standard.

3.3.7 reserved: A keyword referring to bits, bytes, words, fields and code values that are set aside for future standardization. A reserved bit, byte, word or field shall be set to zero, or in accordance with a future extension to this standard. Recipients are not required to check reserved bits, bytes, words or fields for zero values. Receipt of reserved code values in defined fields shall be reported as an error.

3.3.8 restricted: A keyword referring to bits, bytes, words, and fields that are set aside for other identified standardization purposes. A restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears.

3.3.9 shall: A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.3.10 should: A keyword indicating flexibility of choice with a strongly preferred alternative (equivalent to “is strongly recommended”).

3.3.11 vendor specific: Something (e.g., a bit, field, or code value) that is not defined by this standard and may be used differently in various implementations.

3.4 Editorial conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

Names of signals are in all uppercase (e.g., GROUND).

Normal case is used for words having the normal English meaning.

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included between characters in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b or 0_0101_1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Underscores or spaces may be included between characters in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

This standard uses the following conventions for representing decimal numbers:

a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
b) the thousands separator (i.e., separating groups of three digits in a portion of the number) is a space; and
c) the thousands separator is used in both the integer portion and the fraction portion of a number.

Table 2 shows some examples of decimal numbers using various numbering conventions.

Table 2 — Numbering conventions

French	English	This standard
0,6	0.6	0.6
3,141 592 65	3.14159265	3.141 592 65
1 000	1,000	1 000
1 323 462,95	1,323,462.95	1 323 462.95

A decimal number represented in this standard with an overline over one or more digits following the decimal point is a number where the overlined digits are infinitely repeating (e.g., 666.$\overline{6}$ means 666.666 666... or 666 2/3, and 12.$\overline{142\ 857}$ means 12.142 857 142 857... or 12 1/7).

Lists sequenced by letters (e.g., a) red, b) blue, c) green) show no ordering relationship between the listed items. Lists sequenced by numbers (e.g., 1) red, 2) blue, 3) green) show an ordering relationship between the listed items.

In the event of conflicting information the precedence for requirements defined in this standard is:

1) text;
2) tables; and
3) figures.

Notes do not constitute any requirements for implementers.

4 General

4.1 Physical links and phys

A physical link is a set of four wires used as two differential signal pairs. One differential signal transmits in one direction while the other differential signal transmits in the opposite direction. Data may be transmitted in both directions simultaneously.

A physical phy contains a transceiver which electrically interfaces to a physical link, which attaches to another physical phy.

Phys are contained in ports (see SPL-2). Phys interface to a service delivery subsystem (see SAM-5).

Figure 3 shows two phys attached with a physical link.

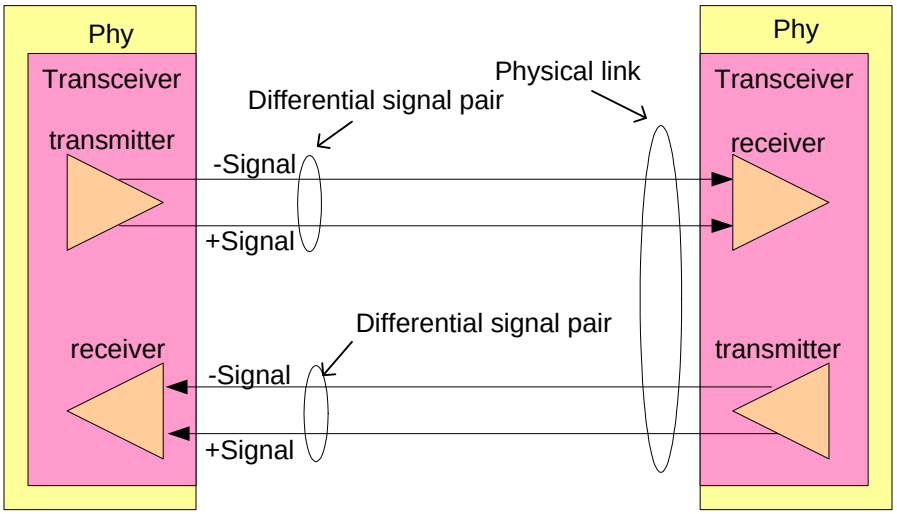

Figure 3 — Physical links and phys

An attached phy is the phy to which a phy is attached over a physical link.

The transceiver follows the electrical specifications defined in 5.9. Phys transmit and receive bits at physical link rates defined in 5.9. The bits are parts of 10-bit characters (see SPL-2), which are parts of dwords (see SPL-2). The physical link rates supported by a phy are specified or indicated by the following fields in the SMP DISCOVER response (see SPL-2), the SMP PHY CONTROL request (see SPL-2), and the Phy Control and Discover mode page (see SPL-2):

a) the NEGOTIATED PHYSICAL LINK RATE field;
b) the HARDWARE MINIMUM PHYSICAL LINK RATE field;
c) the HARDWARE MAXIMUM PHYSICAL LINK RATE field;
d) the PROGRAMMED MINIMUM PHYSICAL LINK RATE field; and
e) the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field.

4.2 Phy test functions

Phy test functions (e.g., transmission of test patterns) are used for phy and interconnect characterization and diagnosis. The phy may be attached to test equipment while performing a phy test function. See SPL-2 for the optional mechanisms for invoking phy test function.

Each phy test function is optional.

If the phy test function requires a specific phy test pattern and/or phy test function physical link rate, then the mechanism for invoking the phy test function (see SPL-2) also specifies the phy test pattern and phy test function physical link rate.

5 Physical layer

5.1 Physical layer overview

The physical layer defines:

a) passive interconnect (e.g., connectors and cable assemblies); and
b) transmitter and receiver device electrical characteristics.

Within this standard, references to connector gender use the terms plug and receptacle as equivalent to the terms free and fixed, respectively, that may be used in the references that define the connectors. Fixed and free terminology has no relationship to the application of the connector.

5.2 Conventions for defining maximum limits for S-parameters

The following values are specified by this standard to define the maximum limits for certain S-parameters (e.g., for cable assemblies and backplanes (see 5.6.3), transmitter devices (see 5.9.4.6.3), and receiver devices (see 5.9.5.7.2)):

a) L is the maximum value in dB at the low frequency asymptote;
b) N is the maximum value in dB at the Nyquist frequency (i.e., f_{max} / 2)(e.g., 3 GHz for 6 Gbps);
c) H is the maximum value in dB at the high frequency asymptote;
d) S is the slope in dB/decade;
e) f_{min} is the minimum frequency of interest; and
f) f_{max} is the maximum frequency of interest.

The frequencies at which L and H intersect the slope S may or may not be within the region of f_{min} to f_{max}.

Figure 4 shows the values in a graph.

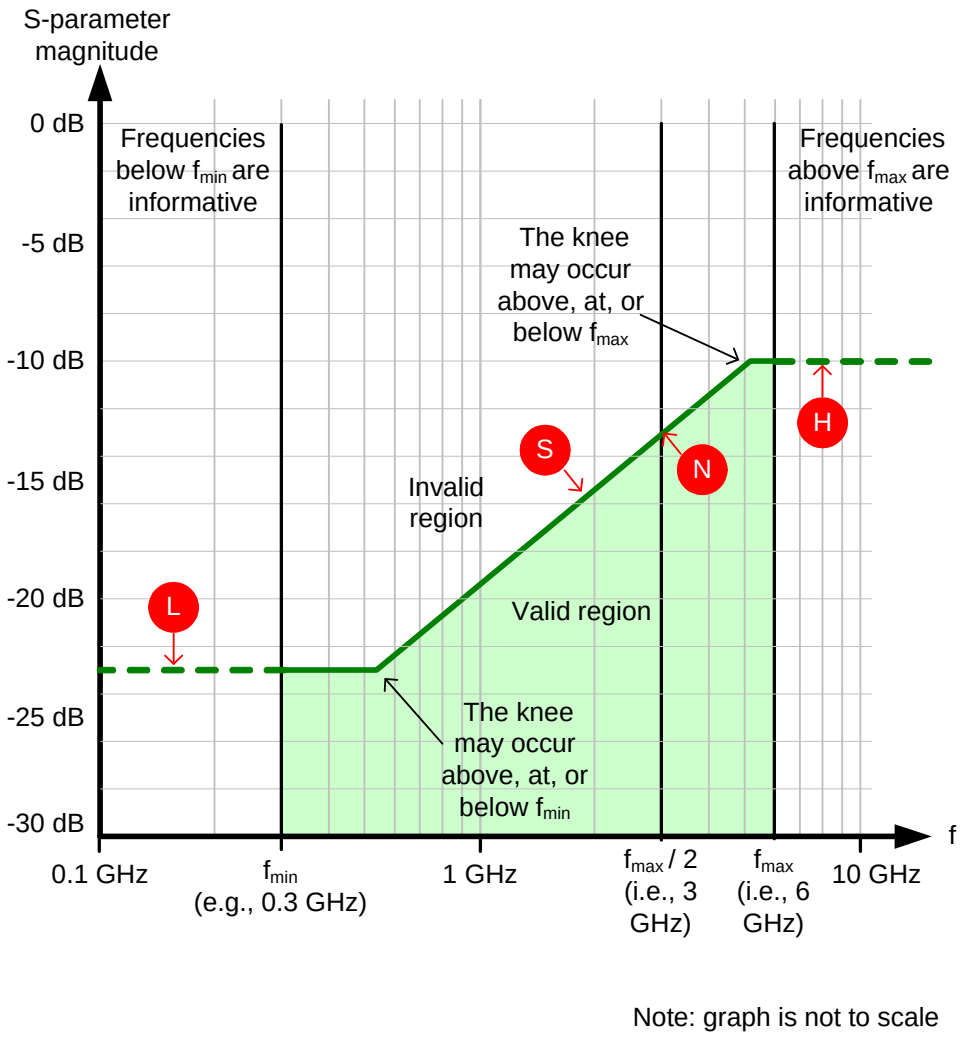

Figure 4 — Maximum limits for S-parameters definitions

5.3 1.5 Gbps, 3 Gbps, and 6 Gbps compliance points

A TxRx connection is the complete simplex signal path between the transmitter circuit (see 3.1.107) and receiver circuit (see 3.1.74).

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in conductive material.

This standard defines the electrical requirements of the signal at the compliance points IT, IR, CT, and CR in a TxRx connection (see table 3). Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this standard only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point.

Signal characteristics for compliance points are measured at physical positions called probe points in a test load (see 5.7). Measurements at the probe points in a test load approximate measurements at the compliance

point in the actual TxRx connection. Some components in the test load may be de-embedded as described in E.5.

Table 3 — 1.5 Gbps, 3 Gbps, and 6 Gbps compliance points

Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device (see 3.1.110), as measured at probe points in a test load attached with an internal connector.
IT_S [a]	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device (see 3.1.77), as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT_S [a]	inter-enclosure (i.e., cabinet)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.

[a] Because the trained 1.5 Gbps, 3 Gbps, and 6 Gbps transmitter device S-parameter specifications do not include the mated connector, transmitter device S-parameter measurement points are at the IT_S compliance point and CT_S compliance point. 1.5 Gbps, 3 Gbps, and 6 Gbps receiver device S-parameter measurement points are at the IR compliance point and CR compliance point.

The TxRx connection includes the characteristics of the mated connectors at both the transmitter device and receiver device ends. One end of a TxRx connection is a IT_S compliance point or CT_S compliance point, and the other end of the TxRx connection is the corresponding IR compliance point or CR compliance point.

Figure 5 shows the locations of the CT compliance points and CR compliance points using an external cable assembly, and shows how two of the compliance points are tested using test loads (see 5.7).

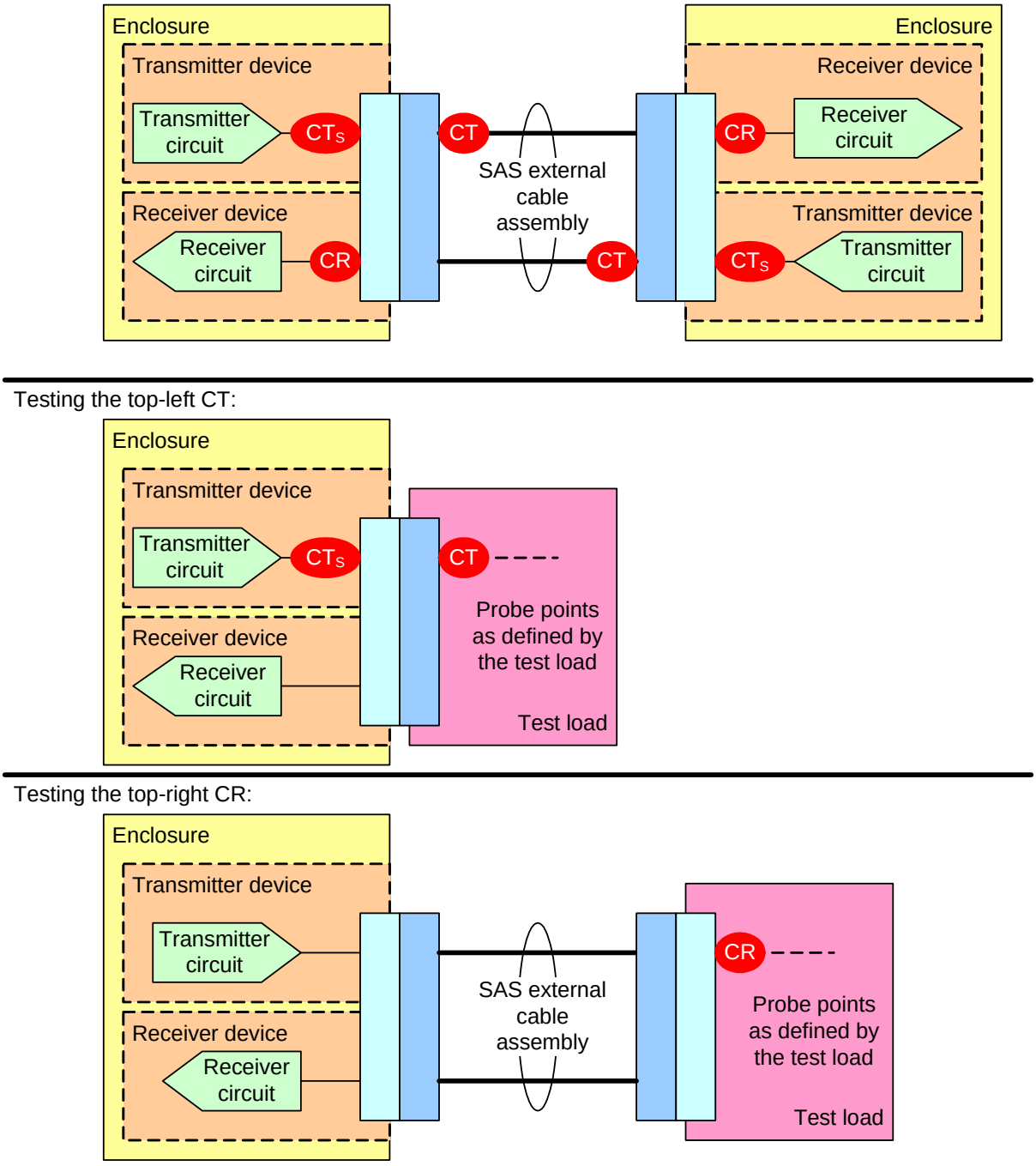

Figure 5 — External cable assembly CT compliance points and CR compliance points

Figure 6 shows the locations of the IT compliance points and IR compliance points using a backplane with a SAS Drive backplane receptacle (see 5.5.3.3.1.3) that is not using SATA, and shows how the compliance points are tested using test loads (see 5.7).

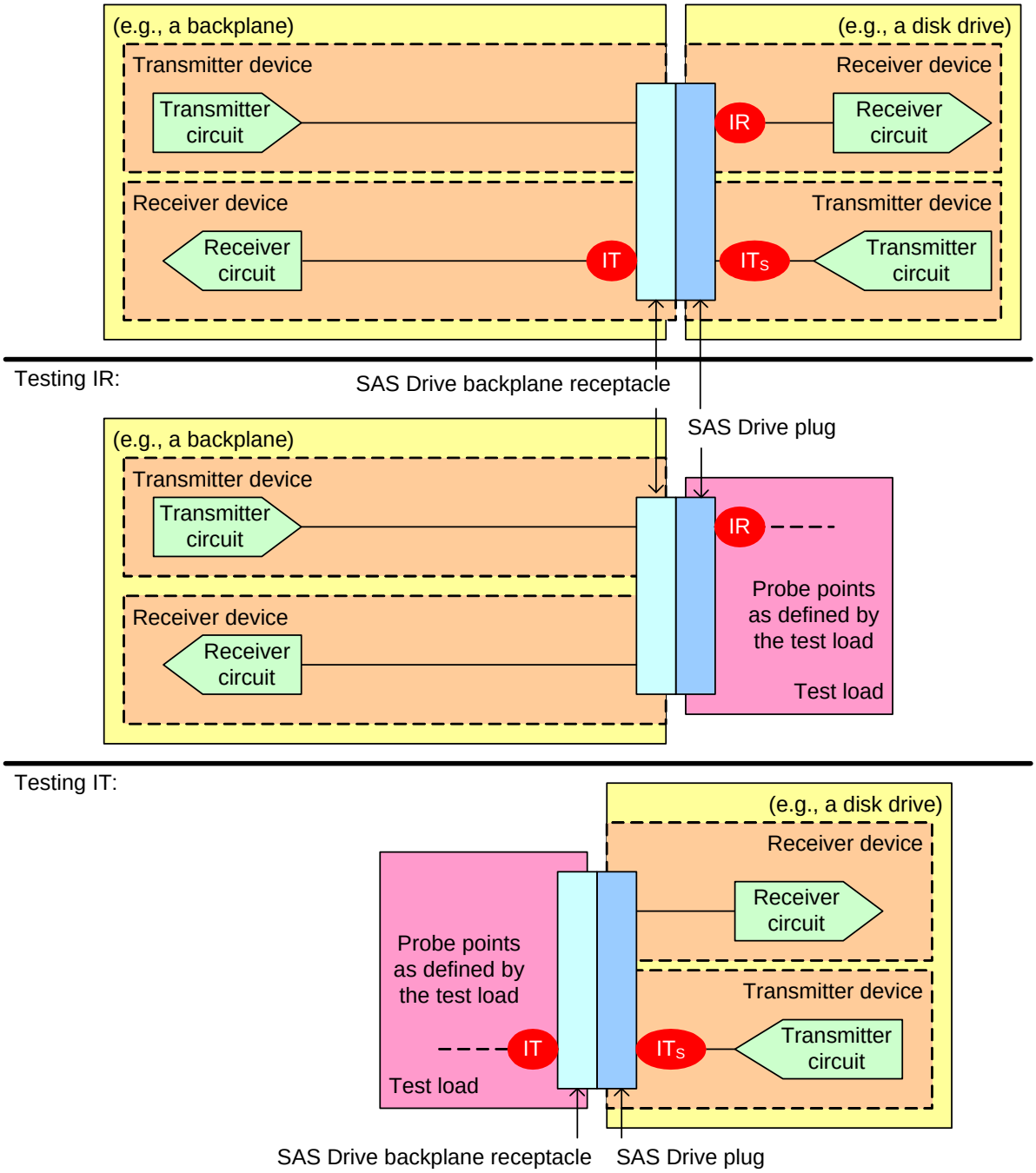

Figure 6 — Backplane with SAS Drive connector IT compliance points and IR compliance points

If the backplane supports SATA, then there are no IT compliance points or IR compliance points. SATA defines the signal characteristics that the SATA phy delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 7.

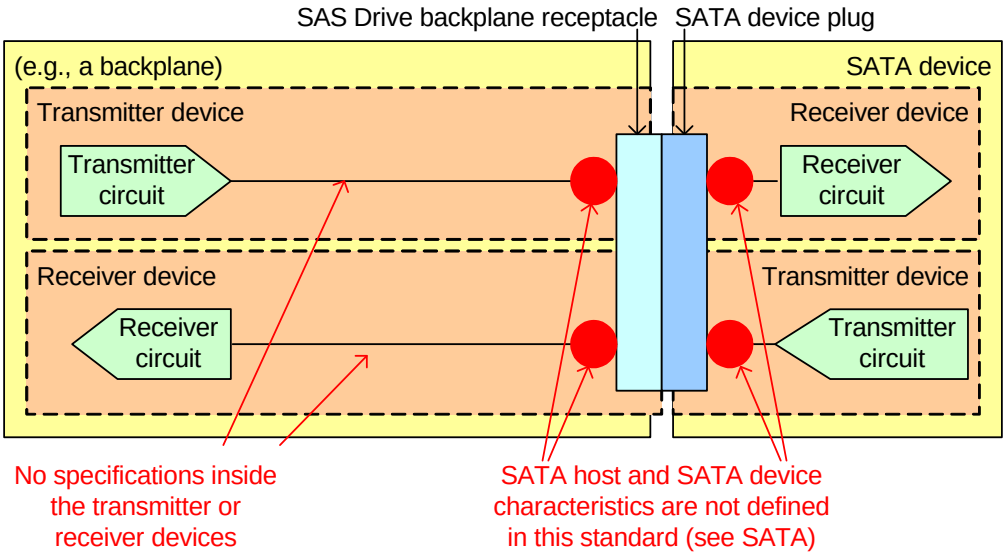

Figure 7 — Backplane with SAS Drive connector compliance points with SATA phy attached

Figure 8 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly, and shows how two of the compliance points are tested using test loads (see 5.7).

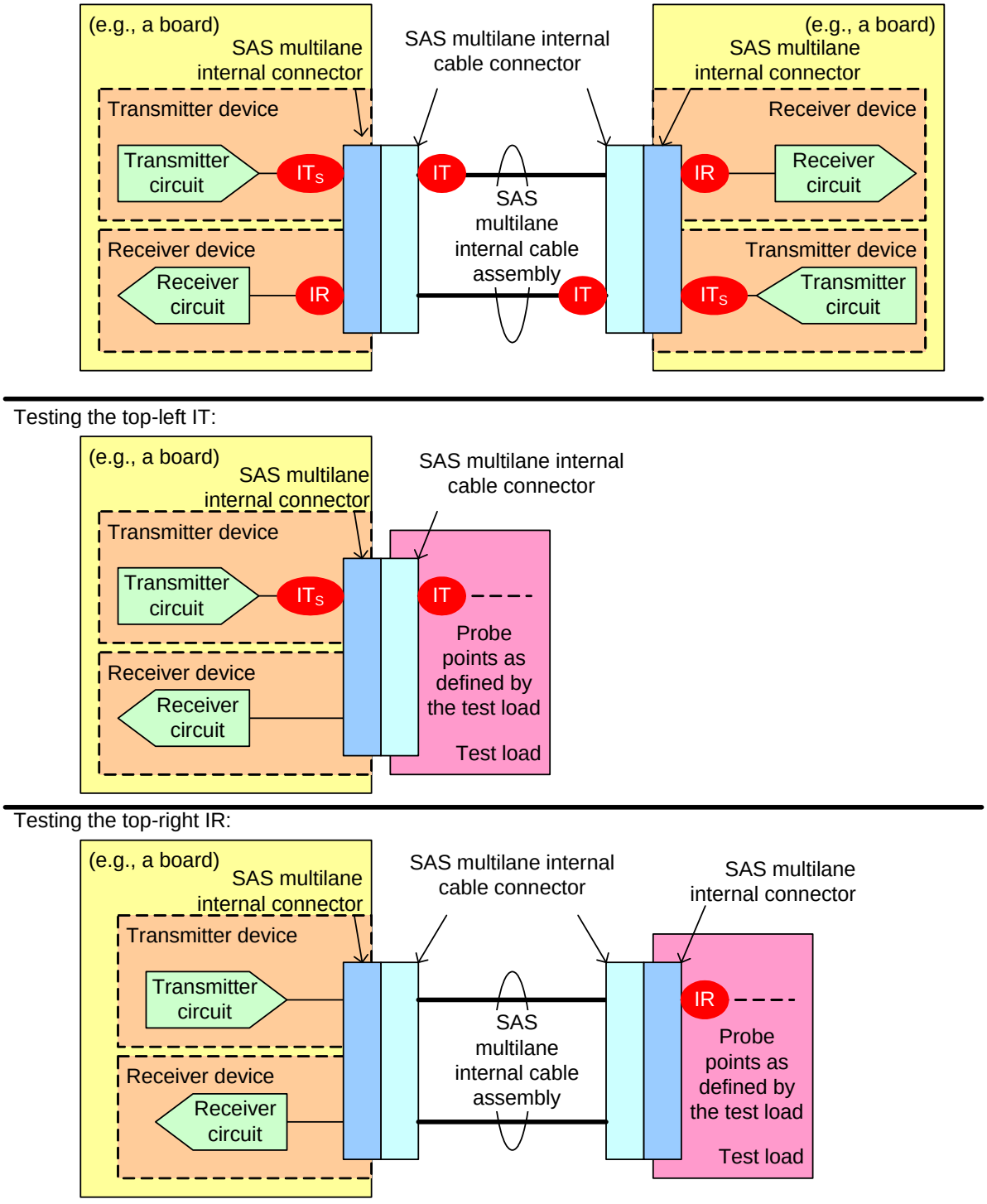

Figure 8 — SAS multilane internal cable assembly IT compliance points and IR compliance points

Figure 9 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.5.3.3.1.3), where the backplane is not attached to a SATA device, and shows how two of the compliance points are tested using test loads (see 5.7).

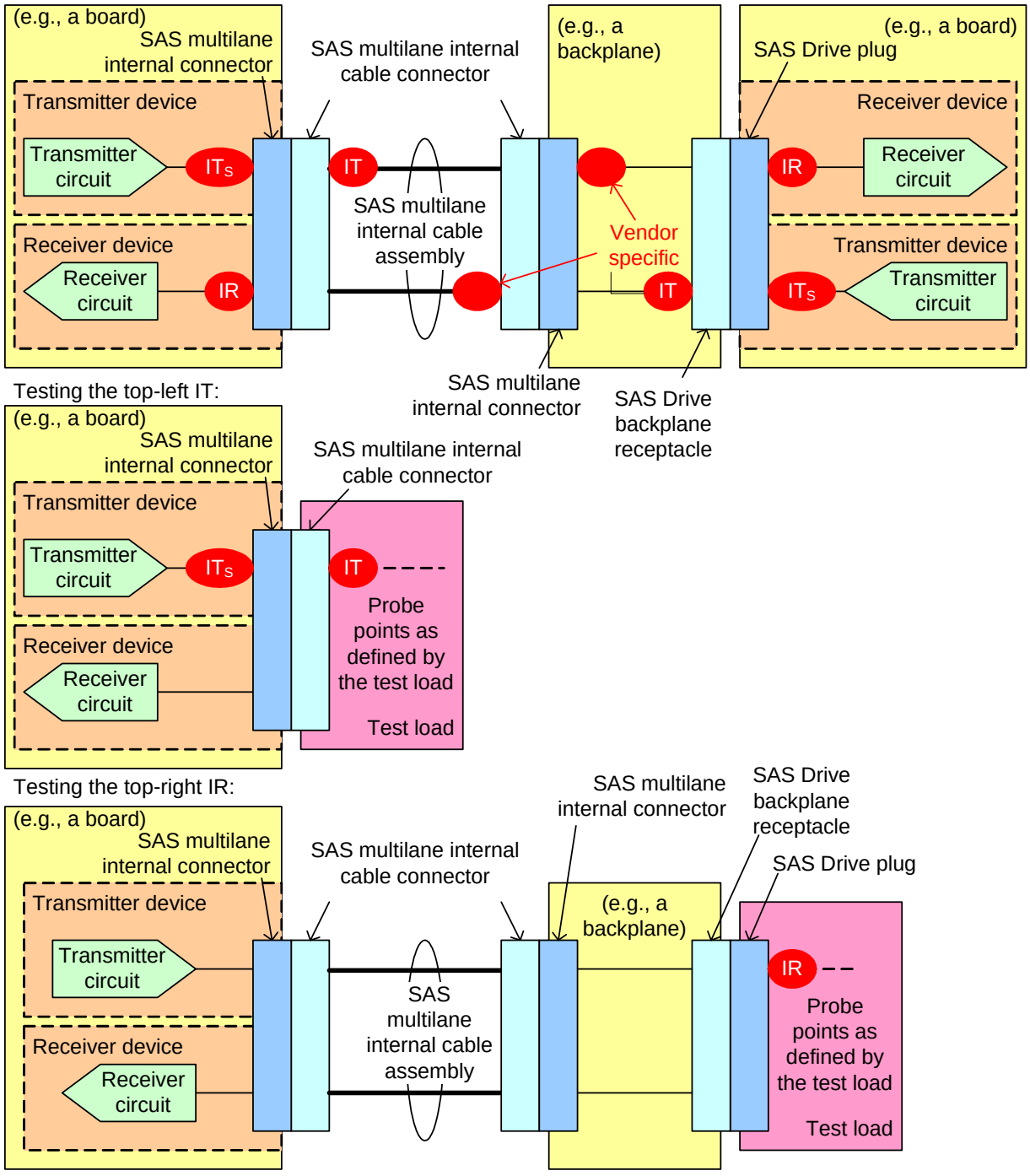

Figure 9 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points

Figure 10 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.5.3.3.1.3) that supports being attached to a SATA device. There are no IT compliance points and IR compliance points at the SAS Drive backplane receptacle connector when a SATA device is attached. In that case, SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device. There are compliance points at the SAS multilane internal connector, however.

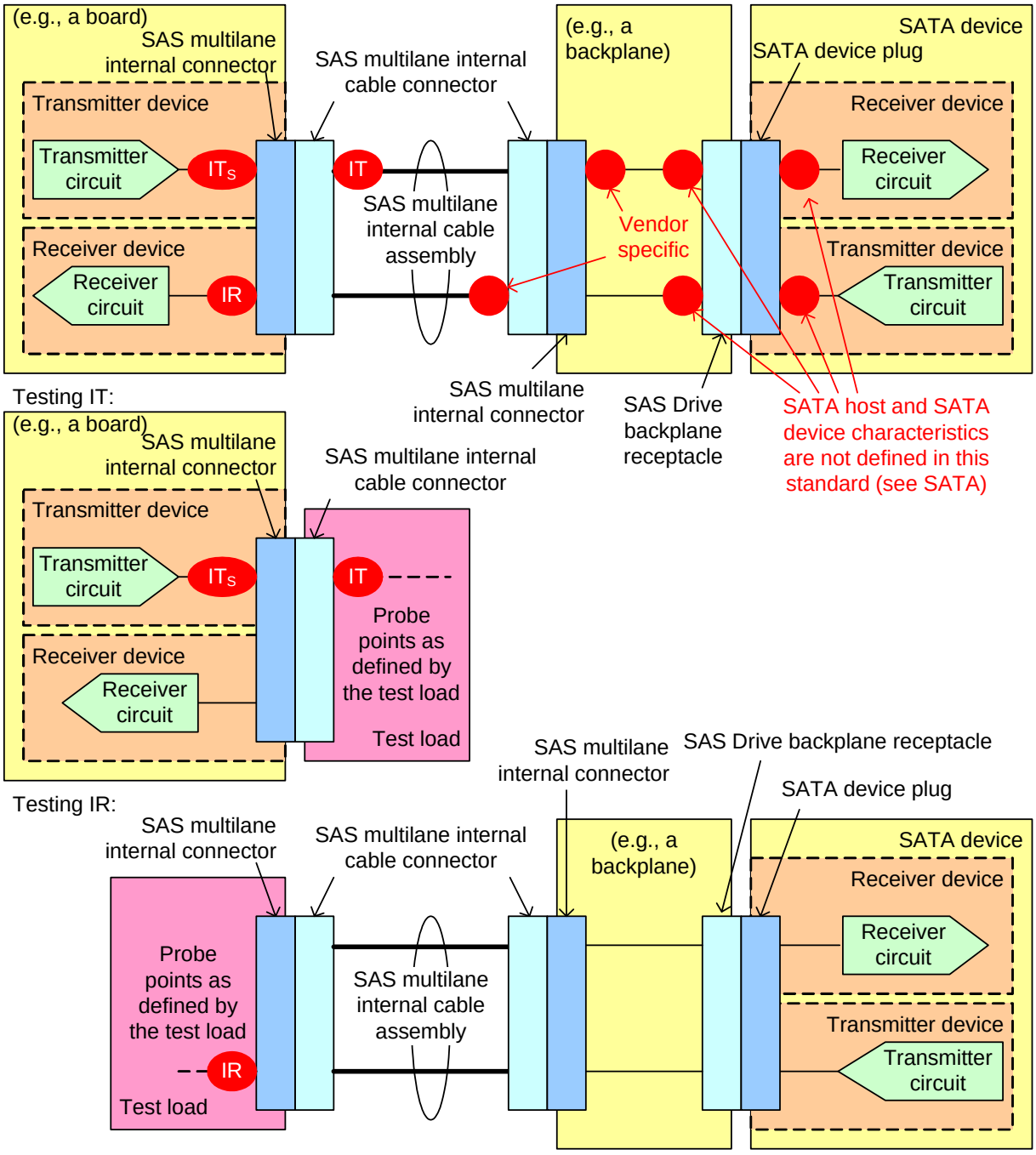

Figure 10 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points with SATA device attached

Figure 11 shows the locations of the IT compliance points and IR compliance points using a SAS Drive cable assembly, and shows how two of the compliance points are tested using test loads (see 5.7).

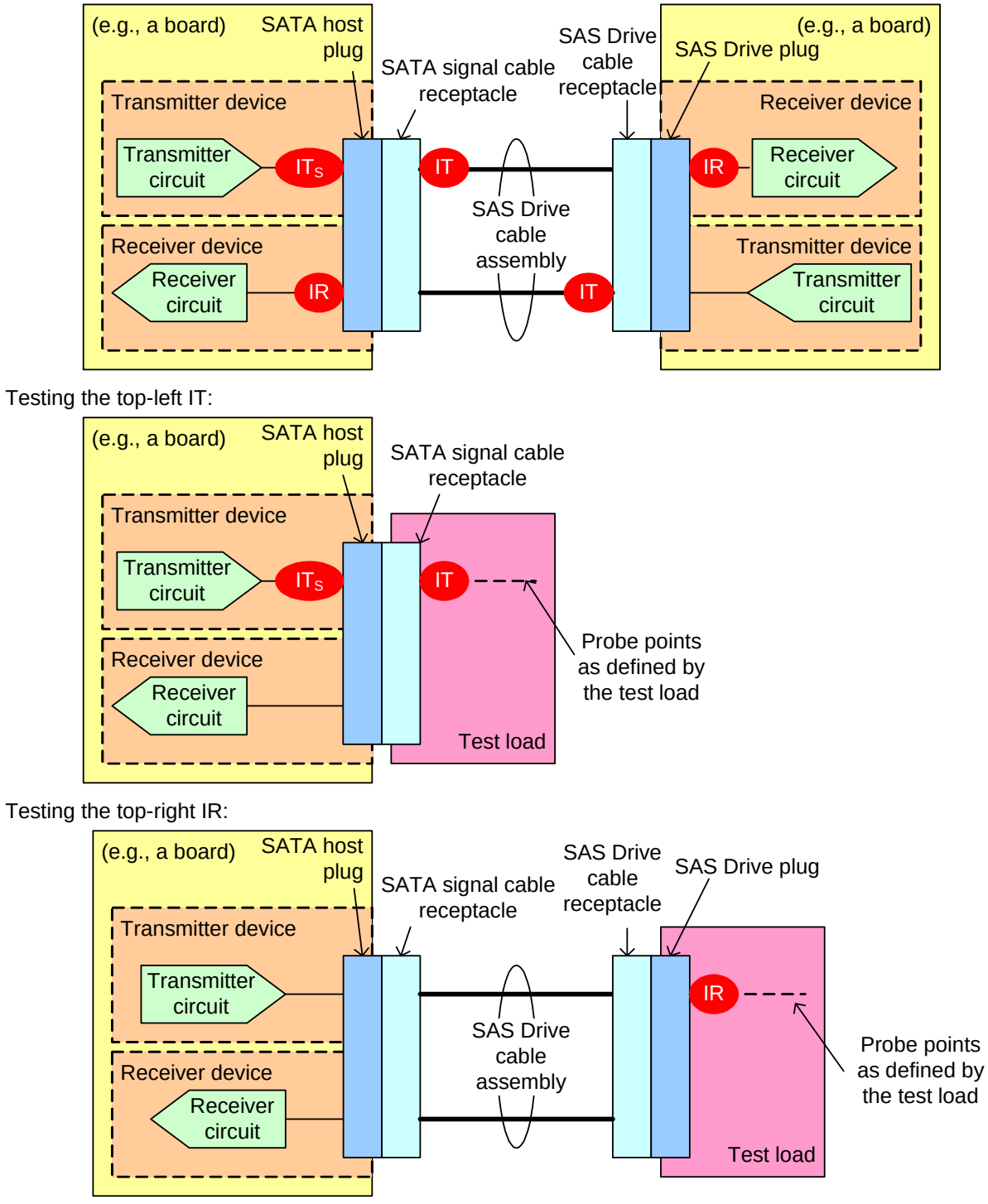

Figure 11 — SAS Drive cable assembly IT compliance points and IR compliance points

5.4 12 Gbps compliance points

A TxRx connection is the complete simplex signal path between the transmitter circuit (see 3.1.107) and receiver circuit (see 3.1.74).

This standard defines the electrical requirements of the signal at the compliance points ET, IT, IR, CT, CR, TC, and ER in a TxRx connection (see table 4). Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this standard only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point. Connector compliance points apply to external cable connections and internal SAS drive connections.

Signal characteristics for connector compliance points are measured at physical positions called probe points in a test load (see 5.7). Measurements at the probe points in a test load approximate measurements at the compliance point in the actual TxRx connection. Some components in the test load may be de-embedded as described in E.5.

Table 4 — 12 Gbps compliance points

Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device (see 3.1.110), as measured at probe points in a test load attached with an internal connector.
IT_S [a]	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device (see 3.1.77), as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT_S	inter-enclosure (i.e., cabinet)	The location of a transmitter device where return loss and S-parameters are measured and where the TxRx connection segment under test begins (see 5.6.6). This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.
ET	transmitter circuit	The output signal from a transmitter circuit measured with the test load, TDCS (see 3.1.111), and TCCS (see 3.1.108) de-embedded.
ER	compliance point	A point defined at the output of the reference receiver device (see 3.1.80)

The TxRx connection characteristics are defined in 5.6.

Figure 12 shows an example TxRx connection for trained 12 Gbps where PICS is the physical interconnect connection segment.

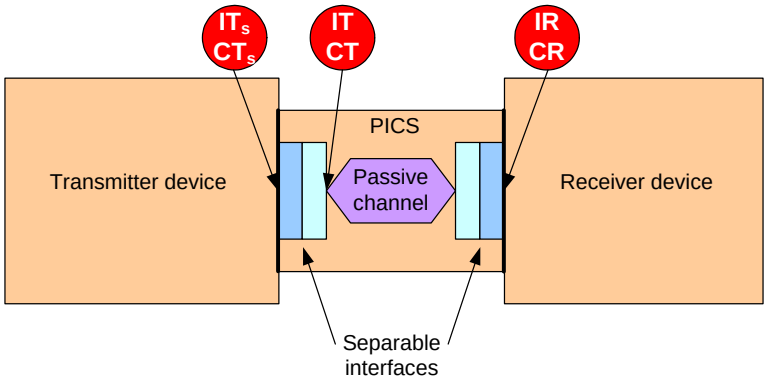

Figure 12 — 12 Gbps TxRx connection and compliance points

Figure 13 shows an example of a simulated TxRx connection for trained 12 Gbps where:

a) TDCS is the transmitter device TxRx connection segment;
b) TCCS is the transmitter circuit TxRx connection segment;
c) RDCS is the receiver device TxRx connection segment;
d) RCCS is the receiver circuit TxRx connection segment; and
e) PICS is the physical interconnect connection segment.

When simulations use a captured signal, the TxRx connection segments located between ET and the compliance point used to capture the signal should be modeled as a single TxRx connection segment. End-to-end simulations (see 5.8.1) compute characteristics of the signal at ET and ER, using measurements taken:

a) at IT, CT, IR or CR; or
b) between CT_S and CR or between IT_S and IR.

Reference TxRx connection segment models provided for end-to-end simulations (see D.2) combine adjacent TxRx connection segments into single models.

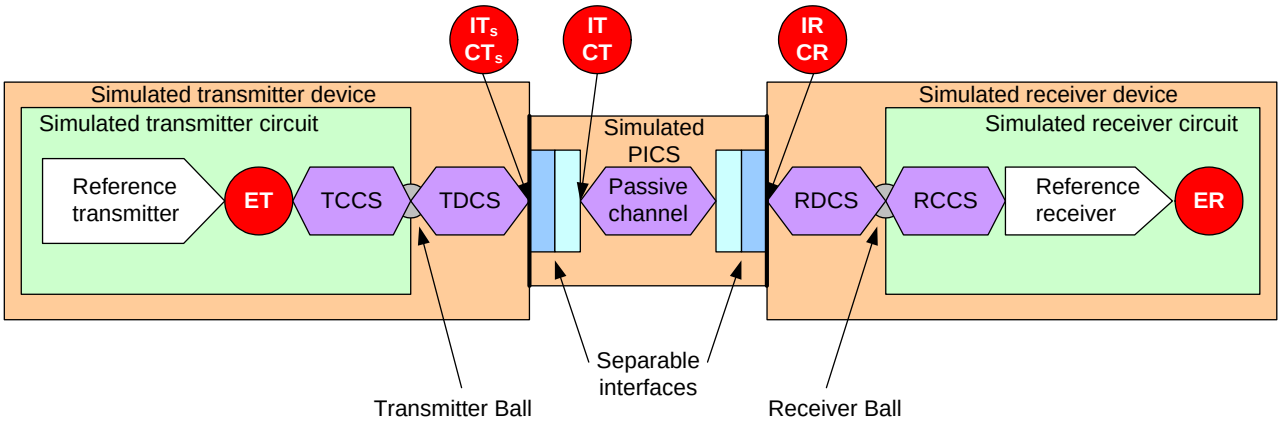

Figure 13 — Simulated 12 GBPS TxRx connection and compliance points

Figure 14 shows the locations of the CT_S compliance points and CR compliance points of an enclosure using an external cable connector, and shows how the enclosure CT_S compliance point and the SAS active cable assembly for 12 Gbps CR compliance point are tested using test loads (see 5.7).

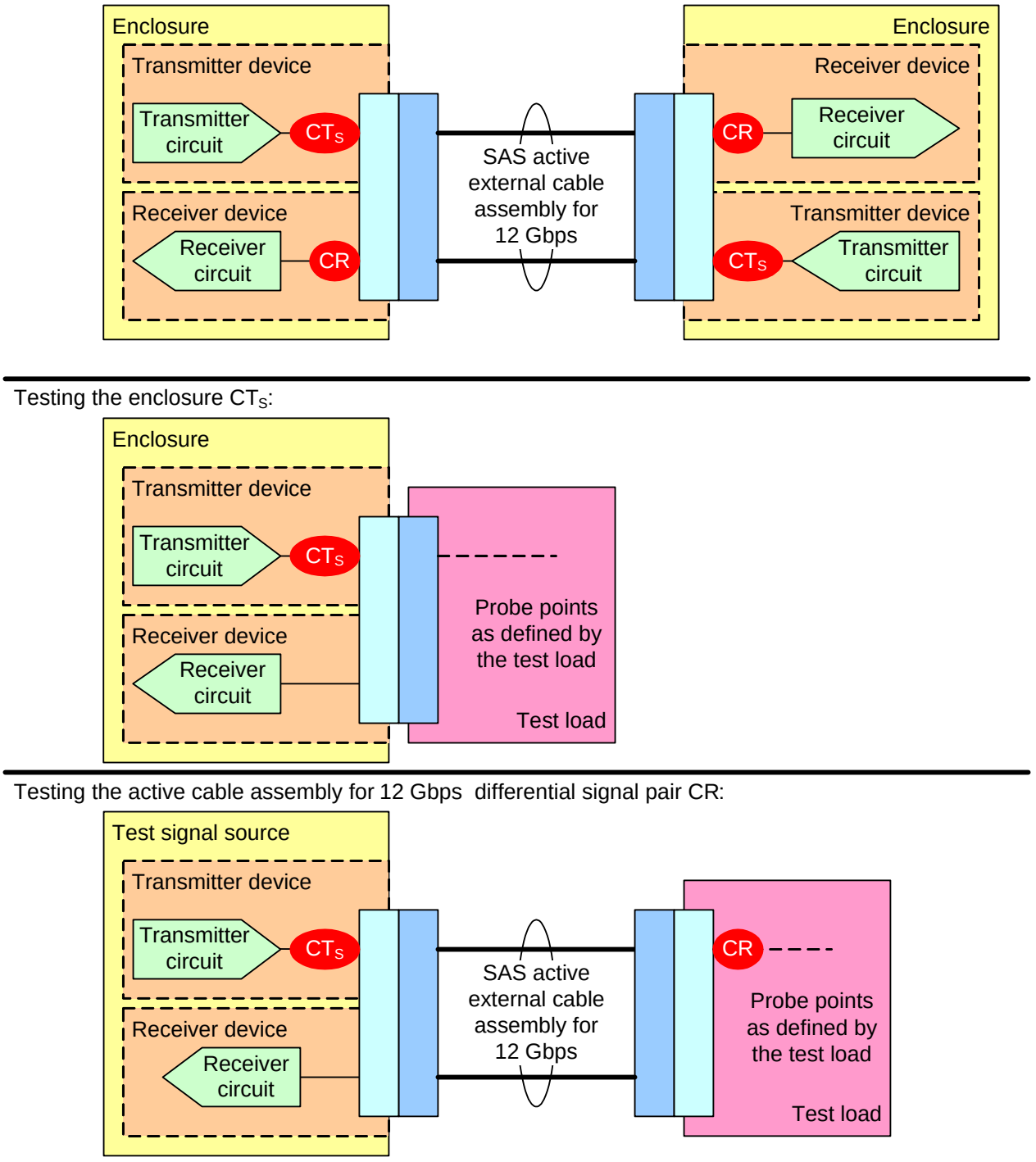

Figure 14 — 12 Gbps CT_S and CR compliance points

5.5 Interconnects

5.5.1 SATA connectors and cable assemblies

Figure 15 shows a representation of the connectors and cables defined by SATA. A SATA host is analogous to a SAS initiator device (see SPL-2) and a SATA device is analogous to a SAS target device (see SPL-2).

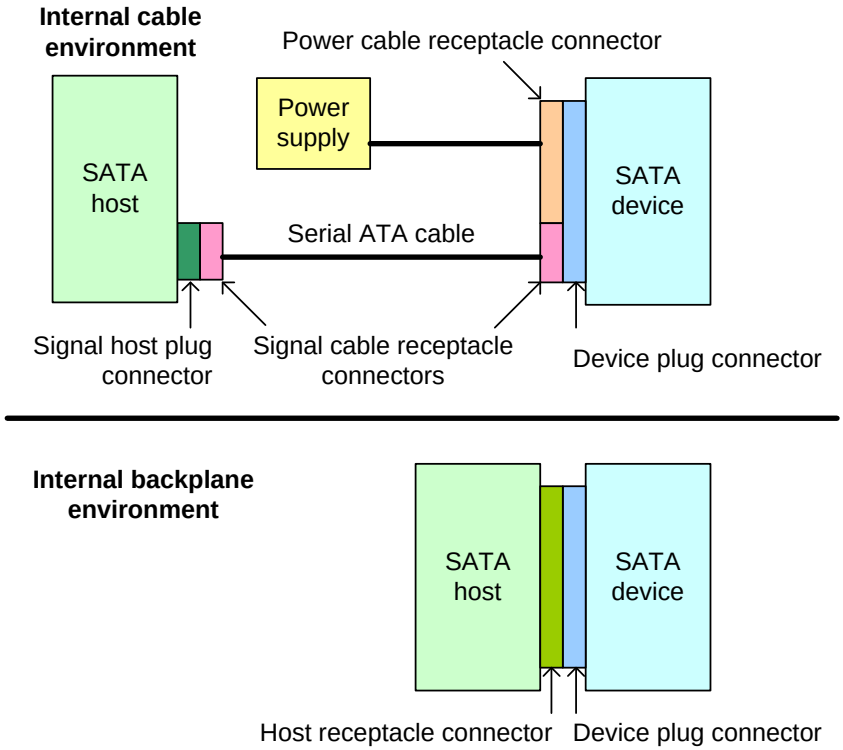

Figure 15 — SATA connectors and cables

5.5.2 SAS connectors and cables

This standard defines SAS Drive cable, SAS Drive backplane, SAS internal cable, and SAS external cable environments.

Figure 16 shows a representation of the SAS Drive cable environments.

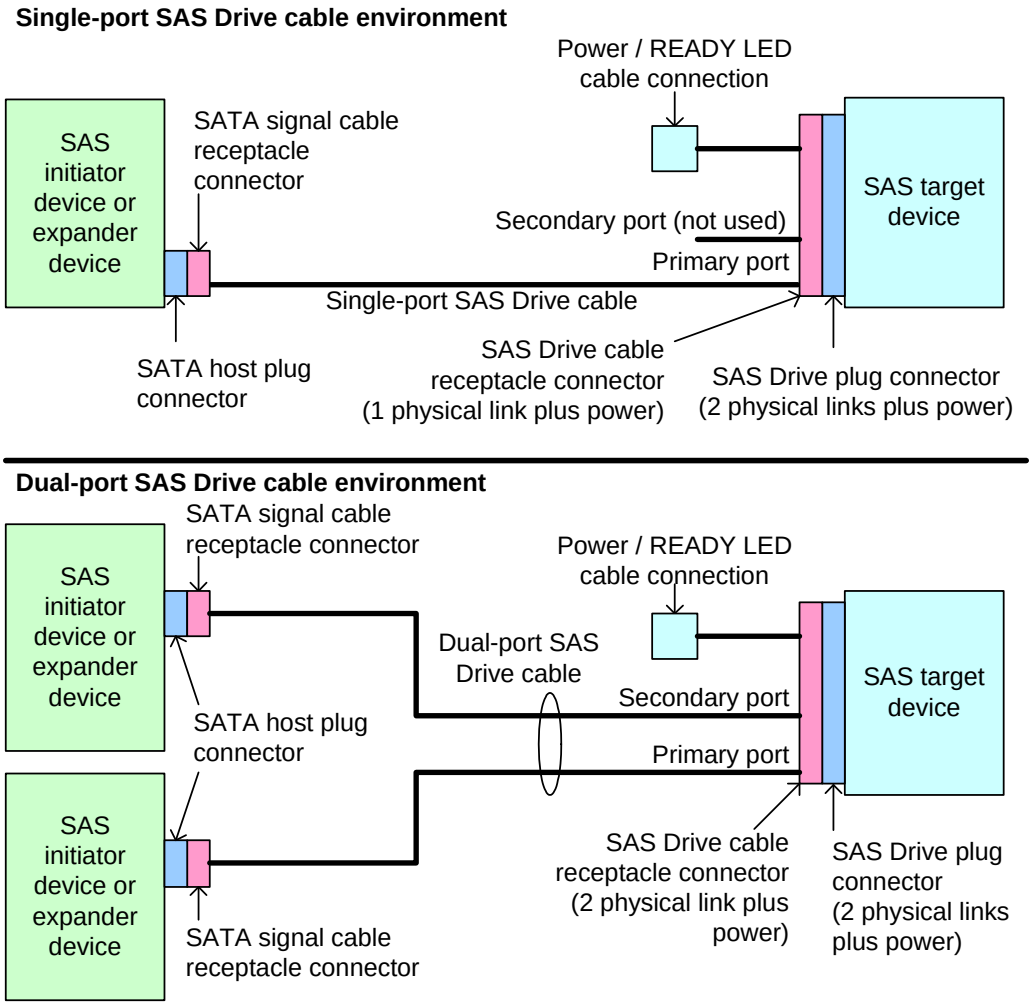

Figure 16 — SAS Drive cable environments

Figure 17 shows a representation of the SAS Drive backplane environment.

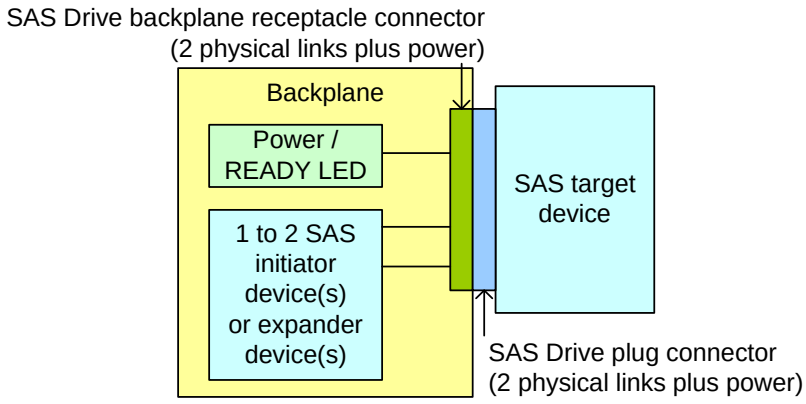

Figure 17 — SAS Drive backplane environment

Figure 18 shows a representation of the SAS external cable environment.

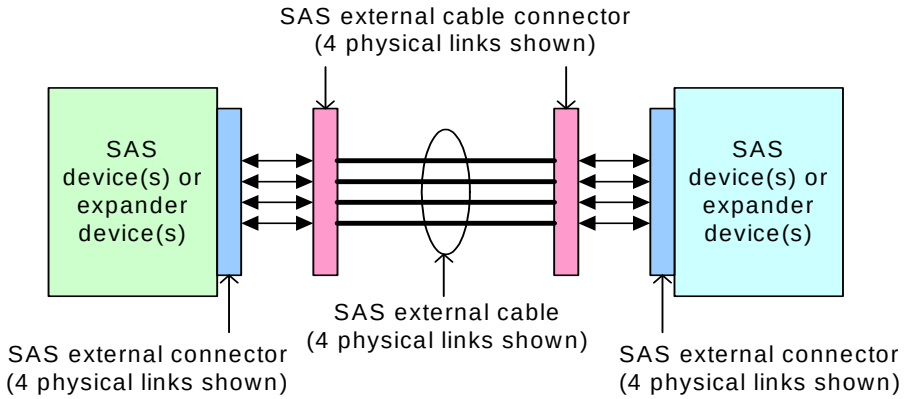

Figure 18 — SAS external cable environment

Figure 19 shows a representation of the SAS internal cable environment attaching a controller to a backplane using a SAS internal symmetric cable (see 5.5.4.1.2).

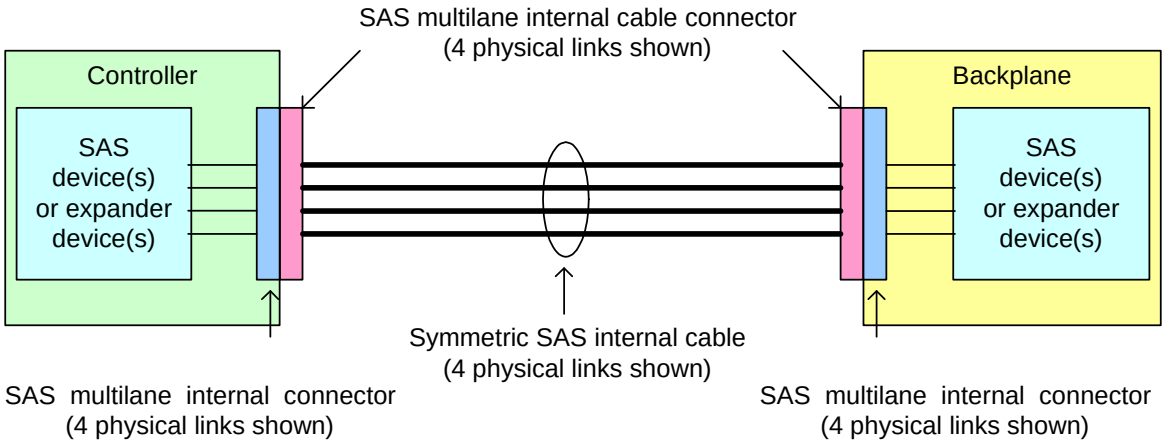

Figure 19 — SAS internal symmetric cable environment - controller to backplane

A SAS internal symmetric cable provides one to eight physical links, and may be used as any combination of wide links and narrow links (see SPL-2) using those physical links.

Figure 20 shows a representation of the SAS internal cable environment attaching a controller to a controller using a SAS internal symmetric cable (see 5.5.4.1.2). Two controllers may also be attached together with a SAS internal symmetric cable.

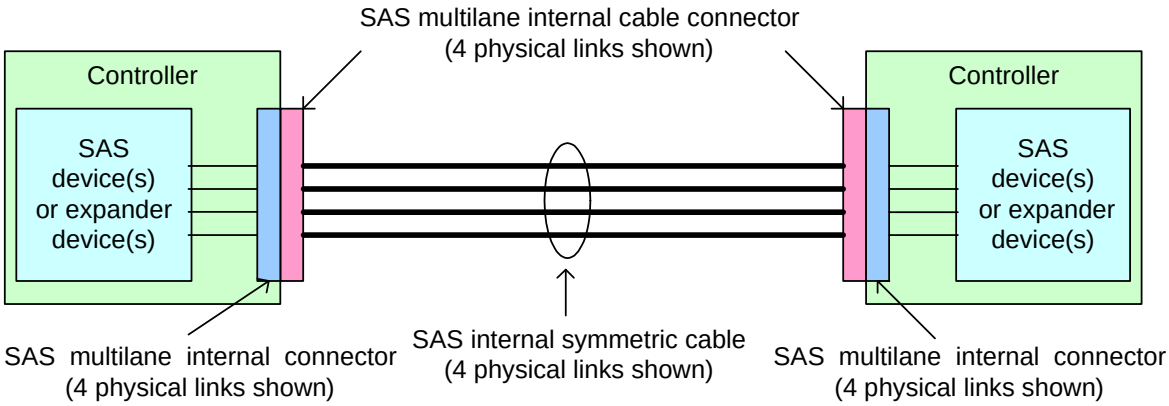

Figure 20 — SAS internal symmetric cable environment - controller to controller

Figure 21 shows a representation of the SAS internal cable environment using a SAS controller-based fanout cable (see 5.5.4.1.3).

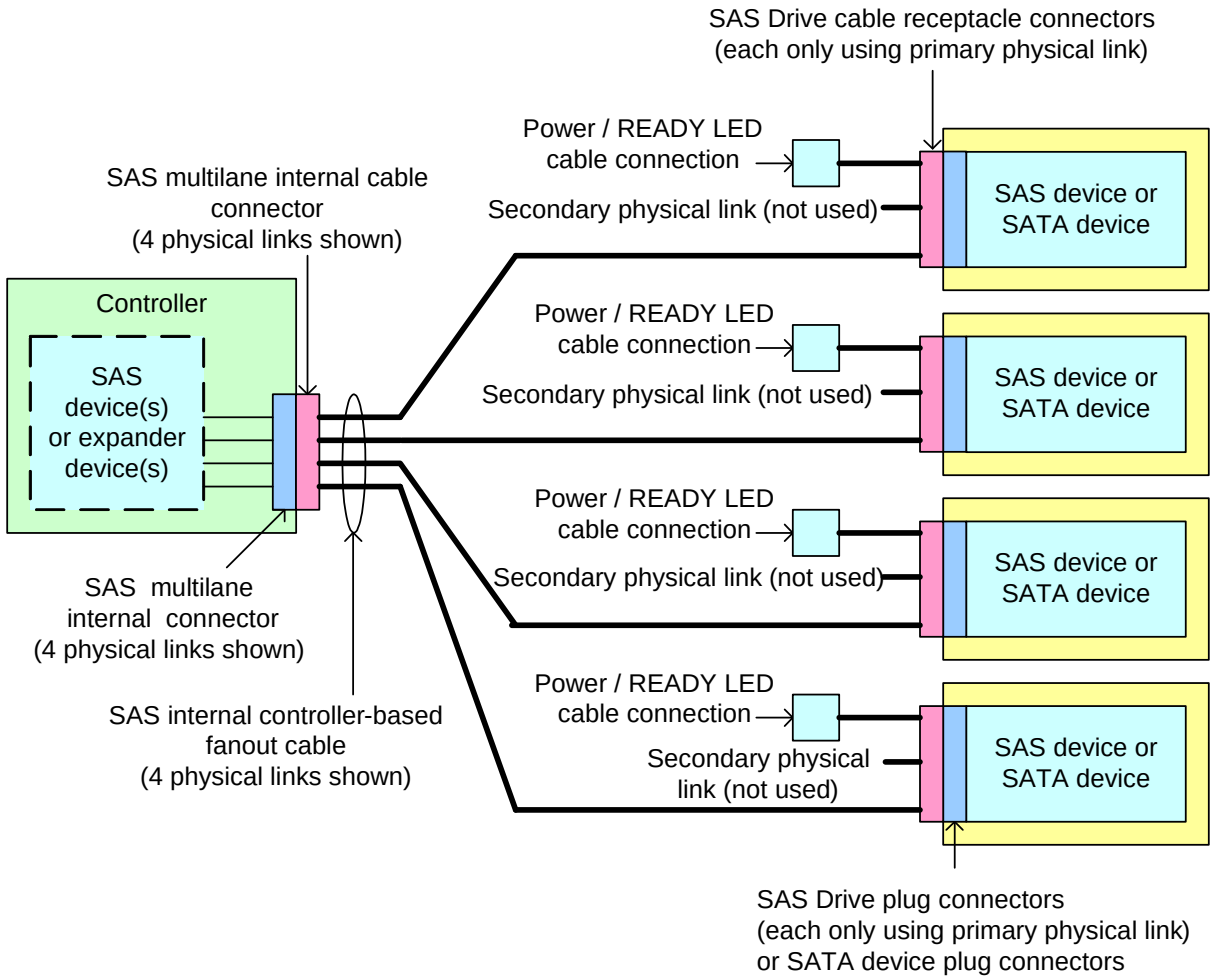

Figure 21 — SAS internal controller-based fanout cable environment

Figure 22 shows a representation of the SAS internal cable environment using a SAS backplane-based fanout cable (see 5.5.4.1.3).

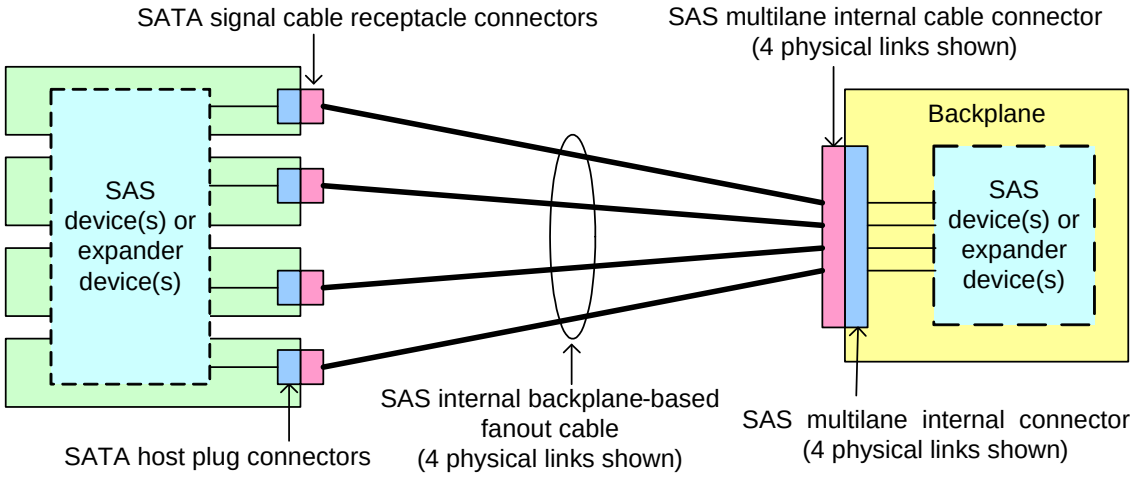

Figure 22 — SAS internal backplane-based fanout cable environment

5.5.3 Connectors

5.5.3.1 Connectors overview

Table 5 summarizes the connectors defined in this standard.

Table 5 — Connectors (part 1 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SATA internal connectors used by SAS					
SATA signal cable receptacle	1	SATA	SATA host plug	1	SATA
SATA host plug	1	SATA	SATA signal cable receptacle	1	SATA
SATA device plug	1	SATA	SAS Drive cable receptacle	1 or 2	5.5.3.3.1.2
			SAS Drive backplane receptacle	2	5.5.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.5.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.5.3.3.1.7
			Multifunction 12 Gb/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
Micro SATA device plug	1	SATA	Micro SAS receptacle	2	5.5.3.3.1.10
Other internal connectors used by SAS					
Multifunction 12 Gb/s 6x Unshielded receptacle connector	6 [a]	SFF-8639	SAS Drive plug	2	5.5.3.3.1.1
			SAS MultiLink Drive plug	4	5.5.3.3.1.5
			SATA device plug	1	SATA
SAS internal connectors - SAS Drive connectors					
SAS Drive plug	2	5.5.3.3.1.1	SAS Drive cable receptacle	1 or 2	5.5.3.3.1.2
			SAS Drive backplane receptacle	2	5.5.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.5.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.5.3.3.1.7
			Multifunction 12 Gb/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
SAS Drive cable receptacle	1 or 2	5.5.3.3.1.2	SAS Drive plug	2	5.5.3.3.1.1
			SAS MultiLink Drive plug	4	5.5.3.3.1.5
			SATA device plug	1	SATA

Table 5 — Connectors (part 2 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SAS Drive backplane receptacle	2	5.5.3.3.1.3	SAS Drive plug	2	5.5.3.3.1.1
			SAS MultiLink Drive plug	4	5.5.3.3.1.5
			SATA device plug	1	SATA
SAS Multilink Drive plug	4	5.5.3.3.1.5	SAS Drive cable receptacle	1 or 2	5.5.3.3.1.2
			SAS Drive backplane receptacle	2	5.5.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.5.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.5.3.3.1.7
			Multifunction 12 Gb/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
SAS MultiLink Drive cable receptacle	4	5.5.3.3.1.6	SAS Drive plug	2	5.5.3.3.1.1
			SAS MultiLink Drive plug	4	5.5.3.3.1.5
			SATA device plug	1	SATA
SAS MultiLink Drive backplane receptacle	4	5.5.3.3.1.7	SAS Drive plug	2	5.5.3.3.1.1
			SAS MultiLink Drive plug	4	5.5.3.3.1.5
			SATA device plug	1	SATA
Micro SAS plug	2	5.5.3.3.1.9	Micro SAS receptacle	2	5.5.3.3.1.10
Micro SAS receptacle	2	5.5.3.3.1.10	Micro SAS plug	2	5.5.3.3.1.9
			Micro SATA device plug	1	SATA
SAS internal connectors - other					
SAS 4i cable receptacle	4	5.5.3.3.2.1	SAS 4i plug	4	5.5.3.3.2.2
SAS 4i plug	4	5.5.3.3.2.2	SAS 4i cable receptacle	4	5.5.3.3.2.1
Mini SAS 4i cable plug	4	5.5.3.3.3.1	Mini SAS 4i receptacle	4	5.5.3.3.3.2
Mini SAS 4i receptacle	4	5.5.3.3.3.2	Mini SAS 4i cable plug	4	5.5.3.3.3.1
Mini SAS HD 4i cable plug	4	5.5.3.3.4.1	Mini SAS HD 4i receptacle	4	5.5.3.3.4.3
			Mini SAS HD 8i receptacle	8	5.5.3.3.4.4
Mini SAS HD 8i cable plug	8	5.5.3.3.4.2	Mini SAS HD 8i cable receptacle	8	5.5.3.3.4.4
Mini SAS HD 4i receptacle	4	5.5.3.3.4.3	Mini SAS HD 4i cable plug	4	5.5.3.3.4.1
Mini SAS HD 8i receptacle	8	5.5.3.3.4.4	Mini SAS HD 4i cable plug	4	5.5.3.3.4.1
			Mini SAS HD 8i cable plug	8	5.5.3.3.4.2

Table 5 — Connectors (part 3 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SAS external connectors					
Mini SAS 4x cable plug	4	5.5.3.4.1.1	Mini SAS 4x receptacle Mini SAS 4x active receptacle	4	5.5.3.4.1.2
Mini SAS 4x receptacle	4	5.5.3.4.1.2	Mini SAS 4x cable plug	4	5.5.3.4.1.1
Mini SAS 4x active cable assembly plug	4	5.5.3.4.1.1	Mini SAS 4x active receptacle	4	5.5.3.4.1.2
Mini SAS 4x active receptacle	4	5.5.3.4.1.2	Mini SAS 4x cable plug Mini SAS 4x active cable assembly plug	4	5.5.3.4.1.1
Mini SAS HD 4x cable plug	4	5.5.3.4.2.1	Mini SAS HD 4x receptacle	4	5.5.3.4.2.3
			Mini SAS HD 8x receptacle	8	5.5.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.5.3.4.2.5
Mini SAS HD 8x cable plug	8	5.5.3.4.2.2	Mini SAS HD 8x receptacle	8	5.5.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.5.3.4.2.5
Mini SAS HD 4x receptacle	4	5.5.3.4.2.3	Mini SAS HD 4x cable plug	4	5.5.3.4.2.1
Mini SAS HD 8x receptacle	8	5.5.3.4.2.4	Mini SAS HD 4x cable plug	4	5.5.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.5.3.4.2.2
Mini SAS HD 16x receptacle	16	5.5.3.4.2.5	Mini SAS HD 4x cable plug	4	5.5.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.5.3.4.2.2
QSFP+ cable plug	4	5.5.3.4.3.1	QSFP+ receptacle	4	5.5.3.4.3.2
QSFP+ receptacle	4	5.5.3.4.3.2	QSFP+ cable plug	4	5.5.3.4.3.1

[a] A maximum of four physical links support SAS applications.

A SAS icon (see annex H) should be placed on or near each SAS connector.

5.5.3.2 Connector categories

The relationship between connector categories and connectors is shown in table 6.

Table 6 — Connector categories

Connector category	Connectors in category
Unmanaged passive	All connectors listed in table 5 (see 5.5.3.1) that are not listed elsewhere in this table
Unmanaged active	Mini SAS 4x active connectors (see 5.5.3.4.1)
Managed	Mini SAS HD external connectors (see 5.5.3.4.2) QSFP+ connectors (see 5.5.3.4.3)

5.5.3.3 SAS internal connectors

5.5.3.3.1 SAS Drive connectors

5.5.3.3.1.1 SAS Drive plug connector

The SAS Drive plug connector is the Device Free (Plug) connector defined in SFF-8482 and SFF-8680.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 23 shows the SAS Drive plug connector.

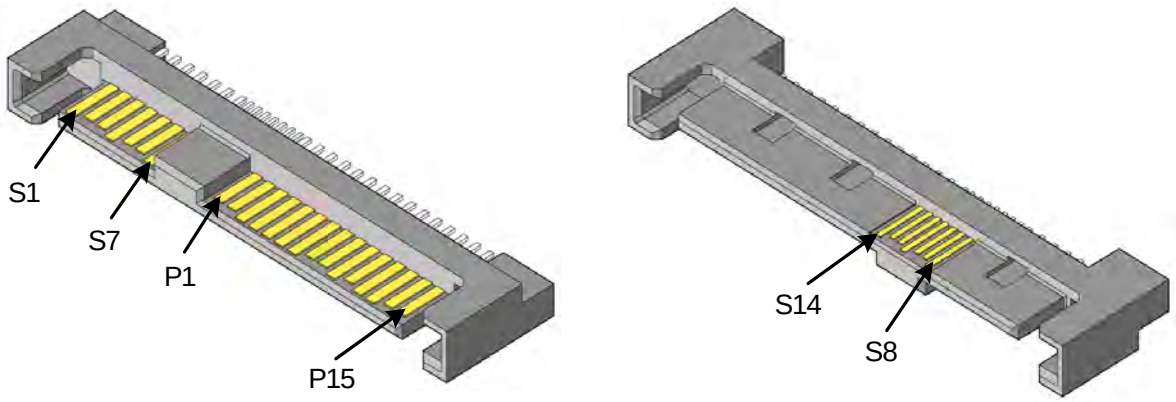

Figure 23 — SAS Drive plug connector

Table 7 (see 5.5.3.3.1.4) defines the pin assignments for the SAS Drive plug connector.

5.5.3.3.1.2 SAS Drive cable receptacle connector

The SAS Drive cable receptacle connector is the Internal Cable Fixed (Receptacle) connector defined in SFF-8482 and SFF-8680.

The single-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link; or
b) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 24 shows the single-port version of the SAS Drive cable receptacle connector.

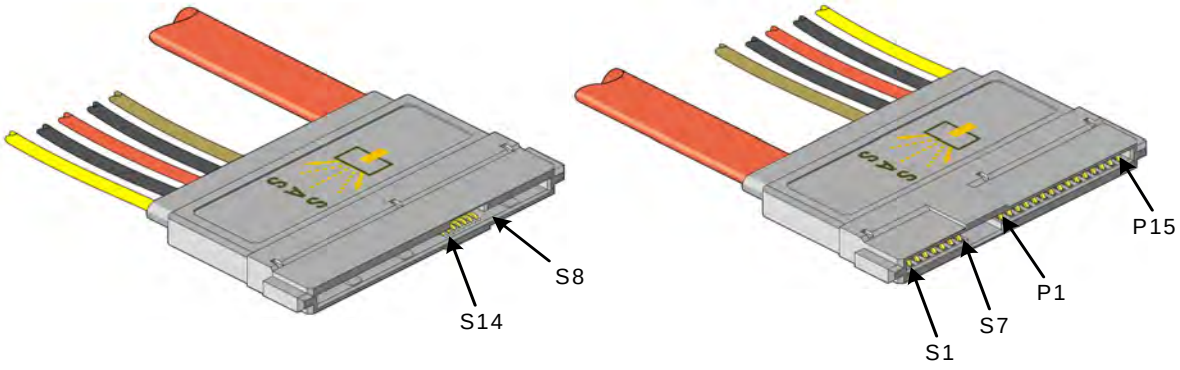

Figure 24 — Single-port SAS Drive cable receptacle connector

The dual-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;

b) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 25 shows the dual-port version of the SAS Drive cable receptacle connector.

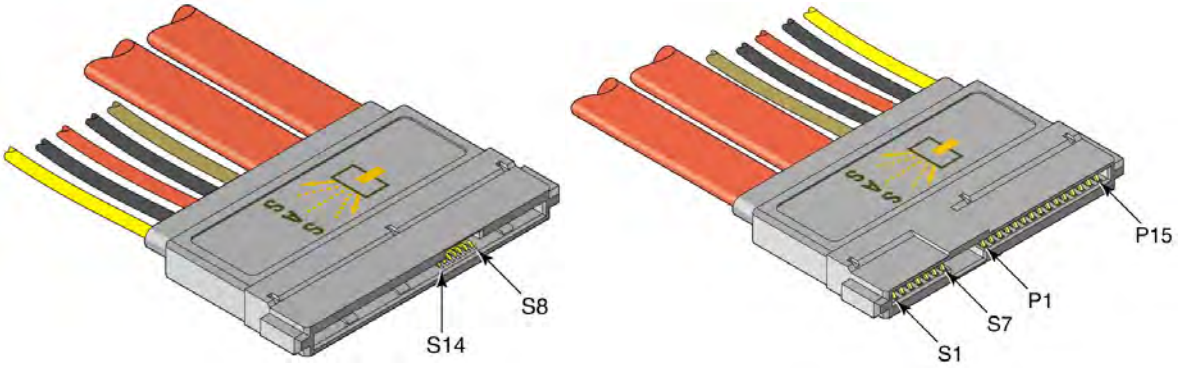

Figure 25 — Dual-port SAS Drive cable receptacle connector

Table 7 (see 5.5.3.3.1.4) defines the pin assignments for the SAS Drive cable receptacle connector. The secondary physical link (i.e., pins S8 through S14) is not supported by the single-port internal cable receptacle.

5.5.3.3.1.3 SAS Drive backplane receptacle connector

The SAS Drive backplane receptacle connector is the Backplane Fixed (Receptacle) connector defined in SFF-8482 and SFF-8680.

The SAS Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 26 shows the SAS Drive backplane receptacle connector.

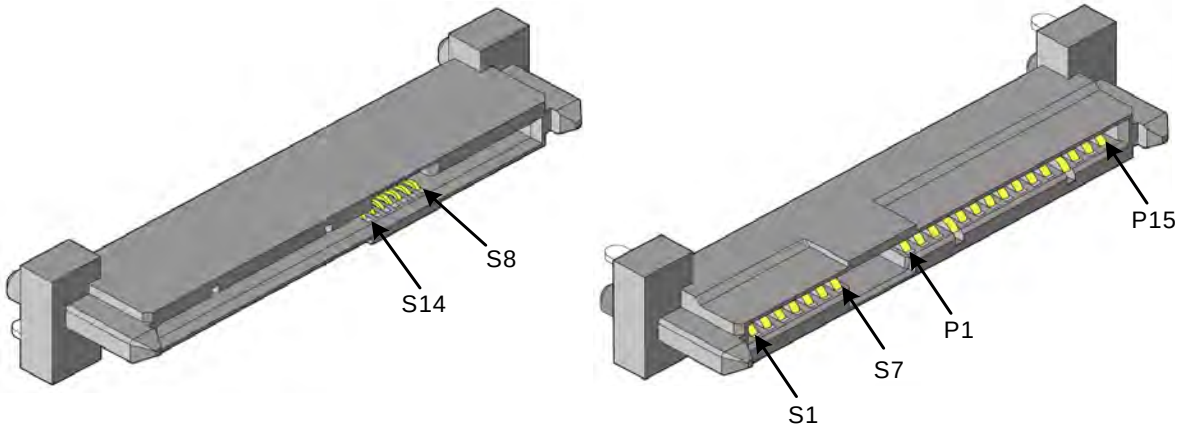

Figure 26 — SAS Drive backplane receptacle connector

Table 7 (see 5.5.3.3.1.4) defines the pin assignments for the SAS Drive backplane receptacle connector.

5.5.3.3.1.4 SAS Drive connector pin assignments

Table 7 defines the SAS target device pin assignments for the SAS Drive plug connector (see 5.5.3.3.1.1), the SAS Drive cable receptacle connector (see 5.5.3.3.1.2), and the SAS Drive backplane receptacle connector (see 5.5.3.3.1.3). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

SAS Drive plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a SATA device plug connector (see SATA).

Table 7 — SAS Drive connector pin assignments

Segment	Pin	Backplane receptacle	SAS Drive plug and SAS Drive cable receptacle
Primary signal segment	S1	SIGNAL GROUND	
	S2	TP+	RP+
	S3	TP-	RP-
	S4	SIGNAL GROUND	
	S5	RP-	TP-
	S6	RP+	TP+
	S7	SIGNAL GROUND	
Secondary signal segment [a]	S8	SIGNAL GROUND	
	S9	TS+	RS+
	S10	TS-	RS-
	S11	SIGNAL GROUND	
	S12	RS-	TS-
	S13	RS+	TS+
	S14	SIGNAL GROUND	
Power segment [b]	P1	V_{33} [c]	
	P2	V_{33} [c]	
	P3	V_{33}, precharge [c]	
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [c]	
	P8	V_5 [c]	
	P9	V_5 [c]	
	P10	GROUND	
	P11	READY LED [d]	
	P12	GROUND	
	P13	V_{12}, precharge [c]	
	P14	V_{12} [c]	
	P15	V_{12} [c]	

[a] S8 through S14 are not connected on single-port implementations.

[b] Backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_{33}, V_5, and V_{12}. SAS Device plug connectors receive V_{33}, V_5, and V_{12}.

[c] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).

[d] Electrical characteristics for READY LED are defined in 5.10 and signal behavior is defined in SPL-2. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.5.3.3.1.5 SAS MultiLink Drive plug connector

The SAS MultiLink Drive plug connector is the Device free (plug) connector defined in SFF-8630.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 27 shows the SAS MultiLink Drive plug connector

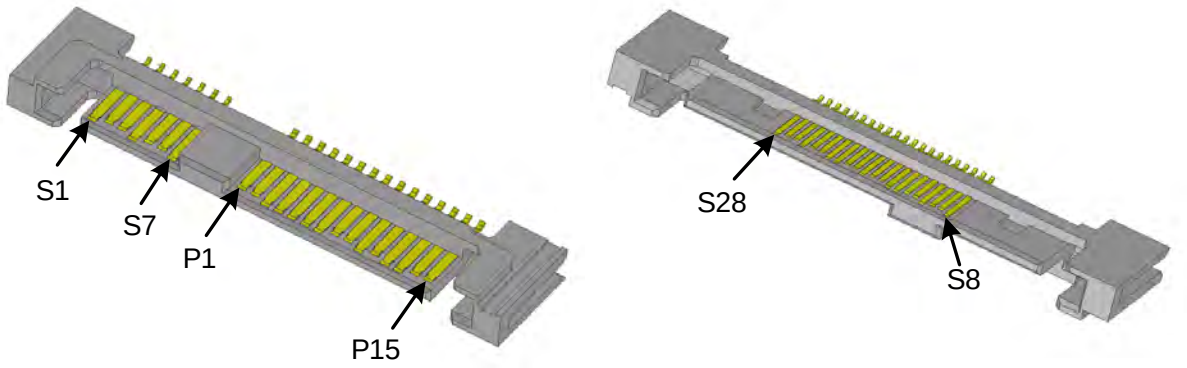

Figure 27 — SAS MultLink Drive plug connector

Table 8 (see 5.5.3.3.1.8) defines the pin assignments for the SAS MultiLink Drive plug connector.

5.5.3.3.1.6 SAS MultiLink Drive cable receptacle connector

The SAS MultiLink Drive cable receptacle connector is the Internal Cable Fixed (Receptacle) connector defined in SFF-8630.

The SAS MultiLink Drive cable receptacle attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 28 shows the SAS MultiLink Drive cable receptacle connector.

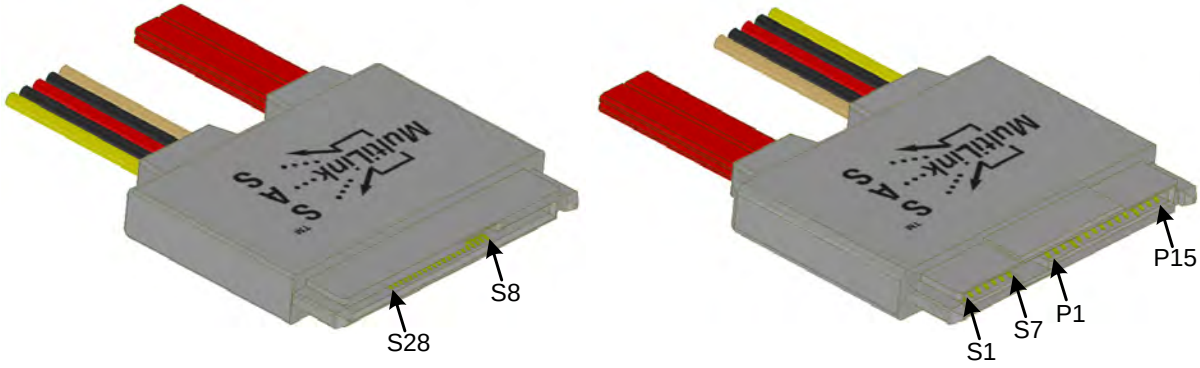

Figure 28 — SAS MultiLink Drive cable receptacle connector

Table 8 (see 5.5.3.3.1.4) defines the pin assignments for the SAS MultiLink Drive cable receptacle connector.

5.5.3.3.1.7 SAS MultiLink Drive backplane receptacle connector

The SAS MultiLink Drive backplane receptacle connector is the Backplane Fixed (Receptacle) connector defined in SFF-8630.

The SAS MultiLink Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 29 shows the SAS MultiLink Drive backplane receptacle connector.

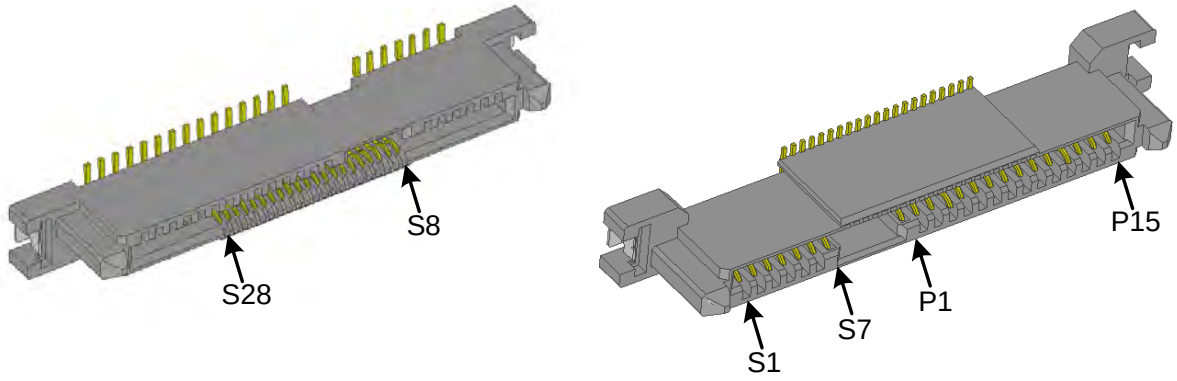

Figure 29 — SAS MultiLink Drive backplane receptacle connector

Table 8 (see 5.5.3.3.1.8) defines the pin assignments for the SAS MultiLink Drive backplane receptacle connector.

5.5.3.3.1.8 SAS MultiLink Drive connector pin assignments

Table 8 defines the SAS target device pin assignments for the SAS MultiLink Drive plug connector (see 5.5.3.3.1.5), the SAS MultiLink Drive cable receptacle connector (see 5.5.3.3.1.6), and the SAS MultiLink Drive backplane receptacle connector (see 5.5.3.3.1.7). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

SAS MultiLink Drive plug connector pin assignments, except for the physical links in addition to the primary physical link, are in the same locations as they are in a SATA device plug connector (see SATA).

Table 8 — SAS MultiLink connector pin assignments (part 1 of 2)

Segment	Pin	SAS MultiLink Drive backplane receptacle	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle
Signal segment 0	S1	SIGNAL GROUND	
	S2	Tx 0+	Rx 0+
	S3	Tx 0-	Rx 0-
	S4	SIGNAL GROUND	
	S5	Rx 0-	Tx 0-
	S6	Rx 0+	Tx 0+
	S7	SIGNAL GROUND	
Signal segment 1 [a]	S8	SIGNAL GROUND	
	S9	Tx 1+	Rx 1+
	S10	Tx 1-	Rx 1-
	S11	SIGNAL GROUND	
	S12	Rx 1-	Tx 1-
	S13	Rx 1+	Tx 1+
	S14	SIGNAL GROUND	
	S15	RESERVED	
Signal segment 2 [a, b]	S16	SIGNAL GROUND	
	S17	Tx 2+	Rx 2+
	S18	Tx 2-	Rx 2-
	S19	SIGNAL GROUND	
	S20	Rx 2-	Tx 2-
	S21	Rx 2+	Tx 2+
	S22	SIGNAL GROUND	
Signal segment 3 [a, b, c]	S23	Tx 3+	Rx 3+
	S24	Tx 3-	Rx 3-
	S25	SIGNAL GROUND	
	S26	Rx 3-	Tx 3-
	S27	Rx 3+	Tx 3+
	S28	SIGNAL GROUND	

Table 8 — SAS MultiLink connector pin assignments (part 2 of 2)

Segment	Pin	SAS MultiLink Drive backplane receptacle	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle
Power segment [d]	P1	RESERVED	
	P2	RESERVED	
	P3	RESERVED	
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [e]	
	P8	V_5 [e]	
	P9	V_5 [e]	
	P10	GROUND	
	P11	READY LED [f]	
	P12	GROUND	
	P13	V_{12}, precharge [e]	
	P14	V_{12} [e]	
	P15	V_{12} [e]	

[a] S8 through S28 are not connected on single-port implementations.
[b] S15 through S28 are not connected on dual-port implementations.
[c] S22 through S28 are not connected on triple-port implementations.
[d] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[e] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V5 pins P8 and P9).
[f] Electrical characteristics for READY LED are defined in 5.10 and signal behavior is defined in SPL-2. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.5.3.3.1.9 Micro SAS plug connector

The Micro SAS plug connector is defined in SFF-8486. The Micro SAS plug mates with the Micro SAS Receptacle (see 5.5.3.3.1.10), but not the Micro SATA receptacle (see SATA).

See SFF-8147 for the Micro SAS plug connector locations on common form factors. Figure 30 shows the Micro SAS plug connector.

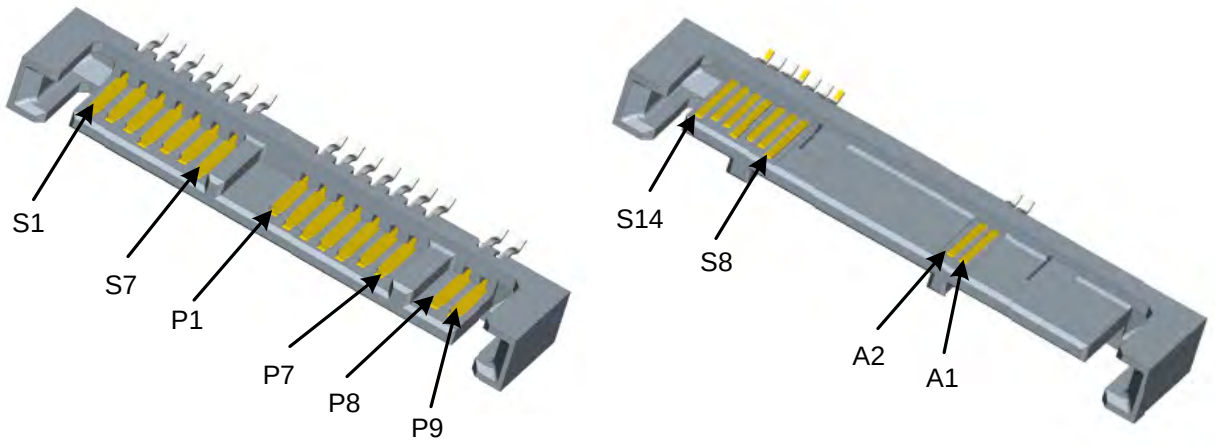

Figure 30 — Micro SAS plug connector

5.5.3.3.1.10 Micro SAS receptacle connector

The Micro SAS receptacle connector is defined in SFF-8486. The Micro SAS receptacle mates with the Micro SAS plug connector (see 5.5.3.3.1.9) or the Micro SATA device plug (see SATA).

Figure 31 shows the Micro SAS receptacle connector.

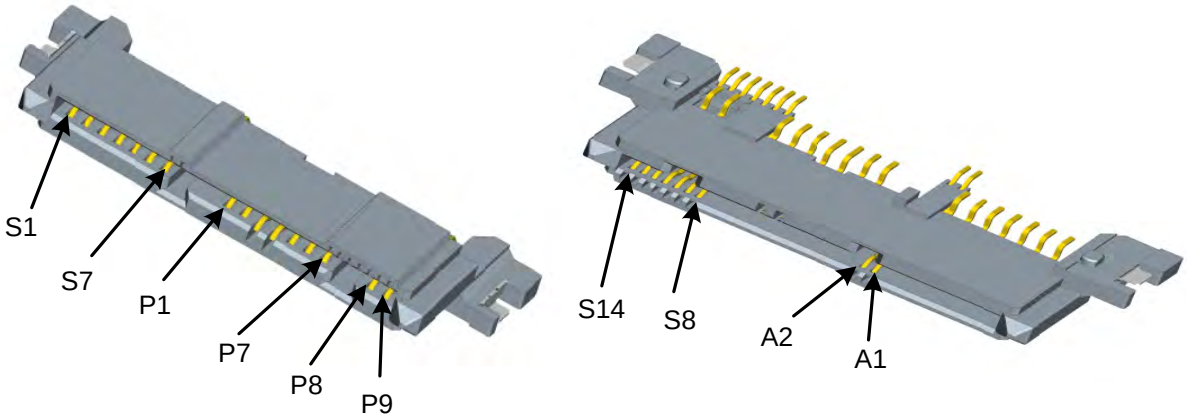

Figure 31 — Micro SAS receptacle connector

5.5.3.3.1.11 Micro SAS connector pin assignments

Table 9 defines the SAS target device pin assignments for the Micro SAS plug connector (see 5.5.3.3.1.9) and the Micro SAS receptacle connector (see 5.5.3.3.1.10). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

Micro SAS plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a Micro SATA device plug connector (see SATA).

Table 9 — Micro SAS connector pin assignments

Segment	Pin	Micro SAS receptacle	Micro SAS plug	Mating level [e]
Primary signal segment	S1	SIGNAL GROUND		Second
	S2	TP+	RP+	Third
	S3	TP-	RP-	Third
	S4	SIGNAL GROUND		Second
	S5	RP-	TP-	Third
	S6	RP+	TP+	Third
	S7	SIGNAL GROUND		Second
Secondary signal segment [a]	S8	SIGNAL GROUND		Second
	S9	TS+	RS+	Third
	S10	TS-	RS-	Third
	S11	SIGNAL GROUND		Second
	S12	RS-	TS-	Third
	S13	RS+	TS+	Third
	S14	SIGNAL GROUND		Second
Power segment [b]	P1	V_{33} [c]		Third
	P2	V_{33}, precharge [c]		Second
	P3	GROUND		First
	P4	GROUND		First
	P5	V_5, precharge [c]		Second
	P6	V_5 [c]		Third
	P7	Reserved		Third
	P8	N/C [d]	Manufacturing diagnostic	Third
	P9	N/C [d]	Manufacturing diagnostic	Third
Auxiliary contacts	A1	Vender specific		Third
	A2	Vender specific		Third

[a] S8 through S14 are not connected on single-port implementations.

[b] The Micro SAS receptacle connector (see 5.5.3.3.1.10) provides V_{33} and V_5. The Micro SATA power receptacle connector (see SATA) provides V_{33} and optionally V_5. The Micro SAS plug connector (see 5.5.3.3.1.9) receives V_{33} and V_5.

[c] Behind a Micro SAS plug connector (see 5.5.3.3.1.9), the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_{33}, precharge pin P2 is connected to the V_{33} pin P1).

[d] N/C = not connected

[e] The mating level assumes zero angular offset between connectors and indicates the physical dimension of the contact (see SFF-8486 and SATA).

5.5.3.3.2 SAS 4i connectors

5.5.3.3.2.1 SAS 4i cable receptacle connector

The SAS 4i cable receptacle connector is the 4 Lane Cable Receptacle (fixed) with Backshell connector defined in SFF-8484.

Figure 32 shows the SAS 4i cable receptacle connector.

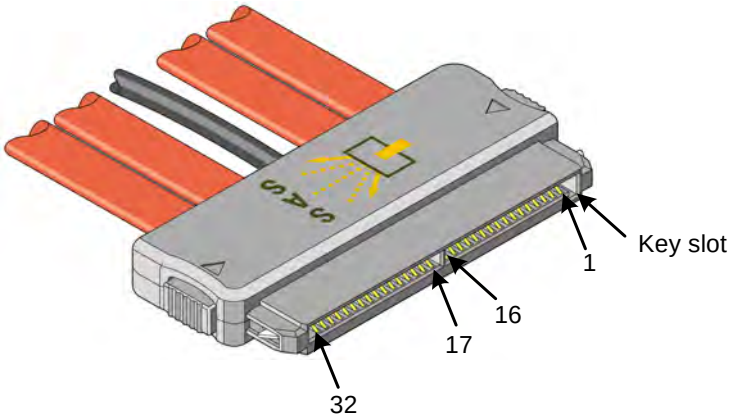

Figure 32 — SAS 4i cable receptacle connector

Table 10 and table 11 (see 5.5.3.3.2.3) define the pin assignments for the SAS 4i cable receptacle connector.

5.5.3.3.2.2 SAS 4i plug connector

The SAS 4i plug connector is the 4 Lane Vertical Plug (free) or 4 Lane R/A Plug (free) connector defined in SFF-8484.

Figure 33 shows the SAS 4i plug connector.

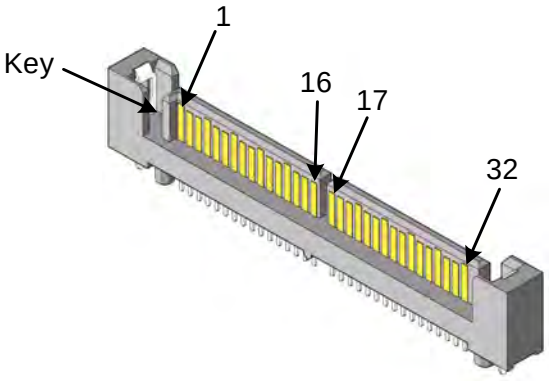

Figure 33 — SAS 4i plug connector

Table 10 and table 11 (see 5.5.3.3.2.3) define the pin assignments for the SAS 4i plug connector.

5.5.3.3.2.3 SAS 4i connector pin assignments

Table 10 defines the pin assignments for SAS 4i cable receptacle connectors (see 5.5.3.3.2.1) and SAS 4i plug connectors (see 5.5.3.3.2.2) for controller applications using one, two, three, or four of the physical links.

Table 10 — Controller SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]			
	One	Two	Three	Four
Rx 0+	2	2	2	2
Rx 0-	3	3	3	3
Tx 0-	5	5	5	5
Tx 0+	6	6	6	6
Rx 1+	N/C	8	8	8
Rx 1-	N/C	9	9	9
Tx 1-	N/C	11	11	11
Tx 1+	N/C	12	12	12
Sideband 0	14	14	14	14
Sideband 1	15	15	15	15
Sideband 2	16	16	16	16
Sideband 3	17	17	17	17
Sideband 4	18	18	18	18
Sideband 5	19	19	19	19
Rx 2+	N/C	N/C	21	21
Rx 2-	N/C	N/C	22	22
Tx 2-	N/C	N/C	24	24
Tx 2+	N/C	N/C	25	25
Rx 3+	N/C	N/C	N/C	27
Rx 3-	N/C	N/C	N/C	28
Tx 3-	N/C	N/C	N/C	30
Tx 3+	N/C	N/C	N/C	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			

[a] N/C = not connected

The use of the sideband signals by a controller is vendor specific. One implementation of the sideband signals by a controller is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 11 defines the pin assignments for SAS 4i plug connectors (see 5.5.3.3.2.1) and SAS 4i cable receptacle connectors (see 5.5.3.3.2.1) for backplane applications using one, two, three, or four of the physical links.

Table 11 — Backplane SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]			
	One	Two	Three	Four
Rx 3+	N/C	N/C	N/C	2
Rx 3-	N/C	N/C	N/C	3
Tx 3-	N/C	N/C	N/C	5
Tx 3+	N/C	N/C	N/C	6
Rx 2+	N/C	N/C	8	8
Rx 2-	N/C	N/C	9	9
Tx 2-	N/C	N/C	11	11
Tx 2+	N/C	N/C	12	12
Sideband 5	14	14	14	14
Sideband 4	15	15	15	15
Sideband 3	16	16	16	16
Sideband 2	17	17	17	17
Sideband 1	18	18	18	18
Sideband 0	19	19	19	19
Rx 1+	N/C	21	21	21
Rx 1-	N/C	22	22	22
Tx 1-	N/C	24	24	24
Tx 1+	N/C	25	25	25
Rx 0+	27	27	27	27
Rx 0-	28	28	28	28
Tx 0-	30	30	30	30
Tx 0+	31	31	31	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			

[a] N/C = not connected

The use of the sideband signals by a backplane is vendor specific. One implementation of the sideband signals by a backplane is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.5.3.3.3 Mini SAS 4i connectors

5.5.3.3.3.1 Mini SAS 4i cable plug connector

The Mini SAS 4i cable plug connector is the free (plug) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 34 shows the Mini SAS 4i cable plug connector.

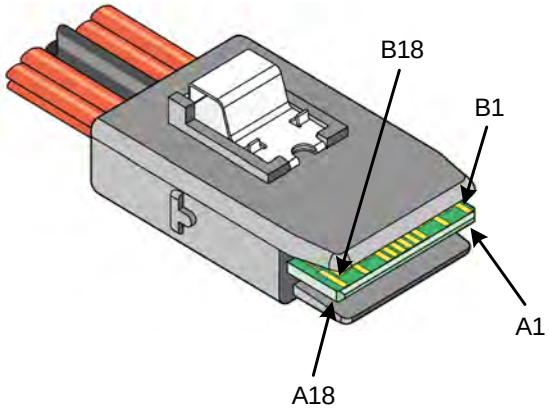

Figure 34 — Mini SAS 4i cable plug connector

Table 12 and table 13 (see 5.5.3.3.3.3) define the pin assignments for the Mini SAS 4i cable plug connector.

5.5.3.3.3.2 Mini SAS 4i receptacle connector

The Mini SAS 4i receptacle connector is the fixed (receptacle) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 35 shows the Mini SAS 4i receptacle connector.

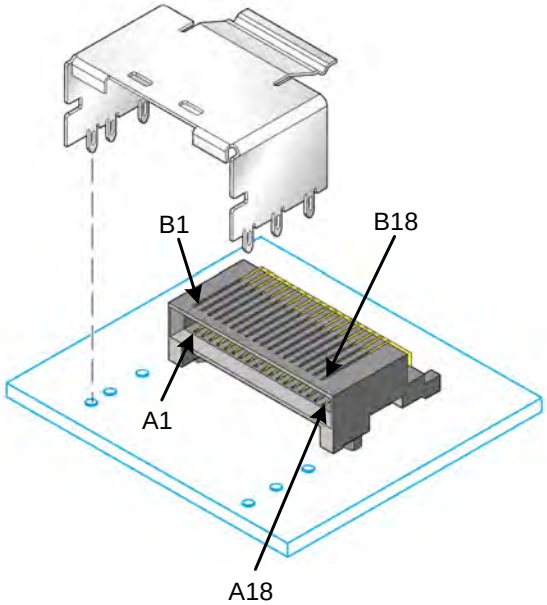

Figure 35 — Mini SAS 4i receptacle connector

Table 12 and table 13 (see 5.5.3.3.4.5) define the pin assignments for the Mini SAS 4i receptacle connector.

5.5.3.3.3.3 Mini SAS 4i connector pin assignments

Table 12 defines the pin assignments for Mini SAS 4i plug connectors (see 5.5.3.3.3.1) and Mini SAS 4i cable receptacle connectors (see 5.5.3.3.3.2) for controller applications using one, two, three, or four of the physical links.

Table 12 — Controller Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Sideband 7	A8	A8	A8	A8	First
Sideband 3	A9	A9	A9	A9	
Sideband 4	A10	A10	A10	A10	
Sideband 5	A11	A11	A11	A11	
Rx 2+	N/C	N/C	A13	A13	Third
Rx 2-	N/C	N/C	A14	A14	
Rx 3+	N/C	N/C	N/C	A16	
Rx 3-	N/C	N/C	N/C	A17	
Tx 0+	B2	B2	B2	B2	Third
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Sideband 0	B8	B8	B8	B8	First
Sideband 1	B9	B9	B9	B9	
Sideband 2	B10	B10	B10	B10	
Sideband 6	B11	B11	B11	B11	
Tx 2+	N/C	N/C	B13	B13	Third
Tx 2-	N/C	N/C	B14	B14	
Tx 3+	N/C	N/C	N/C	B16	
Tx 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 13 defines the pin assignments for Mini SAS 4i plug connectors (see 5.5.3.3.3.1) and Mini SAS 4i cable receptacle connectors (see 5.5.3.3.3.2) for backplane applications using one, two, three, or four of the physical links.

Table 13 — Backplane Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Sideband 0	A8	A8	A8	A8	First
Sideband 1	A9	A9	A9	A9	
Sideband 2	A10	A10	A10	A10	
Sideband 6	A11	A11	A11	A11	
Rx 2+	N/C	N/C	A13	A13	Third
Rx 2-	N/C	N/C	A14	A14	
Rx 3+	N/C	N/C	N/C	A16	
Rx 3-	N/C	N/C	N/C	A17	
Tx 0+	B2	B2	B2	B2	Third
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Sideband 7	B8	B8	B8	B8	First
Sideband 3	B9	B9	B9	B9	
Sideband 4	B10	B10	B10	B10	
Sideband 5	B11	B11	B11	B11	
Tx 2+	N/C	N/C	B13	B13	Third
Tx 2-	N/C	N/C	B14	B14	
Tx 3+	N/C	N/C	N/C	B16	
Tx 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.5.3.3.4 Mini SAS HD internal connectors

5.5.3.3.4.1 Mini SAS HD 4i cable plug connector

The Mini SAS HD 4i cable plug connector is the 4 lane cable (free) connector defined in SFF-8643. Figure 36 shows the Mini SAS HD 4i cable plug connector.

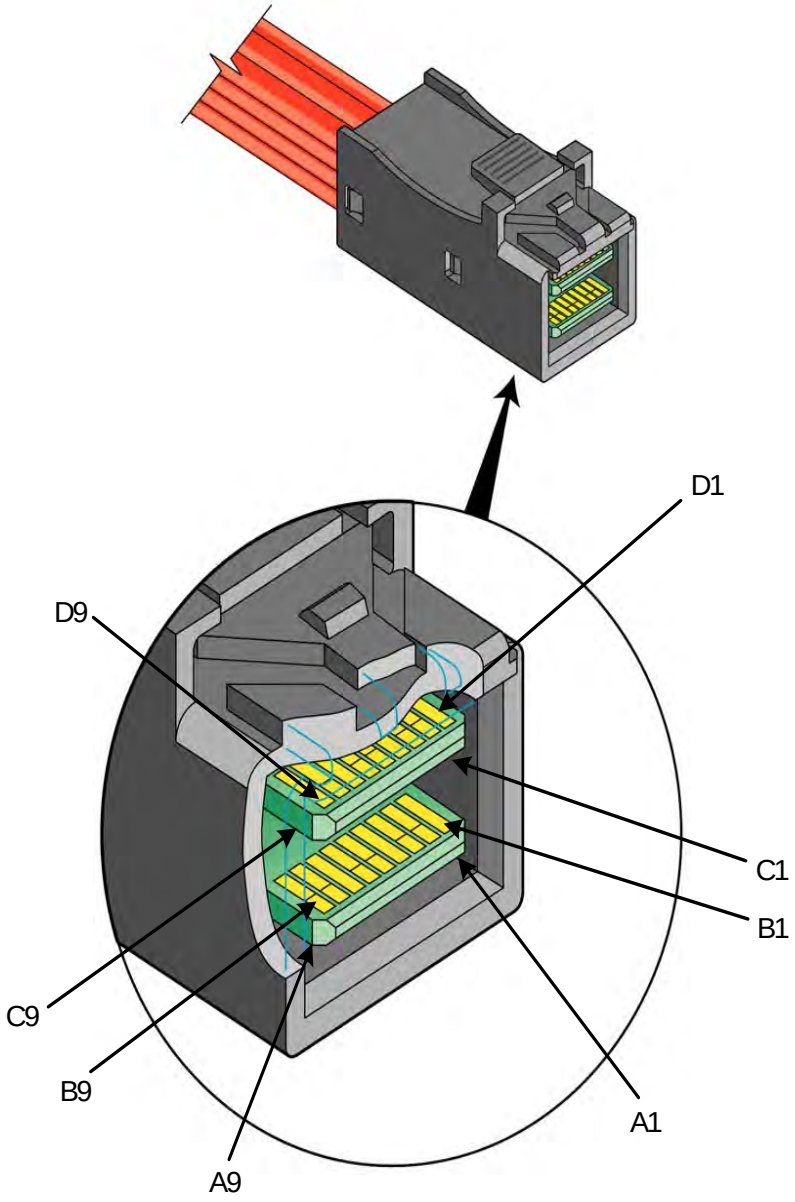

Figure 36 — Mini SAS HD 4i cable plug connector

Table 12 and table 13 (see 5.5.3.3.4.5) define the pin assignments for the Mini SAS HD 4i cable plug connector.

5.5.3.3.4.2 Mini SAS HD 8i cable plug connector

The Mini SAS HD 8i cable plug connector is the dual 4 lane cable plug (free) connector defined in SFF-8643.

Figure 37 shows the Mini SAS HD 8i cable plug connector. This connector is a modular version of repeating Mini SAS HD 4i cable plug connectors (see 5.5.3.3.4.1). Module labeling is shown in figure 37. See figure 36 (see 5.5.3.3.4.1) for pin designations.

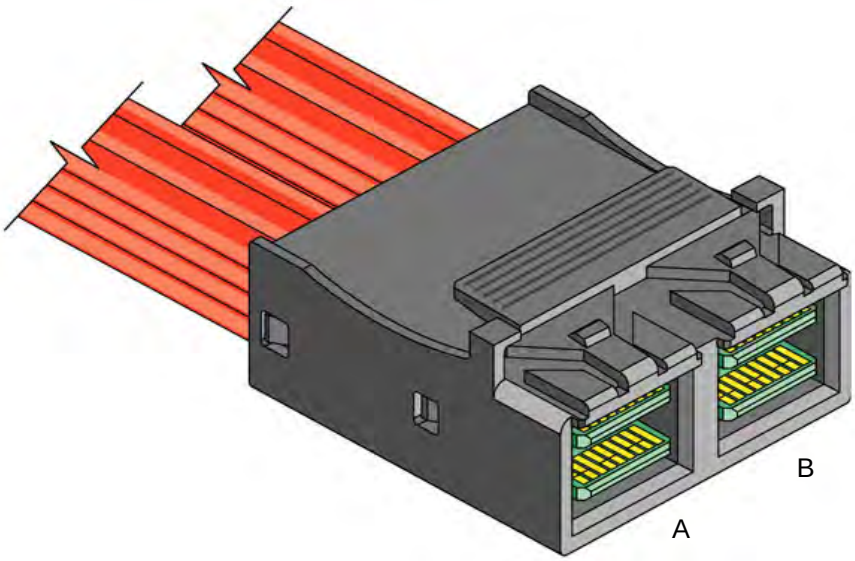

Figure 37 — Mini SAS HD 8i cable plug connector

Table 12 and table 13 (see 5.5.3.3.4.5) define the pin assignments for the Mini SAS HD 4i cable plug connector (see 5.5.3.3.4.1). The pin assignments are repeated for each module of the Mini SAS 8i cable plug connector.

5.5.3.3.4.3 Mini SAS HD 4i receptacle connector

The Mini SAS HD 4i receptacle connector is the 4 lane receptacle (fixed) connector defined in SFF-8643. Figure 38 shows the Mini SAS HD 4i receptacle connector.

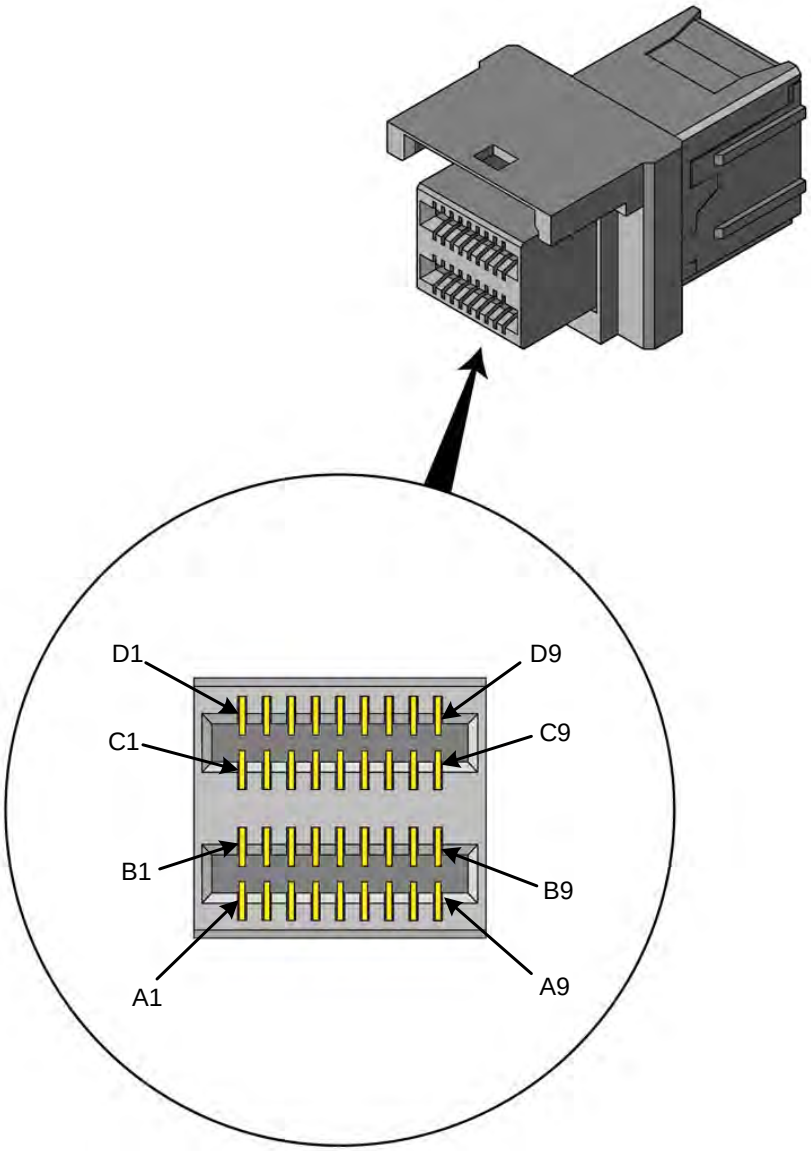

Figure 38 — Mini SAS HD 4i receptacle connector

Table 12 and table 13 (see 5.5.3.3.4.5) define the pin assignments for the Mini SAS HD 4i receptacle connector.

5.5.3.3.4.4 Mini SAS HD 8i receptacle connector

The Mini SAS HD 8i receptacle connector is a dual 4 lane receptacle (fixed) connector defined in SFF-8643. Figure 39 shows the Mini SAS HD 8i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.5.3.3.4.3). Module labeling is shown in figure 39. See figure 38 (see 5.5.3.3.4.3) for pin designations.

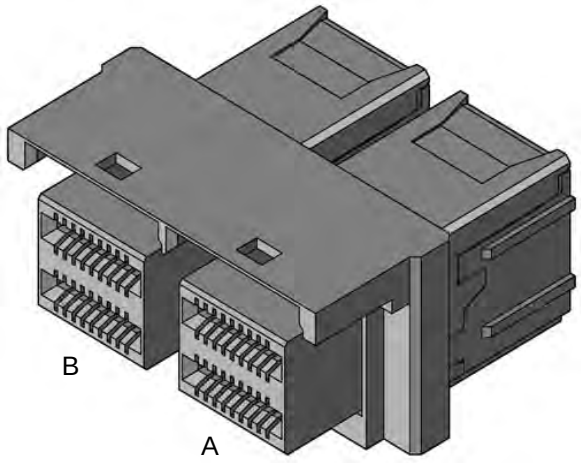

Figure 39 — Mini SAS HD 8i receptacle connector

Table 14 and table 15 (see 5.5.3.3.4.5) define the pin assignments for the Mini SAS HD 8i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.5.3.3.4.3). This connector accepts one Mini SAS HD 8i plug connector (see 5.5.3.3.4.2) or two Mini SAS HD 4i plug connectors (see 5.5.3.3.4.1).

5.5.3.3.4.5 Mini SAS HD 4i connector pin assignments

Table 14 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.5.3.3.4.1) and Mini SAS HD 4i receptacle connectors (see 5.5.3.3.4.3) for controller applications using one, two, three, or four of the physical links.

Table 14 — Controller Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	B4	B4	B4	B4	Third
Rx 0-	B5	B5	B5	B5	
Rx 1+	N/C	A4	A4	A4	
Rx 1-	N/C	A5	A5	A5	
Sideband 7	A1	A1	A1	A1	Second
Sideband 3	B1	B1	B1	B1	
Sideband 4	C1	C1	C1	C1	
Sideband 5	D1	D1	D1	D1	
Rx 2+	N/C	N/C	B7	B7	Third
Rx 2-	N/C	N/C	B8	B8	
Rx 3+	N/C	N/C	N/C	A7	
Rx 3-	N/C	N/C	N/C	A8	
Tx 0+	D4	D4	D4	D4	Third
Tx 0-	D5	D5	D5	D5	
Tx 1+	N/C	C4	C4	C4	
Tx 1-	N/C	C5	C5	C5	
Sideband 0	A2	A2	A2	A2	Second
Sideband 1	B2	B2	B2	B2	
Sideband 2	C2	C2	C2	C2	
Sideband 6	D2	D2	D2	D2	
Tx 2+	N/C	N/C	D7	D7	Third
Tx 2-	N/C	N/C	D8	D8	
Tx 3+	N/C	N/C	N/C	C7	
Tx 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 15 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.5.3.3.4.1) and Mini SAS HD 4i receptacle connectors (see 5.5.3.3.4.3) for backplane applications using one, two, three, or four of the physical links.

Table 15 — Backplane Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	B4	B4	B4	B4	Third
Rx 0-	B5	B5	B5	B5	
Rx 1+	N/C	A4	A4	A4	
Rx 1-	N/C	A5	A5	A5	
Sideband 0	A1	A1	A1	A1	Second
Sideband 1	B1	B1	B1	B1	
Sideband 2	C1	C1	C1	C1	
Sideband 6	D1	D1	D1	D1	
Rx 2+	N/C	N/C	B7	B7	Third
Rx 2-	N/C	N/C	B8	B8	
Rx 3+	N/C	N/C	N/C	A7	
Rx 3-	N/C	N/C	N/C	A8	
Tx 0+	D4	D4	D4	D4	Third
Tx 0-	D5	D5	D5	D5	
Tx 1+	N/C	C4	C4	C4	
Tx 1-	N/C	C5	C5	C5	
Sideband 7	A2	A2	A2	A2	Second
Sideband 3	B2	B2	B2	B2	
Sideband 4	C2	C2	C2	C2	
Sideband 5	D2	D2	D2	D2	
Tx 2+	N/C	N/C	D7	D7	Third
Tx 2-	N/C	N/C	D8	D8	
Tx 3+	N/C	N/C	N/C	C7	
Tx 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.5.3.4 SAS external connectors

5.5.3.4.1 Mini SAS 4x connectors

5.5.3.4.1.1 Mini SAS 4x cable plug connector

The Mini SAS 4x cable plug connector and the MiniSAS 4x active plug connector are the free (plug) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086.

Figure 40 shows the Mini SAS 4x cable plug connector.

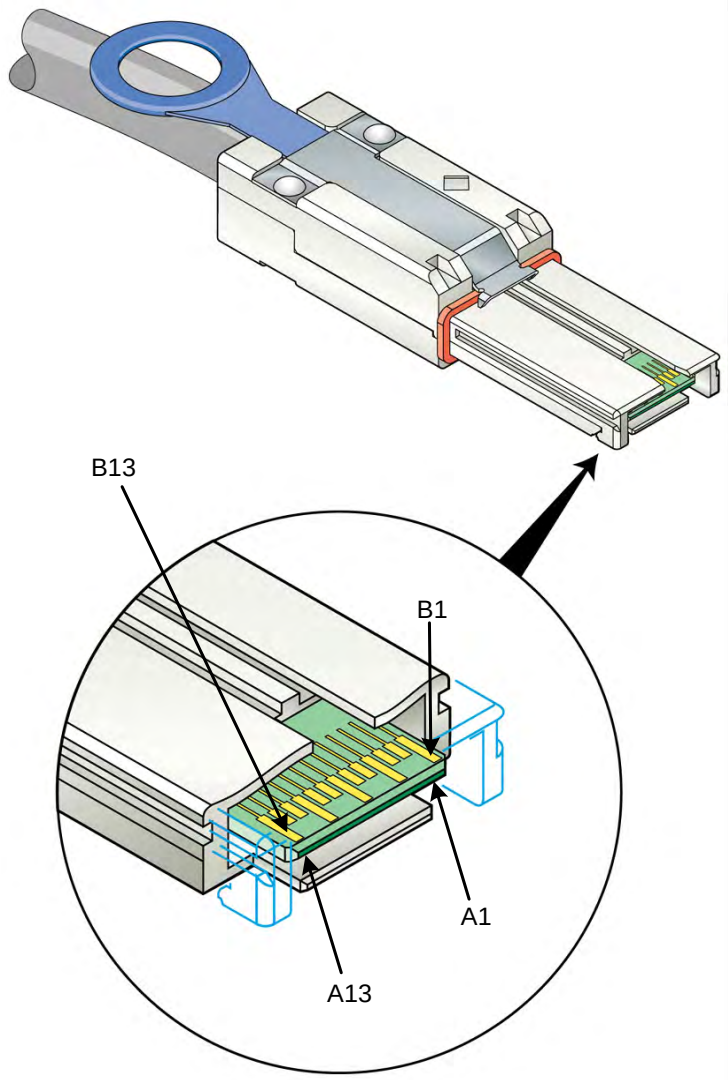

Figure 40 — Mini SAS 4x cable plug connector

If constructed with a pull tab as shown in figure 40, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 18 (see 5.5.3.4.1.3) and table 19 (see 5.5.3.4.1.3) define the pin assignments for the Mini SAS 4x cable plug connector.

Mini SAS 4x cable plug connectors shall include key slots to allow attachment to Mini SAS 4x receptacle connectors (see 5.5.3.4.1.2) with matching keys and key slots.

To ensure active cable assemblies are not intermateable with Mini SAS 4x receptacles that do not support active cable assemblies, differentiating keying shall be provided by having a blocking key on the plug connector in addition to the key slots. Table 16 defines the icons that shall be placed on or near Mini SAS 4x cable plug connectors and the key slot and key positions (see SFF-8088) that shall be used by Mini SAS 4x cable plug connectors.

Table 16 — Mini SAS 4x cable plug connector and Mini SAS 4x active cable plug connector icons, key slot positions, and key positions

End of a SAS external cable		Icon	Key slot positions	Key positions	Reference
Electrical compliance	**Attaches to**				
Untrained 1.5 Gbps and 3 Gbps [a]	Out or in [b]	Diamond and circle	2, 4, 6	none	Figure 41
	Out [c]	Diamond	2, 4	none	Figure 42
	In [d]	Circle	4, 6	none	Figure 43
Trained 1.5 Gbps, 3 Gbps, and 6 Gbps [e]	Out or in [b]	Two diamonds and two circles	2, 4, 6	3	Figure 44
	Out [c]	Two diamonds	2, 4	3	Figure 45
	In [d]	Two circles	4, 6	3	Figure 46
	Out or in [b]	Two triangles, diamond, and circle	2, 4, 6	5	Figure 47 [f]
	Out [c]	Two triangles and diamond	2, 4	5	Figure 48 [f]
	In [d]	Two triangles and circle	4, 6	5	Figure 49 [f]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbps and 3 Gbps (see 5.6.4).
[b] Attaches to an end device, an enclosure out port, an enclosure in port, or an enclosure universal port.
[c] Attaches to an end device, an enclosure out port, or an enclosure universal port.
[d] Attaches to an end device, an enclosure in port, or an enclosure universal port.
[e] Complies with the TxRx connection characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps (see 5.6.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbps and 3 Gbps (see 5.6.4).
[f] Mini SAS 4x active cable plug connector.

Figure 41 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 51, figure 54, and figure 57 in 5.5.3.4.1.2), an enclosure out port (see figure 52, figure 55, and figure 58 in 5.5.3.4.1.2), or an enclosure in port (see figure 53, figure 56, and figure 59 in 5.5.3.4.1.2).

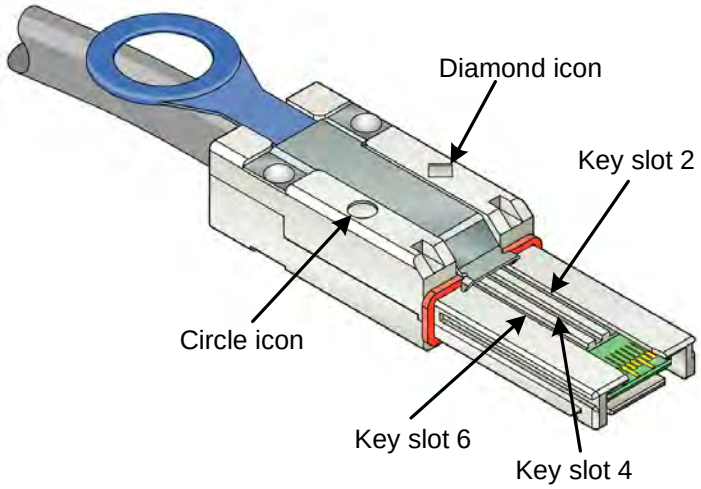

Figure 41 — Mini SAS 4x cable plug connector for untrained 1.5 Gbps and 3 Gbps that attaches to an enclosure out port or an enclosure in port

Figure 42 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 51, figure 54, and figure 57 in 5.5.3.4.1.2) or an enclosure out port (see figure 52, figure 55, and figure 58 in 5.5.3.4.1.2).

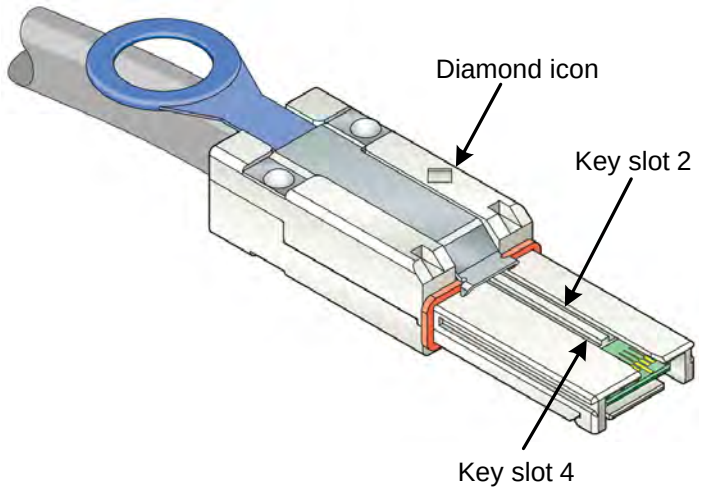

Figure 42 — Mini SAS 4x cable plug connector for untrained 1.5 Gbps and 3 Gbps that attaches to an enclosure out port

Figure 43 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 51, figure 54, and figure 57 in 5.5.3.4.1.2) or an enclosure in port (see figure 53, figure 56, and figure 59 in 5.5.3.4.1.2).

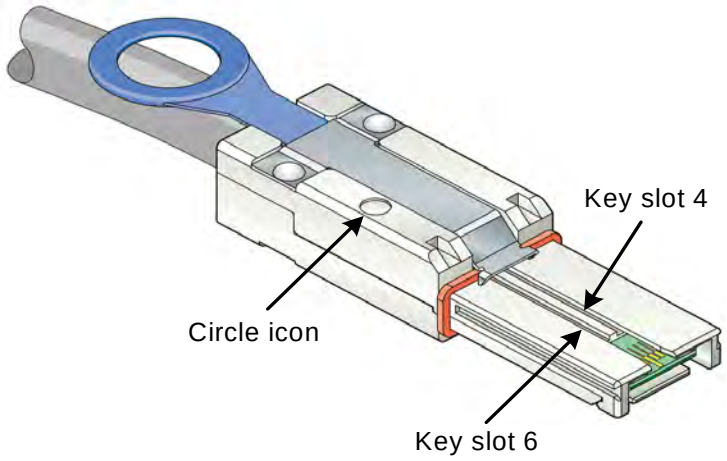

Figure 43 — Mini SAS 4x cable plug connector for untrained 1.5 Gbps and 3 Gbps that attaches to an enclosure in port

Figure 44 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 54 and figure 57 in 5.5.3.4.1.2), an enclosure out port (see figure 55 and figure 58 in 5.5.3.4.1.2), or an enclosure in port (figure 56 and figure 59 in 5.5.3.4.1.2).

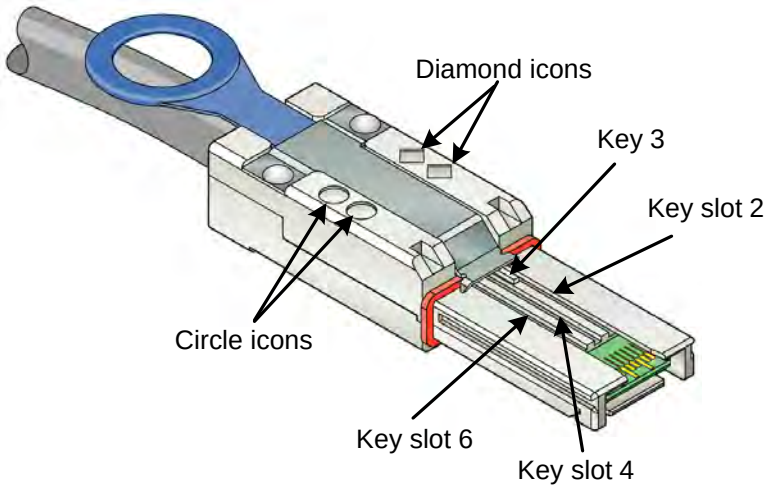

Figure 44 — Mini SAS 4x cable plug connector for trained 1.5 Gbps and 3 Gbps that attaches to an enclosure out port or an enclosure in port

Figure 45 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbps, 3 Gbps, and 6 Gbps that attaches to an end device or an enclosure universal port (see figure 54 and figure 57 in 5.5.3.4.1.2) or an enclosure out port (see figure 55 and figure 58 in 5.5.3.4.1.2).

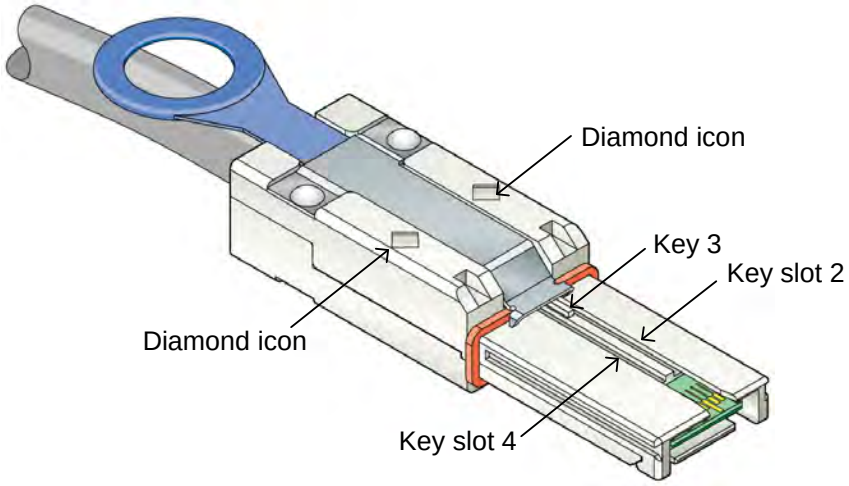

Figure 45 — Mini SAS 4x cable plug connector for trained 1.5 Gbps, 3 Gbps, and 6 Gbps that attaches to an enclosure out port

Figure 46 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbps, 3 Gbps, and 6 Gbps that attaches to an end device or an enclosure universal port ((see figure 54 and figure 57 in 5.5.3.4.1.2) or an enclosure in port (see figure 56 and figure 59 in 5.5.3.4.1.2).

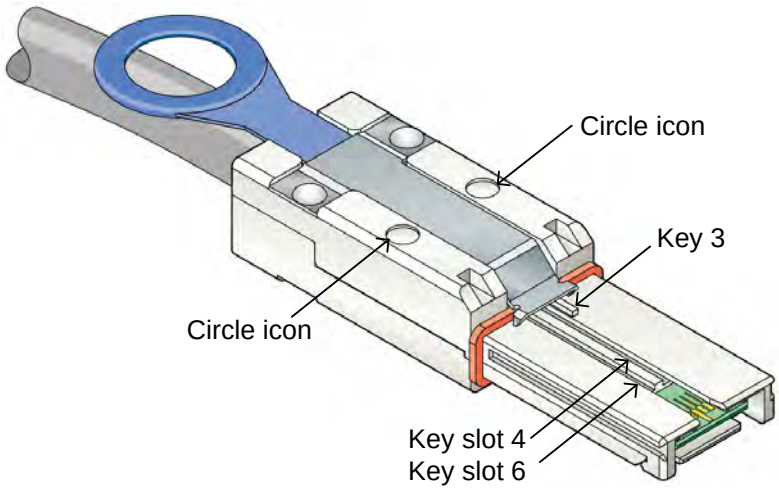

Figure 46 — Mini SAS 4x cable plug connector for trained 1.5 Gbps, 3 Gbps, and 6 Gbps that attaches to an enclosure in port

Figure 47 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 57 in 5.5.3.4.1.2), an enclosure out port (see figure 58 in 5.5.3.4.1.2), or an enclosure in port (see figure 59 in 5.5.3.4.1.2).

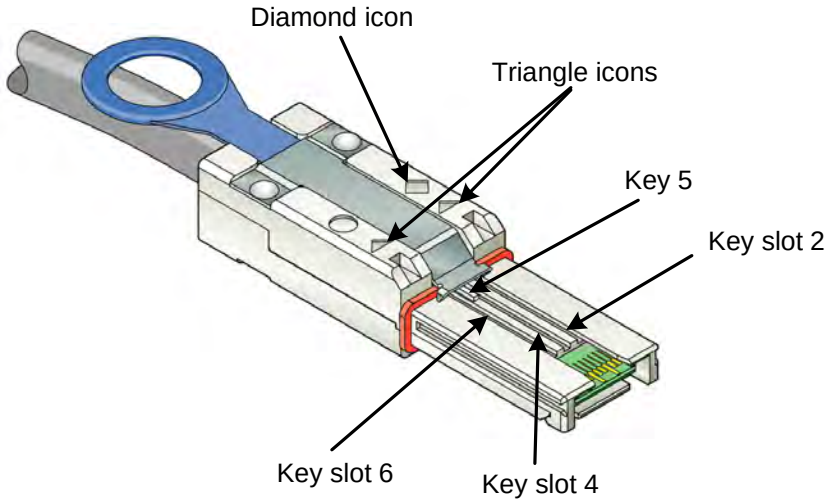

Figure 47 — Mini SAS 4x active cable plug connector that attaches to an enclosure out port or an enclosure in port

Figure 48 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 57 in 5.5.3.4.1.2) or enclosure out port (see figure 58 in 5.5.3.4.1.2).

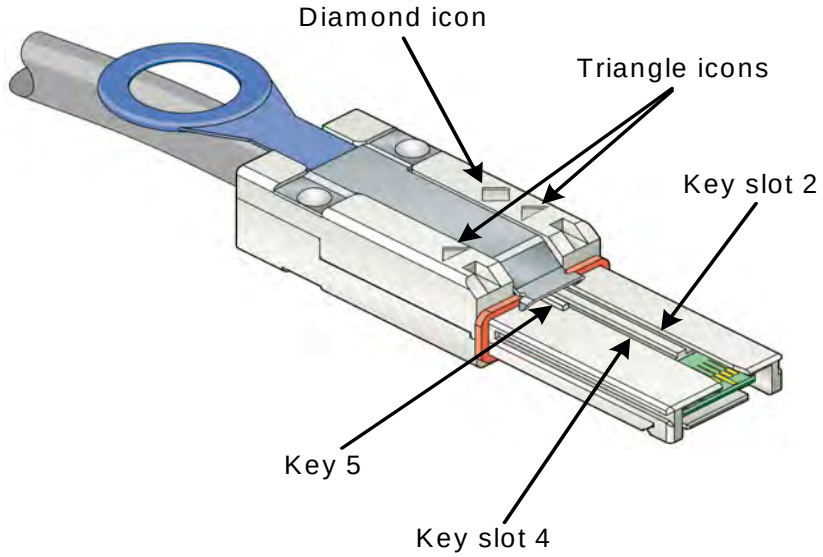

Figure 48 — Mini SAS 4x active cable plug connector that attaches to an enclosure out port

Figure 49 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbps and 3 Gbps that attaches to an end device or an enclosure universal port (see figure 57 in 5.5.3.4.1.2) or an enclosure in port (see figure 59 in 5.5.3.4.1.2).

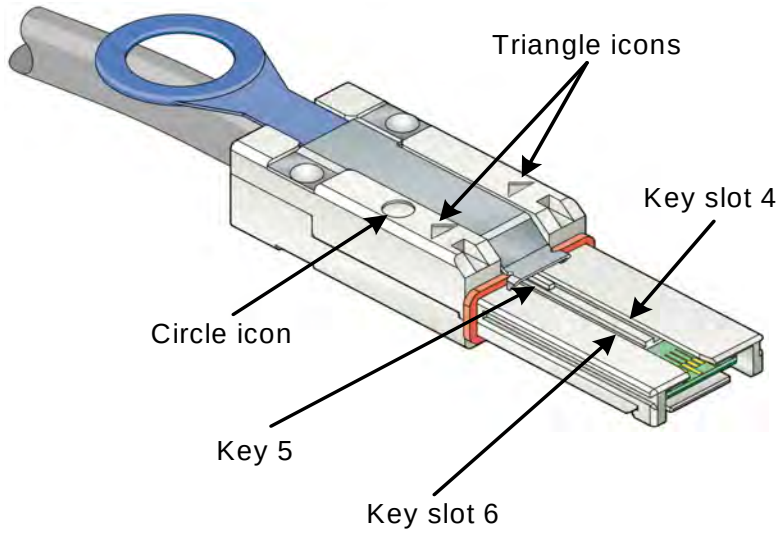

Figure 49 — Mini SAS 4x active cable plug connector that attaches to an enclosure in port

5.5.3.4.1.2 Mini SAS 4x receptacle connector

The Mini SAS 4x receptacle connector is the fixed (receptacle) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086.

A Mini SAS 4x receptacle connector may be used by one or more SAS devices (e.g., one SAS device using physical links 0 and 3, another using physical link 1, and a third using physical link 2).

A Mini SAS 4x receptacle connector shall be used by no more than one expander device at a time, and all physical links shall be used by the same expander port (i.e., all the expander phys shall have the same routing attribute (e.g., subtractive or table) (see SPL-2)).

Figure 50 shows the Mini SAS 4x receptacle connector.

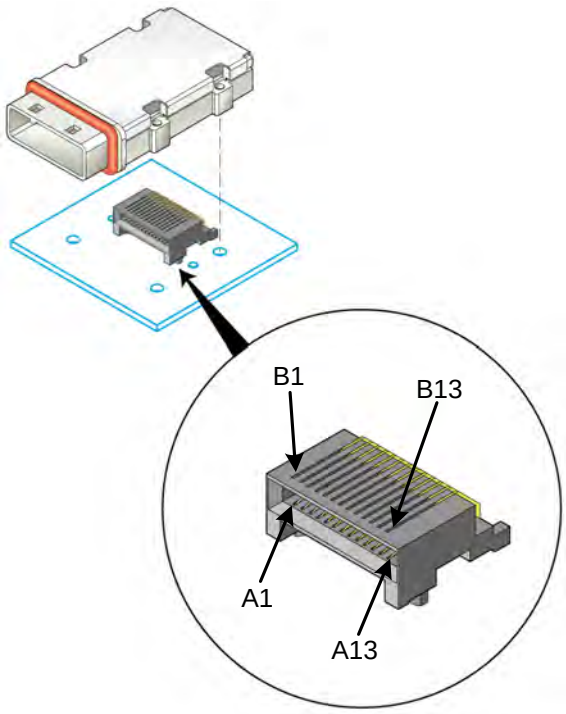

Figure 50 — Mini SAS 4x receptacle connector

Table 18 (see 5.5.3.4.1.3) and table 19 (see 5.5.3.4.1.3) define the pin assignments for the Mini SAS 4x receptacle connector.

Mini SAS 4x receptacle connectors and Mini SAS 4x active receptacle connectors shall include keys and key slots to prevent attachment to Mini SAS 4x cable plug connectors (see 5.5.3.4.1.1) without matching keys and key slots.

Table 17 defines the icons that shall be placed on or near Mini SAS 4x receptacle connectors and the key and key slot positions (see SFF-8088) that shall be used by Mini SAS 4x receptacle connectors.

Table 17 — Mini SAS 4x receptacle connector icons, key positions, and key slot positions

Electrical compliance	Use	Icons	Key position	Key slot position	Reference
Untrained 1.5 Gbps and 3 Gbps [a]	End device or enclosure universal port	Diamond and circle	4	none	Figure 51
	Enclosure out port	Diamond	2	none	Figure 52
	Enclosure in port	Circle	6	none	Figure 53
Trained 1.5 Gbps, 3 Gbps, and 6 Gbps [b]	End device or enclosure universal port	Two diamonds and two circles	4	3	Figure 54
	Enclosure out port	Two diamonds	2	3	Figure 55
	Enclosure in port	Two circles	6	3	Figure 56
	End device or enclosure universal port	Two triangles, diamond, and circle	4	3, 5	Figure 57 [c]
	Enclosure out port	Two triangles and diamond	2	3, 5	Figure 58 [c]
	Enclosure in port	Two triangles and circle	6	3, 5	Figure 59 [c]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbps and 3 Gbps (see 5.6.4).
[b] Complies with the TxRx connection characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps (see 5.6.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbps and 3 Gbps (see 5.6.4).
[c] Mini SAS 4x active receptacle.

Figure 51 shows the key on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports untrained 1.5 Gbps and 3 Gbps. The Mini SAS 4x cable plug connectors shown in figure 41, figure 42, and figure 43 (see 5.5.3.4.1.1) may be attached to this connector.

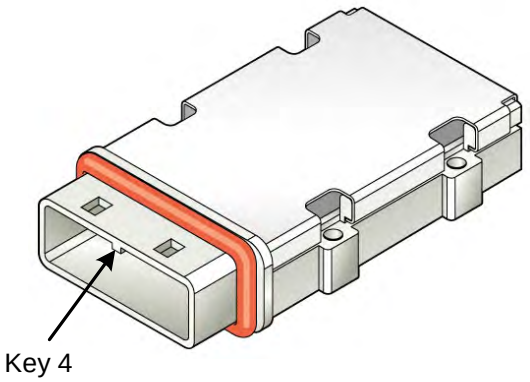

Figure 51 — Mini SAS 4x receptacle connector - end device or enclosure universal port for untrained 1.5 Gbps and 3 Gbps

Figure 52 shows the key on a Mini SAS 4x receptacle connector used by an enclosure out port that supports untrained 1.5 Gbps and 3 Gbps. The Mini SAS 4x cable plug connectors shown in figure 41 and figure 42 (see 5.5.3.4.1.1) may be attached to this connector.

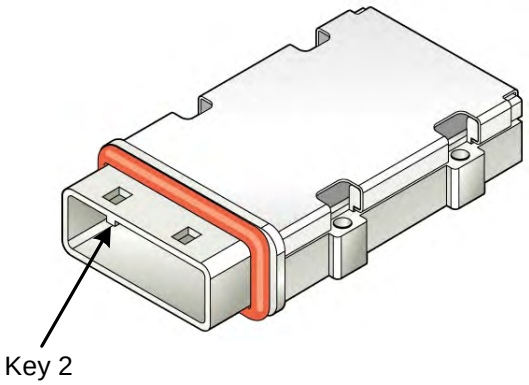

Figure 52 — Mini SAS 4x receptacle connector - enclosure out port for untrained 1.5 Gbps and 3 Gbps

Figure 53 shows the key on a Mini SAS 4x receptacle connector used by an enclosure in port that supports untrained 1.5 Gbps and 3 Gbps. The Mini SAS 4x cable plug connectors shown in figure 41 and figure 43 (see 5.5.3.4.1.1) may be attached to this connector.

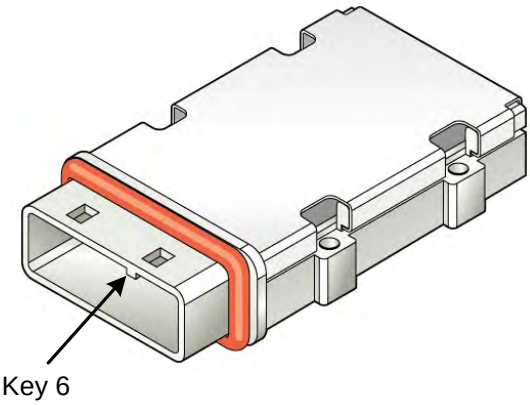

Figure 53 — Mini SAS 4x receptacle connector - enclosure in port for untrained 1.5 Gbps and 3 Gbps

Figure 54 shows the key and key slot on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 42, figure 43, figure 44, figure 45, and figure 46 (see 5.5.3.4.1.1) may be attached to this connector.

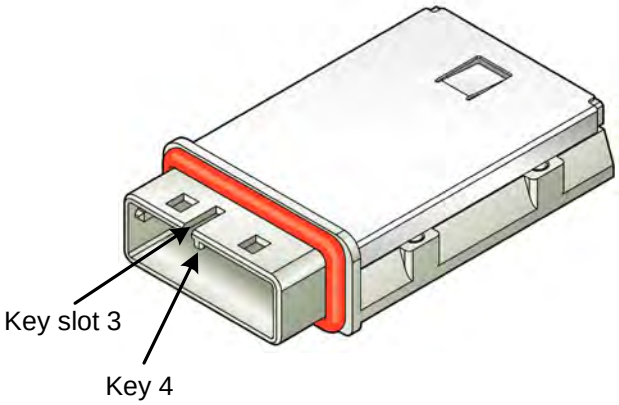

Figure 54 — Mini SAS 4x receptacle connector - end device or enclosure universal port for trained 1.5 Gbps, 3 Gbps, and 6 Gbps and for untrained 1.5 Gbps and 3 Gbps

Figure 55 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 42, figure 44, and figure 45, (see 5.5.3.4.1.1) may be attached to this connector.

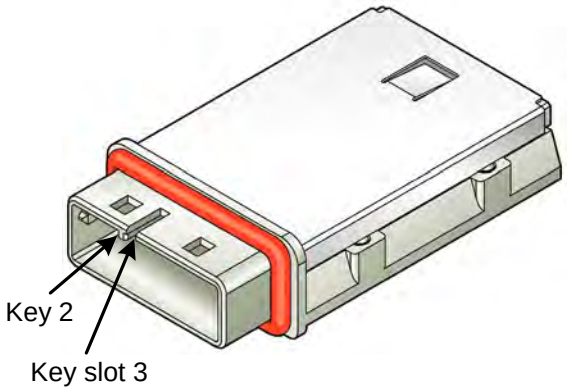

Figure 55 — Mini SAS 4x receptacle connector - enclosure out port for trained 1.5 Gbps, 3 Gbps, and 6 Gbps and for untrained 1.5 Gbps and 3 Gbps

Figure 56 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 43, figure 44, and figure 46 (see 5.5.3.4.1.1) may be attached to this connector.

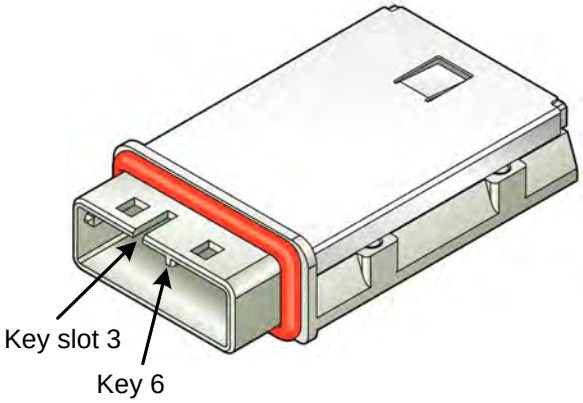

Figure 56 — Mini SAS 4x receptacle connector - enclosure in port for trained 1.5 Gbps, 3 Gbps, and 6 Gbps and for untrained 1.5 Gbps and 3 Gbps

Figure 57 shows an Mini SAS 4x active receptacle connector used by end devices or an enclosure universal port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 42, figure 43, figure 44, figure 45, figure 46, figure 47, figure 48, and figure 49 (see 5.5.3.4.1.1) may be attached to this connector.

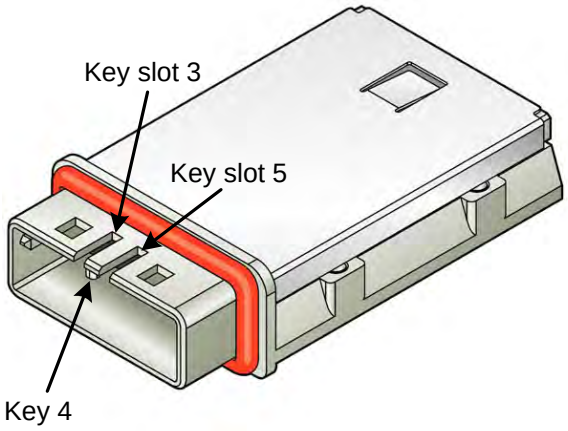

Figure 57 — Mini SAS 4x active receptacle connector - end device or enclosure universal port

Figure 58 shows an Mini SAS 4x active receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 42, figure 44, figure 45, figure 47, and figure 48 (see 5.5.3.4.1.1) may be attached to this connector.

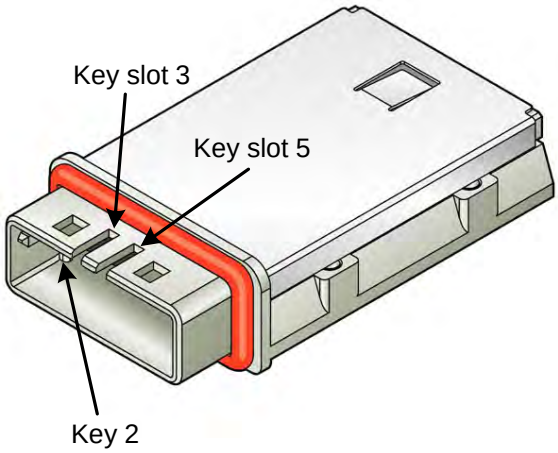

Figure 58 — Mini SAS 4x active receptacle connector - enclosure out port

Figure 59 shows an Mini SAS 4x active receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbps, 3 Gbps, and 6 Gbps; and
b) untrained 1.5 Gbps and 3 Gbps.

The Mini SAS 4x cable plug connectors shown in figure 41, figure 43, figure 44, figure 46, figure 47, and figure 49 (see 5.5.3.4.1.1) may be attached to this connector.

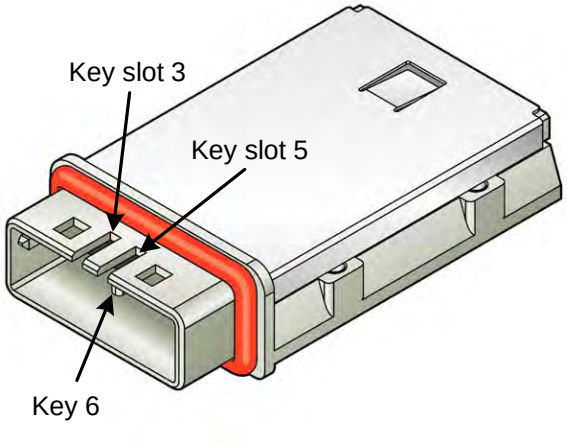

Figure 59 — Mini SAS 4x active receptacle connector - enclosure in port

5.5.3.4.1.3 Mini SAS 4x connector pin assignments

Table 18 defines the pin assignments for Mini SAS 4x cable plug connectors (see 5.5.3.4.1.1) and Mini SAS 4x receptacle connectors (see 5.5.3.4.1.2) for applications using one, two, three, or four of the physical links.

Table 18 — Mini SAS 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Rx 2+	N/C	N/C	A8	A8	
Rx 2-	N/C	N/C	A9	A9	
Rx 3+	N/C	N/C	N/C	A11	
Rx 3-	N/C	N/C	N/C	A12	
Tx 0+	B2	B2	B2	B2	
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Tx 2+	N/C	N/C	B8	B8	
Tx 2-	N/C	N/C	B9	B9	
Tx 3+	N/C	N/C	N/C	B11	
Tx 3-	N/C	N/C	N/C	B12	
SIGNAL GROUND	A1, A4, A7, A10, A13 B1, B4, B7, B10, B13				First
CHASSIS GROUND	Housing				N/A

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.5.3.4.1.4 Mini SAS 4x active connector pin assignments

Table 19 defines the pin assignments for Mini SAS 4x active cable plug connectors (see 5.5.3.4.1.1) and Mini SAS 4x active receptacle connectors (see 5.5.3.4.1.2) for implementations using one, two, three, or four of the physical links.

Table 19 — Mini SAS 4x active connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Rx 2+	N/C	N/C	A8	A8	
Rx 2-	N/C	N/C	A9	A9	
Rx 3+	N/C	N/C	N/C	A11	
Rx 3-	N/C	N/C	N/C	A12	
Tx 0+	B2	B2	B2	B2	
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Tx 2+	N/C	N/C	B8	B8	
Tx 2-	N/C	N/C	B9	B9	
Tx 3+	N/C	N/C	N/C	B11	
Tx 3-	N/C	N/C	N/C	B12	
SENSE [c]	B1				
V_{CC} [d]	B13				
SIGNAL GROUND	A1, A4, A7, A10, A13, B4, B7, B10				First
CHASSIS GROUND	Housing				

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).
[c] Electrical characteristics are definied in 5.5.3.4.1.5.
[d] Electrical characteristics are definied in 5.5.3.4.1.5.

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.5.3.4.1.5 Mini SAS 4x active cable power requirements

Mini SAS 4x active cable assemblies may contain integrated circuitry (e.g., drivers, repeaters, or equalizers). To enable the operation of circuitry inside the Mini SAS 4x active cable assemblies, Mini SAS 4x active receptacle connectors provide power when connected to a Mini SAS 4x active cable assembly (see 5.5.4.2.2). Mini SAS 4x active receptacle connectors shall be intermateable with Mini SAS 4x passive cable assemblies. To be intermateable, Mini SAS 4x active receptacle connectors define a pin (i.e., SENSE (see table 19) (see 5.5.3.4.1.4)) to allow control of power. Power shall only be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x active cable assembly is present. Power shall not be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x passive cable assembly or no cable assembly is present. An example of a power supply logic circuitry design is shown in Annex G.

The voltage and current requirements for the power supplied to the Mini SAS 4x active cable receptacle enable support for Mini SAS 4x active cable assemblies with power consumption of up to 1 W per each end of the cable assembly. These requirements are defined in table 20.

Table 20 — Mini SAS 4x active cable supplied power requirements

Characteristic	Units	Minimum	Nominal	Maximum
Supply voltage	V	3.135 [a]	3.3	3.465 [b]
Supply current	mA			319.4 [c]
Current consumption	mA			288.6 [d]
Power consumption	mW			1 000 [d e]

[a] At the maximum supply current
[b] The power supply shall not exceed this value at any current.
[c] The power supply shall deliver this amount of current at the minimum voltage of 3.135 V.
[d] Maximum consumption for each end of the active cable assembly at the maximum voltage of 3.465 V.
[e] This is a derived quantity obtained from: (maximum supply voltage) x (maximum current consumption).

The Mini SAS 4x active cable assembly shall provide a connection of the SENSE pin to ground through a 5 kohm (±5 %) resistor.

The active cable power circuitry shall enable power to the Mini SAS 4x receptacle connector only when the presence of the sense resistor is detected and power shall be disabled if the SENSE pin is open (i.e., no Mini SAS 4x cable assembly plugged in) or shorted to ground (i.e., Mini SAS 4x passive cable plugged in).

The active cable power circuitry shall have protection against the connection of the V_{CC} pin to ground or excessive current loading.

To support hot plugging, the active cable power circuitry shall be able to detect the sense resistor and provide full current within 50 ms of active cable assembly connection.

The active cable assembly and Mini SAS active cable receptacle power pins (i.e., the V_{CC} pin and SENSE pin) shall be coupled to ground via bypass capacitors so that they possess low impedance to ground from 100 MHz to 1.5 times the fundamental frequency of the maximum baud rate supported by the attached transmitter device and the attached receiver device.

The power planes of the printed circuit board on the receptacle side shall be coupled to ground.

In implementations where the circuitry in the Mini SAS 4x active cable assembly requires voltages other than the provided 3.3 V, voltage regulators may be located within the Mini SAS 4x active cable assembly.

5.5.3.4.2 Mini SAS HD external connectors

5.5.3.4.2.1 Mini SAS HD 4x cable plug connector

The Mini SAS HD 4x cable plug connector is the free (plug) 36-circuit connector defined in SFF-8644.

Figure 60 shows the Mini SAS HD 4x cable plug connector.

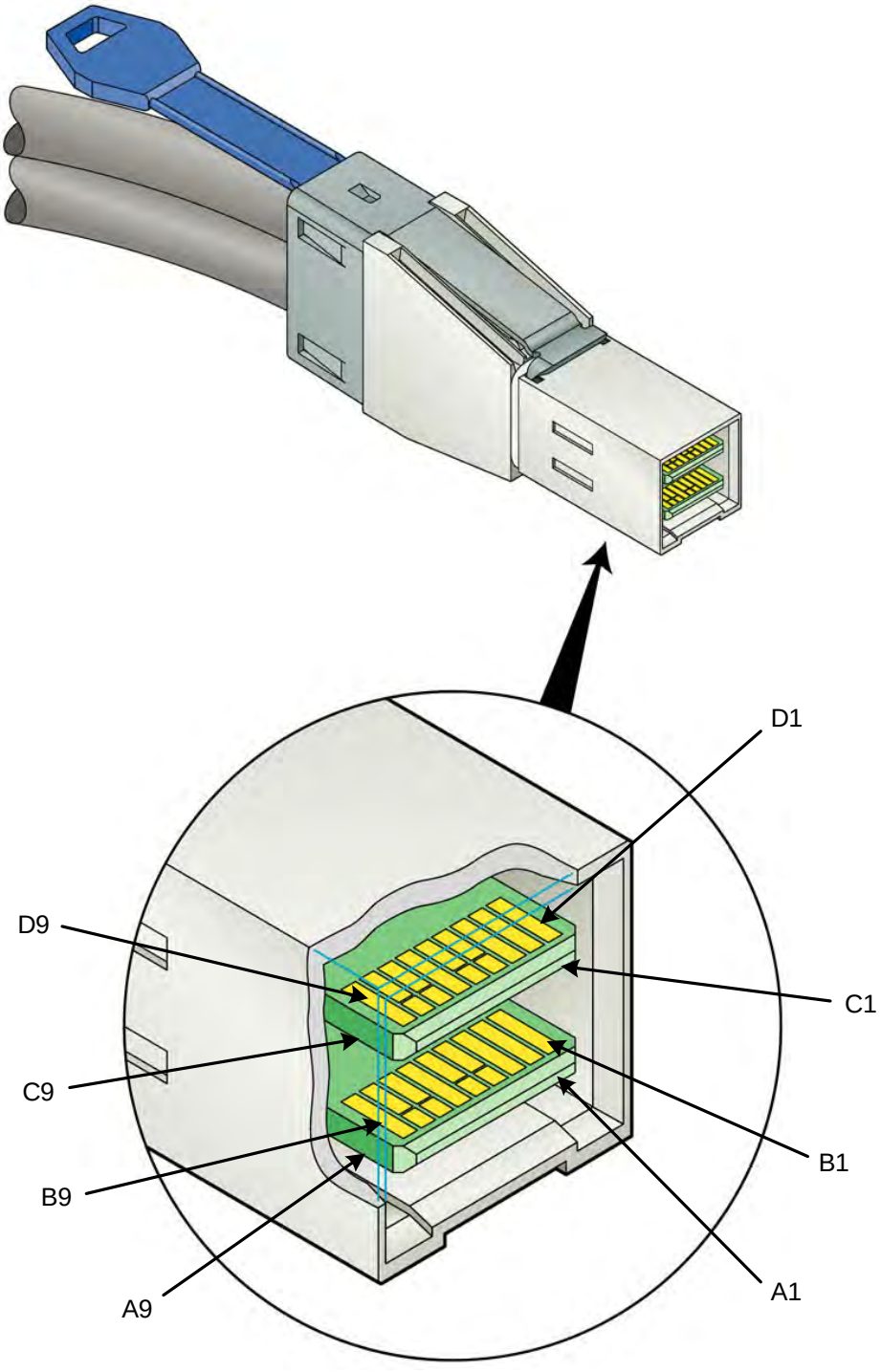

Figure 60 — Mini SAS HD 4x cable plug connector

If constructed with a pull tab as shown in figure 60, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 21 (see 5.5.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector.

The Mini SAS HD 4x cable plug connectors shall not include keying.

5.5.3.4.2.2 Mini SAS HD 8x cable plug connector

The Mini SAS HD 8i cable plug connector is the dual 4 lane cable plug (free) connector defined in SFF-8644. Figure 61 shows the Mini SAS HD 8x cable plug connector. This connector is a modular version of repeating Mini SAS HD 4x cable plug connectors (see 5.5.3.4.2.1). Module labeling is shown in figure 61. See figure 60 (see 5.5.3.4.2.1) for pin designations. Mini SAS HD 8x cable plug connectors shall not include keying.

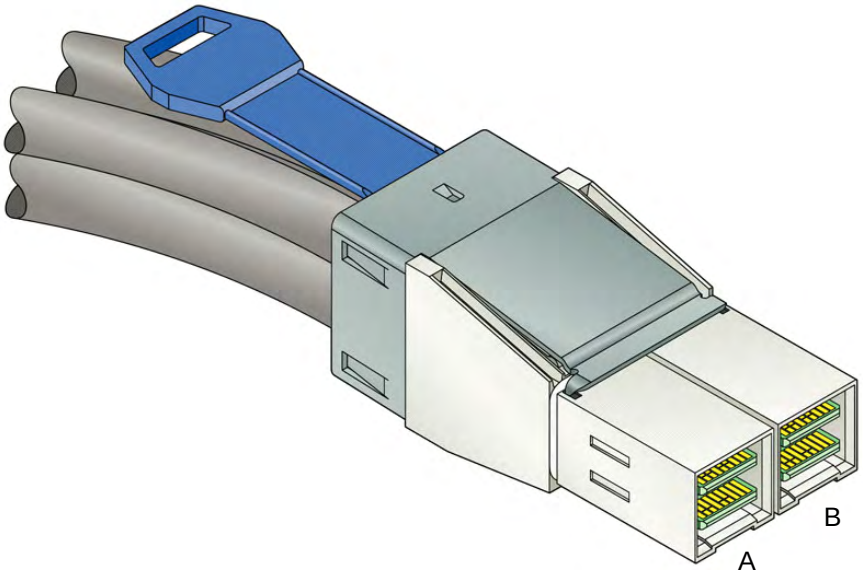

Figure 61 — Mini SAS HD 8x cable plug connector

Table 21 (see 5.5.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector (see 5.5.3.4.2.1). The pin assignments are repeated for each module of the Mini SAS 8x cable plug connector.

5.5.3.4.2.3 Mini SAS HD 4x receptacle connector

The Mini SAS HD 4x receptacle connector is the 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 62 shows the Mini SAS HD 4x receptacle connector.

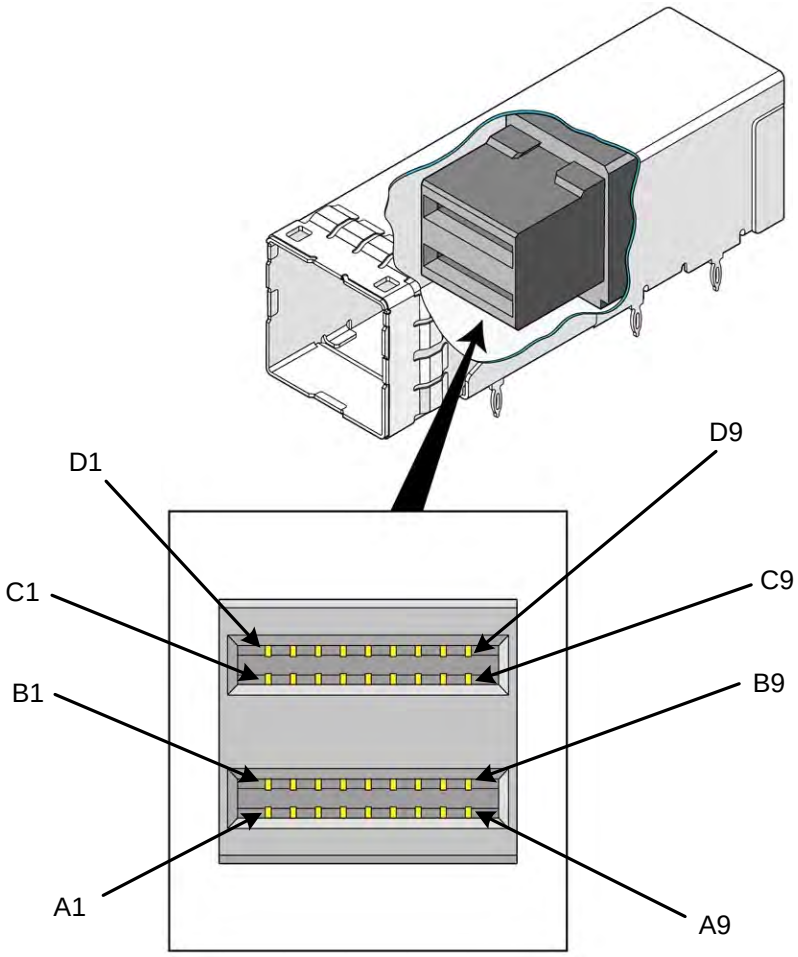

Figure 62 — Mini SAS HD 4x receptacle connector

Table 21 (see 5.5.3.4.2.6) defines the pin assignments for the Mini SAS HD 4x receptacle connector.

5.5.3.4.2.4 Mini SAS HD 8x receptacle connector

The Mini SAS HD 8x receptacle connector is a dual 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 63 shows the Mini SAS HD 8x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.5.3.4.2.3). Module labeling is shown in figure 63. See figure 62 (see 5.5.3.4.2.3) for pin designations.

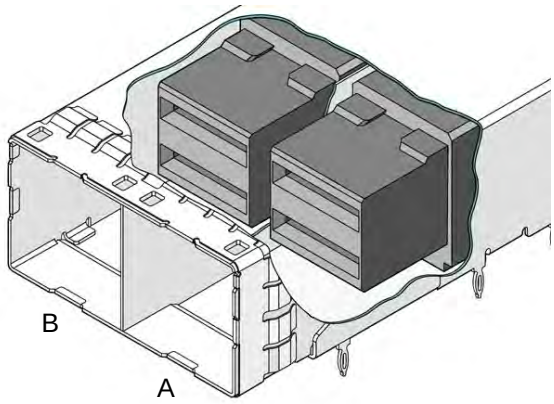

Figure 63 — Mini SAS HD 8x receptacle connector

Table 21 (see 5.5.3.4.2.6) defines the pin assignments for the Mini SAS HD 8x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.5.3.4.2.3). The Mini SAS HD 8x receptacle connector accepts one Mini SAS HD 8x plug connector (see 5.5.3.4.2.2) or one or two Mini SAS HD 4x plug connectors (see 5.5.3.4.2.1).

5.5.3.4.2.5 Mini SAS HD 16x receptacle connector

The Mini SAS HD 16x receptacle connector is a quad 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 64 shows the Mini SAS HD 16x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.5.3.4.2.3). Module labeling is shown in figure 64. See figure 62 (see 5.5.3.4.2.3) for pin designations.

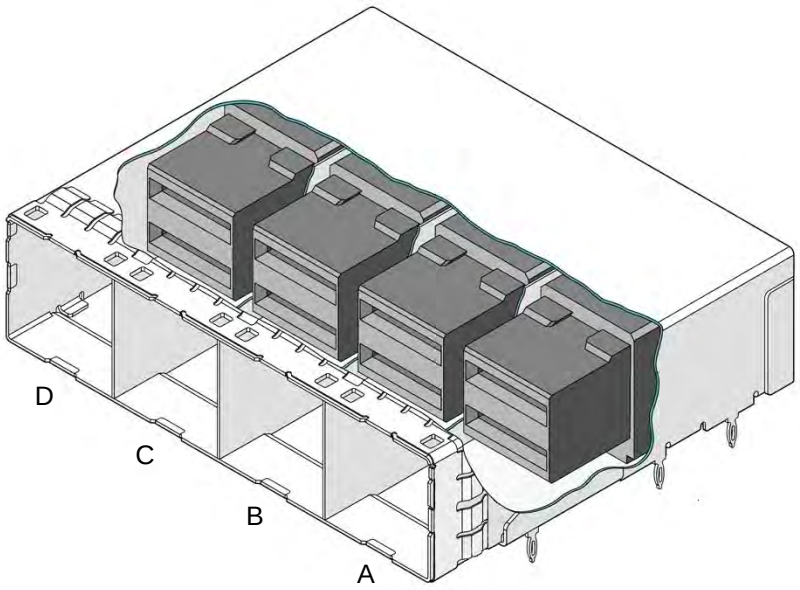

Figure 64 — Mini SAS HD 16x receptacle connector

Table 21 (see 5.5.3.4.2.6) defines the pin assignments for the Mini SAS HD 16x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.5.3.4.2.3). The Mini SAS HD 16x receptacle connector accepts:

a) one or two Mini SAS HD 8x cable plug connectors (see 5.5.3.4.2.2);
b) one, two, three, to four Mini SAS HD 4x cable plug connectors (see 5.5.3.4.2.1); or
c) a combination of one Mini SAS HD 8x cable plug connector (see 5.5.3.4.2.2) and one or two Mini SAS HD 4x cable plug connectors (see 5.5.3.4.2.1).

A Mini SAS HD 4x cable plug connector (see 5.5.3.4.2.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8x cable plug connectors (see 5.5.3.4.2.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.5.3.4.2.6 Mini SAS HD 4x connector pin assignments

Table 21 defines the pin assignments for Mini SAS HD 4x cable plug connectors (see 5.5.3.4.2.1) and Mini SAS HD 4x receptacle connectors (see 5.5.3.4.2.3) for controller applications using one, two, three, or four of the physical links.

Table 21 — Mini SAS HD 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0-	B5	B5	B5	B5	Third
Rx 0+	B4	B4	B4	B4	
Rx 1-	N/C	A5	A5	A5	
Rx 1+	N/C	A4	A4	A4	
IntL [c]	A2	A2	A2	A2	Second
Reserved [c]	A1	A1	A1	A1	
ModPrsL [c]	B2	B2	B2	B2	
Vact [c]	B1	B1	B1	B1	
Rx 2-	N/C	N/C	B8	B8	Third
Rx 2+	N/C	N/C	B7	B7	
Rx 3-	N/C	N/C	N/C	A8	
Rx 3+	N/C	N/C	N/C	A7	
Tx 0-	D5	D5	D5	D5	Third
Tx 0+	D4	D4	D4	D4	
Tx 1-	N/C	C5	C5	C5	
Tx 1+	N/C	C4	C4	C4	
SDA [c]	C2	C2	C2	C2	Second
SCL [c]	C1	C1	C1	C1	
Vman [c]	D2	D2	D2	D2	
Vact [c]	D1	D1	D1	D1	
Tx 2-	N/C	N/C	D8	D8	Third
Tx 2+	N/C	N/C	D7	D7	
Tx 3-	N/C	N/C	N/C	C8	
Tx 3+	N/C	N/C	N/C	C7	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8644).
[c] Table 22 (see 5.5.3.4.2.7) defines the connection requirements of this signal.

5.5.3.4.2.7 Mini SAS HD external connector management interface

Each 4x module shall include a 2-wire serial management interface to:

a) monitor circuitry residing in the cable assembly;
b) control circuitry residing in the cable assembly; and
c) obtain physical characteristics of the cable encoded in a non-volatile storage device located in the cable assembly.

Table 22 defines the connection requirements of the management interface signals. Mini SAS HD 4x receptacle connectors (see 5.5.3.4.2.3), Mini SAS HD 8x receptacle connectors (see 5.5.3.4.2.4), Mini SAS HD 16x receptacle connectors (see 5.5.3.4.2.5), Mini SAS HD 4x cable plug connectors (see 5.5.3.4.2.1), and Mini SAS HD 8x cable plug connectors (see 5.5.3.4.2.2) shall support the signals in table 22 in each 4x module. See SFF-8449 for a complete signal definition, management interface memory map, and timing diagrams for the two-wire interface.

Table 22 — Management interface connection requirements

Signal	Connection requirements [a]
IntL	Active Low Module Interrupt: The cable assembly shall assert this pin to indicate an interrupt bit has been set to one in the management interface memory map. This pin shall be connected to Vman on the receptacle side of the management interface. The source of the interrupt may be identified using the 2-wire serial management interface. If a cable assembly does not support interrupts, then all interrupt bits in the cable management interface memory map shall be set to zero and the cable assembly shall negate this pin (e.g., all interrupt bits of a passive cable assembly may be programmed to a clear state and the IntL pin not connected on the cable plug side of the management interface).
ModPrsL	Active Low Module Present: On the cable plug side of the management interface, ModPrsL shall be connected directly to the signal ground pins specified in table 21 (see 5.5.3.4.2.6). ModPrsL shall be connected to Vman on the receptacle side of the management interface to negate this signal when the plug is not fully mated to the receptacle.
Reserved	This pin shall be not connected on the receptacle side and cable plug side of the management interface.
SCL	Two-wire interface clock: The receptacle side of the management interface shall connect this signal to Vman.
SDA	Two-wire interface data: The receptacle side of the management interface shall connect this signal to Vman.
Vact	Active cable power: If the receptacle side of the management interface supports active cable assemblies, then it shall provide all non-management interface power to the cable assembly on the Vact pins. To support equal loading, both Vact pins shall be connected together on the receptacle side of the management interface. If the receptacle side of the management interface does not support active cable assemblies, then the Vact pins should be not connected.
Vman	Management interface power: The receptacle side of the management interface shall provide power on the Vman pin to enable the management interface circuitry of the cable. Power may be removed to reset the management circuitry in the cable assembly.

[a] Electrical characteristics are defined in SFF-8449.

5.5.3.4.2.8 Mini SAS HD external connector memory map

SFF-8449 defines the Mini SAS HD external connector management interface memory map. The Mini SAS HD external cable assembly shall support the following management interface memory map registers:

a) supported SAS baud rate;

b) vendor name;
c) vendor part number;
d) vendor revision;
e) copper cable attenuation;
f) power class;
g) minimum operating voltage;
h) transmitter technology;
i) cable width; and
j) propagation delay.

5.5.3.4.3 QSFP+ connectors

5.5.3.4.3.1 QSFP+ cable plug

The QSFP+ cable plug connector is the free (plug) 38-circuit connector defined in SFF-8436. Figure 65 shows the QSFP+ cable plug connector.

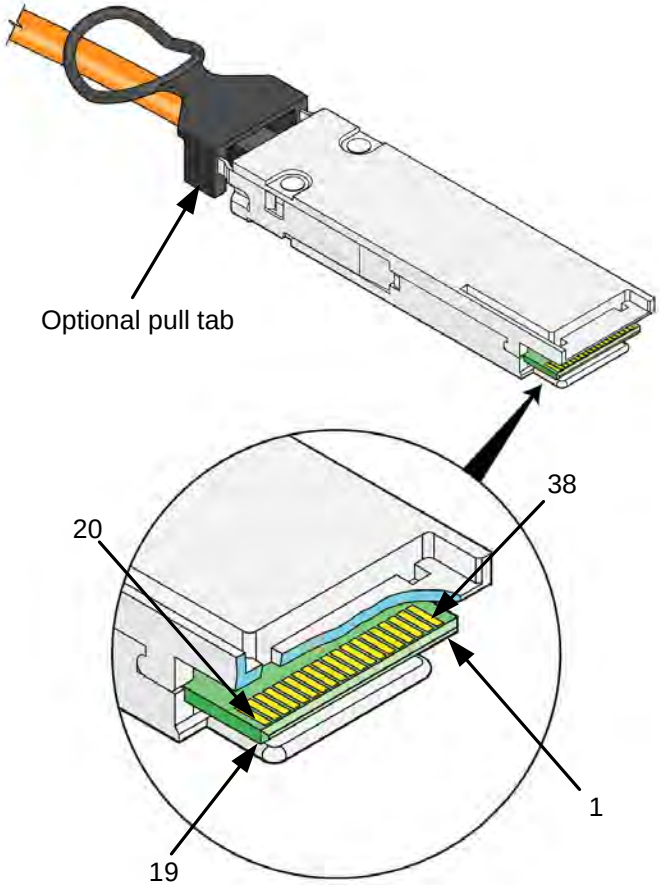

Figure 65 — QSFP+ cable plug connector

Table 23 (see 5.5.3.4.3.3) define the pin assignments for the QSFP+ cable plug connector.

The QSFP+ cable plug connectors shall not include keying.

5.5.3.4.3.2 QSFP+ receptacle

The QSFP+ receptacle connector is the fixed (receptacle) 38-circuit connector defined in SFF-8436. Figure 66 shows the QSFP+ receptacle connector.

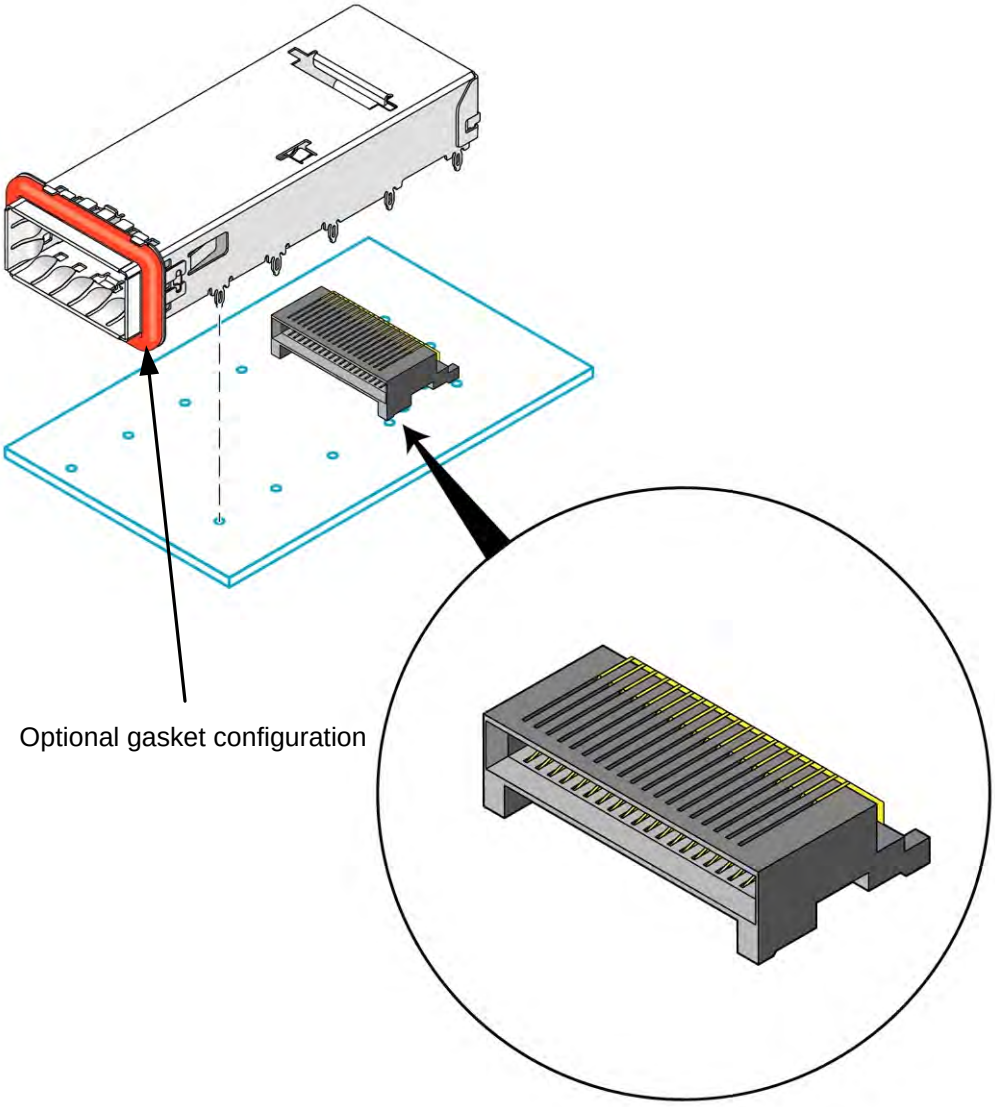

Figure 66 — QSFP+ receptacle **connector**

Table 23 (see 5.5.3.4.3.3) define the pin assignments for the QSFP+ receptacle connector.

The QSFP+ receptacle connectors shall not include keying.

5.5.3.4.3.3 QSFP+ connector pin assignments

Table 23 defines the pin assignments for QSFP+ connectors (see 5.5.3.4.3.1 and 5.5.3.4.3.2). Specific pins are used to provide managed cable communication and power to the cable assembly.

Table 23 — QSFP+ connector pin assignments (part 1 of 2)

Pin	Signal	Description	Mating level [a]
1	GND [b]	Ground	First
2	Tx2n	Transmitter inverted data input	Third
3	Tx2p	Transmitter non-inverted data input	Third
4	GND [b]	Ground	First
5	Tx4n	Transmitter inverted data input	Third
6	Tx4p	Transmitter non-inverted data input	Third
7	GND [b]	Ground	First
8	ModSelL	Module select	Third
9	ResetL	Module reset	Third
10	Vcc Rx [c]	+3.3V power supply receiver	Second
11	SCL	2-wire serial interface clock	Third
12	SDA	2-wire serial interface data	Third
13	GND [b]	Ground	First
14	Rx3p	Receiver non-inverted data output	Third
15	Rx3n	Receiver inverted data output	Third
16	GND [b]	Ground	First
17	Rx1p	Receiver non-inverted data output	Third
18	Rx1n	Receiver inverted data output	Third
19	GND [b]	Ground	First
20	GND [b]	Ground	First
21	Rx2n	Receiver inverted data output	Third
22	Rx2p	Receiver non-inverted data output	Third
23	GND [b]	Ground	First
24	Rx4n	Receiver inverted data output	Third
25	Rx4p	Receiver non-inverted data output	Third
26	GND [b]	Ground	First
27	ModPrsL	Module present	Third
28	IntL	Interrupt	Third
29	Vcc Tx [c]	+3.3V power supply transmitter	Second

Table 23 — QSFP+ connector pin assignments (part 2 of 2)

Pin	Signal	Description	Mating level [a]
30	Vcc1 [c]	+3.3V power supply	Second
31	LPMode	Low power mode	Third
32	GND [b]	Ground	First
33	Tx3p	Transmitter non-inverted data input	Third
34	Tx3n	Transmitter inverted data input	Third
35	GND [b]	Ground	First
36	Tx1p	Transmitter non-inverted data input	Third
37	Tx1n	Transmitter inverted data input	Third
38	GND [b]	Ground	First

[a] The mating level indicates the physical dimension of the contact. See SFF-8436.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

5.5.3.4.3.4 QSFP+ memory map

The memory map for QSFP+ is used for identification information, cable characteristics, control functions, and digital monitoring. The 2-wire serial interface is required for all QSFP+ devices. SFF-8436 defines the supported SAS baud rate codes. See SFF-8436 for register map details and the operation of the 2-wire serial interface.

5.5.4 Cable assemblies

5.5.4.1 SAS internal cable assemblies

5.5.4.1.1 SAS Drive cable assemblies

A SAS Drive cable assembly is either:

a) a single-port SAS Drive cable assembly; or
b) a dual-port SAS Drive cable assembly.

A SAS Drive cable assembly has:

a) a SAS Drive cable receptacle connector (see 5.5.3.3.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL-2).

The power and READY LED signal connection is vendor specific.

A SAS initiator device shall use a SATA host plug connector (see SATA) for connection to a SAS Drive cable assembly. The signal assignment for the SAS initiator device or expander device (see SPL-2) with this connector shall be the same as that defined for a SATA host (see SATA).

Figure 67 shows the Single-port SAS Drive cable assembly.

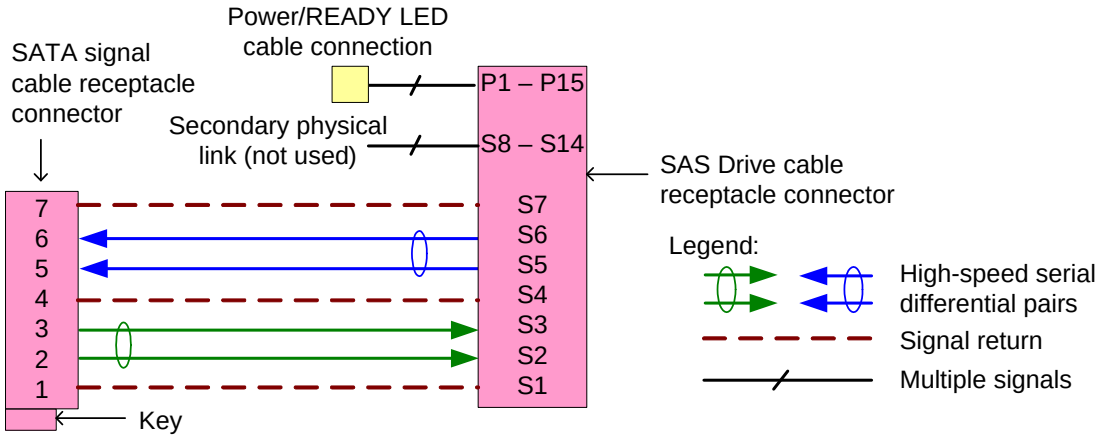

Figure 67 — Single-port SAS Drive cable assembly

Figure 68 shows the Dual-port SAS Drive cable assembly.

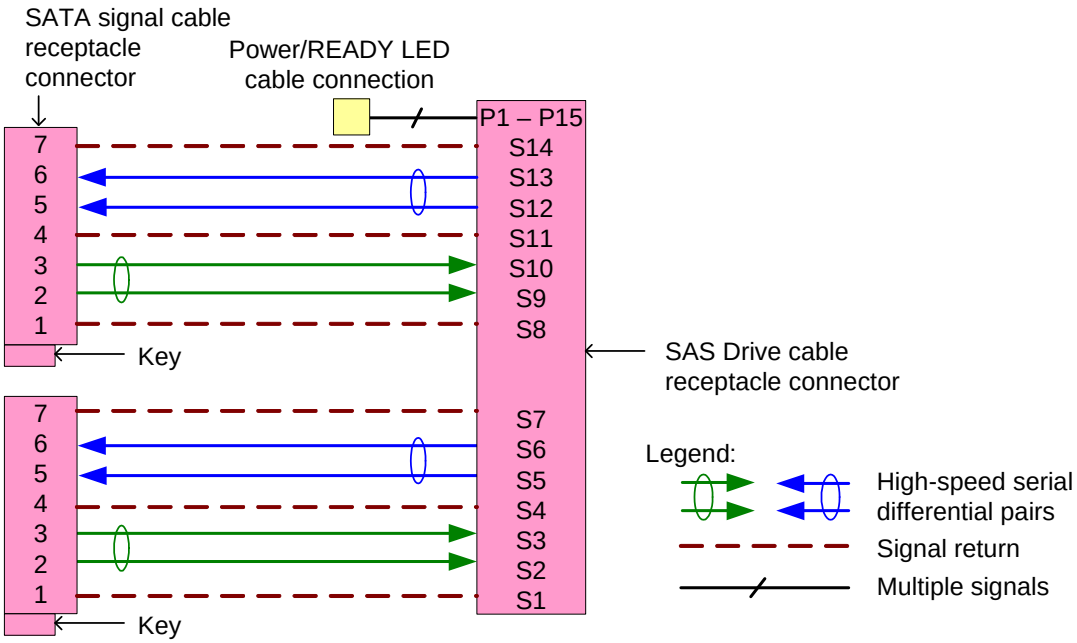

Figure 68 — Dual-port SAS Drive cable assembly

5.5.4.1.2 SAS internal symmetric cable assemblies

5.5.4.1.2.1 SAS internal symmetric cable assemblies overview

A SAS internal symmetric cable assembly has:

a) a SAS 4i cable receptacle connector (see 5.5.3.3.2.1) on each end (see 5.5.4.1.2.2);
b) a Mini SAS 4i cable plug connector (see 5.5.3.3.3.1) on each end (see 5.5.4.1.2.3);
c) a Mini SAS HD 4i cable plug connector on each end;
d) a Mini SAS HD 8i cable plug connector on each end;
e) a SAS 4i cable receptacle connector on one end and a Mini SAS 4i cable plug connector on the other end, with vendor specific sidebands (see 5.5.4.1.2.5);
f) a SAS 4i cable receptacle connector on the controller end and a Mini SAS 4i cable plug connector on the backplane end, with sidebands supporting SGPIO (see 5.5.4.1.2.7);
g) a Mini SAS 4i cable plug connector on the controller end and a SAS 4i cable receptacle connector on the backplane end, with sidebands supporting SGPIO (see 5.5.4.1.2.8); or
h) a Mini SAS 4i cable plug connector on one end and a Mini SAS HD 4i cable plug connector on the other end (see 5.5.4.1.2.9).

In a SAS internal symmetric cable assembly, the Tx signals on one end shall be connected to Rx signals on the other end (e.g., a Tx + of one connector shall connect to an Rx + of the other connector. SAS internal symmetric cable assemblies should be labeled to indicate how many physical links are included (e.g., 1X, 2X, 3X, and 4X on each connector's housing).

5.5.4.1.2.2 SAS internal symmetric cable assembly - SAS 4i

Figure 69 shows the SAS internal symmetric cable assembly with SAS 4i cable receptacle connectors at each end.

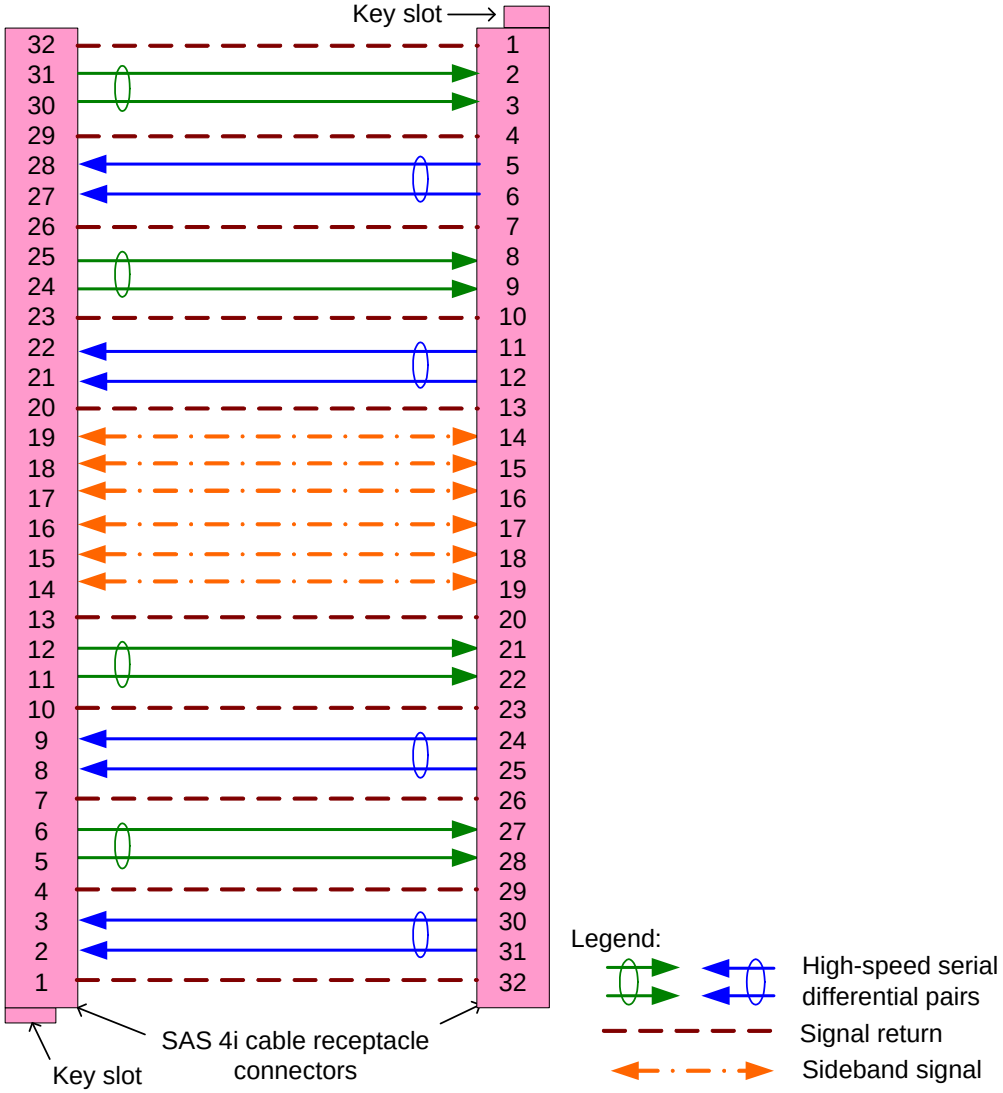

Figure 69 — SAS internal symmetric cable assembly - SAS 4i

In addition to the signal return connections shown in figure 69, one or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications, this cable assembly may support one to four physical links. SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, this cable assembly shall support all four physical links and the controllers should use all four physical links, because one controller's physical links 0 and 1 are attached the other controller's physical links 3 and 2, respectively. If both controllers use one or two physical links starting with physical links 0, communication is not possible. If both controllers use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible. SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND5 of the other controller).

5.5.4.1.2.3 SAS internal symmetric cable assembly - Mini SAS 4i

Figure 70 shows the SAS internal cable assembly with Mini SAS 4i cable plug connectors at each end.

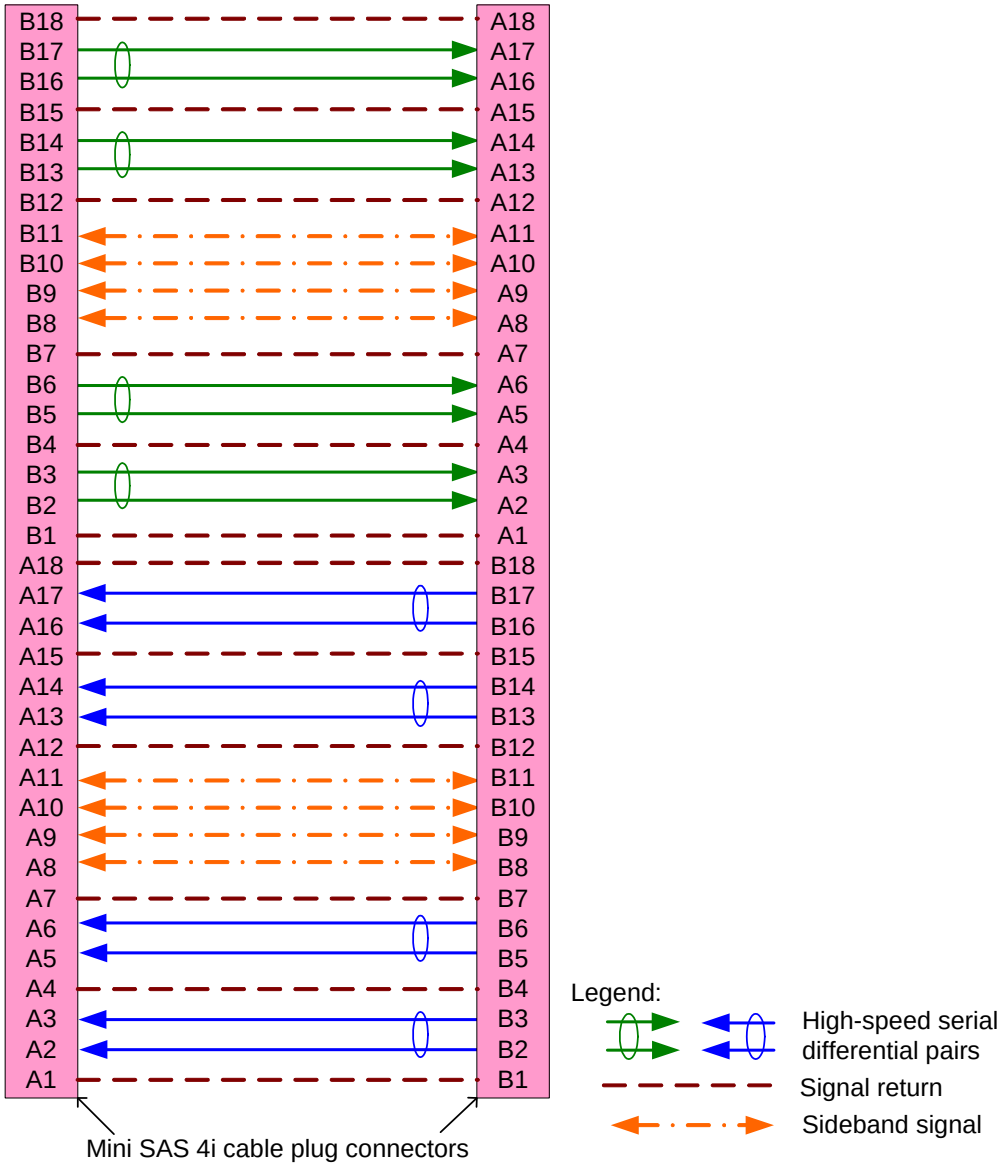

Figure 70 — SAS internal symmetric cable assembly - Mini SAS 4i

In addition to the signal return connections shown in figure 70, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.5.4.1.2.4 SAS internal symmetric cable assembly - Mini SAS HD 4i

Figure 71 shows the SAS internal cable assembly with Mini SAS HD 4i cable plug connectors at each end.

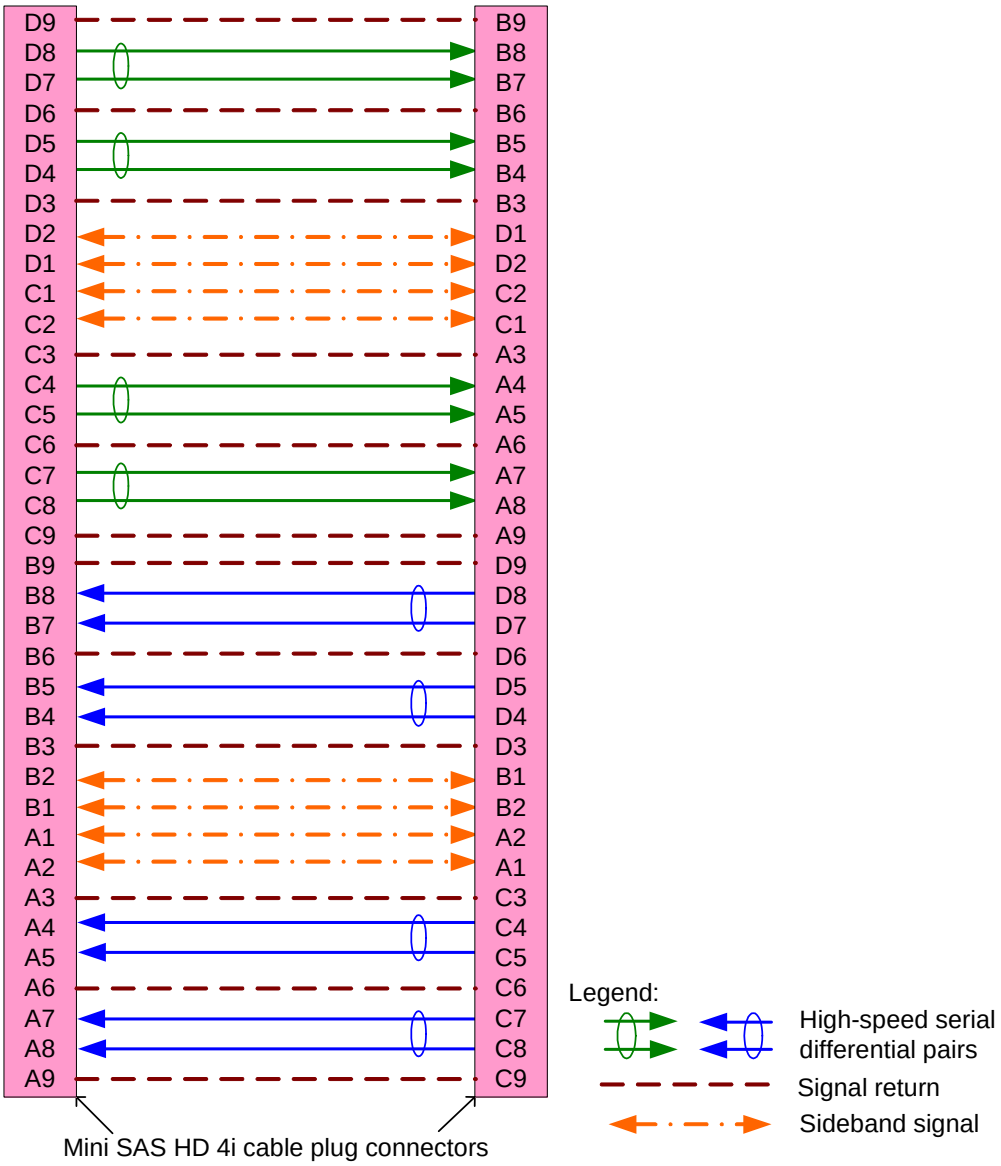

Figure 71 — SAS internal symmetric cable assembly - Mini SAS HD 4i

In addition to the signal return connections shown in figure 71, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.5.4.1.2.5 SAS internal symmetric cable assembly - Mini SAS HD 8i

Figure 72 shows the SAS internal cable assembly with Mini SAS HD 8i cable plug connectors at each end.

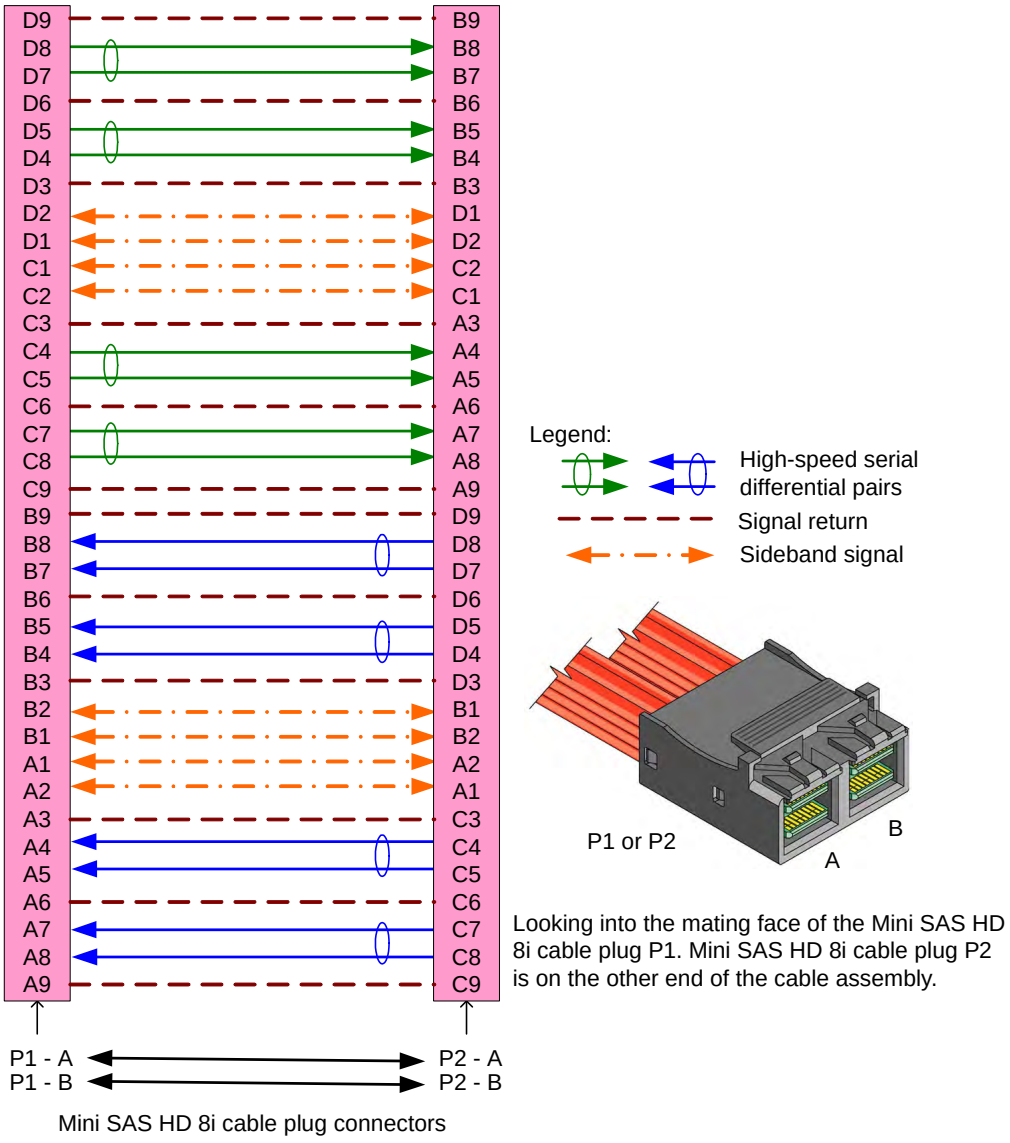

Figure 72 — SAS internal symmetric cable assembly - Mini SAS HD 8i

In addition to the signal return connections shown in figure 72, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.5.3.3.4.5 for connector module pin assingments.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.5.4.1.2.6 SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor specific sidebands

Figure 73 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at one end and a Mini SAS 4i cable plug connector at the other end, with vendor specific sidebands.

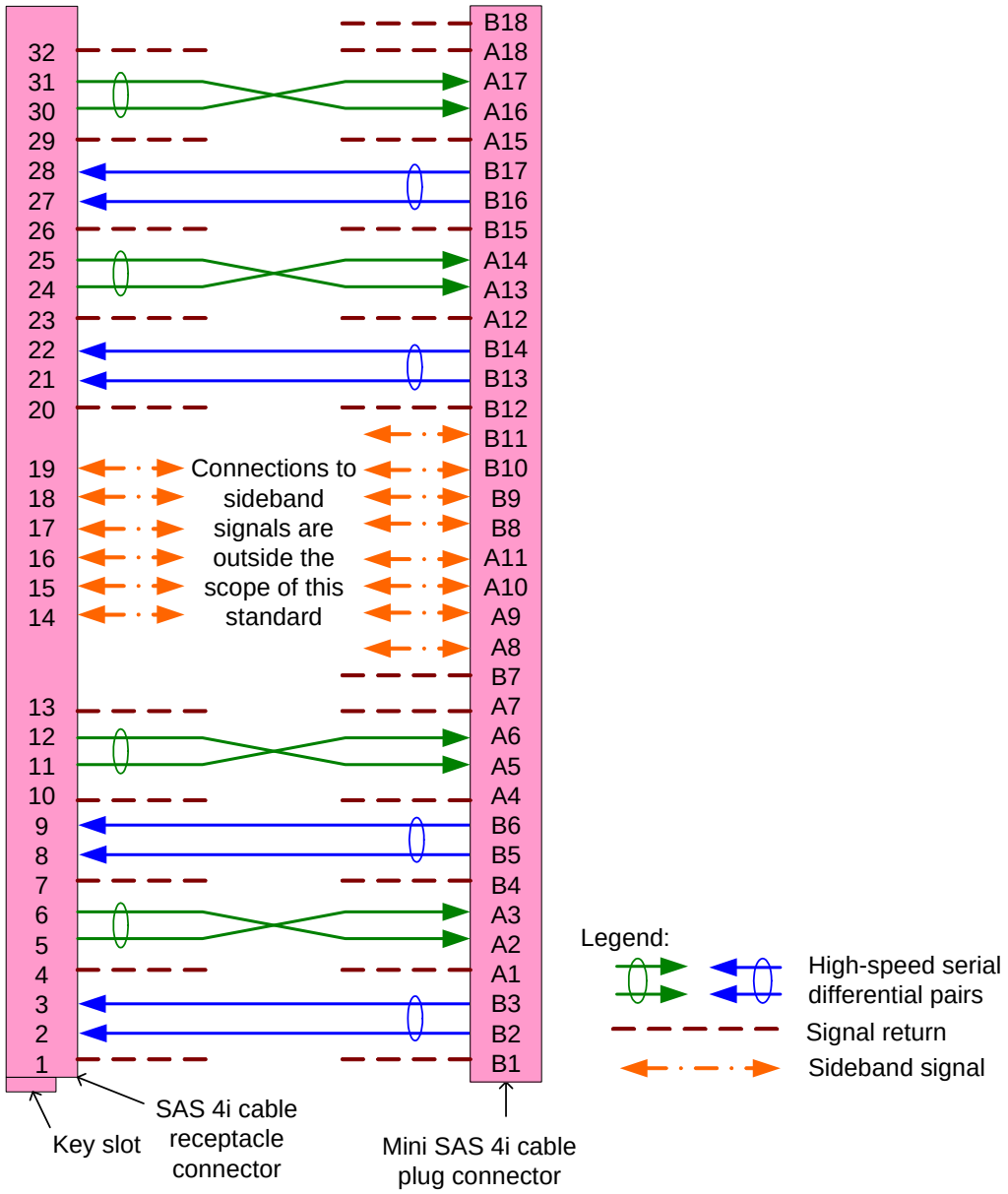

Figure 73 — SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor specific sidebands

NOTE 15 - This cable assembly may require different SIDEBAND signal routing based on whether the controller or backplane is using the SAS 4i connector.

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications with the SAS 4i cable receptacle connector on the controller end, this cable assembly may support one to four physical links.

For controller-to-controller applications, this cable assembly may support one to four physical links.

For controller-to-backplane applications with the Mini SAS 4i cable receptacle connector on the controller end, this cable assembly shall support all four physical links and the controller should use all four physical links, because the controller's physical links 0, 1, 2, and 3 are attached to the backplane's physical links 3, 2, 1, and 0, respectively. If both the controller and the backplane use one or two physical links starting with physical links 0, communication is not possible. If both the controller and the backplane use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible.

5.5.4.1.2.7 SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO

Figure 74 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at the controller end and a Mini SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

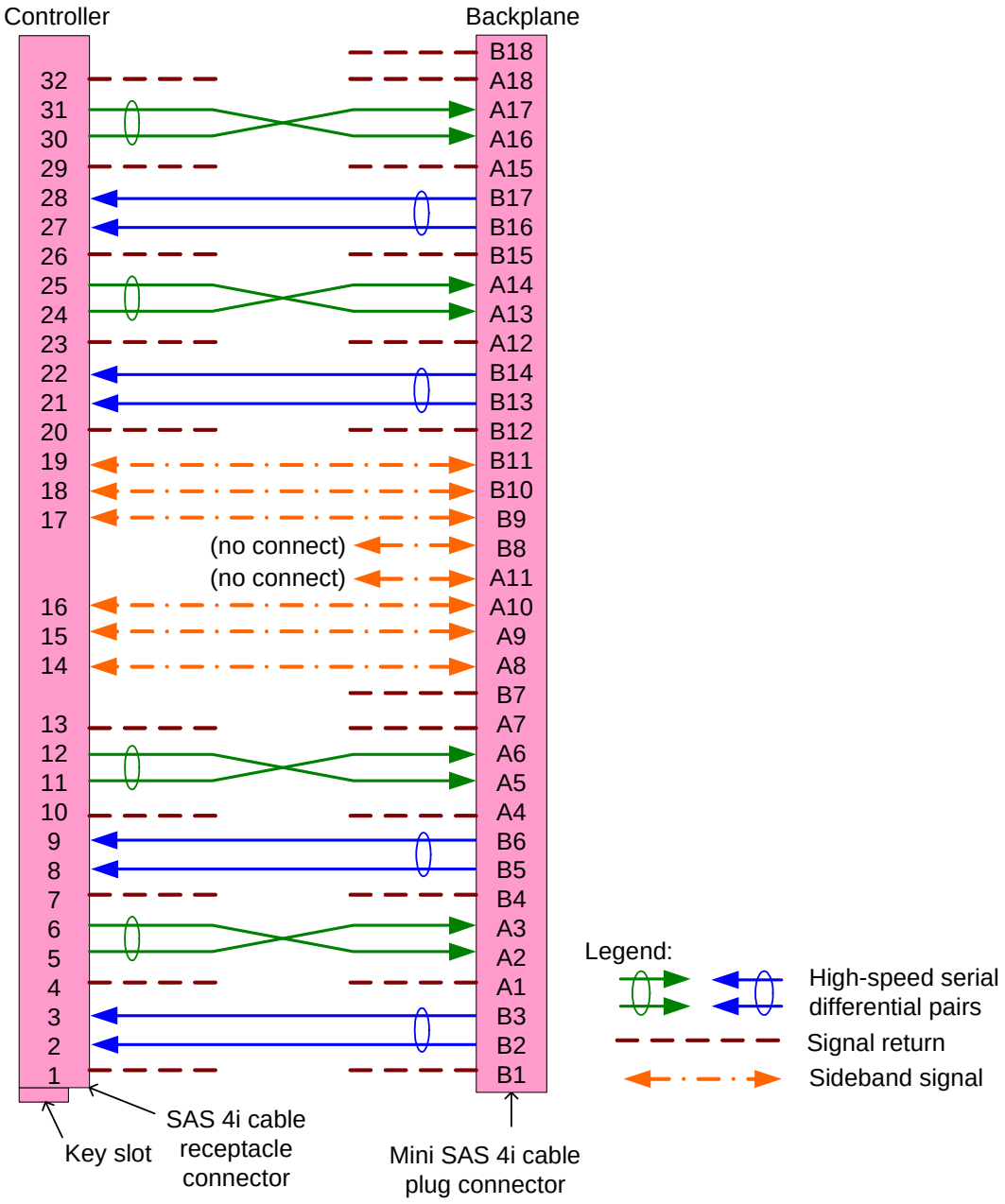

Figure 74 — SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.5.4.1.2.8 SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO

Figure 75 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable receptacle connector at the controller end and a SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

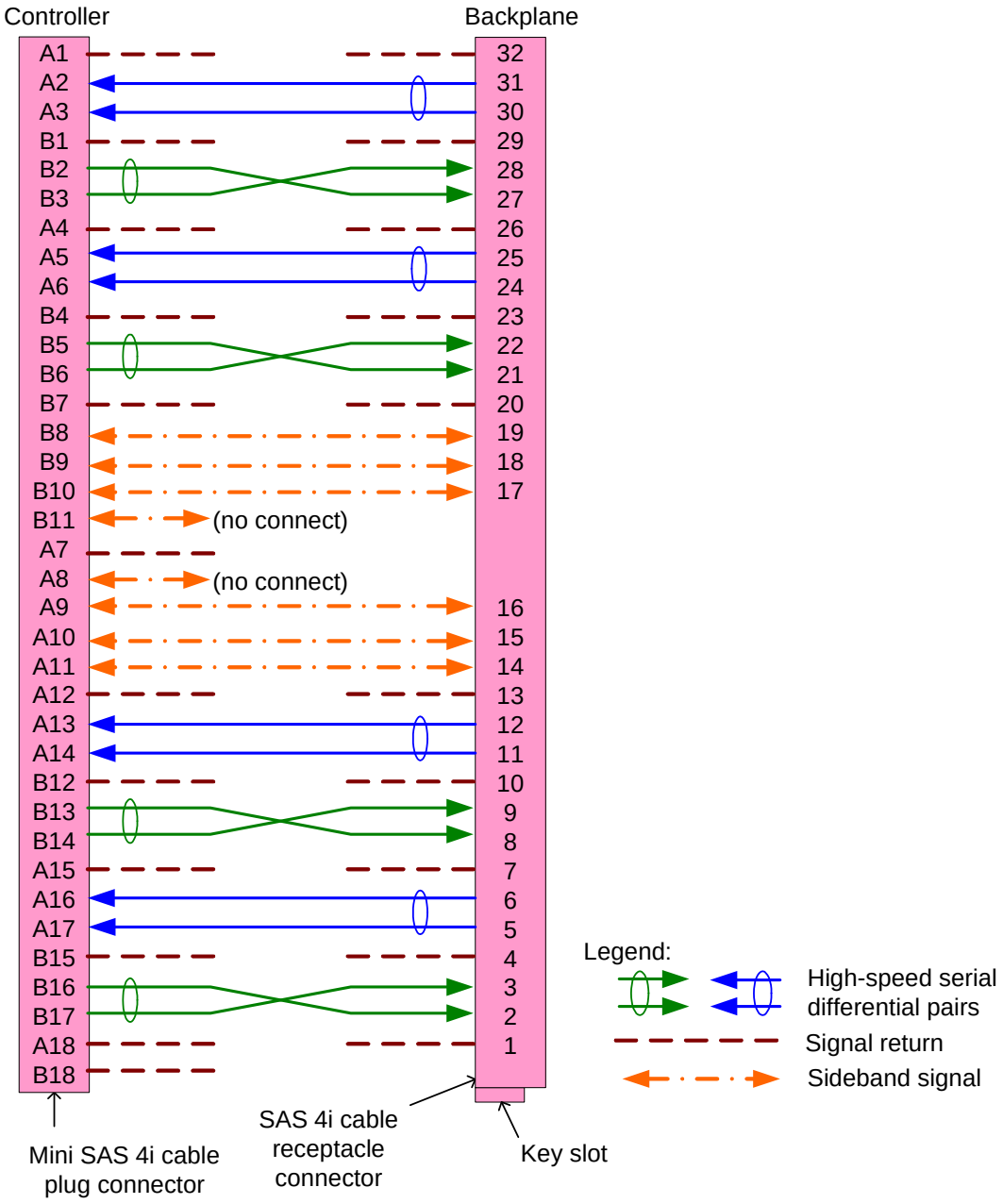

Figure 75 — SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.5.4.1.2.9 SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

Figure 76 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable plug connector at one end and a Mini SAS HD 4i cable plug connector at the other end.

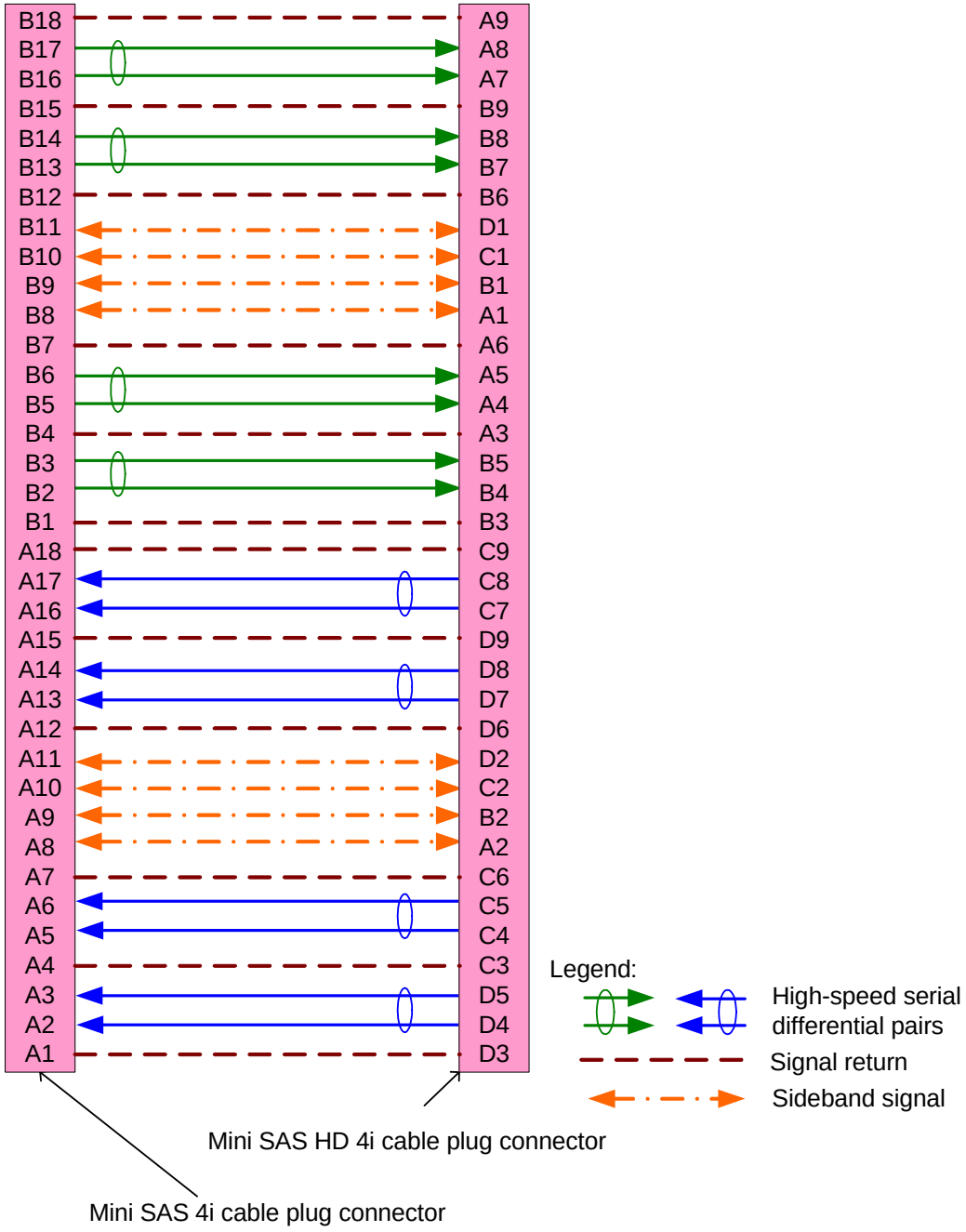

Figure 76 — SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

In addition to the signal return connections shown in figure 76, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.5.4.1.3 SAS internal fanout cable assemblies

5.5.4.1.3.1 SAS internal fanout cable assemblies overview

A SAS internal fanout cable assembly is either:

a) a SAS internal controller-based fanout cable assembly (see 5.5.4.1.3.2) with:
   A) a SAS 4i cable receptacle connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;
   B) a Mini SAS 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end; or
   C) a Mini SAS HD 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;

   or

b) a SAS internal backplane-based fanout cable assembly (see 5.5.4.1.3.3) with:
   A) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a SAS 4i cable receptacle connector on the other end (i.e., the backplane end);
   B) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS 4i cable plug connector on the other end (i.e., the backplane end); or
   C) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS HD 4i cable plug connector on the other end (i.e., the backplane end).

In a SAS internal fanout symmetric cable assembly, the Tx signals on one end shall be connected to Rx signals on the other end (e.g., a Tx + of one connector shall connect to an Rx + of the other connector).

5.5.4.1.3.2 SAS internal controller-based fanout cable assemblies

Figure 77 shows the SAS internal controller-based fanout cable assembly with a SAS 4i cable receptacle connector at the controller end.

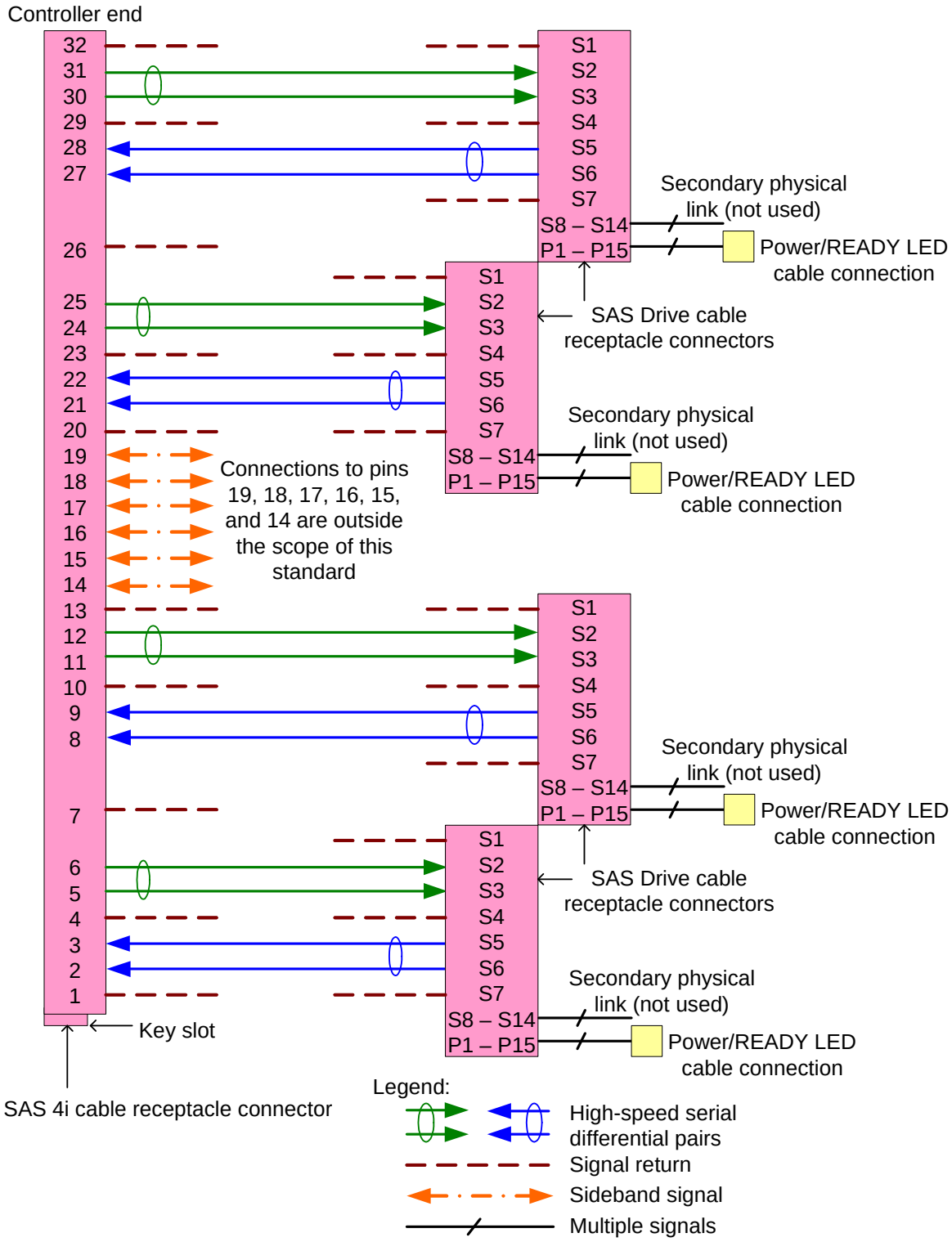

Figure 77 — SAS internal controller-based fanout cable assembly - SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 78 shows the SAS internal controller-based fanout cable assembly with a Mini SAS 4i cable plug connector at the controller end.

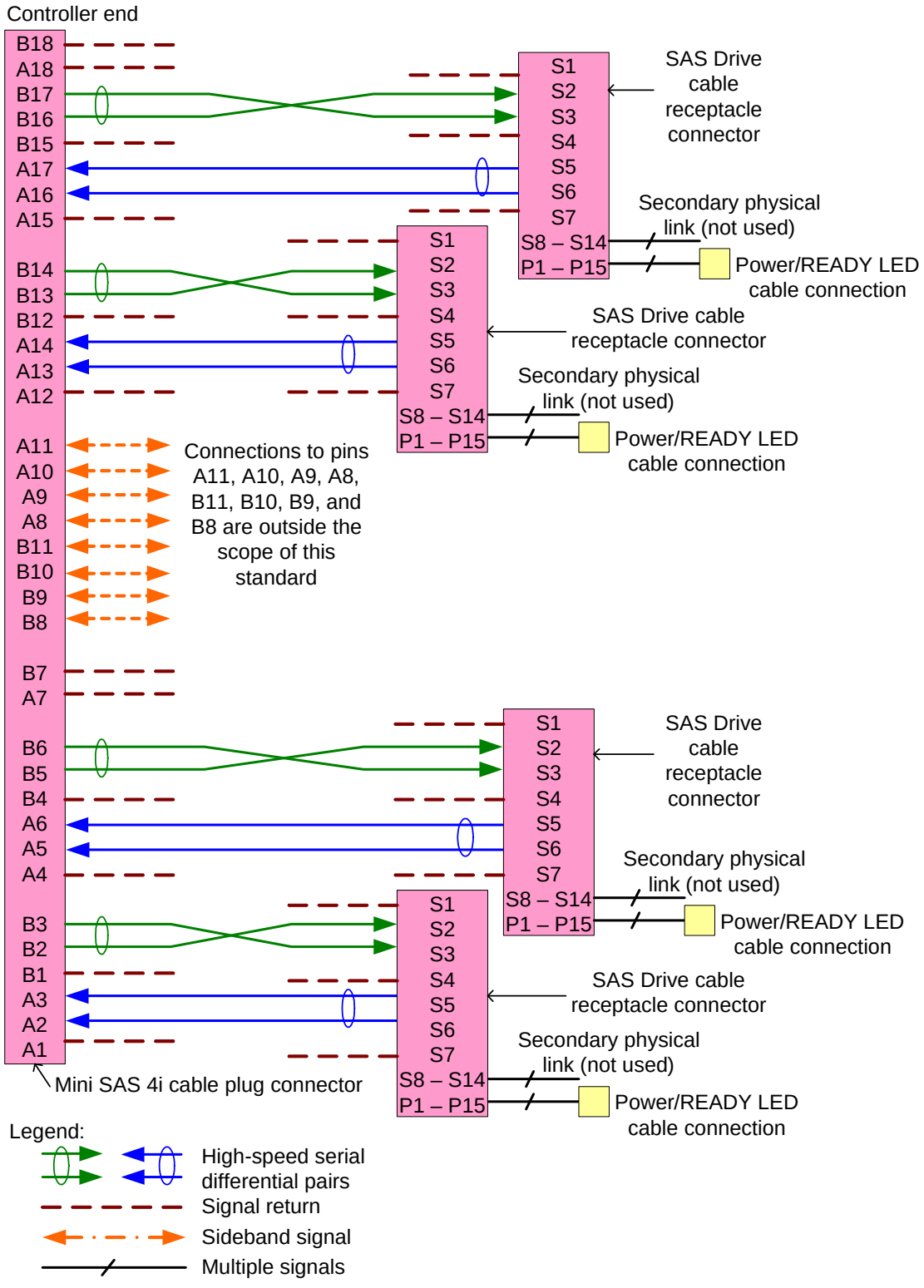

Figure 78 — SAS internal controller-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 79 shows the SAS internal controller-based fanout cable assembly with a Mini SAS HD 4i cable plug connector at the controller end.

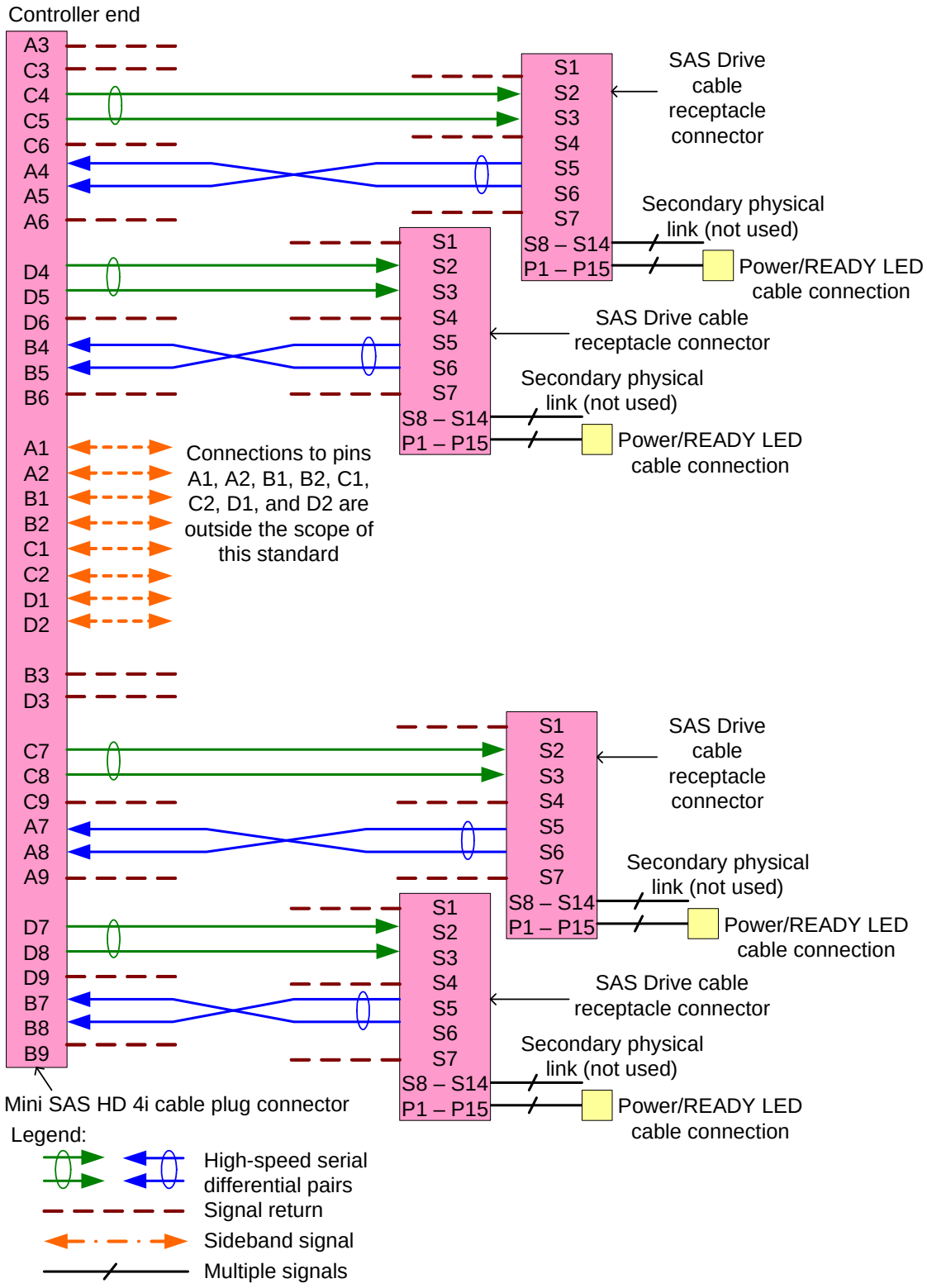

Figure 79 — SAS internal controller-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.5.4.1.3.3 SAS internal backplane-based fanout cable assemblies

Figure 80 shows the SAS internal backplane-based fanout cable assembly with the SAS 4i cable receptacle connector.

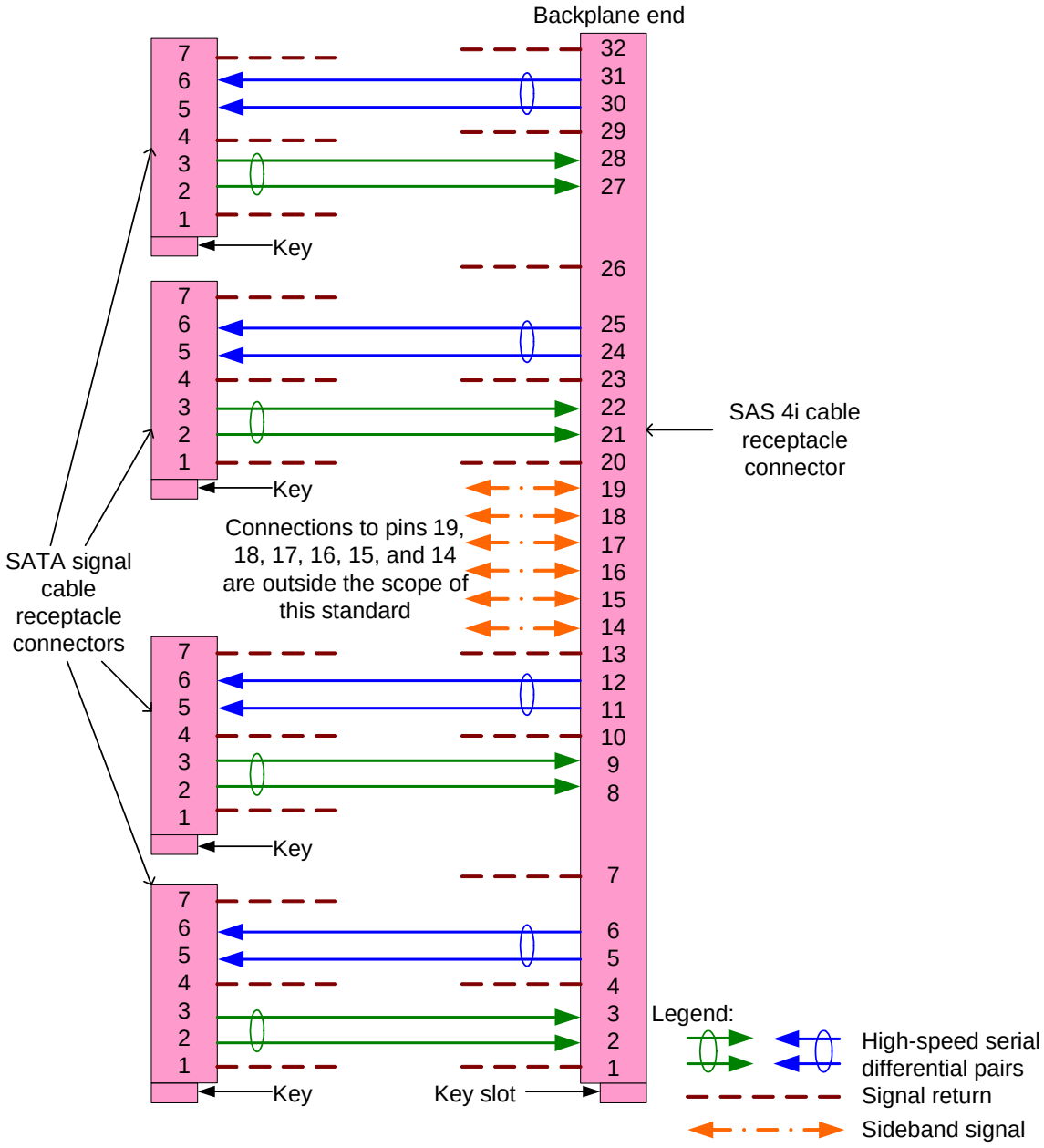

Figure 80 — SAS internal backplane-based fanout cable assembly - SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 81 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS 4i cable receptacle connector.

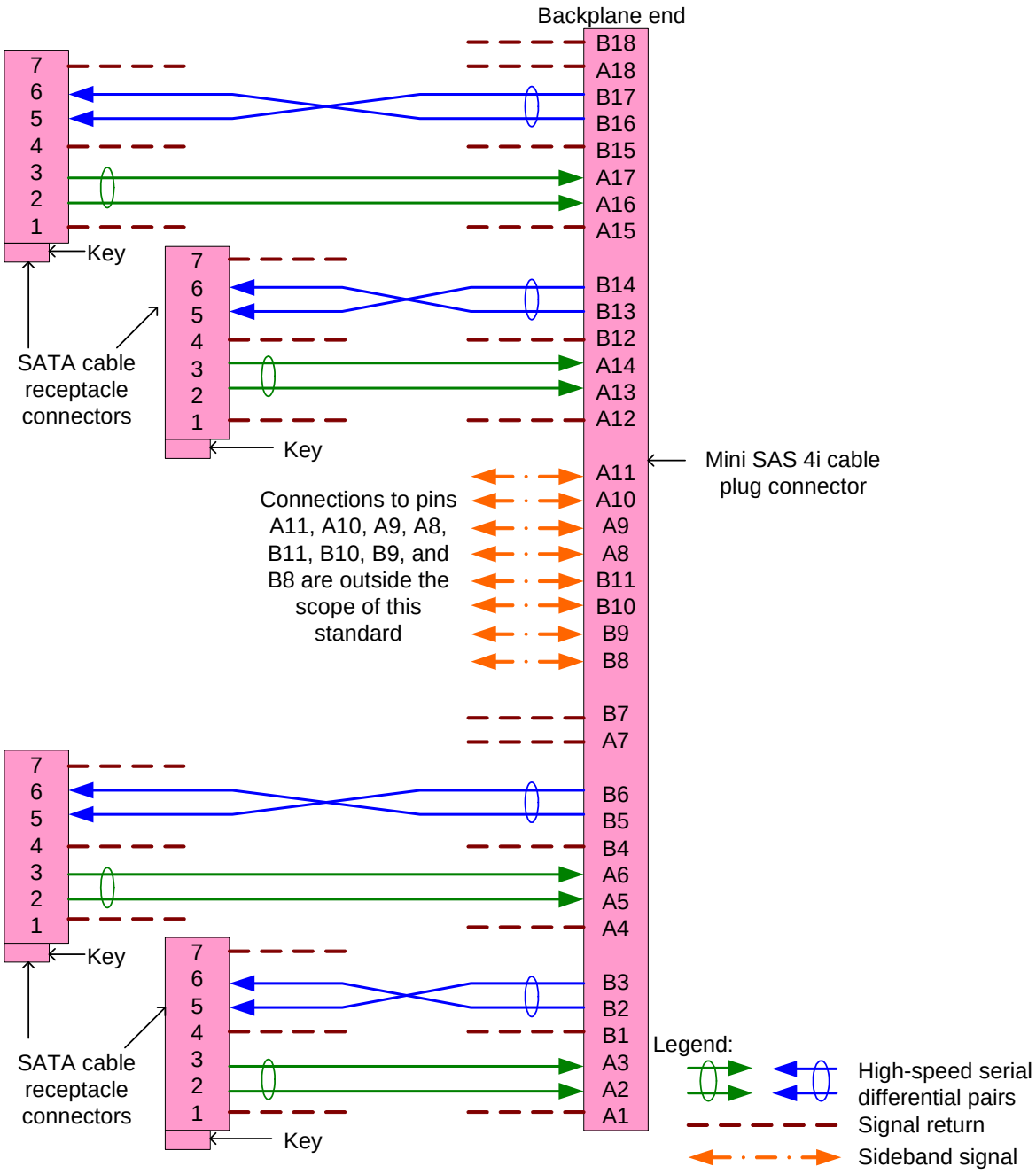

Figure 81 — SAS internal backplane-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 82 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS HD 4i cable receptacle connector.

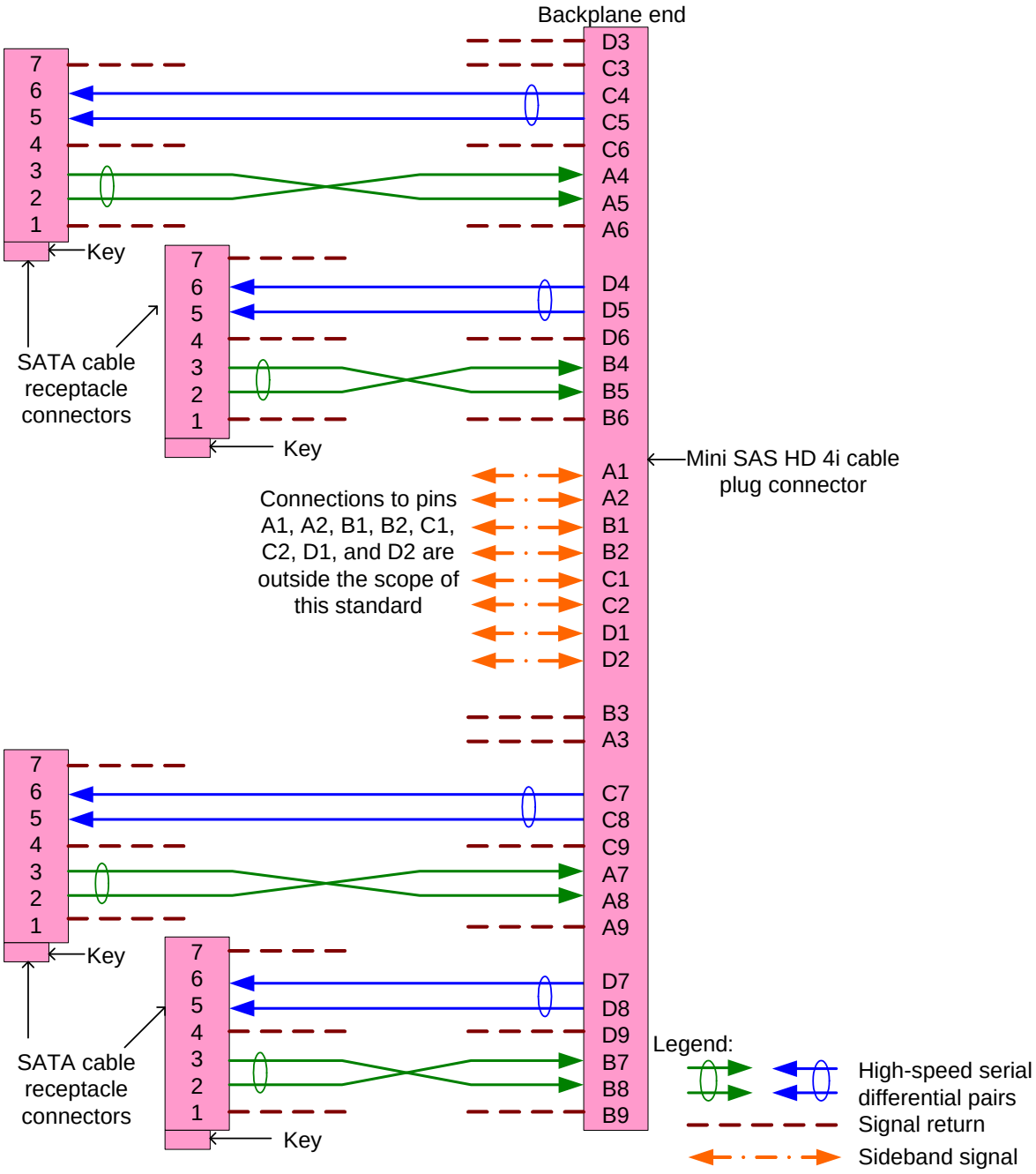

Figure 82 — SAS internal backplane-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.5.4.2 SAS external cable assemblies

5.5.4.2.1 SAS external cable assemblies overview

A SAS external cable assembly has:

a) a Mini SAS 4x cable plug connector (see 5.5.3.4.1.1) at each end (see 5.5.4.2.2);

b) a Mini SAS HD 4x cable plug connector (see 5.5.3.4.2.1) at each end (see 5.5.4.2.3);
c) a Mini SAS HD 8x cable plug connector (see 5.5.3.4.2.2) at each end (see 5.5.4.2.4);
d) a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end (see 5.5.4.2.5); or
e) a QSFP+ cable plug connector (see 5.5.3.4.3.1) at each end (see 5.5.4.2.6).

SAS external cable assemblies do not include power or the READY LED signal.

Although the connector always supports four or eight physical links, a SAS external cable assembly may support one to eight physical links. SAS external cable assemblies should be labeled to indicate how many physical links are included (i.e., 1X, 2X, 3X, 4X, 5X, 6X, 7X, or 8X on each connector's housing).

The Tx signals on one end shall be connected to the corresponding Rx signals of the other end (e.g., Tx 0+ of one connector shall be connected to Rx 0+ of the other connector).

Signal returns shall not be connected to CHASSIS GROUND in the cable assembly.

In addition to the SAS icon (see Annex H), additional icons are defined for external connectors to guide users into making compatible attachments (i.e., not attaching expander device table routing phys to expander device table routing phys in externally configurable expander devices (see SPL-2), which is not allowed (see SPL-2)). Connectors that have one or more matching icons are intended to be attached together. Connectors that do not have a matching icon should not be attached together.

One end of the SAS external cable assembly shall support being attached to an end device, an enclosure out port, or an enclosure universal port. The other end of the SAS external cable assembly shall support being attached to an end device, an enclosure in port, or an enclosure universal port. If a Mini SAS 4x cable plug connector is used, then it shall include icons and key slots as defined in 5.5.3.4.1.1.

5.5.4.2.2 SAS external cable assembly - Mini SAS 4x

Figure 83 shows the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end.

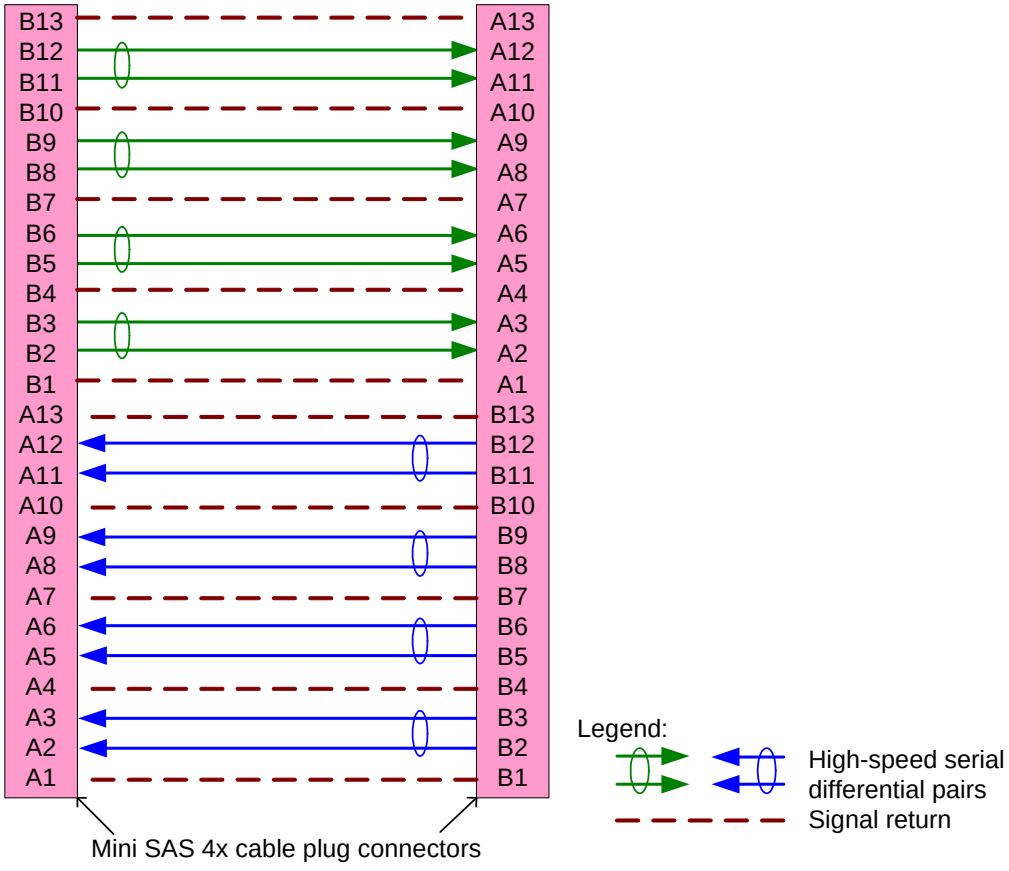

Figure 83 — Mini SAS 4x external cable assembly

In addition to the signal return connections shown in figure 83, one or more of the signal returns may be connected together in this cable assembly.

Figure 84 shows the SAS external cable assembly with Mini SAS 4x active cable assembly plug connectors at each end.

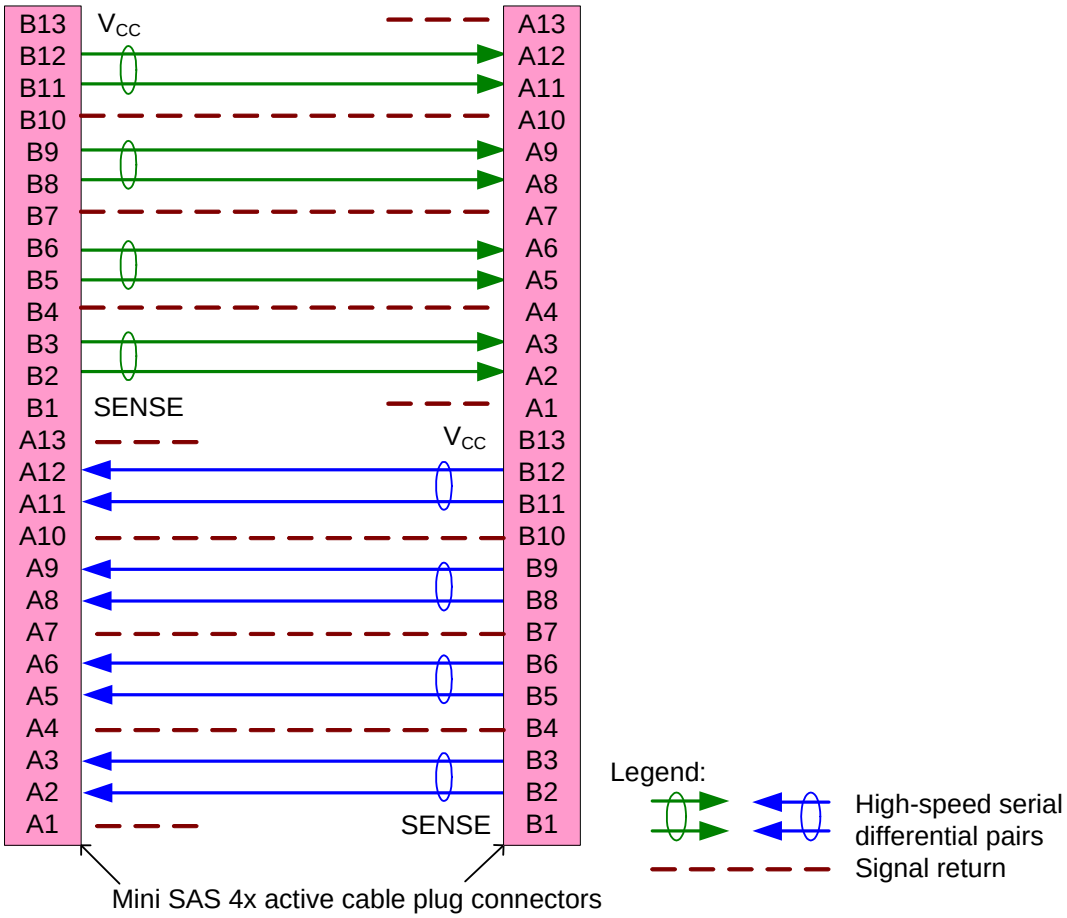

Figure 84 — Mini SAS 4x active external cable assembly

In addition to the signal return connections shown in figure 84, one or more of the signal returns may be connected together in this cable assembly.

Figure 85 shows the an example cable with icons and key slots in the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. Depending on the cable configuration, the Mini SAS 4x cable

connectors may also include different icon, key slot, and key combinations than shown in figure 85 (see 5.5.3.4.1.1).

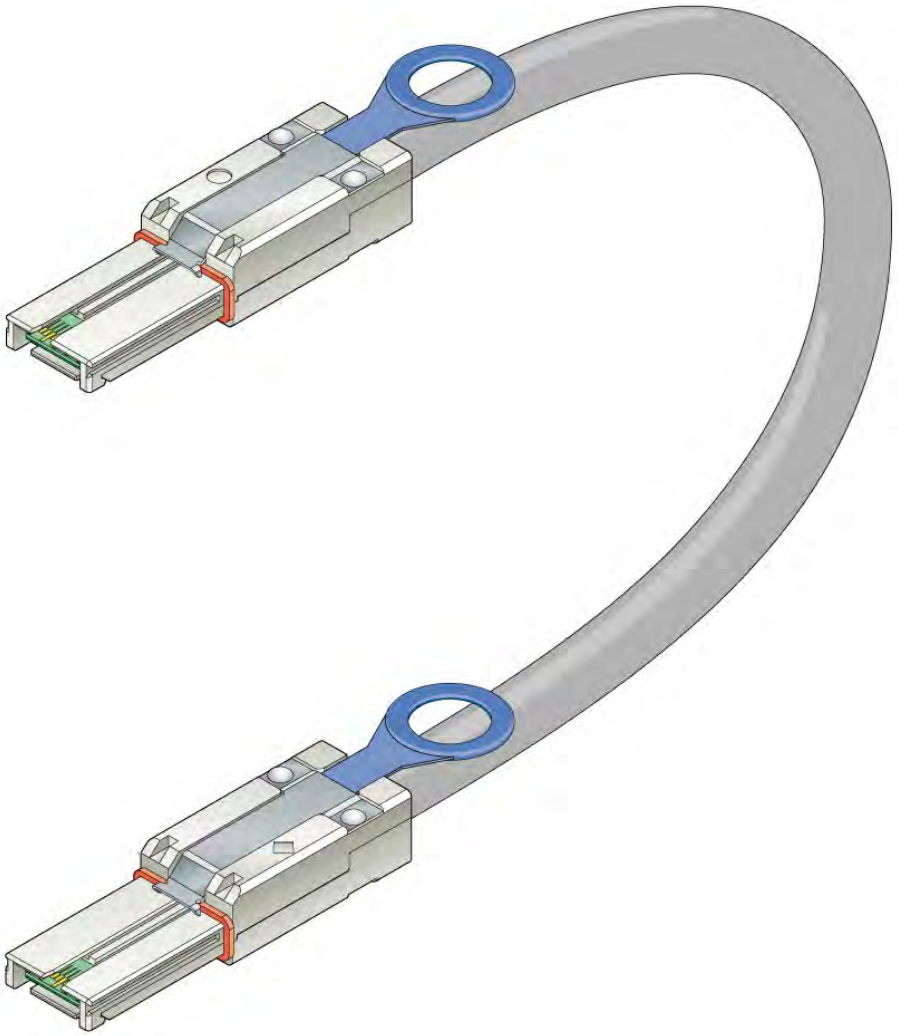

Figure 85 — SAS external cable assembly with Mini SAS 4x cable plug connectors

Although the topology is supported by this standard and SPL-2, a SAS external cable assembly with Mini SAS 4x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL-2.

5.5.4.2.3 SAS external cable assembly - Mini SAS HD 4x

Figure 86 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

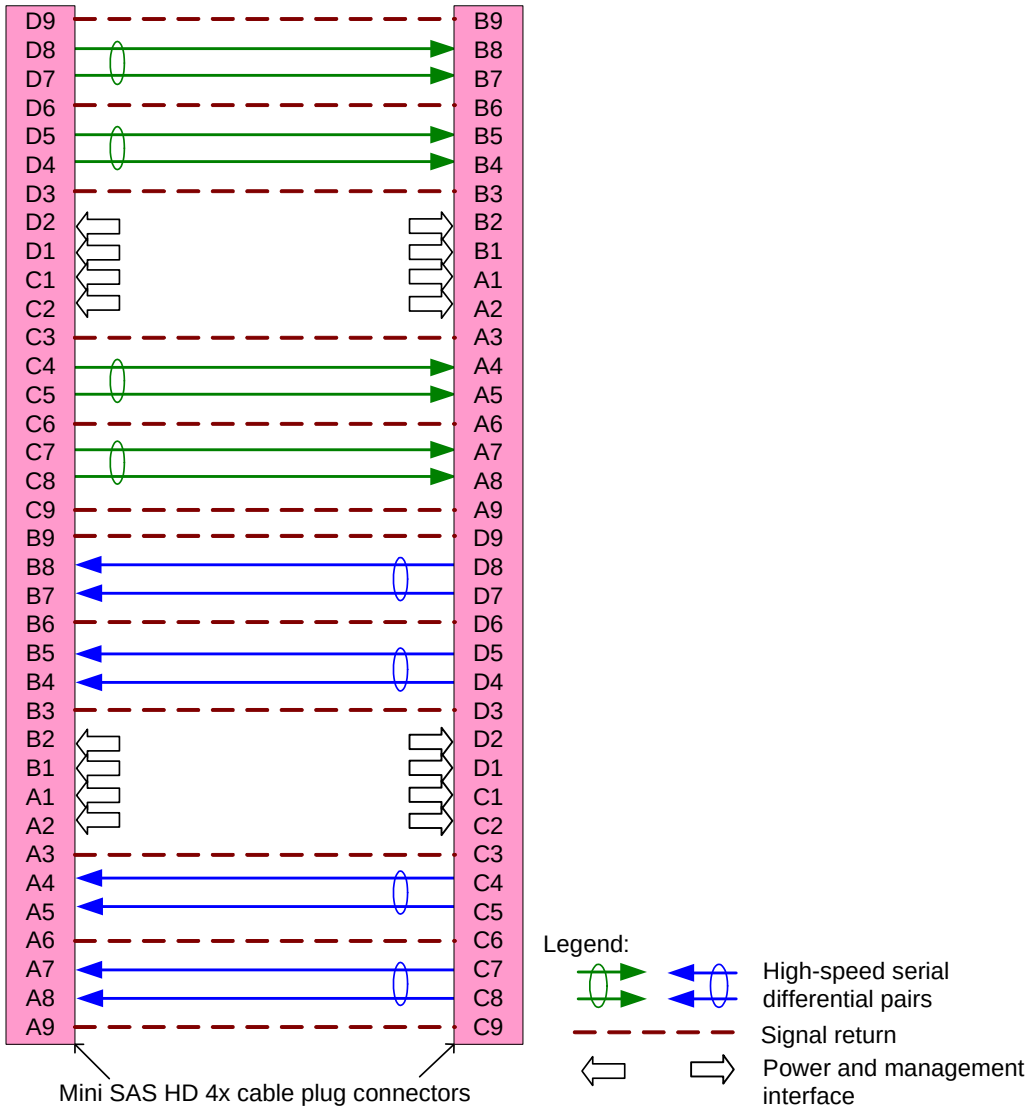

Figure 86 — SAS external cable assembly - Mini SAS HD 4x

In addition to the signal return connections shown in figure 86, one or more of the signal returns may be connected together in this cable assembly.

Figure 87 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

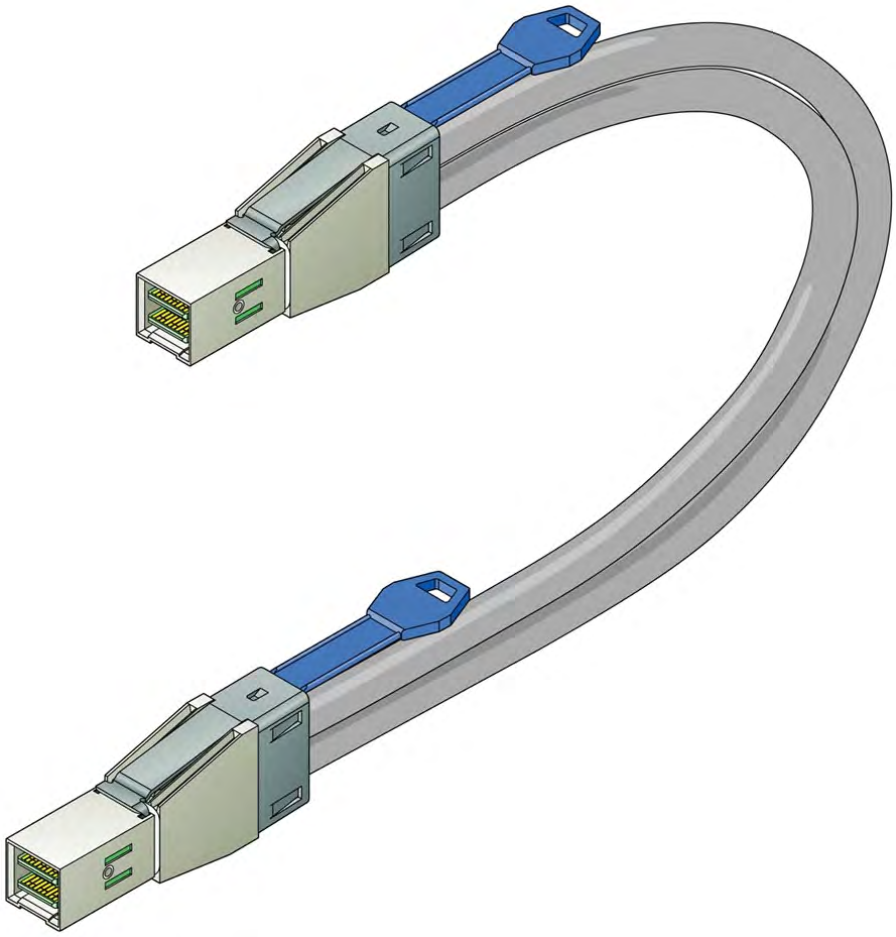

Figure 87 — SAS external cable assembly with Mini SAS HD 4x cable plug connectors

Although the topology is supported by this standard and SPL-2, a SAS external cable assembly with Mini SAS HD 4x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL-2.

5.5.4.2.4 SAS external cable assembly - Mini SAS HD 8x

Figure 88 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

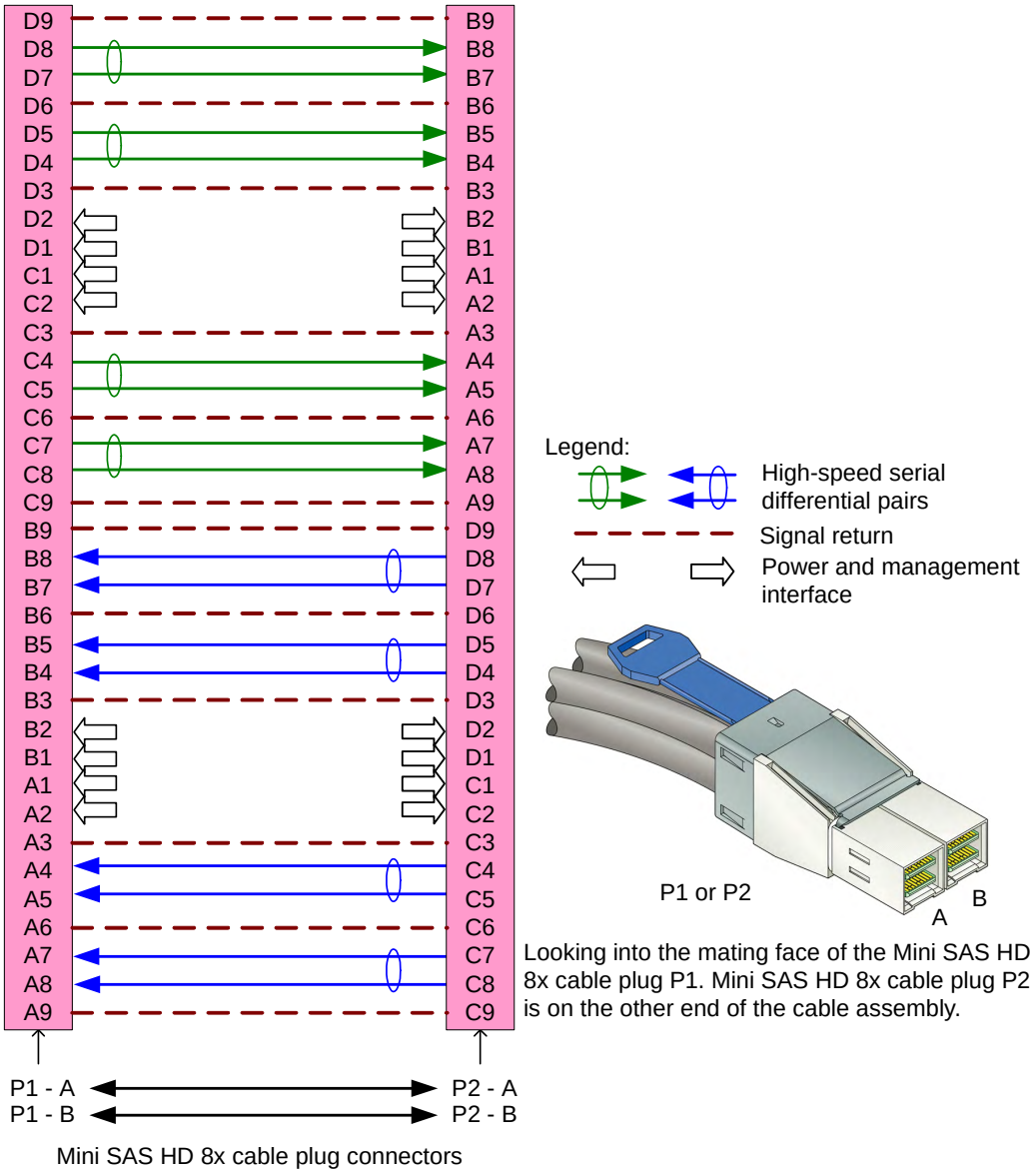

Figure 88 — SAS external cable assembly - Mini SAS HD 8x

In addition to the signal return connections shown in figure 88, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.5.3.4.2.6 for connector module pin assingments.

Figure 89 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

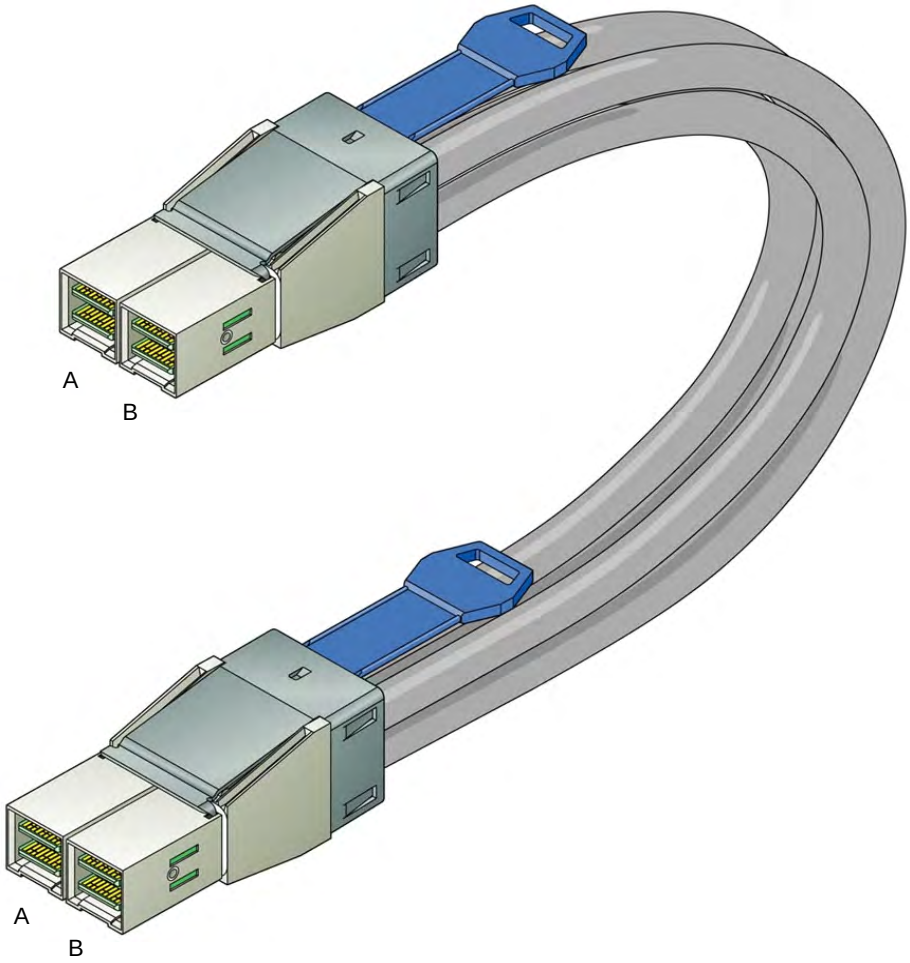

Figure 89 — SAS external cable assembly with Mini SAS HD 8x cable plug connectors

Although the topology is supported by this standard and SPL-2, a SAS external cable assembly with Mini SAS HD 8x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL-2.

5.5.4.2.5 SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 90 shows the SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end.

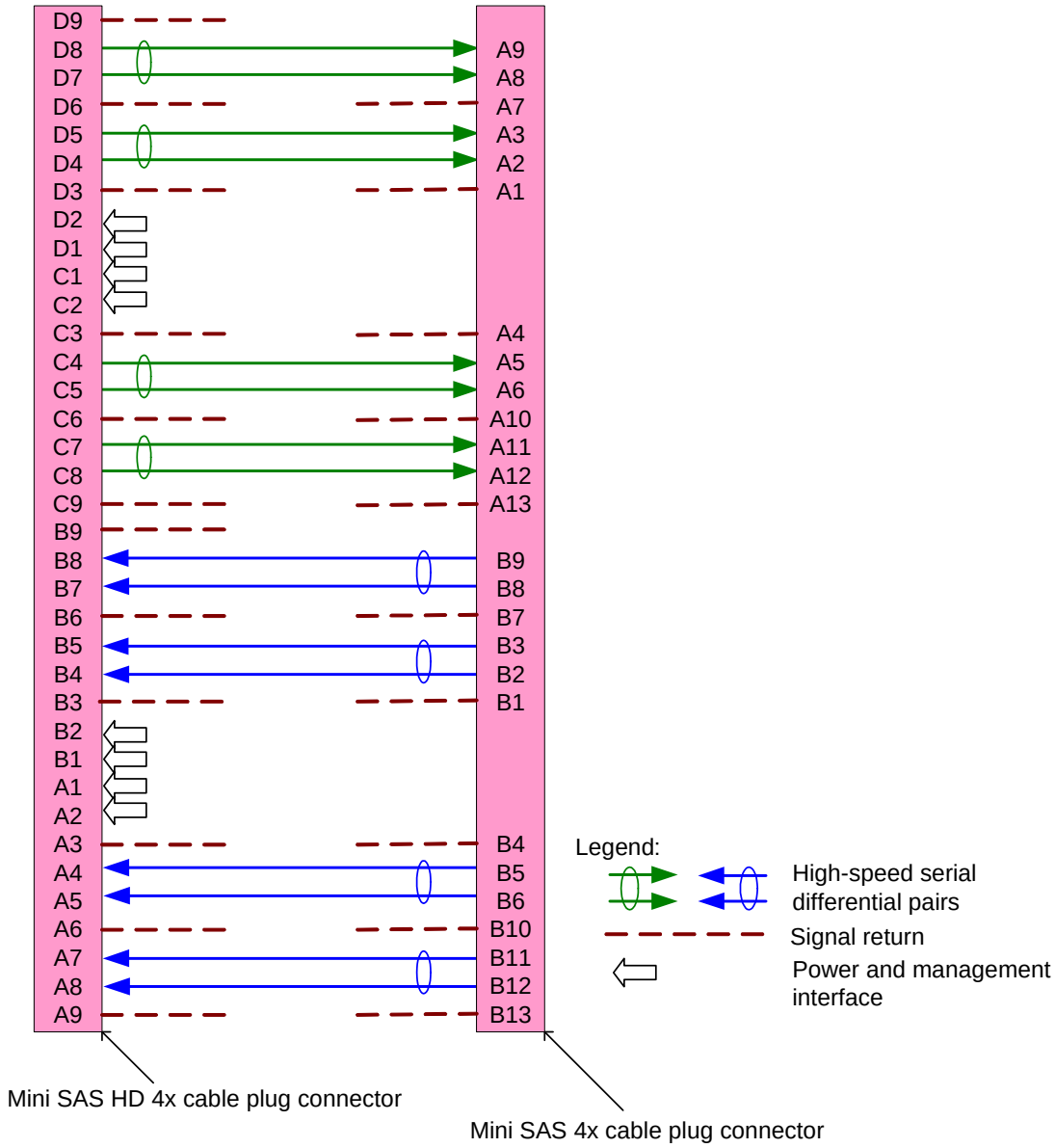

Figure 90 — SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.5.4.2.6 SAS external cable assembly - QSFP+

QSFP+ cable assemblies are defined in SFF-8436. QSFP+ cable assemblies for SAS shall comply with the TxRx connection characteristics specified in this standard (see 5.6).

5.5.5 Backplanes

SAS backplane designs should follow the recommendations in SFF-8460.

5.6 TxRx connection characteristics

5.6.1 TxRx connection characteristics overview

Each TxRx connection shall support a bit error ratio (BER) that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits). The parameters specified in this standard support meeting this requirement under all conditions including the minimum input and output amplitude levels.

A TxRx connection may be constructed from multiple TxRx connection segments (e.g., backplanes and cable assemblies). It is the responsibility of the implementer to ensure that the TxRx connection is constructed from individual TxRx connection segments such that the overall TxRx connection requirements are met. Loss characteristics for individual TxRx connection segments are beyond the scope of this standard.

Each TxRx connection segment shall comply with the impedance requirements detailed in 5.6.2 for the conductive material from which they are formed. A passive equalizer network, if present, shall be considered part of the TxRx connection.

TxRx connections shall be applied only to homogeneous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

5.6.2 TxRx connection general characteristics

Table 24 defines the TxRx connection general characteristics.

Table 24 — TxRx connection general characteristics

Characteristic [a] [b]	Units	Value
Differential impedance (nominal)	ohm	100
Bulk cable or backplane:		
Differential characteristic impedance [d] [e]	ohm	100
Mated connectors:		
Differential characteristic impedance [f]	ohm	100
Passive cable assembly and backplane:		
Maximum propagation delay [c]	ns	53
Minimum $\|S_{DD21}\|$ for internal cable assemblies [g] [h]	dB	-6
Minimum $\|S_{DD21}\|$ for external cable assemblies and backplanes	See 5.6	
Mini SAS 4x active cable assembly:		
Maximum propagation delay [i]	ns	133
Differential characteristic impedance [f]	ohm	100
Managed cable assembly:		
Maximum propagation delay [j]	ns	510
Differential characteristic impedance [f]	ohm	100

[a] All measurements are made through mated connector pairs.

[b] The equivalent maximum TDR rise time from 20 % to 80 % shall be 70 ps. Filtering may be used to obtain the equivalent rise time. The filter consists of the two-way launch/return path of the test fixture, the two-way launch/return path of the test cable, and the software or hardware filtering of the TDR scope. The equivalent rise time is the rise time of the TDR scope output after application of all filter components. When configuring software or hardware filters of the TDR scope to obtain the equivalent rise time, filtering effects of test cables and test fixtures shall be included.

[c] This is based on propagation delay for a 10 m Mini SAS 4x passive cable assembly. See SPL-2 for STP flow control details.

[d] The impedance measurement identifies the impedance mismatches present in the bulk cable or backplane when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the bulk cable or backplane, when present, but includes any intermediate connectors or splices.

[e] Where the bulk cable or backplane has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[f] The characteristic impedance is a measurement reference impedance for the test environment.

[g] An internal cable assembly may be a TxRx connection segment or a full TxRx connection. The full TxRx connection is required to comply with the requirements for intra-enclosure compliance points defined in Figure 111 —.

[h] The range for this frequency domain measurement is 10 MHz to 4 500 MHz.

[i] This is based on propagation delay for a 25 m Mini SAS 4x active cable assembly. TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-2 for STP flow control details.

[j] This is based on propagation delay for a 100 m optical cable. Managed cables shall report the propagation delay through the cable management interface (see 5.5.3.4.2.7). TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-2 for STP flow control details.

5.6.3 Passive TxRx connection S-parameter limits

S-parameters limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}$(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 25 defines the maximum limits for S-parameter of the passive TxRx connection.

Table 25 — Maximum limits for S-parameters of the passive TxRx connection

Characteristic [a b c d]	L [e] (dB)	N [e] (dB)	H [e] (dB)	S [e] (dB / decade)	f_{min} [e] (MHz)	f_{max} [e] (GHz)
[20 × $\log_{10}$($\lvert S_{CD21} \rvert$)] - [20 × $\log_{10}$($\lvert S_{DD21} \rvert$)]	-10			0	100	6.0
Maximum near-end crosstalk (NEXT) for each receive signal pair [f g]	-26			0	100	6.0
20 × $\log_{10}$($\lvert S_{DD22} \rvert$)	-10	-7.9	0	13.3	100	6.0
20 × $\log_{10}$($\lvert S_{CD22} \rvert$)	-26	-12.7	-10	13.3	100	6.0
20 × $\log_{10}$($\lvert S_{CD21} \rvert$)	-18			0	100	6.0

[a] All measurements are made through mated connector pairs.
[b] The range for this frequency domain measurement is 100 MHz to 6 000 MHz.
[c] Specifications apply to any combination of cable assemblies and backplanes that are used to form a passive TxRx connection.
[d] $\lvert S_{CC22} \rvert$ and $\lvert S_{DC22} \rvert$ are not specified.
[e] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.
[f] NEXT is not an S-parameter.
[g] Determine all valid aggressor/victim near-end crosstalk transfer modes. Over the complete frequency range of this measurement, determine the sum of the crosstalk transfer ratios, measured in the frequency domain, of all crosstalk transfer modes. To remove unwanted bias due to test fixture noise, crosstalk sources with magnitudes less than -50 dB (e.g., -60 dB) at all frequencies may be ignored. The following equation details the summation process of the valid near-end crosstalk sources:

$$TotalNEXT(f) = 10 \times \log \sum_{1}^{n} 10^{\langle NEXT(f)/10 \rangle}$$

where:
f frequency; and
n number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

Editor's Note 1: Need to determine if NEXT, FEXT, and other limits are appropriate for 12Gps.

Figure 91 shows the passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits defined in table 25.

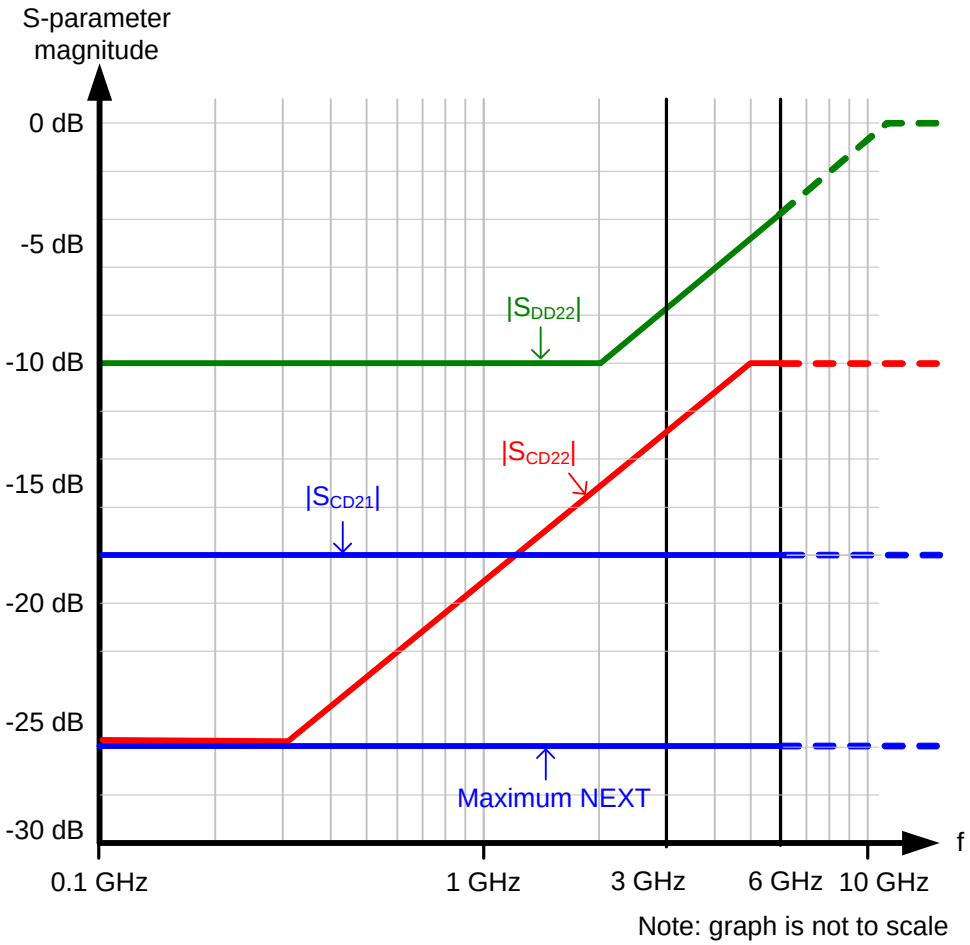

Figure 91 — Passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits

5.6.4 Passive TxRx connection characteristics for untrained 1.5 Gbps, 3 Gbps, and 6 Gbps

For untrained 1.5 Gbps and 3 Gbps, each external passive TxRx connection shall be designed such that its loss characteristics are less than the loss of the TCTF test load plus ISI at CT at 3 Gbps (see figure 102 in 5.7.3) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbps and 3 Gbps, each internal passive TxRx connection shall be designed such that its loss characteristics are less than:

a) the loss of the TCTF test load plus ISI at IT at 3 Gbps (see figure 101 in 5.7.3) over the frequency range of 50 MHz to 3 000 MHz; or
b) if the system supports SATA devices using Gen2i levels (see SATA) but the receiver device does not support SATA Gen2i levels through the TCTF test load (see table 53 in 5.9.5.4), the loss of the low-loss TCTF test load plus ISI (see figure 106 in 5.7.4) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbps and 3 Gbps, each passive TxRx connection shall meet the delivered signal specifications in table 53 (see 5.9.5.4).

For untrained 6 Gbps (i.e., SATA devices using Gen3i levels (see SATA)), then the internal passive TxRx connection should be less than the CIC (see SATA). See SATA for delivered signal specifications.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included in the TxRx connection.

5.6.5 Passive TxRx connection characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, the passive TxRx connection shall support a bit error ratio (BER) that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on simulation results using:

a) S-parameter measurements of the passive TxRx connection;
b) the reference transmitter device (see 5.9.4.6.5); and
c) the reference receiver device (see 5.9.5.7.3).

The simulation shall not include sources of crosstalk. Since simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 92 shows an example circuit for simulation. The specific simulation program used is not specified by this standard. Annex C includes the StatEye program from http://www.stateye.org, which is one such simulation program.

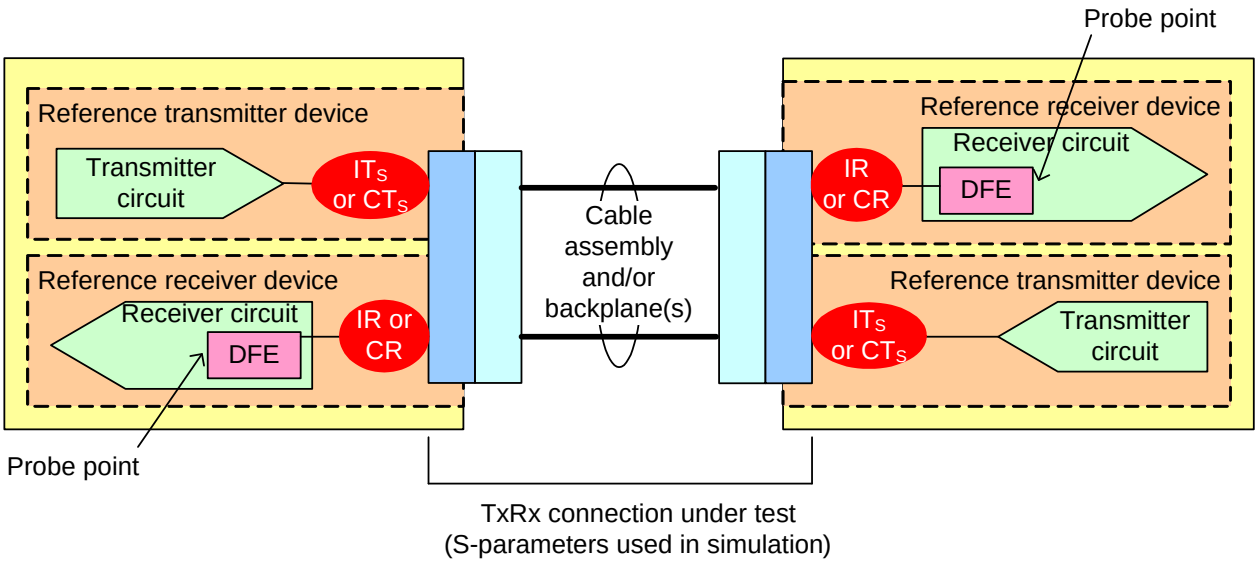

Figure 92 — Example passive TxRx connection compliance testing for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

Table 26 defines the required passive TxRx connection characteristics.

Table 26 — Passive TxRx connection characteristics for trained 6 Gbps

Characteristic	Units	6 Gbps
Minimum voltage [a]	mV(P-P)	84
Maximum TJ [a]	UI	0.64

[a] As reported by simulation of the passive TxRx connection S-parameters with the reference transmitter device and the reference receiver device. Values are reported at a BER of 10^{-15} inside the reference receiver device after equalization at 6 Gbps. This standard does not define values for trained 3 Gbps and 1.5 Gbps. Passive TxRx connections that comply with the 6 Gbps characteristics are expected to operate correctly at slower physical link rates.

For external cable assemblies, these electrical requirements are consistent with using good quality passive Mini SAS 4x cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 10 m long, provided that no other TxRx connection segments are included in the TxRx connection.

A passive TxRx connection supporting trained 1.5 Gbps, 3 Gbps, and 6 Gbps may not support untrained 1.5 Gbps and 3 Gbps and may not support SATA. Trained transceiver devices incorporate features to allow them to operate over the following passive TxRx connections:

a) passive TxRx connections with higher loss than TxRx connections compliant with versions of SAS standards previous to SAS-2;
b) passive TxRx connections defined in this standard for untrained 1.5 Gbps and 3 Gbps (see 5.6.4); and
c) passive TxRx connections supporting SATA.

5.6.6 Passive TxRx connection characteristics for trained 12Gbps

For trained 12 Gbps, the passive TxRx connection shall support a BER that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based onend-to-end simulation results (see 5.8.1) using:

a) S-parameter measurements or model of the passive TxRx connection segment from CT_S to CR or IT_S to IR (see figure 13);
b) S-parameter measurements of the passive connection, S-parameter modelsof the passive connection, or reference S-parameter models (see D.2) from all significant crosstalk aggressors;
c) reference transmitter devices (see 5.9.4.7.3) providing signals the through channel and crosstalk channels with reference equalization coefficients (see 5.8.4) and generating no RJ or TJ;
d) the reference receiver device with optimal DFE weights (see 5.9.5.7.3 and table 27). and
e) reference S-parameter models to complete the simulation schematic (see figure 93), according to the appropriate usage model (see table D.2 in D.2).

The simulation shall include all significant sources of crosstalk. The crosstalk sources shall be modelled as asynchronous to the TxRx connection segment under test (see D.1).

Simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} should yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 93 shows an example TxRx connection for trained 12 Gbps.The TxRx connection segment under test is the segment between CT_S and CR or IT_S and IR. XCS_n represents the crosstalk connection segments, where n is a numerical index identifying multiple crosstalk aggressors.

The specific simulation program used is not specified by this standard.

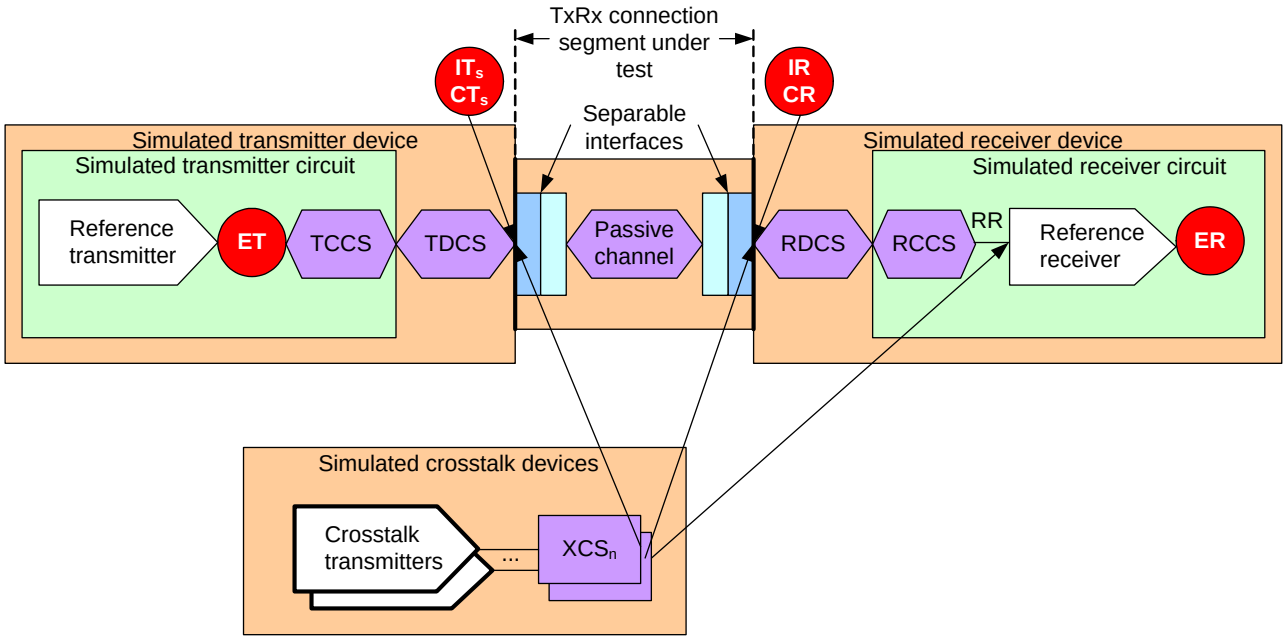

Figure 93 — Example passive TxRx connection compliance testing for trained 12 Gbps

D.1 describes a simulation procedure.

The following reference through transfer functions shall be used for this simulation, according to the appropriate usage model:

a) <usage>_ET_CTs: through between ET and CT_S or between ET and IT_S; and
b) <usage>_CR_RR: through between CR and RR or between IR and RR.

For asymmetrical models, the reverse transfer function between ET and CT_S or between ET and IT_S shall also be used (i.e., <usage>_ET_CTs_rev).

Symmetrical models shall use the same transfer function for both directions (i.e., <usage>_ET_CTs).

For each usage model, four crosstalk aggressors transfer functions are defined for this simulation:

a) <usage>_ET_CTs_FEXT: crosstalk caused by elements between ET and CT_S or between ET and IT_S;
b) <usage>_CR_RR_FEXT: crosstalk caused by elements between CR and RR or between IR and RR;
c) <usage>_CR_RR_NEXT: crosstalk caused by elements between CR and RR or between IR and RR; and
d) <usage>_ET_CTs_NEXT: crosstalk caused by elements between ET and CT_S or between ET and IT_S.

Figure 94 shows the usage of the crosstalk and through files defined for the end-to-end simulation of TxRx connection segments between CT_S and CR or IT_S and IR. The boxes labeled PICS FEXT, PICS NEXT, and PICS indicate measured transfer functions (e.g., S-parameters). The boxes with a dashed boundary and with

labels beginning by <usage> indicate reference transfer functions. <usage> represents a prefix that is set according to the selected usage model (see D.2).

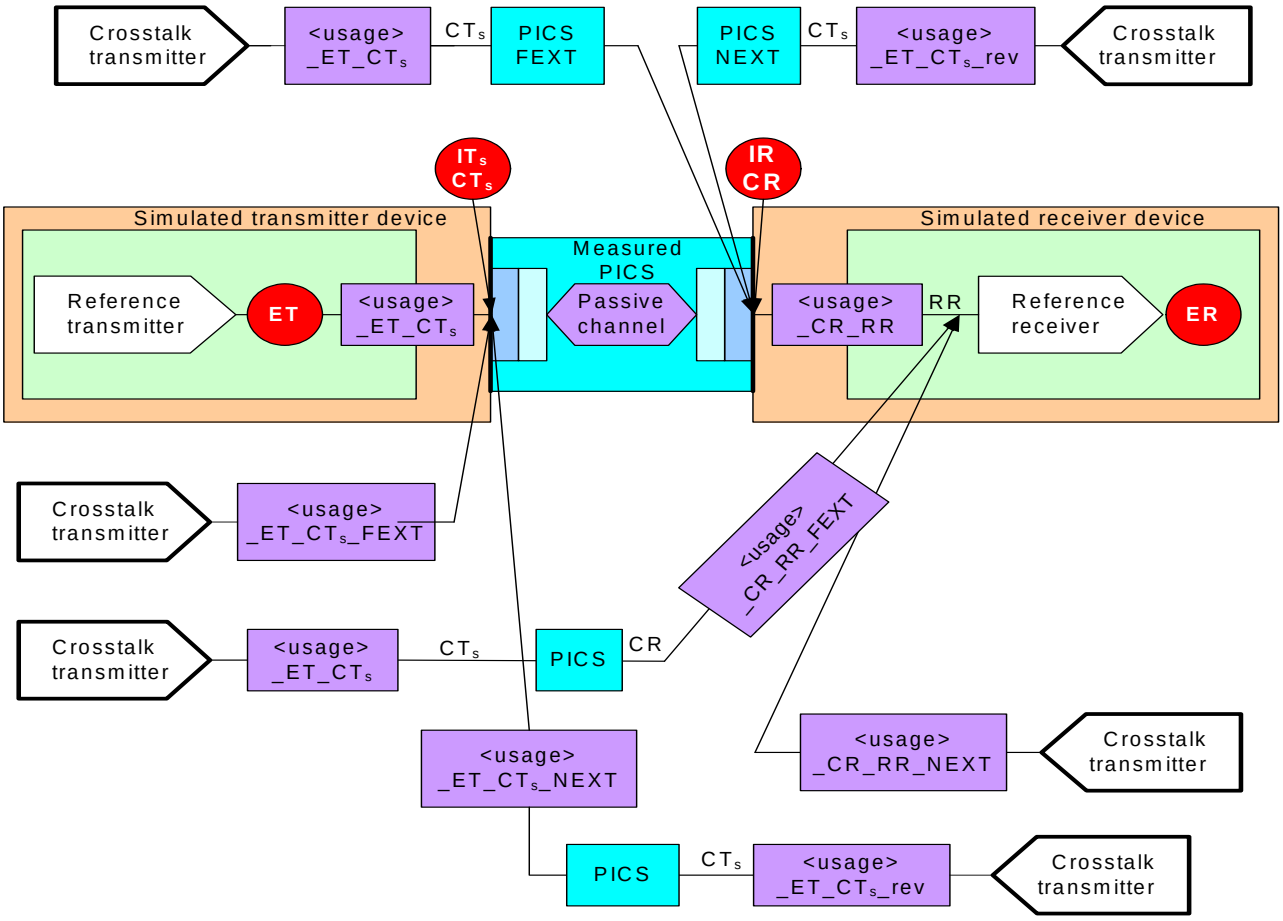

Figure 94 — Passive TxRx connection segment between CT_s and CR or IT_s and IR end-to-end simulation schematic for trained 12 Gbps

Table 27 defines the required passive TxRx connection characteristics. Refer to the reference transmitter device (see 5.9.4.7.3) for definitions of coefficient 1, coefficient 2 and coefficient 3 used in table 27. C1, C2 and C3 represent coefficient 1, coefficient 2 and coefficient 3, respectively.

Table 27 — Passive TxRx connection charateristics for trained 12 Gbps at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a] [b] [c]	V/V	-0.15	0	ET
VMA [d] [e]	mV(P-P)	80	-	ET
Coefficient 3(i.e., C3) [a] [b] [f]	V/V	-0.3	0	ET
Reference pulse response cursor peak-to-peak amplitude [g]	mV(P-P)	72	-	ER
Vertical eye opening to reference pulse response cursor ratio [h] [i] [j]	%	55	-	ER
DFE coefficient amplitude to reference pulse response cursor ratio [k]	%	-75	75	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.
[b] C2 = 1 - |C1| - |C3|.
[c] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.
[d] VMA = $2K_0$ ((C1 + C2 + C3). See 5.9.4.7.3.
[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$((C1' - C1)^2 + (C3' - C3)^2)^{0.5}$

where:
C1' and C3' are values that satisfy the minimum VMA criterion.
[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.
[g] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 113.
[h] The vertical eye opening includes the effects of crosstalk (see D.1).
[i] The end-to-end simulation removes any remaining RJ and TJ (non-ISI) of the transmitter device.
[j] See figure 111.
[k] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(di)) divided by the reference pulse response cursor (see 5.9.5.7.3).

Editor's Note 2: The values in table 27 are based on initial simulations that did not include the complete end-to-end TxRx connection. Final values may be different, but will remain consistent between tables table 27, table 48 and table 62.

For external cable assemblies, these electrical requirements are consistent with using good quality passive Mini SAS HD cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included in the TxRx connection and the total crosstalk is < 50mV (P-P).

5.6.7 TxRx connection characteristics for active cable assemblies

5.6.7.1 Active cable assembly electrical characteristics overview

Active cable assemblies shall support a bit error ratio (BER) that is less than 10^{-12} when used with trained transmitter devices and trained receiver devices defined in Figure 111 —.

In addition to complying with electrical characteristics necessary for the required BER performance, active cable assemblies shall comply with the OOB signaling defined in 5.11. The circuitry incorporated in these cable assemblies preserves D.C. idle with response times that support the OOB signal receiver device idle time detection requirements in table 76 (see 5.11.3).

5.6.7.2 Active cable assembly output electrical characteristics for trained 6 Gbps

Table 28 defines active cable assembly output electrical characteristics for trained 6 Gbps.

Table 28 — Active cable assembly output electrical characteristics for trained 6 Gbps

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage	mV (P-P)	400		1 200
RJ [a b d]	UI			0.22
TJ [a c d]	UI			0.56

[a] Based on TX input per table 37 (see 5.9.4.6.1) and recommended TX interoperability settings per table 40 (see 5.9.4.6.4).
[b] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] The TJ measurement shall be performed with at least 58 dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC enabled.
[d] The measurement shall include the effects of the JTF (see 5.9.3.2).

For active cable assemblies, these characteristics are consistent with good quality half-active (i.e., with circuitry only on the receive end of the assembly) cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 25 m long, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbps and 3 Gbps. Active cables that comply with trained 6 Gbps characteristics should operate within the specified error rate at slower physical link rates.

5.6.7.3 Active cable assembly S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [\, L, \min [\, H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz}) \,] \,]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 29 defines the maximum limits for S-parameters of the active cable assembly.

Table 29 — Maximum limits for S-parameters for active cable assemblies

Characteristic [b] [d]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\|S_{CC22}\|$ [a]	-6.0	-5.0	0	13.3	100	6.0
$\|S_{DD11}\|$, $\|S_{DD22}\|$ [a]	-10	-7.9	0	13.3	100	6.0
$\|S_{CD11}\|$, $\|S_{CD22}\|$ [a]	-20	-12.7	-10	13.3	100	6.0

[a] For $\|S_{CC22}\|$, $\|S_{DD22}\|$ and $\|S_{CD22}\|$ measurements, the transmitter device attached to the active cable assembly under test shall transmit a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See E.11.4.4 and E.11.4.5

[b] $\|S_{CC11}\|$, $\|S_{DC11}\|$ and $\|S_{DC22}\|$ are not specified.

[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

[d] Power shall be applied to the active cable assembly during these measurements.

Figure 95 shows the active cable assembly **$|S_{CC22}|$, $|S_{DD11}|$, $|S_{DD22}|$, $|S_{CD11}|$** and **$|S_{CD22}|$** limits defined in table 29.

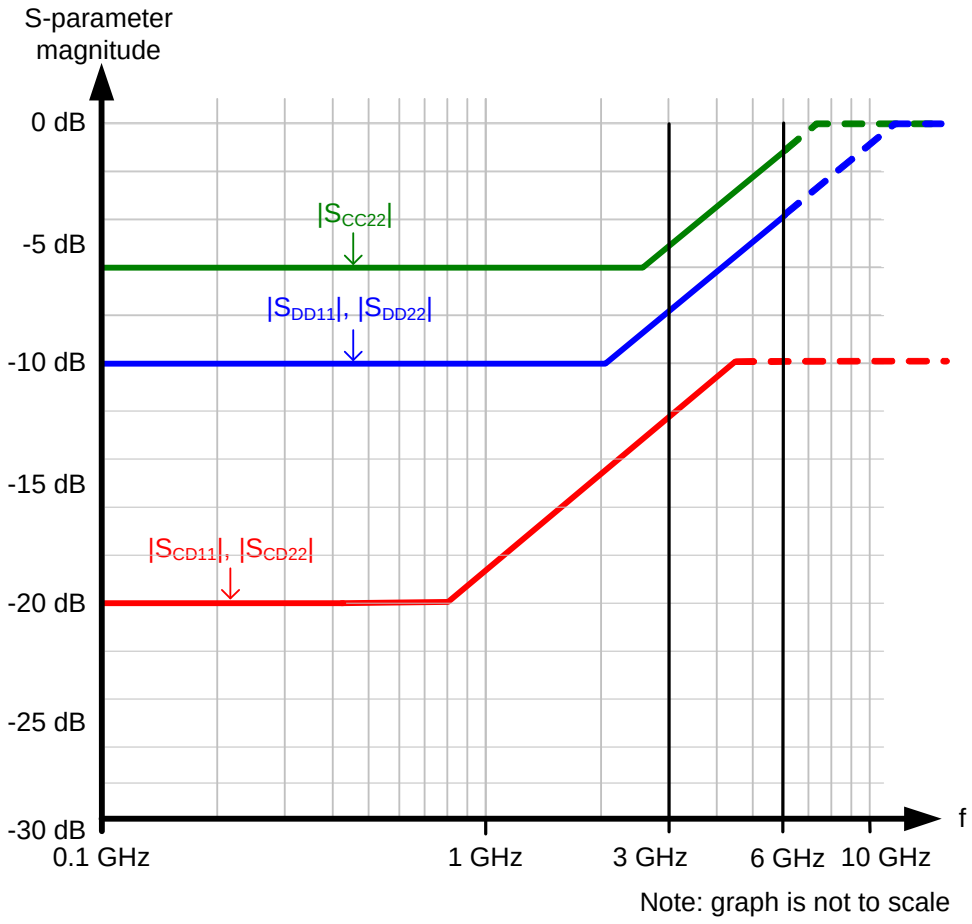

Figure 95 — Active cable S-parameter limits

Editor's Note 3: Add sections for 12G passive cables.

5.6.7.4 Active cable assembly electrical characteristics for 12 Gbps

5.6.7.4.1 Active cable assembly electrical characteristics overview for 12 Gbps

Active cable assemblies supporting 12Gbps operation shall comply with OOB in the optical mode (see 5.11) and shall support pass through of SSC. The optical mode does not support transmitter training. The circuitry incorporated in these cable assemblies preserves OOB signals with response times that support the OOB signal receiver device detection requirements in table 76 (see 5.11.3).

5.6.7.4.2 Active cable assembly electrical characteristics overview for 12 Gbps

Figure 96 describes the eye mask used to calibrate the input in an active cable assembly at CT_S to test the output of an active cable assembly at CR for 12 Gbps.

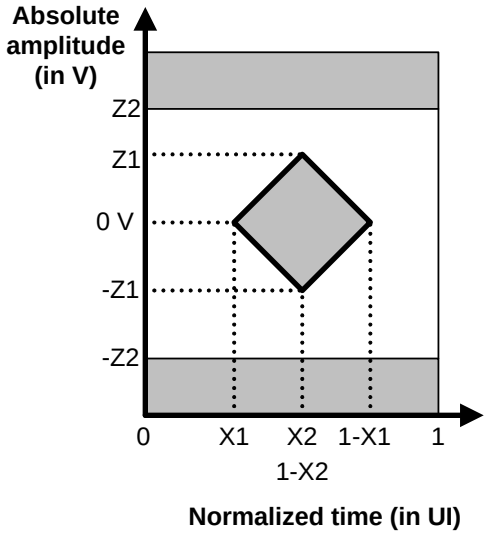

Figure 96 — Active cable eye mask for 12 Gbps

Table 30 defines the signal input and output characteristics for an active cable assembly for 12 Gbps.

Table 30 — Active cable assembly electrical characteristics for 12 Gbps

Signal characteristic	Units	CT_S	CR
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 96) [a]	mV(P-P)	1200	1200
Minimum eye opening (i.e., 2 × Z1 in figure 96) [a]	mV(P-P)	200	190
Maximum half of TJ (i.e., X1 in figure 96) [a] [b] [c]	UI	0.175	0.26
Maximum RJ [a] [c] [d]	UI	0.15	0.27
Center of bit time (i.e., X2 in figure 96)	UI	0.5	0.5

[a] All crosstalk sources shall be active with representative traffic during the measurement.
[b] The TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC enabled for a period of at least 33.3̄ s (i.e., a full SSC cycle).
[c] The measurement shall include the effects of the JTF (see 5.9.3.2).
[d] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.

For active cable assemblies, these characteristics are consistent with good quality full-active cable assemblies (i.e., with circuitry on both ends of each differential signal pair of the cable assembly) constructed with shielded twinaxial cable with 26 AWG solid wire up to 15 m or optical cable assemblies up to 100 m, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbps and 3 Gbps. Active cable assemblies that comply with active cable assembly electrical characteristics for 12 Gbps characteristics should also comply with active cable assembly electrical characteristics for 6 Gbps (see 5.6.7) with optical mode enabled and should operate within the specified bit error ratio at slower physical link rates.

5.7 Test loads

5.7.1 Test loads overview

This standard uses a test load methodology to specify transmitter device signal output characteristics (see 5.9.4.4 and 5.9.4.5) and delivered signal characteristics (see 5.9.5.4). This methodology specifies the signal as measured at specified probe points in specified test loads.

For untrained 1.5 Gbps and 3 Gbps (e.g., the physical link rate is negotiated in Final-SNW (see SPL-2) or the physical link is SATA), the test loads used by the methodology are:

a) zero-length test load (see 5.7.2): used for testing transmitter device compliance points and receiver device compliance points;
b) transmitter compliance transfer function (TCTF) test load (see 5.7.3): used for testing transmitter device compliance points;
c) low-loss TCTF test load (see 5.7.4): used for testing transmitter device compliance points if SATA devices using Gen2i levels (see SATA) are supported and the SAS receiver device does not support the signal levels received through a full TCTF test load (see 5.7.3); and
d) CIC (see SATA): used for testing transmitter device compliance points if SATA devices using Gen3i levels (see SATA) are supported.

For trained (e.g., the physical link rate is negotiated in Train-SNW (see SPL-2)) 1.5 Gbps, 3 Gbps, and 6 Gbps, the test loads used by the methodology are:

a) zero-length test load (see 5.7.2): used for:
   A) testing transmitter device compliance points;
   B) testing receiver device compliance points; and
   C) used with a reference receiver device (see 5.9.5.7.3) in simulation to determine the delivered signal; and
b) reference transmitter test load (see 5.7.5): used with a reference receiver device (see 5.9.5.7.3) in simulation to determine the delivered signal.

Physical positions denoted as probe points identify the position in the test load where the signal properties are measured, but do not imply that physical probing is used for the measurement. Physical probing may be disruptive to the signal and should not be used unless verified to be non-disruptive.

5.7.2 Zero-length test load

Figure 97 shows the zero-length test load as used for testing a transmitter device compliance point.

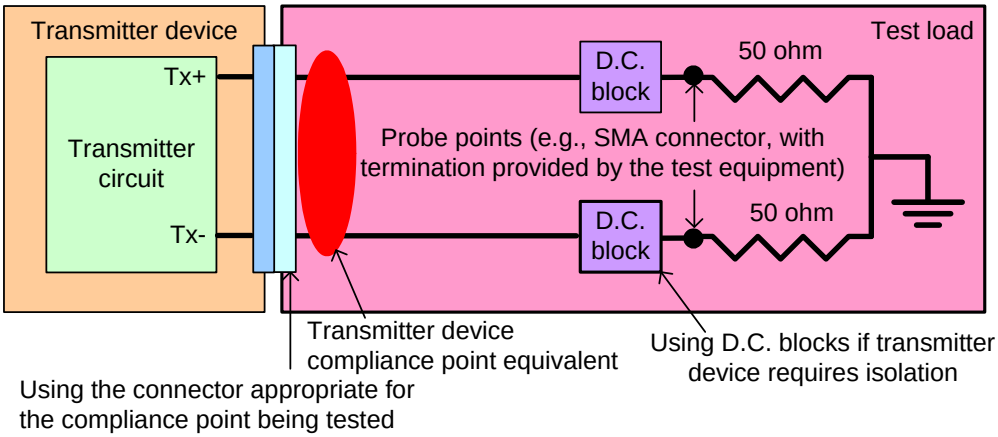

Figure 97 — Zero-length test load for transmitter device compliance point

Figure 98 shows the zero-length test load as used for testing a receiver device compliance point.

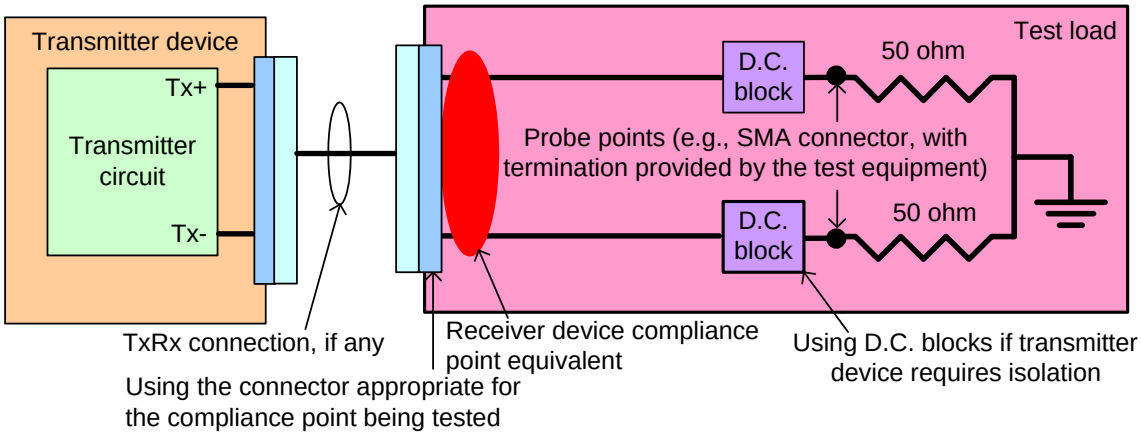

Figure 98 — Zero-length test load for receiver device compliance point

Figure 97 and figure 98 show ideal designs. Implementations may include:

a) insertion loss between the compliance and probe points; and
b) return loss due one or more impedance mismatches between the compliance point and 50 ohm termination points.

Not shown are non-ideal effects of the test equipment raw measurements (e.g., additional insertion loss and return loss). For de-embedding methods to remove non-ideal effects see Annex E.

Usage of fixturing and test equipment shall comply with the requirements defined in this subclause. The requirements in this subclause include the combined effects of the fixturing and test equipment.

The zero-length test load is defined by a set of S-parameters (see E.11). Only the magnitude of $S_{DD21}(f)$ and the magnitude of $S_{DD11}(f)$ are specified by this standard.

The zero-length test load, including all fixturing and instrumentation required for the measurement, shall comply with the following equations:

For 50 MHz < f ≤ 6.0 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.0 \times 10^{-6} \times f^{0.5}) + (2.8 \times 10^{-11} \times f) + (5.3 \times 10^{-21} \times f^{2})) - 0.2$ dB

$|S_{DD11}(f)| \leq -15$ dB

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$;

$|S_{DD11}(f)|$ magnitude of $S_{DD11}(f)$; and

f signal frequency in Hz.

Figure 99 shows the allowable $|S_{DD21}(f)|$ of a zero-length test load and the $|S_{DD21}(f)|$ of a sample zero-length test load.

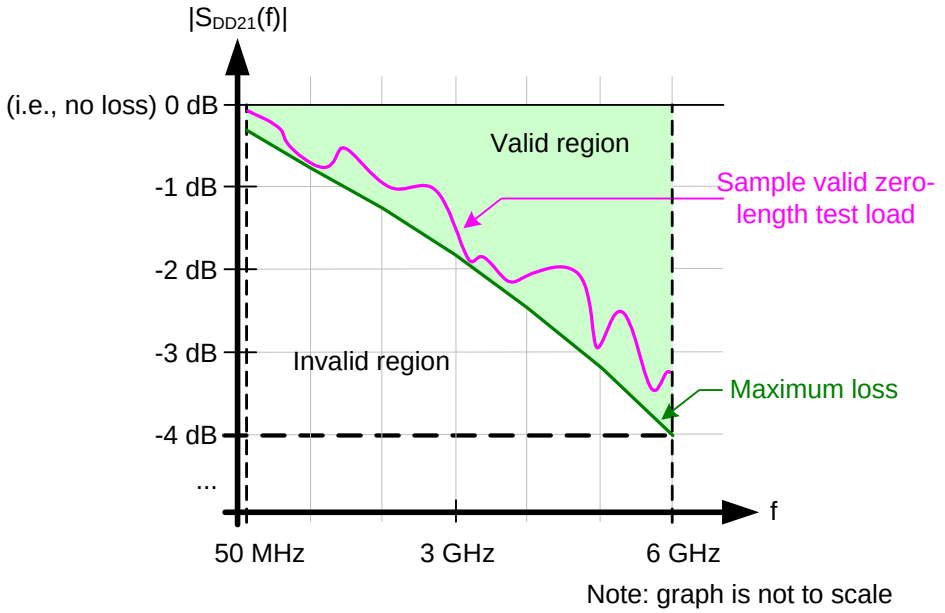

Figure 99 — Zero-length test load $|S_{DD21}(f)|$ requirements

5.7.3 TCTF test load

Figure 100 shows the TCTF test load. This test load is used for untrained 1.5 Gbps and 3 Gbps characterization.

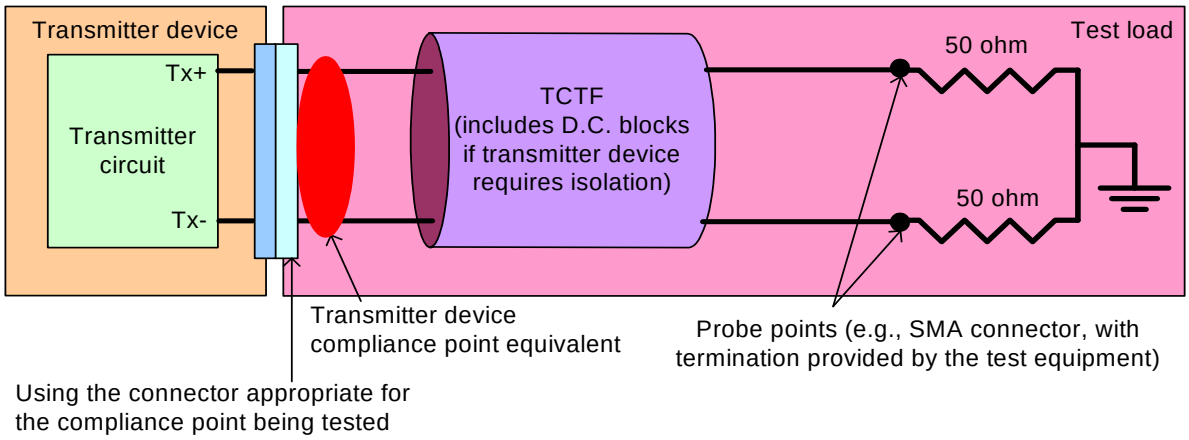

Figure 100 — TCTF test load

The TCTF test load shall meet the requirements in 5.6.2. The nominal impedance shall be the target impedance.

The TCTF test load is defined by a set of S-parameters (see E.11). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

For testing an untrained 3 Gbps transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^{2}))$ dB

and for 3.0 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq -10.9$ dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 300 \text{ MHz})| - |S_{DD21}(f = 1\,500 \text{ MHz})| > 3.9$ dB

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 101 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 3 Gbps.

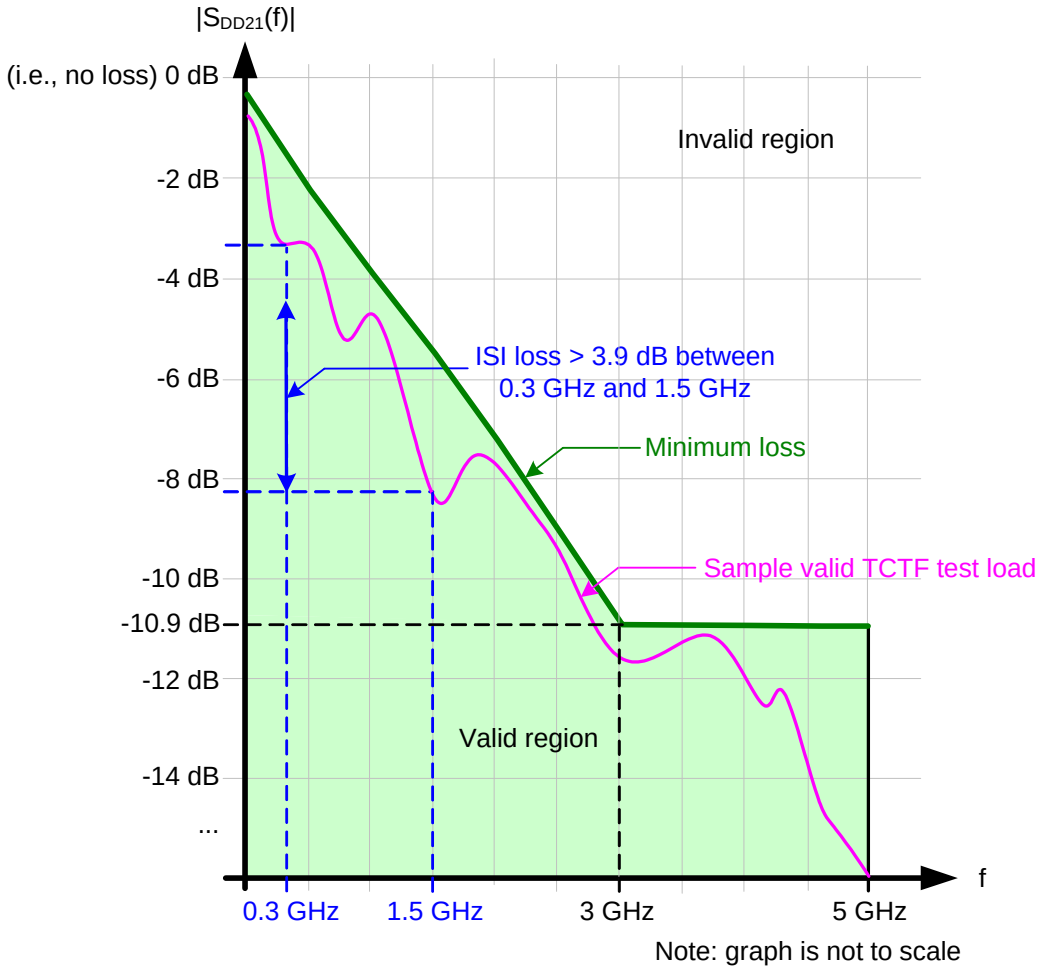

Figure 101 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 3 Gbps

For testing an untrained 3 Gbps transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f))$ dB

and for 3.0 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq -10.7$ dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 300\ MHz)| - |S_{DD21}(f = 1\ 500\ MHz)| > 3.9\ dB$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 102 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 3 Gbps.

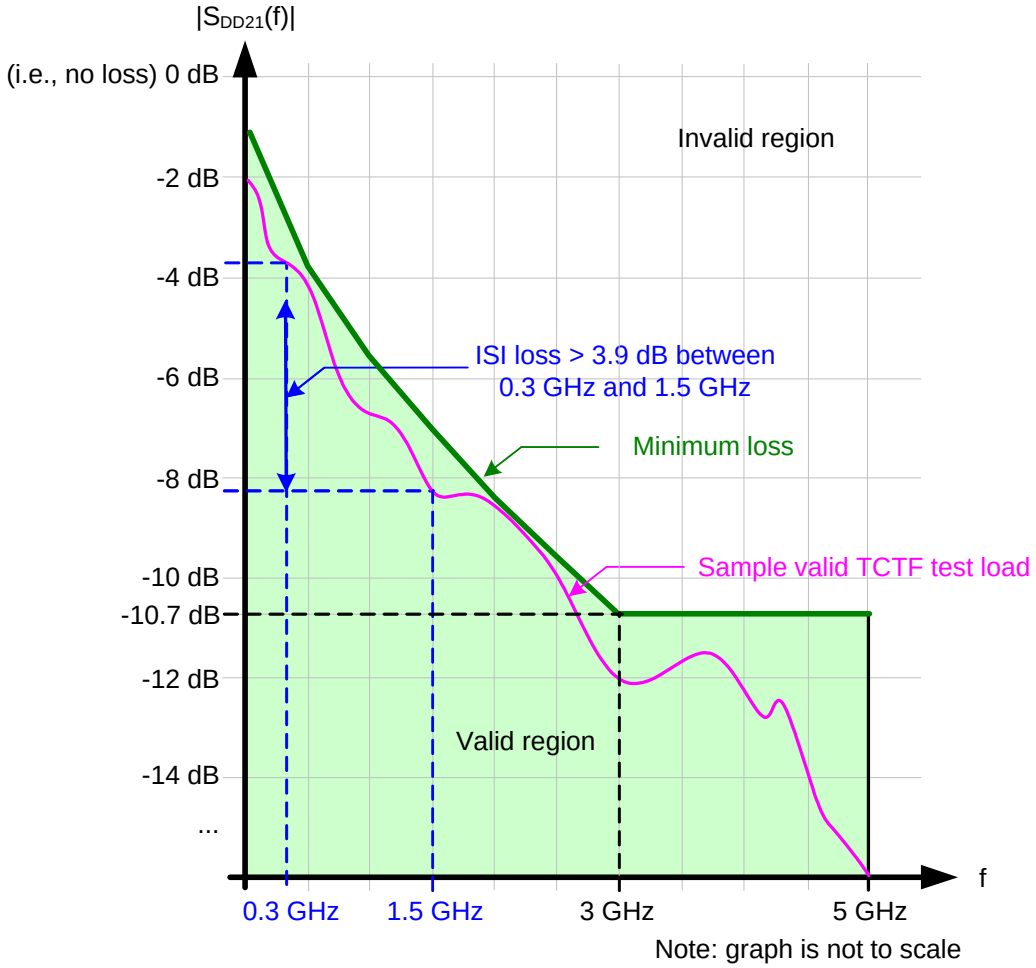

Figure 102 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 3 Gbps

For testing an untrained 1.5 Gbps transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^{2}))\ dB$

and for 1.5 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq -5.4\ dB$

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 150\ MHz)| - |S_{DD21}(f = 750\ MHz)| > 2.0\ dB$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 103 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 1.5 Gbps.

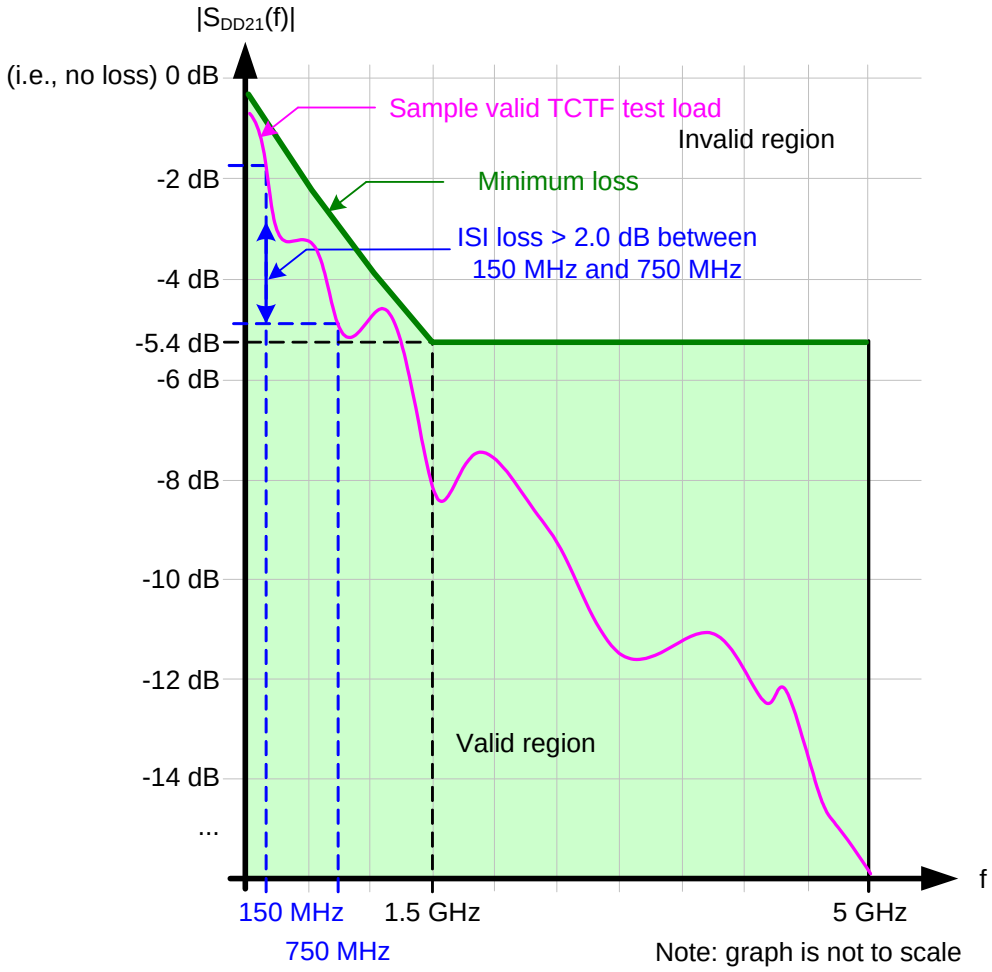

Figure 103 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 1.5 Gbps

For testing an untrained 1.5 Gbps transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f)) \text{ dB}$$

and for 1.5 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -7.0 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 150 \text{ MHz})| - |S_{DD21}(f = 750 \text{ MHz})| > 2.0 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 104 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 1.5 Gbps.

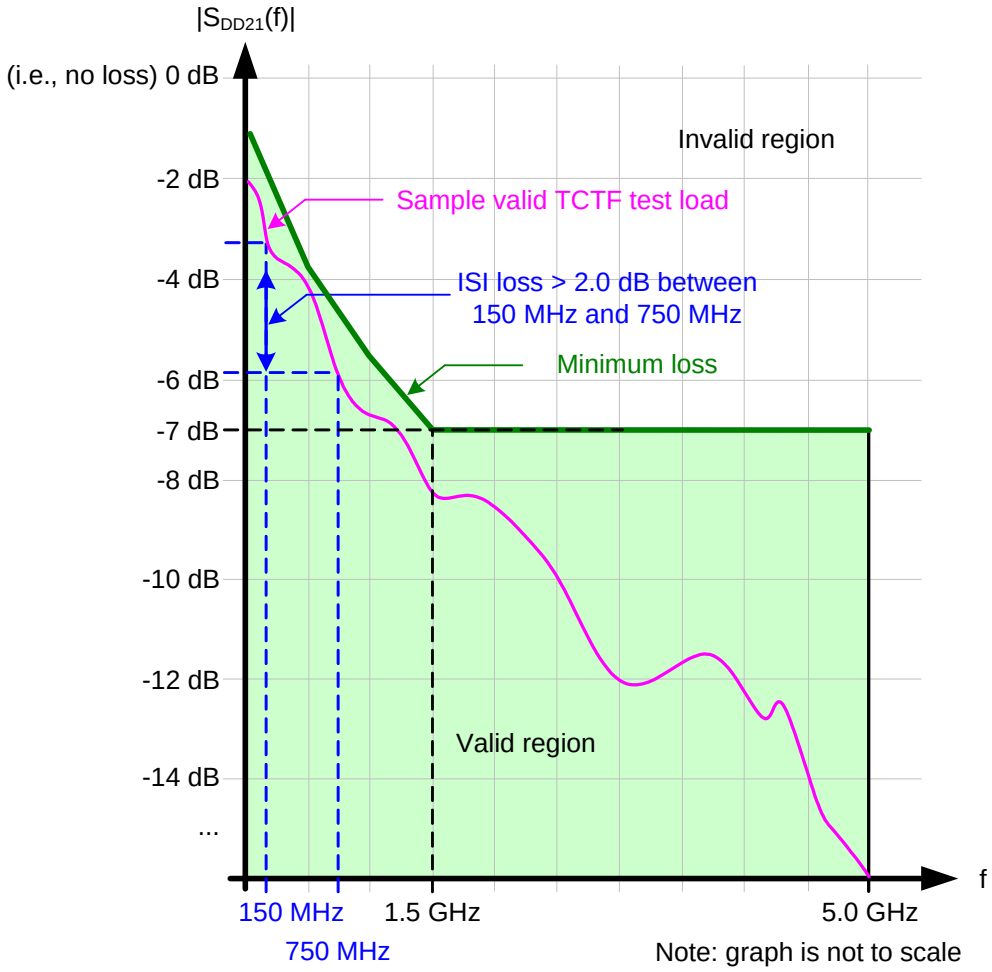

Figure 104 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 1.5 Gbps

5.7.4 Low-loss TCTF test load

Figure 105 shows the low-loss TCTF test load. This test load is used for untrained 1.5 Gbps and 3 Gbps characterization.

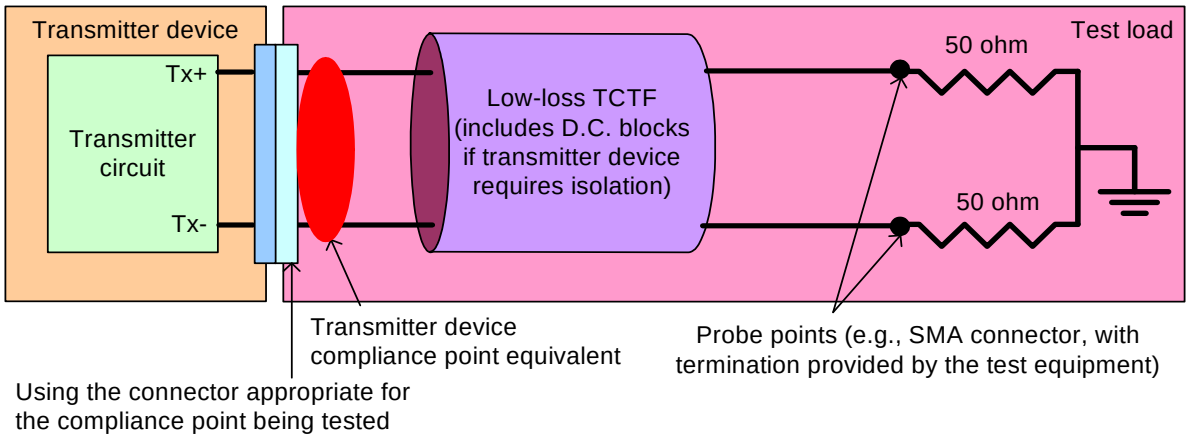

Figure 105 — Low-loss TCTF test load

The low-loss TCTF test load shall meet the requirements defined in 5.6.2. The nominal impedance shall be the target impedance.

The low-loss TCTF test load is defined by a set of S-parameters (see E.11). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

The low-loss TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((2.2 \times 10^{-6} \times f^{0.5}) + (6.9 \times 10^{-11} \times f) + (1.1 \times 10^{-20} \times f^{2})) \text{ dB}$$

for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -3.7 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300 \text{ MHz})| - |S_{DD21}(f = 1\,500 \text{ MHz})| > 1.3 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 106 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a low-loss TCTF test load and the $|S_{DD21}(f)|$ of a sample low-loss TCTF test load.

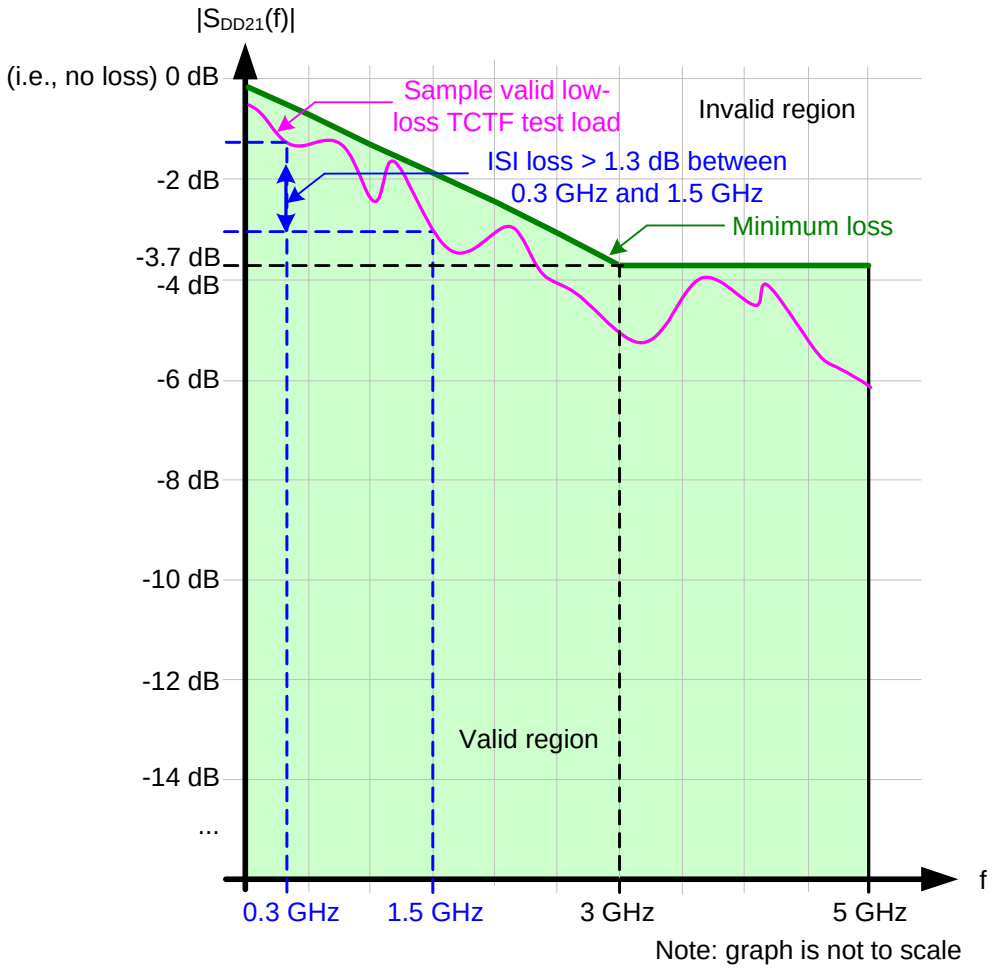

Figure 106 — Low-loss TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements

5.7.5 6Gbps Reference transmitter test load

The reference transmitter test load is a set of parameters defining the electrical performance characteristics of a 10 m Mini SAS 4x cable assembly, used:

a) in simulation to determine compliance of a transmitter device (see 5.9.4.6); and
b) as a representative component of an ISI generator used to determine compliance of a receiver device (see 5.9.5.7.6).

The following Touchstone model of the reference transmitter test load is included with this standard:

a) SAS2_transmittertestload.s4p.

See Annex F for a description of how the Touchstone model was created.

Figure 107 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

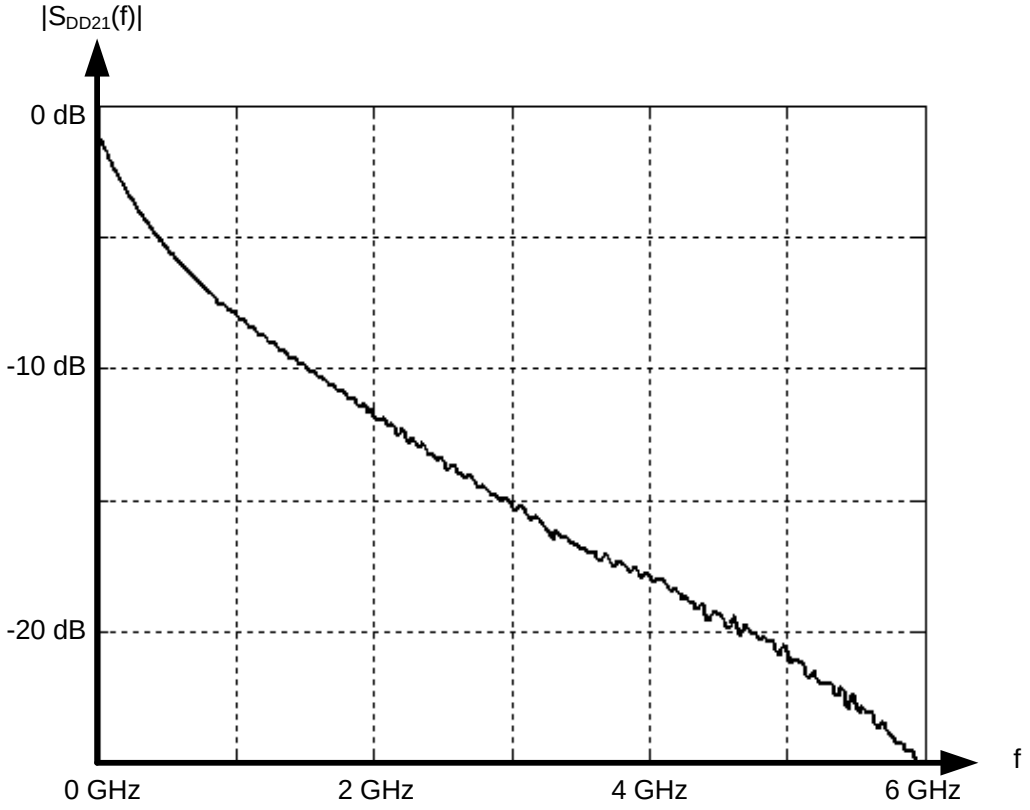

Figure 107 — Reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz

Figure 108 shows the reference transmitter test load pulse response.

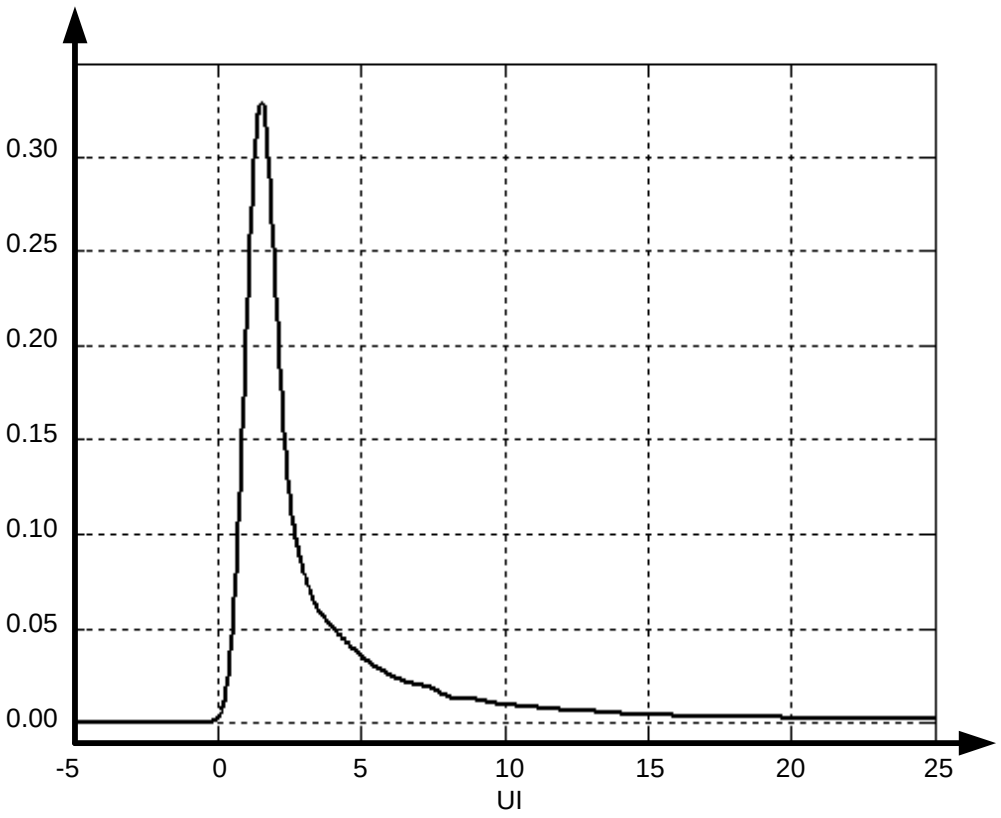

Figure 108 — Reference transmitter test load pulse response

The following impulse response model of the reference transmitter test load is included with this standard:

a) sas2_stressor_6g0_16x.txt.

Figure 109 shows the reference transmitter test load impulse response found in the sas2_stressor_6g0_16x.txt.

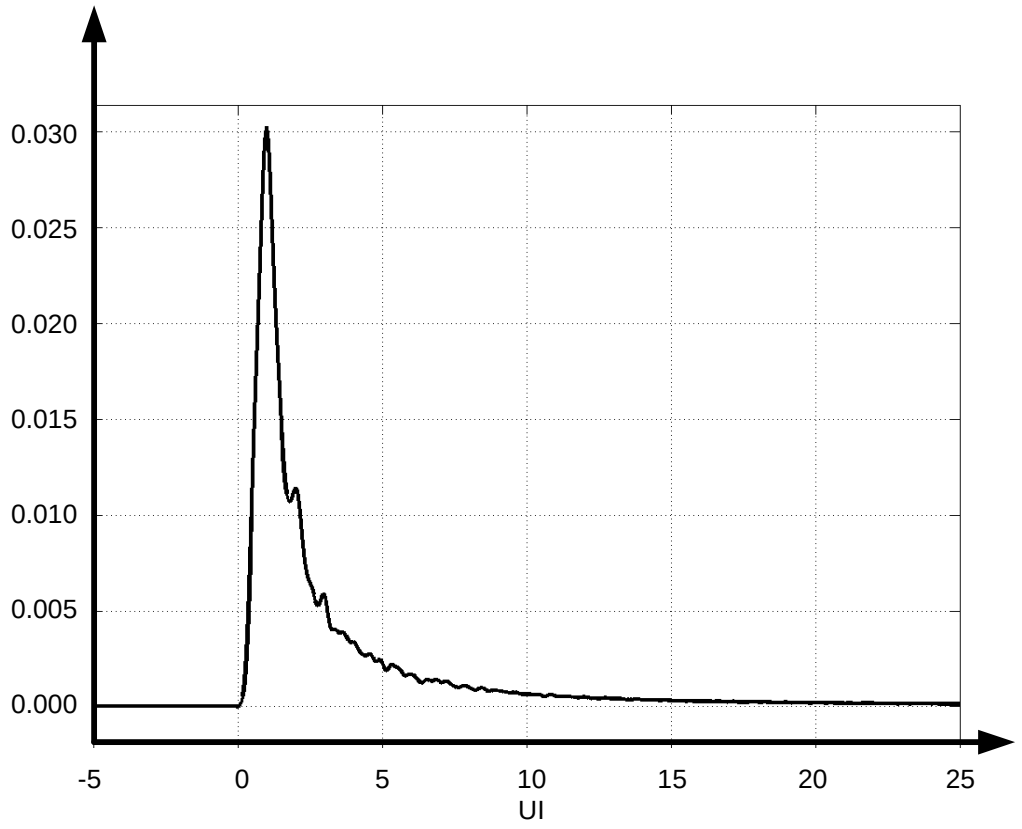

Figure 109 — Reference transmitter test load impulse response

Figure 110 shows the reference transmitter test load repeating 0011b or 1100b pattern (e.g., D24.3) response.

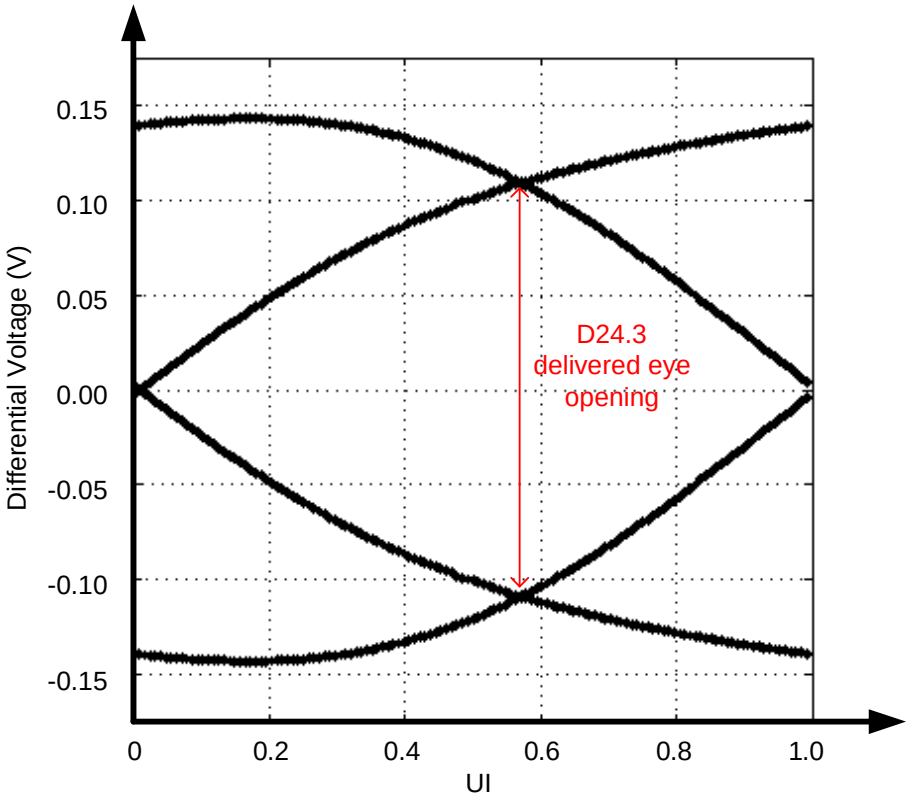

Figure 110 — Reference transmitter test load D24.3 response

5.8 End-to-end simulation for trained 12 Gbps

5.8.1 End-to-end simulation for trained 12 Gbps overview

End-to-end simulation shall be used to verify characteristics of:

a) transmitter devices connected to passive TxRx connections (see 5.9.4.7.4);
b) passive TxRx connections 5.6.6; and
c) ISI generators providing the stressed receiver signal input for receiver devices connected to passive TxRx connections (see 5.9.5.7.6.6)

The specific end-to-end simulation procedures defined in 5.9.4.7.4, 5.6.6 and 5.9.5.7.6.6 follow this general procedure:

1) capture the signal from a transmitter device without SSC into a zero-length test load, or model the transmitter using the reference transmitter (see 5.9.4.7.3);
2) connect passive TxRx connection segments, crosstalk, reference transmitter and reference receiver according to the reference end-to-end simulation schematic (see 5.8.2, D.3, D.4, and D.5);
3) set the transmitter reference equalization (see 5.8.3) and receiver reference DFE equalization (see 5.9.5.7.3); and
4) perform a linear simulation, including the effects of edge rates, ISI and crosstalk (see D.1).

The end-to-end simulation uses a reference transmitter with RJ and TJ set to zero. RJ and TJ and non-linear behavior present in the captured signal used for simulation are removed by the simulation process. Margins for these effects are provided in the required simulation characteristics. The simulation characteristics are processed at a BER of 10^{-15}.

Crosstalk transmitters are simulated using reference transmitters. These reference transmitters shall be set to the characteristics of table D.1 (see D.1). The crosstalk transmitters shall be asynchronous to the data sent to the channel under test.

Characteristics are measured from the simulation at specified measurement points for the usage model and characterization type (see table 48 in 5.9.4.7.4, table 27 in 5.6.6, and table 62 in 5.9.5.7.6.6). Figure 111 shows an example of the reference pulse response cursor and vertical eye opening from an eye diagram derived from output of the simulation.

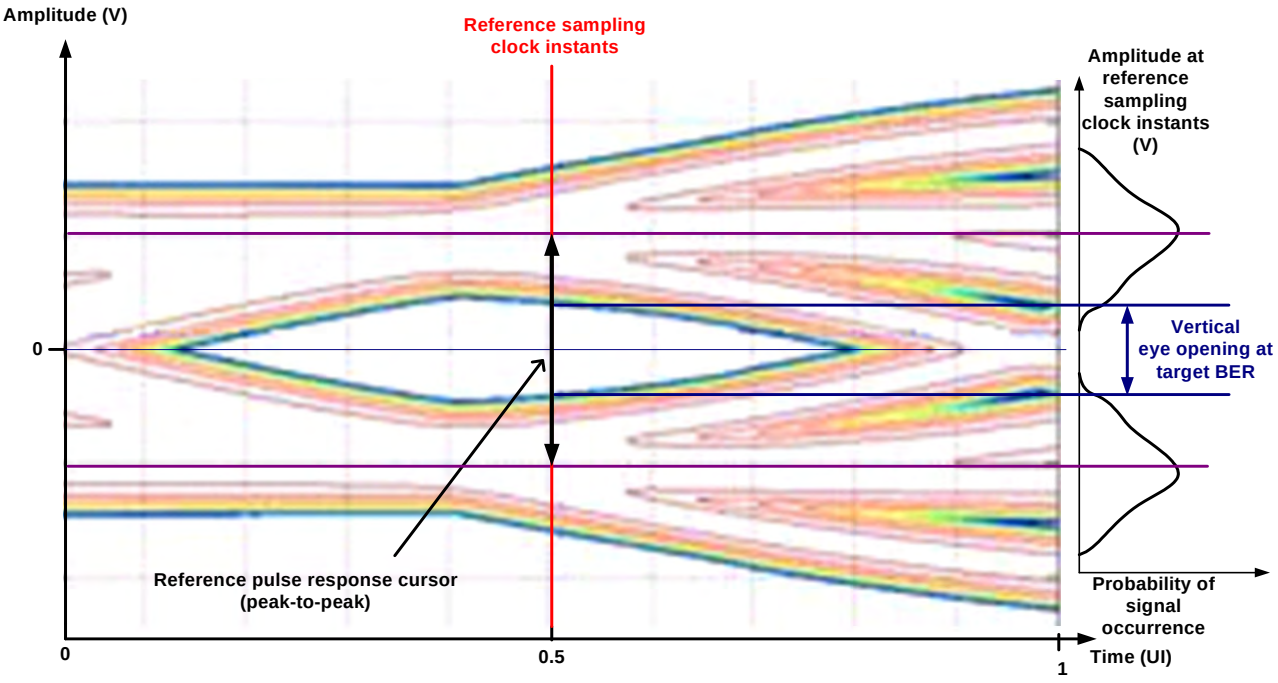

Figure 111 — Simulated vertical eye opening and reference pulse response cursor

5.8.2 Usage models for end-to-end simulation for trained 12 Gbps

A set of transfer functions is required to complement the measured S-parameter or captured signal to provide an end-to-end simulation model. Table D.2 (see D.2) describes the different S-parameter files that shall be used for each usage model, with their associated measurement points.

Each device or passive TxRx connection segment shall be simulated with the appropriate usage model (see D.2), according to its type (i.e., transmitter device, receiver device or passive TxRx connection segment).

The S-parameter files provided in this standard use the port mapping of E.11.3. The FEXT and NEXT S-parameters are extracted as shown in figure 112.

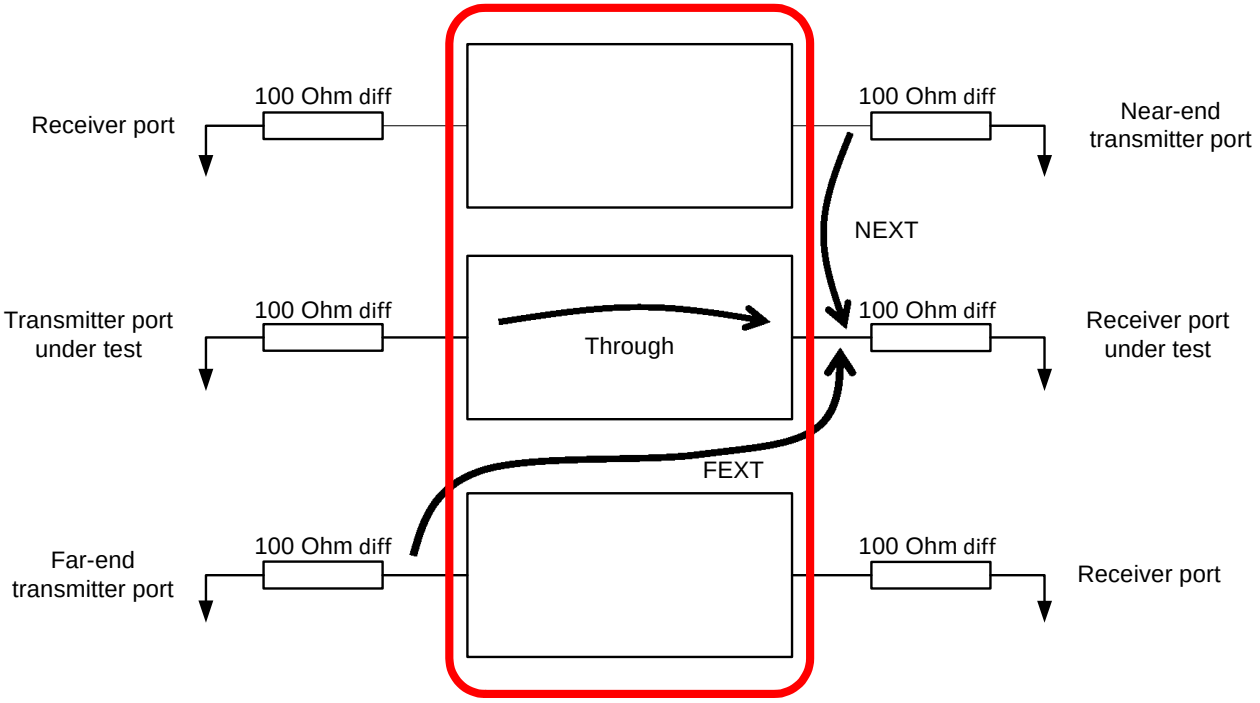

Figure 112 — NEXT and FEXT measurement definition

D.3, D.4, and D.5 describe the schematics that shall be used for end-to-end simulations.

5.8.3 Reference transmitter equalization for trained 12 Gbps

The reference transmitter equalization shall be computed using the following procedure, which requires the unequalized pulse response of the TxRx connection between ET and the input of the reference receiver (i.e., RR) (see D.2). Extraction of pulse responses from captured signals or transfer functions is beyond the scope of this standard. An example is provided in SAS3_EYEOPENING (see SAS3.zip).

Editor's Note 4: Sample S-parameter files and SAS3_EYEOPENING are under development and not included in SAS3r04.zip

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The reference transmitter equalization procedure is as follows:

1) compute the reference sampling instant from the un-equalized pulse response between ET and RR (see figure 113);
2) set coefficient 2 (i.e., C2) of a reference transmitter to 1 and K0 to 1;
3) provide the un-equalized pulse response between ET and RR as the input of the reference transmitter, and compute the coefficient 1 and coefficient 3 (i.e., C1 and C3) that result in a pulse response with the smallest sum of squared error to an ideal pulse, at instants separated from the reference sampling instant by integer multiples of a one-UI period (see figure 114);
4) compute an equalized pulse response by convolving the coefficients obtained in steps 2) and 3) with the un-equalized pulse response between ET and RR;
5) compute the reference sampling instant from the equalized pulse response;
6) repeat steps 2) through 5) until the coefficients and sampling point converge (see figure 115); and

7) normalize the final coefficients found in steps 3) and 4) by dividing them by (|C1| + |C3| + 1).

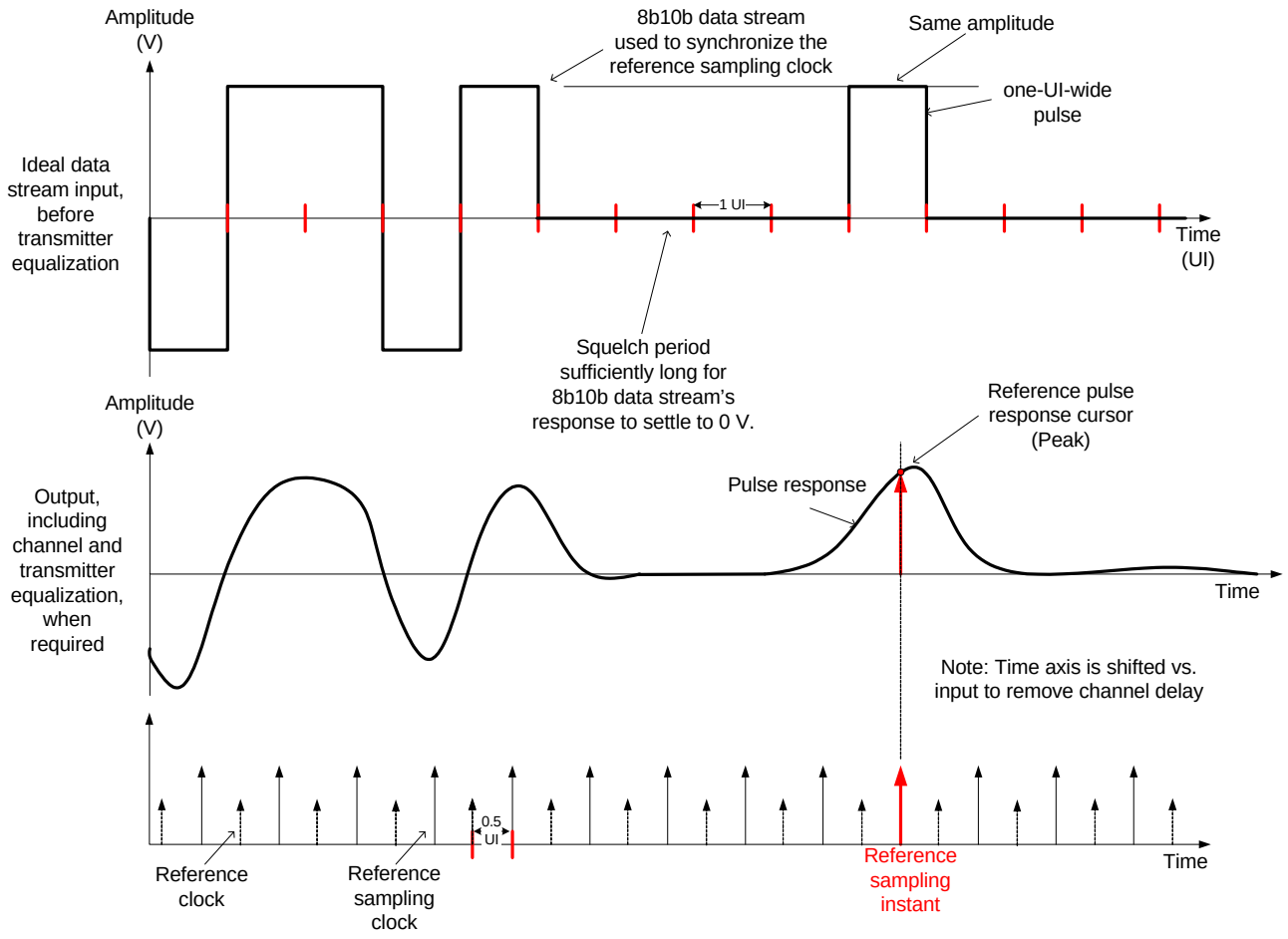


Figure 113 — Reference sampling point and reference pulse response cursor

Figure 114 shows the computations of step 3). A one-UI-spaced filter of coefficients [C1, 1, C3] is convolved with the extracted end-to-end pulse response. Coefficient 1 and coefficient 3 are computed to produce an

equalized pulse response that has the smallest sum of squared errors at the sampling instants defined by a reference sampling clock.

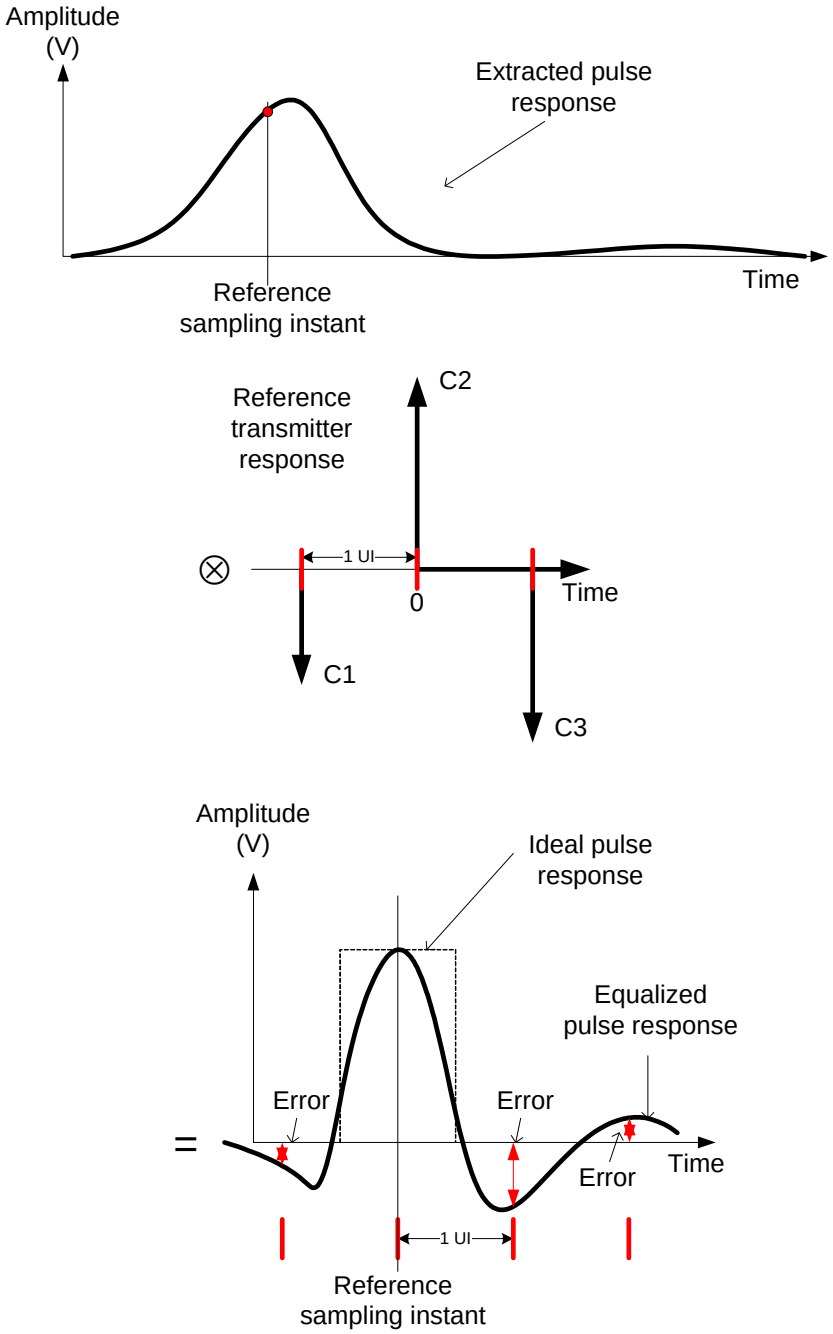


Figure 114 — Reference transmitter coefficient error computation

The reference sampling instant is computed from:

1) the un-equalized pulse response from ET to RR, for the first iteration; and
2) the equalized pulse response using transmitter coefficients from the previous iteration, for other iterations.

The reference sampling instant changes when the coefficients from the current iteration are used to compute the equalized pulse response. As shown in figure 115, the process of calculating C1 and C3 is repeated with

the reference sampling instant computed from the last equalized pulse response, until the coefficients and reference sampling instant converge to stable values.

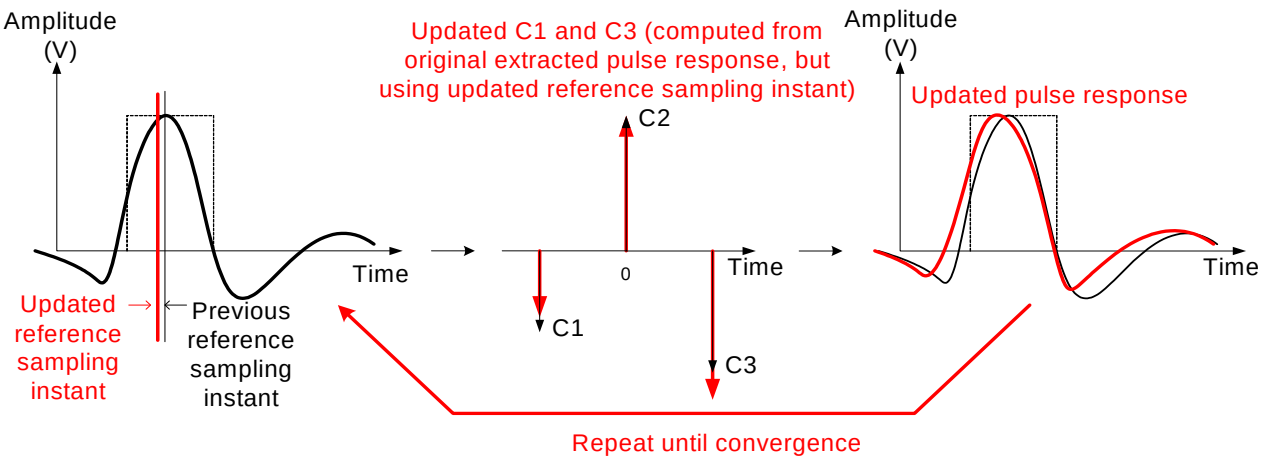


Figure 115 — Convergence of reference traansmitter equalization

If any of coefficient 1 or coefficient 3 takes a positive value during this procedure, its value is forced to zero and only the other coefficient is computed. The procedure stops if both coefficients need to be forced to zero.

5.8.4 Crosstalk measurement for end-to-end simulations and 12Gbps jitter tolerance

End-to-end channel simulation shall include crosstalk. Crosstalk shall be measured using:

a) crosstalk transfer functions (e.g., S-parameters, see E.11); or
b) total peak-to-peak crosstalk measurement.

The following procedure shall be used to measure total peak-to-peak crosstalk:

1) terminate the channel under test on the transmitter end;
2) connect 12 Gbps transmitters to the source of all or a subset of crosstalk channels;
3) set the crosstalk transmitters to transmit asynchronous IDLE patterns (see SPL-2);
4) measure the asynchronous amplitude histogram at the end of the channel under test, into a zero-length test load, with an acquisition bandwidth of at least 9 GHz, and a capture of 10^7 UI;
5) repeat steps 2) through 4) until all crosstalk sources have been measured;
6) when multiple measurements are made, convolve the histograms to obtain the total crosstalk histogram; and
7) evaluate the crosstalk amplitude at a probability of 10^{-6} from the total crosstalk histogram.

To provide a variety of pattern combinations for the crosstalk measurement, the digital IDLE patterns should be aligned differently one crosstalk channel to another, and the transmission frequencies of the crosstalk transmitters should be different one from another.

The channel under test shall be terminated with the characteristics of the transmitter device termination (see table 34) on the transmitter end. The termination should be implemented using:

a) a high-bandwidth termination having impedance close to the nominal differential impedance (see table 24), for TxRx connection segments; or
b) a transmitter device set to transmit D.C. idle while maintaining the characteristics of table 34 for transmitter circuits and ISI generators.

Active circuits create noise when transmitting signals, including D.C. idle. By measuring the crosstalk with active circuits connected, the crosstalk value reported includes this noise. This is expected to represent better the noise generated when the active circuit is transmitting data. When multiple crosstalk measurements are performed, this noise may however be overestimated in the final crosstalk amplitude calculation. Appropriate measurement techniques should be used to minimize these effects.

For transmitter device characterization, the crosstalk transmitters shall set coefficient 1 to 0, set coefficient 3 to 0, and set maximum peak-to-peak voltage.

For receiver ISI stress generators, the crosstalk is measured into a zero-length test load, and shall not include crosstalk from the receiver under test. A crosstalk generator channel should be selected to provide signal characteristics as close as possible to the required crosstalk signal characteristics (see table D.2 in table D.1), with the crosstalk generator characteristics defined by table D.1 (see D.1). Coefficients and peak-to-peak voltage should then be adjusted to meet the required crosstalk characteristics.

5.9 Transmitter device and receiver device electrical characteristics

5.9.1 General electrical characteristics

Table 31 defines the general electrical characteristics, which apply to both transmitter devices and receiver devices.

Table 31 — General electrical characteristics

Characteristic	Units	1.5 Gbps (i.e., G1)	3 Gbps (i.e., G2)	6 Gbps (i.e., G3)	12 Gbps (i.e., G4)
Physical link rate (nominal)	MBps	150	300	600	1 200
Unit interval (UI) (nominal) [a]	ps	$666.\overline{6}$	$333.\overline{3}$	$166.\overline{6}$	$83.\overline{3}$
Baud rate (f_{baud}) (nominal)	Gigasymbols/s	1.5	3	6	12
Maximum A.C. coupling capacitor [b]	nF	12			
Maximum noise during OOB idle time [c] [d]	mV(P-P)	120			

[a] $666.\overline{6}$ equals 2 000 / 3. $333.\overline{3}$ equals 1 000 / 3. $166.\overline{6}$ equals 500 / 3. $83.\overline{3}$ equals 250 / 3.
[b] The coupling capacitor value for A.C. coupled transmit and receive pairs. See 5.9.4.2 for coupling requirements for transmitter devices. See 5.9.5.2 for coupling requirements for receiver devices. The equivalent series resistance at 3 GHz should be less than 1 ohm.
[c] With a measurement bandwidth of 1.5 × f_{baud} (e.g., 9 GHz for 6 Gbps), no signal level during the idle time shall exceed the specified maximum differential amplitude.
[d] This is not applicable when optical mode is enabled.

5.9.2 Transmitter device and receiver device transients

Transients may occur at transmitter devices or receiver devices as a result of changes in supply power conditions or mode transitions.

A mode transition is an event that may result in a measurable transient due to the response of the transmitter device or receiver device. The following conditions constitute a mode transition:

a) enabling or disabling driver circuitry;
b) enabling or disabling receiver common-mode circuitry;
c) hot plug event;
d) adjusting driver amplitude;
e) enabling or disabling de-emphasis; and
f) adjusting terminator impedance.

Transmitter device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 116 during all power state and mode transitions. Receiver device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 117 during all power state and mode transitions. Test conditions shall include power supply power on and power off conditions, voltage sequencing, and mode transitions.

Figure 116 shows the test circuit attached to IT or CT to test transmitter device transients.

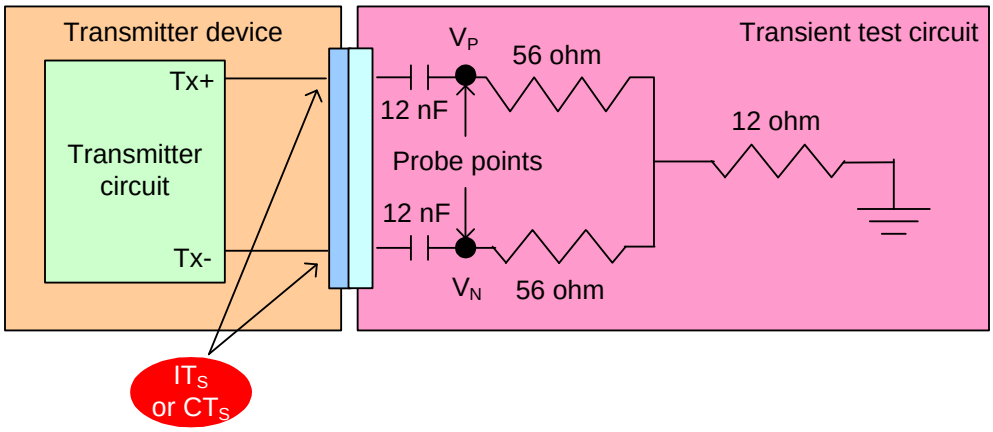


Figure 116 — Transmitter device transient test circuit

Figure 117 shows the test circuit attached to IR or CR to test receiver device transients.

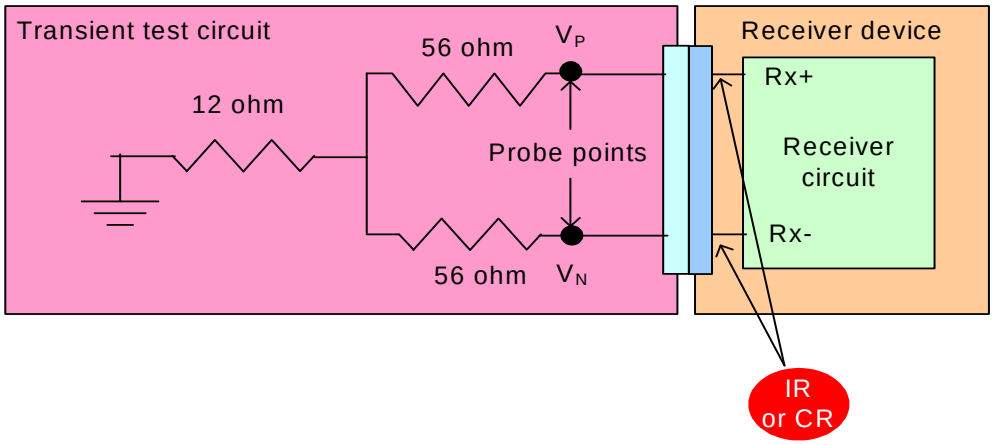


Figure 117 — Receiver device transient test circuit

5.9.3 Eye masks and the jitter transfer function (JTF)

5.9.3.1 Eye masks overview

The eye masks shown in this subclause shall be interpreted as graphical representations of the voltage and time limits of the signal. The eye mask boundaries define the eye contour of:

a) the 10^{-12} jitter population for untrained 1.5 Gbps and 3 Gbps measured eyes; and
b) the 10^{-15} jitter population for trained 1.5 Gbps, 3 Gbps, and 6 Gbps simulated eyes.

For untrained 1.5 Gbps and 3 Gbps, equivalent time sampling oscilloscope technology is not practical for measuring compliance to the eye masks. See MJSQ for methods that are suitable for verifying compliance to these eye masks.

CJTPAT (see Annex A) shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and provides information regarding special considerations for running disparity (see SPL-2) and scrambling (see SPL-2).

5.9.3.2 Jitter transfer function (JTF)

With the possible presence of SSC, the application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667) as specified in versions of SAS standards previous to SAS-2 does not separate the SSC component from the actual jitter and

thus may overstate the transmitter device jitter. To differentiate between allowable timing variation due to SSC and jitter, the frequency-weighting JTF shall be applied to the signal at the compliance point when determining the eye mask.

The jitter measurement device shall comply with the JTF. The reference clock characteristics are controlled by the resulting JTF characteristics obtained by taking the time difference between the PLL output (i.e., the reference clock) and the data stream sourced to the PLL. The PLL's closed loop transfer function's -3 dB corner frequency and other adjustable parameters (e.g., peaking) are determined by the value required to meet the requirements of the JTF.

The JTF shall have the characteristics specified in table 32 for a repeating 0011b or 1100b pattern (e.g., D24.3) See the phy test patterns in the Protocol-Specific diagnostic page in SPL-2.

The JTF -3 dB corner frequency and the magnitude peaking requirements shall be measured with SJ applied, with a peak-to-peak amplitude of 0.3 UI ± 10 %. The relative attenuation at 30 kHz shall be measured with sinusoidal phase (i.e., time) modulation applied, with a peak-to-peak amplitude of 20.8 ns ± 10 %. See Annex E for the detailed calibration procedure.

A proportional decrease of the JTF -3 dB corner frequency should be observed for a decrease in pattern transition density compared to a 0.5 transition density. If a JMD shifts the JTF -3 dB corner frequency in a manner that does not match this characteristic, or does not shift at all, then measurements of jitter with patterns with transition densities different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3 dB corner frequency that is closest to the proportional characteristic of the reference transmitter test load (see 5.7.5) shall be considered correct. This characteristic may be measured with the conditions defined above for measuring the -3 dB corner frequency but substituting other patterns with different transition densities.

Table 32 — JTF parameters

Characteristic	Untrained		Trained without SSC support				Trained with SSC support			
	1.5 Gbps	3 Gbps	1.5 Gbps	3 Gbps	6 Gbps	12 Gbps	1.5 Gbps	3 Gbps	6 Gbps	12 Gbps
JTF -3 dB point (kHz) [a] [b]	900 ± 500	1 800 ± 500	900 ± 500	1 800 ± 500	3 600 ± 500	3 600 ± 500	1 300 ± 500	1 838 ± 500	2 600 ± 500	2 600 ± 500
JTF slope (dB/decade)	20	20	20	20	20	20	40	40	40	40
Attenuation at 30 kHz ± 1 % (dB) [c]	N/A	N/A	N/A	N/A	N/A	N/A	61.5 ± 1.5	67.5 ± 1.5	73.5 ± 1.5	73.5 ± 1.5
Maximum Peaking (dB)	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5

[a] For untrained or trained without SSC support this value equals f_{baud}/1 667 ± 500 kHz.
[b] For trained with SSC support this value equals $(f_{baud})^{0.5}$ x 33.566 x $Hz^{0.5}$ ± 500 kHz.
[c] For trained with SSC support this value equals 73.5 dB + [20 x log(f_{baud} / 6 x 10^9 Hz)] dB ± 1.5 dB.
[d] For the above equations, f_{baud} is expressed in Hz (i.e., 1.5 GHz for 1.5 Gbps, 3.0 GHz for 3 Gbps, 6.0 GHz for 6 Gbps, 12 GHz for 12Gbps).

5.9.3.3 Transmitter device eye mask for untrained 1.5 Gbps and 3 Gbps

Figure 118 describes the eye mask used for testing the signal output of the transmitter device at IT and CT for untrained 1.5 Gbps and 3 Gbps (see table 36 in 5.9.4.5) and OOB signals (see table 50 in 5.9.4.8). This eye mask applies to jitter after the application of the JTF (see 5.9.3.2).

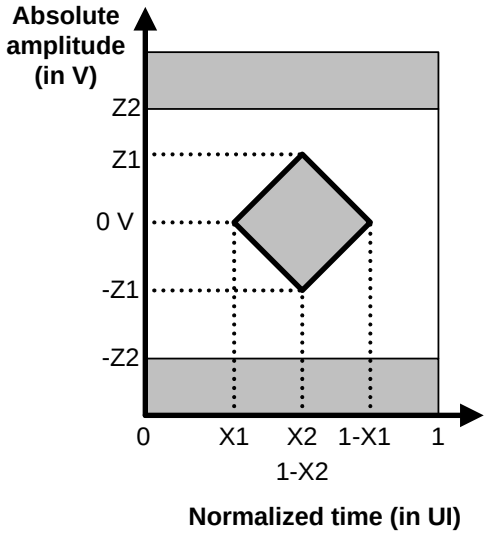


Figure 118 — Transmitter device eye mask

Verifying compliance with the limits represented by the transmitter device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.9.3.4 Receiver device eye mask for untrained 1.5 Gbps and 3 Gbps

Figure 119 describes the eye mask used for testing the signal delivered to the receiver device at IR and CR for untrained 1.5 Gbps and 3 Gbps (see table 53 in 5.9.5.4). This eye mask applies to jitter after the application of the JTF (see 5.9.3.2). This requirement accounts for the low frequency tracking properties and response time of the CDR circuitry in receiver devices.

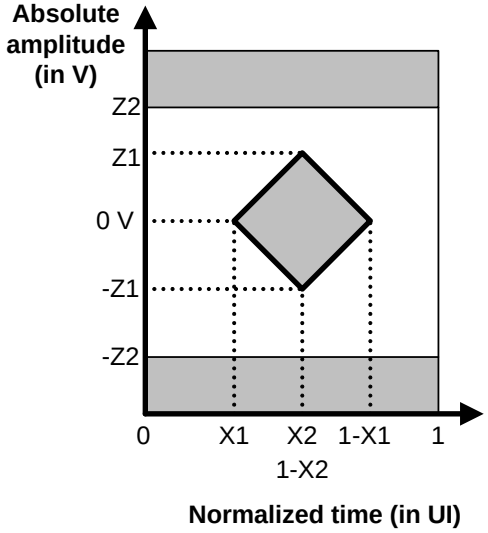


Figure 119 — Receiver device eye mask

Verifying compliance with the limits represented by the receiver device eye mask should be done with reverse channel traffic present on the channel-under-test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.9.3.5 Receiver device jitter tolerance eye mask for untrained 1.5 Gbps and 3 Gbps

Figure 120 describes the eye mask used to test the jitter tolerance of the receiver device at IR and CR for untrained 1.5 Gbps and 3 Gbps (see table 53 in 5.9.5.4). For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, jitter tolerance is included in the delivered signal specifications for stressed receiver device jitter tolerance testing (see 5.9.5.7.6).

The eye mask shall be constructed as follows:

a) X2 and Z2 shall be the values for the delivered signal listed in table 53 (see 5.9.5.4);
b) $X1_{OP}$ shall be half the value of TJ for maximum delivered jitter listed in table 54 (see 5.9.5.5); and
c) $X1_{TOL}$ shall be half the value of TJ for receiver device jitter tolerance listed in table 55 (see 5.9.5.6), for applied SJ frequencies above (f_{baud} / 1 667).

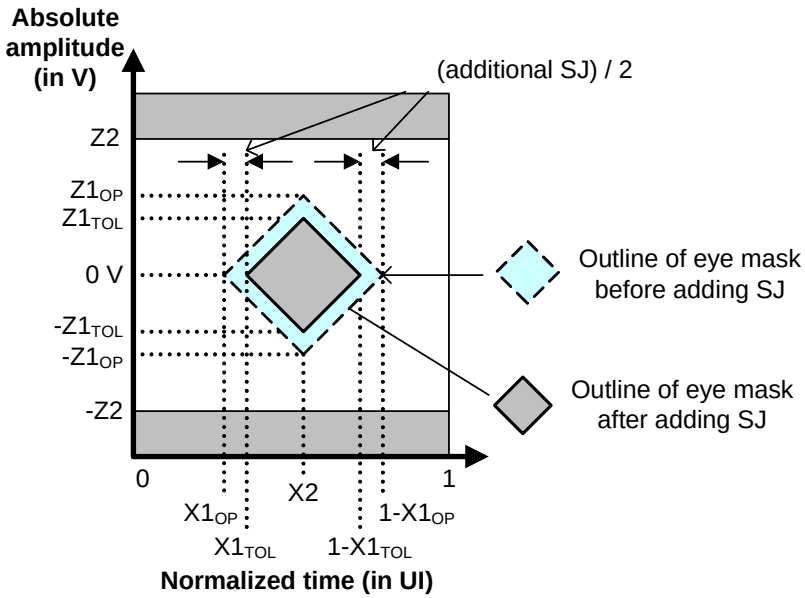


Figure 120 — Deriving a receiver device jitter tolerance eye mask for untrained 1.5 Gbps and 3 Gbps

The leading and trailing edge slopes of the receiver device eye mask in figure 119 (see 5.9.3.4) shall be preserved. As a result, the amplitude value of Z1 is less than that given for the delivered signal in table 53 (see 5.9.5.4), and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2 - \left(\frac{ASJ}{2}\right) - X1_{OP}}{X2 - X1_{OP}}$$

where:

$Z1_{TOL}$	is the value for Z1 to be used for the receiver device jitter tolerance eye mask;
$Z1_{OP}$	is the Z1 value for the delivered signal in table 53;
$X1_{OP}$	is the X1 value for the delivered signal in table 53;
X2	is the X2 value for the delivered signal in table 53; and
ASJ	is the additional SJ for applied SJ frequencies above (f_{baud} / 1 667) (see figure 133 in 5.9.5.6).

The X1 points in the receiver device jitter tolerance eye mask (see figure 120) are greater than the X1 points in the receiver device eye mask (see figure 119) due to the addition of SJ.

5.9.4 Transmitter device characteristics

5.9.4.1 Transmitter device characteristics overview

Transmitter devices operating at 1.5 gbps, 3 Gbps, or 6 Gbps may or may not incorporate de-emphasis (i.e., pre-emphasis) and other forms of compensation. The transmitter device operating at 1.5 gbps, 3 Gbps, or 6 Gbps shall use the same settings (e.g., de-emphasis and voltage swing) with both the zero-length test load and the appropriate TCTF test load or reference transmitter test load (see 5.7). Transmitter devices operating at 6 Gbps should use the transmitter equalization settings provided in table 40. Transmitter devices operating at 6 Gbps may use transmitter training if supported (see 5.9.4.7.1 and SPL-2). Transmitter devices operating at 12 Gbps shall support transmitter training (see SPL-2) unless the transmitter device is operating in the optical mode.

See E.7 for a methodology for measuring transmitter device signal output.

5.9.4.2 Transmitter device coupling requirements

Coupling requirements for transmitter devices are as follows:

a) transmitter devices using inter-enclosure TxRx connections (i.e., attached to CT compliance points) should be D.C. coupled, but may be A.C. coupled to the interconnect through a transmission network;
b) transmitter devices using intra-enclosure TxRx connections (i.e., attached to IT compliance points) should be D.C. coupled, but may be A.C. coupled.

NOTE 16 - If the transmitter device is attached to an IT compliance point supporting SATA, then the coupling requirements of Gen1i devices (see SATA) should be considered regarding its impact to the implementation.

See table 31 (see 5.9.1) for the coupling capacitor value.

5.9.4.3 Transmitter device general electrical characteristics

Table 33 defines the transmitter device general electrical characteristics.

Table 33 — Transmitter device general electrical characteristics

Characteristic	Units	1.5 Gbps	3 Gbps	6 Gbps	12 Gbps
Physical link rate long-term accuracy [a] at IT and CT	ppm	± 100			
Physical link rate SSC modulation at IT and CT	ppm	See table 68 and table 69 in 5.9.6.2			
Maximum transmitter device transients [b]	V	± 1.2			

[a] Physical link rate long-term accuracy should be measured using a frequency counter with adequate resolution (e.g., 100 Hz).
[b] See 5.9.2 for transient test circuits and conditions.

Table 34 defines the transmitter device termination characteristics.

Table 34 — Transmitter device termination characteristics

Characteristic	Units	Untrained 1.5 Gbps and 3 Gbps	Trained 1.5 Gbps and 3 Gbps	6 Gbps and 12Gbps
Differential impedance [a]	ohm	60 minimum 115 maximum	See 5.9.4.6.1	
Maximum differential impedance imbalance [a] [b]	ohm	5	See 5.9.4.6.3 [c]	
Common-mode impedance [b]	ohm	15 minimum 40 maximum	See 5.9.4.6.1	

[a] All transmitter device termination measurements are made through mated connector pairs.
[b] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.
[c] Measurement replaced by S_{CD22} specifications (i.e., differential to common mode conversion).

5.9.4.4 Transmitter device signal output characteristics for untrained 1.5 Gbps and 3 Gbps as measured with the zero-length test load

Table 35 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbps and 3 Gbps as measured with the zero-length test load (see 5.7.2) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.9.4.6 for trained 1.5 Gbps, 3

Gbps, and 6 Gbps transmitter device signal output characteristics. See SATA for untrained 6 Gbps (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 35 — Transmitter device signal output characteristics for untrained 1.5 Gbps and 3 Gbps as measured with the zero-length test load at IT and CT

Signal characteristic [a]	Units	Untrained	
		1.5 Gbps	3 Gbps
Maximum intra-pair skew [b]	ps	20	15
Maximum transmitter device off voltage [c] [d]	mV(P-P)	50	
Maximum (i.e., slowest) rise/fall time [e]	ps	273	137
Minimum (i.e., fastest) rise/fall time [e]	ps	41.6	
Maximum transmitter output imbalance [f]	%	10	

[a] All tests in this table shall be performed with zero-length test load (see 5.7.2).

[b] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal.

[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[d] This is not applicable when optical mode is enabled.

[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link.

[f] The maximum difference between the V+ and V- A.C. rms transmitter device amplitudes measured with CJTPAT (see Annex A) into the zero-length test load shown in figure 97 (see 5.7.2), as a percentage of the average of the V+ and V- A.C. rms amplitudes.

5.9.4.5 Transmitter device signal output characteristics for untrained 1.5 Gbps and 3 Gbps as measured with each test load

Table 36 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbps and 3 Gbps as measured with each test load (i.e., the zero-length test load (see 5.7.2) and either the TCTF test load (see 5.7.3) or the low-loss TCTF test load (see 5.7.4)) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.9.4.6 for trained 1.5 Gbps, 3 Gbps, and 6 Gbps transmitter device signal output characteristics. See SATA for untrained 6 Gbps (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 36 — Transmitter device signal output characteristics for untrained 1.5 Gbps and 3 Gbps as measured with each test load at IT and CT

Signal characteristic	Units	IT, untrained		CT, untrained	
		1.5 Gbps	3 Gbps	1.5 Gbps	3 Gbps
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 118) if SATA is not supported	mV(P-P)	1 600			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 118) if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 118), if SATA is not supported	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 118), if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Maximum DJ [b c d]	UI	0.35			
Maximum half of TJ (i.e., X1 in figure 118) [b c d e f g h]	UI	0.275			
Center of bit time (i.e., X2 in figure 118)	UI	0.50			
Maximum intra-pair skew [i]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] All DJ and TJ values are level 1 (see MJSQ).

[c] The values for jitter in this table are measured at the average signal amplitude point.

[d] The DJ and TJ values in this table apply to jitter measured as described in 5.9.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.

[e] TJ is specified at a CDF level of 10^{-12}.

[f] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.

Jitter peak-to-peak measured < (maximum TJ - |Asymmetry|).

[g] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability, direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[h] The value for X1 is also half the value of TJ for maximum delivered jitter listed in table 54 (see 5.9.5.5). The test or analysis shall include the effects of the JTF (see 5.9.3.2).

[i] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal at the probe points.

5.9.4.6 Transmitter device signal output characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

5.9.4.6.1 Transmitter device signal output characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps overview

Table 37 specifies the signal output characteristics for the transmitter device for trained 1.5 Gbps, 3 Gbps, and 6 Gbps as measured with the zero-length test load (see 5.7.2), unless otherwise specified, attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements.

Table 37 — Transmitter device signal output characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps at IT and CT

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage [b] [c]	mV(P-P)			50
Withstanding voltage (non-operational)	mV(P-P)	2 000		
Rise/fall time [d]	ps	41.6		
Reference differential impedance [e]	ohm		100	
Reference common mode impedance [e]	ohm		25	
Common mode voltage limit (rms) [f]	mV			30
RJ [g] [h]	UI			0.15 [i]
TJ [h] [j]	UI			0.25 [k]
WDP at 6 Gbps [l]	dB			13
WDP at 3 Gbps [l]	dB			7
WDP at 1.5 Gbps [l]	dB			4.5

[a] See 5.9.4.6.6 for the V_{P-P} measurement method.
[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[c] This is not applicable when optical mode is enabled.
[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link.
[e] See 5.9.4.6.3 for transmitter device S-parameters characteristics.
[f] This is a broadband limit. For additional limits on spectral content, see figure 121 and table 38.
[g] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.
[h] The measurement shall include the effects of the JTF (see 5.9.3.2).
[i] 0.15 UI is 25 ps at 6 Gbps, 50 ps at 3 Gbps, and 100 ps at 1.5 Gbps.
[j] The TJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.
[k] 0.25 UI is 41.6 ps at 6 Gbps, 83.3 ps at 3 Gbps, and 166.6 ps at 1.5 Gbps.
[l] See 5.9.4.6.2 for the transmitter device test procedure.

Table 38 defines the transmitter device common mode voltage limit characteristics.

Table 38 — Transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] (dBmV) [b]	N [a] (dBmV) [b] [c]	S [a] (dBmV/decade) [b]	f_{min} [a] (MHz)	f_{max} [a] (GHz)
Spectral limit of common mode voltage [d]	Figure 121	12.7	26.0	13.3	100	6.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 ohms (i.e., the reference impedance for common mode voltage) which is $20 \times \log_{10}(158) = +44$ dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at the Nyquist frequency (i.e., 3 GHz) (see figure 121).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 121 shows the transmitter device common mode voltage limit defined in table 38.

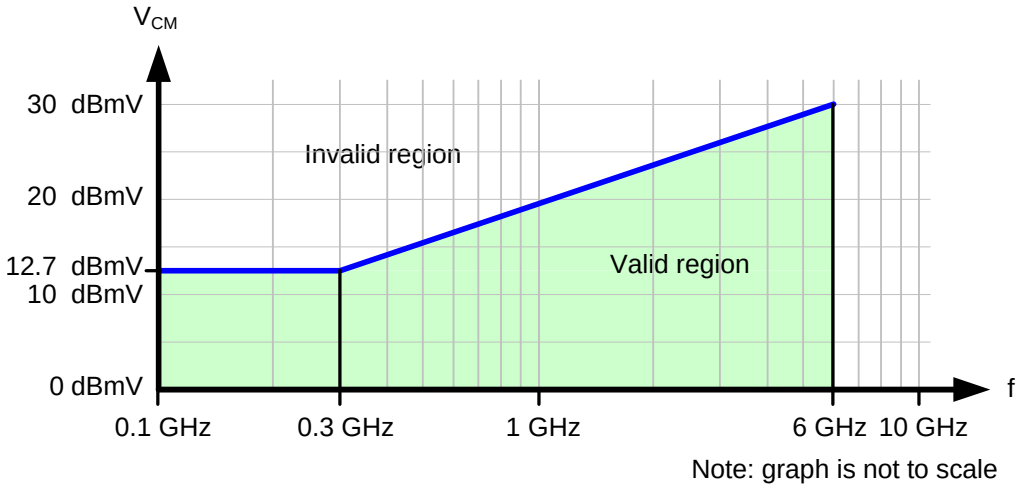


Figure 121 — Transmitter device common mode voltage limit

5.9.4.6.2 Trained 1.5 Gbps, 3 Gbps, and 6 Gbps transmitter device test procedure

The transmitter device test procedure is as follows:

1) attach the transmitter device to a zero-length test load, where its signal output is captured by an oscilloscope;
2) configure the transmitter device to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2);
3) configure the transmitter device to minimize DCD and BUJ;

NOTE 17 - WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

4) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Use averaging to minimize RJ; and
5) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to ‘SAS2_TWDP’.

The WDP value is a characterization of the signal output within the reference receiver device (see 5.9.5.7.3) after equalization.

5.9.4.6.3 1.5 Gbps, 3 Gbps, and 6 Gbps Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}$(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 39 defines the maximum limits for S-parameters of the transmitter device.

Table 39 — Maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\lvert S_{CC22} \rvert$	-6.0	-5.0	0	13.3	100	6.0
$\lvert S_{DD22} \rvert$	-10	-7.9	0	13.3	100	6.0
$\lvert S_{CD22} \rvert$	-26	-12.7	-10	13.3	100	6.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See E.11.4.2.
[b] $\lvert S_{DC22} \rvert$ is not specified.
[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 122 shows the transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 39.

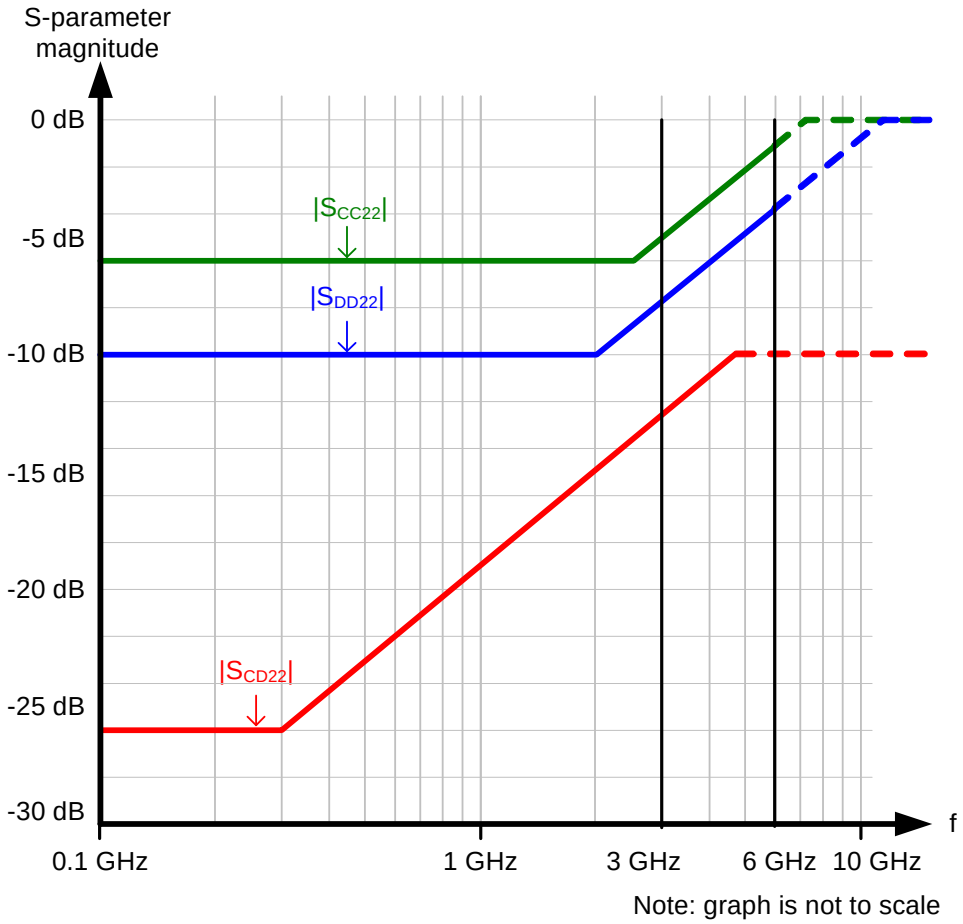


Figure 122 — Transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.9.4.6.4 Recommended 6 Gbps transmitter device settings for interoperability

Table 40 defines recommended values for 6 Gbps transmitter devices to provide interoperability with a broad range of implementations utilizing compliant TxRx connections and compliant receiver devices. The values are based on the evaluation of simulations with a variety of characterized physical hardware. Use of the recommended values does not guarantee that an implementation is capable of achieving a specific BER.

Specific implementations may obtain increased margin by deviating from the recommended values. However, such implementations are beyond the scope of this standard.

Table 40 — Recommended 6 Gbps transmitter device settings at IT and CT

Characteristic	Units	Minimum	Nominal	Maximum
Differential voltage swing (mode) (VMA) [a]	mV	600	707	
Transmitter equalization [a]	dB	2	3	4
[a] See 5.9.4.6.6 for measurement method.				

5.9.4.6.5 6 Gbps reference transmitter device characteristics

The 6 Gbps reference transmitter device is a set of parameters defining the electrical performance characteristics of a transmitter device used in simulation to determine compliance of a TxRx connection (see 5.6.5).

Figure 123 shows a 6 Gbps reference transmitter device.

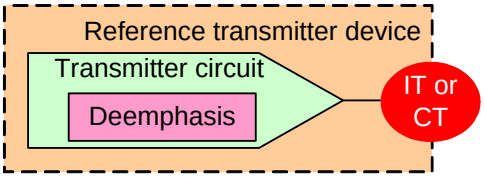


Figure 123 — 6 Gbps reference transmitter device

Table 41 defines the 6 Gbps reference transmitter device characteristics.

Table 41 — 6 Gbps reference transmitter device characteristics at IT and CT

Characteristic	Units	Value
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850
Transmitter equalization [a]	dB	2
Maximum (i.e., slowest) rise/fall time [b]	UI	0.41 [c]
RJ	UI	0.15 [d]
BUJ	UI	0.10 [e]

[a] See 5.9.4.6.6 for measurement method.
[b] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2).
[c] 0.41 UI is 68.3 ps at 6 Gbps, 136.6 ps at 3 Gbps, and 273.3 ps at 1.5 Gbps.
[d] 0.15 UI is 25 ps at 6 Gbps, 50 ps at 3 Gbps, and 100 ps at 1.5 Gbps.
[e] 0.10 UI is 16.6 ps at 6 Gbps, 33.3 ps at 3 Gbps, and 66.6 ps at 1.5 Gbps.

The following Touchstone model of the reference transmitter device termination is included with this standard:

a) SAS2_TxRefTerm.s4p.

Figure 124 shows the S-parameters of the 6 Gbps reference transmitter device termination model.

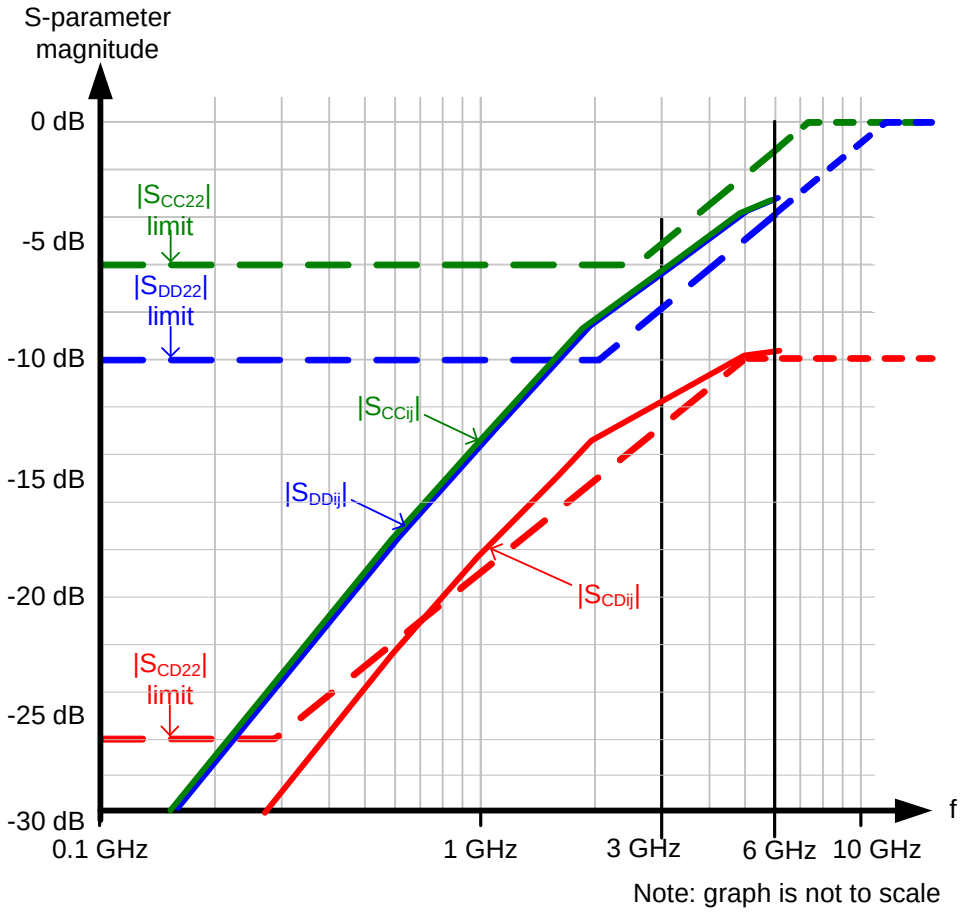


Figure 124 — Reference transmitter device termination S-parameters

The Touchstone model does not exactly match the $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in 5.9.4.6.3 at all frequencies; it is a reasonable approximation for use in simulations. See Annex F for a description of how the Touchstone model was created.

5.9.4.6.6 6 Gbps Transmitter equalization, VMA, and V_{P-P} measurement

The transmitter equalization measurement shall be based on the following values:

a) VMA: a mode (i.e., the most frequent value of a set of data) measurement; and
b) V_{P-P}: a peak-to-peak measurement with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2).

The VMA and V_{P-P} measurements shall be made with the transmitter device terminated through the interoperability point into a zero length test load (see 5.7.2).

The VMA and V_{P-P} measurements shall be made using an equivalent time sampling scope with a histogram function with the following or an equivalent procedure:

1) calibrate the sampling scope for measurement of a 3 GHz signal; and
2) determine VMA and V_{P-P} as shown in figure 125. A sample size of 1 000 minimum to 2 000 maximum histogram hits for VMA shall be used to determine the values. The histogram is a combination of two histograms: an upper histogram for Tx+ and a lower histogram for Tx-. The histograms on the left

represent the test pattern signal displayed on the right. VMA and V_{P-P} are determined by adding the values measured for Tx+ and Tx-.

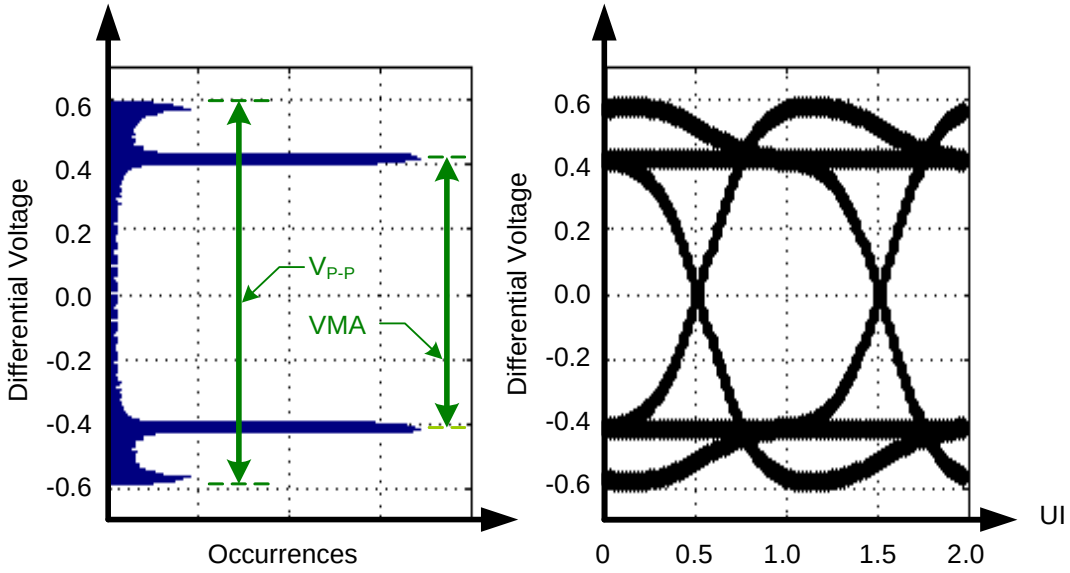


Figure 125 — Transmitter equalization measurement

The following formula shall be used to calculate the transmitter equalization value:

Transmitter equalization = $20 \times \log_{10} (V_{P-P} / VMA)$ dB

where:

V_{P-P} is the peak-to-peak value; and

VMA is the mode value.

5.9.4.7 Transmitter device signal output characteristics for trained 12 Gbps

5.9.4.7.1 Transmitter device signal output characteristics for trained 12 Gbps overview

Table 42 specifies the signal output characteristics for the transmitter device for trained 12 Gbps.

Table 42 — Transmitter device signal output characteristics for trained 12 Gbps at ET

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a] [b]	mV(P-P)	850	1 000	1 200
Transmitter device off voltage [c] [d]	mV(P-P)			50
Withstanding voltage (non-operational)	mV(P-P)	2 000		
Rise/fall time [e]	ps	20.8		
Reference differential impedance [f]	ohm		100	
Reference common mode impedance [f]	ohm		25	
Pre-cursor equalization ratio R_{pre} [g]	V/V	1		1.67
Post-cursor equalization ratio R_{post} [h]	V/V	1		$3.3\overline{3}$
VMA [i]	mV(P-P)	80		
Common mode voltage limit (rms) [j]	mV			30
RJ [k] [l] [m]	UI			0.15 [n]
TJ [l] [m] [o]	UI			0.25 [p]

[a] The V_{P-P} measurement shall be made with the transmitter device set to no equalization (see table 45) and amplitude set to maximum with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2).

[b] Peak-to-peak voltage shall be measured with the transmitter coefficient 2 set to its maximum value.

[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[d] This is not applicable when optical mode is enabled.

[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link.

[f] See 5.9.4.7.2 for transmitter device S-parameters characteristics.

[g] Ratio measured with post-cursor equalization disabled and peak-to-peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-2 and figure 128). When both pre-cursor and post-cursor equalization are active the maximum observed R_{pre} may be as high as 3.8 at the VMA limit.

[h] Ratio measured with pre-cursor equalization disabled and peak-to-peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-2 and figure 128). When both pre-cursor and post-cursor equalization are active the maximum observed R_{post} may be as high as 5.5 at the VMA limit.

[i] Measured as v_2- v_5 (see figure 128) with a repeating TRAIN_DONE primitive (see SPL-2).

[j] This is a broadband limit. For additional limits on spectral content, see figure 126 and table 43.

[k] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[l] The measurement shall include the effects of the JTF (see 5.9.3.2).

[m] RJ and TJ are measured at IT or CT.

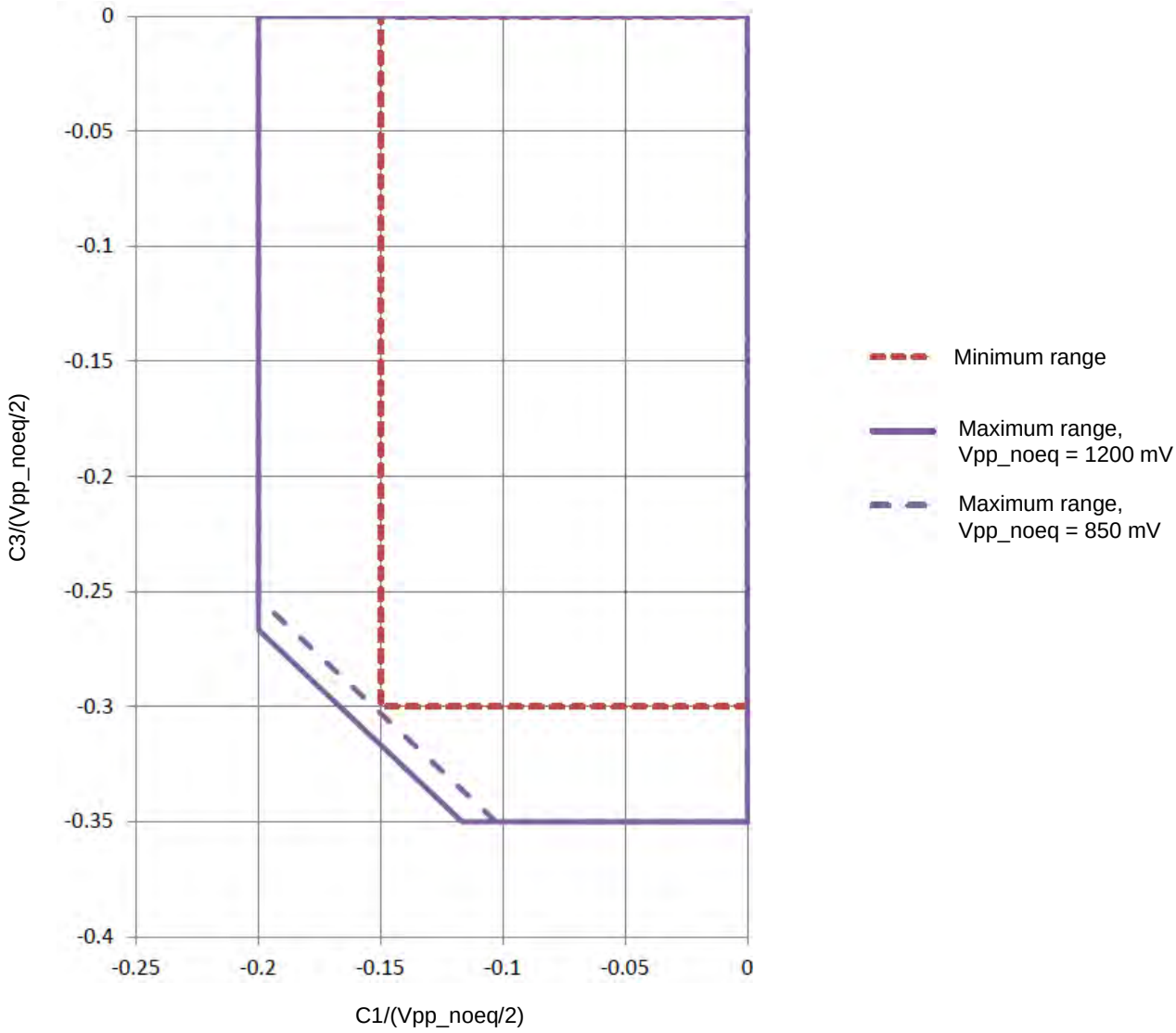
[n] 0.15 UI is 12.5 ps at 12 Gbps.

[o] The TJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[p] 0.25 UI is 20.8 ps at 12 Gbps.

In addition to table 42, figure specifies the transmitter coefficient ranges when the transmitter peak-to-peak voltage is maximum. The coefficients are defined according to the reference transmitter (see 5.9.4.7.3). The bottom left area of the minimum and maximum ranges are limited by VMA and vary according to V_{p-p}_noeq. V_{p-p}_noeq is the amplitude at ET measured with the no_eualization setting as specified in table 45.

Minimum and maximum coefficient ranges at maximum peak-to-peak voltage



Editor's Note 5: Add table here for 12 Gbps drive requirements.

Table 43 defines the transmitter device common mode voltage limit characteristics.

Table 43 — 12 Gbps transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] (dBmV) [b]	N [a] (dBmV) [b] [c]	S [a] (dBmV/decade) [b]	f_{min} [a] (MHz)	f_{max} [a] (GHz)
Spectral limit of common mode voltage [d]	Figure 126	12.7	26.0	13.3	100	6.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 ohms (i.e., the reference impedance for common mode voltage) which is $20 \times \log_{10}(158) = +44$ dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at the Nyquist frequency (i.e., 3 GHz) (see figure 126).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Editor's Note 6: At least note c needs to be changed for 12 Gbps.

Figure 126 shows the transmitter device common mode voltage limit defined in table 43.

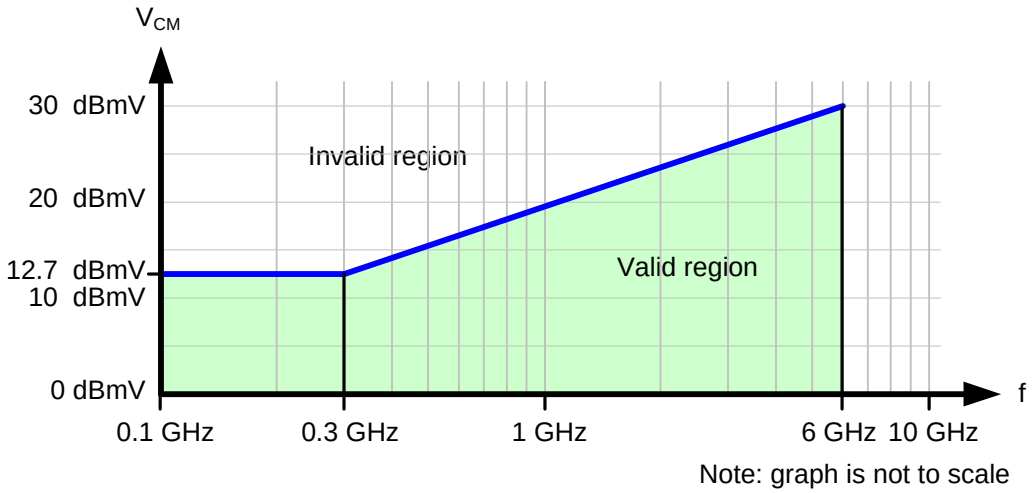


Figure 126 — 12 Gbps transmitter device common mode voltage limit

Transmitter equalization coefficient adjustments are controlled using an algorithm defined in SPL-2. Transmitter circuits that support 12 Gbps, when not operating in optical mode, shall:

a) support the coefficient requests shown in table 44; and
b) provide equalization equivalent to the reference transmitter device (see 5.9.4.7.3).

The algorithm for optimizing the transmitter coefficient is beyond the scope of this standard.

Table 44 — Transmitter coefficient requests and corresponding transmitter circuit response

Coefficient 1 request	Coefficient 2 request	Coefficient 3 request	Description	$V_{HL}(k+1)$-$V_{HL}(k)$ (mV(P-P))	v1(k+1) - V1(k) (mV)	v2(k+1) - V2(k) (mV)	v3(k+1) - V3(k) (mV)
hold [a]	hold [a]	hold [a]	Hold peak-to-peakvoltage and hold equalization	-20 to +20	-10 to +10	-10 to +10	-10 to +10
dec [b]	dec [b]	hold [a]	Increase pre-cursor and hold peak-to-peak voltage	-20 to +20	-40 to -10	-40 to -10	-10 to +10
inc [c]	inc [c]	hold [a]	Decrease pre-cursor and hold peak-to-peak voltage	-20 to +20	+40 to +10	+40 to +10	-10 to +10
hold [a]	dec [b]	dec [b]	Increase post-cursor and hold peak-to-peak voltage	-20 to +20	-10 to +10	-40 to -10	-40 to -10
hold [a]	inc [c]	inc [c]	Decrease post-cursor and hold peak-to-peak voltage	-20 to +20	-10 to +10	+40 to +10	+40 to +10
hold [a]	dec [b]	hold [a]	Decrease peak-to-peak voltage and hold equalization	-40 to -10	-20 to -5	-20 to -5	-20 to -5
hold [a]	inc [c]	hold [a]	Increase peak-to-peak voltage and hold equalization	+40 to +10	+20 to +5	+20 to +5	+20 to +5
dec [b]	hold [a]	hold [a]	Increase pre-cursor and increase peak-to-pea k voltage	+40 to +10	-20 to -5	-20 to -5	+20 to +5
inc [c]	hold [a]	hold [a]	Decrease pre-cursor and decrease peak-to-peak voltage	-40 to -10	+20 to +5	+20 to +5	-20 to -5
hold [a]	hold [a]	dec [b]	Increase post-cursor and increase peak-to-peak voltage	+40 to +10	+20 to +5	-20 to -5	-20 to -5
hold [a]	hold [a]	inc [c]	Decrease post-cursor and decrease amplitude	-40 to -10	-20 to -5	+20 to +5	+20 to +5

[a] hold: Requests no change be made to the coefficient, Equivalent to hold in SPL-2.
[b] dec: Request to make the coefficient more negative. Equivalent to decrement in SPL-2.
[c] inc: Request to make the coefficient more positive. Equivalent to increment in SPL-2.

The transmitter circuit responses specified in table 44 shall be measured with a zero-length test load as shown in figure 127. The test fixture is de-embedded back to output of the transmitter circuit ET. For de-embedding methods to remove non-ideal effects see E.5.

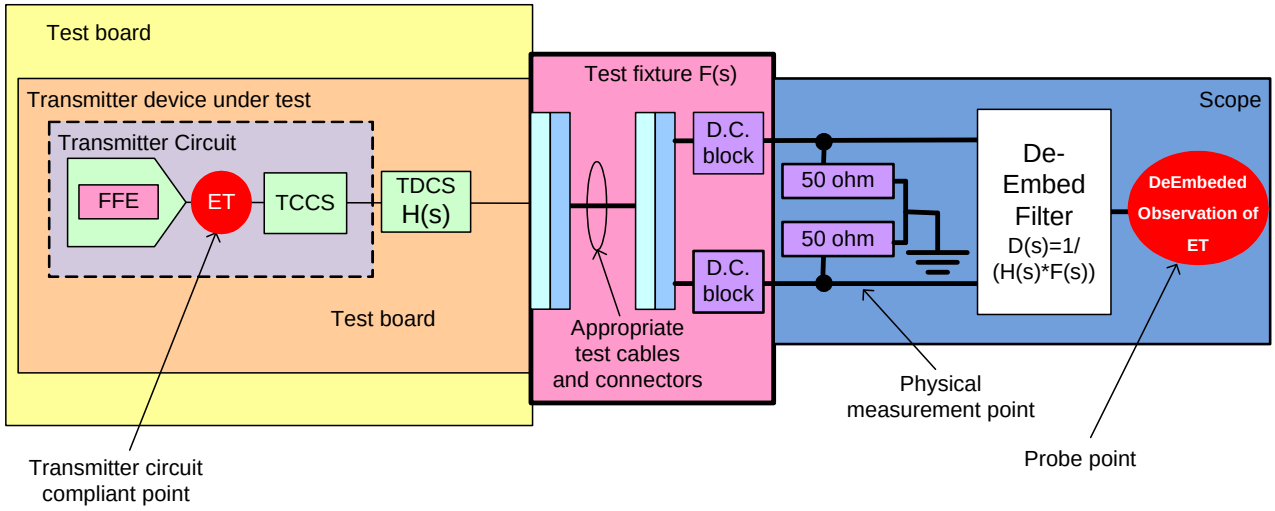


Figure 127 — Transmitter circuit compliance test configuration

All response specifications are based on differential measurements.The output waveform for a TRAIN_DONEprimitive (see SPL-2) is shown in figure 128 where:

a) T is the symbol period;
b) t_1 is the zero-crossing point of the rising edge of the positive 5 UI CID;
c) t_2 is the zero-crossing point of the falling edge of the positive 5 UI CID;
d) t_3 is the zero-crossing point of the falling edge of the positive 5 UI CID;
e) t_4 is the zero-crossing point of the rising edge of the positive 5 UI CID;
f) v_1 is the maximum voltage measured in the interval t_1 to t_1 + T;
g) v_2 is the average voltage measured in the interval t_1 + 2T to t_1 + 3T;
h) v_3 is the maximum voltage measured in the interval t_2 - T to t_2;
i) v_4 is the minimum voltage measured in the interval t_3 to t_3 + T;
j) v_5 is the average voltage measured in the interval t_3 + 2T to t_3 + 3T;
k) v_6 is the maximum voltage measured in the interval t_4 - T to t_4;
l) VMA is v_2 - v_5; and
m) v_{HL} is the peak-to-peak voltage measured in the interval t_1 to t_1 + 80T.

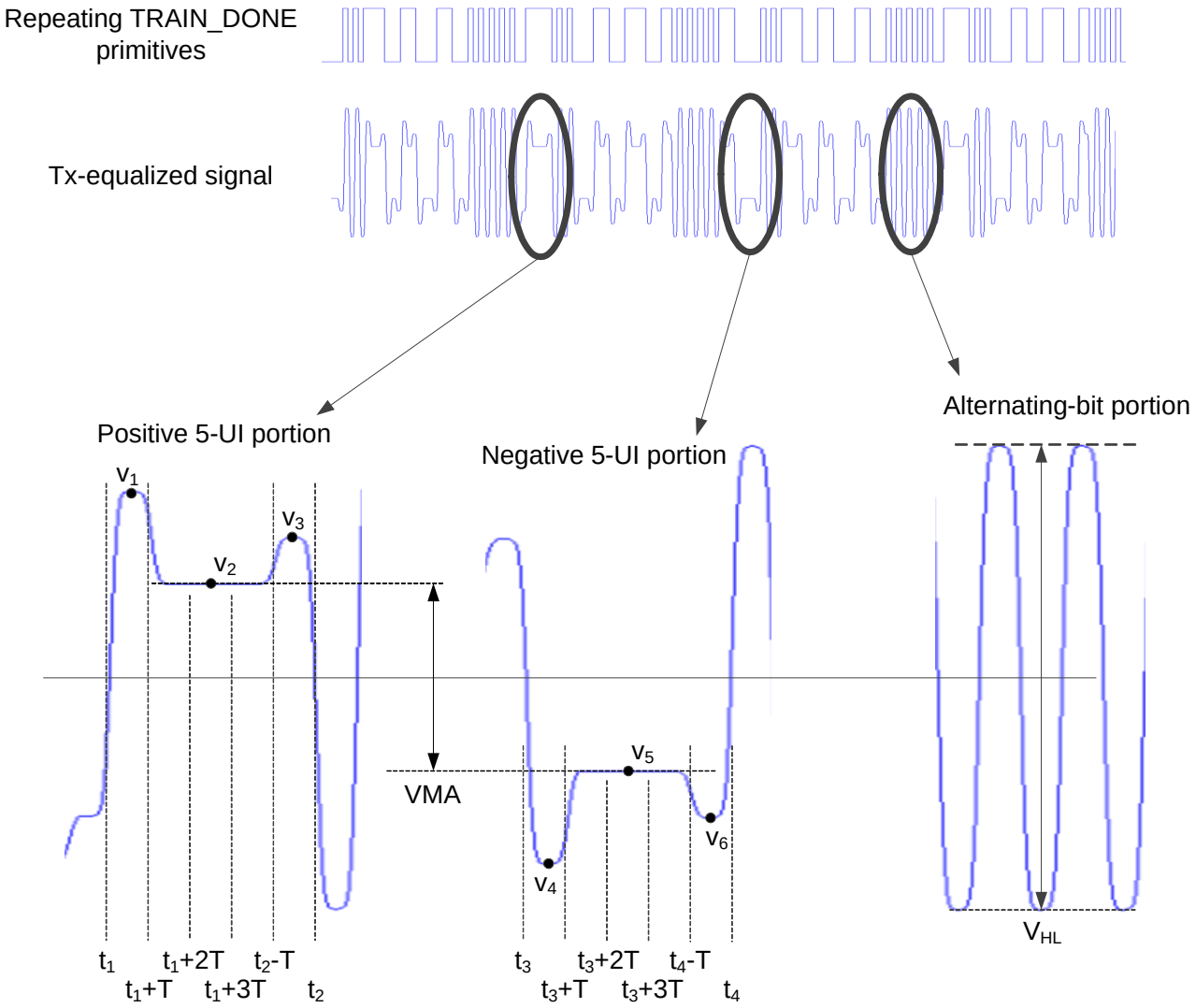


Figure 128 — 12 Gbps transmitter circuit output waveform

Equalization ratios are defined based on these voltages,

$$R_{post} = \frac{v_1}{v_2}$$

$$R_{pre} = \frac{v_3}{v_2}$$

Transmitter coefficient presets may be requested using an algorithm this is defined in the SPL-2 standard. Transmitter circuits that support 12 Gbps shall:

a) support the coefficient settings shown in table 45; and
b) provide equalization equivalent to the reference transmitter device (see 5.9.4.7.3).

Table 45 — Transmitter circuit coefficient presets at ET

Coefficient setting [a]	V_{HL} (mV) [b]		R_{pre} (V/V) [b]			R_{post} (V/V) [b]		
	Min.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.
normal [c]	-	-	-	-	-	-	-	-
reference_1 [d] [e]	850	1 200	~~2.23~~2.10	2.52	~~2.81~~2.97	~~3.12~~2.94	3.52	~~3.92~~4.16
reference_2 [e] [f]	850	1 200	~~1.12~~1.05	1.26	~~1.40~~1.49	~~1.27~~1.19	1.43	~~1.59~~1.68
no_equalization [e] [g]	850	1 200	~~0.88~~0.84	1.00	~~1.12~~1.19	~~0.88~~0.84	1.00	~~1.12~~1.19

Key:

Max. = Maximum
Min. = Minimum.
Nom. = Nominal

[a] The coefficient setting field in the TTIU (see SPL-2).
[b] All measurements shall be performed with a repeating TRAIN_DONE primitive (see SPL-2 and figure 127).
[c] See SPL-2.
[d] Equivalent to the reference transmitter setting transmitter circuit coefficient 1 (i.e., pre-cursor) set to -0.15, coefficient 2 (i.e., main cursor) set to 0.6, and coefficient 3 (i.e., post-cursor) set to -0.25 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[e] The reference7_1, reference_2, and no_equalization presets shall set the transmitter to its maximum peak-to-peak voltage (V_{p-p}).
[f] Equivalent to the reference transmitter setting transmitter circuit coefficient 1 set to -0.075, coefficient 2 set to 0.8, and coefficient 3 set to -0.125 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[g] Equivalent to the reference transmitter setting transmitter circuit coefficient 1 set to 0, coefficient 2 set to 1, and coefficient 3 set to 0 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.

5.9.4.7.2 12 Gbps Transmitter device S-parameter limits

Editor's Note 7: This section needs to be reviewed regarding 12 Gbps values.

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}$(f / 3 GHz)]]

where:

L is the minimum value (i.e., the low frequency asymptote);
H is the maximum value (i.e., the high frequency asymptote);

N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 46 defines the maximum limits for S-parameters of the 12 Gbps transmitter device.

Table 46 — 12 Gbps maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\|S_{CC22}\|$	-6.0	-5.0	0	13.3	100	6.0
$\|S_{DD22}\|$	-10	-7.9	0	13.3	100	6.0
$\|S_{CD22}\|$	-26	-12.7	-10	13.3	100	6.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See E.11.4.2.
[b] $|S_{DC22}|$ is not specified.
[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 129 shows the 12 Gbps transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 46.

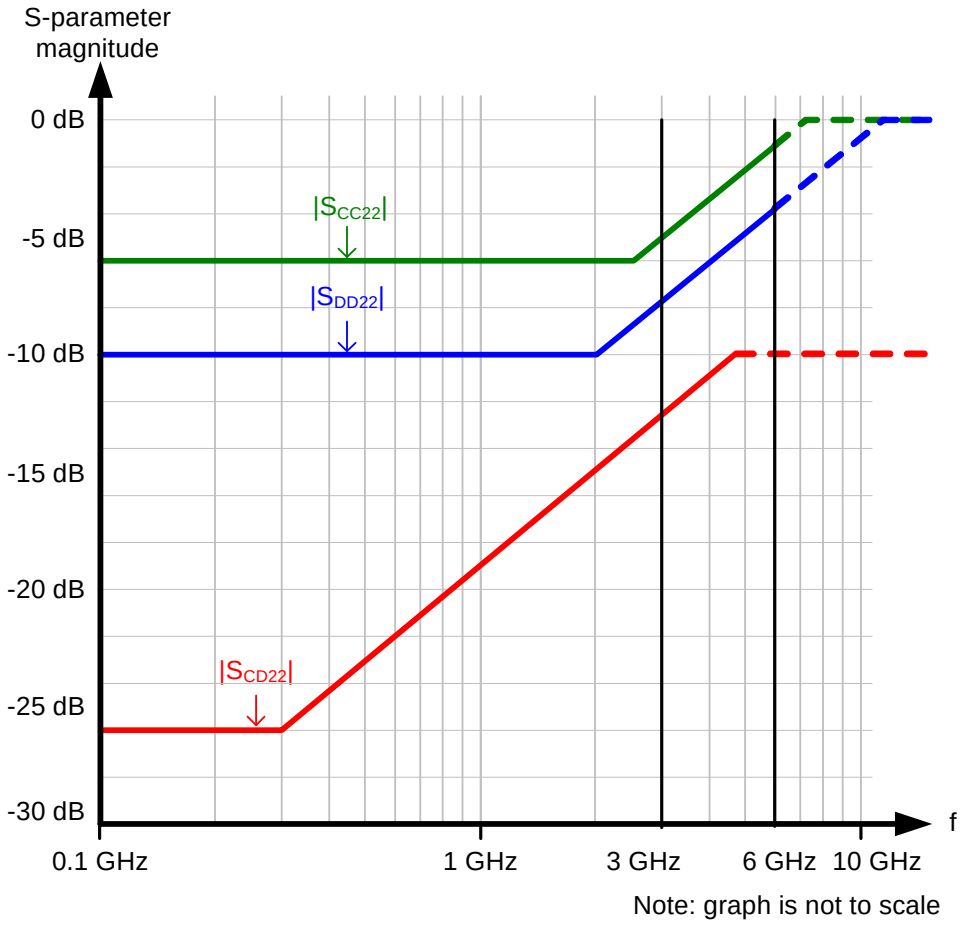


Figure 129 — 12 Gbps transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.9.4.7.3 12 Gbps reference transmitter device

The 12 Gbps reference transmitter device is a set of parameters and equalization filter architecture defining the electrical performance characteristics of a transmitter circuit used in simulation ~~to determine compliance of a passive TxRx connection (see 5.6.6)~~. Figure 130 illustrates the reference transmitter device.

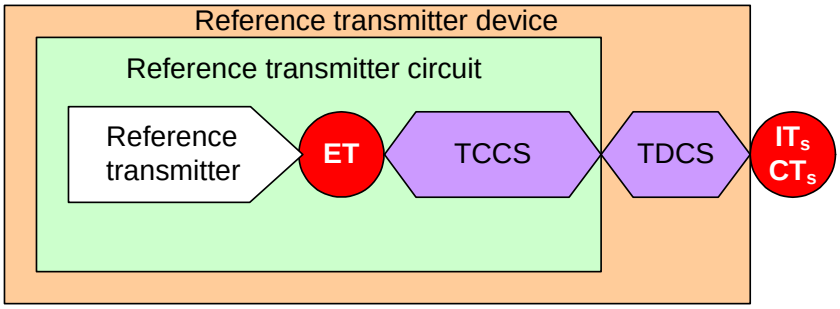


Figure 130 — 12 Gbps reference transmitter device

Figure 131 shows the reference transmitter generating the signal at ET. Passive TxRx connection segments TCCS and TDCS simulate the reference TxRx connection segment between ET and CTS or ET and ITS. See D.2 for the description of the reference TxRx connection segments.

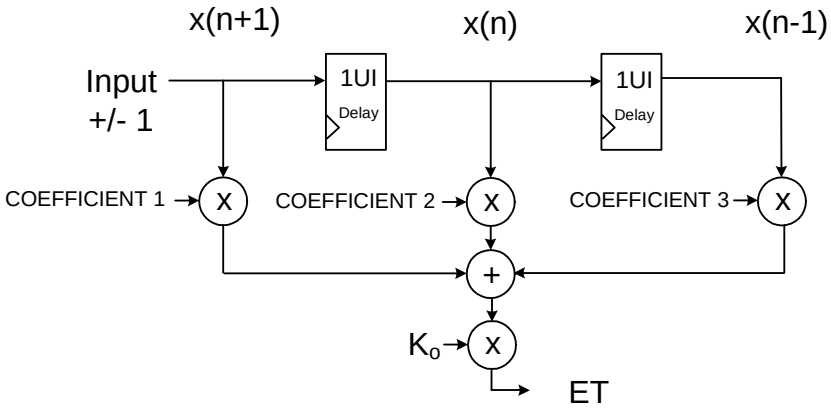


Figure 131 — 12 Gbps reference transmitter

During 12 Gbps ~~channel compliance~~end-to-end simulations ~~(section TBD1~~(see 5.8)~~)~~, the reference transmitter device parameters are optimized to maximize the eye opening at the output of the reference receiver device (5.9.5.7.3) using the procedure defined in ~~TBD2~~5.8.3. Table 47 defines the reference transmitter device characteristics. The reference transmitter device shall use the minimum peak-to-peak voltage and minimum rise/fall time. The input is a unitless stream of pulses representing transmitted data. The amplitude of these

pulses reach +1 or -1. The stream of pulses contains the jitter and rise/fall time characteristics defined in table 47.

Table 47 — 12 Gbps reference transmitter device characteristics at ET

Signal characteristic	Units	Minimum	Nominal	Maximum
Output gain (K_0)	V/V	0.425		
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		
Pre-cursor coefficient (i.e., coefficient 1) [a]	V/V	-0.15		0
VMA [b]	mV(P-P)	80		
Post-cursor coefficient (i.e., coefficient 3) [a]	V/V	-0.3		0
Rise/fall time [c]	ps	25		
RJ [d] [e]	UI			0.15
DJ [f]	UI			0.1

[a] V_{P-P} is constrained in the reference transmitter device by coefficient 2 = 1 - |coefficient 1| - |coefficient 3|.
[b] VMA = $2K_0$ ((C1 + C2 + C3)
[c] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2).
[d] 0.15 UI is 12.5 ps at 12 Gbps.
[e] RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[f] 0.1 UI is 8.3 ps at 12 Gbps.

5.9.4.7.4 Transmitter device end-to-end simulation characteristics for trained 12 Gbps

The end-to-end simulation procedure for transmitter devices connected to passive TxRx connections is as follows:

1) set the transmitter to output the IDLE pattern (see SPL-2);
2) set the transmitter to the no_equalization coefficient setting (see SPL-2);
3) capture the signal at IT or CT into a zero-length test load (see 5.7.2);
4) measure the total crosstalk amplitude 5.8.4 or extract crosstalk transfer functions (e.g., S-parameters);
5) connect TxRx connection segments, crosstalk segments, reference transmitter and reference receiver according to the reference end-to-end simulation schematic (see 5.8.2, and D.3);
6) set the reference transmitter equalization (see 5.8.3) and reference receiver DFE equalization (see 5.9.5.7.3); and
7) perform a linear simulation, including the effects of edge rates, ISI and crosstalk (see D.1).

The characteristics of the signal at specified points in the simulation are defined in table 48. See the reference transmitter device (see 5.9.4.7.3) for definitions of coefficient 1, coefficient 2 and coefficient 3 used in table 48. C1, C2 and C3 represent coefficient 1, coefficient 2 and coefficient 3, respectively.

Table 48 — Transmitter device charateristics for trained 12 Gbps at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a] [b] [c]	V/V	-0.15	0	ET
VMA [d] [e]	mV(P-P)	80	-	ET
Coefficient 3(i.e., C3) [a] [b] [f]	V/V	-0.3	0	ET
Reference pulse response cursor peak-to-peak amplitude [g]	mV(P-P)	72	-	ER
Vertical eye opening to reference pulse response cursor ratio [h] [i] [j]	%	55	-	ER
DFE coefficient amplitude to reference pulse response cursor ratio [k]	%	-75	75	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[b] C2 = 1 - |C1| - |C3|.

[c] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[d] VMA = $2K_0$ ((C1 + C2 + C3). See 5.9.4.7.3.

[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$((C1' - C1)^2 + (\text{~~C2~~}C3' - \text{~~C2~~}C3)^2)^{0.5}$

where:
C1' and C3' are values that satisfy the minimum VMA criterion.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 113.

[h] The vertical eye opening includes the effects of crosstalk (see D.1).

[i] The end-to-end simulation removes any remaining RJ and TJ (non-ISI) of the transmitter device.

[j] See figure 111.

[k] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(di)) divided by the reference pulse response cursor (see 5.9.5.7.3).

Editor's Note 8: The values in table 48 are based on initial simulations that did not include the complete end-to-end TxRx connection. Final values may be different, but remain consistent between table 27, table 48, and table 62.

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter-free reference transmitter with K_0 set to 1 (unit-less value) at the output of the transmitter device, using the transmitter device output as the input of the reference transmitter instead of the +1/-1 digitized stream (see figure 132). For non-separable TxRx connection segments, the reference simulation channel (i.e., <usage>_IT_RR) does not include the reference PICS.

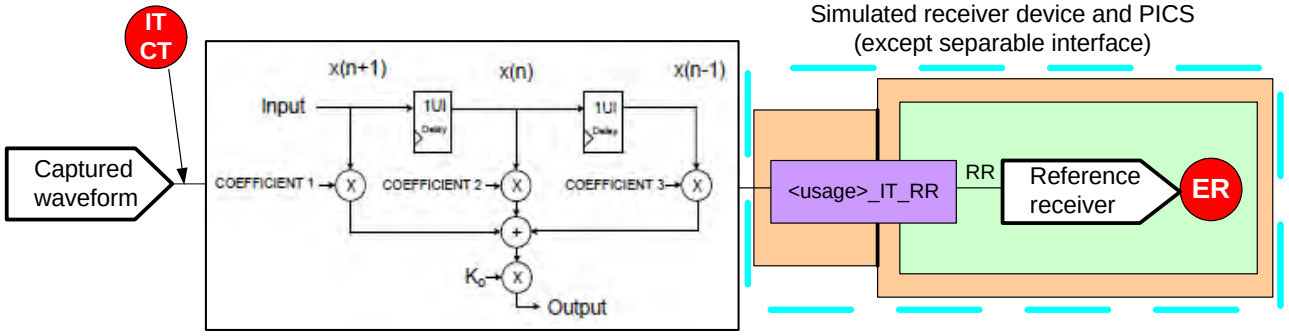


Figure 132 — Simulation of the reference transmitter from a captured signal

5.9.4.7.5 Transmitter device signal output characteristics at CT_S for 12 Gbps when an active cable is connected

Transmitter devices supporting trained 12 Gbps that are connected to an external cable connector shall support the signal characteristics specified in table 49 at CT_S when an active cable is connected.

Table 49 — Transmitter device signal output characteristics for 12 Gbps at CT_S when an active cable is connected

Signal characteristic	Units	CT_S
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 96) [a]	mV(P-P)	1200
Minimum eye opening (i.e., 2 × Z1 in figure 96) [a]	mV(P-P)	200
Maximum half of TJ (i.e., X1 in figure 96) [a b c]	UI	0.175
Maximum RJ [a c d]	UI	0.15
Center of bit time (i.e., X2 in figure 96)	UI	0.5

[a] All crosstalk sources shall be active with representative traffic during the measurement.
[b] The TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC enabled for a period of at least $33.\overline{3}$ s (i.e., a full SSC cycle).
[c] The measurement shall include the effects of the JTF (see 5.9.3.2).
[d] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.

5.9.4.8 Transmitter device signal output characteristics for OOB signals

Transmitter devices supporting SATA shall use SATA Gen1i, Gen2i, or Gen3i signal output levels (see SATA) during the first OOB sequence (see SPL-2) after a power on or hard reset. If the phy does not receive COMINIT within a hot-plug timeout (see SPL-2), then the transmitter device shall increase its transmit levels to the OOB signal output levels specified in table 50 and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence, then the transmitter device shall initiate another OOB sequence using SATA Gen1i, Gen2i, or Gen3i signal output levels. The transmitter device shall continue alternating between transmitting COMINIT using SATA Gen1i, Gen2i, or Gen3i signal output levels and transmitting COMINIT with SAS signal output levels until the phy receives COMINIT.

If the phy both transmits and receives COMSAS (i.e., a SAS phy or expander phy is attached), then the transmitter device shall set its transmit levels to the SAS signal output levels (see 5.9.4.4, 5.9.4.5, and 5.9.4.6) prior to beginning the SAS speed negotiation sequence (see SPL-2). If transmitter device had been using SATA Gen1i, Gen2i, or Gen3i signal output levels, this mode transition (i.e., output voltage change) may result in a transient (see 5.9.2) during the idle time between COMSAS and the SAS speed negotiation sequence.

If the transmitter device is using SAS signal output levels and the phy does not receive COMSAS (i.e., a SATA phy is attached), then the transmitter device shall set its transmit levels to the SATA Gen1i, Gen2i, or Gen3i signal output levels and restart the OOB sequence.

Transmitter devices that do not support SATA or that have optical mode enabled shall transmit OOB signals using SAS signal output levels. In low phy power conditions (see SPL-2) the output common mode specification OOB common mode delta (see table 50) is relaxed to enable transmitter device power savings. During low phy power conditions, the transmitter device should reduce its output swing level to save power. Before exiting a low phy power condition the transmitter device shall wait for its common mode to settle.

Table 50 defines the transmitter device signal output characteristics for OOB signals.

Table 50 — Transmitter device signal output characteristics for OOB signals

Characteristic	Units	IT	CT
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 118) [a]	mV(P-P)	1 600	
OOB offset delta [b] [c]	mV	± 25	
OOB common mode delta [c] [d]	mV	± 50	
Minimum OOB burst amplitude [e], if SATA is not supported	mV(P-P)	240 [f]	
Minimum OOB burst amplitude [e], if SATA is supported	mV(P-P)	240 [f] [g]	N/A

[a] The recommended maximum peak to peak voltage is 1 200 mV(P-P).
[b] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.
[c] This is not applicable when optical mode is enabled or in low phy power conditions.
[d] The maximum difference in the average of the common-mode voltage between the burst times and the idle times of an OOB signal.
[e] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst as measured with each test load at IT and CT.
[f] The OOB burst contains either 1.5 Gbps repeating 0011b or 1100b pattern (e.g., D24.3), 1.5 Gbps ALIGN (0) primitives, or 3 Gbps ALIGN (0) primitives (see SPL-2 and SATA).
[g] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.9.5 Receiver device characteristics

5.9.5.1 Receiver device characteristics overview

The receiver device shall operate within the required BER (see 5.6.1) when a signal with valid voltage and timing characteristics is delivered to the receiver device compliance point from a nominal 100 ohm source. The received signal shall be considered valid if it meets the voltage and timing limits specified in table 53 (see 5.9.5.4) for untrained 1.5 Gbps and 3 Gbps and table 57 (see 5.9.5.7.1) for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps. See SATA for untrained 6 Gbps (i.e., SATA Gen3i) receiver device requirements.

Additionally, for untrained 1.5 Gbps and 3 Gbps the receiver device shall operate within the required BER when the signal has additional SJ present as specified in table 55 (see 5.9.5.6) with the common-mode signal V_{CM} as specified in table 51 (see 5.9.1). Jitter tolerance for receiver device compliance points is shown in figure 120 (see 5.9.3.5). Figure 120 assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver device, the additional 0.1 UI of SJ may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiver device. The additional jitter reduces the eye opening in both voltage and time. For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, the additional jitter and common mode voltage is included in the stressed receiver device jitter tolerance test (see 5.9.5.7.6).

See E.10 for a methodology for measuring receiver device signal tolerance.

A receiver device shall provide equivalent performance to the reference receiver device (see 5.9.5.7.3) and shall operate within the required BER when attached to:

a) any transmitter device compliant with this standard (see 5.9.4); and
b) any TxRx connection compliant with this standard (see 5.6).

5.9.5.2 Receiver device coupling requirements

Coupling requirements for receiver devices are as follows:

a) all receiver devices (i.e., attached to IR or CR compliance points) shall be A.C. coupled to the interconnect through a receive network.

See table 31 (see 5.9.1) for the coupling capacitor value.

5.9.5.3 Receiver device general electrical characteristics

Table 51 defines the receiver device general electrical characteristics.

Table 51 — Receiver device general electrical characteristics

Characteristic	Units	1.5 Gbps	3 Gbps	6 Gbps	12 Gbps
Physical link rate long-term accuracy [a] tolerance at IR if SATA is not supported	ppm	± 100			
Physical link rate long-term accuracy [a] tolerance at IR if SATA is supported	ppm	± 350			
Physical link rate SSC modulation tolerance at IR and CR	ppm	See table 70 in 5.9.6.3			
Maximum receiver device transients [b]	V	± 1.2			
Minimum receiver A.C. common-mode voltage tolerance V_{CM} [c]	mV(P-P)	150			
Receiver A.C. common-mode frequency tolerance range F_{CM} [c] [d]	MHz	2 to 200		2 to 3 000	2 to 6 000

[a] Physical link rate long-term accuracy should be measured using a frequency counter with adequate resolution (e.g., 100 Hz).
[b] See 5.9.2 for transient test circuits and conditions.
[c] Receiver devices shall tolerate sinusoidal common-mode noise components within the peak-to-peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[d] The measurement shall be made with a channel equivalent to the channel used in the zero-length test load (see figure 99) (see 5.7.2).

Table 52 defines the receiver device termination characteristics.

Table 52 — Receiver device termination characteristics

Characteristic	Units	Untrained		Trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps
		1.5 Gbps	3 Gbps	
Differential impedance [a b c]	ohm	100 ± 15		See 5.9.5.7.1
Maximum differential impedance imbalance [a b c d]	ohm	5		See 5.9.5.7.2 [e]
Maximum receiver termination time constant [a b c]	ps	150	100	N/A
Common-mode impedance [a b]	ohm	20 minimum 40 maximum		See 5.9.5.7.1

[a] All receiver device termination measurements are made through mated connector pairs.

[b] The receiver device termination impedance specification applies to all receiver devices in a TxRx connection and covers all time points between the connector nearest the receiver device, the receiver device, and the transmission line terminator. This measurement shall be made from that connector.

[c] At the time point corresponding to the connection of the receiver device to the transmission line, the input capacitance of the receiver device and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. With impedance measured using amplitude in units of ρ (i.e., the reflection coefficient, a dimensionless unit) and duration in units of time, the area of the impedance dip caused by this capacitance is the receiver termination time constant. The receiver termination time constant shall not be greater than the values shown in this table.

An approximate value for the receiver termination time constant is given by the following equation:

RTTC = amp × width

where:

RTTC receiver termination time constant in seconds;

amp amplitude of the dip in units of ρ (i.e., the difference between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point); and

width width of the dip in units of time, as measured at the half amplitude point.

The value of the receiver device excess input capacitance is given by the following equation:

$$C = \frac{RTCC}{(R_0 \parallel R_R)}$$

where:

C receiver device excess input capacitance in farads;

RTCC receiver termination time constant in seconds;

R_0 transmission line characteristic impedance in ohms;

R_R termination resistance at the receiver device in ohms; and

$(R_0 \parallel R_R)$ parallel combination of R_0 and R_R.

[d] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.

[e] Measurement replaced by S_{CD11} specifications (i.e., differential to common mode conversion).

5.9.5.4 Delivered signal characteristics for untrained 1.5 Gbps and 3 Gbps

Table 53 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.7.2) at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbps and 3 Gbps. These also serve as the required signal tolerance characteristics of the receiver device. For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, see 5.9.5.7.

Table 53 — Delivered signal characteristics for untrained 1.5 Gbps and 3 Gbps as measured with the zero length test load at IR and CR

Signal characteristic	Units	IR, untrained		CR, untrained	
		1.5 Gbps	3 Gbps	1.5 Gbps	3 Gbps
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 119) if a SATA phy is not attached	mV(P-P)	1 600		1 600	
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 119) if a SATA phy is attached	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 119), if a SATA phy is not attached	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 119), if a SATA phy using Gen1i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.7.3)	mV(P-P)	225 [a]	N/A	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 119), if a SATA phy using Gen2i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.7.3)	mV(P-P)	N/A	175 [a]	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 119), if a SATA phy is attached and the TxRx connection is characterized with the low-loss TCTF test load (see 5.7.4)	mV(P-P)	275 [a]		N/A	
Jitter tolerance (see figure 120 in 5.9.3.5) [b] [c]	N/A	See table 55 in 5.9.5.6			
Maximum half of TJ (i.e., X1 in figure 119) [d]	UI	0.275			
Center of bit time (i.e., X2 in figure 119)	UI	0.50			
Maximum intra-pair skew [e]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[c] SSC shall be enabled if the receiver device supports being attached to SATA. Jitter setup shall be performed prior to application of SSC.

[d] The value for X1 shall be half the value given for TJ in table 54. When SSC is disabled, the test or analysis shall include the effects of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667).

[e] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal at the probe points.

5.9.5.5 Maximum delivered jitter for untrained 1.5 Gbps and 3 Gbps

Table 54 defines the maximum jitter the system shall deliver to the receiver device at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbps and 3 Gbps. For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, see 5.9.5.7.6.

Table 54 — Maximum delivered jitter for untrained 1.5 Gbps and 3 Gbps at IR and CR

Signal characteristic [a] [b]	Units	Untrained	
		1.5 Gbps	3 Gbps
Deterministic jitter (DJ) [c]	UI	0.35	
Total jitter (TJ) [c] [d] [e]	UI	0.55	

[a] All DJ and TJ values are level 1 (see MJSQ).
[b] The values for jitter in this table are measured at the average signal amplitude point.
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.9.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] TJ is specified at a CDF level of 10^{-12}.
[e] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.
Jitter peak-to-peak measured < (maximum TJ - |Asymmetry|)

5.9.5.6 Receiver device jitter tolerance for untrained 1.5 Gbps and 3 Gbps

Table 55 defines the amount of jitter the receiver device shall tolerate at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbps and 3 Gbps. Receiver device jitter testing shall be performed with the maximum (i.e., slowest) rise/fall times, minimum signal amplitude, and maximum TJ, and should be performed with normal activity in the receiver device (e.g., with other transmitter circuits and receiver circuits on the same board as the receiver device performing normal activity) with SSC enabled if SSC is supported by the receiver device. Jitter setup shall be performed prior to application of SSC. For trained 1.5 Gbps, 3 Gbps, and 6 Gbps, see 5.9.5.7.6.

Table 55 — Receiver device jitter tolerance for untrained 1.5 Gbps and 3 Gbps at IR and CR

Signal characteristic	Units	Untrained	
		1.5 Gbps	3 Gbps
Applied sinusoidal jitter (SJ) from f_c to f_{max} [a]	UI	0.10 [e]	0.10 [f]
Deterministic jitter (DJ) [b] [c]	UI	0.35 [g]	0.35 [h]
Total jitter (TJ) [b] [c] [d]	UI	0.65	

[a] The jitter values given are normative for a combination of applied SJ, DJ, and TJ that receiver devices shall be able to tolerate without exceeding the required BER (see 5.6.1). Receiver devices shall tolerate applied SJ of progressively greater amplitude at lower frequencies than f_c, according to figure 133, with the same DJ and RJ levels as were used from f_c to f_{max}.
[b] All DJ and TJ values are level 1 (see MJSQ).
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.9.3.4. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] No value is given for RJ. For compliance with this standard, the actual RJ amplitude shall be the value that brings TJ to the stated value at a probability of 10^{-12}. The additional 0.1 UI of applied SJ is added to ensure the receiver device has sufficient operating margin in the presence of external interference.
[e] Applied sinusoidal swept frequency for 1.5 Gbps: 900 kHz to 5 MHz.
[f] Applied sinusoidal swept frequency for 3 Gbps: 1 800 kHz to 7.5 MHz.
[g] The measurement bandwidth for 1.5 Gbps shall be 900 kHz to 750 MHz.
[h] The measurement bandwidth for 3 Gbps shall be 1 800 kHz to 1 500 MHz.

Figure 133 defines the applied SJ for table 55.

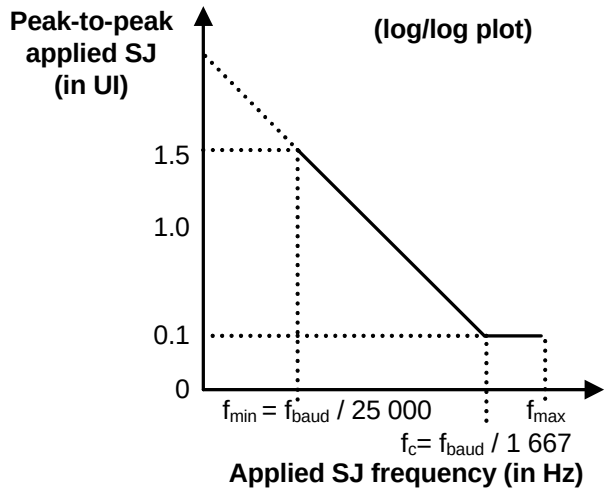


Figure 133 — Applied SJ for untrained 1.5 Gbps and 3 Gbps

Table 56 defines f_{min}, f_c, and f_{max} for figure 133. f_{baud} is defined in table 31 (see 5.9.1).

Table 56 — f_{min}, f_c, and f_{max} for untrained 1.5 Gbps and 3 Gbps

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbps	60 kHz	900 kHz	5 MHz
3 Gbps	120 kHz	1 800 kHz	7.5 MHz

5.9.5.7 Receiver device and delivered signal characteristics for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps

5.9.5.7.1 Delivered signal characteristics for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps

Table 57 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.7.2), unless otherwise specified, attached at the receiver device compliance point (i.e., IR or CR) for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps. These also serve as the required signal tolerance characteristics of the receiver device. All specifications are based on differential measurements.

Table 57 — Delivered signal characteristics for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps at IR and CR

Characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage for trained 1.5 Gbps, 3 Gbps, and 6 Gbps [a] [b]	mV(P-P)			1 200
Non-operational input voltage	mV(P-P)			2 000
Reference differential impedance [c]	ohm		100	
Reference common mode impedance [c]	ohm		25	

[a] See 5.9.4.6.6 for measurement method.
[b] During OOB, SNW-1, SNW-2, and SNW-3 (see SPL-2), the untrained 1.5 Gbps and 3 Gbps specifications in 5.9.5.4 apply.
[c] For receiver device S-parameter characteristics, see 5.9.5.7.2.

5.9.5.7.2 Receiver device S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [L, \min [H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz})]]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 58 defines the maximum limits for S-parameters of the receiver device.

Table 58 — Maximum limits for S-parameters at IR or CR

Characteristic [a]	L [b] (dB)	N [b] (dB)	H [b] (dB)	S [b] (dB / decade)	f_{min} [b] (MHz)	f_{max} [b] (GHz)
$\|S_{CC11}\|$	-6.0	-5.0	0	13.3	100	6.0
$\|S_{DD11}\|$	-10	-7.9	0	13.3	100	6.0
$\|S_{CD11}\|$	-26	-12.7	-10	13.3	100	6.0

[a] $|S_{DC11}|$ is not specified.
[b] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 134 shows the receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in table 58.

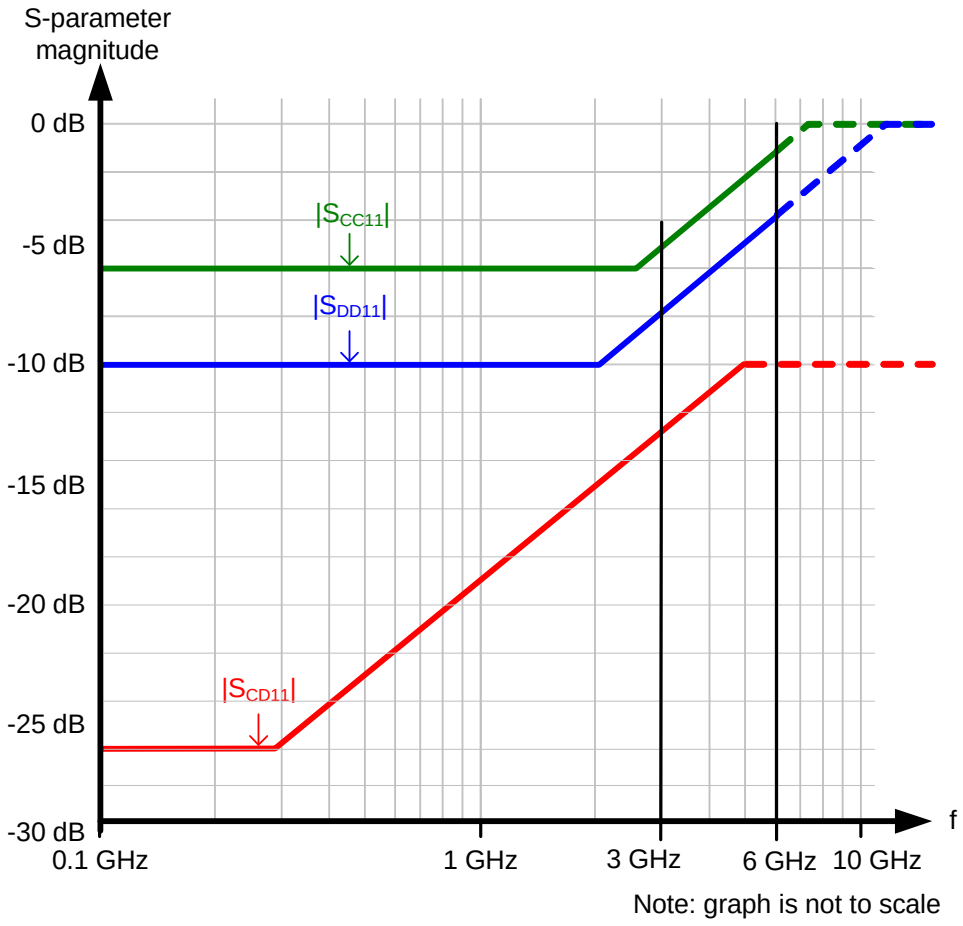


Figure 134 — Receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits

5.9.5.7.3 Reference receiver device characteristics

5.9.5.7.3.1 Reference receiver device overview

The reference receiver device is a set of parameters defining the electrical performance characteristics of a receiver device used in simulation to:

a) determine compliance of a transmitter device (see 5.9.4.6 and 5.9.4.7); and
b) determine compliance of a TxRx connection (see 5.6.5 and 5.6.6).

Figure 135 shows the reference receiver device for trained 1.5 Gbps, 3 Gbps, and 6 Gbps.

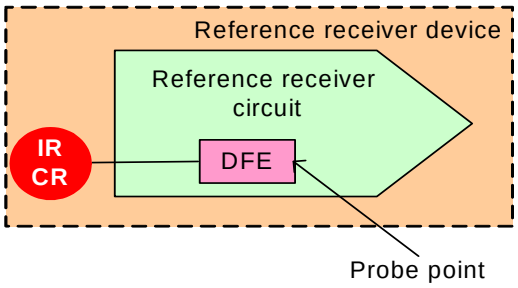


Figure 135 — Reference receiver device for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

Figure 136 shows the reference receiver device for trained 12 Gbps. Passive TxRx connection segments RCCS and RDCS simulate the reference TxRx connection segment between IR and RR or CR and RR. See D.2 for the description of the reference TxRx connection segments.

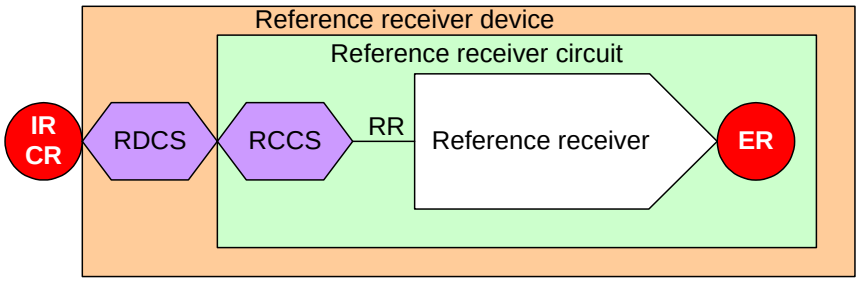


Figure 136 — Reference receiver device for trained 12 Gbps

For trained 12 Gbps, the reference receiver device applies the reference receiver equalization (see 5.9.5.7.3.3), samples the incoming data according to a reference sampling clock (see 3.1.81), and performs the reference DFE equalization.

For trained 1.5 Gbps, 3 Gbps and 6 Gbps, the reference receiver circuit performs the reference DFE equalization at the center of the eye.

The signal at the probe point or at ER is an analog signal.

5.9.5.7.3.2 Reference receiver device DFE

The reference receiver device includes a multiple tap DFE with infinite precision taps and unit interval tap spacing. The reference coefficient adaptation algorithm is the LMS algorithm. The DFE may be modeled as:

$$y_k = x_k - \sum_{i=1}^{Ndfe} d_i \times \mathrm{sgn}(y_{k-i})$$

where:

- y is the equalizer differential output voltage;
- x is the equalizer differential input voltage;
- d is the equalizer feedback coefficient;
- k is the sample index in UI; and
- Ndfe is the number of equalizer DFE taps.

Ndfe = 3 for the trained 1.5 Gbps, 3 Gbps, and 6Gbps reference receiver device. Ndfe = 5 for the 12 Gbps reference receiver device.

The trained 1.5 Gbps, 3 Gbps, and 6Gbps reference receiver device feedback coefficients (i.e., d_i) have absolute magnitudes that are less than 0.5 times the peak of the equivalent pulse response of the reference receiver device. The 12 Gbps reference receiver device equalizer feedback coefficients (i.e., d_i) have absolute magnitudes that are less than 0.75 times the peak of the equivalent pulse response of the reference receiver device.

NOTE 18 - For more information on DFE and LMS, see John R. Barry, Edward A. Lee, and David G. Messerschmitt. *Digital Communication - Third Edition*. Kluwer Academic Publishing, 2003. See http://users.ece.gatech.edu/~barry/digital.

5.9.5.7.3.3 Reference receiver device equalization for trained 12 Gbps

The reference receiver applies a filter composed of three cascaded identical equalization stages. Each of these stages has the characteristics described in table 59. The frequency response of each stage is of the form:

$H(s) = (1 + s/(2\pi \times fz_0)) / [(1 + s/(2\pi \times fp_0)) \times (1 + s/(2\pi \times fp_1))]$

where:

s	represents $2\pi \times f \times (-1)^{0.5}$;
fz_0	is the zero corner frequency;
fp_0	is the first pole corner frequency; and
fp_1	is the second pole corner frequency.

Table 59 — Reference receiver equalization stage characteristics for trained 12 Gbps

Characteristic	Units	Value
Zero corner frequency (fz_0)	GHz	2.5
First pole corner frequency (fp_0)	GHz	4
Second pole corner frequency (fp_1)	GHz	10

5.9.5.7.4 Reference receiver device termination characteristics for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

The following Touchstone model of the reference receiver device termination is included with this standard:

a) SAS2_RxRefTerm.s4p.

Figure 137 shows the S-parameters of the reference receiver device termination model for trained 1.5 Gbps, 3 Gbps, and 6 Gbps.

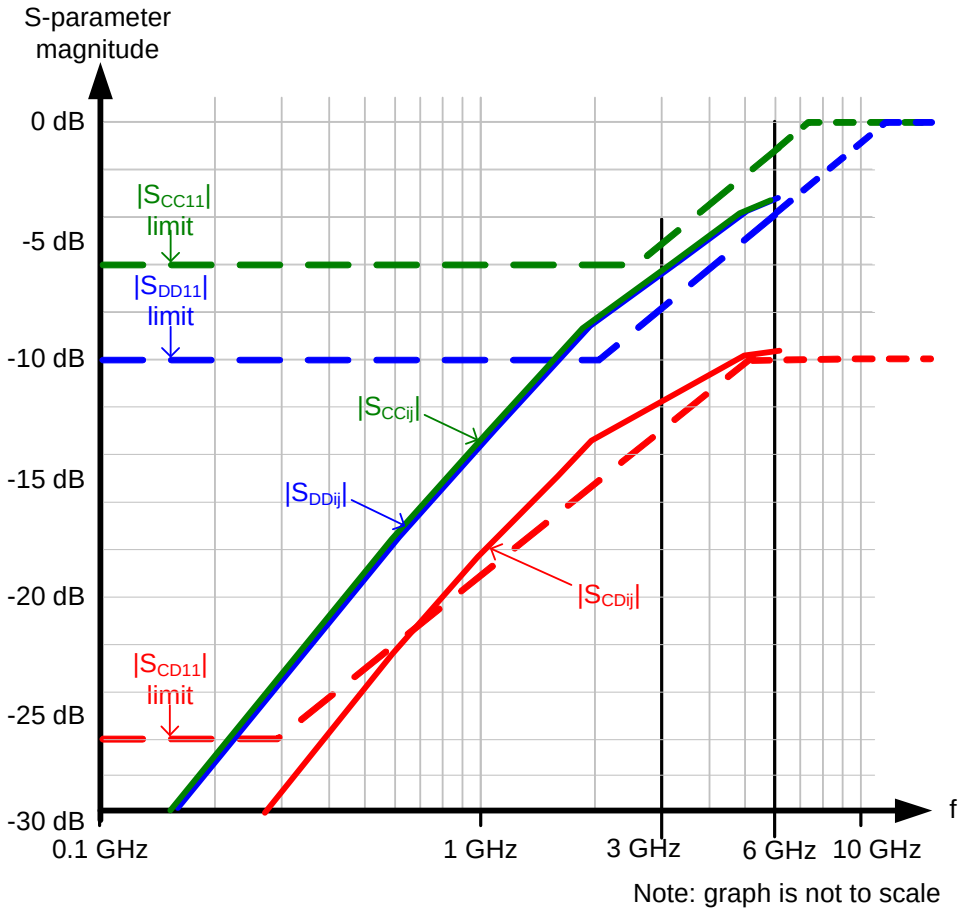


Figure 137 — Reference receiver device termination S-parameters for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

The Touchstone model does not exactly match the $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in 5.9.5.7.2 at all frequencies; it is a reasonable approximation for use in simulations. See Annex F for a description of how the Touchstone model was created.

5.9.5.7.5 Reference receiver device termination characteristics for trained 12 Gbps

The termination characteristics of the reference receiver device for trained 12 Gbps are determined by the reference TxRx connection segments used in the simulations (see D.2). The reference transmitter presents an ideal termination at RR.

5.9.5.7.6 Stressed receiver device jitter tolerance test

5.9.5.7.6.1 Stressed receiver device jitter tolerance test overview for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

A receiver device shall pass the stressed receiver device jitter tolerance test described in this subclause.

The stressed receiver device jitter tolerance test shall be applied at the receiver device compliance point (i.e., IR or CR) as a means to perform physical validation of predicted performance of the receiver device. Any implementation of the stressed signal generation hardware is permitted for the stressed receiver signal as long as it provides the ISI-stressed signal with jitter and noise as defined in this subclause.

Figure 138 shows the block diagram of the stressed receiver device jitter tolerance test.

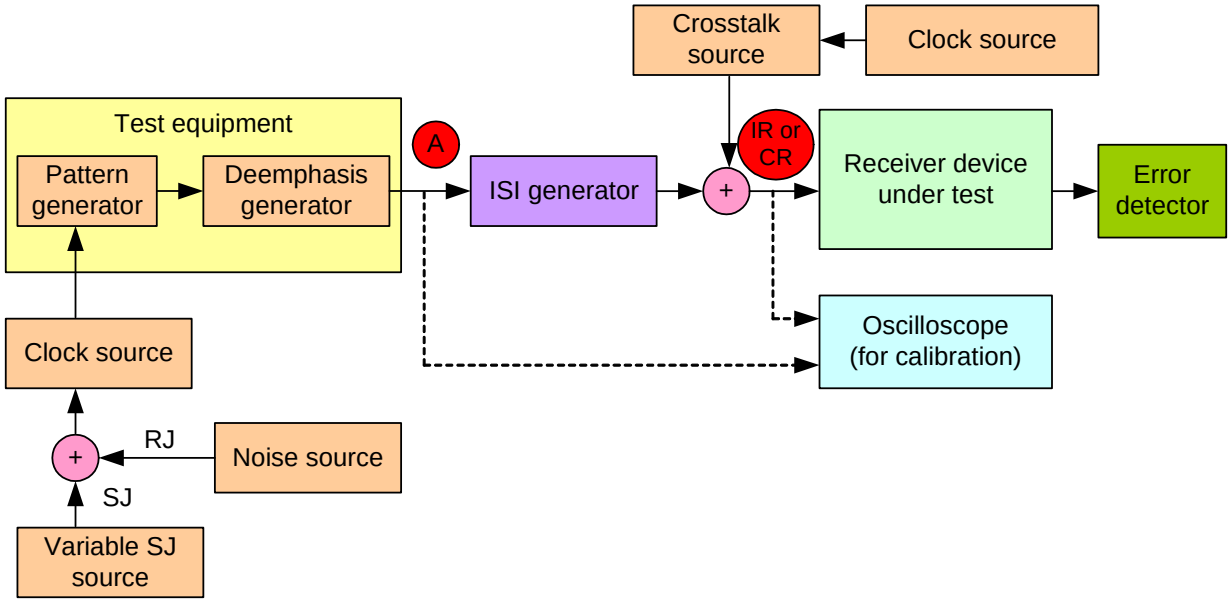


Figure 138 — Stressed receiver device jitter tolerance test block diagram

The ISI generator shall be representative of, and at least as stressful as, the reference transmitter test load (see 5.7.5).

NOTE 19 - The reference transmitter test load (see 5.7.5), with a nominal $|S_{DD21}|$ of -15 dB at (f_{baud} / 2), may be used as a component of the ISI generator.

The receiver device under test demonstrates its ability to compensate for channel intersymbol interference (ISI) representative of the reference transmitter test load (see 5.7.5) while subjected to the budgeted jitter and crosstalk sources.

Table 60 defines the stressed receiver device jitter tolerance test characteristics. Unless otherwise noted, characteristics are measured at IR or CR in figure 138.

Table 60 — Stressed receiver device jitter tolerance test characteristics

Characteristic	Units	Minimum	Nominal	Maximum	Reference
Tx peak to peak voltage [a]	mV(P-P)		850		5.9.4.6.1
Transmitter equalization [a]	dB		2		5.9.4.6.6
Tx RJ [b c d]	UI	0.135 [e]	0.150 [f]	0.165 [g]	5.9.4.6.1
Tx SJ [c]	UI	See figure 142 and figure 143			5.9.5.7.6.9
WDP at 6 Gbps [b h]	dB	13		14.5	
WDP at 3 Gbps [b h]	dB	7		8.5	
WDP at 1.5 Gbps [b h]	dB	4.5		6	
D24.3 eye opening [b i]	mV(P-P)	200	215	230	5.9.3.4
NEXT offset frequency [i j k]	ppm	2 500			
Total crosstalk amplitude [i k]	mV_{rms}	4			
Receiver device configuration [l]					

[a] For a characteristic with only a nominal value, the test setup shall be configured to be as close to that value as possible while still complying with other characteristics in this table.

[b] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.

[c] Measured at point A in figure 138.

[d] Measured after application of the JTF (see 5.9.3.2).

[e] 0.135 UI is ~~11.25 ps at 12 Gbps,~~ 22.5 ps at 6 Gbps, 45 ps at 3 Gbps, and 90 ps at 1.5 Gbps.

[f] 0.150 UI is ~~12.5 ps at 12 Gbps,~~ 25 ps at 6 Gbps, 50 ps at 3 Gbps, and 100 ps at 1.5 Gbps.

[g] 0.165 UI is ~~13.75 ps at 12 Gbps,~~ 27.5 ps at 6 Gbps, 55 ps at 3 Gbps, and 110 ps at 1.5 Gbps.

[h] This value is obtained by simulation with SASWDP (see Annex B). BUJ and RJ shall be minimized for WDP simulations. The WDP value is a characterization of the signal output within the reference receiver device (see 5.9.5.7.3) after equalization.

[i] The repeating 0011b or 1100b pattern (e.g., D24.3) eye opening pertains to the delivered signal at IR or CR. Figure 139 defines this value in an eye diagram.

[j] The NEXT source may use SSC modulation rather than have a fixed offset frequency.

[k] Observed with a histogram of at least 1 000 samples. Additional pseudo-random crosstalk shall be added, if needed, to meet the total crosstalk amplitude specification.

[l] All transmitter devices and receiver devices adjacent to the receiver device under test shall be active with representative traffic with their maximum amplitude and maximum frequency of operation.

Figure 139 shows the stressed receiver device jitter tolerance test repeating 0011b or 1100b pattern (e.g., D24.3) eye opening.

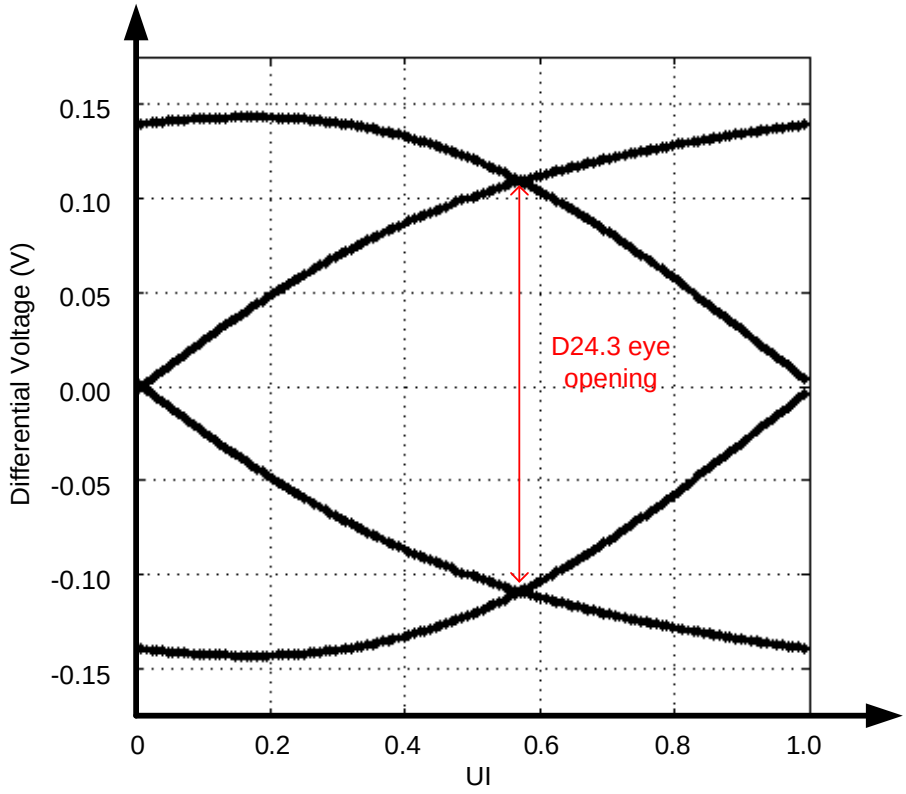


Figure 139 — Stressed receiver device jitter tolerance test D24.3 eye opening

5.9.5.7.6.2 Stressed receiver device jitter tolerance test procedure for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

The stressed receiver device jitter tolerance test procedure is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.9.5.7.6.3;
2) calibrate the crosstalk source as specified in 5.9.5.7.6.4;
3) attach the test equipment and ISI generator and the crosstalk source to the receiver device under test;
4) configure the pattern generator to transmit a Train_RX-SNW pattern (see SPL-2);
5) allow the receiver device to complete the Train_RX-SNW;
6) configure the applied SJ as specified in 5.9.5.7.6.9;
7) configure the pattern generator to transmit CJTPAT (see Annex A); and
8) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

This procedure requires the receiver under test to train during Train_RX-SNW as specified in SPL-2. This training may be performed by:

a) using the mechanisms defined in SPL-2; or
b) using an equivalent procedure.

The use of an equivalent procedure is outside the scope of this standard.

Table 61 defines the number of bits that shall be received with a certain number of errors to have a confidence level of 95 % that the BER is less than 10^{-12}.

Table 61 — Number of bits received per number of errors for desired BER

Number of errors	Number of bits
0	3.00×10^{12}
1	4.74×10^{12}
2	6.30×10^{12}
3	7.75×10^{12}
4	9.15×10^{12}
5	1.05×10^{13}

5.9.5.7.6.3 Test equipment and ISI generator calibration for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

The test equipment and ISI generator calibration procedure is as follows:

1) ensure that the ISI generator has an $|S_{DD21}|$ comparable to that of the reference transmitter test load (see 5.7.5). $|S_{DD21}|$ delivered by the ISI generator shall be measured by observing the D24.3 eye opening at IR or CR as defined in table 60;
2) attach the test equipment and ISI generator to a zero-length test load, where its signal output is captured by an oscilloscope;
3) disable the crosstalk source;
4) disable the variable SJ source and the random noise source;

NOTE 20 - WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5) configure the pattern generator to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2);
6) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Waveform averaging shall be used to minimize the impact of measurement noise and jitter on the WDP calculations;
7) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to ‘SAS2_LDP’; and
8) adjust the ISI generator until the WDP is within the range defined in table 60 (see 5.9.5.7.6.1).

5.9.5.7.6.4 Crosstalk source calibration for trained 1.5 Gbps, 3 Gbps, and 6 Gbps

The crosstalk source calibration procedure is as follows:

1) attach the test equipment and ISI generator and the crosstalk source to a zero-length test load, where its signal output is captured by an oscilloscope;
2) disable the pattern generator;
3) enable the crosstalk source;
4) set the center frequency of the crosstalk source to be frequency offset from the pattern generator to sweep all potential relative phase alignments between the crosstalk source and the signal from the ISI generator;
5) generate a histograph of the signal delivered to the test equipment; and
6) adjust the crosstalk source until the crosstalk amplitude complies with table 60 (see 5.9.5.7.6.1).

5.9.5.7.6.5 Stressed receiver device jitter tolerance test procedure for trained 12 Gbps

The stressed receiver device jitter tolerance test procedure is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.9.5.7.6.6;

2) calibrate the crosstalk source as specified in 5.9.5.7.6.7;
3) attach the test equipment and ISI generator and the crosstalk generator to the receiver device under test;
4) configure the devices on the receiver device board to transmit and receive normal traffic, including the transmitter device associated with the receiver device under test;
5) configure the pattern generator to transmit a Train_TX-SNW pattern (see SPL-2);
6) allow the receiver to complete the Train_TX-SNW;
7) configure the pattern generator to transmit a Train_RX-SNW pattern (see SPL-2);
8) allow the receiver to complete the Train_RX-SNW;
9) configure the applied RJ as specified in 5.9.5.7.6.8;
10) configure the applied SJ as specified in 5.9.5.7.6.9;
11) configure the pattern generator to transmit CJTPAT (see Annex A); and
12) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

The configuration of the transmitter device associated with the receiver device under test may be performed after the receiver training completes.

This procedures requires the receiver under test to train during Train_TX-SNW and Train_RX-SNW as specified in SPL-2 (see figure Fh). This training may be performed by

a) a) using the mechanisms defined in SPL-2; or
b) b) using an equivalent procedure.

The test equipment shall be capable of adjusting its transmitter coefficients as requested by the receiver under test. The use of an equivalent procedure is outside the scope of this standard.

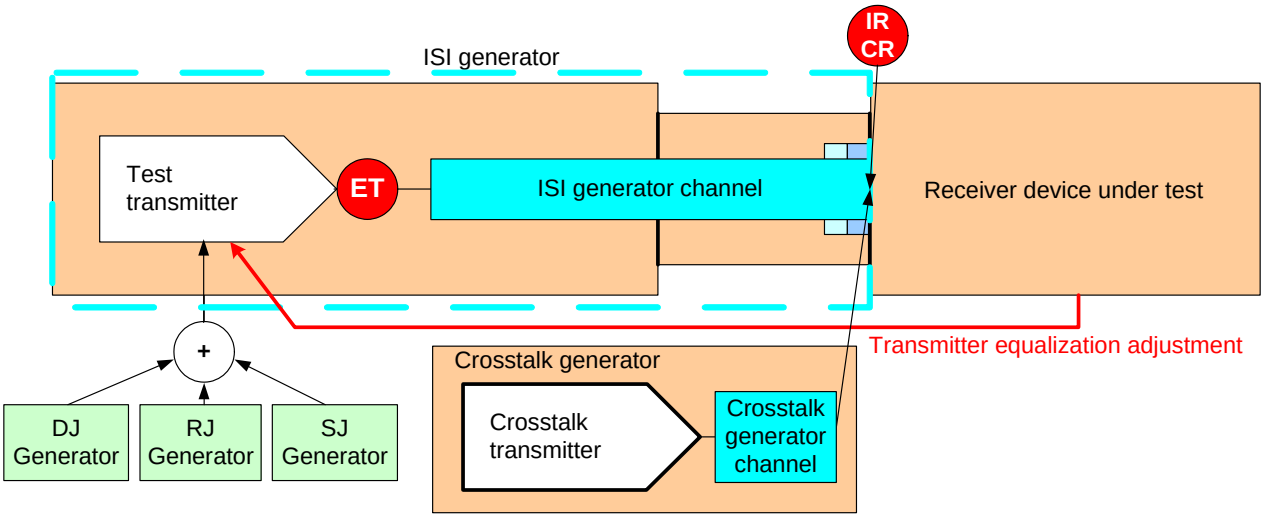


Figure 140 — Stressed receiver transmitter equalization adjustment

5.9.5.7.6.6 ~~Test equipment and~~ ISI generator calibration for trained 12 Gbps

The delivered signal for stressed receiver device jitter tolerance test (see 5.9.5.7.6) shall provide ISI characteristics defined in table 62.

The characteristics at ER shall be measured using end-to-end simulations (see table 5.8.1 and Annex D).

To simplify de-embedding to ET, the peak-to-peak voltage may be measured from the output of the ISI generator's transmitter, when the ISI channel has insertion loss less than 1 dB at 10 MHz. Using this method, the peak-to-peak voltage is computed by scaling down the measured amplitude by the loss of the ISI channel at 10 MHz.

NOTE 21 - Verification required for the 1 dB number. 10 MHz is chosen to represent effective "DC", excluding AC coupling. Two series 8 nF coupling capacitors and 2 x 50 ohms lead to a corner frequency of about 400 kHz, and 10 MHz is 25 times higher.

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter-free reference transmitter with K_0 set to 1 (unit-less value) at the output of the ISI generator, using the ISI generator's output as the input of the reference transmitter, instead of the +1/-1 digitized stream (see figure 141).

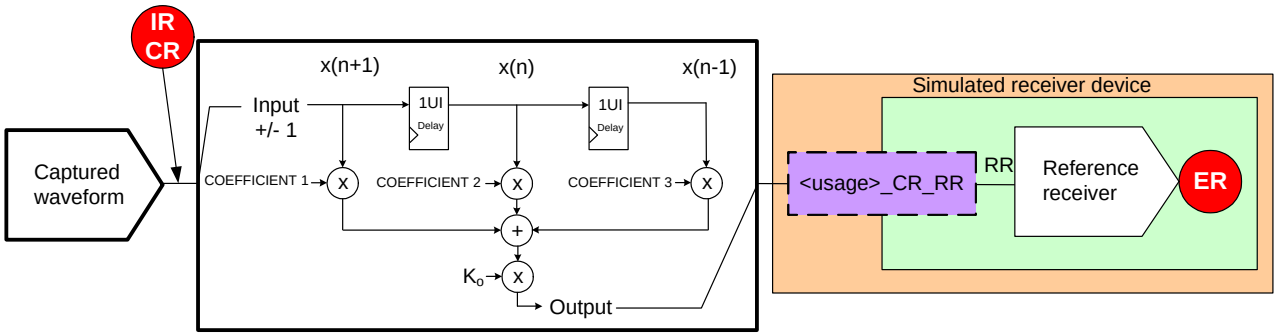


Figure 141 — Simulation of the reference transmitter from a captured signal

The ISI generator's transmitter device shall have the trained 12 Gbps transmitter characteristics (see 5.9.4.7). The ISI generator shall be capable of changing its equalization in response to the attached receiver device's back-channel requests (see SPL-2). This may be performed using a duplex link as defined in SPL-2, or through the use of and equivalent procedure. The use of an equivalent procedure is outside the scope of this standard.

The ISI generator calibration procedure is as follows:

1) set the transmitter of the ISI generator to output no equalization (i.e. C1 set to 0, C2 set to 1, C3 set to 0);
2) attach the test equipment and ISI generator to a zero-length test load;
3) disable the crosstalk source, the ~~random noise~~RJ source, the DJ source, the SSC source and the variable SJ source;
4) configure the pattern generator to transmit a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2);
5) set the transmitter peak-to-peak voltage to the characteristics of table 62;
6) configure the pattern generator to transmit an IDLE pattern (see SPL-2);
7) capture the signal at IR or CR;
8) simulate signal characteristics and reference transmitter characteristics (see D.1), using reference <usage>_CR_RR channel models of the appropriate usage model (see D.2); and
9) adjust the ISI generator channel for end-to-end simulation characteristics defined in table 62.

Table 62 defines the characteristics measured in end-to-end simulation of the delivered signal for trained 12 Gbps stressed receiver device jitter tolerance test.

~~The crosstalk is added to the simulation as a measured peak-to-peak amplitude at a probability of 10^{-6} (see 5.9.5.7.6.7). The amplitude of the crosstalk is defined in table D.2 (see D.2).~~

See the reference transmitter device (see 5.9.4.7.3) for definitions of coefficient 1, coefficient 2 and coefficient 3 used in table 62. C1, C2, and C3 represent coefficient 1, coefficient 2 and coefficient 3, respectively.

Table 62 — ISI generator charateristics for trained 12 Gbps at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Peak-to-peak voltage [a] [b]	mV(P-P)	850	875	ET
Coefficient 1 (i.e., C1) [c] [d] [e]	V/V	-0.15	~~0~~TBD	ET
Coefficient 3(i.e., C3) [c] [d] [f]	V/V	-0.3	~~0~~TBD	ET
VMA [g] [h]	mV(P-P)	80	-	ET
Reference pulse response cursor peak-to-peak amplitude [i] [j]	mV(P-P)	~~72~~65	~~-~~72	ER
Vertical eye opening to reference pulse response cursor ratio [j] [k] [l] [m]	%	~~55~~45	~~-~~55	ER
DFE coefficient magnitude to reference pulse response cursor ratio [n]	%	~~-75~~45	75	ER
~~Crosstalk generator offset frequency~~ [o]	~~ppm~~	~~2 500~~	~~-~~	~~ET~~

[a] The measurement shall be made with the ISI generator transmitter set to no equalization and a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). This measurement includes losses of the ISI generator's channel.

[b] The peak-to-peak voltage is adjusted as close as possible to the minimum limit.

[c] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[d] C2 = 1 - |C1| - |C3|.

[e] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] VMA = $2K_0$ ((C1 + C2 + C3). See 5.9.4.7.3.

[h] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (\text{~~C2~~}C3' - \text{~~C2~~}C3)^2)^{0.5}$$

where:
C1' and C3' are values that satisfy the minimum VMA criterion.

[i] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 113.

[j] The end-to-end simulation removes any remaining RJ and TJ (non-ISI) of the ISI generator's transmitter.

[k] The vertical eye opening includes the effects of crosstalk at a probability of 10^{-6} (see 5.9.5.7.6.7) which shall be subtracted from the verticle eye opening computed from the ISI simulation (see D.1).

[l] The ISI generator is adjusted as close as possible to the maximum reference pulse response cursor and verticle eye opening to reference pulse response cursor ratio limits.

[m] See figure 111.

[n] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(di)) divided by the reference pulse response cursor (see 5.9.5.7.3).

[o] ~~The crosstalk generator may use SSC modulation rather than have a fixed offset frequency~~

Editor's Note 9: The values in table 62 are based on initial simulations that did not include the complete end-to-end TxRx connection. Final values may be different, but remain consistent

between table 27, table 48, and table 62.

5.9.5.7.6.7 Crosstalk calibration for trained 12 Gbps stressed receiver device jitter tolerance test

Total peak-to-peak crosstalk noise shall be measured as defined in 5.8.4 at IR or CR. The crosstalk is added to the simulation as a measured peak-to-peak amplitude at a probability of 10^{-6}. The characteristics of the crosstalk amplitude are defined in table D.2 (see D.2).

The crosstalk shall be generated by a single transmitter with:

a) a minimum fixed offset frequency of 1 000 ppm; or
b) using SSC modulation rather than the fixed offset frequency.

5.9.5.7.6.8 Applied RJ for trained 12 Gbps stressed receiver device jitter tolerance test

The delivered signal for stressed receiver device jitter tolerance test (see 5.9.5.7.6) shall provide RJ characteristics defined in table 63.

Table 63 — RJ charateristics for trained 12 Gbps stressed receiver device tolerance test

Characteristic	Units	Minimum	Nominal	Maximum
Tx RJ [a] [b] [c]	UI	0.135 [d]	0.150 [e]	0.165 [f]

[a] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.
[b] Measured at ER, IR, or CR in figure 140. The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] Measured after application of the JTF (see 5.9.3.2).
[d] 0.135 UI is 11.25 ps at 12 Gbps.
[e] 0.150 UI is 12.5 ps at 12 Gbps.
[f] 0.165 UI is 13.75 ps at 12 Gbps.

5.9.5.7.6.9 Applied SJ

Figure 142 defines the applied SJ for trained receiver devices that do not support SSC.

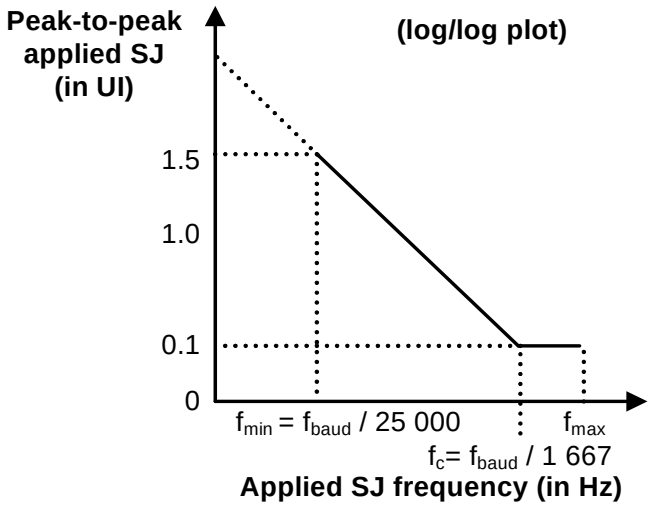


Figure 142 — Applied SJ for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps without SSC support

Table 64 defines f_{min}, f_c, and f_{max} for figure 142. f_{baud} is defined in table 31 (see 5.9.1).

Table 64 — f_{min}, f_c, and f_{max} for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps without SSC support

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbps	60 kHz	900 kHz	5 MHz
3 Gbps	120 kHz	1 800 kHz	7.5 MHz
6 Gbps	240 kHz	3 600 kHz	15 MHz
12 Gbps	240 kHz	3 600 kHz	15 MHz

Figure 143 defines the applied SJ for trained receiver devices that support SSC.

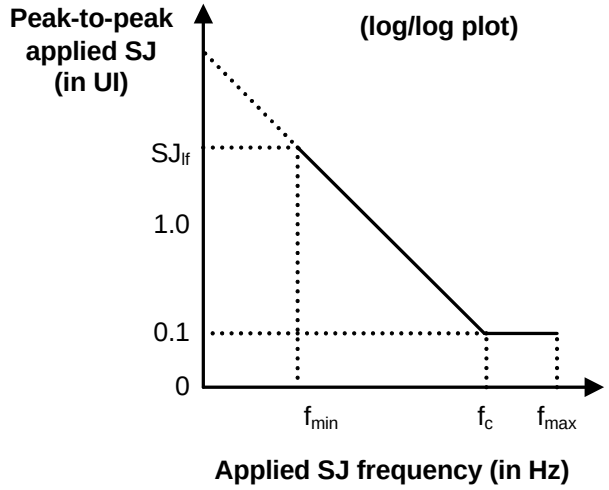


Figure 143 — Applied SJ for trained 1.5 Gbps, 3 Gbps, 6 Gbps and 12 Gbps with SSC support

Table 65 defines f_{min}, f_c, f_{max}, and SJ_{lf} for figure 143.

Table 65 — f_{min}, f_c, f_{max}, and SJ_{lf} for trained 1.5 Gbps, 3 Gbps, 6 Gbps, and 12 Gbps with SSC support

Physical link rate	f_{min}	f_c	f_{max}	SJ_{lf}
1.5 Gbps	97 kHz	1.03 MHz	5 MHz	11.3 UI
3 Gbps	97 kHz	1.46 MHz	7.5 MHz	22.6 UI
6 Gbps	97 kHz	2.06 MHz	15 MHz	45.3 UI
12 Gbps	111 kHz	2.06 MHz	15 MHz	34.6 UI

5.9.5.8 Delivered signal characteristics for OOB signals

Table 66 defines the amplitude requirements of the OOB signal delivered by the system with the zero-length test load (see 5.7.2) at the receiver device compliance point (i.e., IR or CR). These also serve as the required signal tolerance characteristics of the receiver device.

Table 66 — Delivered signal characteristics for OOB signals

Characteristic	Units	IR	CR
Minimum OOB burst amplitude [a], if SATA is not supported	mV(P-P)	240 [b]	
Minimum OOB burst amplitude [a], if SATA is supported	mV(P-P)	225 [c] [d]	N/A

[a] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst.
[b] The OOB burst contains either 1.5 Gbps repeating 0011b or 1100b pattern (e.g., D24.3), 1.5 Gbps ALIGN (0) primitives, or 3 Gbps ALIGN (0) primitives (see SPL-2).
[c] The OOB burst contains either 1.5 Gbps repeating 0011b or 1100b pattern (e.g., D24.3) or 1.5 Gbps ALIGN (0) primitives (see SPL-2 and SATA).
[d] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.9.6 Spread spectrum clocking (SSC)

5.9.6.1 SSC overview

Spread spectrum clocking (SSC) is the technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions.

Phys transmit with SSC as defined in 5.9.6.2 and receive with SSC as defined in 5.9.6.3.

Table 67 defines the SSC modulation types.

Table 67 — SSC modulation types

SSC modulation type	Maximum SSC frequency deviation (SSC_{tol}) [a]			
	1.5 Gbps	3 Gbps	6 Gbps	12 Gbps
Center-spreading	+2 300 / -2 300 ppm			+1 000 / -1 000 ppm
No-spreading	+0 / -0 ppm			+0 / -0 ppm
Down-spreading	+0 / -2 300 ppm			+0 / -1 000 ppm
SATA down-spreading [b]	+0 / -5 000 ppm			N/A

[a] This is in addition to the physical link rate long-term accuracy and tolerance defined in table 33 (see 5.9.4.3) and table 51 (see 5.9.5.3).
[b] This is only used as a receiver parameter.

A phy may be transmitting with a different SSC modulation type than it is receiving (e.g., a phy is transmitting with center-spreading while it is receiving with down-spreading).

If the SSC modulation type is not no-spreading, then the phy shall transmit within the specified maximum SSC frequency deviation with an SSC modulation frequency that is a minimum of 30 kHz and a maximum of 33 kHz.

The SSC modulation profile (e.g., triangular) is vendor specific, but should provide the maximum amount of electromagnetic interference (EMI) reduction. For center-spreading, the average amount of up-spreading (i.e., > 0 ppm) in the SSC modulation profile shall be the same as the average amount of down-spreading (i.e., < 0 ppm). The amount of asymmetry in the SSC modulation profile shall be less than 288 ppm.

NOTE 22 - 288 ppm is the rate of deletable primitives (see SPL-2) that are left over after accounting for the physical link rate long-term accuracy. It is calculated as the deletable primitive rate defined in the SAS standard of 1/2 048 (i.e., 488 ppm) minus the width between the extremes of the physical link rate long-term accuracy of +100/-100 ppm (i.e., 200 ppm).

SSC-induced jitter is included in TJ at the transmitter output.

The slope of the frequency deviation should not exceed 850 ppm/µs when computed over any 0.27 ± 0.01 µs interval of the SSC modulation profile, after filtering of the transmitter device jitter output by a single-pole low-pass filter with a cutoff frequency of 3.7 ± 0.2 MHz. Alternatively, the transmitter device jitter may be filtered by the closed-loop transfer function of a measurement equipment's PLL that is compliant with the JTF.

The slope is computed from the difference equation:

slope = (f(t) - f(t - 0.27 µs)) / 0.27 µs

where:

f(t) is the SSC frequency deviation expressed in ppm.

A ± 2 300 ppm triangular SSC modulation profile has a slope of approximately 310 ppm/µs and meets the informative slope specification. Other SSC modulation profiles (e.g., exponential) may not meet the slope requirement. A modulation profile that has a slope of ± 850 ppm/µs over 0.27 µs creates a residual jitter of approximately 16.7 ps (i.e., 0.10 UI at 6 Gbps) after filtering by the JTF. This consumes the total BUJ budget of the transmitter device, which does not allow the transmitter device to contribute any other type of BUJ.

Activation or deactivation of SSC on a physical link that is not OOB idle or negotiation idle (see SPL-2) shall be done without violating TJ at the transmitter device output after application of the JTF.

5.9.6.2 Transmitter SSC modulation

A SAS phy transmits with the SSC modulation types defined in table 68.

Table 68 — SAS phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Required	**Optional**
While attached to a phy that does not support SSC	No-spreading	
While attached to a phy that supports SSC	No-spreading	Down-spreading

[a] SAS phys compliant with versions of SAS standards previous to SAS-2 only transmitted with an SSC modulation type of no-spreading.

An expander phy transmits with the SSC modulation types defined in table 69.

Table 69 — Expander phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Required	Optional
While attached to a SAS phy or expander phy that does not support SSC	No-spreading	
While attached to a SAS phy or expander phy that supports SSC	No-spreading	Center-spreading
While attached to a SATA phy	No-spreading	Down-spreading

[a] Expander phys compliant with versions of SAS standards previous to SAS-2 only transmitted with an SSC modulation type of no-spreading.

A SAS device (see SPL-2) or expander device (see SPL-2) should provide independent control of SSC on each transmitter device. However, it may implement a common SSC transmit clock in which multiple transmitter devices do not have independent controls to enable and disable SSC. In such implementations, SSC may be disabled on a transmitter device that is already transmitting with SSC enabled if another transmitter device sharing the same common SSC transmit clock is required to perform SNW-1, SNW-2, SNW-3, or Final-SNW (see SPL-2) or SAS speed negotiation (see SPL-2).

If any transmitter device sharing a common SSC transmit clock enters a non-SSC transmission state (e.g., SNW-1, SNW-2, Final-SNW, or Train-SNW with SSC disabled (see SPL-2)), then any transmitter device sharing that common SSC transmit clock may disable SSC. These transmitter devices are compliant with the SSC requirements even if the transmitter device has negotiated SSC enabled but its transmit clock has SSC disabled, provided that the transmitted signal does not exceed the maximum SSC frequency deviation limits specified in table 67.

The disabling and enabling of SSC may occur at any time (see 5.9.6.1) except during SNW-1, SNW-2, and Final-SNW (see SPL-2).

5.9.6.3 Receiver SSC modulation tolerance

SAS phys and expander phys support (i.e., tolerate) receiving with SSC modulation types defined in table 70.

Table 70 — Receiver SSC modulation types tolerance

Type of phys	SSC modulation type(s) [a] [b]	
	Required	Optional [c]
Phys that support being attached to SATA phys	No-spreading and SATA down-spreading	Center-spreading and down-spreading
Phys that do not support being attached to SATA phys	No-spreading	Center-spreading and down-spreading

[a] This is in addition to the physical link rate long-term accuracy tolerance defined in table 51 (see 5.9.5.3).
[b] Phys compliant with versions of SAS standards previous to SAS-2 that do not support being attached to SATA devices were only required to tolerate an SSC modulation type of no-spreading. Phys compliant with versions of SAS standards previous to SAS-2 that support being attached to SATA devices were only required to tolerate SSC modulation types of no-spreading and SATA down-spreading.
[c] If either the SSC modulation type of center-spreading or down-spreading is supported, then both shall be supported.

5.9.6.4 Expander device center-spreading tolerance buffer

Expander devices supporting the SSC modulation type of center-spreading shall support a center-spreading tolerance buffer for each connection with the buffer size defined in table 71. The expander device uses this buffer to hold any dwords that it receives during the up-spreading portion(s) of the SSC modulation period that it is unable to forward because the ECR (see SPL-2) and/or the transmitting expander phy is slower than the receiving expander phy and because the dword stream does not include enough deletable primitives (see SPL-2). The expander device unloads the center-spreading tolerance buffer during the down-spreading portion(s) of the SSC modulation period when the receiving expander phy is slower than the ECR and the transmitting expander phy.

Table 71 — Expander device center-spreading tolerance buffer

Physical link rate	Minimum buffer size
12 Gbps	14 dwords
6 Gbps	14 dwords
3 Gbps	8 dwords
1.5 Gbps	4 dwords

NOTE 23 - The minimum buffer size is based on the number of dwords that may be transmitted during half of the longest allowed SSC modulation period (i.e., half of the period indicated by 30 kHz) at the maximum physical link rate (i.e., +2 400 ppm for 1.5 Gbps, 3 Gbps, and 6 Gbps or +1 100 ppm for 12 Gbps) minus the number that may be transmitted at the minimum physical link rate (i.e., -2 400 ppm for 1.5 Gbps, 3 Gbps, and 6 Gbps or -1 100 ppm for 12 Gbps). This accounts for forwarding dwords in a connection (see SPL-2) that originated from a phy compliant with versions of SAS standards previous to SAS-2 (i.e., a phy with an SSC modulation type of no-spreading and inserting deletable primitives at a rate supporting only the long-term frequency stability).

Figure 144 shows an example of center-spreading tolerance buffer usage.

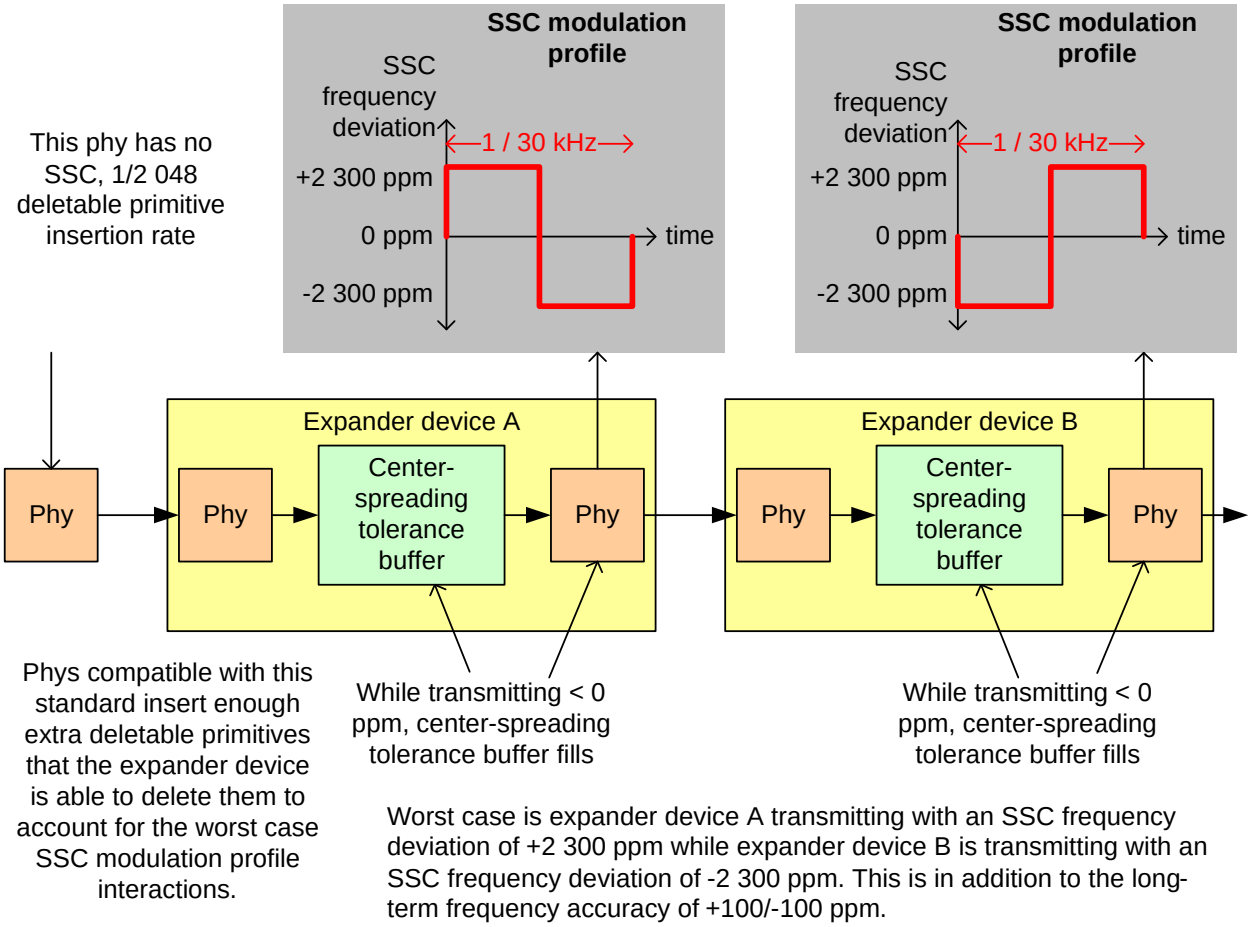


Figure 144 — Center-spreading tolerance buffer

5.9.7 Non-tracking clock architecture

Transceivers shall be designed with a non-tracking clock architecture (i.e., the receive clock derived from the bit stream received by the receiver device shall not be used as the transmit clock by the transmitter device).

Receiver devices that support SATA shall tolerate clock tracking by the SATA device. Receiver devices that do not support SATA are not required to tolerate clock tracking by the SATA device.

5.10 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices (see SPL-2) using the SAS Drive plug connector (see 5.5.3.3.1.1) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 72 describes the output characteristics of the READY LED signal.

Table 72 — Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0 V \leq V_{OH} \leq 3.6 V$	$-100 \mu A < I_{OH} < 100 \mu A$
Asserted (LED on)	$I_{OL} = 15 mA$	$0 \leq V_{OL} \leq 0.225 V$

The READY LED signal behavior is defined in SPL-2.

NOTE 24 - SATA devices use the pin used by the READY LED signal (i.e., P11) for activity indication and staggered spin-up disable (see SATA). The output characteristics differ from those in table 72.

5.11 Out of band (OOB) signals

5.11.1 OOB signals overview

When D.C. mode is enabled, OOB signals are low-speed signal patterns that do not appear in normal data streams. When optical mode is enabled, OOB signals consist of a defined series of dwords. OOB signals consist of defined amounts of idle time followed by defined amounts of burst time. During the idle time, the physical link carries OOB idle. During the burst time, the physical link carries dwords. The signals are differentiated by the length of idle time between the burst times. OOB signals are not decoded unless dword synchronization has been lost (see SPL-2). Once high-speed data transfers are underway, the data pattern amplitude might fall to levels that are falsely detected as OOB signals. A phy shall either have D.C. mode enabled or optical mode enabled. The method to enable D.C. mode or optical mode is outside the scope of this standard.

SATA defines two OOB signals: COMINIT/COMRESET and COMWAKE. COMINIT and COMRESET are used in this standard interchangeably. Phys compliant with this standard identify themselves with an additional SAS-specific OOB signal called COMSAS.

Table 73 defines the timing specifications for OOB signals.

Table 73 — OOB signal timing specifications

Parameter	Minimum	Nominal	Maximum	Comments
OOB Interval (OOBI) [a]	665.0$\overline{6}$ ps [b]	666.$\overline{6}$ ps [c]	668.2$\overline{6}$ ps [d]	The time basis for burst times and idle times used to create OOB signals.
COMSAS detect timeout	13.686 µs [e]			The minimum time a receiver device shall allow to detect COMSAS after transmitting COMSAS.

[a] OOBI is different than UI(OOB) defined in SATA (e.g., SAS has tighter physical link rate long-term accuracy and different SSC frequency deviation). OOBI is based on:
A) 1.5 Gbps UI (see table 31 in 5.9.1);
B) physical link rate long-term accuracy (see table 33 in 5.9.4.3); and
C) center-spreading SSC (see table 67 in 5.9.6.1).

[b] 665.0$\overline{6}$ ps equals 666.$\overline{6}$ × (1 - 0.0024).

[c] 666.$\overline{6}$ equals 2000 / 3.

[d] 668.2$\overline{6}$ ps equals 666.$\overline{6}$ × 1.0024.

[e] 13.686 µs is 512 × 40 × Maximum OOBI.

To interoperate with interconnects compliant with versions of SAS standards previous to SAS-2, phys should create OOB burst times and idle times based on the UI for 1.5 Gbps without SSC modulation.

NOTE 25 - Versions of SAS standards previous to SAS-2 defined OOBI based on the nominal UI for 1.5 Gbps (see table 31 in 5.9.1) with physical link rate long-term accuracy (see table 33 in 5.9.4.3) but not with SSC modulation (see table 67 in 5.9.6.1). Interconnects compliant with versions of SAS standards previous to SAS-2 may have assumed phys had that characteristic.

5.11.2 Transmitting OOB signals

Table 74 describes the OOB signal transmitter requirements for the burst time, idle time, negation times, and signal times that are used to form each OOB signal.

Table 74 — OOB signal transmitter device requirements

Signal	Burst time	Idle time	Negation time	Signal time [a]
COMWAKE	160 OOBI [b]	160 OOBI [b]	280 OOBI [c]	2 200 OOBI [g]
COMINIT/COMRESET	160 OOBI [b]	480 OOBI [d]	800 OOBI [e]	4 640 OOBI [i]
COMSAS	160 OOBI [b]	1 440 OOBI [f]	2 400 OOBI [h]	12 000 OOBI [j]

[a] A signal time is six burst times plus six idle times plus one negation time.
[b] 160 OOBI is nominally 106.$\overline{6}$ ns (see table 73 in 5.11.1).
[c] 280 OOBI is nominally 186.$\overline{6}$ ns.
[d] 480 OOBI is nominally 320 ns.
[e] 800 OOBI is nominally 533.$\overline{3}$ ns.
[f] 1 440 OOBI is nominally 960 ns.
[g] 2 200 OOBI (e.g., COMWAKE) is nominally 1 466.$\overline{6}$ ns.
[h] 2 400 OOBI is nominally 1 600 ns.
[i] 4 640 OOBI (e.g., COMINIT/COMRESET) is nominally 3 093.$\overline{3}$ ns.
[j] 12 000 OOBI (e.g., COMSAS) is nominally 8 000 ns.

When D.C. mode is enabled, an OOB idle consists of the transmission of D.C. idle.

When optical mode is enabled, an OOB idle consists of repetitions of the following steps:

1) transmission of six OOB_IDLE primitives with either starting disparity at 3 Gbps; and
2) transmission of up to 512 data dwords (e.g., two data dwords for COMWAKE idle time, 18 data dwords for COMINIT/COMRESET idle time, and 66 data dwords for COMSAS idle time) set to 0000_0000h that are 8b10b encoded, scrambled, and transmitted at 3 Gbps.

An OOB burst consists of:

a) when D.C. mode is enabled, transmission of repeating 0011b or 1100b patterns (e.g., D24.3) or ALIGN (0) primitives with either starting disparity. The OOB burst should consist of repeating 0011b or 1100b patterns (e.g., D24.3) at 1.5 Gbps; or
b) when optical mode is enabled, transmission of ALIGN (3) primitives with either starting disparity at 3 Gbps.

To transmit an OOB signal, the transmitter device shall repeat these steps six times:

1) transmit OOB idle for an idle time; and
2) transmit an OOB burst for a burst time.

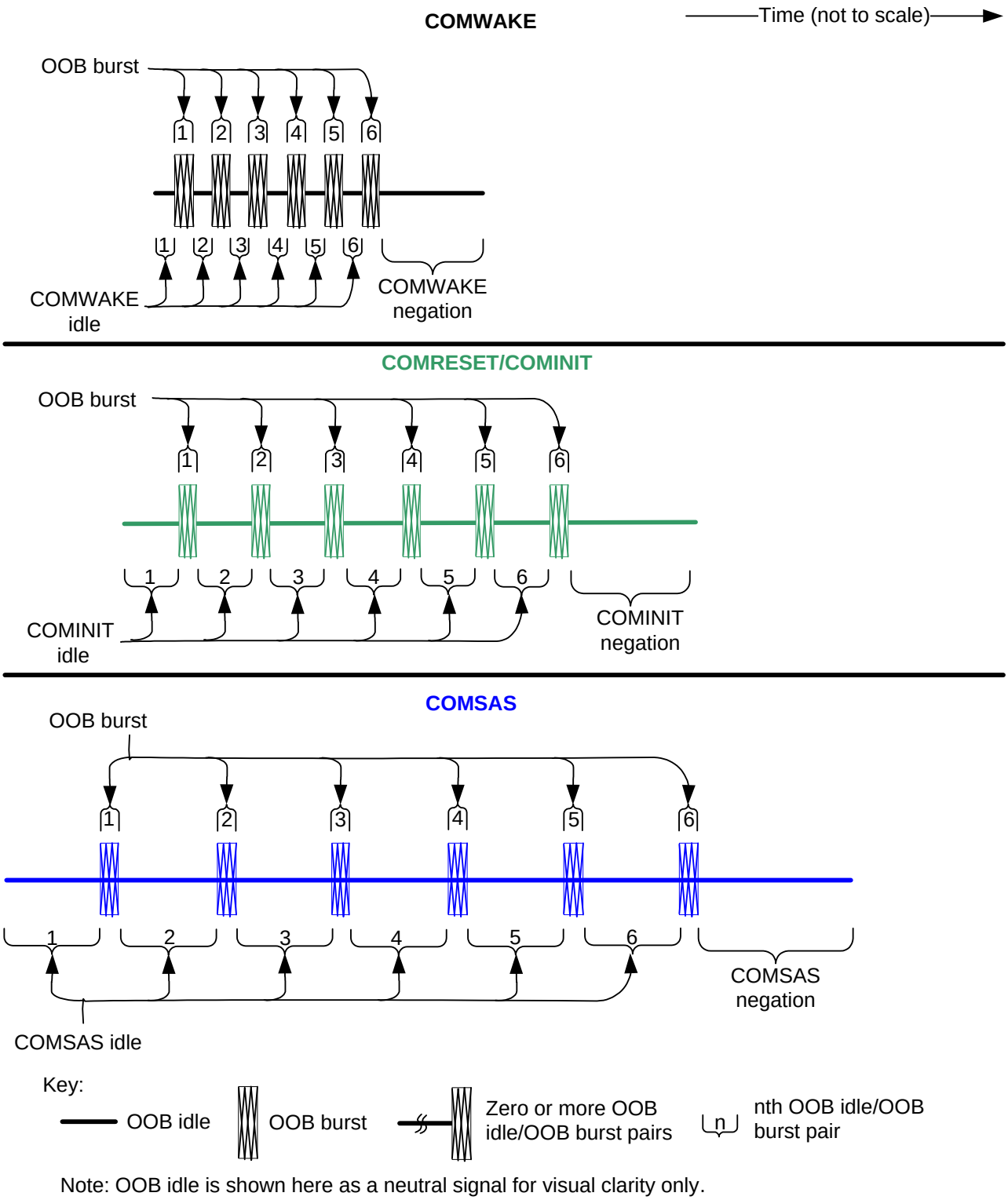
The transmitter device shall then transmit OOB idle for an OOB signal negation time.

The transmitter device shall use signal output levels during burst time and idle time as described in 5.9.4.8.

When D.C. mode is enabled, the repeating 0011b or 1100b patterns (e.g., D24.3) or ALIGN (0) primitives (see SPL-2) used in OOB signals shall be transmitted and the OOB burst is only required to generate an envelope for the detection circuitry, as required for any signaling that may be A.C. coupled. A burst of repeating 0011b or 1100b patterns (e.g., D24.3) at 1.5 Gbps is equivalent to a square wave pattern that has a one for two OOBI and a zero for two OOBI. A transmitter may use this square wave pattern for the OOB burst. The start of the pattern may be one or zero. The signal rise and fall times:

a) shall be greater than (i.e., slower) or equal to the minimum (i.e., fastest) rise and fall times allowed by the fastest supported physical link rate of the transmitter device (see table 35 in 5.9.4.4); and
b) shall be less than (i.e., faster) or equal to the maximum (i.e., slowest) rise and fall times allowed at 1.5 Gbps.

Figure 145 describes OOB signal transmission.



Note: OOB idle is shown here as a neutral signal for visual clarity only.

Figure 145 — OOB signal transmission

5.11.3 Receiving OOB signals

Table 75 describes the OOB signal receiver device requirements for detecting burst times, assuming T_{burst} is the length of the detected burst time. The burst time is not used to distinguish between signals.

Table 75 — OOB signal receiver device burst time detection requirements

Signal [a]	may detect	shall detect
COMWAKE	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 nS < $T_{burst} \leq 112$ ns
COMINIT/COMRESET	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 nS < $T_{burst} \leq 112$ ns
COMSAS	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 nS < $T_{burst} \leq 112$ ns

[a] Each burst time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 74 in 5.11.2).

Table 76 describes the OOB signal receiver device requirements for detecting idle times, assuming T_{idle} is the length of the detected idle time.

Table 76 — OOB signal receiver device idle time detection requirements

Signal	may detect	shall detect	shall not detect
COMWAKE [a]	35 ns $\leq T_{idle} <$ 175 ns	101.3 ns $\leq T_{idle} \leq$ 112 ns	$T_{idle} <$ 35 ns or $T_{idle} \geq$ 175 ns
COMINIT/ COMRESET [b]	175 ns $\leq T_{idle} <$ 525 ns	304 ns $\leq T_{idle} \leq$ 336 ns	$T_{idle} <$ 175 ns or $T_{idle} \geq$ 525 ns
COMSAS [c]	525 ns $\leq T_{idle} <$ 1 575 ns	911.7 ns $\leq T_{idle} \leq$ 1 008 ns	$T_{idle} <$ 525 ns or $T_{idle} \geq$ 1 575 ns

[a] COMWAKE idle time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 74 in 5.11.2).
[b] COMINIT/COMRESET idle time is transmitted as 480 OOBI, which is nominally 320 ns.
[c] COMSAS idle time is transmitted as 1 440 OOBI, which is nominally 960 ns.

Table 77 describes the OOB signal receiver device requirements for detecting negation times, assuming T_{idle} is the length of the detected idle time.

Table 77 — OOB signal receiver device negation time detection requirements

Signal	shall detect
COMWAKE [a]	$T_{idle} >$ 175 ns
COMINIT/COMRESET [b]	$T_{idle} >$ 525 ns
COMSAS [c]	$T_{idle} >$ 1 575 ns

[a] COMWAKE negation time is transmitted as 280 OOBI, which is nominally 186.6 ns (see table 74 in 5.11.2).
[b] COMINIT/COMRESET negation time is transmitted as 800 OOBI, which is nominally 533.$\overline{3}$ ns.
[c] COMSAS negation time, which is transmitted as 2 400 OOBI, which is nominally 1 600 ns.

When D.C. mode is enabled, a SAS receiver device shall detect OOB bursts formed from any of the following:

a) D24.3 characters (see SPL-2) at 1.5 Gbps;
b) ALIGN (0) primitives (see SPL-2) at 1.5 Gbps; or
c) ALIGN (0) primitives at 3 Gbps.

NOTE 26 - Detection of ALIGN (0) primitives at 3 Gbps provides interoperability with transmitter devices compliant with versions of SAS standards previous to SAS-2.

When D.C mode is enabled, a SAS receiver device shall not qualify the OOB burst based on the characters received.

When optical mode is enabled, a SAS receiver device shall detect OOB bursts formed from ALIGN (3) primitives at 3 Gbps.

5.11.4 Transmitting the SATA port selection signal

The SATA port selection signal shown in figure 146 causes the attached SATA port selector (see SPL-2) to select the attached phy (i.e., one of the SATA port selector's host phys) as the active phy (see SATA).

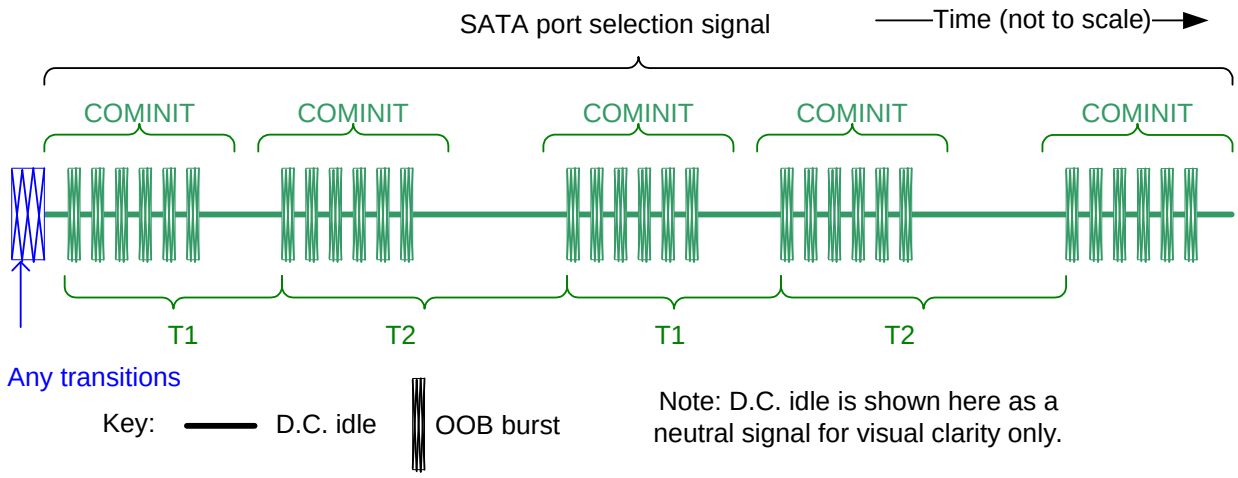


Figure 146 — SATA port selection signal

The SATA port selection signal shall be composed of five COMINIT signals, each starting a specified time interval, T1 or T2, as shown in figure 146, after the start of the OOB burst portion of the previous COMINIT signal. The values of T1 and T2 shall be as shown in table 78.

Table 78 — SATA port selection signal transmitter device requirements

Parameter	Time
T1	3 x 10^6 OOBI [a]
T2	12 x 10^6 OOBI [b]

[a] 3 x 10^6 OOBI is nominally 2 ms (see table 73 in 5.11.1).
[b] 12 x 10^6 OOBI is nominally 8 ms.

See SPL-2 for information on usage of the SATA port selection signal.

Annex A
(normative)

Jitter tolerance pattern (JTPAT)

The jitter tolerance pattern (JTPAT) consists of:

1) a long run of low transition density pattern;
2) a long run of high transition density pattern; and
3) another short run of low transition density pattern.

The transitions between the pattern segments stress the receiver. The JTPAT is designed to contain the phase shift in both polarities, from zero to one and from one to zero. The critical pattern sections with the phase shifts are underlined in table A.1 and table A.2.

Table A.1 shows the JTPAT when there is positive running disparity (RD+) (see SPL-2) at the beginning of the pattern. The 8b and 10b values of each character (see SPL-2) are shown.

Table A.1 — JTPAT for RD+

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD+
		1000011100b	0111100011b	1000011100b	0111100011b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D20.3 (74h)	RD-
		1000011100b	0111100011b	10000<u>11100</u>b	<u>0010111</u>00b	
	The above dword containing phase shift <u>11100001011</u>b is sent one time					
42	RD-	D30.3 (7Eh)	D11.5 (ABh)	D21.5 (B5h)	D21.5 (B5h)	RD+
		01111<u>00011</u>b	<u>110100</u>1010b	1010101010b	1010101010b	
	The above dword containing phase shift <u>00011110100</u>b is sent one time					
43 to 54	RD+	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	RD+
		1010101010b	1010101010b	1010101010b	1010101010b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD+	D21.5 (B5h)	D30.2 (5Eh)	D10.2 (4Ah)	D30.3 (7Eh)	RD+
		1010101<u>010</u>b	<u>10000</u>10101b	0101010<u>101</u>b	<u>01111</u>00011b	
	The above dword containing phase shift <u>01010000</u>b and <u>10101111</u>b is sent one time					

If the same 8b characters specified in table A.1 are used when there is negative running disparity (RD-) at the beginning of the pattern, then the resulting 10b pattern is different than the positive running disparity for the same 8b character and does not provide the critical phase shifts. To achieve the same phase shift effects with RD-, a different 8b pattern is required. Table A.2 shows the JTPAT when there is negative running disparity (RD-) at the beginning of the pattern. The 8b and 10b values of each character are shown.

Table A.2 — JTPAT for RD-

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD-
		0111100011b	1000011100b	0111100011b	1000011100b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D11.3 (6Bh)	RD+
		0111100011b	1000011100b	01111**00011**b	**110100**0011b	
	The above dword containing phase shift **000111101**00b is sent one time					
42	RD+	D30.3 (7Eh)	D20.2 (54h)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		10000**11100**b	**001011**0101b	0101010101b	0101010101b	
	The above dword containing phase shift **11100001011**b is sent one time					
43 to 54	RD-	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		0101010101b	0101010101b	0101010101b	0101010101b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD-	D10.2 (4Ah)	D30.5 (BEh)	D21.5 (B5h)	D30.3 (7Eh)	RD-
		0101010**101**b	**0111**101010b	1010101**010**b	**10000**11100b	
	The above dword containing phase shift **10101111**b and **01010000**b is sent one time					

The compliant jitter tolerance pattern (CJTPAT) is the JTPAT for RD+ (see table A.1) and RD- (see table A.2) included as the payload in an SSP DATA frame or an SMP frame. A phy or test equipment transmitting CJTPAT outside connections may transmit it with fixed content. See SPL-2.

Annex B
(normative)

SASWDP

B.1 SASWDP introduction

SASWDP is a MATLAB program used for transmitter device compliance for trained 1.5 Gbps, 3 Gbps, and 6 Gbps (see 5.9.4.6.1) and for receiver device compliance for trained 1.5 Gbps, 3 Gbps, and 6 Gbps (see 5.9.5.7.6). Equivalent simulation programs may be used if they lead to the same results.

B.2 SASWDP.m

```
% MATLAB (R) script to compute TWDP, WDP, and NC-DDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Version: 1.9
% Date: September 11, 2009
%
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% SELLING, OFFERING FOR SALE OR IMPORTING OF THE SOFTWARE OR PRODUCTS MAKING
% USE OF THE SOFTWARE.
%
% Based on original TWDP methodology described in IEEE Std 802.3aq(TM)-2006
%
% Reference: N. L. Swenson, P. Voois, T. Lindsay, and S. Zeng, "Standards
% compliance testing of optical transmitters using a software-based equalizing
% reference receiver", paper NWC3, Optical Fiber Communication Conference and
% Exposition and The National Fiber Optic Engineers Conference on CD-ROM
```

```
% (Optical Society of America, Washington, DC), Feb. 2007
%
% Syntax:
% [xWDP, ncDDJ, MeasuredxMA, yout] = SASWDP( WaveformFile, TxDataFile, ...
%     SymbolRate, OverSampleRate, Usage, ShowEye )
%
% Inputs:
% -------
% WaveformFile: The waveform consists of exactly N samples per unit interval
%  T, where N is the oversampling rate. The waveform must be circularly
%  shifted to align with the transmit data sequence. The file format is ASCII
%  with a single column of chronological numerical samples, in signal level,
%  with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% TxDataFile: The transmit data sequence should be one of standard test
%  patterns The file format is ASCII with a single column of chronological
%  ones and zeros with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% SymbolRate: The reciprocal of the unit interval in GBd. Enter as a double.
% OverSampleRate: Number of samples, N, per unit interval. Enter as a double.
% Usage: Defines the parameter set specific to the requirement to be verified.
%  In this version, the only permissible values are 'SAS2_TWDP' and
%  'SAS2_LDP'. Enter as a string.
% ShowEye: Controls the graphical display of the slicer input eye. Any value
% greater than zero enables the display (and is the figure number for the
% first figure generated). Enter as a double.
%
% Outputs:
% --------
% xWDP: Waveform Dispersion Penalty (dBe)
% ncDDJ: non-compensable DDJ. This is computed from twice the worst-case eye
%        closure and should be improved.
% MeasuredxMA: Approximative magnitude of the waveform (from 40-60% amplitude
%              of a 5-zeros/5-ones pattern)
% yout is the result of the convolution with the channel response
%      (for debugging purposes).
%
% This script requires the file 'sas2_stressor_6g0_16x.txt' in
% the same directory

%% Function: SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [xWDP,ncDDJ,MeasuredxMA,yout]=...
    SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,ShowEye)
%% Program constants
SymbolPeriod=1/SymbolRate;
Q0=7.94; % BER = 10^(-15)
%% Load input waveform and data sequence, generate filter and other matrices
% Accept vectors
if ischar(WaveformFile)
  yout0=load(WaveformFile);
else
  yout0=WaveformFile(:);
end
if ischar(TxDataFile)
  XmitData=load(TxDataFile);
else
  % Convert to double otherwise toeplitz may think it is logical...
  XmitData=double(TxDataFile(:));
end
%yout0=load(WaveformFile);
%XmitData=load(TxDataFile);
```

```
PtrnLength=length(XmitData);
TotLen=PtrnLength*OverSampleRate;
Fgrid=(-TotLen/2:TotLen/2-1).'/(PtrnLength*SymbolPeriod);

% MG as a first thing, convolve with channel. MeasuredxMA is unused in GetParams
[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
    GetParams(Usage,Fgrid,SymbolPeriod,1);

yout0=real(ifft(fft(yout0).*fftshift(H_chan)));

%% Enforce column vectors
yout0 = yout0(:);
XmitData = XmitData(:);
%% Normalize the received OMA or VMA to 1. Estimate the xMA of the captured
%% waveform by using a linear fit to estimate a pulse response, synthesize a
%% square wave, and calculate the xMA of the synthesized square wave per IEEE
%% 802.3, clause 52.9.5.
ant=4; mem=40; % Anticipation and memory parameters for linear fit
X=zeros(ant+mem+1,PtrnLength); % Size data matrix for linear fit
Y=zeros(OverSampleRate,PtrnLength); % Size observation matrix for linear fit
for ind=1:ant+mem+1 % Wrap appropriately for linear fit
    X(ind,:)=XmitData(mod((0:PtrnLength-1)-ind+ant+1,PtrnLength)+1).';
end
X=[X;ones(1,PtrnLength)]; % The all-ones row is included to compute the bias
for ind=1:OverSampleRate
    Y(ind,:)=yout0((0:PtrnLength-1)*OverSampleRate+ind)'; % 1 bit per column
end
Qmat=Y*X'*(X*X')^(-1); % Coefficient matrix resulting from linear fit. Each
%% column (except the last) is one bit period of the pulse response. The last
%% column is the bias.
SqWvPer=10; % Even number; sets the period of the sq wave used to compute xMA
SqWv=[zeros(SqWvPer/2,1);ones(SqWvPer/2,1)]; % One period of sq wave (column)
X=zeros(ant+mem+1,SqWvPer); % Size data matrix for synthesis
for ind=1:ant+mem+1 % Wrap appropriately for synthesis
    X(ind,:)=SqWv(mod((0:SqWvPer-1)-ind+ant+1,SqWvPer)+1).';
end
X=[X;ones(1,SqWvPer)]; % Include the bias
Y=Qmat*X;Y=Y(:); % Synthesize the modulated square wave, put into one column
Y=AlignY(Y,SqWvPer,OverSampleRate);
avgpos=(0.4*SqWvPer/2*OverSampleRate:0.6*SqWvPer/2*OverSampleRate);
ZeroLevel=mean(Y(round(avgpos),:)); % Average over middle 20% of "zero" run
%% Average over middle 20% of "one" run, compute xMA
MeasuredxMA=mean(Y(round(SqWvPer/2*OverSampleRate+avgpos),:))-ZeroLevel;
%% Subtract zero level and normalize xMA
youtn=(yout0-ZeroLevel)/MeasuredxMA;
%% Get usage parameters for the application

%[MG] Removing the second call to GetParams
%[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
%    GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA);

ONE=ones(PtrnLength,1);
%% Set search range for equalizer delay, specified in symbol periods. Lower end
%% of range is minimum channel delay less 5 for a guardband. Upper end of range
%% accounts for the FFE. Round up and add 5 to guardband for the channel and
%% antialiasing filter.
EqDelMin=-5;
EqDelMax=ceil(EqNf/2)+5;
%% Compute the minimum slicer MSE and corresponding xWDP and ncDDJ
X=toeplitz(XmitData,[XmitData(1);XmitData(end:-1:end+1-EqNb)]);
Xtil=toeplitz(XmitData(mod((0:PtrnLength-1)-EqDelMin,PtrnLength )+1),...
    XmitData(mod(-EqDelMin:-1:-(EqDelMax+EqNb),PtrnLength)+1));
```

```
Rxx=X'*X; % Used in MSE calculation
for ii=1:size(H_chan,2) % index for stressor
    %% Compute the noise autocorrelation sequence at the output of the front-end
    %% antialiasing filter and rate-2/T sampler.
    N0=SymbolPeriod/2/(Q0*10^(PAlloc(ii)/dBscale))^2;
    Snn=N0/2*fftshift(abs(H_r).^2)*1/SymbolPeriod*OverSampleRate;
    Rnn=real(ifft(Snn));
    Corr=Rnn(1:OverSampleRate/2:end);
    C=toeplitz(Corr(1:EqNf));
    % [MG] Removing convolution at this point
    yout=youtn;
%    yout=real(ifft(fft(youtn).*fftshift(H_chan(:,ii))));
    if AAfilter > 0
        %% Process signal through front-end antialiasing filter
        yout=real(ifft(fft(yout).*fftshift(H_r)));
    end
    %% Compute the sampling function and sample the processed waveform
    [yk,tk,index1]=CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP);
    %% Compute MMSE-DFE %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% The MMSE-DFE filter coefficients computed below minimize mean-squared
    %% error at the slicer input. The derivation follows from the fact that the
    %% slicer input over the period of the data sequence can be expressed as
    %% Z = (R+N)*W - X*[0 B]', where R and N are Toeplitz matrices constructed
    %% from the signal and noise components, respectively, at the sampled
    %% output of the antialiasing filter, W is the feedforward filter, X is a
    %% Toeplitz matrix constructed from the input data sequence, and B is the
    %% feedback filter. The computed W and B minimize the mean square error
    %% between the input to the slicer and the transmitted sequence due to
    %% residual ISI and Gaussian noise. Minimize MSE over FFE delay and
    %% determine BER.
    Rout=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    R=Rout(index1:2:end,:);
    RINV=inv([R'*R+PtrnLength*C,R'*ONE;ONE'*R,PtrnLength]);
    R=[R,ONE]; % Add all-ones column to compute optimal offset
    Rxr=Xtil'*R; Px_r=Rxr*RINV*Rxr';
    %% Minimize MSE over equalizer delay
    MseOpt=Inf;
    for kk=1:EqDelMax-EqDelMin+1
        SubRange=(kk:kk+EqNb);
        SubRange=mod(SubRange-1,PtrnLength)+1;
        P=Rxx-Px_r(SubRange,SubRange);
        P00=P(1,1); P01=P(1,2:end); P11=P(2:end,2:end);
        Mse=P00-P01*inv(P11)*P01';
        if (Mse < MseOpt)
            MseOpt=Mse;
            B=-inv(P11)*P01'; % Feedback filter
            XSel=Xtil(:,SubRange);
            W=RINV*R'*XSel*[1;B]; % Feedforward filter
            Z=R*W-XSel*[0;B]; % Input to slicer
            %% Compute BER using semi-analytic method
            MseGaussian=W(1:end-1)'*C*W(1:end-1);
            Ber=mean(0.5*erfc((abs(Z-0.5)/sqrt(MseGaussian))/sqrt(2)));
        end
    end
    %% Compute equivalent SNR %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% This function computes the inverse of the Gaussian error probability
    %% function. The built-in function erfcinv() is not sensitive enough for
    %% low probability of error cases.
    if Ber>10^(-12),Q=sqrt(2)*erfinv(1-2*Ber);
    elseif Ber>10^(-323),Q=2.1143*(-1.0658-log10(Ber)).^0.5024;
    else Q=min(abs(Z-0.5))/sqrt(MseGaussian);
    end
```

```
    %% Compute penalty and ncDDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    RefSNR=dBscale*log10(Q0)+PAlloc(ii);
    xWDP(ii)=RefSNR-dBscale*log10(Q);
    xWDP(ii)=xWDP(ii)-xMAGain(ii); % Offset xWDP by the eligible xMA gain
    ncDDJ(ii)=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian,...
        ShowEye,Usage,ii,MeasuredxMA,Q,Q0,xWDP(ii),dBscale);
end
%% End of SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
    GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA)
switch upper(Usage)
    case 'SAS2_TWDP'
        EqNf=1;
        EqNb=3;
        %% Import stressor response from file %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        %% stressorFile : Contains the stressor impulse response(s) sampled
        %% at an interval of "stressorStep". The file format is ASCII with a
        %% column of chronological numerical samples for each stressor with
        %% no headers or footers.
        stressorFile='sas2_stressor_6g0_16x.txt';
        stressorStep=1/(16*6.0);
        %% Resample the stressor at an interval of "SymbolPeriod/OverSampleRate"
        OverSampleRate=round(length(Fgrid)*mean(diff(Fgrid))*SymbolPeriod);
        stressor0=load(stressorFile);
        stressor0Time=(0:length(stressor0)-1)*stressorStep;
        stressorTime=(0:length(Fgrid)-1)*SymbolPeriod/OverSampleRate;
        stressor=interp1(stressor0Time,stressor0.',stressorTime,'linear',0);
        stressor=stressor*SymbolPeriod/(OverSampleRate*stressorStep);
        H_chan=fftshift(fft(stressor.'),1);
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
       AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    case 'SAS2_LDP'
        EqNf=1;
        EqNb=3;
        H_chan=1;
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
       AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
```

```
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    otherwise
        error('Usage not recognized.');
end
%% End of GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function Y = AlignY(Y0,SqWvPer,OverSampleRate)
%% Aligns the mid crossing of the xMA square waveform to its ideal position.
Y=Y0-mean(Y0); % AC-couple so crossings are at 0.
%% Look only for the crossing in the middle by ignoring any within ~2 UI from
%% its beginning. Due to possible misalignment of the captured waveform, this
%% is the only crossing that is certain.
%% x=find(sign(Y(2*OverSampleRate:end-1))~=...
%%     sign(Y(2*OverSampleRate+1:end)),1)+2*OverSampleRate-1;
x=min(find(sign(Y(2*OverSampleRate:end-1))~=...
    sign(Y(2*OverSampleRate+1:end))))+2*OverSampleRate-1;
%% Find a more exact crossing point.
xinterp=interp1([Y(x),Y(x+1)],[x,x+1],0);
%% Shift to create the aligned square waveform.
SqWvLen=SqWvPer*OverSampleRate;
Y=Y0(mod((0:SqWvLen-1)-SqWvLen/2+x,SqWvLen)+1); % Coarse shift.
X=(1:length(Y))';Y=interp1(X,Y,(1:length(Y))'+xinterp-x,'spline'); % Fine shift.
%% End of AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [yk,tk,index1] = ...
    CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP)
%% Derive normalized frequency grid from the input arguments
TotLen=OverSampleRate*PtrnLength;
Fgridn=(-TotLen/2:TotLen/2-1).'/PtrnLength;
%% Compute the frequency response for spectral line bandpass filter
w1=2*pi*(1-1/3000); % Define the pass band (normalized to signaling speed)
w2=2*pi*(1+1/3000);
w0=sqrt(w1*w2);
Bw=w2-w1;
% Denominator and numerator coefficients for a prototype low pass filter
ap=[1,2,1];
bp=[0,2,1];
% Apply frequency transformation to realize the desired bandpass filter
s=j*2*pi*Fgridn(find(Fgridn ~= 0));
sprime=(s.^2+w0^2)./(Bw*s);
Hp=zeros(1,TotLen);
Hp(find(Fgridn ~= 0))=polyval(bp,sprime)./polyval(ap,sprime);
%% Compute the sampling function and sample the waveform
km1=mod((0:TotLen-1)-1,TotLen)+1;
kp1=mod((0:TotLen-1)+1,TotLen)+1;
if UseLAMP > 0
    ylim=tanh(10*(yout-mean(yout)));
    yclk=real(ifft(fft(abs(ylim(kp1)-ylim(km1))).*fftshift(Hp(:))));
else
    yclk=real(ifft(fft(abs(yout(kp1)-yout(km1))).*fftshift(Hp(:))));
end
yclk=yclk(kp1)-yclk(km1);
time=(0:TotLen).'/OverSampleRate; % Wrap waveforms to ensure all edges are
yout=[yout;yout(1)];              % are detected
yclk=[yclk;yclk(1)];
yclk=yclk/(max(yclk)-min(yclk))+0.5; % Normalize clock waveform
kr=find(diff(yclk > 0.5) > 0); % Eye center index
kf=find(diff(yclk > 0.5) < 0); % Eye crossing index
```

```
k=sort([kr;kf]);
index1=double(kr(1) > kf(1))+1; % Index of the first eye center
tk=time(k)-(1/OverSampleRate)*(yclk(k)-0.5)./(yclk(k+1)-yclk(k));
yk=interp1(time,yout,tk);
%% End of CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function ncDDJ=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian, ...
    showEye,usage,ii,MeasuredxMA,Q,Q0,xWDP,dBscale)
%% Extract required equalizer parameters from the input arguments.
EqNf=length(W)-1; % Number of T/2-spaced feed-forward taps
EqNb=length(B); % Number of T-spaced feedback taps
xr=XSel(:, 1); % Error-free decisions
%% Define the axes of the bit error ratio map
dphi=1/100; % Phase step (unit interval)
dvee=1/200; % Eye diagram amplitude step (unit amplitude)
phiList=linspace(-0.5,0.5,round(1/dphi)+1);
veeList=linspace(-0.5,0.5,round(1/dvee)+1);
if ~(showEye > 0),veeList = 0;end
%% Compute the bit error ratio at each point in the time-amplitude grid.
PtrnLength=length(xr);
OverSampleRate=round(length(yout)/PtrnLength);
time=(0:OverSampleRate*PtrnLength).'/OverSampleRate;
yout=[yout;yout(1)];
for jj=1:length(phiList)
    phi=phiList(jj);
    yk=interp1(time,yout,mod(tk+phi,time(end)));
    Y=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    Y=Y(index1:2:end,:);
    Y=[Y,ones(PtrnLength,1)];
    zk=Y*W-XSel*[0; B];
    %% Compute the minimum distance from the noiseless, equalized samples
    %% to the decision threshold.
    eyeLid0(jj)=max(zk(find(xr == 0)));
    eyeLid1(jj)=min(zk(find(xr == 1)));
    %% Compute the bit error ratio as a function of offset from the nominal
    %% sampling time and decision threshold.
    dk=ones(length(veeList),1)*zk.'-veeList(:)*ones(1,PtrnLength);
    dk(:,find(xr == 0))=0.5-dk(:,find(xr == 0));
    dk(:,find(xr == 1))=dk(:,find(xr == 1))-0.5;
    berMap(:, jj)=mean(erfc(dk/sqrt(2*MseGaussian))/2,2);
end
eyeList=2*min([0.5-eyeLid0;eyeLid1-0.5]);
%% Compute the non-compensable jitter.
kDDJ=find(abs(diff(eyeList > 0)) > 0);
phiDDJ=phiList(kDDJ)-dphi*eyeList(kDDJ)./(eyeList(kDDJ+1)-eyeList(kDDJ));
if length(phiDDJ) == 0
    phiDDJ=[0,0];
end
if length(phiDDJ) == 1
    phiDDJ=sort([phiDDJ,-sign(phiDDJ)/2]);
end
ncDDJ=1-2*max(min([-phiDDJ(1),phiDDJ(2)]),0);
%% Display the bit error ratio map, if requested.
if showEye > 0
    figure(showEye-1+ii);
    clf;
    imagesc(phiList,veeList+0.5,log10(berMap));
    hold on
    plot(phiList,eyeLid0,'--','Color','white');
    plot(phiList,eyeLid1,'--','Color','white');
    hold off
```

```
    jetColors=jet;
    colormap(jet);
    caxis([round(log10(erfc(Q0/sqrt(2))/2)),0]);
    colorbar;
    set(gca,'YDir','normal');
    set(gca,'Color',jetColors(end,:));
    if dBscale == 10,units={'W','dBo'};
    else units={'V','dBe'};end
    tapStr=sprintf('\nxMA = %.3e %s',MeasuredxMA,units{1});
    tapStr=[tapStr,sprintf('\nW = [%.3f', W(1))];
    for jj=2:EqNf
        tapStr=[tapStr,sprintf(', %.3f',W(jj))];
    end
    tapStr=[tapStr, ']'];
    if EqNb > 0
        tapStr=[tapStr,sprintf('\nB = [%.3f',B(1))];
        for jj=2:EqNb
            tapStr=[tapStr,sprintf(', %.3f',B(jj))];
        end
        tapStr=[tapStr,']'];
    else
        tapStr=[tapStr,sprintf('\nB = []')];
    end
    eyeStr=sprintf('SNR = %.1f %s\n',dBscale*log10(Q),units{2});
    eyeStr=[eyeStr,sprintf('xWDP = %.1f %s\n',xWDP,units{2})];
    eyeStr=[eyeStr,sprintf('NC-DDJ = %.3f UI\n',ncDDJ)];
    titleStr=sprintf('[SASWDP] %s',usage);
    titleStr=[titleStr,sprintf('(%d): Bit error ratio map',ii)];
    text(-0.45,0.90,tapStr,'Color','white');
    text(-0.45,0.10,eyeStr,'Color','white');
    title(titleStr, 'Interpreter','none');
    ylabel('Normalized amplitude');
    xlabel('Time (UI)');
end
%% End of AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.3 SASWDP_testcase.m

The following MATLAB program runs SASWDP with a variety of input files.

```
% SASWDP_testcase.m
clear all,close all
format compact
x1='SCRAMBLED_0RDP10m_symbols.txt';
x2='SCRAMBLED_0RDN10m_symbols.txt';
x3='SCRAMBLED_0RDP_symbols.txt';
x4='SCRAMBLED_0RDN_symbols.txt';
y1='SCRAMBLED_0RDP10m_samples.txt';
y2='SCRAMBLED_0RDN10m_samples.txt';
y3='SCRAMBLED_0RDP_samples.txt';
y4='SCRAMBLED_0RDN_samples.txt';
if 1==0 % to check oversample rate
z=load('WaveformFile_0m-prbs10.txt')
plot(mod([1:length(z)],12),z,'.')
clf,plot(mod([1:length(z)],16),z,'.')
end
for i=1:2
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
```

```
OverSampleRate = 16;
Usage = 'SAS2_LDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,Sh
     owEye)
end
for i=3:4
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
OverSampleRate = 16;
Usage = 'SAS2_TWDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,Sh
     owEye)
end
```

Annex C
(informative)

StatEye

C.1 StatEye introduction

StatEye is a Python program that may be used for simulating TxRx connection compliance for trained 1.5 Gbps, 3 Gbps, and 6 Gbps (see 5.6.5). Equivalent simulation programs may be used if they lead to the same results.

NOTE 27 - See http://www.stateye.org for more information on StatEye.

C.2 analysis.py

The following Python file loads pattern measurement files, and is not used for TxRx connection compliance simulations.

```
from string import rstrip
from re import split, search

version = “071210.a”

def loadcsv(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0

for line in file(‘%s.csv’%filename) :
      if flag == 0:
            if search(‘^[0-9,]’,line) :
                  flag = 1

      if flag == 1:
            _line += 1
            if (_line > endline) and (endline>0) :
                  break
            if _line > startline :
                  line = rstrip(line)
                  a = split(‘,’,line)
                  _time = eval(a[timecol])
                  _signal = eval(a[sigcol])
                  time += [_time]
                  signal += [_signal]

return([time,signal])

def loadtxt(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0
```

```
for line in file('%s.txt'%filename) :
      if flag == 0:
            if search('^[0-9,]',line) :
                  flag = 1

      if flag == 1:
            _line += 1
            if (_line > endline) and (endline>0) :
                  break
            if _line > startline :
                  line = rstrip(line)
                  a = split(' ',line)
                  _time = eval(a[timecol])
                  _signal = eval(a[sigcol])
                  time += [_time]
                  signal += [_signal]

return([time,signal])


def polar2rect(r, w, deg=0):# radian if deg=0; degree if deg=1
    from math import cos, sin, pi
    if deg:
w = pi * w / 180.0
    return [r * cos(w), r * sin(w)]

def rect2polar(x, y, deg=0):# radian if deg=0; degree if deg=1
    from math import hypot, atan2, pi
    if deg:
return hypot(x, y), 180.0 * atan2(y, x) / pi
    else:
return [hypot(x, y), atan2(y, x)]
```

C.3 cdr.py

The following Python file extracts the clock from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from numpy import *
from pylab import *

# version 071210.a

def cdr (edges,k,m,name) :

period0 = min(diff(edges[10:2000]))

period = [period0]

phase = [edges[0]]
phaseError = []
nperiod = []
phaseInOld = edges[0]-period[-1]
```

```
for phaseIn in edges :
      nperiod += [ floor( (phaseIn+0.5*period[-1] - phaseInOld) / period[-1])
]
      phaseInOld = phaseIn
      _phaseError = phaseIn - phase[-1] + period[-1]/2
      phaseError += [ mod( _phaseError , period[-1]) - period[-1]/2 ]
      period += [period[-1] + phaseError[-1] * k]
      phase += [phase[-1] + phaseError[-1] * m + nperiod[-1]*period[-1]]

figure()
subplot(3,1,1)
hold(0)
plot(phase/mean(period))
hold(1)
plot(edges/mean(period))
grid(1)
xlabel('time [UI]')
ylabel('Absolute Phase[UI]')
title(name)

subplot(3,1,2)
plot(diff(edges))
hold(1)
plot(array(period))
grid(1)
xlabel('time [UI]')
ylabel('Period\nDeviation [%mean]')

subplot(3,1,3)
plot(array(phaseError) / mean(period) )
grid(1)
xlabel('time [UI]')
ylabel('Phase Error[UI]')

savefig('cdrExtraction.png')

return([phaseError, period])
```

C.4 extractJitter.py

The following Python file extracts jitter from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from numpy import *
from pylab import *

# version 071210.a

def extractJitter(inputT, outputsignalF, signalF, offset, RJ, timestep,
mylength) :

# the offset parameter will eventually be automatically calculated
```

```
from scipy.special import erfinv
from penrose import
extractApproxEdge,extractAccurateEdge,extractAccurateEdge
from cdr import cdr
import pdb

_inputT = extractApproxEdge(inputT)
_outputsignalF = extractAccurateEdge(outputsignalF)
_signalF = extractAccurateEdge(signalF)

j = array(_inputT)[offset:len(_outputsignalF)+offset] - (
array(_outputsignalF) - array(_signalF)[offset:len(_outputsignalF)+offset] )

# extract the noise inbetween two edges
# this could be improved!!
noise = []
for i in range(len(_outputsignalF)-1) :
      noise += [ signalF[ int( (_signalF[offset+i]+_signalF[offset+i+1])/2.0
) ] - outputsignalF[ int( (_outputsignalF[i]+_outputsignalF[i+1])/2.0 ) ] ]


figure()
hold(0)
plot(noise)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
title('Transmitter Noise')
savefig('noise.png')

outtime  = arange(len(noise)) * timestep
outfile = open('noise.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],noise[index]))
outfile.close()

if 0:
      figure()
      hold(0)
      plot(_inputT,'x')
      hold(1)
      plot(_outputsignalF,'x')
      plot(_signalF,'x')
      plot(j,'o')
      grid(1)

[pe,per]=cdr(j,0.005,0.005,'CDR Jitter Extraction')

_per = mean(per[1000:])
[pdf,t]=histogram(array(pe[1000:])/_per,100)

# pdb.set_trace()

pdf[find(pdf<5)] = 0
pdf = pdf*1.0 / sum(pdf)
mid = min(find(t>0))
left = max(find(pdf[:mid] == 0)) + 1
```

```
rght = min(find(pdf[mid:] == 0)) - 1 + mid

leftcdf = cumsum(pdf[left:mid])
leftcdf[find(leftcdf==1)] = 1-1e-15
rghtcdf = flipud(cumsum(flipud(pdf[mid:rght])))
rghtcdf[find(rghtcdf==1)] = 1-1e-15

leftt = t[left:mid]
rghtt = t[mid:rght]

Qleft = -sqrt(2) * erfinv( 2.0 * (1 - leftcdf) -1 )
Qrght = -sqrt(2) * erfinv( 2.0 * (1 - rghtcdf) -1 )

npoints = 4
# Pleft = polyfit(leftt[0:npoints],Qleft[0:npoints],1)
# Prght = polyfit(rghtt[-npoints:],Qrght[-npoints:],1)

_Qleft = concatenate(( [-7] , Qleft ))
_Qrght = concatenate(( Qrght , [-7] ))

# _RJ = ( 1.0 / abs(Pleft[0]) + 1.0 / abs(Prght[0]) ) / 2.0
DJ = -Qrght[-1] * RJ - Qleft[0] * RJ

_leftt = concatenate(( [ leftt[0] - (Qleft[0]+7)*RJ ] , leftt ))
_rghtt = concatenate(( rghtt , [ rghtt[-1] + (Qrght[-1]+7)*RJ ] ))

print 'Extracted RJ = %0.4f, DJ = %0.4f'%(RJ, DJ)

figure()
hold(0)
plot(_leftt,_Qleft)
hold(1)
plot(_rghtt,_Qrght)
grid(1)
xlabel('Time [UI]')
ylabel('Q')
title('Extracted Transmit Jitter, RJ = %0.4f, DJ = %0.4f'%(RJ, DJ) )
savefig('ExtractedJitter.png')

return([RJ,DJ])
```

C.5 penrose.py

The following Python file extracts the step response from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from analysis import *
from numpy import *
import numpy
from pylab import *
import time
from string import rsplit, rstrip
from scipy import linalg, interp
from re import *
```

```
import pdb

# version 080110.a

def extractApproxEdge(x) :
y = find( abs(diff( (array(x)>0)*1.0 )) == 1.0 )
return(y)


def extractAccurateEdge(x) :
from scipy import interp
y = []
for i in range(len(x)-1) :
      if ( ((x[i] < 0.0) and (x[i+1] > 0.0)) or ((x[i] > 0.0) and (x[i+1] <
0.0)) ) :
            _y = interp([0],[x[i],x[i+1]],[i,i+1])[0]
            y += [_y]
return(y)

def filter(x,k) :
y = [x[0]]
for _x in x:
      y += [ (_x-y[-1])*k + y[-1] ]
return(y)

def buildM(x,l) :
M = []
for i in range(len(x)-l) :
      M += [ x[i:i+l] ]
return(M)


def penrose(filename, mylength,start,finish,timecol,sigcol) :
#mylength = 800
#start      = 37000
#finish     = 41000
signalFilter= 0.90
stimFilter= 0.90
outputFilter= 0.90


[time,signal]=loadcsv(filename,start,finish,timecol,sigcol)
start = (array(signal)<0).nonzero()[0][0]
end = (array(signal)>0).nonzero()[0][-1]

print 'Signal analysis from %d to %d'%(start,end)

signalF = filter(signal,signalFilter)
signalF = signalF[start:end+1]
inputT      = (array(signalF)>0)*2.0-1.0
inputF      = filter(inputT,stimFilter)
M_inputF = buildM(inputF,mylength)
IM_inputF = linalg.pinv(transpose(M_inputF))
taps        =
matrixmultiply(transpose(IM_inputF),(signalF[mylength/2:mylength/2 +
len(IM_inputF)]))
outputsignal= matrixmultiply(M_inputF,taps)
```

```
outputsignalF = filter(outputsignal,outputFilter)

testT             = ones(mylength*10)*-1.0
testT[mylength*5:]= 1.0
testF             = filter(testT,stimFilter)
M_testF           = buildM(testF,mylength)
outputtest  = matrixmultiply(M_testF,taps)
outputtestF = filter(outputtest,outputFilter)

#figure()
#hold(0)
#plot(taps)
#grid(1)
#xlabel('time [sample #]')
#ylabel('amplitude [V]')
#savefig('taps.png')

figure()
llength = 10000
hold(0)
plot(signalF[mylength/2-1:llength])
hold(1)
plot(inputF[mylength/2-1:llength])
plot(outputsignalF[:llength])
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
legend(['Measured Signal', 'Fundamental Transmitter', 'Reconstructed'])
title('Signal Reconstruction')
axis([axis()[1]/2,axis()[1]/2+1000,axis()[2],axis()[3]])
savefig('inAndOutSignal.png')

figure()
hold(0)
plot(outputtestF)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
#axis([4900,5100,axis()[2],axis()[3]])
title('Extracted Step Response')
savefig('step.png')

outtime  = arange(len(outputtestF)) * (time[1]-time[0])
outfile = open('extractedStep.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],outputtestF[index]))
outfile.close()

return([inputT, outputsignalF, signalF, time[1]-time[0]])
```

C.6 portalocker.py

The following Python file locks files for exclusive access.

NOTE 28 - See the ActiveState Code web site at http://aspn.activestate.com/ASPN/Cookbook/Python/Recipe/65203 for information about the portalocker code recipe.

```
# portalocker.py - Cross-platform (posix/nt) API for flock-style file
locking.
#                  Requires python 1.5.2 or better.
# The MIT License
#
# Copyright (c) 2008 Jonathan Feinberg
#
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copy
# of this software and associated documentation files (the “Software”), to
deal
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# LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING
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# OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN
# THE SOFTWARE.

“””Cross-platform (posix/nt) API for flock-style file locking.

Synopsis:

   import portalocker
   file = open(“somefile”, “r+”)
   portalocker.lock(file, portalocker.LOCK_EX)
   file.seek(12)
   file.write(“foo”)
   file.close()

If you know what you’re doing, you may choose to

   portalocker.unlock(file)

before closing the file, but why?

Methods:

   lock( file, flags )
   unlock( file )

Constants:
```

```
   LOCK_EX
   LOCK_SH
   LOCK_NB

Exceptions:

    LockException

Notes:

For the 'nt' platform, this module requires the Python Extensions for
Windows.
Be aware that this may not work as expected on Windows 95/98/ME.

History:

I learned the win32 technique for locking files from sample code
provided by John Nielsen <nielsenjf@my-deja.com> in the documentation
that accompanies the win32 modules.

Author: Jonathan Feinberg <jdf@pobox.com>,
        Lowell Alleman <lalleman@mfps.com>
Version: $Id: portalocker.py 5474 2008-05-16 20:53:50Z lowell $

"""


__all__ = [
    "lock",
    "unlock",
    "LOCK_EX",
    "LOCK_SH",
    "LOCK_NB",
    "LockException",
]

import os

class LockException(Exception):
    # Error codes:
    LOCK_FAILED = 1

if os.name == 'nt':
    import win32con
    import win32file
    import pywintypes
    LOCK_EX = win32con.LOCKFILE_EXCLUSIVE_LOCK
    LOCK_SH = 0 # the default
    LOCK_NB = win32con.LOCKFILE_FAIL_IMMEDIATELY
    # is there any reason not to reuse the following structure?
    __overlapped = pywintypes.OVERLAPPED()
elif os.name == 'posix':
    import fcntl
    LOCK_EX = fcntl.LOCK_EX
    LOCK_SH = fcntl.LOCK_SH
    LOCK_NB = fcntl.LOCK_NB
else:
```

```
        raise RuntimeError, “PortaLocker only defined for nt and posix platforms”

    if os.name == ‘nt’:
        def lock(file, flags):
            hfile = win32file._get_osfhandle(file.fileno())
            try:
                win32file.LockFileEx(hfile, flags, 0, -0x10000, __overlapped)
            except pywintypes.error, exc_value:
                # error: (33, ‘LockFileEx’, ‘The process cannot access the file
    because another process has locked a portion of the file.’)
                if exc_value[0] == 33:
                    raise LockException(LockException.LOCK_FAILED, exc_value[2])
                else:
                    # Q:  Are there exceptions/codes we should be dealing with
    here?
                    raise

        def unlock(file):
            hfile = win32file._get_osfhandle(file.fileno())
            try:
                win32file.UnlockFileEx(hfile, 0, -0x10000, __overlapped)
            except pywintypes.error, exc_value:
                if exc_value[0] == 158:
                    # error: (158, ‘UnlockFileEx’, ‘The segment is already
    unlocked.’)
                    # To match the ‘posix’ implementation, silently ignore this
    error
                    pass
                else:
                    # Q:  Are there exceptions/codes we should be dealing with
    here?
                    raise

    elif os.name == ‘posix’:
        def lock(file, flags):
            try:
                fcntl.flock(file.fileno(), flags)
            except IOError, exc_value:
                #  IOError: [Errno 11] Resource temporarily unavailable
                if exc_value[0] == 11:
                    raise LockException(LockException.LOCK_FAILED, exc_value[1])
                else:
                    raise

        def unlock(file):
            fcntl.flock(file.fileno(), fcntl.LOCK_UN)



    if __name__ == ‘__main__’:
        from time import time, strftime, localtime
        import sys
        import portalocker

        log = open(‘log.txt’, “a+”)
        portalocker.lock(log, portalocker.LOCK_EX)
```

```
        timestamp = strftime(“%m/%d/%Y %H:%M:%S\n”, localtime(time()))
        log.write( timestamp )

        print “Wrote lines. Hit enter to release lock.”
        dummy = sys.stdin.readline()

        log.close()
```

C.7 stateye.py

The following Python file computes the statistical eye.

```
from numpy import *
import pdb
import time
from matplotlib import *

################################################################
# stateye class

class stateye :

################################################################
# constructor

def __init__(self) :

      self.version=’080110.a’

      # debug file
      self.debug = open(‘stateye.debug’,’w’)

      # transitionState[currentState] = [<possible next state>]
      self.transitionState= []

      # edge[currentState] = [<edge index corresponding to transitionState>]
      self.edge   = []

      # step[<edge index>] = [<time vs. amplitude>]
      # where @t=0;a=0, @t=inf;a=final
      self.step   = []

      # length of each step must be the same and equal to rxLength
      self.UImax  = 0

      # number of states.
      self.nStates= 0

      # bins construction
      # bins is a Markov pdf; bin[<state>][<amplitude index>]
      self.bins   = []
      # see binIndex and binValue for explanation of bin coefficients
      self.noBins = 4001
      self.midBin = 2001
```

```
      self.kBin   = 2000
      self.binMax = 2.0
      self.binaxis= (arange(self.noBins) - self.midBin) * self.binMax /
self.kBin

      # parameters for cursor to step time conversion
      # are loaded when generating step responses
      # see cursor2index for details
      self.nomUI  = 1         # number of time indexes in step response for
UI
      self.nomOffset= 0       # simple offset for peak centring
      # amplitude of pulse width shrinkage
      self.pws    = 0         # in UI

def __del__(self) :
      self.debug.flush()
      self.debug.close()

#############################################################
# simple routine to index into pdf bins given a value
def binIndex(self, x) :
      return( round(x / self.binMax * self.kBin) + self.midBin )

#############################################################
# simple route to find value for pdf bin given a index
def binValue(self, i):
      return( 1.0 * (i-self.midBin) / self.kBin * self.binMax )

#############################################################
# simple routine to convert cursor index and sweep offset into time index of
step response
def cursor2index(self, cursor, sweep) :
      return( int( round( (cursor+sweep) * self.nomUI + self.nomOffset ) ) )

#############################################################
# simple routine to convert index to cursor
def index2cursor(self, index) :
      return( (index - self.nomOffset) * 1.0 / self.nomUI )

#############################################################
# shift a pdf bin description as convolution
def binShift(self, bin, x) :
      i = self.midBin - self.binIndex(x)
      if i < 0 :
            return( concatenate(( bin[-i:], zeros(-i) )) )
      if i > 0 :
            return( concatenate(( zeros(i), bin[0:-i] )) )
      if i==0 :
            return(bin)

# perform stateye algorithm for single sample phase
# clearly includes pws but not mid band jitter
def calcpdf(self,sweepdelta,startCursor,lastCursor,dj,rj,noise_x,noise_y) :
                from pylab import find
      import pdb
      self.cdf=[]
      self.sweep = arange(-0.75,0.75,sweepdelta)
```

```
      #self.sweep = [0.0]
      self.pdf=zeros(( len(self.sweep), len(self.binaxis) ))

      # generate a pre-indexed step response for acceleration of the pdf
calculation
      # should consider this for other variable as well, e.g. dfecoef
      self.stepK = []
      for _step in self.step :
            _stepK = []
            for __step in _step :
                  _stepK += [self.midBin - self.binIndex(__step)]
            self.stepK += [ _stepK ]

      print 'folding %d steps'%len(self.sweep)
      binstore = [ 1.0*zeros((self.nStates,self.noBins)),
1.0*zeros((self.nStates,self.noBins)) ]
      for i_sweep in range(len(self.sweep)) :
            #self.debug.writelines('at sweep %d from
%d\n'%(i_sweep,len(self.sweep)))
            #delta = time.time() - tag
            print '%d'%(i_sweep+1),
            #tag = time.time()
            # scan from last cursor to first cursor
            # i.e. back cursor tracing
            # for debug
            bintag = 0
            _bins = binstore[bintag]
            bins = binstore[1-bintag]
            bins = self.start_bins
            _bins[:] = 0.0
            # the value of the step for the given cursor and sweep
            _sweep      = self.sweep[i_sweep]
            for cursor in flipud(range(startCursor,lastCursor)) :
                  # self.debug.writelines('at cursor %d\n'%cursor)
                  #print 'at cursor %d'%cursor

                  # where am I on the time axis
                  currentIndex = self.cursor2index(cursor,_sweep)

                  # next Markov pdf contents
                  # perform Markov convolution
                  # scan through each state
                  for state in range(self.nStates) :

                        # enable for tracking speed of exection
                        # print 'at state %d'%state

                        # scan each possible transition from this state
                        for transition in
range(len(self.transitionState[state])) :
                              # sweep the pws assuming a simple dirac
distribution
                              # for debug
                              # for pws in [-self.pws,self.pws] :
                              for pws in [0] :
                                    # calculate the next state for the given
state
```

```
                                    _nextState =
self.transitionState[state][transition]

                                    # the edge needed to get to this state
                                    _edge       =
self.edge[state][transition]

                                    # when pws is enabled then currentIndex
clearly needs to be correctly modulated
                                    _delta      = -self.stepK[ _edge ][
currentIndex + pws]

                                    # perform a convoltion using a simple
shift and addition for the state given
                                    if _delta==0 :
                                          _bins[_nextState]+=  bins[state]
                                    else :
                                          if (_delta<0) :
                                                _t = bins[state][-_delta:]
                                                _bins[_nextState][:len(_t)]
+=  _t
                                          else :
                                                _t = bins[state][:-_delta]
                                                _bins[_nextState][-len(_t):]
+= _t


                  # enable for dumping the pdfs as they are built up
                  #for _state in range(self.nStates) :
                  #     if len(pylab.find(bins[_state]>0) > 0) :
                  #           print '%s =
%s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_state]>
0))))

                  bintag = 1-bintag
                  _bins = binstore[bintag]
                  bins = binstore[1-bintag]
                  _bins[:] = 0.0

                  # dfe condition
                  # this is also taking a second
                  if cursor==2 :
                        for dfeCoef in self.dfeCoef :
                              for state in range(self.nStates) :

                                    # going to make a big assumption here!!!
That the threshold for greater than and less than is the same
                                    # also going to make a bug assumption
that the gt and lt results index are also inverse
                                    if 1:
                                          _threshold =
self.binIndex(self.gt_h0[state])

                                          _shift      = self.binShift( \
                                                      concatenate(( \

zeros(_threshold), bins[state][_threshold:] )), \
```

```
    -self.gt_true[state] * dfeCoef )
                                                _bins[state] = add(_bins[state],
    _shift)

                                                _shift      = self.binShift( \
                                                              concatenate(( \

    bins[state][:_threshold],  zeros(self.noBins - _threshold) )), \

    -self.gt_false[state] * dfeCoef )
                                                _bins[state] = add(_bins[state],
    _shift)
                                          else :
                                                for binIndex in range(self.noBins)
    :
                                                      if self.binValue(binIndex) >
    self.gt_h0[state] :
                                                            _binValue =
    self.binValue(binIndex) + self.gt_true[state] * dfeCoef
                                                      else :
                                                            _binValue =
    self.binValue(binIndex) + self.gt_false[state] * dfeCoef

    _bins[state][self.binIndex(_binValue)] += bins[state][binIndex]

                                    bintag = 1-bintag
                                    _bins = binstore[bintag]
                                    bins = binstore[1-bintag]
                                    _bins[:] = 0.0

                              # enable for dumping the pdfs as they are built up
                              #for _state in range(self.nStates) :
                              #     if len(pylab.find(bins[_state]>0) > 0) :
                              #           print '%s =
    %s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_state]>
    0))))

                  _pdf = zeros(self.noBins)

                  # typical good place to break for debugging
                  # pdb.set_trace()
                  # firstly what if sum = 0; secondly the sum for difference states
    may be different???
                  # this scaling of the pdf is still not quite workig correctly
                  bins = bins / bins.sum()
                  for state in range(self.nStates) :
                        _pdf = add(_pdf, bins[state])
                        # this additional of the fliped array is mainly for 8b10b
    support. As we only run one set of the codes
                        # we need to add in the other half. I believe this is
    correct, but am checking it again
                        _pdf = add(_pdf, flipud(bins[state]))
                  _pdf = _pdf / _pdf.sum()
                  self.pdf[i_sweep] = _pdf
                  self.debug.writelines('final =
    %s\n'%(array2string(self.binValue(find(_pdf>0)))))
```

```
      print '\nfolding noise'
      # convolve the noise into
      if 0:
            self.pdf_n = zeros(( len(self.sweep), len(self.binaxis) ))
            for i_sweep in range(len(self.sweep)) :
                  for _noise in range(len(noise_x)) :
                        if noise_y[_noise] >0 :
                              _shift = self.binShift(self.pdf[i_sweep],
noise_x[_noise] ) * noise_y[_noise]
                              self.pdf_n[i_sweep]  =
add(self.pdf_n[i_sweep], _shift)
                  self.pdf_n[i_sweep] = self.pdf_n[i_sweep] /
(self.pdf_n[i_sweep]).sum()
      else :
            self.pdf_n = self.pdf

      print 'folding jitter'
      # final pdf containing the jittered version
      if 1:
        self.p = []
        sigma = rj;
        mean  = dj/2;
        for _sweep in self.sweep :
            p = 1/(sigma*sqrt(2*pi)) * exp(-((_sweep-mean)**2)/(2*sigma**2))
+ \
                  1/(sigma*sqrt(2*pi)) *
exp(-((_sweep+mean)**2)/(2*sigma**2)) + \
                  1/(sigma*sqrt(2*pi)) * exp(-((_sweep)**2)/(2*sigma**2));
            if p>1.0e-12 :
                  self.p += [p]
            else :
                  self.p += [0.0]

        self.p = self.p / sum(self.p);

        self.pdf_pj=zeros(( len(self.sweep), len(self.binaxis) ))
        _jmid = len(self.sweep)/2
        for _i in range(len(self.sweep)) :
                  #print 'at sweep %d'%_i
                        for _j in range(len(self.sweep)) :
                            _k = _i + _j - _jmid
                            if (_k > 0) and (_k<len(self.sweep)) :
                  self.pdf_pj[_i] += self.p[_j] * self.pdf_n[_k]
                  self.pdf_pj[_i] = self.pdf_pj[_i] / self.pdf_pj[_i].sum()

def loadStep(self, inputStep, _ui, _pws) :
      from pylab import find
      # define pulse response
      self.inputStep = inputStep
      self.converge= max(inputStep)
      self.pulse = add(-inputStep[:-_ui], +inputStep[_ui:])
      self.nomOffset = find(self.pulse==max(self.pulse))[0]

      # load the step response parameters for
      self.nomUI= _ui
      self.pws= _pws
```

```
      # start and last cursor must allow for some margin
      self.startCursor =
(range(self.nomOffset,0,-_ui)[-2]-self.nomOffset)/_ui
      self.lastCursor=
(range(self.nomOffset,len(inputStep),_ui)[-2]-self.nomOffset)/_ui
      self.xindex =
arange(self.cursor2index(self.startCursor,0),self.cursor2index(self.lastCurs
or,0))

      #print 'start cursor %d, finish cursor
%d'%(self.startCursor,self.lastCursor)

def create2TapFIR(self, c, noDFEtaps) :
      from pylab import find
      # input step is the fundamental step response of the system to a 1V
step, and is assumed to be 0@t=0
      # c is a 1x2 array containing the FIR coefficients
      # this function defines the transitionStates, edge transitions and
generates the necessary steps

      self.nStates = 4

      # for each state x
      #                              0      1      2      3
      x                 = [   [0,0],      [0,1],      [1,0],      [1,1] ]
      x = array(x)*2.0 - 1.0
      self.states = [   '00',       '01',       '10',       '11'  ]
      # load the possible state transition
      self.transitionState = [ [0,1], [2,3], [0,1],   [2,3] ]
      # define the edge used to move from state to state
      self.edge   = [   [0,1],      [2,3],      [4,5],      [6,7] ]
      # load empty steps
      self.step   = [     [],[],        [],[],[],[],[],[] ]

      # preload the Markov pdf with the converged values for the two stable
states,
      # leave the other state empty
      self.start_bins               = zeros((self.nStates,self.noBins))
      self.start_bins[0][self.binIndex( sum(x[0]*c)*self.converge )] = 1
      self.start_bins[3][self.binIndex( sum(x[3]*c)*self.converge )] = 1

      # this could be more efficient in storage of the indexes, but for a
simple example it doesn't matter
      # for each state and transitions an edge is defined
      # copy the inputStep into each step array, given the correct factor
needed to move states
      for _state in range(self.nStates) :
            for _transition in range(len(self.edge[_state])) :
                  k =
(sum(x[self.transitionState[_state][_transition]]*flipud(c)) -
sum(x[_state]*flipud(c)))
                  self.debug.writelines('in state %d, transitioning to state
%d, using %0.3f\n'\

%(_state,self.transitionState[_state][_transition],k))
                  self.step[self.edge[_state][_transition]] = self.inputStep
```

```
* k

      # this is the post equalised step response
      self.pulse = add( add ( \
                  self.step[ self.edge[0][1] ][self.nomUI*2:] , \
                  self.step[ self.edge[1][0] ][self.nomUI:-self.nomUI] ) , \
                  self.step[ self.edge[2][0] ][:-self.nomUI*2] )
      self.pulse = self.pulse/2.0
      self.nomOffset = find(self.pulse==max(self.pulse))[0]

      self.dfeCoef = []
      h0 = self.pulse[self.cursor2index(0 , 0)]
      print 'found h0=%0.3f'%h0
      #                  00    01    10    11
      self.gt_h0 = [-h0, +h0, -h0,  +h0]
      self.gt_true = [-1.0, -1.0,-1.0,-1.0]
      self.gt_false = [+1.0, +1.0,+1.0,+1.0]
      self.lt_h0 = [-h0,+h0,  -h0,  +h0]
      self.lt_true = [+1.0,+1.0,+1.0, +1.0]
      self.lt_false = [-1.0,-1.0,-1.0, -1.0]

      # clearly we need to include here the proper algorithm for finding the
optimum sampling point!!
      for cursor in range(noDFEtaps) :
            self.dfeCoef += [ abs( self.pulse[self.cursor2index(cursor+1,
0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])


def create8b10b_2TapFIR(self,c,noDFEtaps) :
      from pylab import find
      import pdb

      word10b_p = def8b10b()
      words = sort(word10b_p)
      states = ['x','x']

      # scan through all possible 8b10b codes, truncating to a given length l
      # collect all possible codes
      for l in range(1,11) :
            for _words in words :
                  short = _words[:l]
                  if not(any(array(states)==short)) :
                        states += [short]

      # initialise the transition state matrix
      transitionState = []
      for i in range(len(states)) :
            transitionState += [[]]

      # fill transition state matrx
      for i in range(len(states)) :
            # as we search for where this code could have come from, we only
start searching when the
            # code would be a minimum of 2 characters long. e.g. if the code
word is 1001, we search for
```

```
            # 100 as the source of this code word
            if len(states[i])>1 :
                  # find the index into the state matrix, for the source of
the current word
                  source = find(states[i][:-1]==array(states))[0]
                  # add this code word index to the transition matrix entry
for the source of this code wor
                  # clearly we will only find one single source per code word
                  transitionState[source] += [i]
            # if we are at the final word, then also add the transitions to
this entry in the transition
            # matrix for getting back to 0 & 1. However, as we are
implementing a 2 tap FIR, we must maintain
            # also the second entry, hence the starting states are 00,01,10 &
11
            if len(states[i])==10 :
                  if states[i][-1]=='0' :
                        transitionState[i] += [0]
                        transitionState[i] += [1]
                  if states[i][-1]=='1' :
                        transitionState[i] += [2]
                        transitionState[i] += [3]

      # as stated above we must over write the first four states to be
correct
      states[0:4] = ['00','01','10','11']
      transitionState[0] = transitionState[2]
      transitionState[1] = transitionState[3]

      # generate all possible transitions
      k = []
      transitionLookUp = []
      step  = []
      for _i in range(2**3) :
            if _i > 0 :
                  transitionLookUp += [binary_repr(_i)]
            else :
                  transitionLookUp += ['']
            while(len(transitionLookUp[-1])<3) :
                  transitionLookUp[-1] = '0' + transitionLookUp[-1]
            _k = 0
            for _j in range(2) :
                  # the polarity here needs to be checked
                  _k -= (eval(transitionLookUp[-1][_j])*2.0-1.0) *
flipud(c)[_j] - (eval(transitionLookUp[-1][_j+1])*2.0-1.0) * flipud(c)[_j]
            k += [_k]
            step += [self.inputStep * _k]
            self.debug.writelines('edge %s/%d is
%0.3f\n'%(transitionLookUp[-1],_i,_k))

      # scan through actual transitions and enter edge index into array
      edgeText = []
      edge = []
      for _state in range(len(states)) :
            _edgeText=[]
            _edge=[]
            for _transition in range(len(transitionState[_state])) :
```

```
                  _nextstate = transitionState[_state][_transition]
                  __edgeText = states[_state][-2:] + states[_nextstate][-1]
                  _edgeText += [__edgeText]
                  __edge = find( __edgeText == array(transitionLookUp) )
                  _edge += [__edge]
                  self.debug.writelines('from %s to %s using
%s/%d\n'%(states[_state],states[_nextstate],__edgeText,__edge))
            edge += [_edge]
            edgeText += [_edgeText]

      self.states = states
      self.transitionState = transitionState
      self.edge   = edge
      self.step   = step

      self.nStates      = len(self.states)
      self.start_bins               = zeros((self.nStates,self.noBins))
      # this is the current initialisation matrix which need extending
      # see the commented conditional statements below
      if 0 :
            self.start_bins[0][self.binIndex( self.converge *
sum(array([-1,-1])*c) )] = 1
            self.start_bins[3][self.binIndex( self.converge *
sum(array([+1,+1])*c) )] = 1
      else :
            for _states in range(len(states)) :
                  if (states[_states][-2:]=='00') :
                        self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,-1])*c) )] = 1
                  #if (states[_states][-2:]=='01') :
                  #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,+1])*c) )] = 1
                  #if (states[_states][-2:]=='10') :
                  #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,-1])*c) )] = 1
                  if (states[_states][-2:]=='11') :
                        self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,+1])*c) )] = 1

      # this is the post equalised step response
      self.pulse = add( add ( \
                  self.step[ 1 ][self.nomUI*2:] , \
                  self.step[ 2 ][self.nomUI:-self.nomUI] ) , \
                  self.step[ 4 ][:-self.nomUI*2] )
      self.pulse = self.pulse/2.0
      self.nomOffset = find(self.pulse==max(self.pulse))[0]
      self.dfeCoef = []
      h0 = self.pulse[self.cursor2index(0 , 0)]

      # clearly we need to include here the proper algorithm for finding the
optimum sampling point!!
      for cursor in range(noDFEtaps) :
            self.dfeCoef += [ abs( self.pulse[self.cursor2index(cursor+1,
0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])
```

```
      # setup the DFE correction matrix
      self.gt_h0 = []
      self.gt_true = []
      self.gt_false= []
      self.lt_h0 = []
      self.lt_true = []
      self.lt_false= []
      #pdb.set_trace()
      for _states in states :
            if (_states[-2:]==’00’) or (_states[-2:]==’10’) :
                  self.gt_h0 += [-h0]
                  self.gt_true+= [-1.0]
                  self.gt_false+= [+1.0]
                  self.lt_h0 += [-h0]
                  self.lt_true+= [+1.0]
                  self.lt_false+= [-1.0]
            if (_states[-2:]==’01’) or (_states[-2:]==’11’) :
                  self.gt_h0 += [+h0]
                  self.gt_true+= [-1.0]
                  self.gt_false+= [+1.0]
                  self.lt_h0 += [+h0]
                  self.lt_true+= [+1.0]
                  self.lt_false+= [-1.0]



# simple example based on step.py in steptheory
# probably doesn’t work anymore since extending the code to support more
features
def bist(self) :
      # states are
      # 0 = 0 0
      # 1 = 0 1
      # 2 = 1 0
      # 3 = 1 1
      self.transitionState = [[0,1],[2,3],[0,1],[2,3]]
      self.edge            = [[0,1],[2,3],[4,5],[6,7]]
      self.step   = [[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 1.04,
1.3600000000000001, 1.5200000000000002, 1.6000000000000001,
1.6000000000000001, 1.6000000000000001], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
-1.1700000000000002, -1.53, -1.7100000000000002, -1.8, -1.8, -1.8], [0.0,
0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -0.12999999999999998,
-0.16999999999999996, -0.18999999999999997, -0.19999999999999996,
-0.19999999999999996, -0.19999999999999996], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.12999999999999998, 0.16999999999999996, 0.18999999999999997,
0.19999999999999996, 0.19999999999999996, 0.19999999999999996], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
1.1700000000000002, 1.53, 1.7100000000000002, 1.8, 1.8, 1.8], [0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -1.04, -1.3600000000000001,
-1.5200000000000002, -1.6000000000000001, -1.6000000000000001,
-1.6000000000000001], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0]]
```

```
        self.stepLength= 15
        self.nStates= 4
        self.start_bins= 1.0*zeros((self.nStates,self.noBins))
        self.start_bins[0][self.binIndex(-0.7)] = 1.0
        self.start_bins[3][self.binIndex(+0.7)] = 1.0
        self.calcpdf()


    ###############################################################
    # simple functions to load all the possible 8b10b words
    ###############################################################
    def def8b10b() :
    word8b=[
    “00000000”, “00000001”, “00000010”, “00000011”,
    “00000100”, “00000101”, “00000110”, “00000111”,
    “00001000”, “00001001”, “00001010”, “00001011”,
    “00001100”, “00001101”, “00001110”, “00001111”,
    “00010000”, “00010001”, “00010010”, “00010011”,
    “00010100”, “00010101”, “00010110”, “00010111”,
    “00011000”, “00011001”, “00011010”, “00011011”,
    “00011100”, “00011101”, “00011110”, “00011111”,
    “00100000”, “00100001”, “00100010”, “00100011”,
    “00100100”, “00100101”, “00100110”, “00100111”,
    “00101000”, “00101001”, “00101010”, “00101011”,
    “00101100”, “00101101”, “00101110”, “00101111”,
    “00110000”, “00110001”, “00110010”, “00110011”,
    “00110100”, “00110101”, “00110110”, “00110111”,
    “00111000”, “00111001”, “00111010”, “00111011”,
    “00111100”, “00111101”, “00111110”, “00111111”,
    “01000000”, “01000001”, “01000010”, “01000011”,
    “01000100”, “01000101”, “01000110”, “01000111”,
    “01001000”, “01001001”, “01001010”, “01001011”,
    “01001100”, “01001101”, “01001110”, “01001111”,
    “01010000”, “01010001”, “01010010”, “01010011”,
    “01010100”, “01010101”, “01010110”, “01010111”,
    “01011000”, “01011001”, “01011010”, “01011011”,
    “01011100”, “01011101”, “01011110”, “01011111”,
    “01100000”, “01100001”, “01100010”, “01100011”,
    “01100100”, “01100101”, “01100110”, “01100111”,
    “01101000”, “01101001”, “01101010”, “01101011”,
    “01101100”, “01101101”, “01101110”, “01101111”,
    “01110000”, “01110001”, “01110010”, “01110011”,
    “01110100”, “01110101”, “01110110”, “01110111”,
    “01111000”, “01111001”, “01111010”, “01111011”,
    “01111100”, “01111101”, “01111110”, “01111111”,
    “10000000”, “10000001”, “10000010”, “10000011”,
    “10000100”, “10000101”, “10000110”, “10000111”,
    “10001000”, “10001001”, “10001010”, “10001011”,
    “10001100”, “10001101”, “10001110”, “10001111”,
    “10010000”, “10010001”, “10010010”, “10010011”,
    “10010100”, “10010101”, “10010110”, “10010111”,
    “10011000”, “10011001”, “10011010”, “10011011”,
    “10011100”, “10011101”, “10011110”, “10011111”,
    “10100000”, “10100001”, “10100010”, “10100011”,
    “10100100”, “10100101”, “10100110”, “10100111”,
    “10101000”, “10101001”, “10101010”, “10101011”,
    “10101100”, “10101101”, “10101110”, “10101111”,
```

```
“10110000”, “10110001”, “10110010”, “10110011”,
“10110100”, “10110101”, “10110110”, “10110111”,
“10111000”, “10111001”, “10111010”, “10111011”,
“10111100”, “10111101”, “10111110”, “10111111”,
“11000000”, “11000001”, “11000010”, “11000011”,
“11000100”, “11000101”, “11000110”, “11000111”,
“11001000”, “11001001”, “11001010”, “11001011”,
“11001100”, “11001101”, “11001110”, “11001111”,
“11010000”, “11010001”, “11010010”, “11010011”,
“11010100”, “11010101”, “11010110”, “11010111”,
“11011000”, “11011001”, “11011010”, “11011011”,
“11011100”, “11011101”, “11011110”, “11011111”,
“11100000”, “11100001”, “11100010”, “11100011”,
“11100100”, “11100101”, “11100110”, “11100111”,
“11101000”, “11101001”, “11101010”, “11101011”,
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return(word10b_p)
```

C.8 touchstone.py

The following Python file inputs a Touchstone file and calculates the step response.

```
class touchstone :
def __init__(self) :
      self.version=’080111.a’
      self.nports = 4# default for Touchstone 1.0 files
      self.frequency = []
      # currently I’m keeping these as lists, but I may change this to a
comple 3-d array
```

```
        self.raw_s = []
        self.s = []
        self.t = []

    def getStep(self, resolution, measStep, measNoise,TxNorm) :
        from numpy import concatenate, cumsum, arange, flipud, conj, real,
    array
        import numpy
        from string import rsplit
        from re import split
        from pylab import find
        import pdb

        # currently no padding
        t = concatenate(( flipud(conj(self.t[1:])), self.t ))
        impulse = real(numpy.fft.ifft(numpy.fft.ifftshift(t)))
        timeStep = 1.0/(2.0*max(self.frequency))
        timeAxis = arange(len(impulse)) * timeStep
        self.impulse =
    numpy.interp(arange(timeAxis[0],timeAxis[-1],resolution),timeAxis,impulse)
        self.impulse = self.impulse * (resolution/timeStep)

        if len(measStep) :
              txtime = []
              txsignal = []
              for line in file(measStep) :
                    line = rsplit(line)
                    col = split(‘,’,line[0])
                    txtime += [eval(col[0])]
                    txsignal += [eval(col[1])]
              # this 0.5 comes about, because it comes from a ‘0’ -> ‘1’
    transition of a measurement
              # and is not based on the pulse step, i.e. ‘Z’ -> ‘1’
              txsignal = 0.5 * array(txsignal)
              txsignal = txsignal - txsignal[0]
              _txsignal =
    numpy.interp(arange(timeAxis[0],timeAxis[-1],resolution),txtime,txsignal)
              f1 = numpy.fft.fft(_txsignal)
              f2 = numpy.fft.fft(self.impulse)
              f3 = f1 * f2
              self.step = real(numpy.fft.ifft(f3))
              i = find(min(self.step)==self.step)[0]
              self.step = self.step - self.step[i]
              self.step[:i] = 0.0
        else :
              self.step = cumsum(real(self.impulse)) * 0.5 * TxNorm

        if len(measNoise) :
              txtime = []
              txsignal = []
              for line in file(measNoise) :
                    line = rsplit(line)
                    col = split(‘,’,line[0])
                    txtime += [eval(col[0])]
                    txsignal += [eval(col[1])]
              txsignal = array(txsignal)
              txsignal = txsignal - txsignal[0]
```

```
            _txsignal =
numpy.interp(arange(timeAxis[0],timeAxis[-1],resolution),txtime,txsignal)
            f1 = numpy.fft.fft(_txsignal)
            f2 = numpy.fft.fft(self.impulse)
            f3 = f1 * f2
            self.noise = real(numpy.fft.ifft(f3))


    def map(self,p) :
          from numpy import array,zeros
          p = (array(p)-1).tolist()
          m = [1-1,2-1,5-1,6-1]
          for _raw in self.raw_s :
                _s = (zeros(( 8,8 ))*0.0).tolist()
                _s[3-1][7-1] = 1.0
                _s[4-1][8-1] = 1.0
                _s[7-1][3-1] = 1.0
                _s[8-1][4-1] = 1.0
                for i in range(4) :
                      for j in range(4) :
                            _s[m[i]][m[j]] = _raw[p[i]][p[j]]

                self.s += [_s]
          self.nports = 8


    def cascadeSimple(self,r,c,pole) :
          from numpy import zeros, dot,pi
          from touchstone import s2t, t2s
          import pdb

          self.rl = []
          self.h = []


          _sPRE = zeros(( self.nports,self.nports )) * (0.0+1j*0.0)
          for ii in range(len(self.s)) :
                _s = self.s[ii]
                _f = self.frequency[ii]
                _t = s2t(_s)

                Z  = 1.0 / ( 1.0/r + _f * 1j * 2 * pi * c)
                RL = ( Z - 50 ) / ( Z + 50 )
                H  = 1.0 / ( 1.0 + ( 2.0 * pi * _f * 1j ) / ( 2.0 * pi * pole ) )
                self.rl += [RL]
                self.h  += [H]
                for i in range(self.nports) :
                      _sPRE[i][i] = RL
                for i in range(self.nports/2) :
                      _sPRE[i][i+self.nports/2] = H
                      _sPRE[i+self.nports/2][i] = H

                # pdb.set_trace()
                _tPRE = s2t(_sPRE)

                _tCASCADE = dot( dot( _tPRE, _t ), _tPRE )
```

```
            _sCASCADE = t2s(_tCASCADE)

            self.s[ii] = _sCASCADE



    def extractTransfer(self,pi,ni,pj,nj) :
          from numpy import array, dot, zeros
          T = array( [[+1.0,+1.0,+0.0,+0.0],\
                      [+1.0,-1.0,+0.0,+0.0],\
                      [+0.0,+0.0,+1.0,+1.0],\
                      [+0.0,+0.0,+1.0,-1.0]])
          Tp = array([[+0.5,+0.5,+0.0,+0.0],\
                      [+0.5,-0.5,+0.0,+0.0],\
                      [+0.0,+0.0,+0.5,+0.5],\
                      [+0.0,+0.0,+0.5,-0.5]])
          map = [pi-1,ni-1,pj-1,nj-1]

          for _s in self.s :
                s = zeros((4,4)) * (0.0+0.0j)
                for i in range(4) :
                      for j in range(4) :
                            s[i][j] = _s[map[i],map[j]]
                _t = dot(dot(T,s),Tp)
                # clearly this needs extending to include the other modes
                self.t += [_t[1,3]]

    def get(self,i,j) :
          r = []
          for _s in self.s :
                r += [_s[i-1][j-1]]
          return r

    # going to assume here that we only have one missing point!!! Needs extending
    for the final release
    def addDC(self,n) :
          from numpy import zeros, log10, absolute, polyfit, arange, diff,
    poly1d, angle, exp, transpose, flipud, floor, unwrap, pi
          from numpy.lib import linspace
          from scipy import interp
          import pdb
          import math
          from pylab import plot,figure,hold

          frequency = arange(0.0,self.frequency[0],diff(self.frequency[:2])[0])

          t = zeros(len(frequency)) * (0.0+0.0j)
          mag =[]
          for k in range(n) :
                mag += [log10((absolute(self.t[k])))]
          p = poly1d(polyfit(self.frequency[:n],mag,1))
          mag = p(frequency)
          # calculate r, when minimum frequency is too high and a 2pi wrap is
    necessary
          angleStep = min(diff(unwrap(angle(self.t[0:10]))))
          phase = arange(len(frequency)) * angleStep
          #pdb.set_trace()
```

```
      t = 10.0**mag * exp(1j*phase)
      figure()
      plot(self.frequency[0:20],angle(self.t[0:20]))
      hold(1)
      plot(self.frequency[0:20],angle(self.t[0:20]),'o')
      #print 'we are here'
      self.t = t.tolist() + self.t
      self.frequency = frequency.tolist() + self.frequency

      plot(self.frequency[0:20],angle(self.t[0:20]))
      plot(self.frequency[0:20],angle(self.t[0:20]),'x')


def loadFile(self,filename) :
      from string import upper,lstrip,rstrip
      from re import split, match
      from numpy import zeros
      from math import sin,cos,pi
      import sys

      # defaults for Touchstone 1.0 files
      victim_tx_P = 1   # ports in touchstone file for transmitter and
receiver
      victim_tx_N = 3
      victim_rx_P = 2
      victim_rx_N = 4

      i = -1
      j = -1
      part = 0
      tsfile = open(filename)
      try:
            for line in tsfile :
                  line = lstrip(rstrip(line))

                  #print 'found line <%s>'%line
                  #if ((len(line)>0) and (not line.startswith('!'))) :
                  if line.startswith('!') or len(line)==0:
                        pass # print "Ignoring comment"
                  else:
                        col = split('\s*', line)# FIXFIX usually works, but
Touchstone 2.0 allows wrapping
                        if col[0]=='#':
                              # option line format is: <frequency unit>
<parameter> <format> R <n>
                              # specifically: [HZ/KHZ/MHZ/GHZ] [S/Y/Z/G/H]
[MA/DB/RI] [R n]
                              # FIXFIX Touchstone 2.0 allows these in any
order
                              if upper(col[1])=='HZ' :
                                    print 'S-parameter file uses Hz units'
                                    Kfrequency = 1.0
                              elif upper(col[1])=='KHZ' :
                                    print 'S-parameter file uses KHz units'
                                    Kfrequency = 10.0**3
                              elif upper(col[1])=='MHZ' :
```

```
                                    print 'S-parameter file uses MHz units'
                                    Kfrequency = 10.0**6
                              elif upper(col[1])=='GHZ' :
                                    print 'S-parameter file uses GHz units'
                                    Kfrequency = 10.0**9

                              # RI for real-imaginary, MA for
magnitude-angle, DB for dB-angle
                              Ktype = upper(col[3])
                              if Ktype=='RI' :
                                    print 'S-parameter file uses
real-imaginary format'
                              elif Ktype=='MA' :
                                    print 'S-parameter file uses magnitude
format'
                              elif Ktype=='DB' :
                                    print 'S-parameter file uses dB format'
                              else :
                                    print 'S-parameter file uses unknown
format%s'%Ktype
                                    sys.exit()
                        elif upper(col[0])=='[VERSION]':
                              print 'Version: %s'%col[1]
                        elif upper(col[0])=='[NUMBER_OF_PORTS]':
                              print 'Number of Ports: %s'%col[1]
                              self.nports = int(col[1])
                        elif upper(col[0])=='[TWO-PORT_DATA_ORDER]':
                              print 'Two-Port Data Order (ignored): %s
%s'%(col[1], col[2])
                        elif upper(col[0])=='[REFERENCE]':
                              print 'Reference (ignored): %s'%col[1]
                        elif upper(col[0])=='[NUMBER_OF_FREQUENCIES]':
                              print 'Number of Frequencies (ignored):
%s'%col[1]
                        elif upper(col[0])=='[NUMBER_OF_NOISE_FREQUENCIES]':
                              print 'Number of Noise Frequencies (ignored):
%s'%col[1]
                        elif upper(col[0])=='[MATRIX_FORMAT]':
                              if upper(col[1]) == 'FULL' :
                                    print 'Matrix Format: %s'%col[1]
                              else :
                                    print 'Matrix Formats other than Full
are not supported: %s'%col[1]
                                    sys.exit()
                        elif upper(col[0])=='[INTERCONNECT_PORT_GROUPS]':
                              print 'Interconnect Port Groups: %s
%s'%(col[1], col[2])
                              numbers = split (',', col[1])
                              victim_tx_P = int(numbers[0])
                              victim_rx_P = int(numbers[1])
                              numbers = split (',', col[2])
                              victim_tx_N = int(numbers[0])
                              victim_rx_N = int(numbers[1])
                              print 'TX_P: %d -> RX_P: %d'%(victim_tx_P,
victim_rx_P)
                              print 'TX_N: %d -> RX_N: %d'%(victim_tx_N,
victim_rx_N)
```

```
                        else :
                              #print 'found data <%s>'%col
                              for _col in col :
                                    if (i==-1) and (j==-1) :
                                          i = 0
                                          j = 0
                                          self.frequency += [eval(col[0]) *
Kfrequency]
                                          s =
zeros((self.nports,self.nports)) * (0.0+0.0j)
                                          #print 'found frequency
%e'%self.frequency[-1]
                                    else :
                                          if part==0 :
                                                oldcol = _col
                                                part = 1
                                          else :
                                                if Ktype=='RI' :
                                                      s[i][j] = eval(oldcol)
+ 1.0j*eval(_col)

                                                elif Ktype=='MA' :
                                                      s[i][j] = eval(oldcol)
* cos(eval(_col) * pi / 180.0) \
                                                      + 1.0j * eval(oldcol)
* sin(eval(_col) * pi / 180.0)
                                                      #print 'added to %d,%d
%e'%(i,j,s[i][j])

                                                elif Ktype=='DB' :
                                                      magnitude =
10**(eval(oldcol)/20)
                                                      #print "Magnitude
%f"%magnitude
                                                      s[i][j] = magnitude *
cos(eval(_col) * pi / 180.0) \
                                                      + 1.0j * magnitude *
sin(eval (_col) * pi / 180.0)
                                                else :
                                                      print 'Unknown
format%s'%Ktype
                                                      tsfile.close()
                                                      sys.exit()
                                          part = 0
                                          i += 1
                                          if i==self.nports :
                                                i=0
                                                j+=1
                                                if j==self.nports :
                                                      j=-1
                                                      i=-1
                                                      self.raw_s +=
[s]
                                                      #print 'end of
array'
      finally:
            tsfile.close()
      return([self.nports, victim_tx_P, victim_rx_P, victim_tx_N,
victim_rx_N])
```

```
def s2t(s) :
from numpy import dot,concatenate,transpose,linalg,identity,pi

s_a = transpose(transpose(s[0:4])[0:4])
s_b = transpose(transpose(s[0:4])[4:8])
s_g = transpose(transpose(s[4:8])[0:4])
s_t = transpose(transpose(s[4:8])[4:8])

si = linalg.inv(s)

si_a = transpose(transpose(si[0:4])[0:4])
si_b = transpose(transpose(si[0:4])[4:8])
si_g = transpose(transpose(si[4:8])[0:4])
si_t = transpose(transpose(si[4:8])[4:8])

# print (identity(4) - dot(s_a, si_a))
# print linalg.inv(identity(4) - dot(s_a, si_a))

t_a = dot(dot( linalg.inv(identity(4) - dot(s_a, si_a)) , s_a), si_b)
t_b =            dot( linalg.inv(identity(4) - dot(s_a, si_a)) , s_b)
t_g =            dot( linalg.inv(identity(4) - dot(si_a, s_a)) , si_b)
t_t = dot(dot( linalg.inv(identity(4) - dot(si_a, s_a)) , si_a), s_b)

t = concatenate((transpose(concatenate((transpose(t_b),transpose(t_a)))),
transpose(concatenate((transpose(t_t),transpose(t_g)))) ))

return(t)


def t2s(t) :
from numpy import dot,concatenate,transpose,linalg,identity,pi

t_b = transpose(transpose(t[0:4])[0:4])
t_a = transpose(transpose(t[0:4])[4:8])
t_t = transpose(transpose(t[4:8])[0:4])
t_g = transpose(transpose(t[4:8])[4:8])

t = concatenate((transpose(concatenate((transpose(t_a),transpose(t_b)))),
transpose(concatenate((transpose(t_g),transpose(t_t)))) ))

ti = linalg.inv(t)

ti_a = transpose(transpose(ti[0:4])[0:4])
ti_b = transpose(transpose(ti[0:4])[4:8])
ti_g = transpose(transpose(ti[4:8])[0:4])
ti_t = transpose(transpose(ti[4:8])[4:8])

s_a = dot(dot( linalg.inv(identity(4) - dot(t_a,  ti_a)) , t_a),  ti_b)
s_b =            dot( linalg.inv(identity(4) - dot(t_a,  ti_a)) , t_b)
s_g =            dot( linalg.inv(identity(4) - dot(ti_a, t_a)) ,  ti_b)
s_t = dot(dot( linalg.inv(identity(4) - dot(ti_a, t_a)) ,  ti_a), t_b)

s = concatenate((transpose(concatenate((transpose(s_a),transpose(s_b)))),
transpose(concatenate((transpose(s_g),transpose(s_t)))) ))

return(s)
```

```
def test_s2t() :
from numpy import array,dot
from touchstone import s2t,t2s

left = array([

[-0.4555-0.0072j,-0.1140+0.1402j,-0.0000-0.0000j,-0.0000-0.0000j,+0.0002-0.0
010j,-0.0004+0.0008j,-0.0000-0.0000j,-0.0000-0.0000j],

[-0.1026+0.1374j,-0.0524-0.3005j,-0.0000-0.0000j,-0.0000-0.0000j,-0.0006+0.0
008j,+0.0008-0.0001j,-0.0000-0.0000j,-0.0000-0.0000j],

[-0.0000-0.0000j,-0.0000-0.0000j,-0.4289-0.0203j,-0.1083+0.0955j,-0.0009+0.0
012j,+0.0005-0.0011j,+1.0000+0.0000j,-0.0000-0.0000j],

[-0.0000-0.0000j,-0.0000-0.0000j,-0.0997+0.0949j,+0.0323-0.3276j,+0.0009-0.0
007j,-0.0004+0.0004j,-0.0000-0.0000j,+1.0000+0.0000j],

[+0.0002-0.0010j,-0.0006+0.0007j,-0.0008+0.0012j,+0.0009-0.0007j,+0.0532-0.3
280j,+0.0015-0.0362j,-0.0008+0.0012j,+0.0009-0.0007j],

[-0.0003+0.0008j,+0.0008-0.0001j,+0.0004-0.0011j,-0.0004+0.0004j,+0.0028-0.0
374j,+0.0756+0.0069j,+0.0004-0.0011j,-0.0004+0.0004j],

[-0.0000-0.0000j,-0.0000-0.0000j,+1.0000+0.0000j,-0.0000-0.0000j,-0.0009+0.0
012j,+0.0005-0.0011j,-0.4289-0.0203j,-0.1083+0.0955j],

[-0.0000-0.0000j,-0.0000-0.0000j,-0.0000-0.0000j,+1.0000+0.0000j,+0.0009-0.0
007j,-0.0004+0.0004j,-0.0997+0.0949j,+0.0323-0.3276j]])

right = array([
[0,0,0,0,1,0,0,0],
[0,0,0,0,0,1,0,0],
[0,0,0,0,0,0,1,0],
[0,0,0,0,0,0,0,1],
[1,0,0,0,0,0,0,0],
[0,1,0,0,0,0,0,0],
[0,0,1,0,0,0,0,0],
[0,0,0,1,0,0,0,0]])

left_t = s2t(left)
right_t = s2t(right)

answer_t = dot(left_t,right_t)
answer = t2s(answer_t)

return(answer)


def printM(m) :
for i in range(m) :
      for j in range(m[0]) :
            print '%8.3,'%(real(m[i][j])),
      print '\n'
```

C.9 testcase.py

The following Python file runs a single StatEye simulation.

```
# Simple test script for stateye v5

# class found on python.org to “print to screen and file with one print statement”
# http://mail.python.org/pipermail/python-list/2003-February/188788.html
class writer :
     def __init__(self, *writers) :
            self.writers = writers

     def write(self, text) :
            for w in self.writers :
                  w.write(text)

import sys
sys.path += [‘../v5’]
import warnings
warnings.filterwarnings(‘ignore’)
import portalocker

# User defined parameters

csvfile    = ‘all.csv’
altcsvfile = ‘all_alt.csv’
filename= ‘SAS2_transmittertestload.s4p’

timeResolution  = 2.0e-12

#txfilename= ‘PHY_CJTPAT_clean_6G_wfm’
txfilename= ‘’
responselength= 50
startsample     = 0 # 20000
#finishsample = 600000
finishsample= 100000
timecol    = 3
sigcol     = 4
txStep     = ‘extractedStep.csv’
txNoise    = ‘noise.csv’

# default values for Touchstone 1.0 files
numberPorts = 4          # number of port in touchstone file
victim_tx_P = 1   # ports in touchstone file for transmitter and receiver
victim_tx_N = 3
victim_rx_P = 2
victim_rx_N = 4

scrambled= 0      # is analysis based on scrambled or 8b10b data
# Changed to 8b/10b data (scrambled = 0) on December 9, 2009 document 10-007r0
# scrambled = 1 # is analysis based on scrambled or 8b10b data
deemphasis= 0.0   # which de-emphasis, in dB
dfetaps    = 3          # how many DFE taps
baudrate= 6.0e9   # what baud rate
padR       = 50         # pad DC termination resistance
padCap     = 950e-15# pad capacitance
lpf        = 10.0e9# 1st order LPF corner frequency
pws        = 0          # pulse width shrinkage, or edge jitter in UI
BUJ        = 0.10       # Deterministic pp jitter
RJ         = 0.15/15.883# Random RMS jitter, measured using 10101010 pattern
# Replaced RJ = 0.15/14.0 with RJ = 0.15/15.883 on December 9, 2009 document 10-007r0
# RJ = 0.15/14.0 # Random RMS jitter, measured using 10101010 pattern
```

```
TxNorm= 1.0       # Normalised transmit amplitude, only relevant when tx signal is being
     generated
BER        = -15

# Simulation parameters (probably best not to touch)
sweepResolution = 0.01
startCursor = -8
finishCursor = 30
DCextrapolation = 6

#################################################################
# execution starts here. Don't change anything unless you
# know what you are doing
#################################################################

# try to cleanup environment, in case this is not the first time
try :
     del mySParam
except :
     print "no need to delete mySParam data structure"
try :
     del myStateye
except :
     print "no need to delete myStateye data structure"

# load and reload all necessary modules

import pdb
from numpy import *
import numpy
from pylab import *
import time
from string import rsplit, rstrip
from scipy import linalg
from re import *

import penrose
import stateye
import analysis
import touchstone
import extractJitter
import getopt

#################################################################
# when running from the command line, get the options used
# and overwrite the script defaults
#################################################################

outfilemodifier = ''
ion()

def usage():
    print "Arguments: -s <s4p filename> [-a N][-d N][-t N][-b N][-8]"
    print "-s <s4p filename>   input .s4p file (mandatory argument)"
    print "-a N               transmitter amplitude (in Vpp); default is 1 (ampN added to
     output filenames)"
    print "-d N                transmitter deemphasis (in dB); default is 0 (deempN added
     to output filenames)"
    print "-t N                receiver dfe taps; default is 3 (.dfeN added to output
     filename)"
    print "-c 8|R             coding - 8b10b (.8b10b added to output filenames) or random
     (.rand added to output filename)"
```

```
    print “-b N              baud rate (in bps); default is 6.0e9 (.baudN added to output
     filename)”
     print “                    default is random.  8b10b simulations take longer.”
    print “An optional argument only contributes to the output filename if used - default
     settings do not.”

try:
     opts, args = getopt.getopt(sys.argv[1:], “a:c:d:s:t:b:q”, [“help”])
except getopt.GetoptError:
    usage()
    sys.exit(2)
for opt, arg in opts:
    if opt in (“-h”, “--help”):
        usage()
        sys.exit()
    elif opt == “-a”:  # amplitude
        TxNorm = float(arg)
        outfilemodifier += ‘_amp’ + arg
    elif opt == “-d”:  # deemp
        deemphasis = float(arg)
        outfilemodifier += ‘_deemp’ + arg
    elif opt == “-t”:  # dfetaps
        dfetaps = int(arg)
        outfilemodifier += ‘_dfe’ + arg
    elif opt == “-c”:  # coding scrambled/8b10b
        if arg == “8”:
            scrambled = 0
            outfilemodifier += ‘_8b10b’
        elif arg == “r”:
            scrambled = 1
            outfilemodifier += ‘_rand’
    elif opt == “-b”:  # baudrate
        baudrate = float(arg)
        outfilemodifier += ‘_baud’ + arg
    elif opt == “-s”:  # --s4p filename
        filename = arg
    elif opt == “-q” : # quiet
        ioff()

resultPrefix = filename.replace(“.s4p”, “”);
resultPrefix = filename.replace(“.s8p”, “”);  # RE kludge

# output all print statements to both screen and a .log file
savedstdout = sys.stdout
fout = file(resultPrefix + outfilemodifier + ‘.log’, ‘w’)
sys.stdout = writer(sys.stdout, fout)

print “Major settings: \n\tfilename=%s \n\tamp=%f \n\tdeemphasis=%f \n\tdfetaps=%d
     \n\tcoding=%d \n\tbaudrate=%0.2e”%(filename, TxNorm, deemphasis, dfetaps, scrambled,
     baudrate)

############################################################
# Main script initialise objects
############################################################

myStateye = stateye.stateye()

if len(txfilename)>0 :
     print ‘extracting step response from measurement’
     tag = time.time()
     [inputT, outputsignalF, signalF, timestep] =
     penrose.penrose(txfilename,responselength,startsample,finishsample,timecol,sigcol)
```

```
     print 'finished in %0.1f sec'%(time.time()-tag)

     print 'extracting jitter from measurement'
     tag = time.time()
     [RJ,BUJ] = extractJitter.extractJitter(inputT, outputsignalF, signalF, 2, RJ,
     timestep, responselength)
     print 'finished in %0.1f sec'%(time.time()-tag)

mySParam = touchstone.touchstone()
# load the Touchstone file
print 'loading Touchstone file'
tag = time.time()
[numberPorts, victim_tx_P, victim_rx_P, victim_tx_N, victim_rx_N] =
     mySParam.loadFile(filename)
print 'finished loading in %0.1f sec'%(time.time()-tag)

# print 'Nyquist Sdd21=%f'%(mySParam.frequency[long(baudrate/2)])

mySParam.map( [victim_tx_P,victim_tx_N,victim_rx_P,victim_rx_N ])
mySParam.cascadeSimple(padR,padCap,lpf)

print 'creating step responses'
tag = time.time()
# extract to Dc

# extract the differential transfer function, given the port definitions
mySParam.extractTransfer(1,2,5,6)
mySParam.addDC(DCextrapolation)

# generation the step, and interpolate down to necessary resolution
print 'generating time step'
if len(txfilename)>0 :
     mySParam.getStep(timeResolution, txStep, txNoise,0)
else :
     mySParam.getStep(timeResolution, [], [],TxNorm)

# calculate how many time steps in one UI
UI = int(floor(1.0/baudrate/timeResolution))

# load the step response into stateye objects
myStateye.loadStep(mySParam.step, UI, pws)
print 'finished time step in %0.1f sec'%(time.time()-tag)

# calculated the FIR tap for de-emphasis
fir = -(1.0 - 10**(-deemphasis / 20)) / 2.0

# create states and transition edges
print 'creating transitions'
tag = time.time()
if scrambled :
     myStateye.create2TapFIR( [1.0+fir, fir], dfetaps)
else :
     myStateye.create8b10b_2TapFIR( [1.0+fir, fir], dfetaps)
print 'finished in %0.1f sec'%(time.time()-tag)

# calculate the ISI pdf
print 'calculating pdf'
tag = time.time()
noise_x = [0]
noise_y = [1]
myStateye.calcpdf(sweepResolution,startCursor,finishCursor,BUJ,RJ,noise_x,noise_y)
print 'finished pdf in %0.1f sec'%(time.time()-tag)
```

```
# initially the transfer function
print ‘graphing spectrum’
figure()
plot(mySParam.frequency,20*log10(absolute(mySParam.t)))
hold(1)
plot(mySParam.frequency[-len(mySParam.rl):],20*log10(absolute(mySParam.rl)))
plot(mySParam.frequency[-len(mySParam.rl):],20*log10(absolute(mySParam.h)))
legend([‘Victim’,’Return Loss’,’Damping’],’center right’)
xlabel(‘Frequency [Hz]’)
ylabel(‘Sdd21 [dB]’)
title(‘Channel Response’)
grid(1)
axis([0,baudrate*2,-40,0])
savefig(resultPrefix + outfilemodifier + ‘_spectrum.png’)

# pulse and step response
print ‘graphing pulse and step response’
figure()
hold(0)
x = []
y = []
y2 = []
for cursor in arange(startCursor,finishCursor,0.01) :
     x += [cursor]
     y += [myStateye.pulse[myStateye.cursor2index(0,cursor)]]
     y2 += [myStateye.inputStep[myStateye.cursor2index(0,cursor+2)]]

plot(x,y)
hold(1)
plot(x,y2)
grid(1)
xlabel(‘Time [UI]’)
ylabel(‘Amplitude [V]’)
title(‘Post channel Pulse and Step Response’)
savefig(resultPrefix + outfilemodifier + ‘_pulse_step.png’)

# jitter statistical eye
print ‘graphing stateye’
figure()
pdf_pj_log = ( log10(transpose(myStateye.pdf_pj)+1.0e-17) )
contourf(myStateye.sweep, myStateye.binaxis , pdf_pj_log,arange(-15,0,0.5))
maxamp = 0.0
minamp = myStateye.midBin

for _a in transpose(pdf_pj_log)[2:-2] :
     _maxamp = min(find(_a[myStateye.midBin:] > BER ))
     _minamp = max(find(_a[:myStateye.midBin] > BER ))
     if _maxamp > maxamp :
            maxamp = _maxamp
     if _minamp < minamp :
            minamp = _minamp
amplitude = myStateye.binaxis[myStateye.midBin + maxamp]-myStateye.binaxis[minamp]
print ‘Amplitude is %0.3f’%(amplitude)
Jmin = max(find( pdf_pj_log[myStateye.midBin][:len(myStateye.sweep)/2] > BER ))
Jmax = min(find( pdf_pj_log[myStateye.midBin][len(myStateye.sweep)/2:] > BER )) +
     len(myStateye.sweep)/2
jitter = 1.0 - (myStateye.sweep[Jmax] - myStateye.sweep[Jmin])
print ‘Jitter is %0.3f’%(jitter)

grid(1)
eyeLeft = find( max( pdf_pj_log[myStateye.midBin][:len(myStateye.sweep)/2] ) ==
```

```
     pdf_pj_log[myStateye.midBin][:len(myStateye.sweep)/2] )[0]
eyeRght = find( max( pdf_pj_log[myStateye.midBin][len(myStateye.sweep)/2:] ) ==
     pdf_pj_log[myStateye.midBin][len(myStateye.sweep)/2:] )[0] + len(myStateye.sweep)/2
axisMax = myStateye.binaxis[ max(find(transpose(pdf_pj_log)[0]>-17)) ]
axisMin = myStateye.binaxis[ min(find(transpose(pdf_pj_log)[0]>-17)) ]
axis([myStateye.sweep[eyeLeft],myStateye.sweep[eyeRght],axisMin*1.2,axisMax*1.2])
xlabel('Time [UI]')
ylabel('Amplitude [V]')
title('Eye Opening %0.3fV, Jitter %0.3fUIpp\nTx=%0.3fmV, BER=10%d'%(amplitude,
     jitter,TxNorm,BER))
savefig(resultPrefix + outfilemodifier + '_stateye.png')

print('\"%s\", \"%s\", %f, %f, %d, %e, %d, %f, %f\n'\
                  %(resultPrefix + outfilemodifier, time.strftime("%Y%m%d %H:%M:%S",
     time.localtime()), \
                    TxNorm, deemphasis, dfetaps, baudrate, scrambled, amplitude, jitter))

# add results to output database. Simplistic handling of a file lock
# conflict - just write to a backup database instead
try:
     f = open(csvfile,'a')
     portalocker.lock (f, portalocker.LOCK_EX);
     f.writelines('\"%s\", \"%s\", %f, %f, %d, %e, %d, %f, %f\n'\
                          %(resultPrefix + outfilemodifier, time.strftime("%Y%m%d
     %H:%M:%S", time.localtime()), \
                            TxNorm, deemphasis, dfetaps, baudrate, scrambled, amplitude,
     jitter))
     f.close()
except IOError:
     print "Error opening csvfile %s, trying alternate %s"%(csvfile, altcsvfile)
     f = open(altcsvfile,'a')
     portalocker.lock (f, portalocker.LOCK_EX);
     f.writelines('\"%s\", \"%s\", %f, %f, %d, %e, %d, %f, %f\n'\
                          %(resultPrefix + outfilemodifier, time.strftime("%Y%m%d
     %H:%M:%S", time.localtime()), \
                            TxNorm, deemphasis, dfetaps, baudrate, scrambled, amplitude,
     jitter))
     f.close()

# close the .log file and return to using stdout only
sys.stdout = savedstdout
fout.close()
```

C.10 testall.py

The following Python file runs a set of StatEye simulations.

```
import fnmatch
import os
import subprocess
import string
import sys

pythonPath = "c:/program files/python25/python.exe"   # or
     "c:/python25/python.exe"
rootPath = string.replace(string.rstrip(os.popen('cd').readlines()[0]),'\\','/')
#rootPath = 'c:/pub/stateye/v5.080111'  # location of the .s4p files, if the
```

```
    current directory is not the one

# run simulations with all combinations of the following
sparmfiles = [ '*.s4p']  # s4p filename(s), honors UNIX shell-style wildcards
amps = [ '0.850' ] # TxNorm amplitude settings
deemps = [ '2', '3', '4' ]  # deemphasis settings
dfetaps = [ '3' ]  # dfetaps settings
# Changed default coding to '8'=8b10b document 10-007r0 on December 9, 2009
codings = [ '8'  ]  # scrambled settings '8'=8b10b, 'r'=random
rates = [ '6.0e9' ] # physical link rates (bits per second)

# FIXFIX add a linux equivalent, parsing /proc/cpuinfo
numprocs = int(os.getenv('NUMBER_OF_PROCESSORS'));
print "%d processors available"%numprocs;
# use at least 1 process, but leave 1 processor free if multiple are available
if (numprocs == 0):
    numprocs = 1;
    numprocs = 1;
if (numprocs > 2):
    numprocs = numprocs - 1;
if (numprocs > 3):
    print "code changes needed in testall.py needed to support more than 3
    subprocesses";
    numprocs = 3;
print "using %d subprocesses"%numprocs;
procslot = 0;

print "Running Stateye"
for sparmfile in sparmfiles:
    for root, dirs, files in os.walk(rootPath):
        for filename in files:
            if fnmatch.fnmatch(filename, sparmfile):
                for coding in codings:
                    for amp in amps:
                        for deemp in deemps:
                            for dfetap in dfetaps:
                                for rate in rates:
                                    cmd = [\
                                        pythonPath,\
                                        "testcase.py",\
                                        "-s", os.path.join(root, filename),\
                                        "-a", amp,\
                                        "-d", deemp,\
                                        "-t", dfetap,\
                                        "-c", coding,\
                                        "-b", rate\
                                        ]
                                    print "Running testcase.py -s %s -a %s -d %s
    -t %s -c %s -b %s"%(filename, amp, deemp, dfetap, coding, rate)
                                    #retcode = subprocess.call(cmd)
                                # FIXFIX can python handle an array of objects?
    workaround for now...
                                    if (procslot == 0):
                                        p0 = subprocess.Popen (cmd);
                                    elif (procslot == 1):
                                        p1 = subprocess.Popen (cmd);
                                    elif (procslot == 2):
```

```
                                        p2 = subprocess.Popen (cmd);

                                    procslot = procslot + 1;

                                    if (procslot == numprocs):
                                        print “Waiting for 3 completions”
                                        retcode0 = p0.wait();
                                        retcode1 = p1.wait();
                                        retcode2 = p2.wait();
                                        procslot = 0;
                                        print “Completed 3 with retcode=%d %d
    %d”%(retcode0, retcode1, retcode2)

# if any jobs are left over, wait for completion
if (procslot == 2):
    print “Waiting for 2 completions”
    retcode0 = p0.wait();
    retcode1 = p1.wait();
    print “Completed 2 with retcode=%d %d”%(retcode0, retcode1)
elif (procslot == 1):
    print “Waiting for 1 completion”
    retcode0 = p0.wait();
    print “Completed 1 with retcode=%d”%retcode0

print “Stateye done”
```

C.11 File StatEye_readme.pdf

How to install and run the SAS-2.1 StatEye.

StatEye is used to determine if a channel’s insertion loss is compliant with the SAS-2 specification. The files included in the SAS2,1.zip file run StatEye on the SAS-2 reference channel with the appropriate reference transmitter and receiver settings.

Step 1: Download SAS2.1.zip from the T10 site.

www.T10.org

Step 2: Download and Install Python (version 2.5) from the Python web site.

www.Python.org

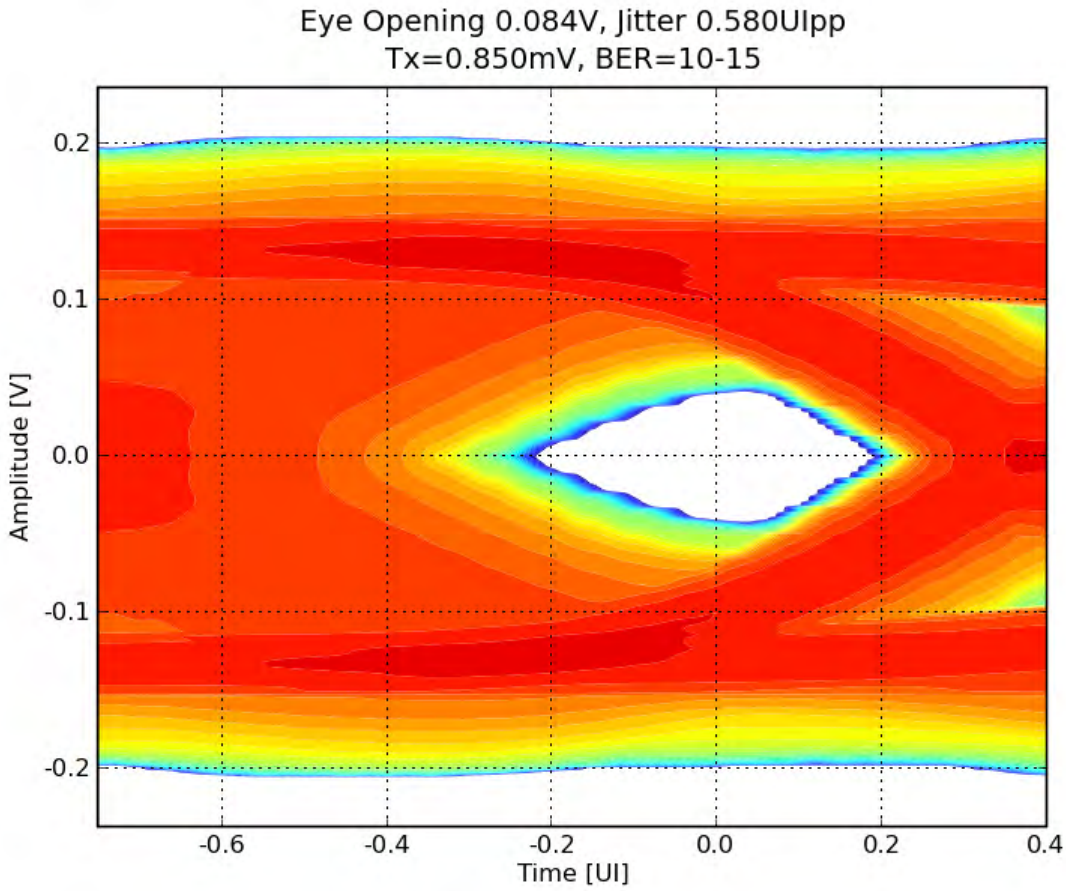
The Python installation path is typically "c:/python25/python.exe." If your installation is different edit testall.py to reflect your installation path.

pythonPath = "your_path/python.py"

Step 3: Run the primary script.

testall.pl

The run takes about 20 minutes and should produce the following StatEye result.



You can see the reference channel (i.e., SAS2_transmittertestload.s4p) is compliant because the Eye Opening is 84mV and total jitter is 0.58UI.

Step 4: To determine if your channel is compliant, edit testall.pl to point to your file.

sparmfiles = ['your_channel.s4p']

Step 5: Re-Run testall.pl and verify the eye opening meets the SAS-2 requirements.

Annex D
(normative)

End-to-end simulation for trained 12 Gbps

D.1 Detailed end-to-end simulation procedure description for trained 12 Gbps

The following procedure describes the end-to-end simulation process:

1) extract the un-equalized pulse response between ET and RR from:
    a) the captured signal into a zero-length test load or measured transfer function; and
    b) the reference transfer functions of the appropriate end-to-end simulation schematic (see D.3, D.4, and D.5);
2) compute the reference transmitter equalization (see 5.8.3);
3) compute reference receiver DFE equalization (see 5.9.5.7.3);
4) compute an equalized pulse response by applying the reference transmitter equalization and the reference receiver DFE equalization to the un-equalized pulse response between ET and RR;
5) compute the Vertical eye opening at the sampling instants defined by a reference sampling clock (see figure 113 in figure 5.8.3), for a BER of 10^{-15} assuming 8b10b data, using the equalized pulse response and the asynchronous crosstalk from all significant crosstalk sources;
6) measure the peak-to-peak reference pulse response cursor from the equalized pulse response (see figure 113 in figure 5.8.3); and
7) compute the vertical eye opening to reference pulse response cursor ratio.

Crosstalk information is provided as:

a) crosstalk transfer functions; or
b) a crosstalk signal amplitude that occurs at a probability of 10^{-6}.

When crosstalk information is provided as crosstalk transfer functions, the vertical eye opening is simulated at a BER of 10^{-15}, using the following procedure:

1) connect asynchronous reference transmitters to generate crosstalk according to the appropriate end-to-end simulation schematic (see D.3, D.4, and D.5);
2) set the characteristics of the crosstalk transmitters per table D.1;
3) simulate the resulting amplitude due to crosstalk; and
4) compute the vertical eye opening at a BER of 10^{-15}.

Table D.1 — Crosstalk transmitter characteristics

Characteristic	Units	Value
Peak-to-peak voltage (V_{p-p})	mV(P-P)	1 200
Output gain (K_0)	V/V	0.6
Rise/fall time	ps	20.8
Differential impedance	ohm	100
Common-mode impedance	ohm	25
Coefficient 1	V/V	0
Coefficient 2	V/V	1
Coefficient 3	V/V	0

When crosstalk information is provided as a signal amplitude at a probability of 10^{-6}, the vertical eye opening is computed by summing:

a) the simulated ISI not equalized by the transmitter equalization and receiver DFE equalization, at a BER of 10^{-15} assuming 8b10b data; and
b) the total crosstalk at a probability of 10^{-6}, scaled by the maximum gain of the TxRx connection segment between the crosstalk measurement point and the reference receiver input.

The maximum gain of the reference channel is computed by simulation using the following procedure:

1) connect a reference transmitter to the TxRx connection segment between the crosstalk measurement point and the reference receiver input;
2) terminate the TxRx connection segment on the receiver end;
3) set the reference transmitter coefficient 1 to 0, coefficient 2 to 1, coefficient 3 to 0 and K_0 to 0.5; and
4) compute the maximum gain as the maximum peak-to-peak voltage at the output of the TxRx connection segment, assuming 8b10b data.

D.2 Usage models, S-parameter files and crosstalk amplitude

Table D.2 describes the usage models used for:

a) transmitter devices connected to passive TxRx connections;
b) passive TxRx connection segments between CT_S and CR or IT_S and IR; and

c) receiver devices connected to passive TxRx connections.

Table D.2 — S-parameter files and crosstalk amplitude per usage models

End-to-end simulation type [a]	S-parameter files [b] [c]	Measurement point	Description of S-parameter files	Crosstalk amplitude at a probability of 10^{-6} (mV_{p-p}) [d]	
				Min	Max
Usage model: Long passive cable, drive to host					
Transmitter devices (see figure D.1, figure D.2, and figure D.2)	LongPassiveD2H_IT_RR.s4p LongPassiveD2H_IT_RR_NEXTx.s4p LongPassiveD2H_IT_RR_FEXTx.s4p LongPassiveD2H_ET_IT.s4p LongPassiveD2H_IT_PR_rev.s4p LongPassiveD2H_ET_IT_rev.s4p	IT or CT	PICS - connector + RDCS + D2H RCCS	NA	NA
	LongPassiveD2H_IT_RR.s4p LongPassiveD2H_IT_RR_NEXTx.s4p LongPassiveD2H_IT_RR_FEXTx.s4p LongPassiveD2H_ET_IT.s4p LongPassiveD2H_ET_ITs_rev.s4p	IT	RDCS + D2H RCCS	NA	NA
TxRx connection segment between IT_S and IR or CT_S and CR	LongPassiveD2H_ET_CTs.s4p LongPassiveD2H_CR_RR.s4p LongPassiveD2H_ET_CTs_NEXTx.s4p LongPassiveD2H_ET_CTs_FEXTx.s4p LongPassiveD2H_CR_RR_NEXT.s4p LongPassiveD2H_CR_RR_FEXT.s4p LongPassiveD2H_ET_CTs_rev.s4p	From IT_S to IR or from CT_S to CR	D2H TCCS + TDCS; and RDCS + D2H RCCS	NA	NA
Stressed receiver device (see figure D.4)	LongPassiveD2H_CR_RR.s4p	IR or CR	RDCS + D2H RCCS	15	20

Key:
Max. = Maximum
Min. = Minimum.
NA = Not applicable

[a] When many cases are provided for a single simulation type, the measurement shall be taken at the available measurement point that is the closest to the receiver end of the link.
[b] When multiple through files are provided, the first one shall be used before the PICS under test (i.e. between ET and the first measurement point), and the second one shall be used after the PICS under test (i.e. between the second measurement point and RR). See 5.6.6.
[c] See figure 112 for a description of the NEXT and FEXT extraction.
[d] This is the crosstalk measured from the crosstalk generator only. See 5.8.4 and 5.9.5.7.6.7.

Table D.2 — S-parameter files and crosstalk amplitude per usage models

End-to-end simulation type [a]	S-parameter files [b] [c]	Measurement point	Description of S-parameter files	Crosstalk amplitude at a probability of 10^{-6} (mV_{p-p}) [d]	
				Min	Max
Usage model: Long passive cable, host to drive					
Transmitter devices (see figure D.1, figure D.2, and figure D.3)	LongPassiveH2D_IT_RR.s4p LongPassiveH2D_IT_RR_NEXTx.s4p LongPassiveH2D_IT_RR_FEXTx.s4p LongPassiveH2D_ET_IT.s4p LongPassiveH2D_IT_PR_rev.s4p LongPassiveH2D_ET_IT_rev.s4p	IT or CT	PICS - connector + RDCS + H2D RCCS	NA	NA
	LongPassiveH2D_IT_RR.s4p LongPassiveH2D_IT_RR_NEXTx.s4p LongPassiveH2D_IT_RR_FEXTx.s4p LongPassiveH2D_ET_IT.s4p LongPassiveH2D_ET_ITs_rev.s4p	IT	RDCS + H2D RCCS	NA	NA
TxRx connection segment between IT_S and IR or CT_S and CR	LongPassiveH2D_ET_CTs.s4p LongPassiveH2D_CR_RR.s4p LongPassiveH2D_ET_CTs_NEXTx.s4p LongPassiveH2D_ET_CTs_FEXTx.s4p LongPassiveH2D_CR_RR_NEXT.s4p LongPassiveH2D_CR_RR_FEXT.s4p LongPassiveH2D_ET_CTs_rev.s4p	From IT_S to IR or from CT_S to CR	H2D TCCS + TDCS; and RDCS + H2D RCCS	NA	NA
Stressed receiver device (see figure D.4)	LongPassiveH2D_CR_RR.s4p	IR or CR	RDCS + H2D RCCS	15	20

Key:
Max. = Maximum
Min. = Minimum.
NA = Not applicable

[a] When many cases are provided for a single simulation type, the measurement shall be taken at the available measurement point that is the closest to the receiver end of the link.
[b] When multiple through files are provided, the first one shall be used before the PICS under test (i.e. between ET and the first measurement point), and the second one shall be used after the PICS under test (i.e. between the second measurement point and RR). See 5.6.6.
[c] See figure 112 for a description of the NEXT and FEXT extraction.
[d] This is the crosstalk measured from the crosstalk generator only. See 5.8.4 and 5.9.5.7.6.7.

Editor's Note 10: S-parameter files listed in table D.2 are under development and not available for inclusion in SAS3r04.zip at the time of posting.

D.3, D.4 and D.5 describe end-to-end simulation schematics for each device or relevant TxRx connection

segment. Refer to D.6 for an example usage.

D.3 Transmitter device end-to-end simulation schematic

Figure D.1 shows the end-to-end simulation schematic for trained 12 Gbps transmitter devices connected to a separable TxRx connection segment (see 5.9.4.7.4) and the asymmetrical reverse transfer functions (i.e., <usage>_ET_IT_rev). Symmetrical transfer functions use the same transfer function for both directions (i.e., <usage>_ET_IT).

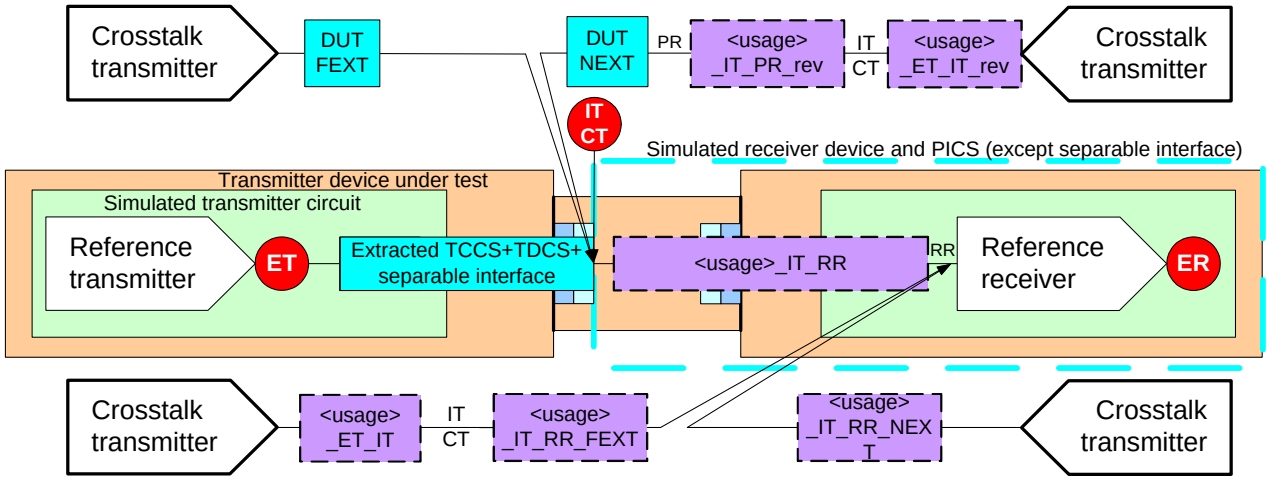


Figure D.1 — Transmitter device end-to-end simulation schematic that includes a separable TxRx connection segment

Figure D.2 shows PR on a crosstalk TxRx connection

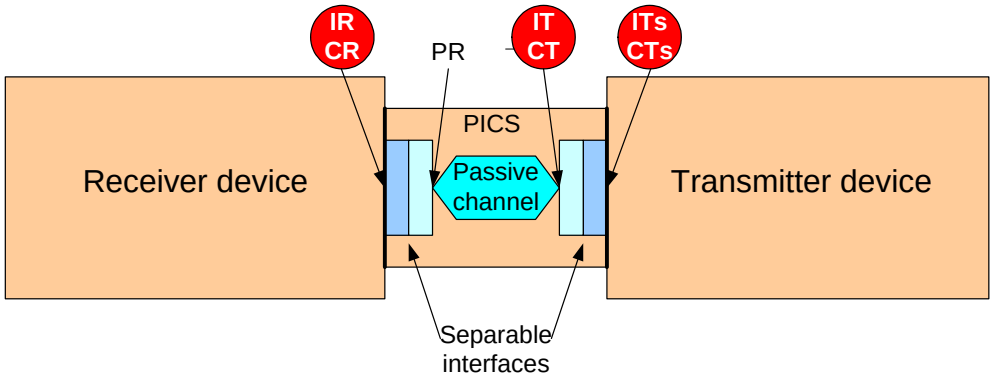


Figure D.2 — Crosstalk TxRx connection points

Figure D.3 shows the end-to-end simulation schematic for trained 12 Gbps transmitter devices not connected to a separable TxRx connection segment (see 5.9.4.7.4) and the asymmetrical reverse transfer functions (i.e.,

<usage>_ET_ITs_rev). Symmetrical transfer functions use the same transfer function for both directions (i.e., <usage>_ET_ITs).

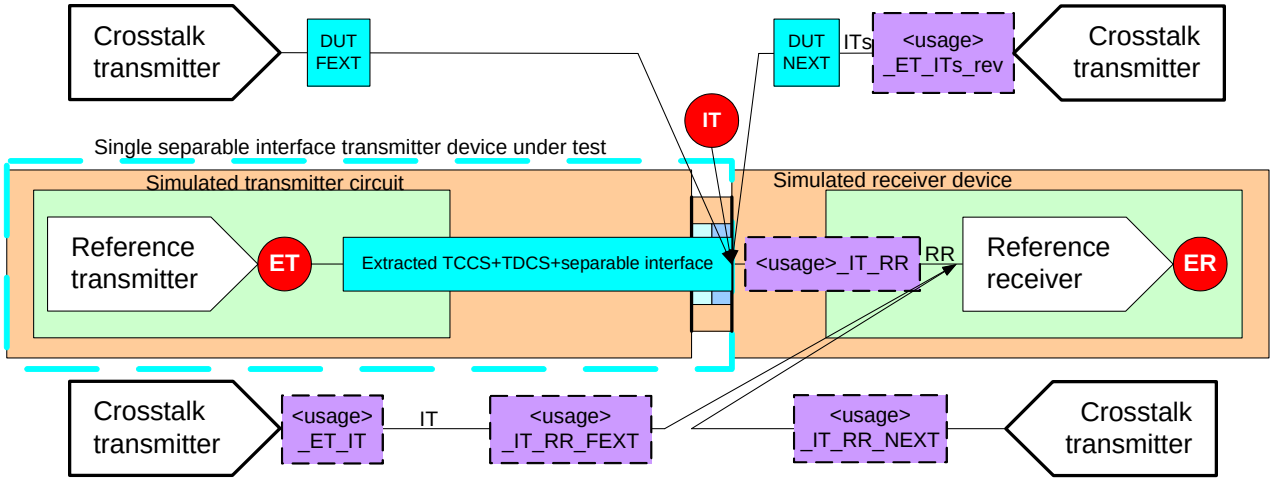


Figure D.3 — Transmitter device end-to-end simulation schematic that includes a non-separable TxRx connection segment

D.4 Passive TxRx connection segment end-to-end simulation schematic

Figure 94 (see 5.6.6) shows the end-to-end simulation schematic for passive TxRx connection segments between IT_S and IR or between CT_S and CR for trained 12 Gbps.

D.5 Stressed Receiver device delivered signal calibration end-to-end simulation schematic

Figure D.4 shows the end-to-end simulation schematic for the stressed receiver device delivered signal calibration for trained 12 Gbps (see 5.9.5.7.6.6). For the calibration, noise sources (DJ, RJ, SJ and SSC) shall not be activated.

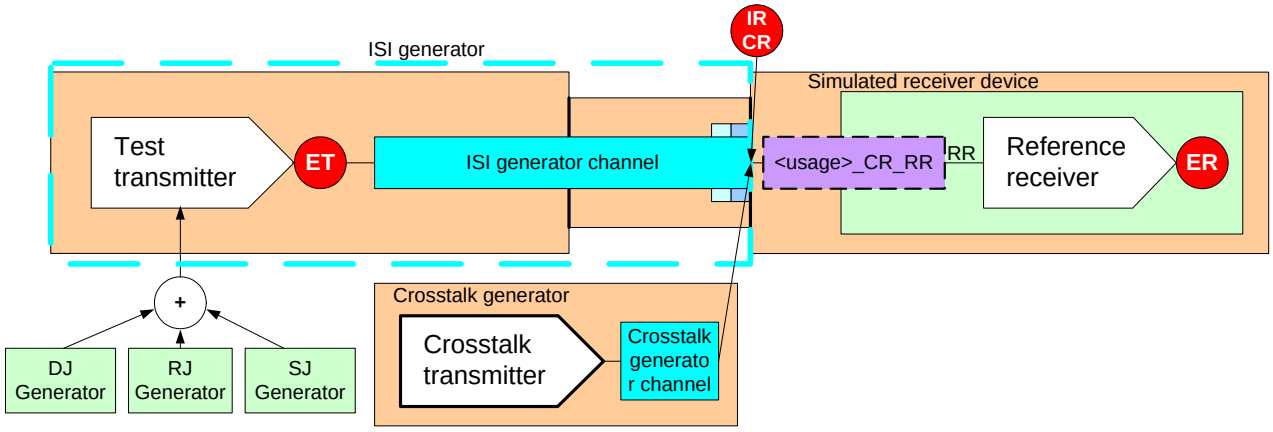


Figure D.4 — Stressed receiver device delivered signal calibration end-to-end simulation schematic

D.6 End-to-end simulation templates using SAS3_EYEOPENING (informative)

SAS3.zip contains example configuration files for use with SAS3_EYEOPENING, for end-to-end compliance. When using this simulator, the compliance process is simplified to the following steps:

Editor's Note 11: Example configuration files are under development and not available for inclusion in SAS3r04.zip at the time of posting.

1) capture the S-parameters (passive TxRx connection segment compliance) or capture the real-time signal (all other compliances) at compliance(s) point(s);
2) edit the configuration script template (i.e., SAS3_template.m) to select the desired usage model and the compliance type (e.g., transmitter device, passive connection segment, etc.)(see figure D.5);

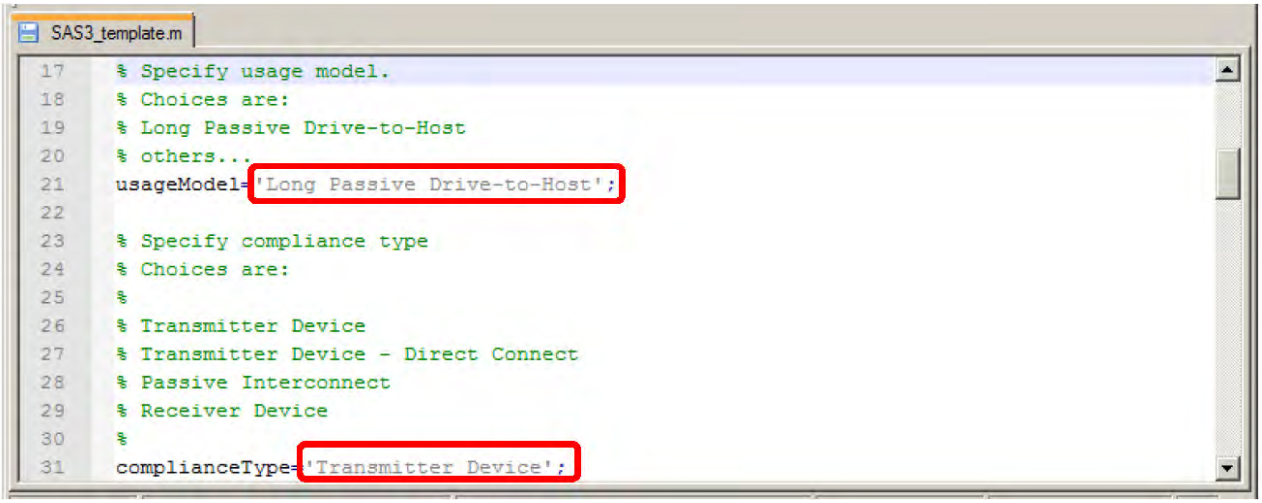
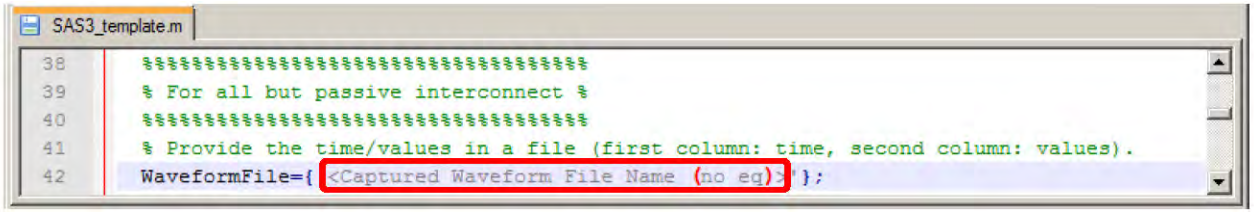


Figure D.5 — SAS3_EYEOPENING usage model and compliance type

3) edit the configuration script to reference the captured signal file from step 1 according to the type of measurement (i.e., captured signal or S-parameter) as shown in figure D.6;



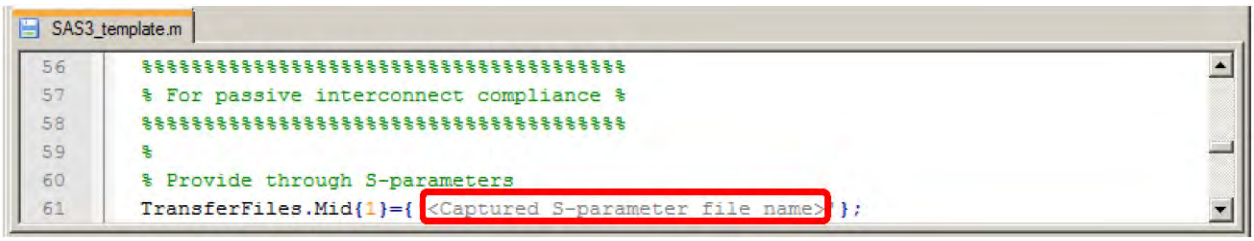


Figure D.6 — SAS3_EYEOPENING configuration script for file measurement type

4) when real-time captured signals are used, edit the configuration script to modify the oversampling rate and optionally provide reference digital data stream as shown in figure D.7;

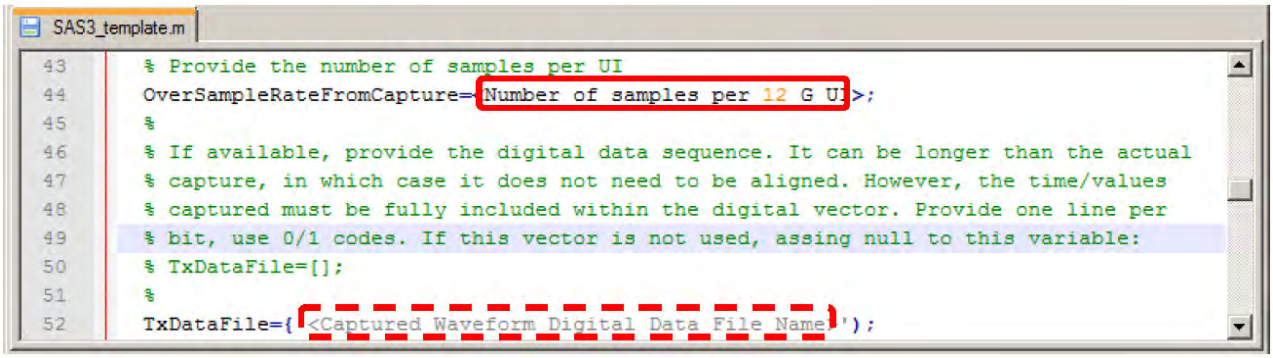


Figure D.7 — SAS3_EYEOPENING oversampling rate and reference data stream configuration scripts

5) capture the S-parameters of crosstalk aggressors, or measure the crosstalk amplitude (see X.4);
6) edit the configuration script to reference the captured signal from step 5 (see figure D.8); and

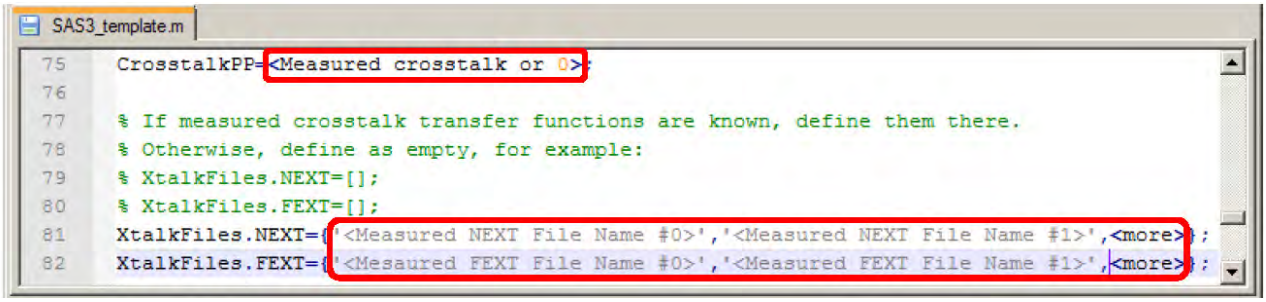


Figure D.8 — SAS3_EYEOPENING script configuration for crosstalk

7) run the edited configuration script using an appropriate tool, such as Octave (see http://www.gnu.org/software/octave/) or equivalent, in the correct directory (see figure D.9).

Figure D.9 — SAS3_EYEOPENING example directories

To capture a real-time signal, set the transmitter to the no_equalization coefficient setting (see SPL-2), and capture 20 000 consecutive UI at a sampling rate of 40 Gbps or more into a zero-length test load. The captured signal should have a fixed average number of samples per UI, so SSC is not allowed to be enabled.

Table D.3 lists the available usage models contained in SAS3.zip.

Table D.3 — Available usage models

Usage model class	Usage model
Trained 12 Gbps passive TxRx connection	Long passive cable connection, drive to host
	Long passive cable connection, host to drive

Annex E
(informative)

Signal performance measurements

E.1 Signal performance measurements overview

This annex describes methodologies for making electrical performance measurements, including signal output, signal tolerance, and return loss. Standard loads are used in all cases so that independent specification of connection components and transportability of the measurement results are possible.

E.2 Glossary

E.2.1 port: In this annex, the physical input or output connection of an instrument or device.

E.3 Simple physical link

E.3.1 Simple physical link overview

The physical link consists of the following component parts:

a) the transmitter device;
b) the interconnect; and
c) the receiver device.

Each of these components is connected by a separable connector. On a TxRx connection, signals travel in opposite directions down the same nominal path.

Figure E.1 shows a physical link and the location of the connectors.

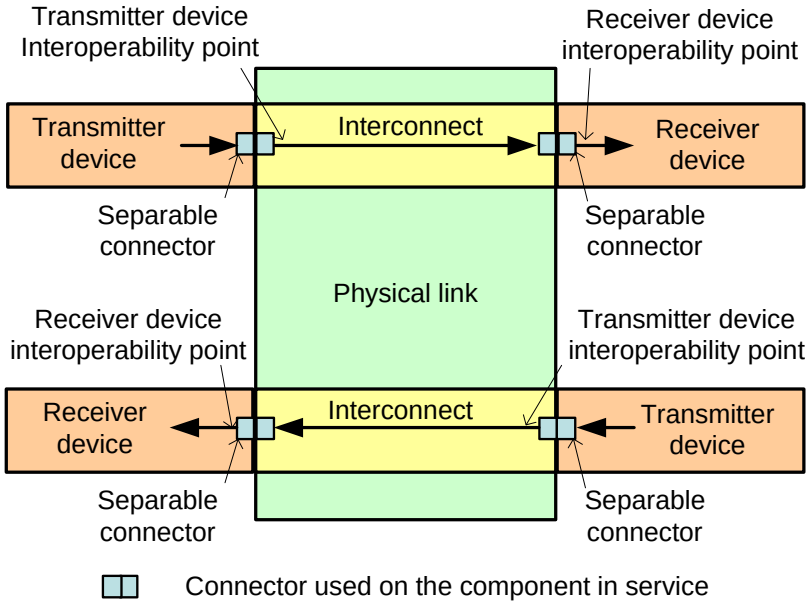


Figure E.1 — A simple physical link

Since connectors are always used in the mated condition, the only practical access to the signals is before the signal enters the mated connector (i.e., upstream) or after the signal exits the connector (i.e., downstream). Even if signals were able to be accessed at the point of mating within the connector, such access may disturb the connector to the point that the measurement of the signal is compromised (e.g., attempting to access the unmated connector with probes does not provide valid results because the connector is not in the same condition when unmated as when mated and the probe contact points are not at the same location as the connector contact points).

In this annex, signal outputs are always measured downstream of the mated connector (see figure E.1) so that the contribution of the mated connector to the signal properties is included in the measurement. This approach assigns a portion of the connector losses to the upstream component, but it also makes the signal measurement conservative. If the connectors on both ends of the interconnect are the same, then the additional loss at the downstream connector is offset by the reduced loss at the upstream connector.

E.3.2 Assumptions for the structure of the transmitter device and the receiver device

Figure E.2 shows the details of a transmitter device.

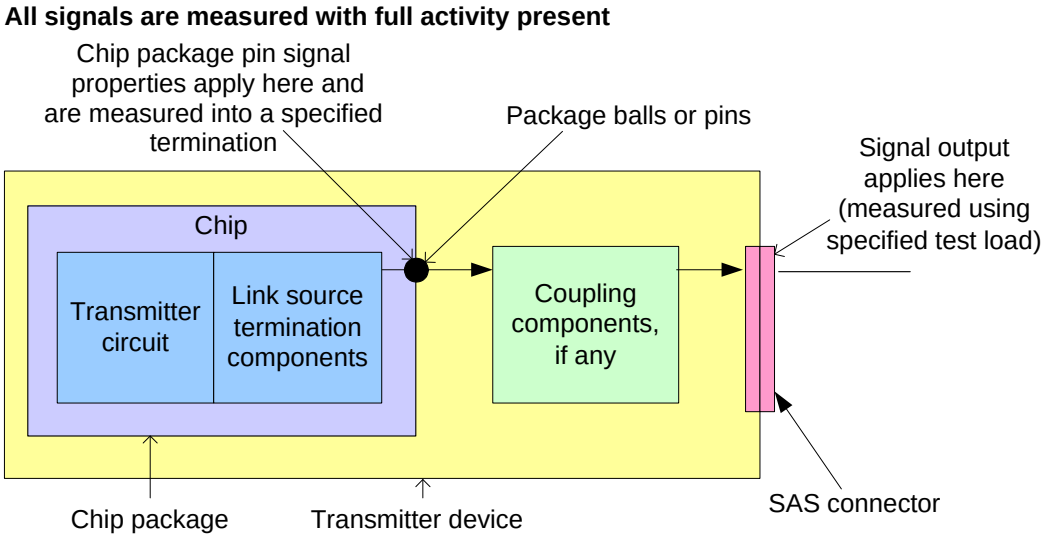


Figure E.2 — Transmitter device details

As figure E.2 shows, any of the following internal parts of this transmitter device may be labeled as the transmitter:

a) the transmitter circuit in the chip;
b) the chip itself; or
c) the chip and its associated chip package.

The term transmitter is therefore not well defined and is not used in the terminology without a modifier.

The transmitter device contains:

a) a connector (i.e., half a mated pair);
b) coupling components. if any;
c) PCB traces and vias;
d) the chip package;
e) ESD protection devices, if any;
f) the source termination; and
g) the transmitter circuit.

It is assumed that the source termination is contained within the chip package.

Although interoperability points are defined at the chip package pins in some standards (e.g., Ethernet XAUI), this standard does not define requirements at chip package pins.

Figure E.3 shows the details of a receiver device. It is similar to the transmitter device.

All signals measured with full activity present

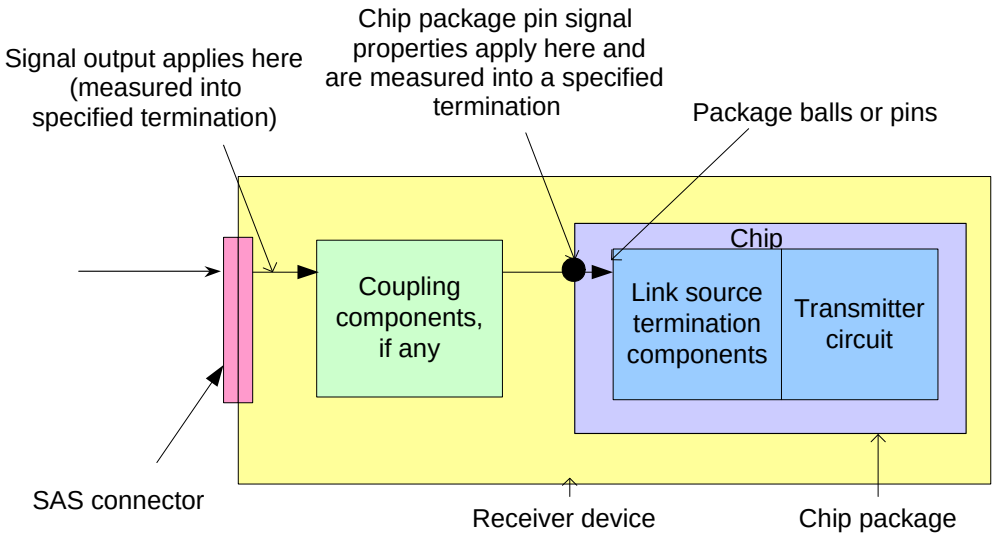


Figure E.3 — Receiver device details

As figure E.3 shows, any of the following internal parts of this receiver device may be labeled as the receiver:

a) the receiver circuit in the chip;
b) the chip itself; or
c) the chip and its associated chip package.

The term receiver is therefore not well defined and is not used in the terminology without a modifier.

The receiver device contains:

a) a connector (i.e., half a mated pair);
b) coupling components, if any;
c) PCB traces and vias;
d) the chip package;
e) ESD protection devices, if any;
f) the physical link termination; and
g) the receiver circuit.

It is assumed that the physical link termination is contained within the chip package.

E.3.3 Definition of receiver sensitivity and receiver device sensitivity

The term receiver sensitivity is not well-defined and is therefore not used in this standard. A related term applicable to the receiver device input signal is receiver device sensitivity. While these two terms are related, they are significantly different because of the noise environment assumed. The description in this subclause is used to define these terms with the understanding that this standard discourages usage of either term.

For 1.5 Gbps and 3 Gbps, receiver device sensitivity is defined as the minimum vertical inner eye opening measured at the signal output point for the input to the receiver device at which the receiver chip (i.e., the receiver circuit in the chip package on the board containing the receiver device interoperability point as shown in figure E.3) delivers the required BER (see 5.9.1) with:

a) the minimum horizontal eye opening;
b) all activity expected in the application for the receiver circuit present (i.e., not quiesced as for the receiver sensitivity definition); and
c) the CJTPAT pattern being received (see Annex A).

For 6 Gbps, receiver device sensitivity is defined as the minimum vertical inner eye opening determined by simulation. The signal measured at the input to the receiver device is processed in a manner to simulate the additional interconnect losses (e.g., board traces, chip package). Then, the equalization function provided by the receiver circuit is applied to determine the resulting eye opening.

E.10 describes special test conditions to measure these sensitivities.

This standard uses the term signal tolerance instead of receiver device sensitivity.

E.4 Signal measurement architecture

E.4.1 General

Signal specifications are only meaningful if the signals are able to be measured with practical instrumentation and if different laboratories making measurements on the same signal get the same results within acceptable measurement error (i.e., the measurements need to be accessible, verifiable, and transportable). As of the publishing of this standard, there are no accepted standards for creating signals with traceable properties and with all the properties needed for an effective signal specification architecture for high speed serial applications.

Some of the elements necessary for practical, verifiable, and transportable signal measurements are included in this standard.

Having signal specifications at interoperability points that do not depend on the actual properties of the other physical link components not under test requires that specified known test loads be used for the signal measurements. In service, the load presented to the interoperability point is that of the actual component and environment.

Interfacing with practical instruments requires that specified impedance environments be used. This forces a signal measurement architecture where the impedance environment is 50 ohm single-ended (i.e., 100 ohm differential) and also forces the requirement for instrumentation-quality loads of the correct value.

Instrumentation-quality loads are readily available for simple transmission line termination. However, no instrumentation-quality loads are available for more complex loads that include specified propagation time, insertion loss properties, crosstalk properties, and jitter creation properties.

For signal tolerance measurements, the signal is calibrated before applying it to the interoperability point under test. This signal calibration is done by adjusting the properties of the specified signal source system as measured into a laboratory-quality test load until the desired signal tolerance specifications are met. The signal source system is then disconnected from the laboratory-quality test load and connected to the interoperability point under test. It is assumed that any changes to the signal from the calibration state to the measurement state are caused by the interoperability point under test and are therefore part of the performance sought by the measurement.

E.4.2 Relationship between signal compliance measurements at interoperability points and operation in systems

The signal measurements in this standard apply under specified test conditions that simulate some parts of the conditions existing in service (e.g., this simulation includes full-duplex traffic on all phys and under all applicable environmental conditions). Other features existing in service (e.g., non-ideal return loss in parts of the physical link that are not present when measuring signals in the specified test conditions) may be included in the signal specifications themselves. This methodology results in signal performance requirements for each side of the interoperability point that do not depend on knowing the properties of the other side.

Measuring signals in an actual functioning system at an interoperability point does not verify compliance for the components on either side of the interoperability point, although it does verify that the specific combination of components in the system at the time of the measurement produces compliant signals. Interaction between components on either side of the interoperability point may allow the signal measured to be compliant, but this

compliance may have resulted because one component does not meet the signal specifications while the other exceeds the signal specifications.

Additional margin should be allowed when performing signal compliance measurements to account for conditions existing in service that may not have been accounted for in the specified measurements and signal specifications.

E.5 De-embedding connectors in test fixtures

Connectors are part of the test fixtures (e.g. test loads) needed for obtaining access to the interoperability points. This is intrinsic for most practical measurements because the connectors used on the service components are different from those used on the instrumentation.

The effects of the portions of the connector used on the test fixture are taken into account when measurements are made using the fixture so that the results of interoperability point under test are not influenced by the performance of the test fixture connector. This accounting process is termed de-embedding.

Figure E.4 shows two cases that apply.

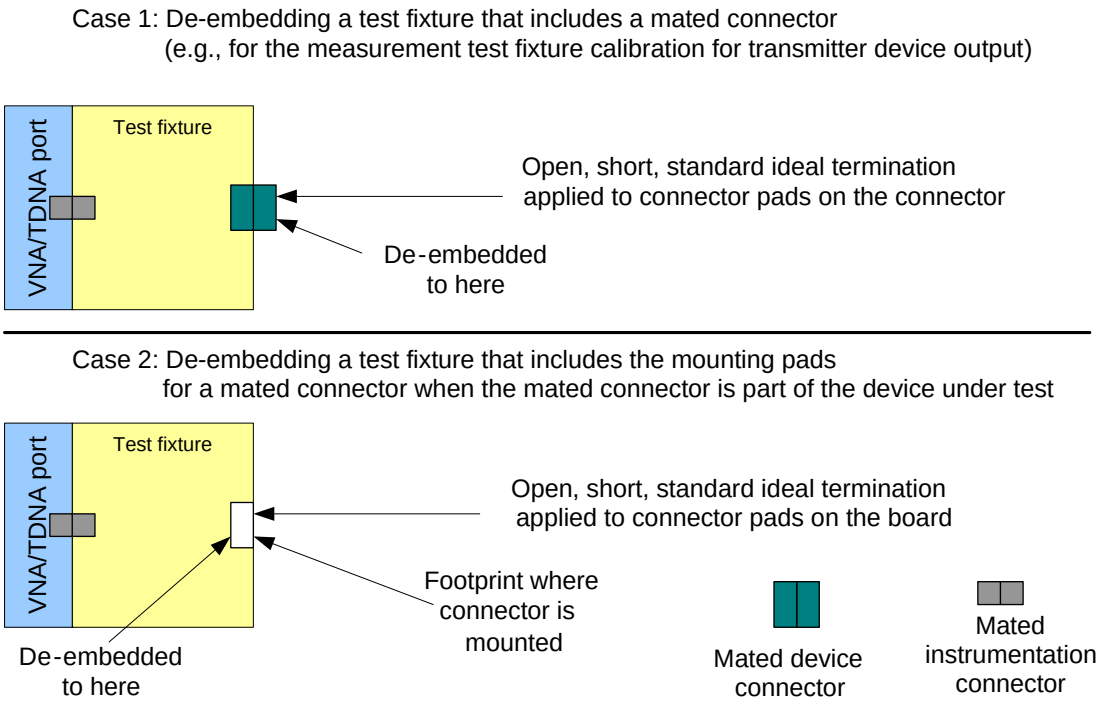


Figure E.4 — De-embedding of connectors in test fixtures

The de-embedding process assumes that the test fixture is linear and that S-parameter methodologies (see E.11) are used. An S-parameter model for the test fixture with or without the connector in place is the result. Knowing this model for the test fixture, with or without the connector in place, allows simulation of the impact of the test fixture on the signal measurement.

E.6 De-embedding test fixture for 12 Gbps Transmitter compliance

Connectors and board traces are part of the test fixtures (e.g. test loads) needed for obtaining access to transmitter compliance point (TC). The effects of the test fixture and test board de-embedding by creation of a de-embedding filter to cancel their effects on the measurements.

Figure E.5 shows the test fixture for a Transmitter compliance test.

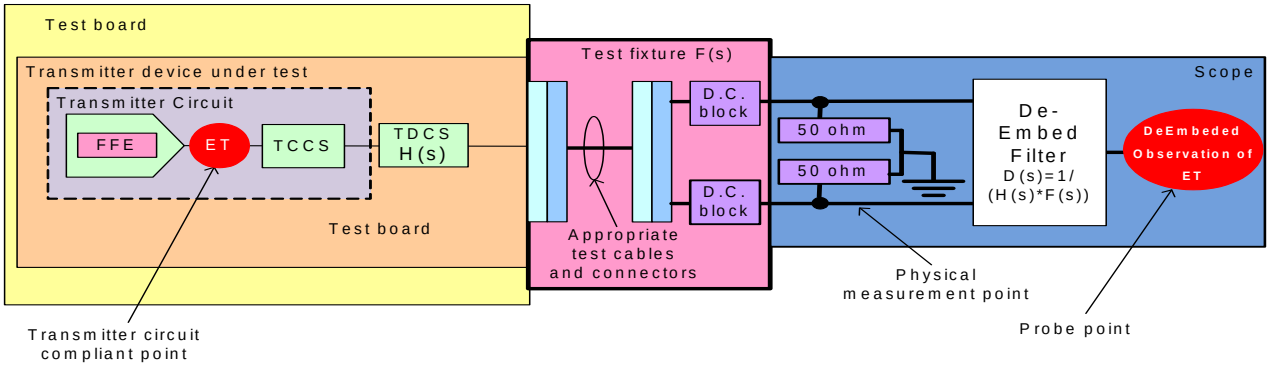


Figure E.5 — De-embedding of connectors in test fixtures

Figure E.6 shows a test structure for measuring the channel to be de-embedded.

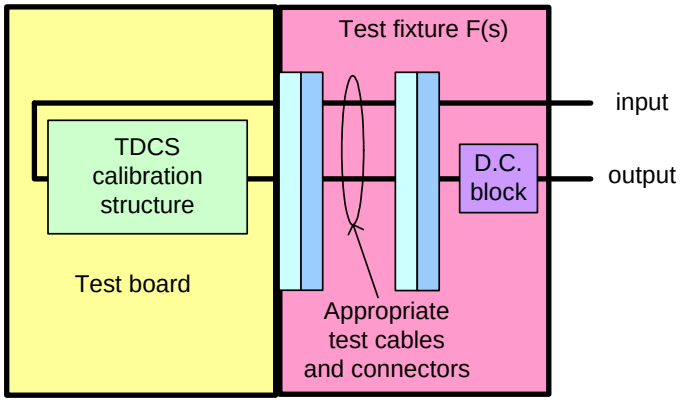


Figure E.6 — De-embedding calibration test structure

The de-embedding process consist of the following steps:

1) Measure a de-embedding test structure equivalent to the TDCS H(s) and test fixture F(s).
2) Compute an appropriate de-embedding filter D(s).
3) Exercise the transmitter to demonstrate compliance observed at the output of the de-embedding filter.

E.7 Measurement conditions for signal output at the transmitter device

The measurement conditions for a differential transmitter device signal output are shown in figure E.7. Figure E.7 applies to the following cases:

a) the transmitter device is directly attached to the zero length test load (see 5.7.2); and
b) the transmitter device is attached to the TCTF test load (see 5.7.3).

To simulate the properties of the interconnect assembly, instrumentation-quality test loads as shown in figure E.8 are used.

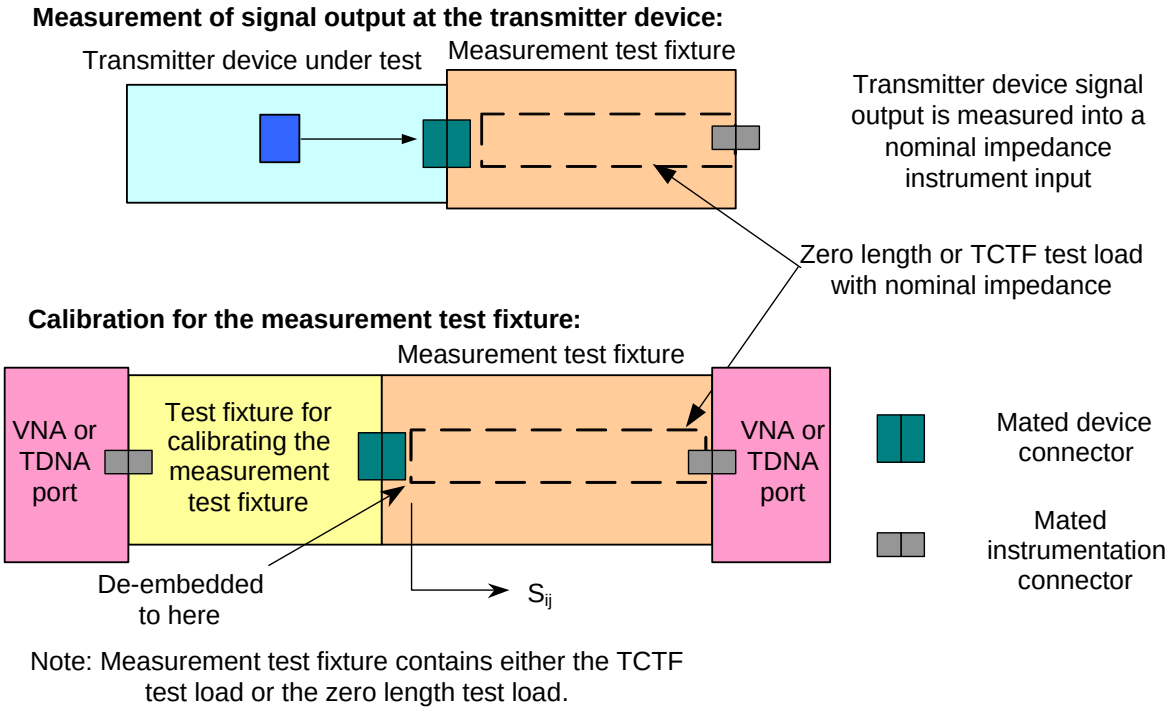


Figure E.7 — Measurement conditions for signal output at the transmitter device

An instrumentation-quality cable assembly connects the measurement test fixture to the instrumentation port. This cable assembly is considered part of the instrumentation and is not specifically shown in figure E.7, figure E.8, figure E.9, figure E.10, figure E.11, figure E.12, and figure E.13.

A measurement test fixture may be constructed from an instrumentation-quality TCTF test load with instrumentation-quality connectors and a connector adapter as shown in figure E.8. This method may be useful when using multiple device connector types but adds extra components that may increase loss and delay. For best accuracy, this method is not recommended. Extra components make it more difficult for the transmitter device to meet the required output specifications.

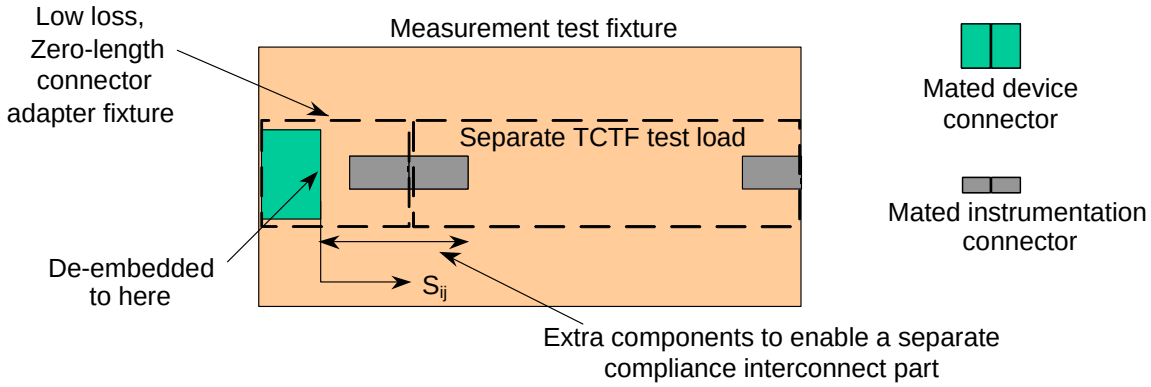


Figure E.8 — Transmitter device signal output measurement test fixture details

E.8 Measurement conditions for signal tolerance at the transmitter device

The measurement conditions for the signal tolerance at the differential transmitter device interoperability point are shown in figure E.9. Figure E.9 shows the test signal is launched into the interconnect assembly (e.g., cable assembly or PCB) that is attached to the receiver device.

This standard does not include this performance requirement, but it is included here for completeness.

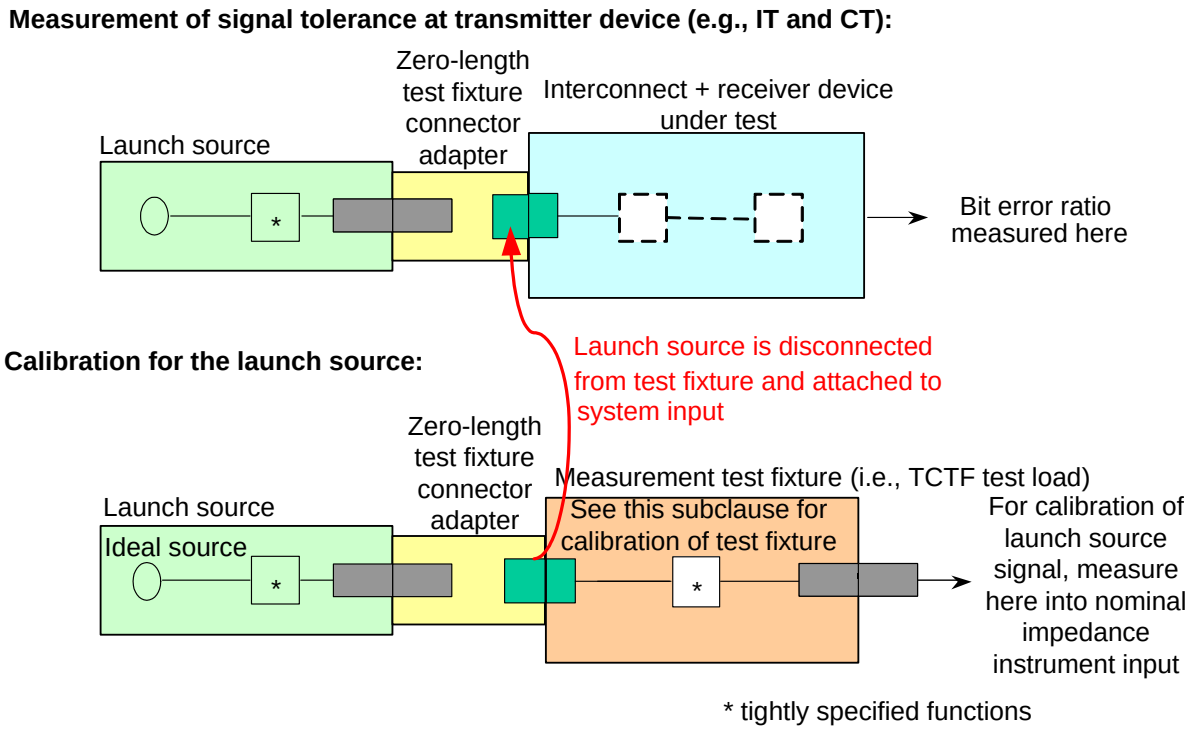


Figure E.9 — Measurement conditions for signal tolerance at the transmitter device

Figure E.10 shows calibration of the measurement test fixture.

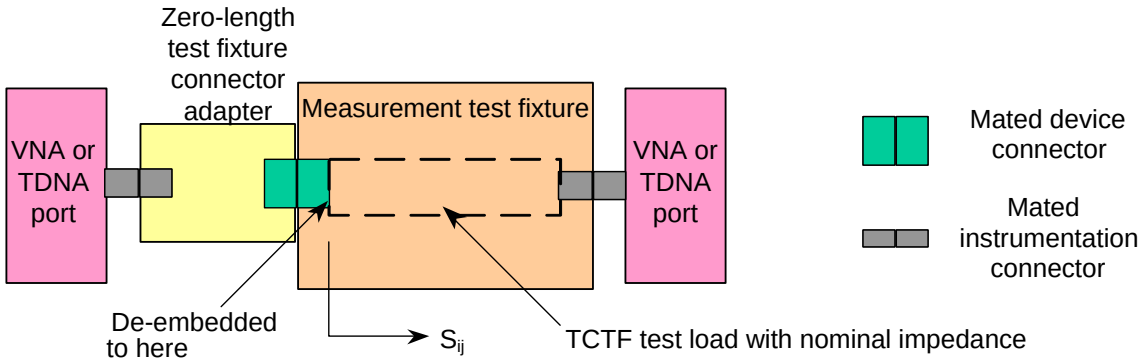


Figure E.10 — Calibration of test fixture for signal tolerance at the transmitter device

E.9 Measurement conditions for signal output at the receiver device

Figure E.11 shows the measurement conditions for the signal output at the receiver device.

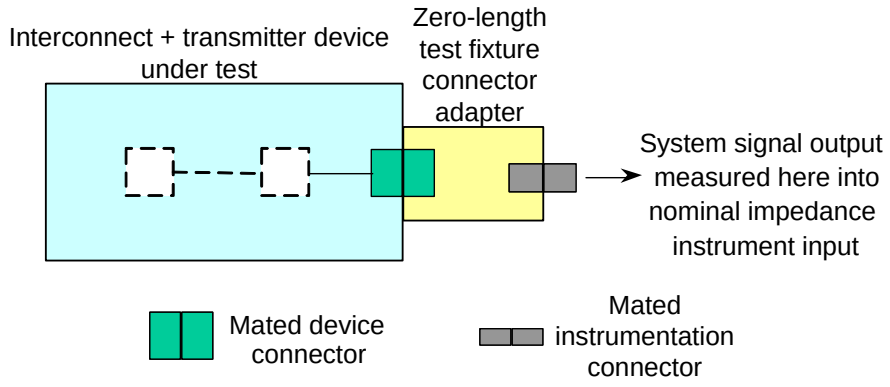


Figure E.11 — Measurement conditions for signal output at the receiver device

The interconnect may be the zero-length connector adaptor where the transmitter device is connected directly to the receiver device.

E.10 Measurement conditions for signal tolerance at the receiver device

Figure E.12 shows the measurement conditions for the signal tolerance at the differential receiver device interoperability point (see 5.9.5.4).

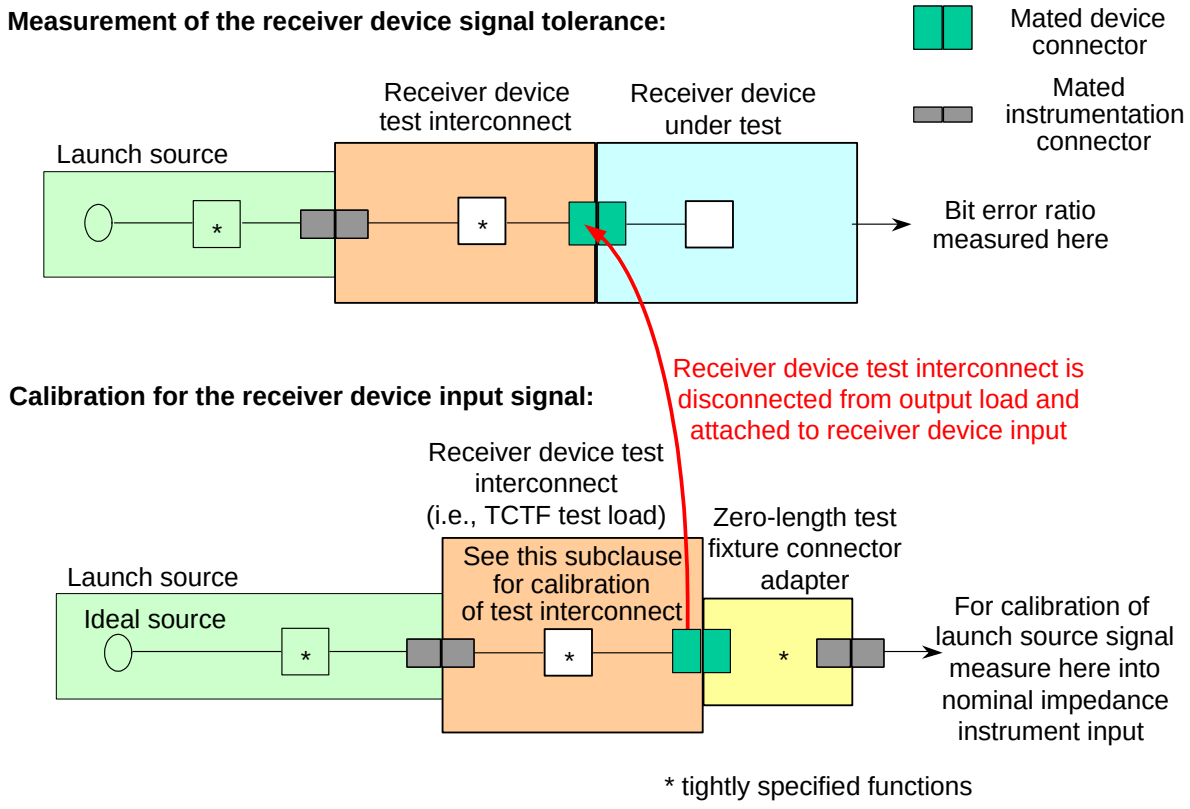
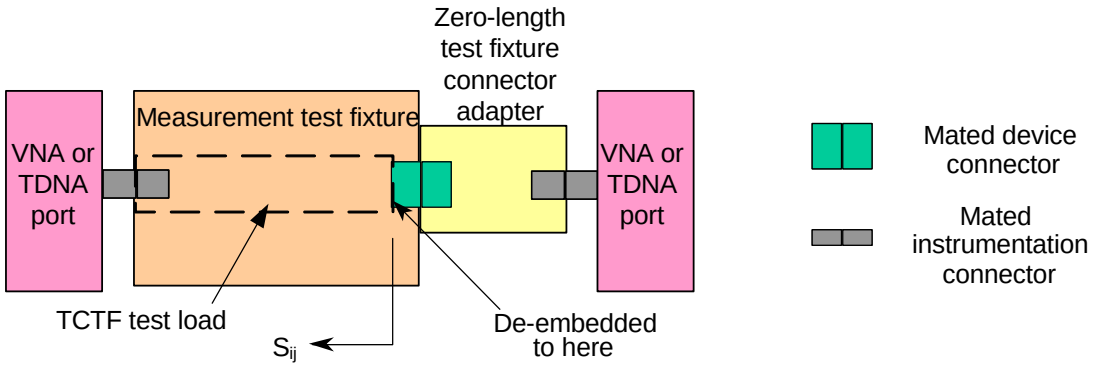


Figure E.12 — Measurement conditions for signal tolerance at the receiver device

Figure E.13 shows calibration of the measurement test fixture.



NOTE 1 - This is not identical to the measurement test fixture used for the transmitter output signal even though the connector genders are the same. The pins used in the SAS connector are for the Rx (i.e., not the Tx) signals and the signals flow the other way. The S_{22} measurement here is the same as the S_{11} measurement for the transmitter output signal but on different pins.

NOTE 2 - The S_{21} and S_{12} are used to create the desired jitter in this application and are not as critical.

Figure E.13 — Calibration of test fixture for signal tolerance at the receiver device

E.11 S-parameter measurements

E.11.1 S-parameter overview

Properties of physical link elements that are linear may be represented by S-parameter (i.e., scattering parameter) spectra.

S-parameters are the preferred method of capturing the linear properties of physical link elements. A frequency domain spectrum output is used for all S-parameters and specifying pass/fail limits to such a spectrum may overconstrain the system because some peaks and properties are benign to the application.

There are two problematic areas when applying S-parameters to differential electrical physical links:

a) naming conventions (see E.11.2); and
b) use of single-ended vector network methods on differential and common-mode systems (see E.11.3).

E.11.4 describes using special test fixtures to make S-parameter measurements.

E.11.2 S-parameter naming conventions

There are two types of measurements performed with S-parameters:

a) return loss from the same port of the element; and
b) insertion loss across the element.

Each S-parameter is a function of frequency returning complex numbers and is expressed with:

a) a magnitude component, usually expressed in dB; and
b) a phase component.

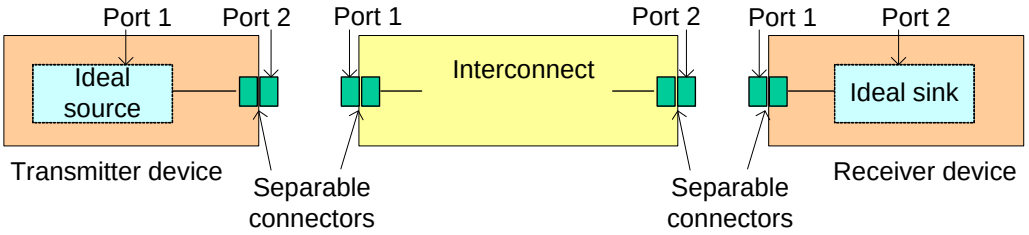
For a two-port linear element having ports i and j with the signals being either differential or common-mode, S_{ij} is the ratio of the signal coming out of the ith port (i.e., the response) to the signal coming into the jth port (i.e., the stimulus).

A port number convention is used where the downstream port is always port 2 and the upstream port is always port 1. The stream direction is determined by the direction of the primary signal launched from the transmitter device to the receiver device (e.g., in this standard, since each differential pair carries a signal in only one direction, the port nearest the transmitter device is port 1 and the port nearest the receiver device is port 2).

There are four combinations of ports for a two-ported system yielding the following S-parameters:

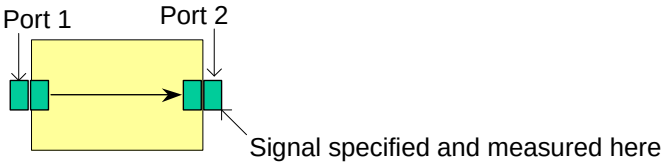
a) S_{11} (i.e., negative return loss): measured at port 1;
b) S_{21} (i.e., negative insertion loss): measured at port 1;
c) S_{22} (i.e., negative upstream return loss): measured at port 2 of the element. The measurement is the same kind of measurement that is done at port 1 to measure S_{11}; and
d) S_{12} (i.e., negative upstream insertion loss): measured at port 2 of the element. The measurement is the same kind of measurement that is done at port 1 to measure S_{21}.

Figure E.14 shows the port naming conventions for physical link elements, loads, and where those elements exit.



The transmitter device port 1 and receiver device port 2 are internal and are not defined.

Port definitions for loads used for signal output testing and S-parameter measurements in multiline configurations:



This load has ideal differential and common mode properties

Figure E.14 — S-parameter port naming conventions

E.11.3 Use of single-ended instrumentation in differential applications

There are four categories of S-parameters for a differential system:

a) S_{DDij}: differential stimulus, differential response;
b) S_{CDij}: differential stimulus, common-mode response (i.e., mode conversion causing emissions);
c) S_{DCij}: common-mode stimulus, differential response (i.e., mode conversion causing susceptibility); and
d) S_{CCij}: common-mode stimulus, common-mode response.

Figure E.15 shows the connections that are made to a four port VNA or TDNA for measuring S-parameters on a four single-ended port black box device.

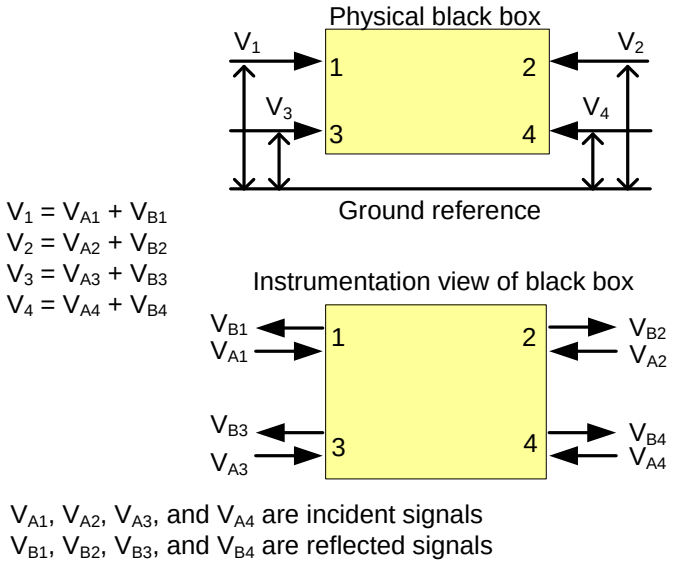
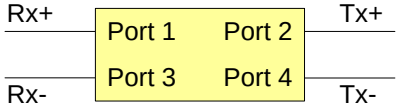


Figure E.15 — Four single-ended port or two differential port element

Since VNA ports are all single-ended, the differential and common-mode properties for differential ports are calculated internal to the VNA or are mathematically derived. If using a TDNA, consult the details for the specific instrument. Four analyzer ports are needed to measure the properties of two differential ports.

Figure E.16 shows the set of S-parameters for a single-ended system and for a differential system.

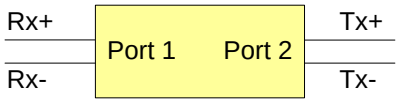
Single-ended



S-parameters:

		Stimulus	
Response			
		S_{11} S_{12} S_{13} S_{14}	
		S_{21} S_{22} S_{23} S_{24}	
		S_{31} S_{32} S_{33} S_{34}	
		S_{41} S_{42} S_{43} S_{44}	

Differential



S-parameters:

		Stimulus	
		Differential	Common-mode
Response	Differential	S_{DD11} S_{DD12} S_{DD21} S_{DD22}	S_{DC11} S_{DC12} S_{DC21} S_{DC22}
	Common-mode	S_{CD11} S_{CD12} S_{CD21} S_{CD22}	S_{CC11} S_{CC12} S_{CC21} S_{CC22}

Converting single-ended to mixed-mode:

$$S_{mm} = 0.5 \times \begin{bmatrix} S_{11} - S_{13} - S_{31} - S_{33} & S_{12} - S_{14} - S_{32} - S_{34} & S_{11} - S_{13} - S_{31} - S_{33} & S_{12} - S_{14} - S_{32} - S_{34} \\ S_{21} - S_{23} - S_{41} - S_{43} & S_{22} - S_{24} - S_{42} - S_{44} & S_{21} - S_{23} - S_{41} - S_{43} & S_{22} - S_{24} - S_{42} - S_{44} \\ S_{11} - S_{13} - S_{31} - S_{33} & S_{12} - S_{14} - S_{32} - S_{34} & S_{11} - S_{13} - S_{31} - S_{33} & S_{12} - S_{14} - S_{32} - S_{34} \\ S_{21} - S_{23} - S_{41} - S_{43} & S_{22} - S_{24} - S_{42} - S_{44} & S_{21} - S_{23} - S_{41} - S_{43} & S_{22} - S_{24} - S_{42} - S_{44} \end{bmatrix}$$

S_{DD11} S_{DC11} S_{CD11} S_{CC11}

Figure E.16 — S-parameters for single-ended and differential systems

See SFF-8416 for details on differential S-parameter measurements.

E.11.4 Measurement configurations for physical link elements

E.11.4.1 Measurement configuration overview

Special test fixtures are needed to make S-parameter measurements partly because the connectors used on real physical link elements are different from those used on instrumentation. The goal is for these test fixtures to be as invisible as possible.

All of the measurements in this annex are of S_{11} or S_{22}. A more complete set of S-parameters is used as part of the calibration process for test fixtures.

E.11.4.2 Transmitter device S_{22} measurements

Figure E.17 shows the configuration to be used for the transmitter device S_{22} measurements.

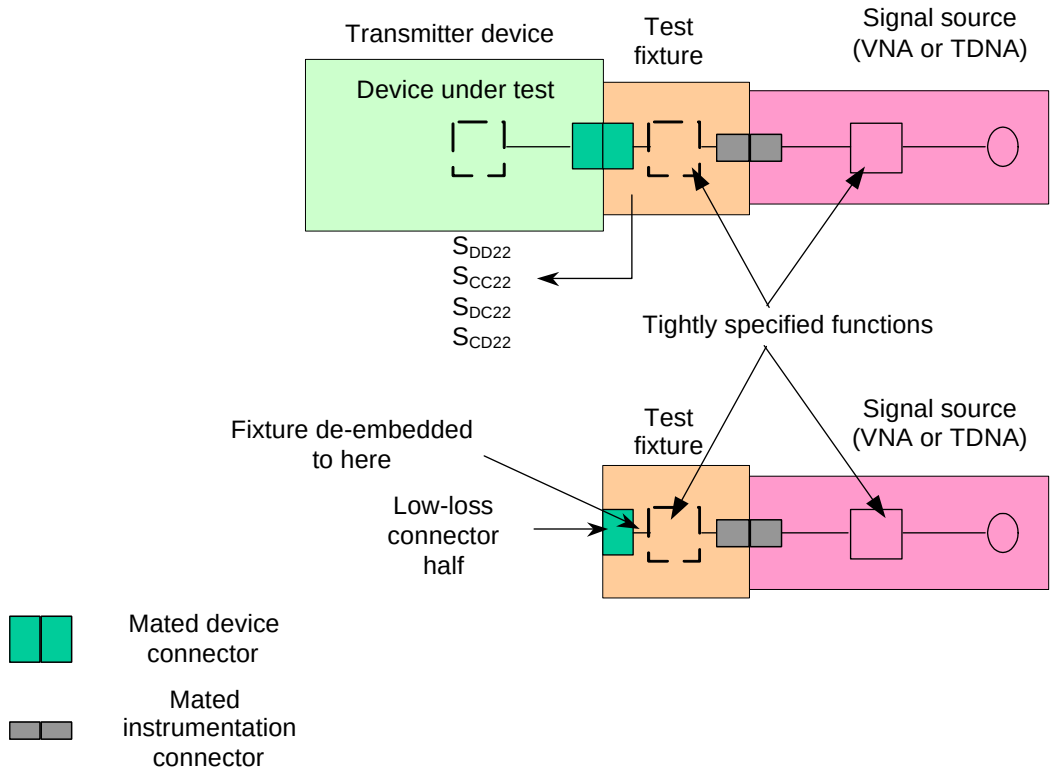


Figure E.17 — Measurement conditions for S_{22} at the transmitter device connector

The test fixture in figure E.17 uses low loss connectors to avoid penalizing the transmitter device under test for the test fixture half of the connector.

The test fixture losses up to the mounting points for the device connector are de-embedded using the methods described in figure E.4.

E.11.4.3 Receiver device S_{11} measurements

Figure E.18 shows the configuration to be used for the receiver device S_{11} measurements.

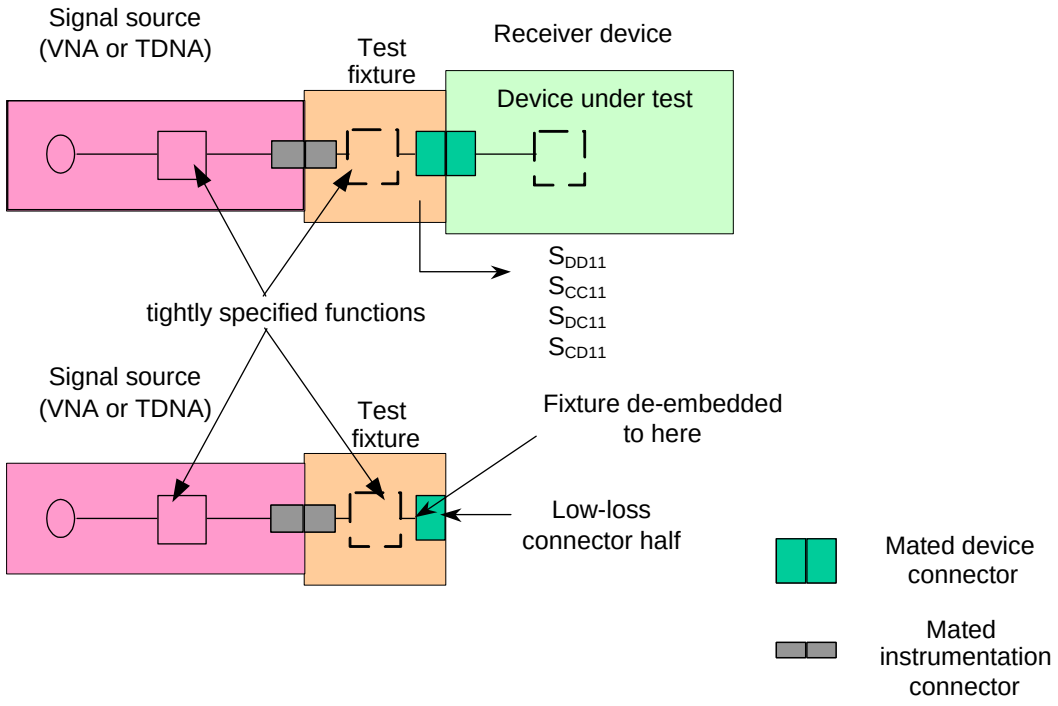


Figure E.18 — Measurement conditions for S_{11} at the receiver device connector

The test fixture in figure E.18 uses low loss connectors to avoid penalizing the receiver device under test for the test fixture half of the connector.

The test fixture losses up to the mounting points for the device connector are de-embedded using the methods described in figure E.4.

E.11.4.4 TxRx connection S_{11} measurements at IT or CT

Figure E.19 shows the conditions for making S_{11} measurements of the interconnect attached to the transmitter device.

This measurement, like the signal tolerance measurement at the transmitter device connector, has both the interconnect and the receiver device in place when the combination is measured. If the receiver device is replaced by an ideal load, then S_{11} does not represent in-service conditions. If the interconnect is very lossy, then the effects of the load on the far end (i.e., where the receiver device is located) are not significant and an ideal load may be used. However, if the interconnect is not very lossy (e.g., the zero length test load), then the measured S_{11} may be dominated by the properties of the receiver device and not the properties of the interconnect.

For short physical links, S_{11} performance may be the limiting factor for the entire physical link due to severe unattenuated reflections that create large DJ.

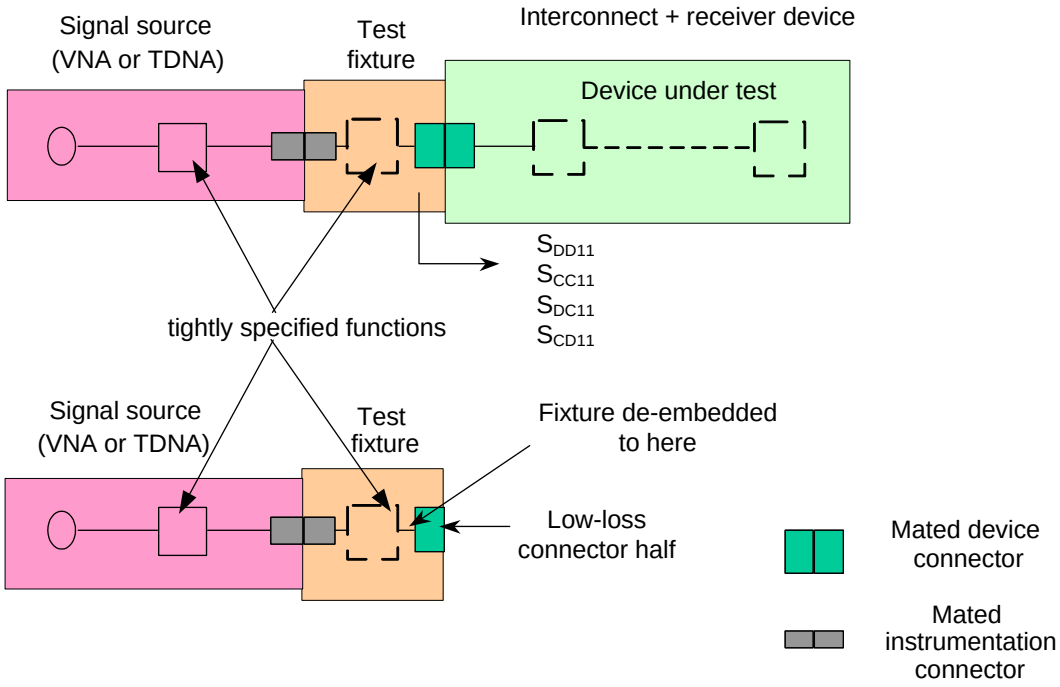


Figure E.19 — Measurement conditions for S_{11} at IT or CT

E.11.4.5 TxRx connection S_{22} measurements at IR or CR

Figure E.20 shows the conditions for making S_{22} measurements of the interconnect attached to the receiver device.

This measurement has both the interconnect and the transmitter device in place when the combination is measured. This may be considered a reverse direction signal tolerance measurement. If the transmitter device is replaced by an ideal load, then S_{22} does not represent in-service conditions. If the interconnect is very lossy, then the effects of the load on the far end (i.e., where the transmitter device is located) are not significant and an ideal load may be used. However, if the interconnect is not very lossy (e.g., the zero length test load), then the measured S_{22} may be dominated by the properties of the transmitter device and not the properties of the interconnect.

For short physical links, S_{22} may be the limiting factor for the entire physical link due to severe unattenuated reflections that create large DJ.

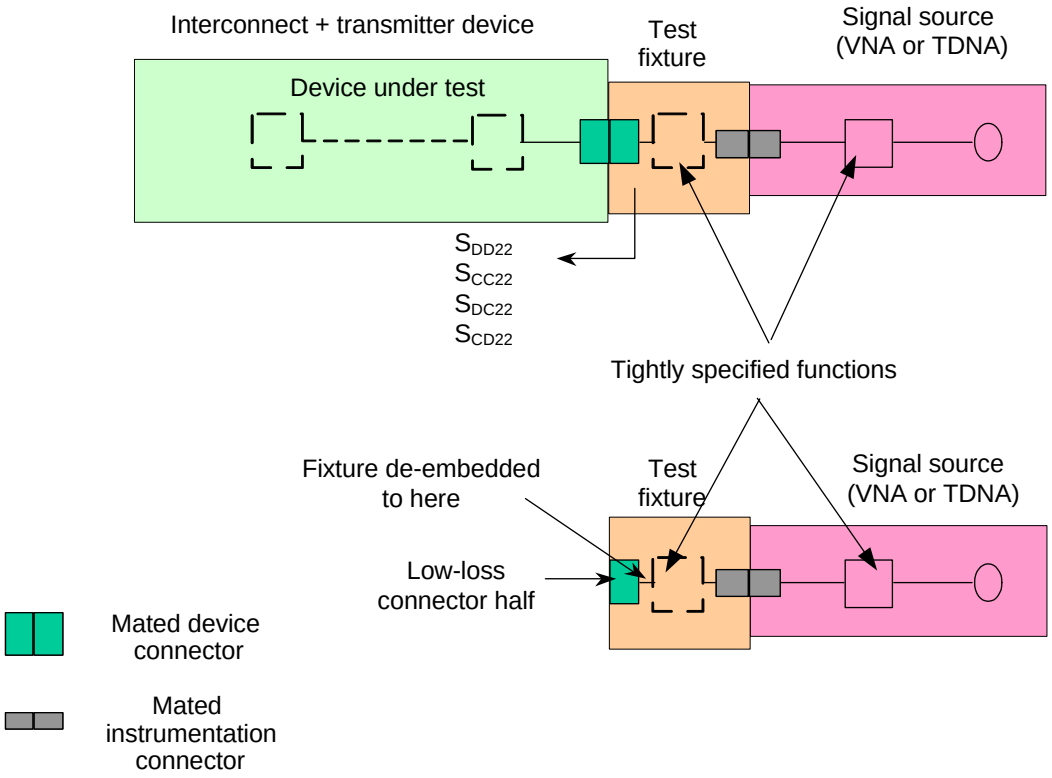


Figure E.20 — Measurement conditions for S_{22} at IR or CR

E.12 Calibration of JMDs

E.12.1 Calibration of JMDs overview

E.12.1.1 Purpose of JMD calibration

The response of a JMD to known jitter levels is calibrated and verified in two frequency bands:

a) the lower frequency band; and
b) the frequency band around the -3 dB frequency and the peak frequency of the JTF.

By calibrating the JMD to these two bands, the response to jitter is calibrated and allows for improved correlation among JMDs.

The test sequence for all measurements removes the baseline DJ, the DJ of the source, and the DJ of the JMD so that the measurement only reports the added test jitter.

E.12.1.2 Overview of low frequency calibration for SSC configurations

For configurations supporting SSC, the lower frequency band requirement is tested with a repeating 0011b or 1100b pattern (e.g., D24.3) on which a sinusoidal phase modulation of 30 kHz ± 1 % is added. The amplitude of this modulation is 20.83 ns peak-to-peak. The ratio of the reported jitter to the amount applied is the attenuation (see 5.9.3.2).

This calibration procedure ensures that the measurement equipment responds properly to the fundamental characteristics of the JTF.

For any SSC modulation, there are three important characteristics that affect the response of the JMD and the ability to generate jitter:

a) the peak-to-peak phase excursion experienced through an SSC cycle;
b) the extreme instantaneous frequency modulation; and
c) the extreme instantaneous frequency modulation rate.

The peak-to-peak phase excursion experienced through an SSC cycle is an important parameter for jitter generating equipment.

The extreme instantaneous frequency modulation stresses the ability of the JMD to track large frequency modulation. All systems have practical limitations beyond which the response changes shape (e.g. the system response becomes 20 dB/decade instead of 40 dB/decade). The amplitude of the peak-to-peak frequency modulation under which the JMD maintains a 40 dB/decade response indicates the JMD's limitation to behave as a linear system.

The extreme instantaneous frequency modulation rate (e.g., the minimal negative and maximal positive) stresses the ability of the JMD to respond with the 40 dB/decade low frequency JTF slope specified by this standard. The remaining jitter, after being filtered by the JTF, is proportional to the extreme ffrequency modulation rate. The maximal amount of remaining jitter a JMD reports is a direct indication of its linear performance in the expected 40 dB/decade response region.

An example of an SSC profile is a balanced triangular SSC waveform (e.g., ± 2 300 ppm).

In this calibration procedure, a sinusoidal phase modulation is applied. Even though this modulation is defined as a phase modulation, its variation in time makes it equivalent to a frequency modulation having comparable characteristics to that of a triangular SSC profile.

The triangular SSC profile is defined by the following equations:

for $k/f_m \le t < (k+0.5)/f_m$:

$$\Delta f(t) = f_{baud} \times mod\_max \times (-1 + modulo(t,1/f_m) \times f_m \times 4) \text{ Hz}$$

and for $(k+0.5)/f_m \le t < (k+1)/f_m$:

$$\Delta f(t) = f_{baud} \times mod\_max \times (3 - modulo(t,1/f_m) \times f_m \times 4) \text{ Hz}$$

where:

$\Delta f(t)$	is the frequency deviation in Hz;
f_{baud}	is the baud rate (e.g., 6 GHz for 6 Gbps) (see 5.9.1);
mod_max	is the peak excursion of the frequency modulation as a ratio of the current baud rate (e.g., 2.3×10^{-3} for a ± 2 300 ppm modulation);
modulo(t,1/f_m)	modulo operator, the result is x modulo y and limited to range [0,y];
f_m	is the modulation frequency in Hz; and
k	is an integer.

The bit transitions are expected to happen for t where the following equation reaches any integer value m:

$$(f_{baud} + \Delta f(t)) \times t = m$$

where the characteristics for this pattern are:

a) peak-to-peak phase excursion = $2 \times \pi \times mod\_max \times f_{baud} / (4 \times f_m)$ radians (or peak-to-peak time excursion = $mod\_max / (4 \times f_m)$ seconds);
b) extreme instantaneous frequency modulation = $\pm\ mod\_max \times f_{baud}$ Hz; and
c) extreme instantaneous frequency modulation rate = $\pm\ 4 \times mod\_max \times f_m \times f_{baud}$ Hz/s (or $\pm\ 4 \times mod\_max \times f_m$ ppm/µs

A sinusoidal phase modulation is defined by:

$$PJ(t) = A_{ppu}/2 \times \sin(2 \times \pi \times f_{ms} \times t) \text{ UI}$$

where:

A_{ppu} is the peak-to-peak modulation in UI; and

f_{ms} is the frequency of the phase modulation in Hz.

This is equivalent to A_{pps}, the peak-to-peak time modulation in seconds, knowing that

$$A_{pps} = A_{ppu}/f_{baud}$$

The bit transitions are expected to happen for t where the following equation reaches any integer value n:

$$f_{baud} \times t + PJ(t) = n$$

where the characteristics for this pattern are:

a) peak-to-peak phase excursion = $2 \times \pi \times A_{pps} \times f_{baud}$ radians (or Appu UI);
b) extreme instantaneous frequency modulation = $\pm \pi \times A_{pps} \times f_{baud} \times f_{ms}$ Hz; and
c) extreme instantaneous frequency modulation rate = $\pm 2 \times (\pi \times f_{ms})^2 \times A_{pps} \times f_{baud}$ Hz/s (or $\pm 2 \times (\pi \times f_{ms})^2 \times A_{pps}$ ppm/µs).

The JMD calibration procedure uses sinusoidal phase modulation where:

a) A_{pps} = 20.83 ns; and
b) f_{ms} = 30 kHz.

By comparing the equations of the characteristics, it is possible to compute the parameters of the equivalent triangular SSC profile to the prescribed sinusoidal phase modulation. Defining that $f_m = f_{ms}$ = 30 kHz:

a) the equivalent peak-to-peak phase excursion of the sinusoidal phase modulation (i.e., 20.83 ns) corresponds to a triangular SSC profile having a mod_max parameter of ± 2 500 ppm;
b) the equivalent extreme instantaneous frequency modulation of the sinusoidal phase modulation (i.e., 11.78 UI/µs) to a triangular SSC profile having a mod_max parameter of ±1 963 ppm; and
c) the equivalent extreme instantaneous frequency modulation rate of the sinusoidal phase modulation (i.e., 370 ppm/µs) corresponds to a triangular SSC profile having a mod_max parameter of ± 3 084ppm.

As a result, using a sinusoidal jitter with a 20.83 ns peak-to-peak excursion at 30 kHz produces a modulation with fundamental parameters balanced around the specified maximal ± 2 300 ppm amplitude of the SSC profile at a modulation rate of 30 kHz.

E.12.1.3 Overview of low frequency calibration for non-SSC configurations

For configurations not supporting SSC, the lower frequency band requirement is tested with a repeating 0011b or 1100b pattern (e.g., D24.3) at the desired baud rate on which sinusoidal phase modulation is added. The ratio of the jitter applied to the jitter reported is the attenuation.

Unlike the SSC supported cases, there is no specific frequency defined for this measurement. It is recommended to verify the attenuate using PJ at a frequency 10 times below the -3 dB frequency (e.g., 90 kHz for 1.5 Gbps, 180 kHz for 3 Gbps, or 360 kHz for 6 Gbps). The phase modulation amplitude used for these tests is calibrated to be 3 UI peak-to-peak at the current baud rate, which is 20 dB more than the 0.3 UI used at high frequency (see E.12.1.4).

E.12.1.4 High frequency Calibration

The calibration described in this subclause applies for all configurations, independent of SSC support.

To do a high frequency calibration two tests are performed in the higher frequency band:

a) adjustment of the -3 dB bandwidth of the JTF; and
b) verification of the peaking (see 5.9.3.2).

Both of these tests use a repeating 0011b or 1100b pattern (e.g., D24.3) with sinusoidal periodic phase modulation or PJ that has been independently verified to produce 0.3 UI ± 10 % peak-to-peak at the baud rate being tested over a frequency range of 0.5 MHz to 50 MHz. This corresponds to the values in table E.1.

Table E.1 — High frequency jitter source amplitudes

Baud rate (Gbps)	Peak-to-peak jitter for high frequency test (ps)	Tolerance (ps)	Range (MHz)
1.5	200	± 20	0.5 to 50
3	100	± 10	0.5 to 50
6	50	± 5	0.5 to 50

The programmed source PJ level may vary over the frequency range in order to keep the generated PJ at 0.3 UI ± 10 %.

There are two typical JMD adjustments for clock recovery:

a) loop bandwidth; and
b) peaking (i.e., damping).

These adjustments may refer to the closed loop response or be specific to a particular design, so they may not be used directly to ensure the JTF response to jitter. The loop bandwidth is initially adjusted with the peaking fixed. If both the low frequency band requirements and the high frequency band requirements are not able to be simultaneously met, then the peaking is adjusted to modify the JTF shape in the upper band. In the case of hardware based reference clocks, moderate levels of peaking may be needed to achieve the proper attenuation at 30 kHz. The peaking setting is usually specific to the JMD. With software based clock recovery, the suggested starting peaking level may be low, close to the critically damped condition of peaking of 0.707.

E.12.2 TJMD calibration procedure

E.12.2.1 General characteristics and equipment

This calibration procedure is based on the JTF characteristics defined in 5.9.3.2 for:

a) the -3 dB corner frequency of the JTF;
b) the magnitude peaking of the JTF;
c) the attenuation at 30 kHz when SSC is supported; and
d) the low frequency attenuation when SSC is not supported.

The required JMD calibration equipment for configurations supporting SSC is as follows:

a) a pattern generator for SAS signals;
b) a sine wave source of 30 kHz;
c) test cables; and
d) a JMD.

The JMD calibration equipment is as follows:

a) a pattern generator for SAS signals;
b) a sine wave source covering the range from 90 kHz to 360 kHz;
c) a sine wave source covering the range from 0.5 MHz to 50 MHz;
d) test cables; and
e) a JMD.

The response to jitter of the JMD is measured with three different jitter modulation frequencies corresponding to the three cases:

a) low frequency jitter (i.e., the JMD fully tracks);
b) high-frequency jitter (i.e., the JMD does not track); and
c) the boundary between low-frequency jitter and high-frequency jitter.

The jitter source is independently verified by separate means to ensure that the jitter response of the JMD is reproducible across different test setups.

The JMD calibration pattern is a square wave at 0.25 × f_{baud} ± 0.01 % (i.e., a repeating 0011b or 1100b pattern (e.g., D24.3)) with rise time longer than 0.25 UI 20 % to 80 %.

When testing 6 Gbps, a repeating 0011b or 1100b pattern (e.g., D24.3) at 6 Gbps is used. When testing 3 Gbps or 1.5 Gbps, the same pattern is used, but at 3 Gbps or 1.5 Gbps, respectively. This applies to all jitter frequencies.

An independent, separate means of verification of the JMD calibration pattern is used to ensure that the level of the modulation is correct.

E.12.2.2 Calibration of the JMD for testing SSC configurations

This procedure checks the JTF attenuation and the JTF bandwidth for testing configurations with training and SSC support.

The following test procedure is performed for each baud rate tested (e.g., 1.5 Gbps, 3 Gbps, and 6 Gbps as applicable):

1) set the pattern generator to output the JMD calibration pattern with a sinusoidal phase modulation of 20.8 ns ± 10 % peak to peak at 30 kHz ± 1 %;
2) verify the level of modulation meets the requirements and record the peak-to-peak level as DJ_SSC (e.g., the independent, separate means of verification of the 30 kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator) measured with:
   A) a time interval error plot with constant frequency clock on a real time oscilloscope;
   B) an equivalent time oscilloscope; or
   C) a frequency demodulator;
3) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_SSCOFF;
4) turn on the sinusoidal phase modulation. Record the reported DJ as DJ_SSCON;
5) calculate and record the reported DJ as DJ_MSSC by subtracting the DJ with modulation off from DJ with modulation on (i.e., DJ_MSSC = DJ_SSCON - DJ_SSCOFF), calculate the jitter attenuation by 20 × $\log_{10}$(DJ_MSSC / DJ_SSC), adjust the JMD settings so the value falls within the range specified in 5.9.3.2 for the selected baud rate;
6) set the pattern generator to output the JMD calibration pattern with sinusoidal phase modulation of 0.3 UI ± 10 % peak to peak over a frequency range of 0.5 MHz to 50 MHz for the selected baud rate (see table E.1);
7) verify the level of modulation meets the requirements and record the peak-to-peak level as DJ_M (e.g., the independent verification of the 50 MHz test signal is a jitter measurement by separate means from the JMD under calibration) measured with:
   A) a time interval error plot with constant frequency clock on a real time oscilloscope;
   B) an equivalent time oscilloscope with histogram and constant frequency clock;
   C) a bit error rate tester (BERT) using a constant frequency clock; or
   D) a spectral analysis with the Bessel expansion of angle modulated sidebands;
8) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_MOFF;
9) turn on the sinusoidal phase modulation, record the reported DJ as DJ_MON;
10) calculate the following:
   A) the difference in reported DJ (i.e., DJ_MM = DJ_MON - DJ_MOFF); and
   B) the -3 dB value (i.e., DJ_3DB = DJ_MM × 0.707);
11) adjust the frequency of the PJ source to the specified -3 dB frequency for the baud rate being tested per table 32 (5.9.3.2), measure the reported DJ difference between PJ on versus PJ off (i.e., DJ = DJ_ON - DJ_OFF) and compare DJ to DJ_3DB. Shift the frequency of the PJ source until the reported DJ difference between PJ on and PJ off is equal to DJ_3DB. The PJ frequency is the -3 dB bandwidth of the JTF, record this value as F_3DB;
12) adjust the JMD settings to bring F_3DB to the corner frequency specified in table 32 (5.9.3.2) or the baud rate being tested;

13) repeat steps 4) through 12) until both the jitter attenuation and -3 dB frequency are in the acceptable ranges;
14) check the peaking of the JTF, set the pattern generator to output the JMD calibration pattern with sinusoidal phase modulation of 0.3 ± 10 % UI peak-to-peak at F_3DB, increase the frequency of the modulation to find the maximum reported DJ (i.e., it is not necessary to increase beyond 20 MHz), measure the reported DJ difference between PJ on versus PJ off as DJ_PK = DJ_PKON - DJ_PKOFF; and
15) calculate the JTF Peaking value: $20 \times \log_{10}$ (DJ_PK / DJ_MM), verify that the peaking is below the limits set in 5.9.3.2, if peaking is above the limits repeat the procedure until all specifications are met.

E.12.2.3 Calibration of the JMD for testing non-SSC configurations

This test procedure verifies the JTF attenuation and the JTF bandwidth for SAS devices that:

a) support training with no SSC support; or
b) do not support training.

This procedure is performed for each baud rate tested (e.g., 1.5 Gbps, 3 Gbps, and 6 Gbps as applicable):

1) set the pattern generator to output the JMD calibration pattern with a sinusoidal phase modulation of 1.5 UI ± 10 % peak-to-peak at f_{baud}/33.333 kHz (see table E.2);
2) verify the level of modulation meets the requirements and record the peak-to-peak level as DJ_LF (e.g., the independent, separate means of verification of the low frequency test signal is equivalent to a frequency demodulator or wide range phase demodulator), measured with:
   A) continuously gated frequency counter;
   B) a time interval error plot with constant frequency clock on a real time oscilloscope;
   C) an equivalent time oscilloscope; or
   D) a frequency demodulator;
3) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_LFOFF;
4) turn on the sinusoidal phase modulation, record the reported DJ as DJ_LFON;
5) calculate and record the reported DJ as DJ_MLF by subtracting the DJ with modulation off from DJ with modulation on (i.e., DJ_MLF = DJ_LFON - DJ_LFOFF), calculate the jitter attenuation by $20 \times \log_{10}$ (DJ_MLF / DJ_LF), adjust the JMD settings so the attenuation value falls within the range specified in table E.3; and
6) continue with the high frequency tests of the corner frequency and peaking by following steps 6 through 15 of in D.10.2.2, repeat the this procedure until all specifications are met.

Table E.2 — Low frequency jitter source calibration amplitudes

Baud rate (Gbps)	Phase modulation frequency (kHz)	Peak-to-peak modulation (UI)	Peak-to-peak modulation (ns)	Modulation tolerance
1.5	45	1.5	1.0	± 0.15
3	90	1.5	0.5	± 0.15
6	180	1.5	0.25	± 0.15

Table E.3 — Low frequency jitter attenuation targets

Baud rate (Gbps)	Phase modulation frequency (kHz)	Peak-to-peak modulation (UI)	Target attenuation (dB) [a] [b]	Target attenuation tolerance (dB)
1.5	45	1.5	26	± 1.5
3	90	1.5	26	± 1.5
6	180	1.5	26	± 1.5

[a] Target Attenuation = $20 \times \log_{10} ((f / fc) / (1+ (f / fc)^{2})^{0.5})$, where fc is the -3 dB frequency.
[b] This is derived from a nominal first-order frequency response.

Annex F
(informative)

Description of the included Touchstone models

F.1 Description of the included Touchstone models overview

Touchstone models are included with this standard to represent:

a) reference transmitter device termination (see 5.9.4.6.5 and F.2);
b) reference receiver device termination (see 5.9.5.7.3 and F.3); and
c) reference transmitter test load (see 5.7.5 and F.5).

Figure F.1 shows the circuit models used to create the Touchstone models of reference transmitter device termination and reference receiver device termination.

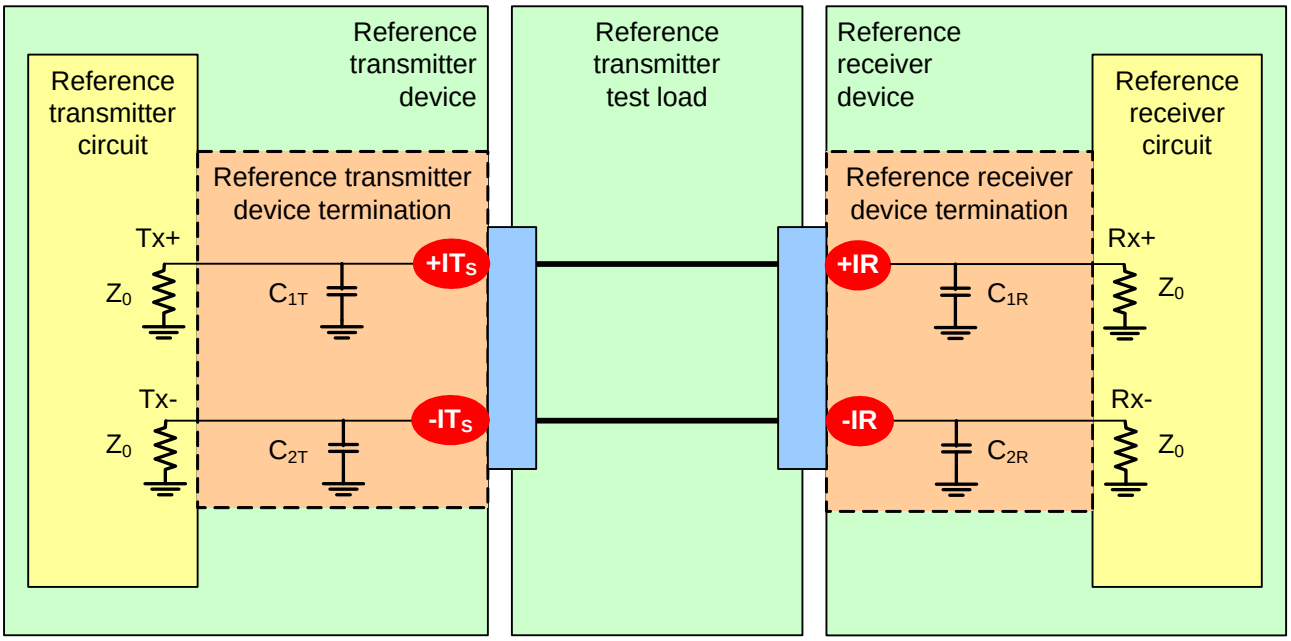


Figure F.1 — Reference transmitter device and reference receiver device termination circuit model

F.2 Reference transmitter device termination model

From the circuit model shown in figure F.1 (see F.1), the S-parameters of the reference transmitter device termination were derived using the following calculations:

$$\tau_1 = \frac{Z_0 \times C_{1T}}{2}$$

$$\tau_2 = \frac{Z_0 \times C_{2T}}{2}$$

$$S_{11} = \frac{-s \times \tau_1}{1 + (s \times \tau_1)}$$

$$S_{12} = 0$$

$$S_{22} = \frac{-s \times \tau_2}{1 + (s \times \tau_2)}$$

$$S_{DDij} = S_{CCij} = \frac{S_{11} + S_{22}}{2}$$

$$S_{CDij} = S_{DCij} = \frac{S_{11} - S_{22}}{2}$$

where:

τ_1	is the Tx+ termination time constant;
τ_2	is the Tx- termination time constant;
Z_0	is the impedance as specified by this standard (i.e., 50 ohm);
C_{1T}	is the Tx+ termination capacitance; and
C_{2T}	is the Tx- termination capacitance.

Figure 124 (see 5.9.4.6.5) shows the graph of the S-parameters based on the following values:

a) Z_0 is set to 50 ohm;
b) C_{1T} is set to 0.5 pF, so τ_1 becomes 12.5 ps; and
c) C_{2T} is set to 2 pF, so τ_2 becomes 50 ps.

F.3 Reference receiver device termination model

From the circuit model shown in figure F.1 (see F.1), the S-parameters of the reference receiver device termination were derived using the following calculations:

$$\tau_1 = \frac{Z_0 \times C_{1R}}{2}$$

$$\tau_2 = \frac{Z_0 \times C_{2R}}{2}$$

$$S_{11} = \frac{-s \times \tau_1}{1 + (s \times \tau_1)}$$

$$S_{12} = 0$$

$$S_{22} = \frac{-s \times \tau_2}{1 + (s \times \tau_2)}$$

$$S_{DDij} = S_{CCij} = \frac{S_{11} + S_{22}}{2}$$

$$S_{CDij} = S_{DCij} = \frac{S_{11} - S_{22}}{2}$$

where:

τ_1 is the Rx+ termination time constant;

τ_2 is the Rx- termination time constant;

Z_0 is the impedance as specified by this standard (i.e., 50 ohm);

C_{1R} is the Rx+ termination capacitance; and

C_{2R} is the Rx- termination capacitance.

Figure 137 (see 5.9.5.7.3) shows the graph of the S-parameters based on the following values:

a) Z_0 is set to 50 ohm;
b) C_{1R} is set to 2 pF, so τ_1 becomes 50 ps; and
c) C_{2R} is set to 0.5 pF, so τ_2 becomes 12.5 ps.

F.4 Generic return loss circuit model

Figure F.2 shows a generic circuit model for return loss, upon which the circuit models for transmitter device termination in F.2 and receiver device termination in F.3 are based.

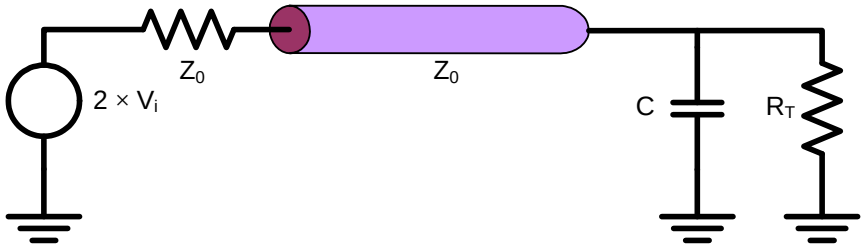


Figure F.2 — Generic return loss circuit model

$|S_{11}|$ (i.e., negative return loss) may be derived by defining points on a curve using the following calculations:

$$LF = 20 \times \log_{10}\left(\frac{tol}{2 + tol}\right)$$

$$R_T = Z_0 \times (1 + tol)$$

$$F_{zero} = \frac{tol}{(2 \times \pi \times R_T \times C \times (1 + tol))}$$

$$F_{pole} = \frac{2 + tol}{(2 \times \pi \times R_T \times C \times (1 + tol))}$$

where:

LF is the low frequency asymptote of $|S_{11}|$;

tol is the tolerance of R_T;

Z_0 is the impedance specified by this standard (i.e., 50 ohm);

R_T is the far end load;

C is the far end capacitance;

F_{zero} is the frequency at which a 20 dB/decade asymptote intersects the LF asymptote; and

F_{pole} is the frequency at which a 20 dB/decade asymptote intersects the 0 dB asymptote.

Because the effects of the far end load are not significant, the equations may be simplified as follows:

$$LF \sim 20 \times \log_{10}\left(\frac{tol}{2}\right)$$

$$F_{zero} \sim \frac{tol}{(2 \times \pi \times R_T \times C)}$$

$$F_{pole} \sim \frac{1}{(\pi \times R_T \times C)}$$

Using the simplified equations, $|S_{11}|$ may be derived from LF, F_{zero}, and F_{pole} as shown in figure F.3.

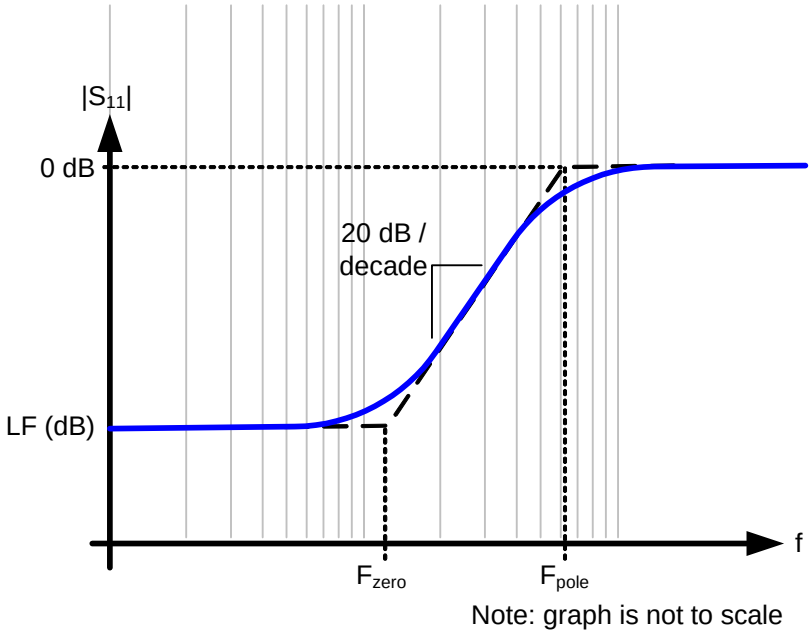


Figure F.3 — Generic return loss model $|S_{11}|$

F.5 Reference transmitter test load

The Touchstone model of the reference transmitter test load (see 5.7.5) is based on physical measurements.

The following components of a TxRx connection were measured:

a) an etch length of 50.8 mm with an etch width of 177.8 µm between IT_S (see 5.3.6.5.4) and the Mini SAS 4x cable plug in a Nelco® 4000-13 material environment. This etch is part of the transmitter device;
b) a 10 m Mini SAS 4x cable assembly using 24 AWG solid wire from pin B5 to pin A5 and from pin B6 to pin A6 (see 5.5.3.4.1.3); and
c) an etch length of 50.8 mm with an etch width of 177.8 µm between IR (see 5.3.7.4.3) and the Mini SAS 4x cable plug in a Nelco® 4000-13 material environment. This etch is part of the receiver device.

NOTE 29 - Nelco® 4000-13 material is a product supplied by Park Electrochemical Corporation. This information is given for the convenience of users of this standard and does not constitute an endorsement by ANSI or ISO. Equivalent products may be used if they lead to the same results.

Although the etches between the transmission points and probe points add extra loss to the TxRx connection, they are considered to be an acceptable amount of loss for simulation purposes.

The following list of equipment was used to perform the measurement:

a) Agilent N1957B Physical Layer Test System (PLTS), including:
   A) Agilent E8364B PNA Network Analyzer (10 MHz to 50 GHz);
   B) Agilent N4421B S-parameter Test Set (10 MHz to 50 GHz); and
   C) Agilent N1930B Physical Layer Test System Software version 3.01;

   and

b) Molex 26-circuit External iPass™ Test Fixture (PCB 73931-2540).

NOTE 30 - The Agilent Technologies® Corporation and Molex® equipment are examples of a suitable product(s) available commercially. iPass™ is a product supplied by Molex Incorporated. This information is given for the convenience of users of this standard and does not constitute an endorsement by ANSI or ISO of these products. Equivalent products may be used if they lead to the same results.

The equipment was interconnected as shown in figure F.4.

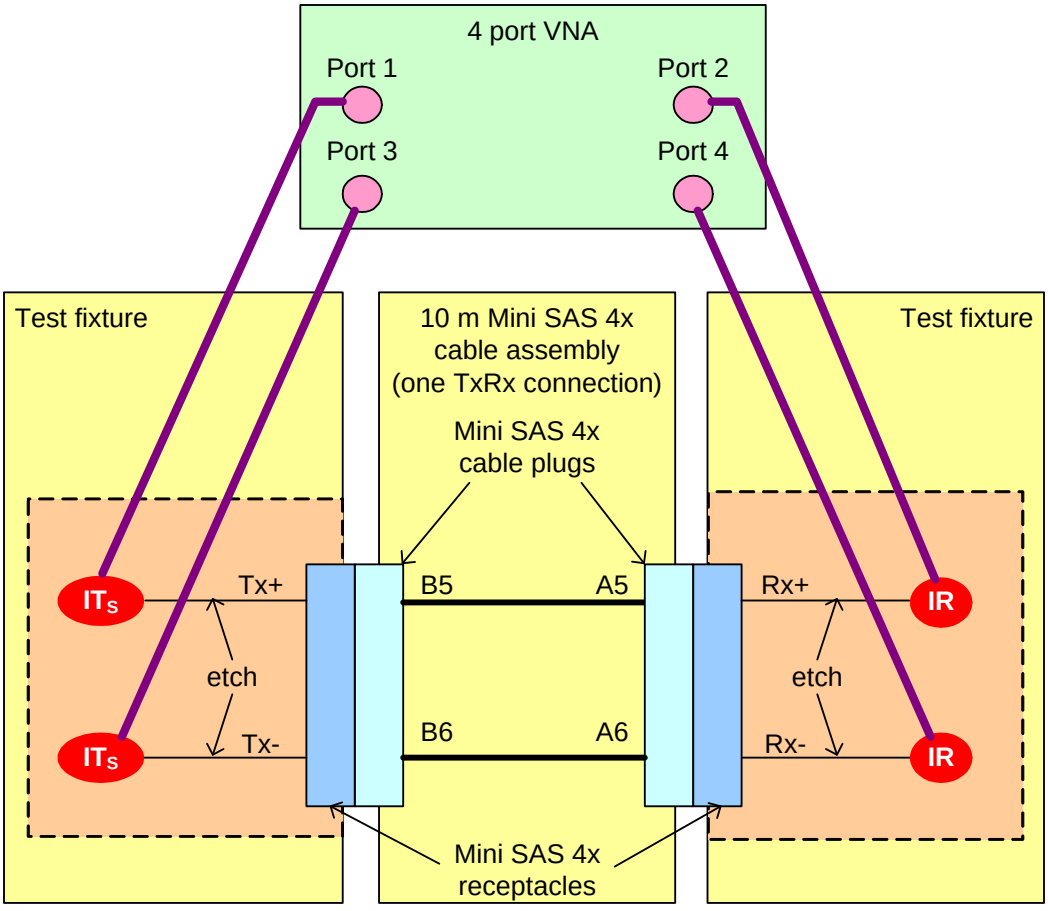


Figure F.4 — Reference transmitter test load measurement setup

The Short-Open-Load-Through (SOLT) calibration procedure should be run before generating the S-parameters.

Samples were taken from 10 MHz to 20 GHz in 1 MHz steps.

Figure 107 (see 5.7.5) shows the graph of the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

Figure F.5 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 20 GHz.

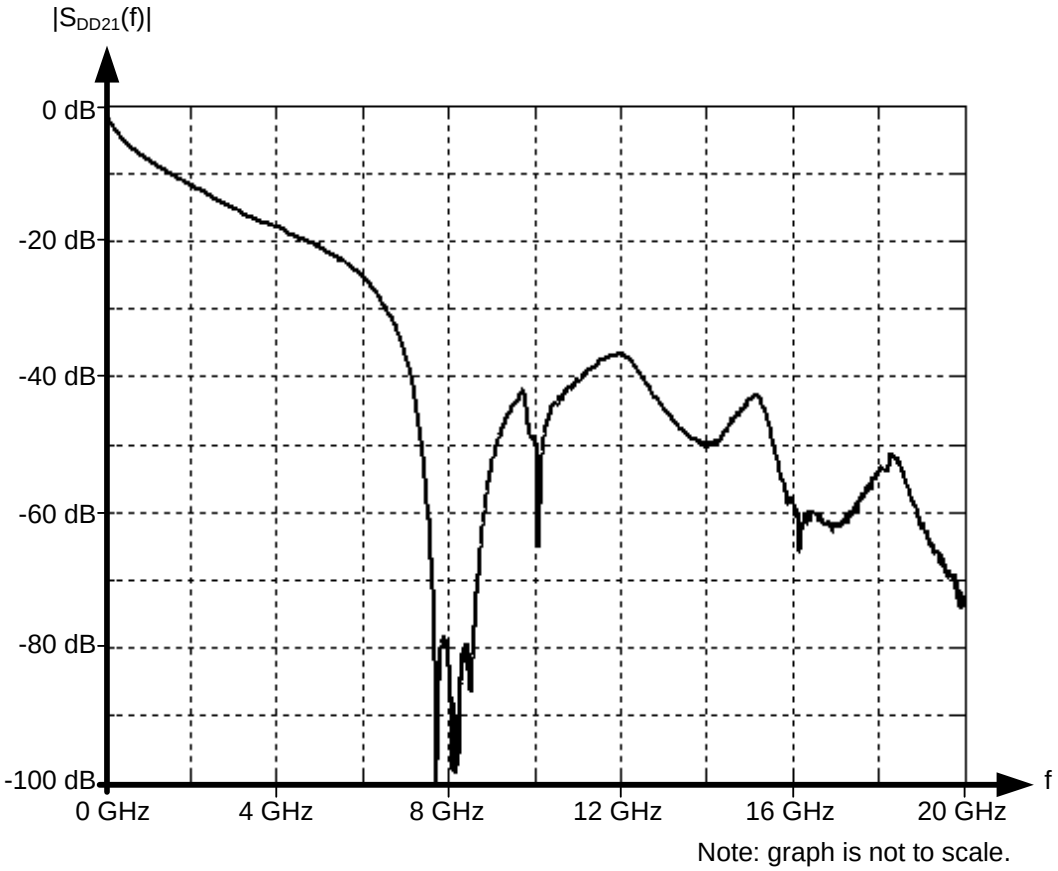


Figure F.5 — Reference transmitter test load $|S_{DD21}(f)|$ up to 20 GHz

Annex G
(informative)

Mini SAS 4x active cable assembly power supply and voltage detection circuitry

SAS devices and expander devices with Mini SAS 4x active receptacle connectors should operate with Mini SAS 4x passive cables which have the Vcc pin tied to ground. There should be a mechanism that turns on the power to the receptacle only when active cable assembly presence is detected to avoid shorting power to ground. A SENSE pin is provided (see 5.5.3.4.1.5) to detect if an active cable assembly is present. This pin may also be used to detect the status of a specific port or to implement other features within a switch device.

Figure G.1 is an example design utilizing a dual comparator to determine from the SENSE pin on the active cable assembly plug. If an active cable assembly is present, then the circuit supplies power to the receptacle upon detection of an active cable assembly. For proper function during hot plug, B1 and B13 should be mated to the Mini SAS 4x cable plug connector (see 5.5.3.4.1.1) simultaneously.

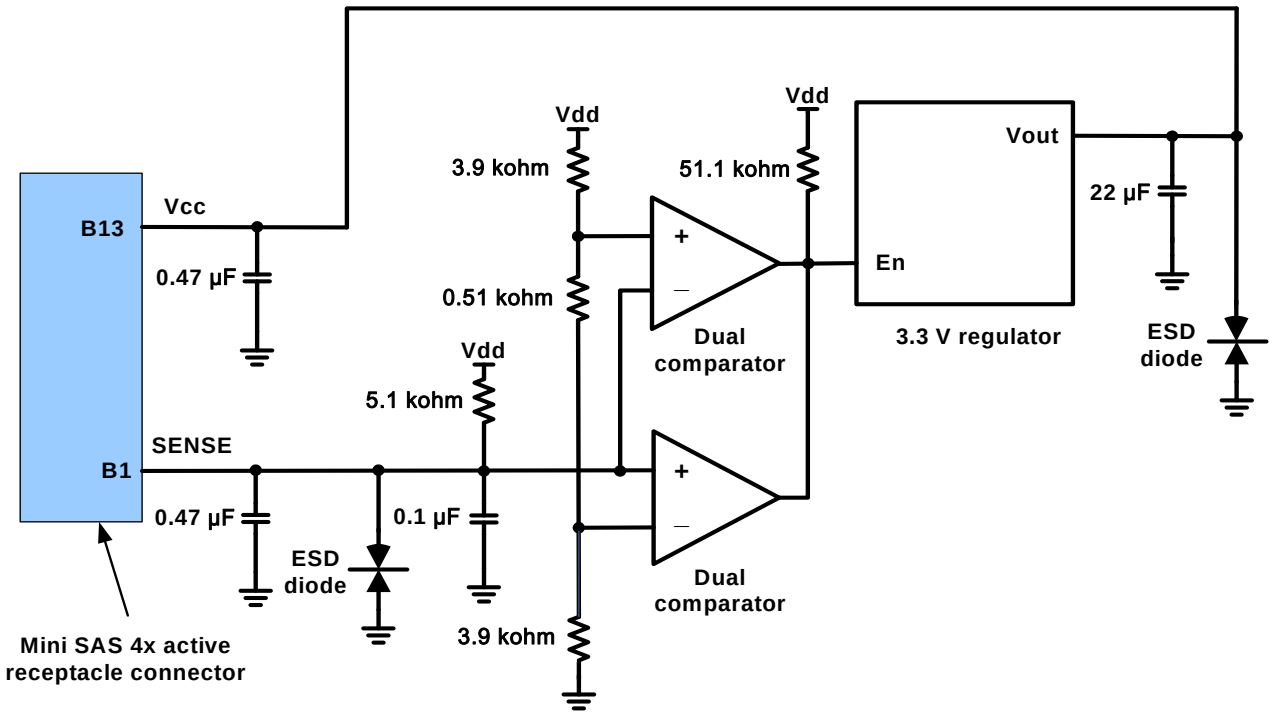


Figure G.1 — Dual comparator design for active cable assembly detection

The power supply characteristics are specified in table 20 (see 5.5.3.4.1.5). The type of power supply may either be a switching regulator or a linear regulator.

Annex H
(informative)

SAS icons

A SAS icon should be included on or near all connectors used by devices compliant with both this standard and SPL-2.

NOTE 31 - Contact the SCSI Trade Association (see http://www.scsita.org) for versions of the SAS icons in various graphics formats.

Figure H.1 shows the primary SAS icon.

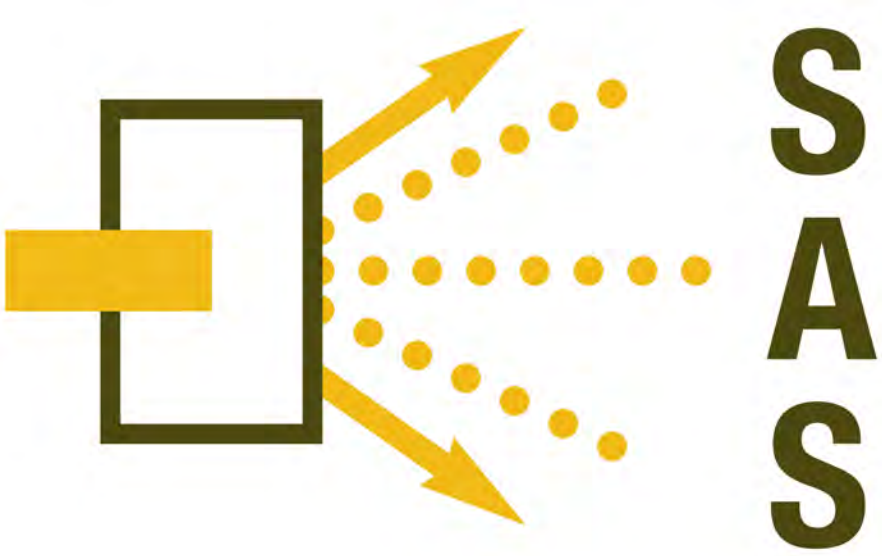


Figure H.1 — SAS primary icon

Figure H.2 shows an alternate SAS icon that may be used instead of the primary SAS icon when the area for the icon is small.

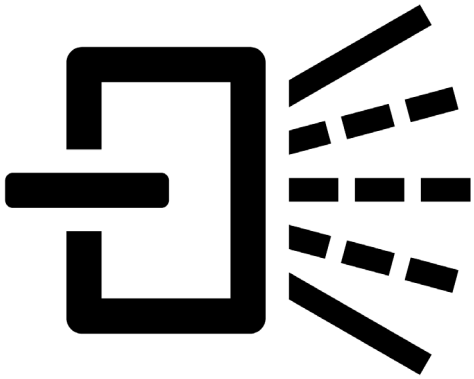


Figure H.2 — SAS alternate icon

Figure H.3 shows an alternate SAS icon with the SAS abbreviation letters alongside.

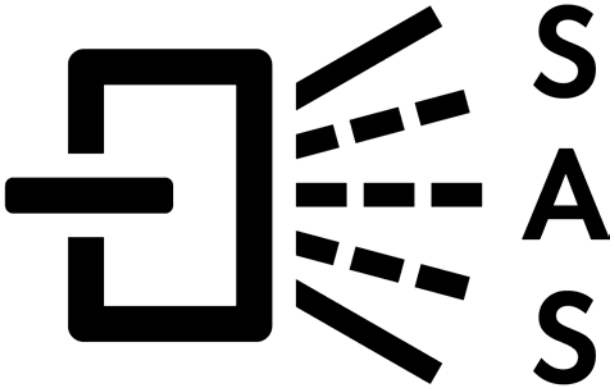


Figure H.3 — SAS alternate icon with SAS letters