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Information technology - Serial Attached SCSI - 4 (SAS-4)

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American National Standard
for Information Technology

Serial Attached SCSI - 4 (SAS-4)

Secretariat
Information Technology Industry Council

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ABSTRACT

This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer - 4 (SPL-4) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 4 (SAS-4). This standard is intended to be used in conjunction with SCSI and ATA command set standards.

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Revision Information

R.1 Revision SAS4r00 (23 December 2014)

First release of SAS-4. The project proposal was 13-215r1.
Incorporated these:

a) this revision contains the physical contents of the SAS-3 standard;
b) movement of informative connector electrical characteristics to an annex;
c) annex revisions to remove actual code from the standard and reference the associated zip file;
d) various editorial revisions to formats and references to align with the T10 style guide;
e) addition of several editor notes; and
f) editorial comments from ISO editors for SAS-2.1 were added.

R.2 Revision SAS4r01 (11 March 2015)

Incorporated these:

a) 14-087r4 SAS-4 MsX Proposal for SAS (Jay Neer, Molex);
b) 15-015r1 SlimLine Internal Connector proposal for inclusion to SAS 4 (McSorley, Amphenol);
c) 15-018r0 SlimLine Internal Connector proposal for inclusion to SAS 4 (Alvin Cox, Seagate); and
d) 15-038r1 SAS-4 update to include 22.5 Gbit/s (Alvin Cox, Seagate).

R.3 Revision SAS4r02 (26 October 2015)

Incorporated these:

a) 15-119r0 SAS-4 removal of withstanding voltage requirement (Alvin Cox. Seagate);
b) 15-124r2 SAS-4 SlimLine SAS Cable Assembly Connection Wiring Diagram Definitions Proposal (Paul Coddington, Amphenol);
c) 15-148r2 SAS-4 Mini-Link Cable Assembly Wiring Diagram Proposal (Darian Schulz, Molex);
d) 15-175r1 Electrical Performance Limits Proposal For SAS-4 22.5 Gbit/s Connectors (Michael Craton, FCI); and
e) various minor editorial corrections and updates.

R.4 Revision SAS4r03 (25 November 2015)

Incorporated these:

a) 15-274r0 SAS-4 connector ILD proposal (Kyle Klinger, TE Connectivity);
b) 15-277r0 SAS-4 r02 corrections (Alex Haser, Molex); and
c) various minor editorial corrections and formatting updates not highlighted with change bars.

R.5 Revision SAS4r04 (15 January 2016)

Incorporated this:

a) 15-291r0 SAS-4: Update to drive connector SFF references in SAS (Fred Fons, Foxconn).

R.6 Revision SAS4r05 (17 March 2016)

Incorporated these:

a) Updated references to list entries per ANSI and ISO/IEC requirements,
b) 16-045r1 SAS-4: Usage of Notes (Alvin Cox, Seagate),
c) 16-085r0 SAS-4 error in note d of table 7 (Alvin Cox, Seagate), and
d) 16-089r0 AFCI SI proposal for SAS4 Specification (Michael Craton, Amphenol).

Contents

Tables

Figures

Foreword (This foreword is not part of this standard)

This standard defines the physical layer of the Serial Attached SCSI (SAS) interconnect.

This standard contains eleven annexes. Annexes A, B, and C are normative and are considered part of this standard. Annexes D through K are informative and are not considered part of this standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, International Committee for Information Technology Standards, Information Technology Institute, 1101 K Street, NW, Suite 610, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by the International Committee for Information Technology Standards (INCITS). Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, INCITS had the following members:

INCITS Technical Committee T10 on SCSI Storage Interfaces, which developed and reviewed this standard, had the following members:

Ralph O. Weber, Chair William Martin, Vice-Chair John Geldman, Secretary

Introduction

This standard defines the Serial Attached SCSI (SAS) interconnect.

The standard is organized as follows:

Clause 1 (Scope) describes the relationship of this standard to the SCSI and ATA families of standards.
Clause 2 (Normative references) provides references to other standards and documents.
Clause 3 (Definitions, symbols, abbreviations, keywords, and conventions) defines terms and conventions used throughout this standard.
Clause 4 (General) describes the SAS physical architecture.
Clause 5 (Physical layer) describes the physical layer. It describes passive interconnect components (connectors, cables, and backplanes), the transmitter device and receiver device electrical characteristics, and out of band (OOB) signals.
Normative Annex A (Jitter tolerance pattern (JTPAT)) describes the jitter tolerance patterns.
Normative Annex B (SASWDP) includes the simulation program used for transmitter device and receiver device compliance.
Normative Annex C (End to end simulation for trained 12 Gbit/s) includes end to end simulation procedures and reference S-parameter file descriptions for trained 12 Gbit/s.
Informative Annex D (StatEye) includes a simulation program that may be used for TxRx connection compliance.
Informative Annex E (12 Gbit/s S-parameters and end to end simulation) provides information regarding S-parameter measurement and an end to end simulation tool description for trained 12 Gbit/s.
Informative Annex F (Signal performance measurements) describes signal measurement techniques.
Informative Annex G (Description of the included Touchstone models for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s) provides information about how S-parameter models included with this standard were derived.
Informative Annex I (Mini SAS 4x active cable assembly power supply and voltage detection circuitry) provides a sample circuit diagram for detecting the presence of a Mini SAS 4x active cable assembly.
Informative Annex H (Recommended electrical performance for connector mated pairs supporting rates of 12 Gbit/s) provides recommended electrical performance characteristics for connector mated pairs supporting rates of 12 Gbit/s.
Informative Annex J (Recommended electrical performance for connector mated pairs supporting rates of 22.5 Gbit/s) provides recommended electrical performance characteristics for connector mated pairs supporting rates of 22.5 Gbit/s.
Informative Annex K (SAS icons) defines the SAS icons.
Informative Annex L (Standards bodies contact information) shows standards bodies and their web sites.
Informative Bibliography lists a bibliography for this standard.

American National Standard
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Serial Attached SCSI - 4 (SAS-4)

1 Scope

The SCSI family of standards provides for many different transport protocols that define the rules for exchanging information between different SCSI devices. This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer - 4 (SPL-4) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 4 (SAS-4), defining the rules for exchanging information between SCSI devices using a serial interconnect. Other SCSI transport protocol standards define the rules for exchanging information between SCSI devices using other interconnects.

Figure 1 shows the relationship of this standard to the other standards and related projects in the SCSI family of standards.

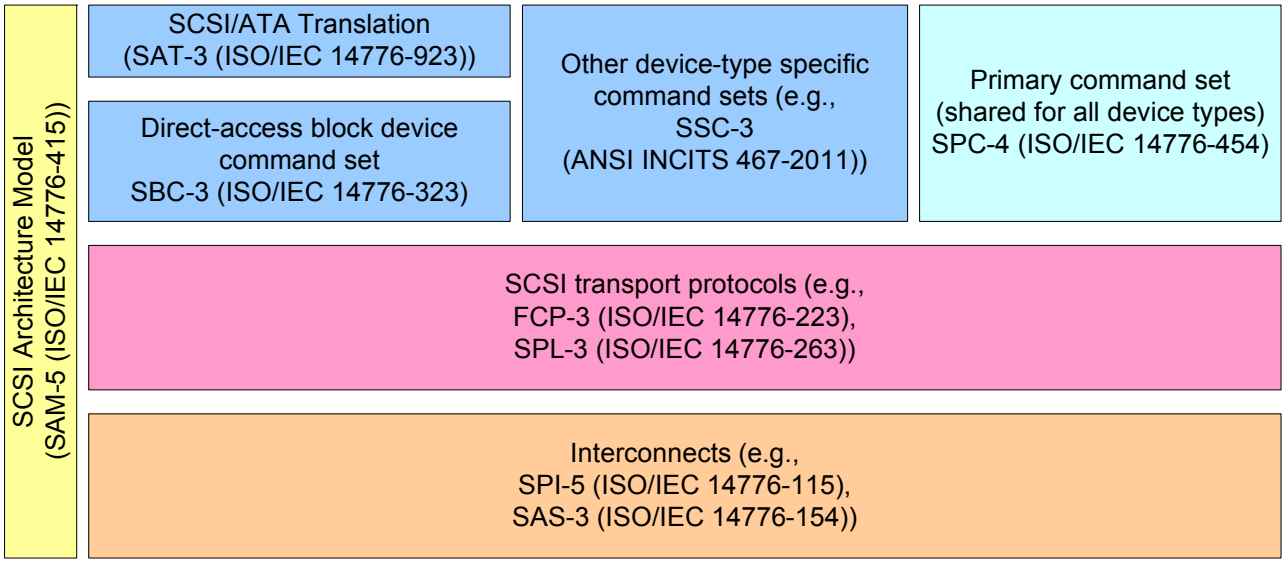

Figure 1 — SCSI document relationships

Figure 2 shows the relationship of this standard to other standards and related projects in the ATA family of standards.

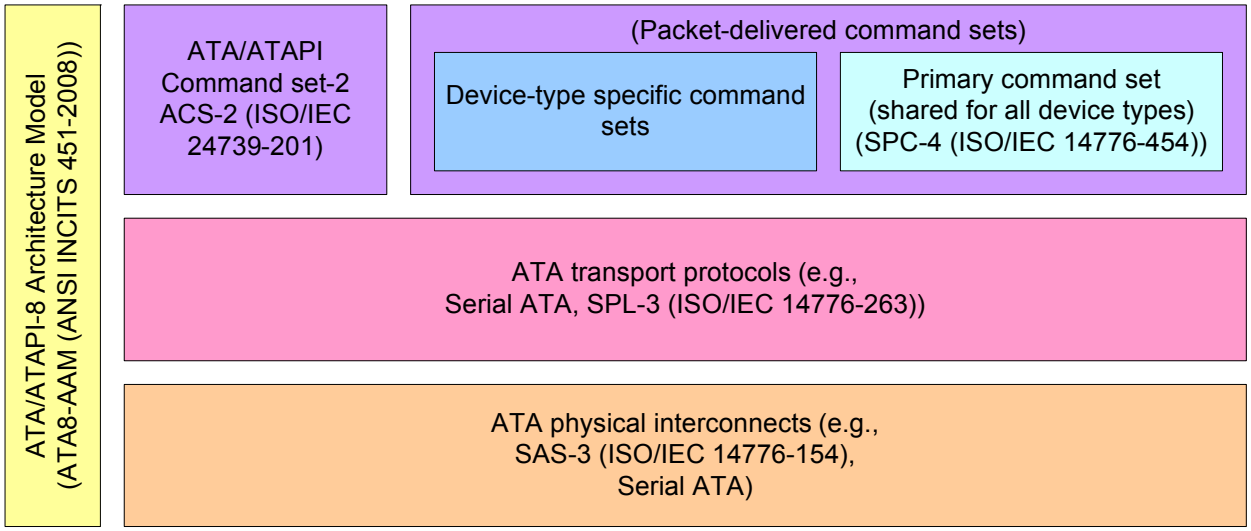

Figure 2 — ATA document relationships

Figure 1 and figure 2 show the general relationship of the documents to one another, and do not imply a relationship such as a hierarchy, protocol stack, or system architecture.

These standards specify the interfaces, functions, and operations necessary to ensure interoperability between conforming implementations. This standard is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

Editor's Note 1: Update references in figure 1 and figure 2.

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2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

Additional availability contact information is provided in Annex L.

ISO/IEC 14776-151, *Serial Attached SCSI -1.1 (SAS-1.1)*

ISO/IEC 14776-152, *Information Technology - Serial Attached SCSI - 2 (SAS-2)*

ISO/IEC 14776-153, *Information Technology - Serial Attached SCSI - 2.1 (SAS-2.1)*

ISO/IEC 14776-154, *Serial Attached SCSI - 3 (SAS-3)*

ISO/IEC 14776-264, *SAS Protocol Layer - 4 (SPL-4)*

ANSI INCITS TR-35-2004, *Methodologies for Jitter and Signal Quality Specification (MJSQ)*. When MJSQ is referenced from this standard, the FC Port terminology used within MJSQ should be substituted with SAS phy terminology

IEC 60169-15, First edition 1979-01, *Radio-frequency connectors. Part 15: R.F. coaxial connectors with inner diameter of outer conductor 4.13 mm (0.163 in) with screw coupling — Characteristic impedance 50 Ω (Type SMA)*

BSR INCITS 515, *Information technology - SCSI Architecture Model - 5 (SAM-5)* (planned as ISO/IEC 14776-415)

ISO 80000-2, *Quantities and units -- Part 2: Mathematical signs and symbols to be used in the natural sciences and technology*

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

Serial ATA Revision 3.1 (SATA). 18 July 2011

For information on the current status of Serial ATA documents, contact the Serial ATA International

NOTE 1 - For information on the current status of Serial ATA documents, contact the Serial ATA international Organization (see www.sata-io.org).

SFF-8086, *Mini Multilane 4X10 Gb/s Common Elements Connector*

SFF-8087, *Mini Multilane 4X Unshielded Connector Shell and Plug*

SFF-8088, *Mini Multilane 4X Shielded Connector Shell and Plug*

SFF-8147, *54mm x 71mm Form Factor with Micro SAS Connector*

SFF-8223, *2.5inch Form Factor Drive with Serial Attached Connector*

SFF-8323, *3.5inch Form Factor Drive with Serial Attached Connector*

SFF-8449, *Mini Multilane Series Management Interface*

SFF-8410, *HSS Copper Testing and Performance Requirements*

SFF-8416, *HPEI Bulk Cable Measurement/Performance Requirements*

SFF-8482, *Serial Attachment 2X Unshielded Connector*

SFF-8485, *Serial GPIO (General Purpose Inuput/Output) Bus*

SFF-8486, *Serial Attachment 4X Unshielded Micro Connector*

SFF-8523, *5.25inch Form Factor Drive w/Serial Attachment Connector*

SFF-8611, *MiniLink 4/8X I/O Cable Assemblies*

SFF-8612, *MiniLink 4/8X Shielded Connector*

SFF-8630, *Serial Attachment 4X 12 Gbs Unshielded Connector*

SFF-8636, *Management Interface for cabled Environments*

SFF-8639, *Multifunction 6X Unshielded Connector*

SFF-8643, *Mini Multilane 4/8X 12 Gb/s Unshielded Connector (HD12un)*

SFF-8644, *Mini Multilane 4/8X 12 Gb/s Shielded Connector (HD12sh)*

SFF-8654, *0.6mm 4/8X Unshielded I/O Connector*

SFF-8685, *QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)*

SFF-9639, *Multifunction 6X Unshielded Connector Pinouts*

NOTE 2 - For more information on the current status of SFF documentsor to obtain copies of these documents, contact the SFF Committee (see http://www.sffcommittee.org).

ASTM Standard B 258-02, 2002, *Standard specification for standard nominal diameters and cross-sectional areas of AWG sizes of solid round wires used as electrical conductors*, ASTM International, West Conshohocken, PA, USA.

NOTE 3 - For more information on ASTM International standards, see www.astm.org.

PANTONE® Color Formula Guide

NOTE 4 - Pantone® is a registered trademark of Pantone, Inc. For more information on Pantone colors, contact Pantone, Inc. (see http://www.pantone.com).

Touchstone® File Format Specification. Revision 1.1. IBIS Open Forum.

NOTE 5 - Touchstone® is a registered trademark of Agilent Corporation. For more information on the Touchstone specification, contact the IBIS Open Forum (see http://www.eigroup.org).

MATLAB® 7 Programming Fundamentals. Release 2008b.

NOTE 6 - MATLAB® is a registered trademark of The MathWorks, Inc. For more information on MATLAB, contact The Mathworks, Inc. (see http://www.mathworks.com).

GNU Octave 3.6.4 or newer

NOTE 7 - For more information on Octave and to obtain a copy of this software, see http://www.gnu.org/software/octave/.

3 Definitions, symbols, abbreviations, keywords, and conventions

3.1 Definitions

3.1.1 active cable assembly
cable assembly (see 3.1.9) that requires power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.2 alternating current (A.C.)
non-D.C. component of a signal

Note 1 to entry: In this standard, all frequency components greater than or equal to 100 kHz.

3.1.3 baud rate
nominal signaling speed, expressed as the maximum number of times per second that the signal (see 3.1.99) may change the state of the physical link (see 3.1.67)

Note 1 to entry: Each state change produces a transition (i.e., signal edge).

Note 2 to entry: Baud rate is the reciprocal of the UI (i.e., $f_{baud} = 1 / UI$) (see 3.1.118).

3.1.4 bit error ratio (BER)
number of logical bits output from a receiver circuit that differ from the correct transmitted logical bits, divided by the number of transmitted logical bits

Note 1 to entry: BER is computed on the raw bit stream before 10b8b or 150b128b decoding.

Note 2 to entry: BER is usually expressed as a coefficient and a power of 10 (e.g., 2 erroneous bits out of 100 000 bits transmitted is expressed as 2 out of 10^5 or 2×10^{-5}).

Note 3 to entry: See MJSQ.

3.1.5 bit time
nominal duration of a signal transmission bit (e.g., $666.\overline{6}$ ps at 1.5 Gbit/s, $333.\overline{3}$ ps at 3 Gbit/s, $166.\overline{6}$ ps at 6 Gbit/s, $83.\overline{3}$ ps at 12 Gbit/s, and $44.\overline{4}$ ps at 22.5 Gbit/s)

3.1.6 bounded uncorrelated jitter (BUJ)
part of DJ (see 3.1.24) not aligned in time with the signal being measured

Note 1 to entry: Specifically, BUJ excludes ISI (see 3.1.48) and duty cycle distortion.

Note 2 to entry: See MJSQ.

3.1.7 burst time
part of an OOB signal (see 3.1.61) where the OOB burst (see 3.1.57) is transmitted

Note 1 to entry: See 5.11.

3.1.8 byte
sequence of eight contiguous bits considered as a unit

3.1.9 cable assembly
bulk cable with a separable connector at each end plus any retention, backshell, shielding features, or circuitry used for cable management or signal transmission

Note 1 to entry: See 5.4.3.

3.1.10 clock data recovery (CDR)
function provided by the receiver circuit responsible for producing a regular clock signal (i.e., the recovered clock) from the received signal and for aligning the recovered clock to the symbols (i.e., bits) being transmitted with the signal

Note 1 to entry: CDR uses the recovered clock to recover the bits.

Note 2 to entry: See MJSQ.

3.1.11 common SSC transmit clock
implementation that employs a single transmit clock for multiple transmitter devices and enables or disables SSC (see 5.8.6) on the transmit clock signal to all transmitter devices in common rather than allowing each transmitter device to independently control SSC

3.1.12 compliance point
interoperability point where interoperability specifications are met

Note 1 to entry: See 5.3.

3.1.13 compliant jitter tolerance pattern (CJTPAT)
test pattern for jitter testing in SAS dword mode

Note 1 to entry: See 5.8.3.5 and Annex A.

3.1.14 connector
electro-mechanical components consisting of a receptacle and a plug that provide a separable interface between two transmission segments

Note 1 to entry: See 5.4.3.

3.1.15 consecutive identical digits (CID)
serial bit stream with repeated data bits of the same binary value

3.1.16 cumulative distribution function (CDF)
probability that jitter (see 3.1.49) is less than a given value

Note 1 to entry: See MJSQ.

3.1.17 D.C. idle
differential signal level that is nominally 0 V(P-P), used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61) when D.C. mode (see 3.1.18) is enabled

Note 1 to entry: See 5.8.4.

3.1.18 D.C. mode
mode in which D.C. idle (see 3.1.17) is used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61)

3.1.19 data dependent jitter (DDJ)
jitter (see 3.1.49) that is added when the transmission pattern is changed from a clock-like to a non-clock-like pattern

Note 1 to entry: See MJSQ.

3.1.20 decibel (dB)
ten times the common logarithm (i.e., lg) of the ratio of relative powers

Note 1 to entry: The ratio of powers P_1 and P_2 in dB is $10 \times \lg (P_1 / P_2)$. If $P_1 = V_1^2 / R_1$, $P_2 = V_2^2 / R_2$, and $R_1 = R_2$, then this ratio is equivalent to 20 times the common logarithm of the relative voltage ratio (i.e., dB is $20 \times \lg (V_1 / V_2)$). A ratio of 1 results in a dB value of 0 (e.g., $20 \times \lg (1) = 0$ dB), a ratio greater than

1 results in a positive dB value (e.g., 20 × lg (2) = 6 dB) and a ratio less than 1 results in a negative dB value (e.g., 20 × lg (0.5) = -6 dB).

3.1.21 dB millivolts (dBmV)
decibel ratio of an rms voltage value relative to 1 mV

Note 1 to entry: 20 mV(rms) is equal to 20 × lg(20 mV / 1 mV) = 26 dBmV. This does not depend on the impedance level.

3.1.22 dB milliwatts (dBm)
decibel ratio of a power value relative to 1 mW

Note 1 to entry: 20 mW is equal to 10 × lg(20 mW / 1 mW) = 13 dBm. If power is measured with a 50 Ω impedance level, then 20 mW is equivalent to $(0.02 \text{ W} \times 50\ \Omega)^{(1/2)}$ = 1 V or 60 dBmV. If power is measured with a 25 Ω impedance level (i.e., the reference impedance for common mode measurements), then 20 mW is equivalent to $(0.02 \text{ W} \times 25\ \Omega)^{(1/2)}$ = 0.707 V or 57 dBmV.

3.1.23 decision feedback equalizer (DFE)
nonlinear equalizer that uses a feedback loop based on previously decoded symbols

3.1.24 deterministic jitter (DJ)
jitter (see 3.1.49) with non-Gaussian distribution that is bounded in amplitude and has specific causes

Note 1 to entry: See MJSQ.

3.1.25 direct current (D.C.)
non-A.C. component of a signal

Note 1 to entry: In this standard, all frequency components below 100 kHz.

3.1.26 disparity
difference between the number of ones and zeros in a character

Note 1 to entry: See SPL-4.

3.1.27 dispersion
signal pulse broadening and distortion from all causes

3.1.28 duty cycle distortion (DCD)
one-half of the difference of the average width of a one and the average width of a zero in a signal waveform eye pattern measurement

Note 1 to entry: See MJSQ.

3.1.29 dword
sequence of four contiguous bytes or four contiguous characters considered as a unit

Note 1 to entry: See SPL-4.

3.1.30 electromagnetic interference (EMI)

any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment

3.1.31 enclosure
box, rack, or set of boxes providing the powering, cooling, mechanical protection, EMI protection, and external electronic interfaces for one or more end device(s) (see 3.1.35) and/or expander device(s) (see SPL-4)

Note 1 to entry: Provides the outermost electromagnetic boundary and acts as an EMI barrier.

3.1.32 enclosure in port
set of expander phys with subtractive routing attributes using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL-4.

3.1.33 enclosure out port
set of expander phys with table routing attributes in an expander device that does not support table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL-4.

3.1.34 enclosure universal port
set of expander phys with table routing attributes in an expander device that supports table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL-4.

3.1.35 end device
SAS device or SATA device that is not contained within an expander device (see 3.1.38)

Note 1 to entry: See SPL-4.

3.1.36 end to end simulation
simulation performed from a reference transmitter or from a captured signal to a reference receiver device

3.1.37 etch
printed circuit board copper conductor path

3.1.38 expander device
device that is part of a service delivery subsystem (see SAM-5), facilitates communication between SAS devices (see 3.1.89) and SATA devices (see 3.1.95)

Note 1 to entry: See SPL-4.

3.1.39 expander phy
phy in an expander device that interfaces to a service delivery subsystem (see SAM-5)

Note 1 to entry: See SPL-4.

3.1.40 expander port
expander device object that interfaces to a service delivery subsystem (see SAM-5) and to SAS ports in other devices

Note 1 to entry: See SPL-4.

3.1.41 external connector
bulkhead connector (see 3.1.14) that carries signals into and out of an enclosure (see 3.1.31) and exits the enclosure with only minor compromise to the shield effectiveness of the enclosure (e.g., a Mini SAS 4x receptacle or Mini SAS HD receptacle)

Note 1 to entry: See 5.4.3.4.

3.1.42 eye contour
locus of points in a signal level versus time eye diagram where the CDF of 10^{-12} in the actual signal population exists

Note 1 to entry: Comparison of the measured eye contour to the jitter eye mask determines whether a jitter eye mask violation has occurred.

Note 2 to entry: For simulations, a CDF of 10^{-15} is used.

Note 3 to entry: See 5.8.3 and MJSQ.

3.1.43 fall time
time interval for the falling signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 80 % and 20 % voltage levels.

Note 2 to entry: Also see rise time (see 3.1.88).

3.1.44 fanout cable assembly
cable assembly with one connector on one end and multiple connectors on the other end

Note 1 to entry: See 5.4.4.1.3.

3.1.45 field
group of one or more contiguous bits

3.1.46 idle time
part of an OOB signal (see 3.1.61) where OOB idle (see 3.1.17) is being transmitted

Note 1 to entry: See 5.11.

3.1.47 insertion loss
ratio of incident power to delivered power

Note 1 to entry: The dB magnitude of S_{12} or S_{21} is the negative of insertion loss in dB.

Note 2 to entry: See F.11.

3.1.48 intersymbol interference (ISI)
reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses

Note 1 to entry: Neighboring pulses are pulses that are close enough to have significant energy overlapping the affected pulse and does not imply or exclude adjacent pulses (i.e., many bit times (see 3.1.5) may separate the pulses, especially in the case of reflections).

Note 2 to entry: May result in DDJ and vertical eye closure.

Note 3 to entry: Produced by several mechanisms (e.g., dispersion, reflections, and circuits that lead to baseline wander).

Note 4 to entry: See MJSQ.

3.1.49 jitter
collection of instantaneous deviations of signal edge times at a defined signal level of the signal from the reference times for those events

Note 1 to entry: Reference times are, for example, times defined by the jitter timing reference.

Note 2 to entry: See MJSQ.

3.1.50 jitter timing reference
signal used as the basis for calculating the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.51 jitter tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal applied to the receiver device compliance point

Note 1 to entry: See MJSQ.

3.1.52 jitter tolerance pattern (JTPAT)
data test pattern for jitter testing in SAS dword mode of a receiver device contained within CJTPAT

Note 1 to entry: See Annex A.

3.1.53 least mean square (LMS)
algorithm for adaptively adjusting the tap coefficients of a DFE (see 3.1.23) based on the difference between the desired and actual signal

3.1.54 managed connector category
category of connectors that support a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.55 near-end crosstalk (NEXT)
crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the disturbing channel

Note 1 to entry: The terminals of the disturbed channel, at which the near-end crosstalk is present, and the energized terminals of the disturbing channel are usually near each other.

3.1.56 negation time
part of an OOB signal (see 3.1.61) during which OOB idle (see 3.1.58) is transmitted after the last OOB burst (see 3.1.57)

Note 1 to entry: See 5.11.

3.1.57 OOB burst
transmission of signal transitions or ALIGN3 primitives for a burst time (see 3.1.7)

Note 1 to entry: See 5.11.1.

3.1.58 OOB idle
transmission of D.C. idle (see 3.1.17) when D.C. mode (see 3.1.18) is enabled or a defined sequence of dwords when optical mode (see 3.1.62) is enabled

3.1.59 OOB interval
time basis for burst times (see 3.1.7), idle times (see 3.1.46), negation times (see 3.1.56), and signal times (see 3.1.102) used to create OOB signals (see 3.1.61)

Note 1 to entry: See 5.11.1.

3.1.60 OOB sequence
sequence where two phys exchange OOB signals (see 3.1.61)

Note 1 to entry: See SPL-4.

3.1.61 OOB signal
pattern of idle time (see 3.1.46), burst time (see 3.1.7), and negation time (see 3.1.56) used during the link reset sequence

Note 1 to entry: See 5.11.

3.1.62 optical mode
mode in which a defined sequence of dwords is used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61)

Note 1 to entry: See 5.11.

3.1.63 passive cable assembly
cable assembly (see 3.1.9) that does not require external power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.64 passive TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.111) and receiver circuit (see 3.1.75) that does not include powered circuitry used in the transmission of the signal through the TxRx connection (see 3.1.116)

Note 1 to entry: See 5.5.1.

3.1.65 phy
object in a device that is used to interface to other devices

Note 1 to entry: Other devices are, for example, expander phys and SAS phys.

Note 2 to entry: See 4.1.

3.1.66 physical interconnect TxRx connection segment (PICS)
TxRx connection segment (see 3.1.117) used to model channel loss between the TDCS (see 3.1.115) and the RDCS (see 3.1.79)

Note 1 to entry: See 5.3.3.

3.1.67 physical link
two differential signal pairs, one pair in each direction, that connect two physical phys (see 3.1.65)

Note 1 to entry: See 4.1.

3.1.68 physical link rate
link rate between two physical phys established as a result of speed negotiation between those phys

3.1.69 power on
power being applied

3.1.70 probe point
physical position in a test load where signal characteristics for compliance points are measured

Note 1 to entry: See 5.6.

3.1.71 post cursor equalization ratio (R_{post})
ratio of the equalization peak signal voltage to the nominal signal voltage after a signal voltage change

Note 1 to entry: See 5.8.4.7.1.

3.1.72 precursor equalization ratio (R_{pre})
ratio of the equalization peak signal voltage to the nominal signal voltage prior to a signal voltage change

Note 1 to entry: See 5.8.4.7.1.

3.1.73 random jitter (RJ)
jitter (see 3.1.49) characterized by a Gaussian distribution and that is unbounded

Note 1 to entry: See MJSQ.

3.1.74 rate
data transfer rate of a physical or logical link

Note 1 to entry: Data transfer rates are, for example,1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, 12 Gbit/s, or 22.5 Gbit/s.

3.1.75 receiver circuit
electronic circuit that converts an analog serial input signal to a logic signal

3.1.76 receiver circuit TxRx connection segment (RCCS)
TxRx connection segment (see 3.1.117) used to model package loss within the simulated receiver circuit (see 3.1.75)

3.1.77 reference clock
clock generated by the PLL

Note 1 to entry: This clock is filtered by the JTF (see 5.8.3.2) and aligned with the zero-crossing instants.

3.1.78 receiver device (Rx)
device downstream from a receiver device compliance point (see 3.1.12) containing a portion of the physical link and a receiver circuit (see 3.1.75)

3.1.79 receiver device TxRx connection segment (RDCS)
TxRx connection segment (see 3.1.117) between the simulated receiver circuit (see 3.1.75) and a separable connector

3.1.80 reference pulse response cursor (peak to peak)
cursor that is twice the amplitude of the response to a one UI wide positive pulse of the same amplitude and transmitter equalization as the data stream it represents (see 5.7.3), sampled at the reference sampling instant (see 3.1.83)

3.1.81 reference receiver device
set of parameters defining electrical performance characteristics that provide a set of minimum electrical performance requirements for a receiver device and that are also used in mathematical modeling to determine compliance of a TxRx connection or transmitter device

Note 1 to entry: See 5.8.5.7.3.

3.1.82 reference sampling clock
reference clock (see 3.1.77) shifted by 0.5 UI (see 3.1.118)

3.1.83 reference sampling instant
instant at which a reference sampling clock (see 3.1.82) samples the maximum amplitude of the response to a positive pulse generated using the reference sampling clock

Note 1 to entry: See figure 135.

3.1.84 reference transmitter device
set of parameters defining electrical performance characteristics of a transmitter device that are used in mathematical modeling to determine compliance of a TxRx connection

Note 1 to entry: See 5.8.4.6.5 and 5.8.4.7.3.

3.1.85 reference transmitter test load
set of S-parameters defining the electrical characteristics of a TxRx connection used as the basis for transmitter device and receiver device performance evaluation through mathematical modeling

Note 1 to entry: See 5.6.5.

3.1.86 reflection coefficient (ρ)
ratio of reflected voltage to incident voltage

3.1.87 return loss
ratio of incident power to reflected power

Note 1 to entry: The dB magnitude of S_{11} or S_{22} is the negative of return loss in dB.

Note 2 to entry: Return loss is usually expressed in decibel (dB).

Note 3 to entry: See F.11.

3.1.88 rise time
time interval for the rising signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 20 % and 80 % voltage levels.

Note 2 to entry: Also see fall time (see 3.1.43).

3.1.89 SAS device
SAS initiator device (see SPL-4) and/or SAS target device (see SPL-4)

3.1.90 SAS dword mode
physical link rate is less than or equal to 12 Gbit/s (i.e., G1, G2, G3, or G4)

Note 1 to entry: See SPL-4.

3.1.91 SAS packet mode
physical link rate is greater than 12 Gbit/s (i.e., G5)

Note 1 to entry: See SPL-4.

3.1.92 SAS phy
phy in a SAS device (see 3.1.89) that interfaces to a service delivery subsystem (see SAM-5)

3.1.93 SAS target device
device containing SSP, STP, and/or SMP target ports in a SAS domain

Note 1 to entry: See SPL-4.

3.1.94 SAS target device circuitry
at a minimum, the circuitry in the SAS target device (see SPL-4) providing control of the SAS phy (see 3.1.92) and protocol support for communication through the physical link (see 3.1.67)

Note 1 to entry: Application of power to the SAS target device circuitry results in actions defined for power on (see SPL-4).

3.1.95 SATA device
ATA device that contains a SATA device port in an ATA domain

Note 1 to entry: See SPL-4.

3.1.96 SATA phy
phy in a SATA device (see SPL-4) or SATA port selector (see SPL-4) that interfaces to a service delivery subsystem (see SAM-5)

Note 1 to entry: Analogous to a SAS phy (see 3.1.92).

3.1.97 Serial ATA (SATA)
protocol defined by SATA

Note 1 to entry: See SATA.

3.1.98 Serial Attached SCSI (SAS)
set of protocols defined in SPL-4 and the interconnect defined by this standard

3.1.99 signal
detectable transmitted energy that is used to carry information

3.1.100 signal amplitude
property of the overall signal (see 3.1.99) that describes the peak or peak to peak values of the signal level (see 3.1.101)

3.1.101 signal level
instantaneous intensity of a signal (see 3.1.99) measured in volts

3.1.102 signal time
time of an OOB signal (see 3.1.61), consisting of six burst times (see 3.1.7), six idle times (see 3.1.46), and one negation time (see 3.1.56)

Note 1 to entry: See 5.11.

3.1.103 signal tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream with maximum jitter and minimum amplitude

Note 1 to entry: See MJSQ.

3.1.104 significant crosstalk
crosstalk source having a magnitude point of its transfer function in excess of -50 dB in the range of frequencies up to 6 GHz

3.1.105 sinusoidal jitter (SJ)
single frequency jitter (see 3.1.49) applied during signal tolerance testing

Note 1 to entry: See MJSQ.

3.1.106 spread spectrum clocking (SSC)
technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions

Note 1 to entry: The operating frequency of a transmitted signal is the physical link rate

Note 2 to entry: See SPL-4.

3.1.107 symbol
smallest unit of data transmission on a physical link

Note 1 to entry: The smallest unit of data is a bit.

Note 2 to entry: A symbol represents a single transition if the maximum transition rate (i.e., a 0101b pattern) is occurring.

3.1.108 total jitter (TJ)
jitter (see 3.1.49) from all sources

Note 1 to entry: See MJSQ.

3.1.109 trained
physical link rate negotiated with Train_Rx-SNW

Note 1 to entry: See SPL-4.

3.1.110 transceiver
physical entity that contains both a transmitter device (see 3.1.114) and a receiver device (see 3.1.78)

3.1.111 transmitter circuit
electronic circuit that converts a logic signal to an analog serial output signal

3.1.112 transmitter circuit TxRx connection segment (TCCS)
TxRx connection segment (see 3.1.117) used to model package loss within the simulated transmitter circuit (see 3.1.111)

3.1.113 transmitter compliance transfer function (TCTF)
mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask

Note 1 to entry: See 5.8.4.1.

3.1.114 transmitter device (Tx)
device upstream from a transmitter device compliance point (see 3.1.12) containing a portion of the physical link and a transmitter circuit (see 3.1.111)

3.1.115 transmitter device TxRx connection segment (TDCS)
TxRx connection segment (see 3.1.117) between the transmitter circuit (see 3.1.111) and a separable connector

3.1.116 TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.111) and receiver circuit (see 3.1.75)

Note 1 to entry: See 5.5.1.

3.1.117 TxRx connection segment
portion of a TxRx connection (see 3.1.116) delimited by separable connectors or changes in the conductive material

Note 1 to entry: See 5.5.1.

3.1.118 unit interval (UI)
normalized, dimensionless, nominal duration of a symbol (see 3.1.107)

Note 1 to entry: IUs are, for example, 666.$\overline{6}$ ps at 1.5 Gbit/s, 333.$\overline{3}$ ps at 3 Gbit/s, 166.$\overline{6}$ ps at 6 Gbit/s, 83.$\overline{3}$ ps at 12 Gbit/s, and 44.$\overline{4}$ ps at 22.5 Gbit/s.

Note 2 to entry: The UI is the reciprocal of the baud rate (i.e., UI = 1 / f_{baud}) (see 3.1.3).

3.1.119 unmanaged active connector category
category of connectors that support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) but do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.120 unmanaged passive connector category
category of connectors that do not support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) and do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.121 untrained
physical link rate not negotiated with Train_Rx-SNW

Note 1 to entry: See SPL-4.

3.1.122 usage variable
SASWDP parameter set to a value that determines if the stressor file is to be added to the simulation

Note 1 to entry: See Annex B.

3.1.123 voltage modulation amplitude (VMA)
difference in electrical voltage of a signal (see 3.1.99) between the stable one level and the stable zero level

3.1.124 waveform dispersion penalty (WDP)

simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device

Note 1 to entry: See 5.8.4.6.1 and Annex B.

3.2 Symbols and abbreviations

3.2.1 Abbreviations

See Annex L for abbreviations of standards bodies (e.g., ISO).

Units and abbreviations used in this standard:

Abbreviation	Meaning
A.C.	alternating current (see 3.1.2)
ATA	AT attachment
AWG	American wire gauge (see ASTM Standard B 258-02 (see clause 2))
BER	bit error ratio (see 3.1.4)
BUJ	bounded uncorrelated jitter (see 3.1.6)
C1	coefficient 1 (see 5.8.4.7.3)
C2	coefficient 2 (see 5.8.4.7.3)
C3	coefficient 3 (see 5.8.4.7.3)
CDF	cumulative distribution function (see 3.1.16)
CDR	clock data recovery (see 3.1.10)
CIC	compliance interconnect channel (see SATA)
CID	consecutive identical digits (see 3.1.15)
CJTPAT	compliant jitter tolerance pattern (see 3.1.13)
CR	inter-enclosure (i.e., cabinet) receiver device compliance point (see 5.3)
CT	inter-enclosure (i.e., cabinet) transmitter device compliance point (see 5.3)
D.C.	direct current (see 3.1.25)
DCD	duty cycle distortion (see 3.1.28)
DDJ	data dependent jitter (see 3.1.19)
DFE	decision feedback equalizer (see 3.1.23)
DJ	deterministic jitter (see 3.1.24)
EMI	electromagnetic interference (see 3.1.30)
ER	end to end transmitter device compliance point (see 5.3)
ESD	electrostatic discharge
ET	end to end receiver device compliance point (see 5.3)
G1	generation 1 physical link rate (i.e., 1.5 Gbit/s)
G2	generation 2 physical link rate (i.e., 3 Gbit/s)
G3	generation 3 physical link rate (i.e., 6 Gbit/s)
G4	generation 4 physical link rate (i.e., 12 Gbit/s)
G5	generation 5 physical link rate (i.e., 22.5 Gbit/s)
Gbit/s	gigabit per second (i.e., 10^9 bits per second)
Gen1i	SATA generation 1 physical link rate (i.e., 1.5 Gbit/s) (see SATA)

Abbreviation	Meaning
Gen2i	SATA generation 2 physical link rate (i.e., 3 Gbit/s) (see SATA)
Gen3i	SATA generation 3 physical link rate (i.e., 6 Gbit/s) (see SATA)
GPIO	general purpose input/output
HD	high-density
ICN	integrated crosstalk noise
IR	intra-enclosure (i.e., internal) receiver device compliance point (see 5.3)
ISI	intersymbol interference (see 3.1.48)
IT	intra-enclosure (i.e., internal) transmitter device compliance point (see 5.3)
JMD	jitter measurement device
JTF	jitter transfer function (see 5.8.3.2)
JTPAT	jitter tolerance pattern (see 3.1.52)
LED	light-emitting diode
LMS	least mean square (see 3.1.53)
MJSQ	Methodologies for Jitter and Signal Quality Specification
N/A	not applicable
N/C	not connected
NEXT	near-end crosstalk (see 3.1.55)
OOB	out-of-band
OOBI	out-of-band interval (see 3.1.59)
PCB	printed circuit board
PICS	physical interconnect TxRx connection segment (see 3.1.66)
PJ	periodic jitter
PLL	phase lock loop
P-P	peak to peak
RCCS	receiver circuit TxRx connection segment (see 3.1.76)
RD	running disparity (see SPL-4)
RDCS	receiver device TxRx connection segment (see 3.1.79)
RJ	random jitter (see 3.1.73)
RR	receiver device die attachment point to RCCS
Rx	receiver device (see 3.1.78)
SAM-5	SCSI Architecture Model - 5 standard (see clause 2)
SAS	Serial Attached SCSI (see 3.1.98)
SATA	Serial ATA (see 3.1.97) or the Serial ATA 3.1 specification (see clause 2)
SCSI	Small Computer System Interface
SGPIO	serial GPIO (see clause 2)
SJ	sinusoidal jitter (see 3.1.105)
SMA	subminiature version A connector (see clause 2)
SPL-4	SAS Protocol Layer - 4 (see clause 2)
SSC	spread spectrum clocking
STP	Serial ATA Tunneled Protocol
TCCS	transmitter circuit TxRx connection segment (see 3.1.112)

Abbreviation	Meaning
TCTF	transmitter compliance transfer function (see 3.1.113)
TDCS	transmitter device TxRx connection segment (see 3.1.115)
TDNA	time domain network analyzer (i.e., TDR/TDT plus analysis software that performs a VNA-style output)
TDR	time domain reflectometer
TDT	time domain transmission
TJ	total jitter (see 3.1.108)
Tx	transmitter device (see 3.1.114)
UI	unit interval (see 3.1.118)
VMA	voltage modulation amplitude (see 3.1.123)
VNA	vector network analyzer
WDP	waveform dispersion penalty (see 3.1.124)
XCS	crosstalk connection segment (see 5.5.6)

3.2.2 Units

Units used in this standard:

Units	Meaning
dB	decibel (see 3.1.20)
dBm	decibel milliwatts (see 3.1.22)
dBmV	decibel millivolts (see 3.1.21)
Gbit/s	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)(i.e., s^{-9})
Hz	hertz (i.e., cycles per second)(i.e., s^{-1})
in	inche
kHz	kilohertz (i.e., 10^3 cycles per second)(i.e., s^{-3})
kΩ	kilohm (i.e., 10^3 ohms)
µA	microampere (i.e., 10^{-6} amperes)
µs	microsecond (i.e., 10^{-6} seconds)
m	meter
mA	milliampere (i.e., 10^{-3} amperes)
MBps	megabytes per second (i.e., 10^6 bytes per second)
MHz	megahertz (i.e., 10^6 cycles per second)(i.e., s^{-6})
mm	millimeter (i.e., 10^{-3} meters)
ms	millisecond (i.e., 10^{-3} seconds)
mV	millivolt (i.e., 10^{-3} volts)
mW	milliwatt (i.e., 10^{-3} watts)
nF	nanofarad (i.e., 10^{-9} farads)
ns	nanosecond (i.e., 10^{-9} seconds)
pF	picofarad (i.e., 10^{-12} farads)
ppm	parts per million (i.e., 10^{-6})
ps	picosecond (i.e., 10^{-12} seconds)

Units	Meaning
rms	root mean square (i.e., quadratic mean)
s	second (unit of time)
V	volt
W	watt

3.2.3 Symbols

Symbols used in this standard:

Symbols	Meaning
Dxx.y	data character (see 3.1.19)
K_0	output gain
R_{post}	post cursor equalization ratio (see 3.1.71)
R_{pre}	precursor equalization ratio (see 3.1.72)
®	registered trademark
S_{ij}	S-parameter for port j to port i (see F.11)
S_{CCij}	S-parameter for common mode to common mode port j to port i (see F.11)
S_{CDij}	S-parameter for differential to common mode port j to port i (see F.11)
S_{DCij}	S-parameter for common mode to differential port j to port i (see F.11)
S_{DDij}	S-parameter for differential to differential port j to port i (see F.11)
Δ (delta)	difference operator
ϕ (phi)	phase
π (pi)	3.141 59... , the ratio of the circumference of a circle to its diameter
ρ (rho)	reflection coefficient (see 3.1.86)
τ (tau)	time constant
Ω (omega)	ohm (unit of electrical resistance)

3.2.4 Mathematical operators

Mathematical operators used in this standard:

Mathematical Operators	Meaning
e	2.718 28..., the base of the natural (i.e., hyperbolic) system of logarithms
lg	$\log_{10}$
sgn	signum function (i.e., sign function)
^	exclusive logical OR
<	less than
$\leq$	less than or equal to
>	greater than
$\geq$	greater than or equal to
±	plus or minus
×	multiplication
/	division
|v|	the absolute value (i.e., magnitude) of v

Mathematical Operators	Meaning
~	approximately equal to
⊗	convolution

3.3 Keywords

3.3.1 invalid
keyword used to describe an illegal or unsupported bit, byte, word, field or code value

Note 1 to entry: Receipt of an invalid bit, byte, word, field or code value shall be reported as an error.

3.3.2 mandatory
keyword indicating an item that is required to be implemented as defined in this standard

3.3.3 may
keyword that indicates flexibility of choice with no implied preference

3.3.4 may not
keyword that indicates flexibility of choice with no implied preference

3.3.5 obsolete
keyword indicating that an item was defined in prior SCSI standards but has been removed from this standard

3.3.6 option, optional
keywords that describe features that are not required to be implemented by this standard

Note 1 to entry: If any optional feature defined by this standard is implemented, then it shall be implemented as defined in this standard

3.3.7 prohibited
keyword used to describe a feature, function, or coded value that is defined in a a non-SCSI standard (i.e., a standard that is not a member of the SCSI family of standards) to which this standard makes a normative reference where the use of said feature, function, or coded value is not allowed for implementations of this standard

3.3.8 reserved
keyword referring to bits, bytes, words, fields, and code values that are set aside for future standardization

Note 1 to entry: A reserved bit, byte, word, or field shall be set to zero, or in accordance with a future extension to this standard.

Note 2 to entry: Recipients are not required to check reserved bits, bytes, words, or fields for zero values.

Note 3 to entry: Receipt of reserved code values in defined fields shall be reported as error.

3.3.9 restricted
keyword referring to bits, bytes, words, and fields that are set aside for other identified standardization purposes

Note 1 to entry: A restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears.

3.3.10 shall
keyword indicating a mandatory requirement

Note 1 to entry: Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.3.11 should
keyword indicating flexibility of choice with a strongly preferred alternative

3.3.12 vendor specific

something (e.g., a bit, field, code value) that is not defined by this standard

Note 1 to entry: Specification of the referenced item is determined by the SCSI device vendor and may be used differently in various implementations.

3.4 Editorial conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear.

Uppercase is used when referring to the name of a numeric value defined in this specification or a formal attribute possessed by an entity. When necessary for clarity, names of objects, procedure calls, arguments or discrete states are capitalized or set in bold type. Names of fields are identified using small capital letters (e.g., NACA bit).

Quantities having a defined numeric value are identified by large capital letters (e.g., CHECK CONDITION). Quantities having a discrete but unspecified value are identified using small capital letters. (e.g., TASK COMPLETE, indicates a quantity returned by the **Execute Command** procedure call). Such quantities are associated with an event or indication whose observable behavior or value is specific to a given implementation standard.

Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a) red (i.e., one of the following colors):
   A) crimson; or
   B) amber;
b) blue; or
c) green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1) top;
2) middle; and
3) bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a) or 1) entry).

If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

Notes and examples do not constitute any requirements for implementors and notes are numbered consecutively throughout this standard.

3.5 Numeric and character conventions

3.5.1 Numeric conventions

A binary number is represented in this standard by any sequence of digits comprised of only the Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 00010101 11001110b, 00010101_11001110b, 0 0101 1010b, or 0_0101_1010b).

A hexadecimal number is represented in this standard by any sequence of digits comprised of only the Arabic numerals 0 to 9 and/or the upper-case English letters A to F immediately followed by a lower-case h (e.g.,

FA23h). Underscores or spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this standard by any sequence of digits comprised of only the Arabic numerals 0 to 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

A range of numeric values is represented in this standard in the form “a to z”, where a is the first value included in the range, all values between a and z are included in the range, and z is the last value included in the range (e.g., the representation “0h to 3h” includes the values 0h, 1h, 2h, and 3h).

This standard uses the following conventions for representing decimal numbers:

a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
b) the thousands separator (i.e., separating groups of three digits in a portion of the number) is a space;
c) the thousands separator is used in both the integer portion and the fraction portion of a number; and
d) the decimal representation for a year is 1999 not 1 999.

Table 1 shows some examples of decimal numbers using various conventions.

Table 1 — Numbering conventions

French	English	This standard
0,6	0.6	0.6
3,141 592 65	3.14159265	3.141 592 65
1 000	1,000	1 000
1 323 462,95	1,323,462.95	1 323 462.95

3.5.2 Units of measure

This standard represents values using both decimal units of measure and binary units of measure. Values are represented by the following formats:

a) for values based on decimal units of measure:
   1) numerical value (e.g., 100);
   2) space; and
   3) prefix symbol and unit:
      1) decimal prefix symbol (e.g., M) (see table 2); and
      2) unit abbreviation (e.g., B);

   and

b) for values based on binary units of measure:
   1) numerical value (e.g., 1 024);
   2) space;
   3) prefix symbol and unit:
      1) binary prefix symbol (e.g., Gi) (see table 2); and
      2) unit abbreviation (e.g., b).

Table 2 compares the prefix, symbols, and power of the binary and decimal units.

Table 2 — Comparison of decimal prefixes and binary prefixes

Decimal			Binary		
Prefix name	**Prefix symbol**	**Power (base-10)**	**Prefix name**	**Prefix symbol**	**Power (base-2)**
kilo	k	10^3	kibi	Ki	2^{10}
mega	M	10^6	mebi	Mi	2^{20}
giga	G	10^9	gibi	Gi	2^{30}
tera	T	10^{12}	tebi	Ti	2^{40}
peta	P	10^{15}	pebi	Pi	2^{50}
exa	E	10^{18}	exbi	Ei	2^{60}
zetta	Z	10^{21}	zebi	Zi	2^{70}
yotta	Y	10^{24}	yobi	Yi	2^{80}

3.5.3 Byte encoded character strings conventions

When this standard requires one or more bytes to contain specific encoded characters, the specific characters are enclosed in single quotation marks. The single quotation marks identify the start and end of the characters that are required to be encoded but are not themselves to be encoded. The characters that are to be encoded are shown in the case that is to be encoded.

An ASCII space character (i.e., 20h) may be represented in a string by the character '¬' (e.g., 'SCSI¬device').

The encoded characters and the single quotation marks that enclose them are preceded by text that specifies the character encoding methodology and the number of characters required to be encoded.

EXAMPLE - Using the notation described in this subclause, stating that eleven ASCII characters 'SCSI device' are to be encoded would be the same writing out the following sequence of byte values: 53h 43h 53h 49h 20h 64h 65h 76h 69h 63h 65h.

4 General

4.1 Physical links and phys

A physical link is a set of four wires used as two differential signal pairs. One differential signal transmits in one direction while the other differential signal transmits in the opposite direction. Data may be transmitted in both directions simultaneously.

A physical phy contains a transceiver which electrically interfaces to a physical link, which attaches to another physical phy.

Phys are contained in ports (see SPL-4). Phys interface to a service delivery subsystem (see SAM-5).

Figure 3 shows two phys attached with a physical link.

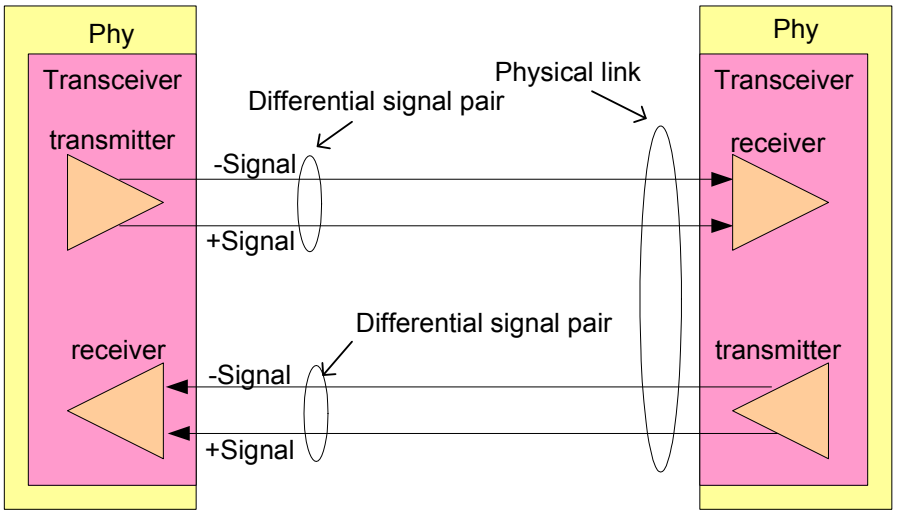


Figure 3 — Physical links and phys

An attached phy is the phy to which a phy is attached over a physical link.

The transceiver follows the electrical specifications defined in 5.8. Phys transmit and receive bits at physical link rates defined in 5.8. In the SAS dword mode the bits are parts of 10-bit characters (see SPL-4), which are parts of dwords (see SPL-4). In the SAS packet mode the bits are parts of 150-bit SPL packets (see SPL-4). The physical link rates supported by a phy are specified or indicated by the following fields in the SMP DISCOVER response (see SPL-4), the SMP PHY CONTROL request (see SPL-4), and the Phy Control and Discover mode page (see SPL-4):

a) the NEGOTIATED PHYSICAL LINK RATE field;
b) the HARDWARE MINIMUM PHYSICAL LINK RATE field;
c) the HARDWARE MAXIMUM PHYSICAL LINK RATE field;
d) the PROGRAMMED MINIMUM PHYSICAL LINK RATE field; and
e) the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field.

4.2 Phy test functions

Phy test functions (e.g., transmission of test patterns) are used for phy and interconnect characterization and diagnosis. The phy may be attached to test equipment while performing a phy test function. See SPL-4 for the optional mechanisms for invoking phy test function.

Each phy test function is optional.

If the phy test function requires a specific phy test pattern and/or phy test function physical link rate, then the mechanism for invoking the phy test function (see SPL-4) also specifies the phy test pattern and phy test function physical link rate.

5 Physical layer

5.1 Physical layer overview

The physical layer defines:

a) passive interconnect (e.g., connectors and cable assemblies); and
b) transmitter and receiver device electrical characteristics.

Within this standard, references to connector gender use the terms plug and receptacle as equivalent to the terms free and fixed, respectively, that may be used in the references that define the connectors. Fixed and free terminology has no relationship to the application of the connector.

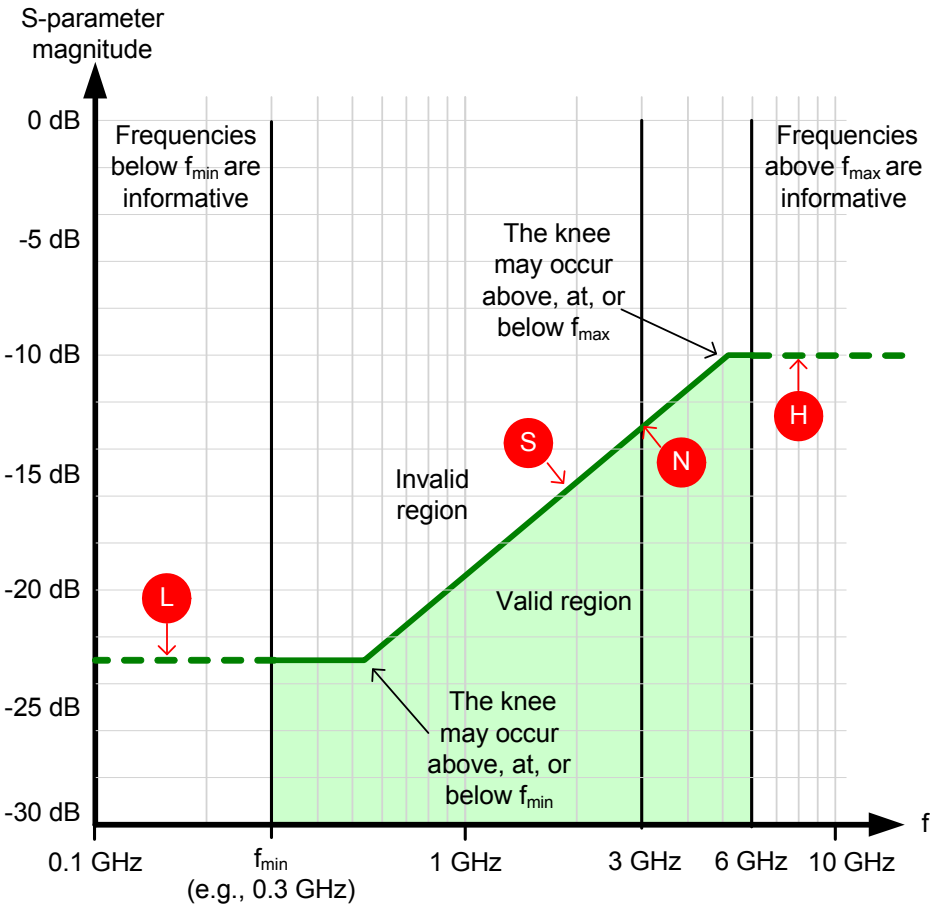
5.2 Conventions for defining maximum limits for S-parameters

The following values are specified by this standard to define the maximum limits for certain S-parameters (e.g., for cable assemblies and backplanes (see 5.5.3), transmitter devices (see 5.8.4.6.3), and receiver devices (see 5.8.5.7.2)):

a) L is the maximum value in dB at the low frequency asymptote;
b) N is the maximum value in dB at 3 GHz;
c) H is the maximum value in dB at the high frequency asymptote;
d) S is the slope in dB/decade;
e) f_{min} is the minimum frequency of interest; and
f) f_{max} is the maximum frequency of interest.

The frequencies at which L and H intersect the slope S may or may not be within the region of f_{min} to f_{max}. The frequency for N is based on the Nyquist at 6 Gbit/s.

Figure 4 shows the values in a graph.



Note: graph is not to scale

Figure 4 — Maximum limits for S-parameters definitions

5.3 Compliance points

5.3.1 Compliance points overview

A TxRx connection is the complete simplex signal path between the transmitter circuit and receiver circuit.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in conductive material.

This standard defines the electrical requirements of the signal at the following compliance points in a TxRx connection (see table 3):

a) for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT, IR, CT, and CR; and
b) for 12 Gbit/s IT, IR, CT, CR, ET, and ER.

Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

The TxRx connection characteristics are defined in 5.5.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this standard only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point.

Signal characteristics for compliance points are measured at physical positions called probe points in a test load (see 5.6). Measurements at the probe points in a test load approximate measurements at the compliance point in the actual TxRx connection. Some components in the test load may be de-embedded as described in F.5.

Table 3 — Compliance points

Compliance point	Type	Description
1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s compliance points		
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device , as measured at probe points in a test load attached with an internal connector.
IT_S	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device, as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT_S	inter-enclosure (i.e., cabinet)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.
12 Gbit/s only compliance points		
ET	transmitter circuit	The output signal from a transmitter circuit measured with the test load, TDCS, and TCCS de-embedded.
ER	receiver post equalization	A point defined at the output of the reference receiver device.

5.3.2 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s compliance points

The 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s TxRx connection includes the characteristics of the mated connectors at both the transmitter device and receiver device ends. One end of a TxRx connection is a IT_S compliance point or CT_S compliance point, and the other end of the TxRx connection is the corresponding IR compliance point or CR compliance point.

Figure 5 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s CT compliance points and CR compliance points using an external cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

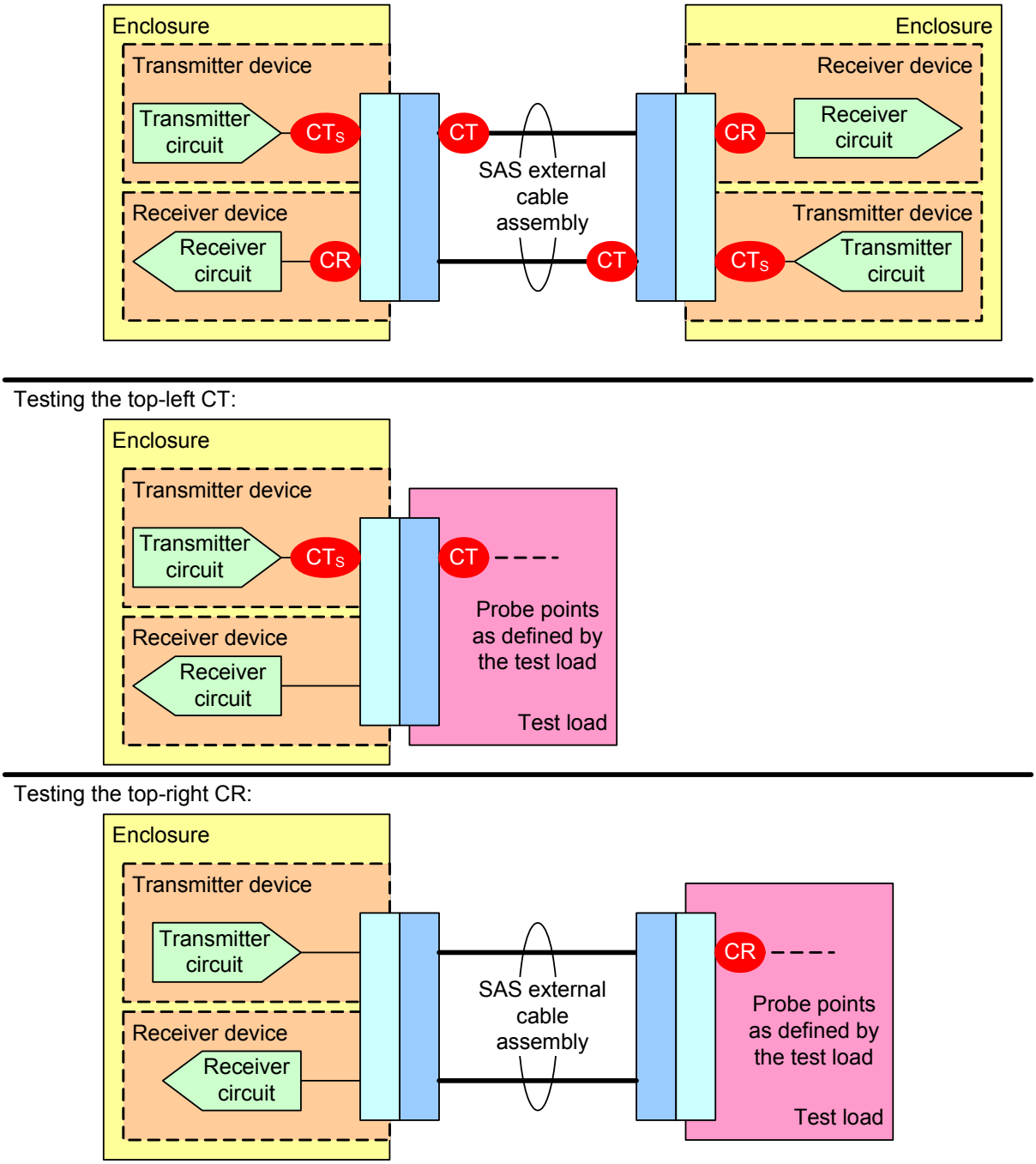


Figure 5 — 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s External cable assembly CT compliance points and CR compliance points

Figure 6 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that is not using SATA and shows how the compliance points are tested using test loads (see 5.6).

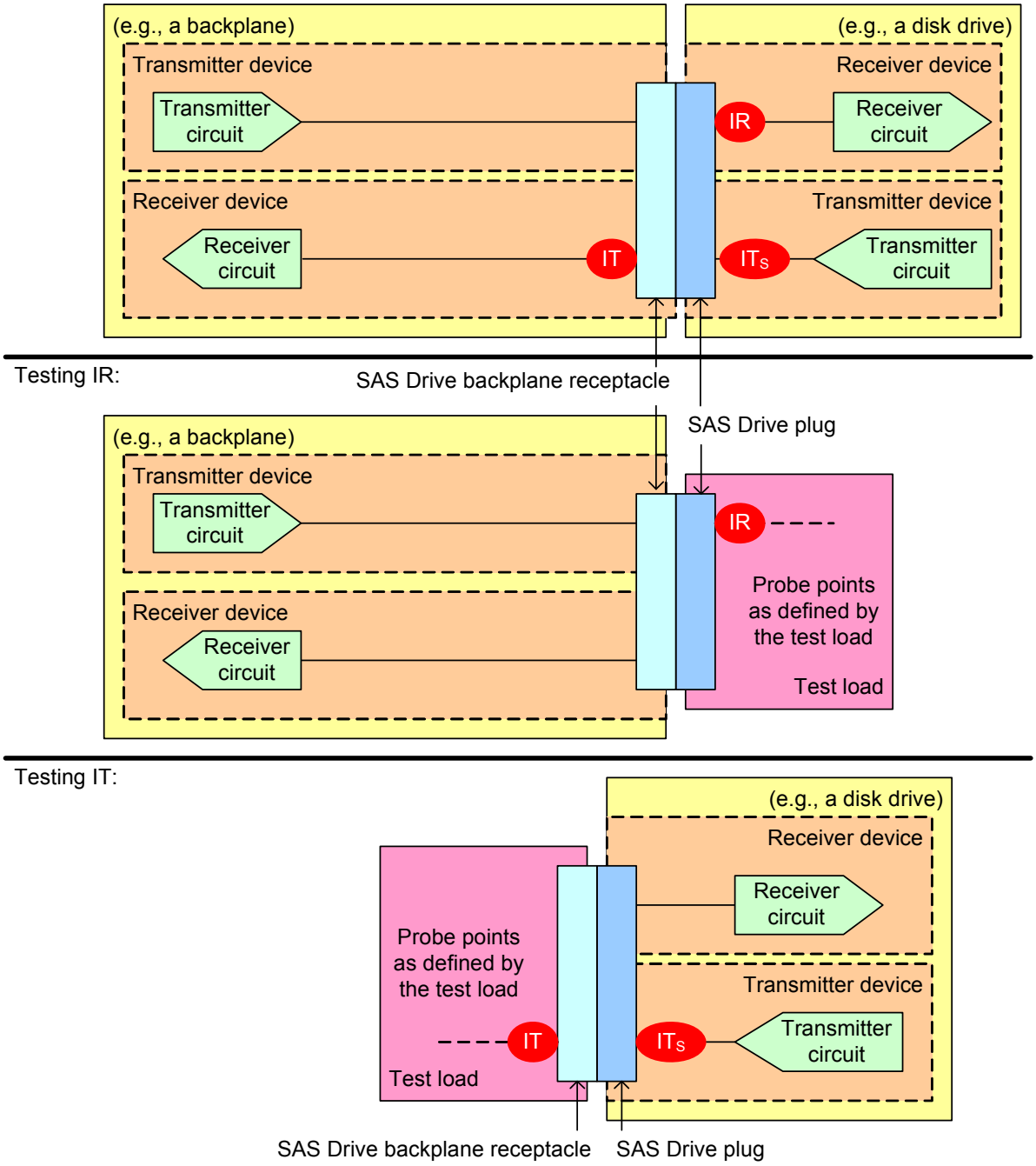


Figure 6 — Backplane with SAS Drive connector 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

If the backplane supports SATA, then there are no 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points or IR compliance points. SATA defines the signal characteristics that the SATA phy delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 7.

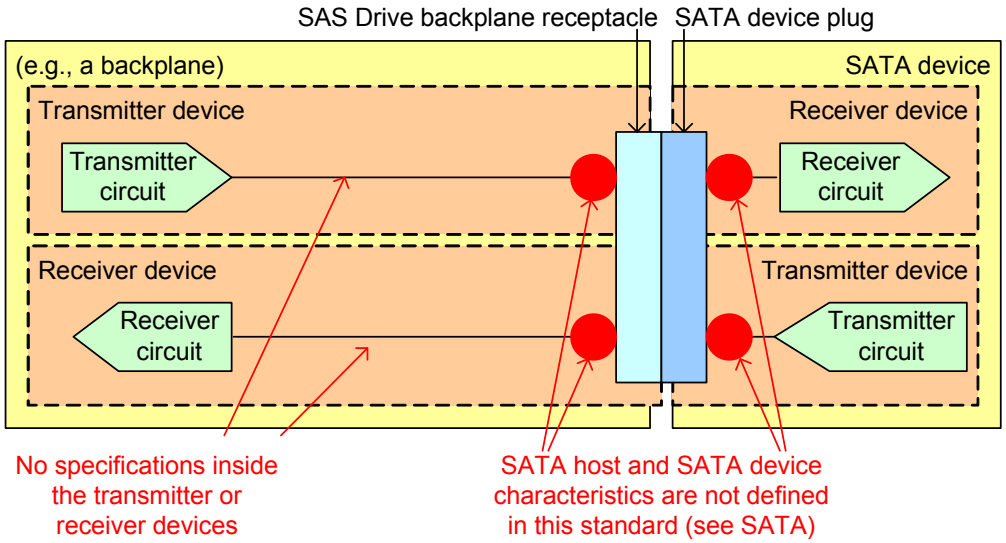


Figure 7 — Backplane with SAS Drive connector 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s compliance points with SATA phy attached

Figure 8 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

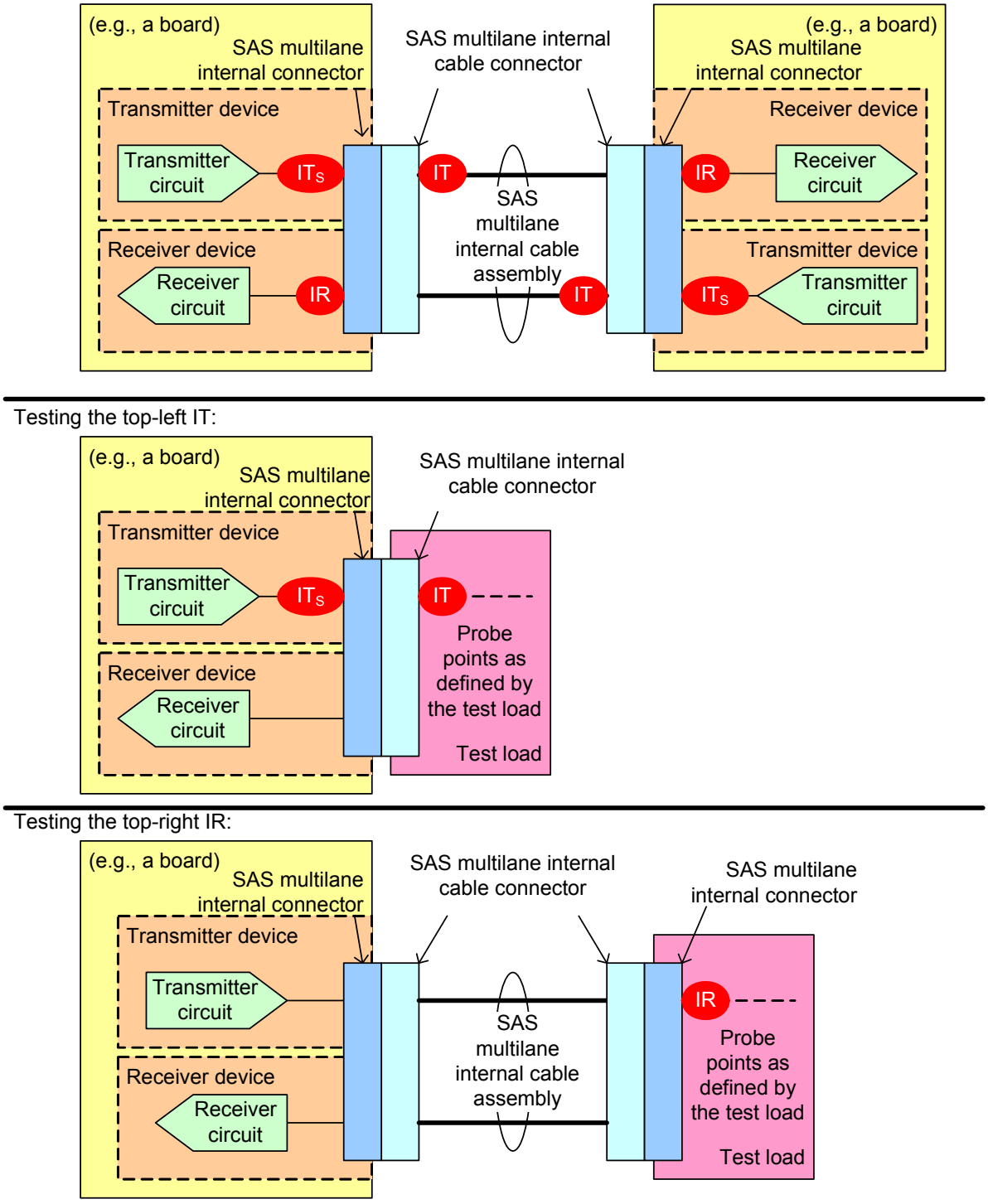


Figure 8 — SAS multilane internal cable assembly 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

Figure 9 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3), where the backplane is not attached to a SATA device, and shows how two of the compliance points are tested using test loads (see 5.6).

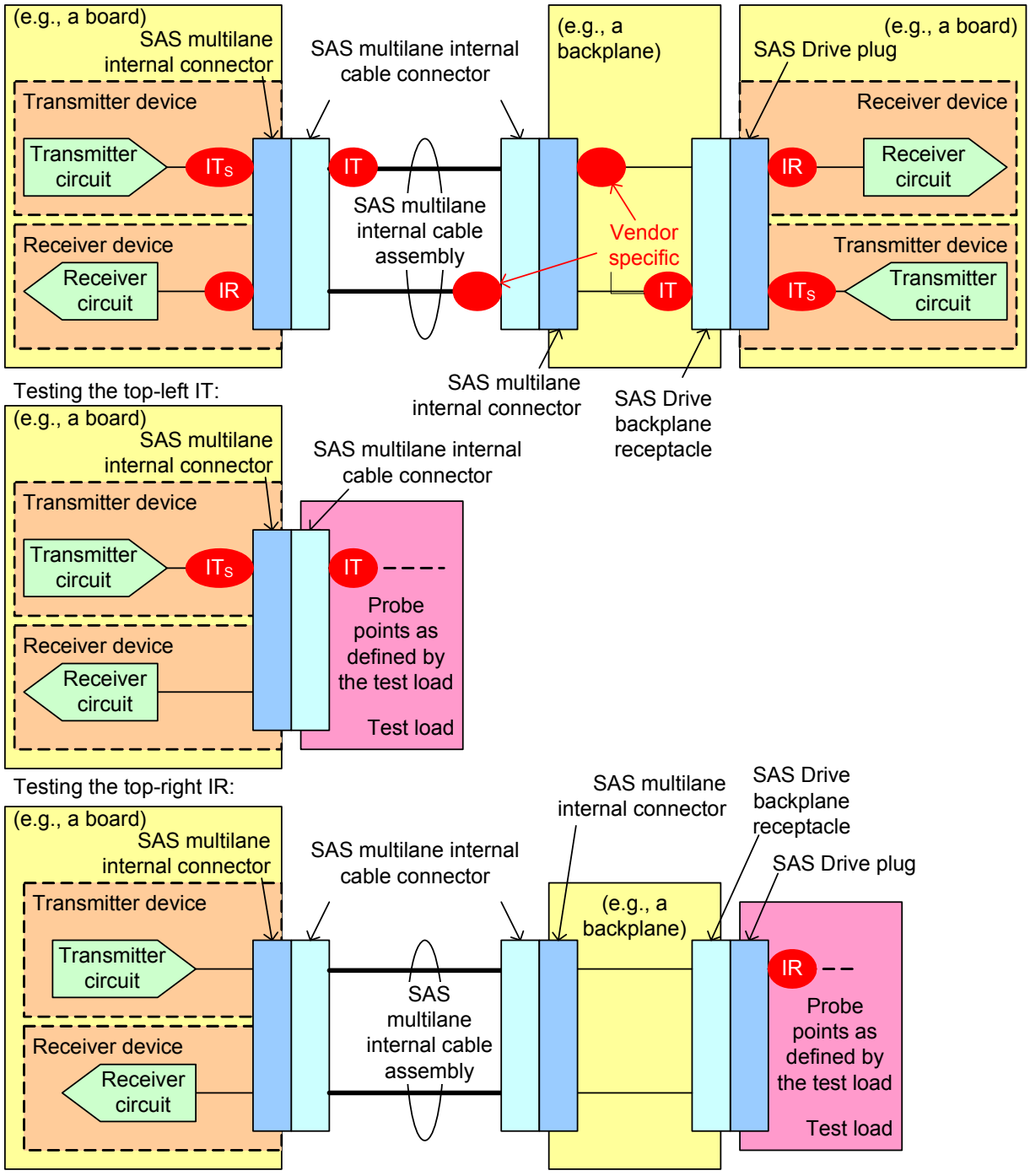


Figure 9 — SAS multilane internal cable assembly and backplane 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

Figure 10 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that supports being attached to a SATA device. There are no IT compliance points and IR compliance points at the SAS Drive backplane receptacle connector when a SATA device is attached. In that case, SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device. There are compliance points at the SAS multilane internal connector.

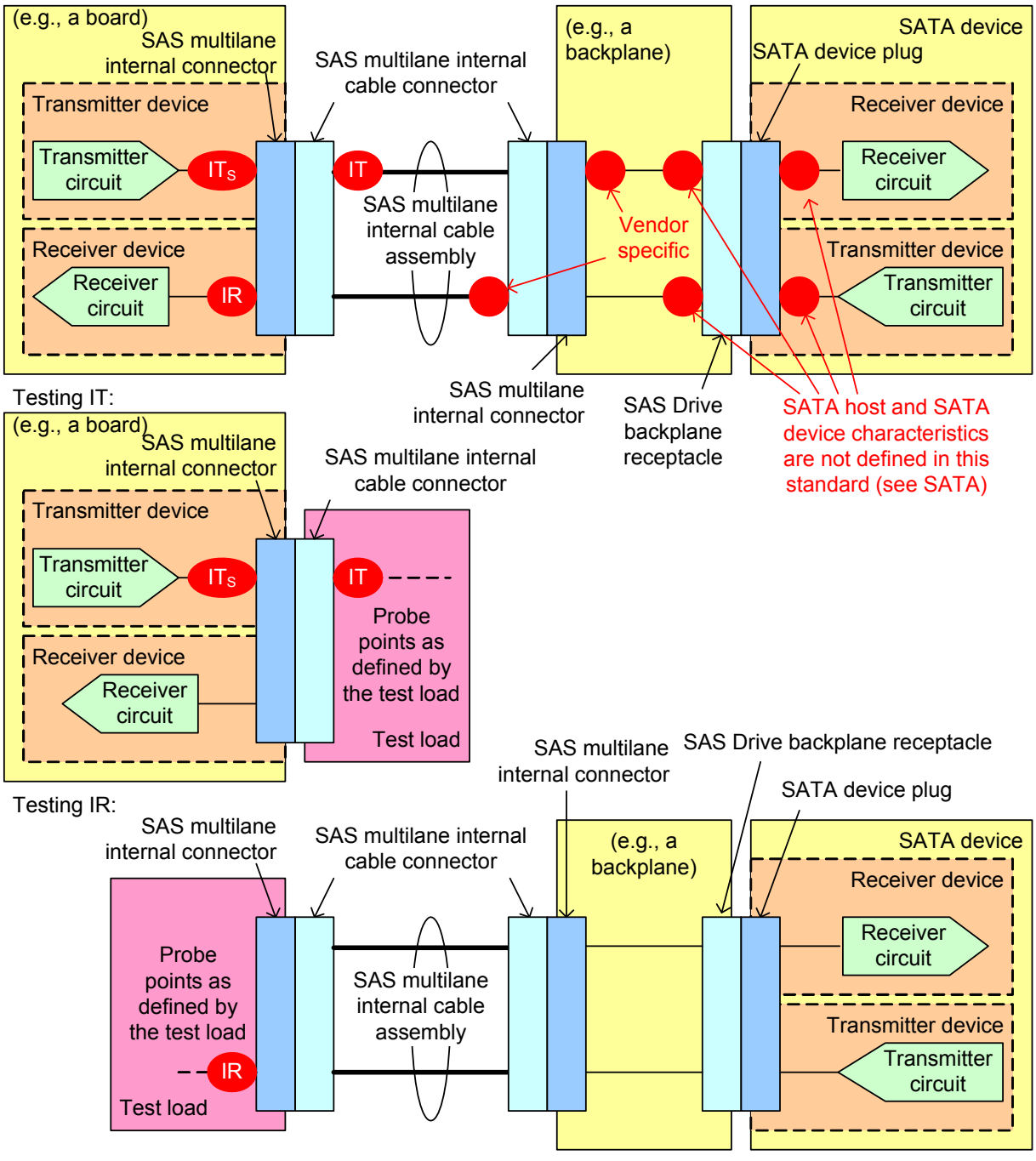


Figure 10 — SAS multilane internal cable assembly and backplane 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points with SATA device attached

Figure 11 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS Drive cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

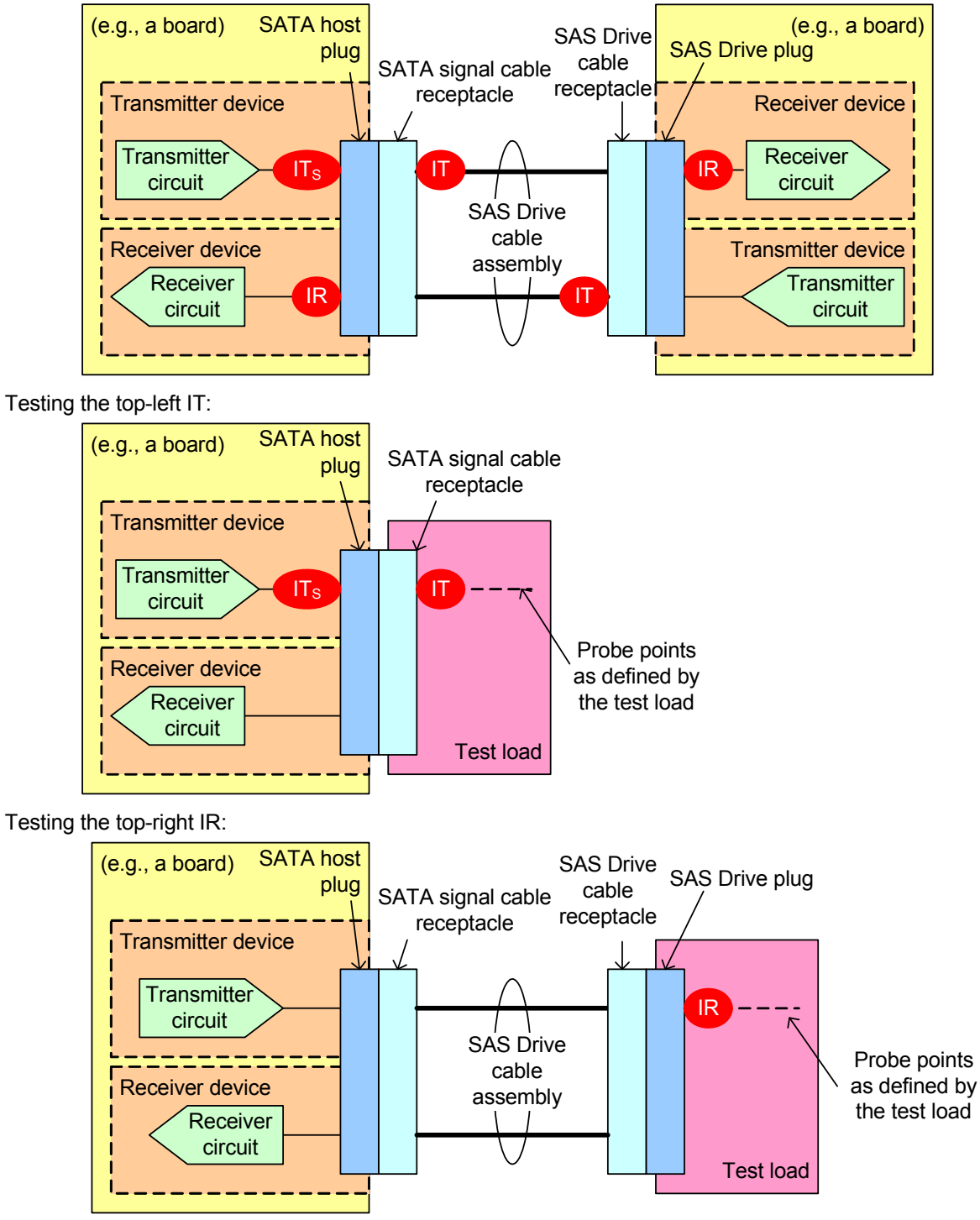


Figure 11 — SAS Drive cable assembly 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

5.3.3 12 Gbit/s compliance points

Figure 12 shows an example TxRx connection for trained 12 Gbit/s where PICS is the physical interconnect connection segment.

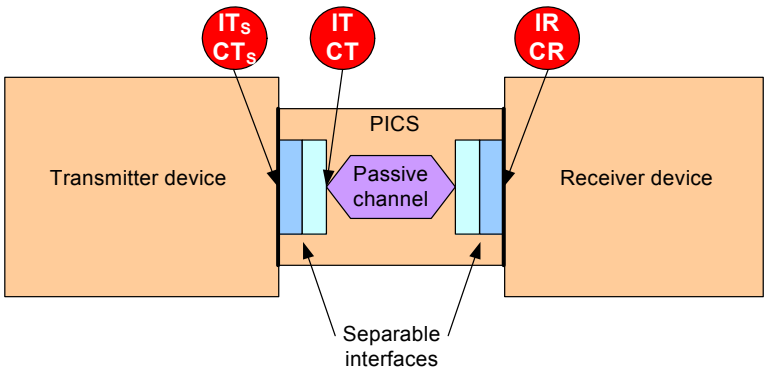


Figure 12 — 12 Gbit/s TxRx connection and compliance points

Figure 13 shows an example of a simulated TxRx connection for trained 12 Gbit/s where:

a) TDCS is the transmitter device TxRx connection segment;
b) TCCS is the transmitter circuit TxRx connection segment;
c) RDCS is the receiver device TxRx connection segment;
d) RCCS is the receiver circuit TxRx connection segment; and
e) PICS is the physical interconnect connection segment.

If simulations use a captured signal, then the TxRx connection segments located between ET and the compliance point used to capture the signal should be modeled as a single TxRx connection segment. End to end simulations (see 5.7.1) compute characteristics of the signal at ET and ER, using measurements taken:

a) at:
   A) IT;
   B) CT;
   C) IR; or
   D) CR;
   or
b) between:
   A) CT_S and CR; or
   B) IT_S and IR.

If the reference TxRx connection segment models provided for end to end simulations (see C.2) represent TxRx connection segments that are adjacent in the TxRx connection segment, then the TxRx connection segment models may be combined to simulate a single TxRx connection segment model.

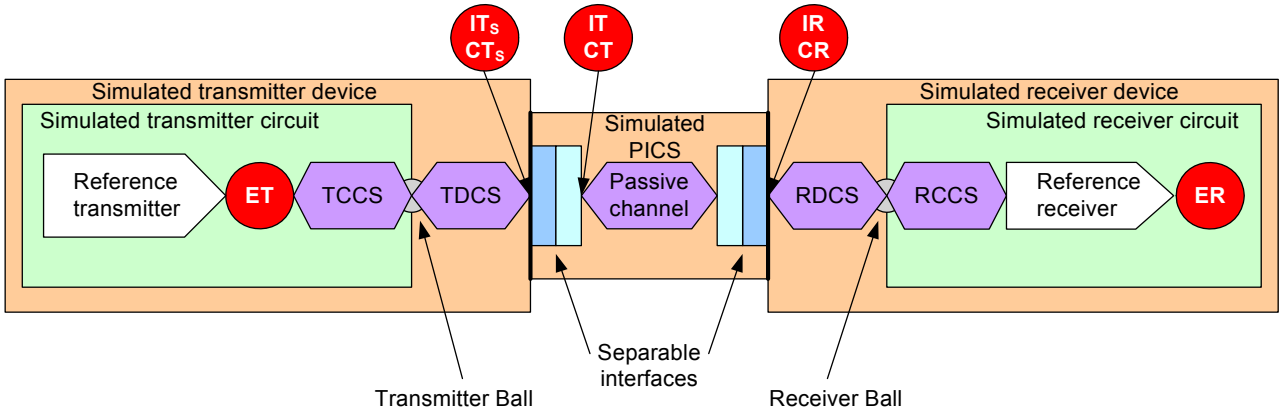


Figure 13 — Simulated 12 Gbit/s TxRx connection and compliance points

Figure 14 shows:

a) the locations of the CT_S compliance points and CR compliance points of an enclosure using an external cable connector; and
b) how the enclosure CT_S compliance point and the SAS active cable assembly for 12 Gbit/s CR compliance point are tested using test loads (see 5.6).

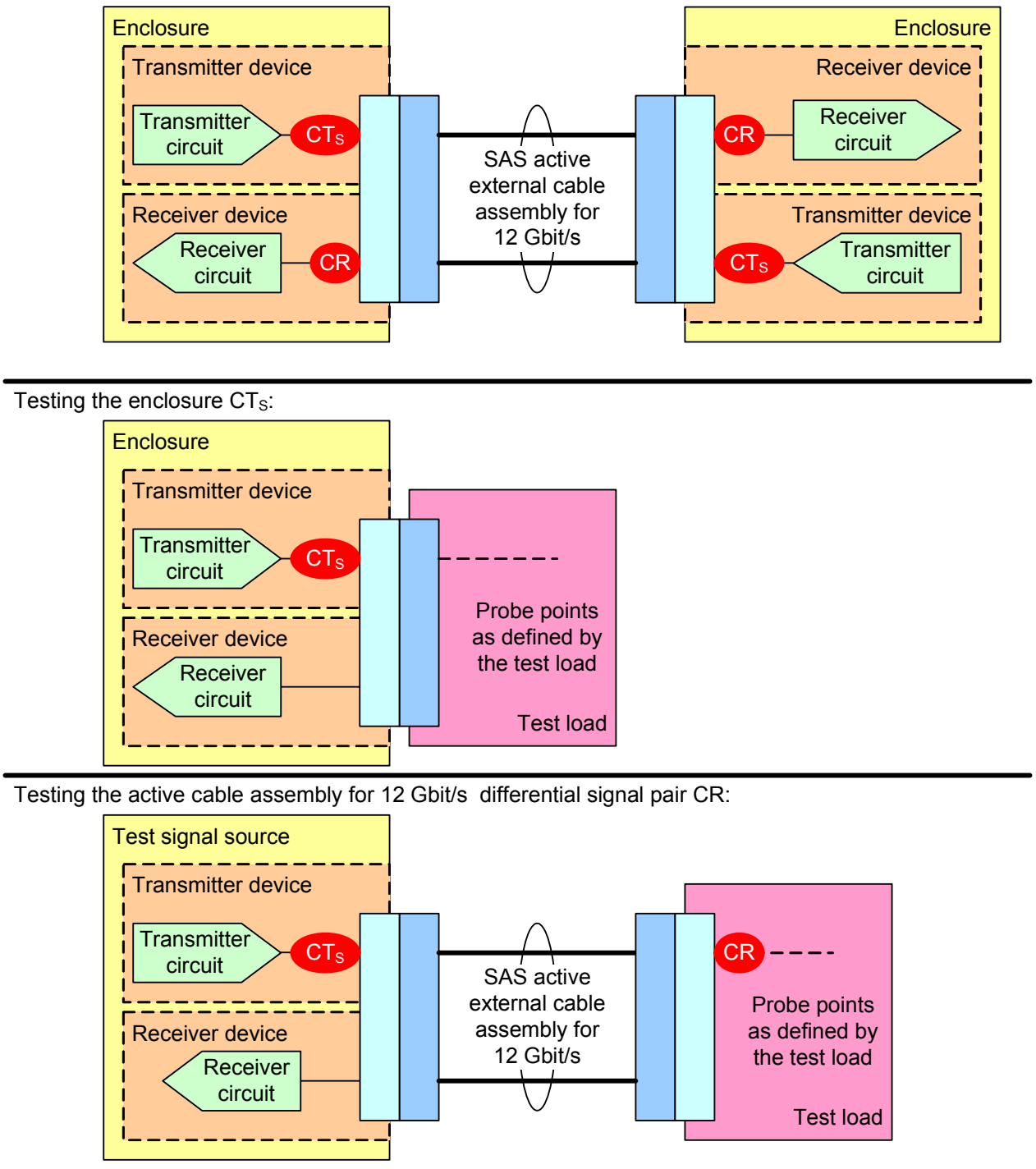


Figure 14 — 12 Gbit/s CT_S and CR compliance points

5.4 Interconnects

5.4.1 SATA connectors and cable assemblies

Figure 15 shows a representation of the connectors and cables defined by SATA. A SATA host is analogous to a SAS initiator device (see SPL-4) and a SATA device is analogous to a SAS target device (see SPL-4).

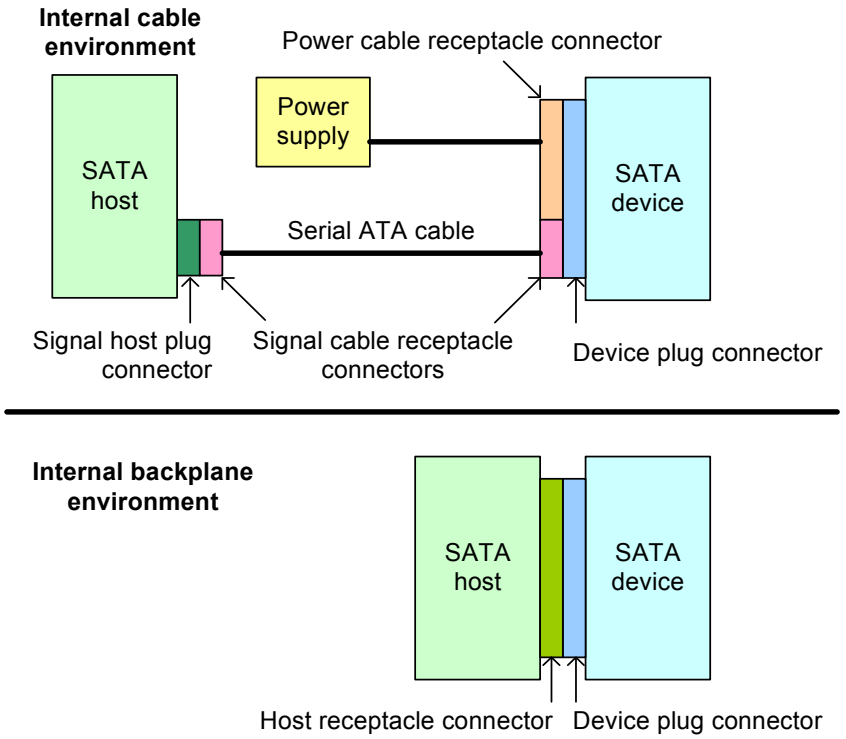


Figure 15 — SATA connectors and cables

5.4.2 SAS connectors and cables

This standard defines SAS Drive cable, SAS Drive backplane, SAS internal cable, and SAS external cable environments.

Figure 16 shows a representation of the SAS Drive cable environments.

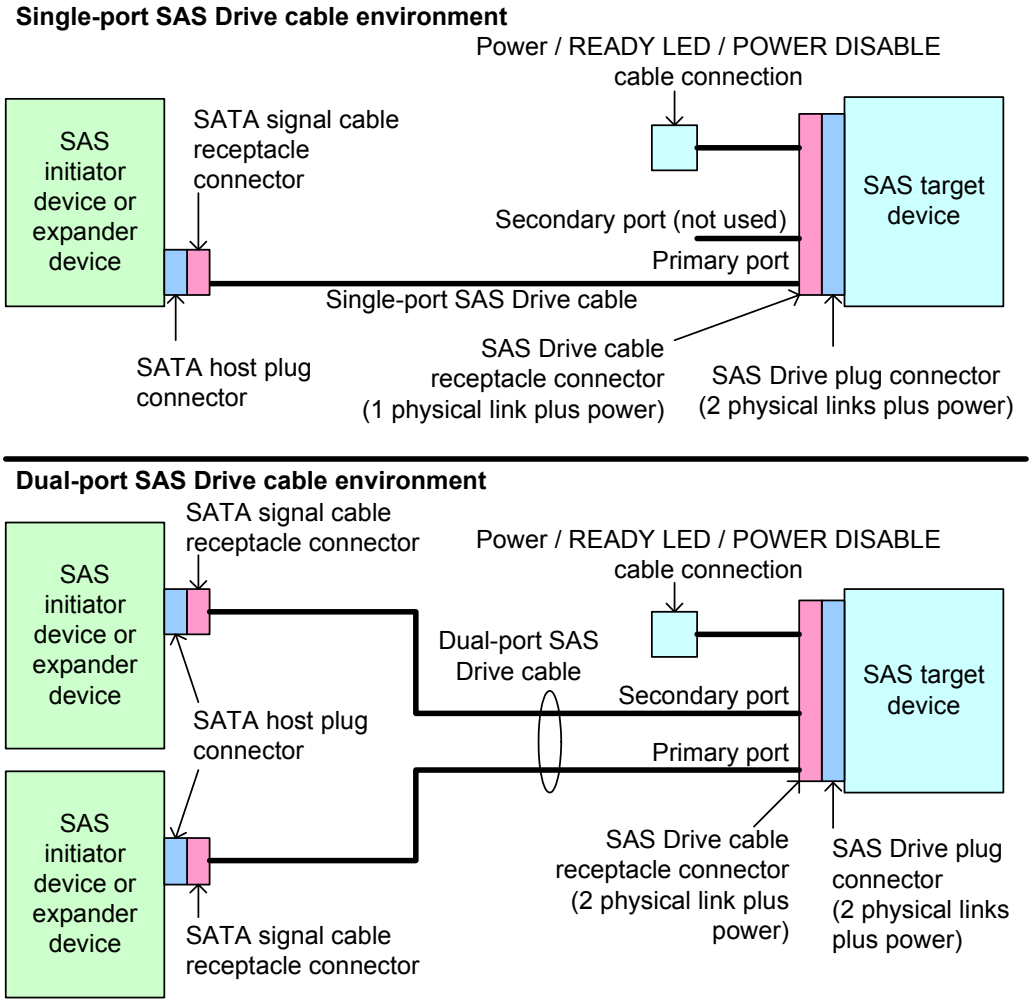


Figure 16 — SAS Drive cable environments

Figure 17 shows a representation of the SAS Drive backplane environment.

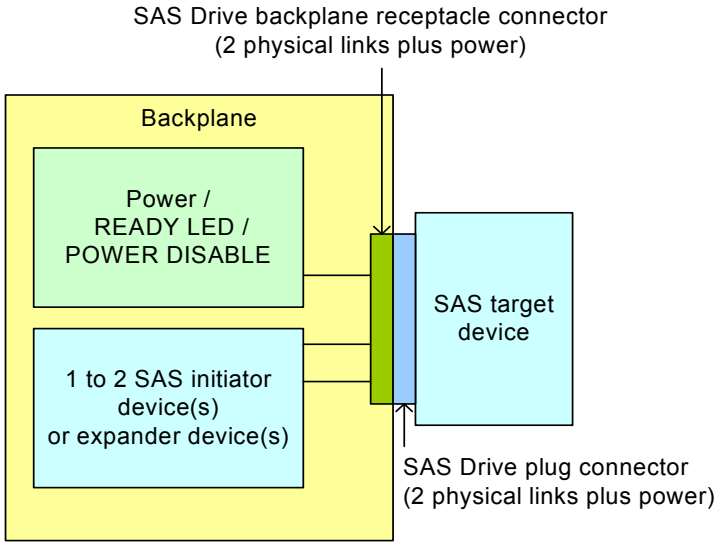


Figure 17 — SAS Drive backplane environment

Figure 18 shows a representation of the SAS external cable environment.

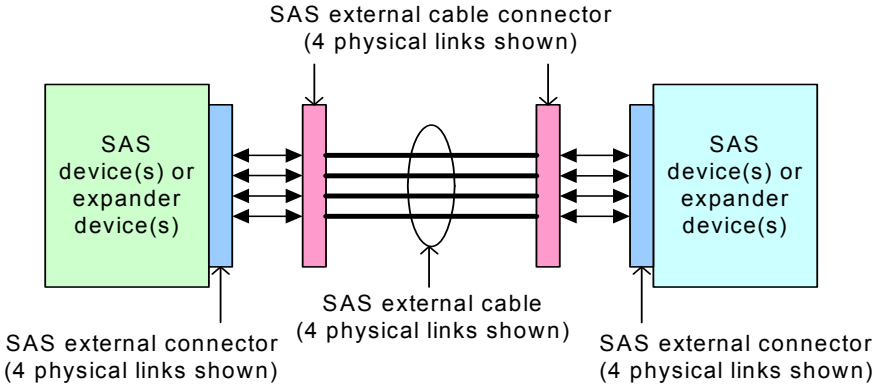


Figure 18 — SAS external cable environment

Figure 19 shows a representation of the SAS internal cable environment attaching a controller to a backplane using a SAS internal symmetric cable (see 5.4.4.1.2).

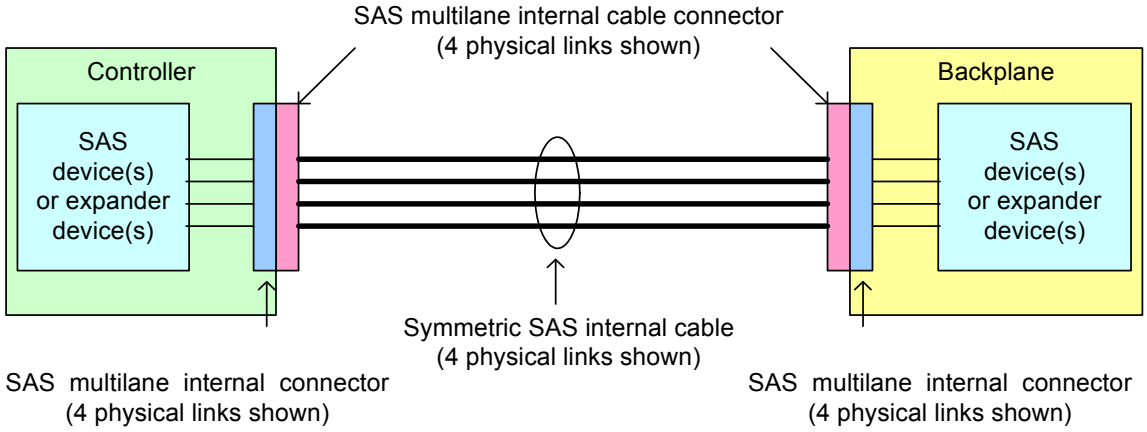


Figure 19 — SAS internal symmetric cable environment - controller to backplane

A SAS internal symmetric cable provides one to eight physical links, and may be used as any combination of wide links and narrow links (see SPL-4) using those physical links.

Figure 20 shows a representation of the SAS internal cable environment attaching a controller to a controller using a SAS internal symmetric cable (see 5.4.4.1.2).

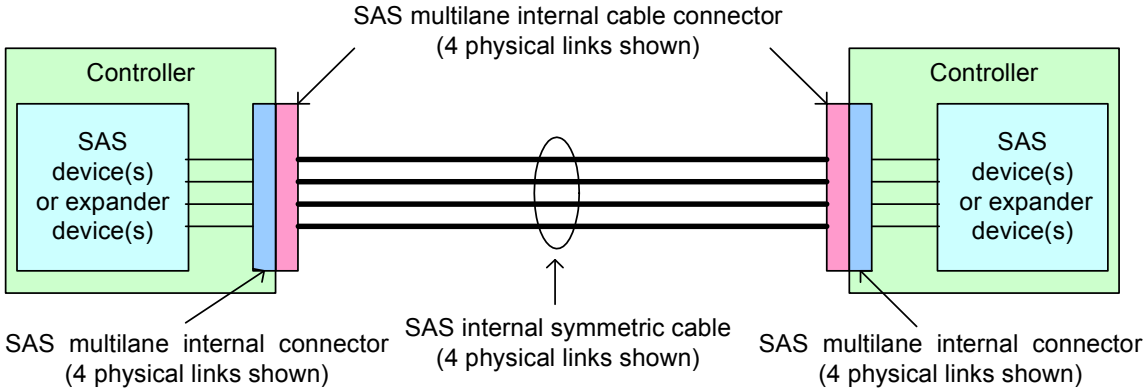


Figure 20 — SAS internal symmetric cable environment - controller to controller

Figure 21 shows a representation of the SAS internal cable environment using a SAS controller-based fanout cable (see 5.4.4.1.3).

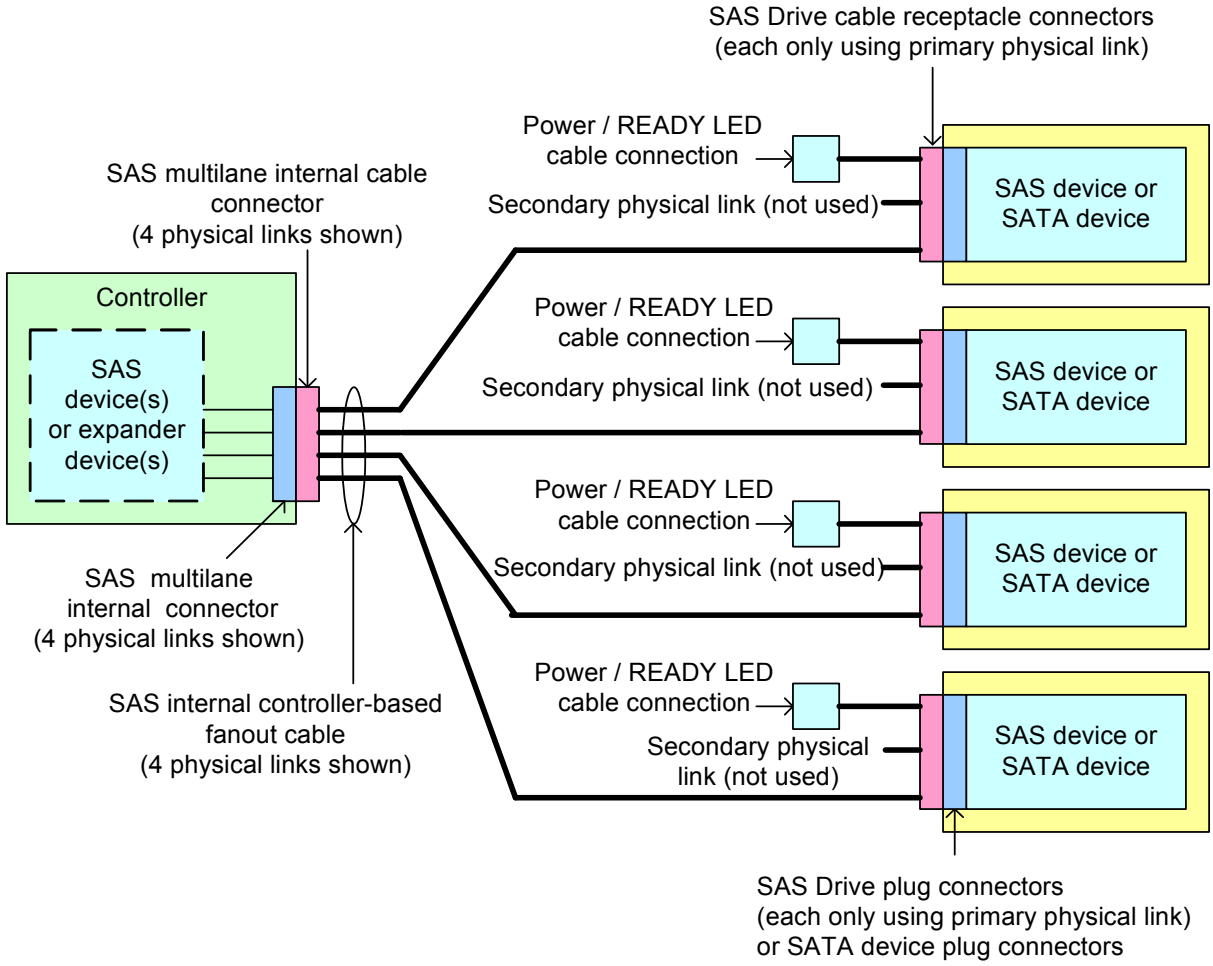


Figure 21 — SAS internal controller-based fanout cable environment

Figure 22 shows a representation of the SAS internal cable environment using a SAS backplane-based fanout cable (see 5.4.4.1.3).

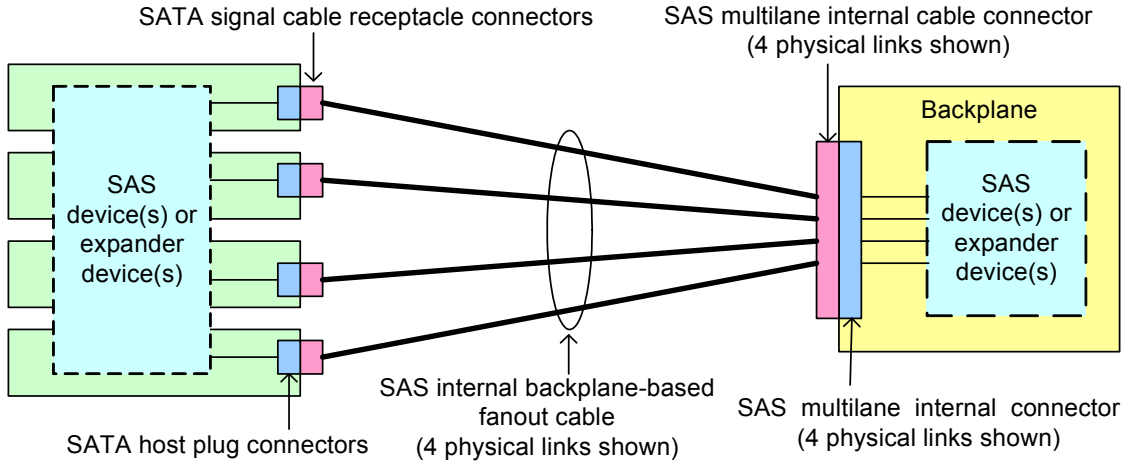


Figure 22 — SAS internal backplane-based fanout cable environment

5.4.3 Connectors

5.4.3.1 Connectors overview

Table 4 summarizes the connectors defined in this standard.

Table 4 — Connectors (part 1 of 4)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SATA internal connectors used by SAS					
SATA signal cable receptacle	1	SATA	SATA host plug	1	SATA
SATA host plug	1	SATA	SATA signal cable receptacle	1	SATA
SATA device plug	1	SATA	SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2
			SAS Drive backplane receptacle	2	5.4.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.3.1.7
			Multifunction 6X Unshielded receptacle connector	6 [a]	SFF-8639
Micro SATA device plug	1	SATA	Micro SAS receptacle	2	5.4.3.3.1.10
SAS internal connectors - SAS Drive connectors					
SAS Drive plug	2	5.4.3.3.1.1	SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2
			SAS Drive backplane receptacle	2	5.4.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.3.1.7
			Multifunction 6X Unshielded receptacle connector	6 [a]	SFF-8639
SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2	SAS Drive plug	2	5.4.3.3.1.1
			SAS MultiLink Drive plug	4	5.4.3.3.1.5
			SATA device plug	1	SATA
SAS Drive backplane receptacle	2	5.4.3.3.1.3	SAS Drive plug	2	5.4.3.3.1.1
			SAS MultiLink Drive plug	4	5.4.3.3.1.5
			SATA device plug	1	SATA

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 6 Gbit/s.

Table 4 — Connectors (part 2 of 4)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SAS Multilink Drive plug	4	5.4.3.3.1.5	SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2
			SAS Drive backplane receptacle	2	5.4.3.3.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.3.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.3.1.7
			Multifunction 6X Unshielded receptacle connector	6 [a]	SFF-8639
SAS MultiLink Drive cable receptacle	4	5.4.3.3.1.6	SAS Drive plug	2	5.4.3.3.1.1
			SAS MultiLink Drive plug	4	5.4.3.3.1.5
			SATA device plug	1	SATA
SAS MultiLink Drive backplane receptacle	4	5.4.3.3.1.7	SAS Drive plug	2	5.4.3.3.1.1
			SAS MultiLink Drive plug	4	5.4.3.3.1.5
			SATA device plug	1	SATA
Multifunction 12 Gb/s 6x Unshielded receptacle connector	6 [a]	SFF-8639	SAS Drive plug	2	5.4.3.3.1.1
			SAS MultiLink Drive plug	4	5.4.3.3.1.5
			SATA device plug	1	SATA
Micro SAS plug	2	5.4.3.3.1.9	Micro SAS receptacle	2	5.4.3.3.1.10
Micro SAS receptacle	2	5.4.3.3.1.10	Micro SAS plug	2	5.4.3.3.1.9
			Micro SATA device plug	1	SATA
SAS internal connectors - other					
SAS 4i cable receptacle		Obsolete			
SAS 4i plug		Obsolete			
Mini SAS 4i cable plug	4	5.4.3.3.2.1	Mini SAS 4i receptacle	4	5.4.3.3.2.2
Mini SAS 4i receptacle	4	5.4.3.3.2.2	Mini SAS 4i cable plug	4	5.4.3.3.2.1
Mini SAS HD 4i cable plug	4	5.4.3.3.3.1	Mini SAS HD 4i receptacle	4	5.4.3.3.3.3
			Mini SAS HD 8i receptacle	8	5.4.3.3.3.4
			Mini SAS HD 16i receptacle	16	5.4.3.3.3.5
Mini SAS HD 8i cable plug	8	5.4.3.3.3.2	Mini SAS HD 8i receptacle	8	5.4.3.3.3.4
			Mini SAS HD 16i receptacle	16	5.4.3.3.3.5
Mini SAS HD 4i receptacle	4	5.4.3.3.3.3	Mini SAS HD 4i cable plug	4	5.4.3.3.3.1
Mini SAS HD 8i receptacle	8	5.4.3.3.3.4	Mini SAS HD 4i cable plug	4	5.4.3.3.3.1
			Mini SAS HD 8i cable plug	8	5.4.3.3.3.2

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 6 Gbit/s.

Table 4 — Connectors (part 3 of 4)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
Mini SAS HD 16i receptacle	16	5.4.3.3.3.5	Mini SAS HD 4i cable plug	4	5.4.3.3.3.1
			Mini SAS HD 8i cable plug	8	5.4.3.3.3.2
SAS SlimLine 4i cable plug	4	5.4.3.3.4.1	SAS SlimLine 4i receptacle	4	5.4.3.3.4.3
SAS SlimLine 4i receptacle	4	5.4.3.3.4.3	SAS SlimLine 4i cable plug	4	5.4.3.3.4.1
SAS SlimLine 8i cable plug	8	5.4.3.3.4.2	SAS SlimLine 8i receptacle	8	5.4.3.3.4.4
SAS SlimLine 8i receptacle	8	5.4.3.3.4.4	SAS SlimLine 8i cable plug	8	5.4.3.3.4.2
SAS MiniLink 4i cable plug	4	5.4.3.3.5.1	SAS MiniLink 4i receptacle	4	5.4.3.3.5.3
SAS MiniLink 4i receptacle	4	5.4.3.3.5.3	SAS MiniLink 4i cable plug	4	5.4.3.3.5.1
SAS MiniLink 8i cable plug	8	5.4.3.3.5.2	SAS MiniLink 8i receptacle	8	5.4.3.3.5.4
SAS MiniLink 8i receptacle	8	5.4.3.3.5.4	SAS MiniLink 8i cable plug	8	5.4.3.3.5.2
SAS external connectors					
Mini SAS 4x cable plug [b]	4	5.4.3.4.1.1	Mini SAS 4x receptacle [b] Mini SAS 4x active receptacle [b]	4	5.4.3.4.1.2
Mini SAS 4x receptacle [b]	4	5.4.3.4.1.2	Mini SAS 4x cable plug [b]	4	5.4.3.4.1.1
Mini SAS 4x active cable assembly plug [b]	4	5.4.3.4.1.1	Mini SAS 4x active receptacle [b]	4	5.4.3.4.1.2
Mini SAS 4x active receptacle [b]	4	5.4.3.4.1.2	Mini SAS 4x cable plug [b] Mini SAS 4x active cable assembly plug [b]	4	5.4.3.4.1.1
Mini SAS HD 4x cable plug	4	5.4.3.4.2.1	Mini SAS HD 4x receptacle	4	5.4.3.4.2.3
			Mini SAS HD 8x receptacle	8	5.4.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.4.2.5
Mini SAS HD 8x cable plug	8	5.4.3.4.2.2	Mini SAS HD 8x receptacle	8	5.4.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.4.2.5
Mini SAS HD 4x receptacle	4	5.4.3.4.2.3	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
Mini SAS HD 8x receptacle	8	5.4.3.4.2.4	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.4.2.2
Mini SAS HD 16x receptacle	16	5.4.3.4.2.5	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.4.2.2

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 6 Gbit/s.

Table 4 — Connectors (part 4 of 4)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
QSFP+ cable plug	4	5.4.3.4.3.1	QSFP+ receptacle	4	5.4.3.4.3.2
QSFP+ receptacle	4	5.4.3.4.3.2	QSFP+ cable plug	4	5.4.3.4.3.1

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 6 Gbit/s.

A SAS icon (see annex I.1) should be placed on or near each SAS connector.

5.4.3.2 Connector categories

The relationship between connector categories and connectors is shown in table 5.

Table 5 — Connector categories

Connector category	Connectors in category
Unmanaged passive	All connectors listed in table 4 (see 5.4.3.1) that are not listed elsewhere in this table
Unmanaged active	Mini SAS 4x active connectors (see 5.4.3.4.1)
Managed	Mini SAS HD external connectors (see 5.4.3.4.2) QSFP+ connectors (see 5.4.3.4.3)

5.4.3.3 SAS internal connectors

5.4.3.3.1 SAS Drive connectors

5.4.3.3.1.1 SAS Drive plug connector

The SAS Drive plug connector mechanical interface is the Device Free (Plug) connector defined in SFF-8482. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 23 shows the SAS Drive plug connector.

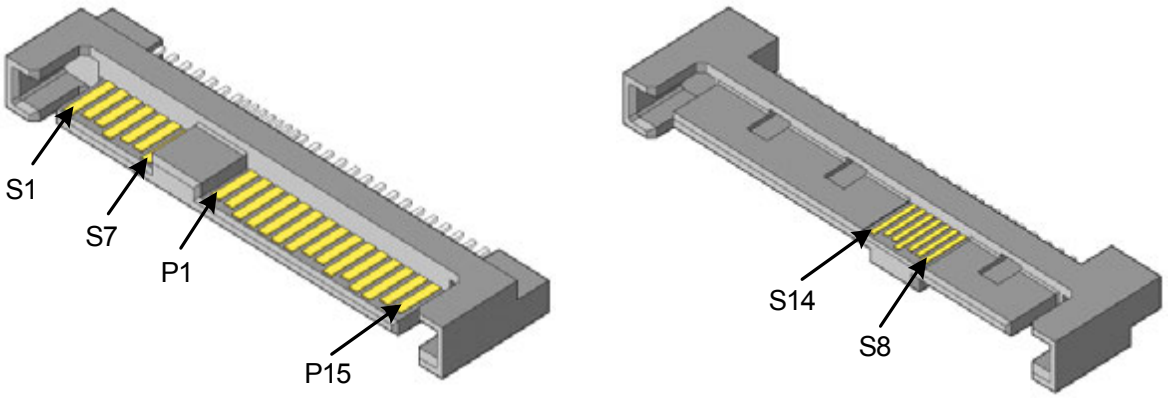


Figure 23 — SAS Drive plug connector

Table 6 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive plug connector.

5.4.3.3.1.2 SAS Drive cable receptacle connector

The SAS Drive cable receptacle connector mechanical interface is the Internal Cable Fixed (Receptacle) connector defined in SFF-8482. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

The single-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and only the primary physical link; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 24 shows the single-port version of the SAS Drive cable receptacle connector.

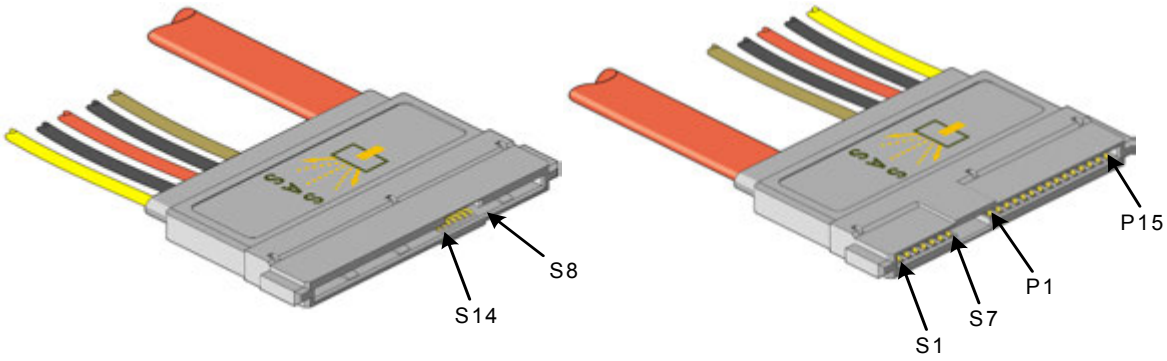


Figure 24 — Single-port SAS Drive cable receptacle connector

The dual-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links;
c) a SAS MultiLink Drive plug connector, providing contact for the power pins and both the primary and secondary physical links; or
d) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 25 shows the dual-port version of the SAS Drive cable receptacle connector.

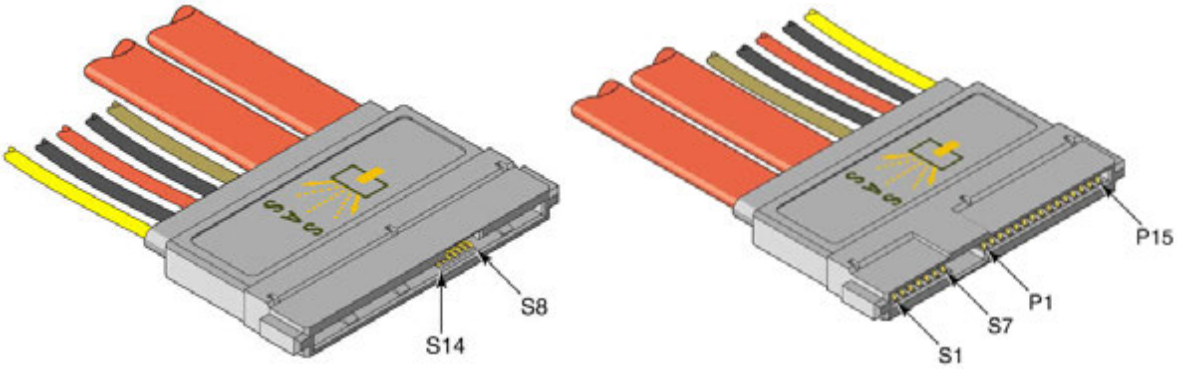


Figure 25 — Dual-port SAS Drive cable receptacle connector

Table 6 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive cable receptacle connector. The secondary physical link (i.e., pins S8 through S14) is not supported by the single-port internal cable receptacle.

5.4.3.3.1.3 SAS Drive backplane receptacle connector

The SAS Drive backplane receptacle connector mechanical interface is the Backplane Fixed (Receptacle) connector defined in SFF-8482. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

The SAS Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links;
c) a SAS MultiLink Drive plug connector, providing contact for the power pins and both primary and secondary physical links; or
d) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 26 shows the SAS Drive backplane receptacle connector.

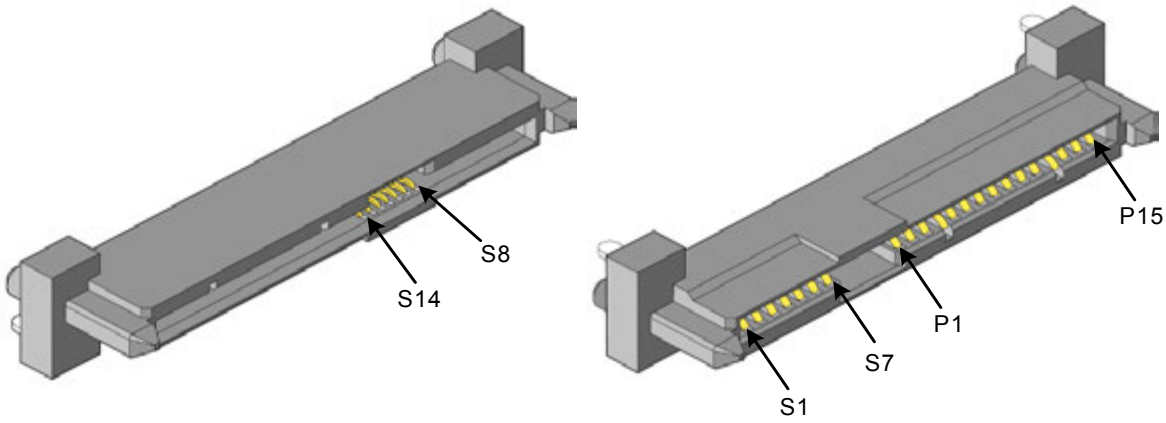


Figure 26 — SAS Drive backplane receptacle connector

Table 6 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive backplane receptacle connector.

5.4.3.3.1.4 SAS Drive connector pin assignments

Table 6 defines the SAS target device pin assignments for the SAS Drive plug connector (see 5.4.3.3.1.1), the SAS Drive cable receptacle connector (see 5.4.3.3.1.2), and the SAS Drive backplane receptacle connector (see 5.4.3.3.1.3). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

SAS Drive plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a SATA device plug connector (see SATA).

Table 6 — SAS Drive connector pin assignments (part 1 of 2)

Segment	Pin [a]	Backplane receptacle [a]	SAS Drive plug and SAS Drive cable receptacle [a]
Primary signal segment	S1	SIGNAL GROUND	
	S2	TP+	RP+
	S3	TP-	RP-
	S4	SIGNAL GROUND	
	S5	RP-	TP-
	S6	RP+	TP+
	S7	SIGNAL GROUND	
Secondary signal segment [b]	S8	SIGNAL GROUND	
	S9	TS+	RS+
	S10	TS-	RS-
	S11	SIGNAL GROUND	
	S12	RS-	TS-
	S13	RS+	TS+
	S14	SIGNAL GROUND	

[a] Devices supporting other interfaces have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[b] S8 through S14 are not connected on single-port implementations.
[c] SAS drive backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_5 and V_{12}. SAS Drive plug connectors receive V_5 and V_{12}.
[d] Behind a SAS Drive plug connector, P1 and P2 are only connected to each other.
[e] SAS devices (see SPL-4) with SAS Drive plug connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together. SAS Drive backplane connectors and SAS Drive cable receptacle connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[f] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors (see 5.4.3.3.1.7), and SAS MultiLink Drive cable receptacle connectors (see 5.4.3.3.1.6) are beyond the scope of this specification.
[g] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[h] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[i] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-4. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 6 — SAS Drive connector pin assignments (part 2 of 2)

Segment	Pin [a]	Backplane receptacle [a]	SAS Drive plug and SAS Drive cable receptacle [a]
Power segment [c]	P1	Vendor specific	See [d] [e]
	P2	Vendor specific	See [d] [e]
	P3	Vendor specific or POWER DISABLE [e] [g]	POWER DISABLE [e] [g]
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [h]	
	P8	V_5 [h]	
	P9	V_5 [h]	
	P10	GROUND	
	P11	READY LED [i]	
	P12	GROUND	
	P13	V_{12}, precharge [h]	
	P14	V_{12} [h]	
	P15	V_{12} [h]	

[a] Devices supporting other interfaces have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[b] S8 through S14 are not connected on single-port implementations.
[c] SAS drive backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_5 and V_{12}. SAS Drive plug connectors receive V_5 and V_{12}.
[d] Behind a SAS Drive plug connector, P1 and P2 are only connected to each other.
[e] SAS devices (see SPL-4) with SAS Drive plug connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together. SAS Drive backplane connectors and SAS Drive cable receptacle connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[f] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors (see 5.4.3.3.1.7), and SAS MultiLink Drive cable receptacle connectors (see 5.4.3.3.1.6) are beyond the scope of this specification.
[g] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[h] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[i] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-4. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.4.3.3.1.5 SAS MultiLink Drive plug connector

The SAS MultiLink Drive plug connector mechanical interface is the Device free (plug) connector defined in SFF-8630. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 27 shows the SAS MultiLink Drive plug connector

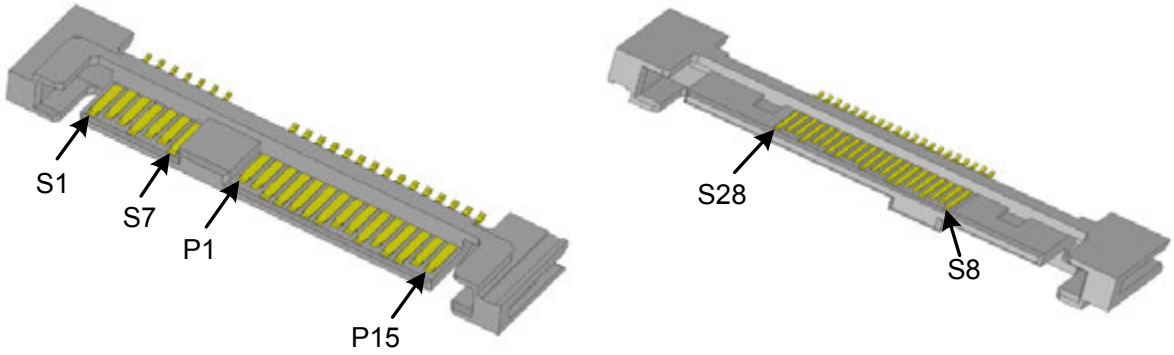


Figure 27 — SAS MultLink Drive plug connector

Table 7 (see 5.4.3.3.1.8) defines the pin assignments for the SAS MultiLink Drive plug connector.

5.4.3.3.1.6 SAS MultiLink Drive cable receptacle connector

The SAS MultiLink Drive cable receptacle connector mechanical interface is the Internal Cable Fixed (Receptacle) connector defined in SFF-8630. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

The SAS MultiLink Drive cable receptacle attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 28 shows the SAS MultiLink Drive cable receptacle connector.

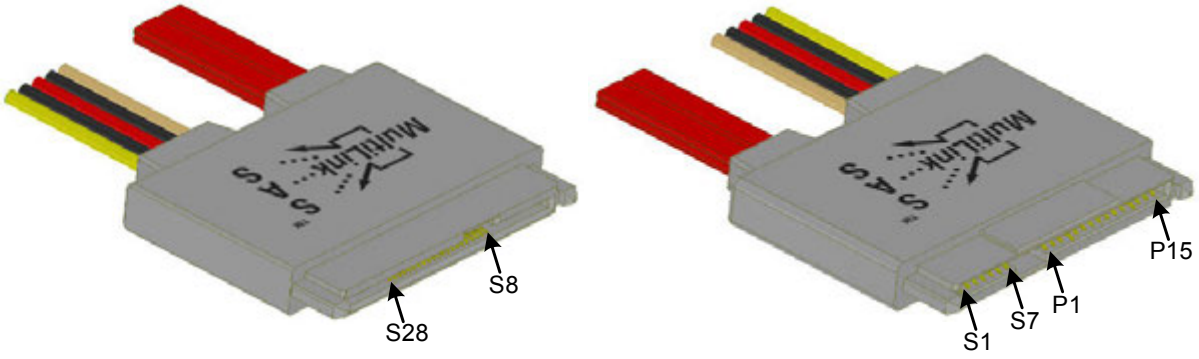


Figure 28 — SAS MultiLink Drive cable receptacle connector

Table 7 (see 5.4.3.3.1.4) defines the pin assignments for the SAS MultiLink Drive cable receptacle connector.

5.4.3.3.1.7 SAS MultiLink Drive backplane receptacle connector

The SAS MultiLink Drive backplane receptacle connector mechanical interface is the Backplane Fixed (Receptacle) connector defined in SFF-8630. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J.

The SAS MultiLink Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 29 shows the SAS MultiLink Drive backplane receptacle connector.

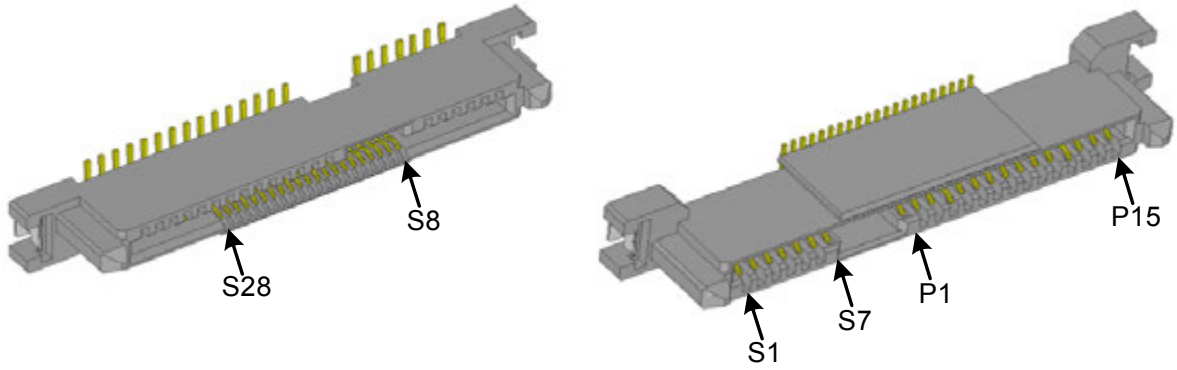


Figure 29 — SAS MultiLink Drive backplane receptacle connector

Table 7 (see 5.4.3.3.1.8) defines the pin assignments for the SAS MultiLink Drive backplane receptacle connector.

5.4.3.3.1.8 SAS MultiLink Drive connector pin assignments

Table 7 defines the SAS target device pin assignments for the SAS MultiLink Drive plug connector (see 5.4.3.3.1.5), the SAS MultiLink Drive cable receptacle connector (see 5.4.3.3.1.6), and the SAS MultiLink Drive backplane receptacle connector (see 5.4.3.3.1.7). TX0+, TX0-, RX0+, and RX0- are used by the signal segment 0 physical link. TX1+, TX1-, RX1+, and RX1- are used by the signal segment 1 physical link, if any. TX2+, TX2-, RX2+, and RX2- are used by the signal segment 2 physical link, if any. TX3+, TX3-, RX3+, and RX3- are used by the signal segment 3 physical link, if any.

Table 7 — SAS MultiLink connector pin assignments (part 1 of 3)

Segment	Pin [a]	SAS MultiLink Drive backplane receptacle [a]	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle [a]
Signal segment 0	S1	SIGNAL GROUND	
	S2	TX 0+	RX 0+
	S3	TX 0-	RX 0-
	S4	SIGNAL GROUND	
	S5	RX 0-	TX 0-
	S6	RX 0+	TX 0+
	S7	SIGNAL GROUND	
Signal segment 1 [b]	S8	SIGNAL GROUND	
	S9	TX 1+	RX 1+
	S10	TX 1-	RX 1-
	S11	SIGNAL GROUND	
	S12	RX 1-	TX 1-
	S13	RX 1+	TX 1+
	S14	SIGNAL GROUND	
	S15	RESERVED	

[a] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[b] S8 through S28 are not connected on single-port implementations.
[c] S16 through S28 are not connected on dual-port implementations.
[d] S~~22~~23 through S28 are not connected on triple-port implementations.
[e] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[f] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[g] SAS devices (see SPL-4) with SAS Drive plug connectors (see 5.4.3.3.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[h] SAS Drive backplane connectors (see 5.4.3.3.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.3.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[i] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-4. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 7 — SAS MultiLink connector pin assignments (part 2 of 3)

Segment	Pin [a]	SAS MultiLink Drive backplane receptacle [a]	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle [a]
Signal segment 2 [b] [c]	S16	SIGNAL GROUND	
	S17	TX 2+	RX 2+
	S18	TX 2-	RX 2-
	S19	SIGNAL GROUND	
	S20	RX 2-	TX 2-
	S21	RX 2+	TX 2+
	S22	SIGNAL GROUND	
Signal segment 3 [b] [c] [d]	S23	TX 3+	RX 3+
	S24	TX 3-	RX 3-
	S25	SIGNAL GROUND	
	S26	RX 3-	TX 3-
	S27	RX 3+	TX 3+
	S28	SIGNAL GROUND	

[a] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[b] S8 through S28 are not connected on single-port implementations.
[c] S16 through S28 are not connected on dual-port implementations.
[d] S~~22~~23 through S28 are not connected on triple-port implementations.
[e] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[f] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[g] SAS devices (see SPL-4) with SAS Drive plug connectors (see 5.4.3.3.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[h] SAS Drive backplane connectors (see 5.4.3.3.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.3.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[i] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-4. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 7 — SAS MultiLink connector pin assignments (part 3 of 3)

Segment	Pin [a]	SAS MultiLink Drive backplane receptacle [a]	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle [a]
Power segment [e]	P1	Vendor specific [g h i]	See [f g h i]
	P2	Vendor specific [g h i]	See [f g h i]
	P3	Vendor specific or POWER DISABLE [g h i j]	POWER DISABLE [g h i j]
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [k]	
	P8	V_5 [k]	
	P9	V_5 [k]	
	P10	GROUND	
	P11	READY LED [l]	
	P12	GROUND	
	P13	V_{12}, precharge [k]	
	P14	V_{12} [k]	
	P15	V_{12} [k]	

[a] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[b] S8 through S28 are not connected on single-port implementations.
[c] S16 through S28 are not connected on dual-port implementations.
[d] S~~22~~23 through S28 are not connected on triple-port implementations.
[e] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[f] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[g] SAS devices (see SPL-4) with SAS Drive plug connectors (see 5.4.3.3.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[h] SAS Drive backplane connectors (see 5.4.3.3.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.3.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[i] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-4. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.4.3.3.1.9 Micro SAS plug connector

The Micro SAS plug connector mechanical interface is defined in SFF-8486. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J. The Micro SAS plug mates with the Micro SAS Receptacle (see 5.4.3.3.1.10), but not the Micro SATA receptacle (see SATA).

See SFF-8147 for the Micro SAS plug connector locations on common form factors. Figure 30 shows the Micro SAS plug connector.

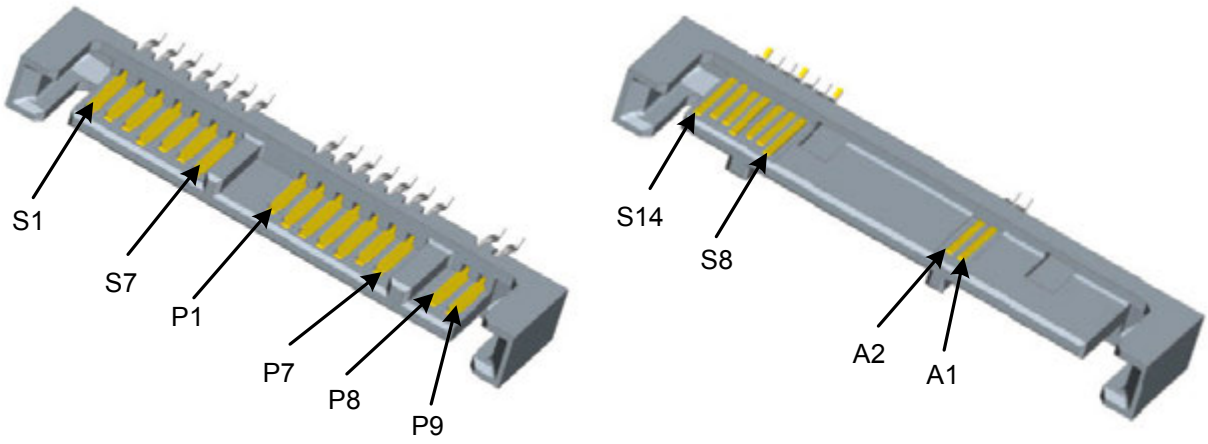


Figure 30 — Micro SAS plug connector

5.4.3.3.1.10 Micro SAS receptacle connector

The Micro SAS receptacle connector mechanical interface is defined in SFF-8486. The recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s are defined in Annex J. The Micro SAS receptacle mates with the Micro SAS plug connector (see 5.4.3.3.1.9) or the Micro SATA device plug (see SATA).

Figure 31 shows the Micro SAS receptacle connector.

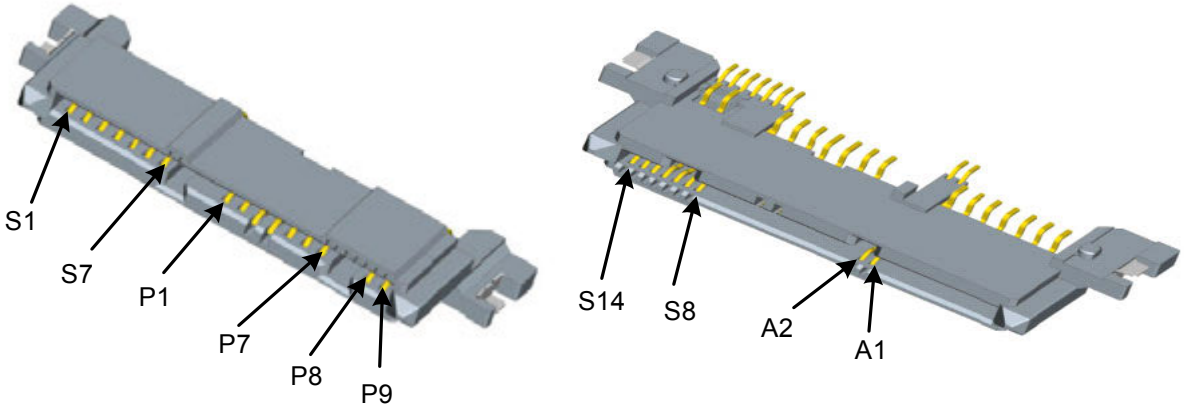


Figure 31 — Micro SAS receptacle connector

5.4.3.3.1.11 Micro SAS connector pin assignments

Table 8 defines the SAS target device pin assignments for the Micro SAS plug connector (see 5.4.3.3.1.9) and the Micro SAS receptacle connector (see 5.4.3.3.1.10). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

Micro SAS plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a Micro SATA device plug connector (see SATA).

Table 8 — Micro SAS connector pin assignments

Segment	Pin	Micro SAS receptacle	Micro SAS plug	Mating level [a]
Primary signal segment	S1	SIGNAL GROUND		Second
	S2	TP+	RP+	Third
	S3	TP-	RP-	Third
	S4	SIGNAL GROUND		Second
	S5	RP-	TP-	Third
	S6	RP+	TP+	Third
	S7	SIGNAL GROUND		Second
Secondary signal segment [b]	S8	SIGNAL GROUND		Second
	S9	TS+	RS+	Third
	S10	TS-	RS-	Third
	S11	SIGNAL GROUND		Second
	S12	RS-	TS-	Third
	S13	RS+	TS+	Third
	S14	SIGNAL GROUND		Second
Power segment [c]	P1	V_{33} [d]		Third
	P2	V_{33}, precharge [d]		Second
	P3	GROUND		First
	P4	GROUND		First
	P5	V_5, precharge [d]		Second
	P6	V_5 [d]		Third
	P7	Reserved		Third
	P8	Not connected	Manufacturing diagnostic	Third
	P9	Not connected	Manufacturing diagnostic	Third
Auxiliary contacts	A1	Vender specific		Third
	A2	Vender specific		Third

[a] The mating level assumes zero angular offset between connectors and indicates the physical dimension of the contact (see SFF-8486 and SATA).

[b] S8 through S14 are not connected on single-port implementations.

[c] The Micro SAS receptacle connector (see 5.4.3.3.1.10) provides V_{33} and V_5. The Micro SATA power receptacle connector (see SATA) provides V_{33} and optionally V_5. The Micro SAS plug connector (see 5.4.3.3.1.9) receives V_{33} and V_5.

[d] Behind a Micro SAS plug connector (see 5.4.3.3.1.9), the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_{33}, precharge pin P2 is connected to the V_{33} pin P1).

5.4.3.3.2 Mini SAS 4i connectors

5.4.3.3.2.1 Mini SAS 4i cable plug connector

The Mini SAS 4i cable plug connector is the free (plug) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 32 shows the Mini SAS 4i cable plug connector.

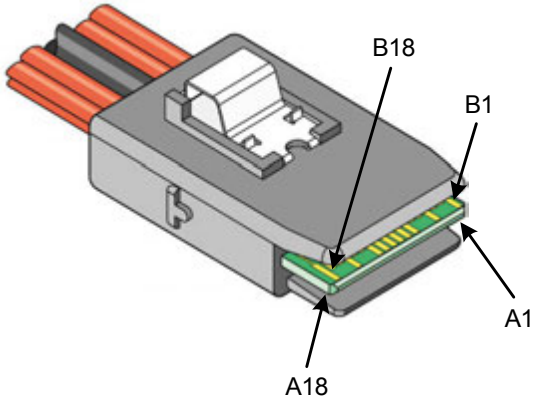


Figure 32 — Mini SAS 4i cable plug connector

Table 9 and table 10 (see 5.4.3.3.2.3) define the pin assignments for the Mini SAS 4i cable plug connector.

5.4.3.3.2.2 Mini SAS 4i receptacle connector

The Mini SAS 4i receptacle connector is the fixed (receptacle) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 33 shows the Mini SAS 4i receptacle connector.

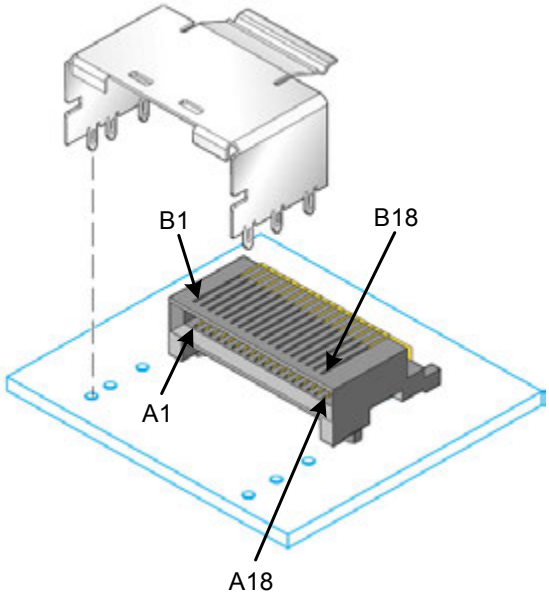


Figure 33 — Mini SAS 4i receptacle connector

Table 9 and table 10 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS 4i receptacle connector.

5.4.3.3.2.3 Mini SAS 4i connector pin assignments

Table 9 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.3.2.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.3.2.2) for controller applications using one, two, three, or four of the physical links.

Table 9 — Controller Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 7	A8	A8	A8	A8	First
SIDEBAND 3	A9	A9	A9	A9	
SIDEBAND 4	A10	A10	A10	A10	
SIDEBAND 5	A11	A11	A11	A11	
RX 2+	N/C	N/C	A13	A13	Third
RX 2-	N/C	N/C	A14	A14	
RX 3+	N/C	N/C	N/C	A16	
RX 3-	N/C	N/C	N/C	A17	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 0	B8	B8	B8	B8	First
SIDEBAND 1	B9	B9	B9	B9	
SIDEBAND 2	B10	B10	B10	B10	
SIDEBAND 6	B11	B11	B11	B11	
TX 2+	N/C	N/C	B13	B13	Third
TX 2-	N/C	N/C	B14	B14	
TX 3+	N/C	N/C	N/C	B16	
TX 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 10 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.3.2.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.3.2.2) for backplane applications using one, two, three, or four of the physical links.

Table 10 — Backplane Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 0	A8	A8	A8	A8	First
SIDEBAND 1	A9	A9	A9	A9	
SIDEBAND 2	A10	A10	A10	A10	
SIDEBAND 6	A11	A11	A11	A11	
RX 2+	N/C	N/C	A13	A13	Third
RX 2-	N/C	N/C	A14	A14	
RX 3+	N/C	N/C	N/C	A16	
RX 3-	N/C	N/C	N/C	A17	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 7	B8	B8	B8	B8	First
SIDEBAND 3	B9	B9	B9	B9	
SIDEBAND 4	B10	B10	B10	B10	
SIDEBAND 5	B11	B11	B11	B11	
TX 2+	N/C	N/C	B13	B13	Third
TX 2-	N/C	N/C	B14	B14	
TX 3+	N/C	N/C	N/C	B16	
TX 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.3.3 Mini SAS HD internal connectors

5.4.3.3.3.1 Mini SAS HD 4i cable plug connector

The Mini SAS HD 4i cable plug connector is the four lane cable (free) connector defined in SFF-8643. Figure 34 shows the Mini SAS HD 4i cable plug connector.

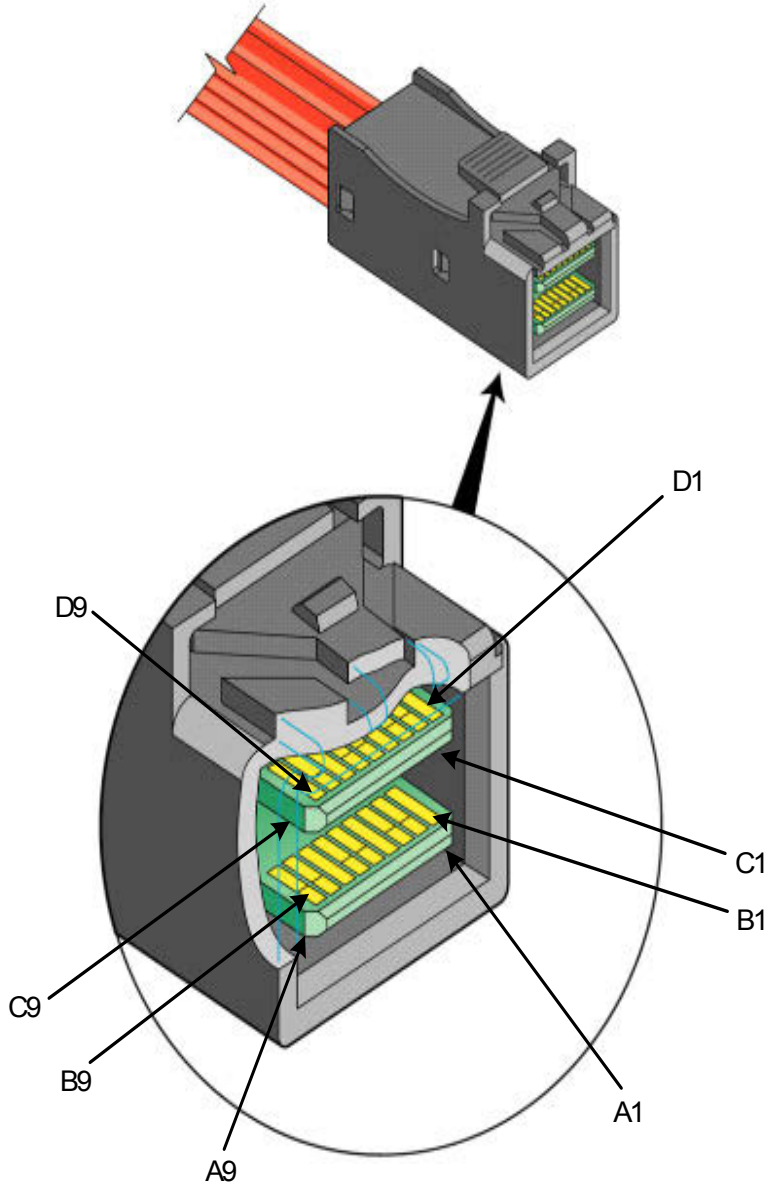


Figure 34 — Mini SAS HD 4i cable plug connector

Table 9 and table 10 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS HD 4i cable plug connector.

5.4.3.3.3.2 Mini SAS HD 8i cable plug connector

The Mini SAS HD 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8643.

Figure 35 shows the Mini SAS HD 8i cable plug connector. This connector is a modular version of repeating Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1). Module labeling is shown in figure 35. See figure 34 (see 5.4.3.3.3.1) for pin designations.

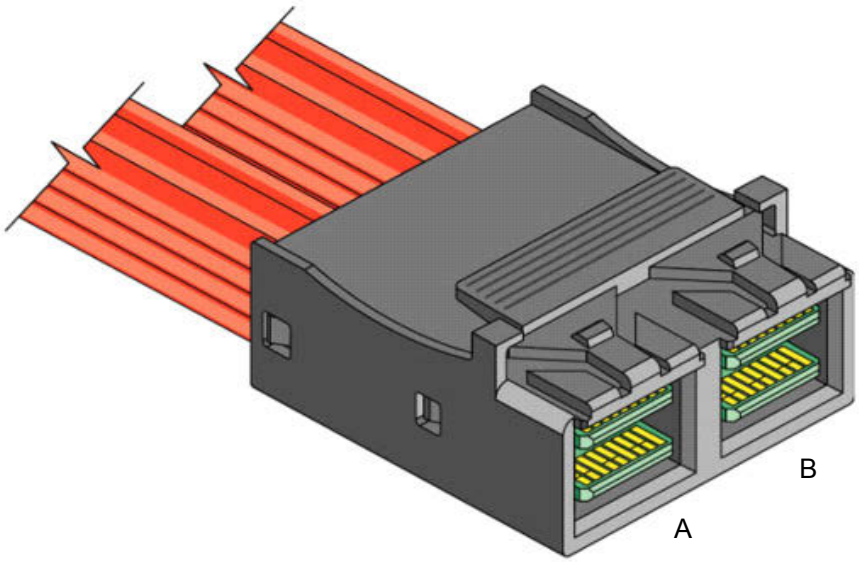


Figure 35 — Mini SAS HD 8i cable plug connector

Table 9 and table 10 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1). The pin assignments are repeated for each module of the Mini SAS 8i cable plug connector.

5.4.3.3.3.3 Mini SAS HD 4i receptacle connector

The Mini SAS HD 4i receptacle connector is the four lane receptacle (fixed) connector defined in SFF-8643. Figure 36 shows the Mini SAS HD 4i receptacle connector.

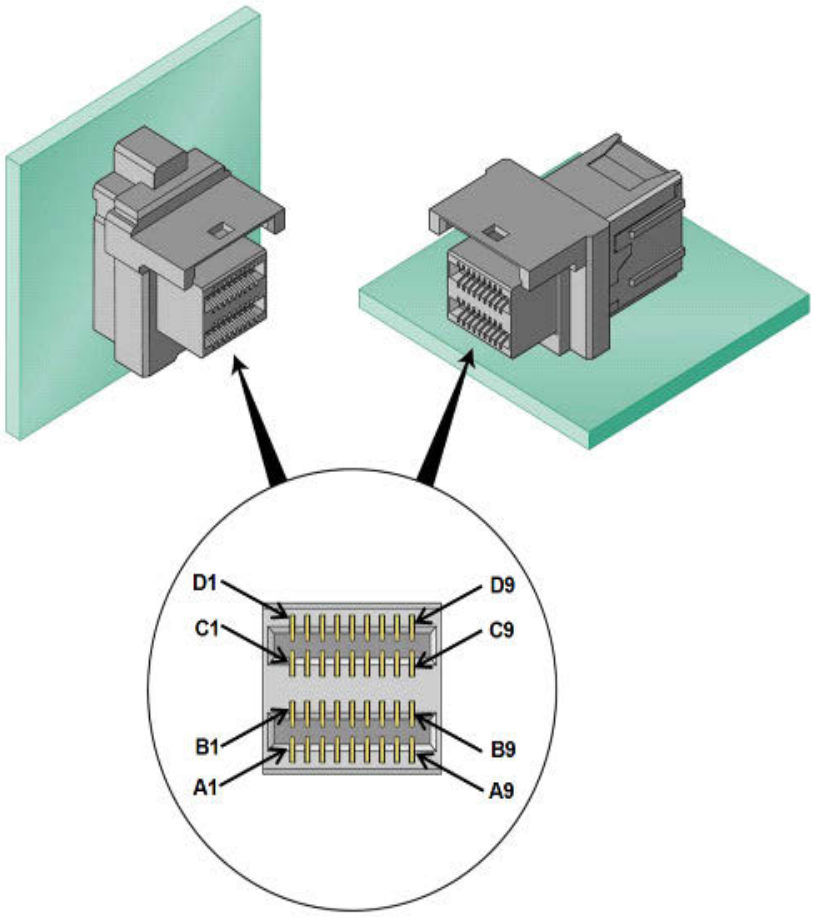


Figure 36 — Mini SAS HD 4i receptacle connector

Table 9 and table 10 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS HD 4i receptacle connector.

5.4.3.3.3.4 Mini SAS HD 8i receptacle connector

The Mini SAS HD 8i receptacle connector is a dual four lane receptacle (fixed) connector defined in SFF-8643. Figure 37 shows the Mini SAS HD 8i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.4.3.3.3.3). Module labeling is shown in figure 37. See figure 36 (see 5.4.3.3.3.3) for pin designations.

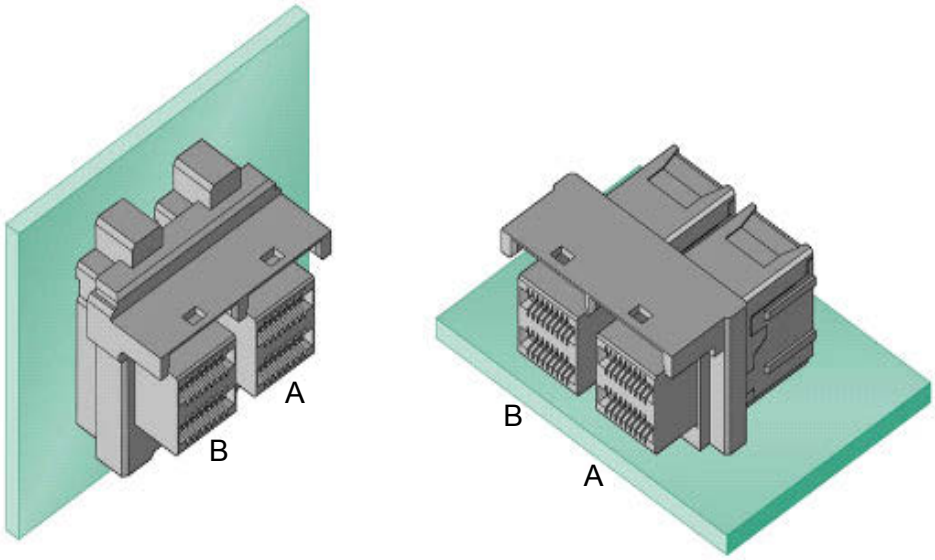


Figure 37 — Mini SAS HD 8i receptacle connector

Table 11 and table 12 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS HD 8i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.4.3.3.3.3). This connector accepts one Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) or two Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1).

5.4.3.3.3.5 Mini SAS HD 16i receptacle connector

The Mini SAS HD 16i receptacle connector is a quad four lane receptacle (fixed) connector defined in SFF-8643. Figure 38 shows the Mini SAS HD 16i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.4.3.3.3.3). Module labeling is shown in figure 38. See figure 36 (see 5.4.3.3.3.3) for pin designations.

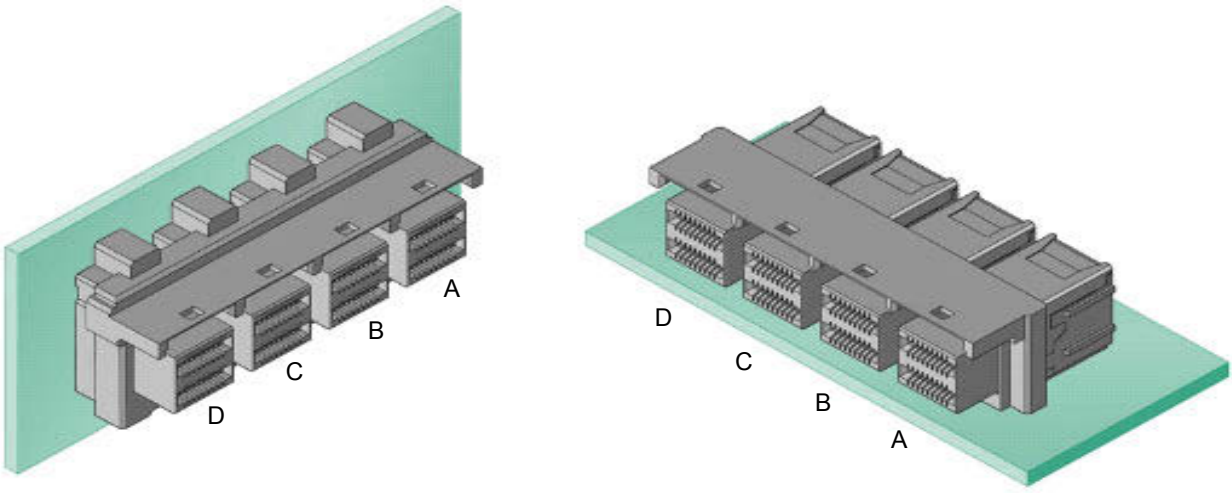


Figure 38 — Mini SAS HD 16i receptacle connector

Table 11 and table 12 (see 5.4.3.3.3.6) define the pin assignments for the Mini SAS HD 16i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.4.3.3.3.3). The Mini SAS HD 16i receptacle connector accepts:

a) one or two Mini SAS HD 8i cable plug connectors (see 5.4.3.3.3.2);
b) one, two, three, or four Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1); or
c) a combination of one Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) and one or two Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1).

A Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.4.3.3.3.6 Mini SAS HD 4i connector pin assignments

Table 11 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.3.3.3) for controller applications using one, two, three, or four of the physical links.

Table 11 — Controller Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	B4	B4	B4	B4	Third
RX 0-	B5	B5	B5	B5	
RX 1+	N/C	A4	A4	A4	
RX 1-	N/C	A5	A5	A5	
SIDEBAND 7	A1	A1	A1	A1	Second
SIDEBAND 3	B1	B1	B1	B1	
SIDEBAND 4	C1	C1	C1	C1	
SIDEBAND 5	D1	D1	D1	D1	
RX 2+	N/C	N/C	B7	B7	Third
RX 2-	N/C	N/C	B8	B8	
RX 3+	N/C	N/C	N/C	A7	
RX 3-	N/C	N/C	N/C	A8	
TX 0+	D4	D4	D4	D4	Third
TX 0-	D5	D5	D5	D5	
TX 1+	N/C	C4	C4	C4	
TX 1-	N/C	C5	C5	C5	
SIDEBAND 0	A2	A2	A2	A2	Second
SIDEBAND 1	B2	B2	B2	B2	
SIDEBAND 2	C2	C2	C2	C2	
SIDEBAND 6	D2	D2	D2	D2	
TX 2+	N/C	N/C	D7	D7	Third
TX 2-	N/C	N/C	D8	D8	
TX 3+	N/C	N/C	N/C	C7	
TX 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 12 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.3.3.3) for backplane applications using one, two, three, or four of the physical links.

Table 12 — Backplane Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	B4	B4	B4	B4	Third
RX 0-	B5	B5	B5	B5	
RX 1+	N/C	A4	A4	A4	
RX 1-	N/C	A5	A5	A5	
SIDEBAND 0	A1	A1	A1	A1	Second
SIDEBAND 1	B1	B1	B1	B1	
SIDEBAND 2	C1	C1	C1	C1	
SIDEBAND 6	D1	D1	D1	D1	
RX 2+	N/C	N/C	B7	B7	Third
RX 2-	N/C	N/C	B8	B8	
RX 3+	N/C	N/C	N/C	A7	
RX 3-	N/C	N/C	N/C	A8	
TX 0+	D4	D4	D4	D4	Third
TX 0-	D5	D5	D5	D5	
TX 1+	N/C	C4	C4	C4	
TX 1-	N/C	C5	C5	C5	
SIDEBAND 7	A2	A2	A2	A2	Second
SIDEBAND 3	B2	B2	B2	B2	
SIDEBAND 4	C2	C2	C2	C2	
SIDEBAND 5	D2	D2	D2	D2	
TX 2+	N/C	N/C	D7	D7	Third
TX 2-	N/C	N/C	D8	D8	
TX 3+	N/C	N/C	N/C	C7	
TX 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.3.4 SAS SlimLine internal connectors

5.4.3.3.4.1 SAS SlimLine 4i cable plug connector

The SAS SlimLine 4i cable plug connector is the four lane cable (free) connector defined in SFF-8654. Figure 39 shows the SAS SlimLine 4i cable plug connector.

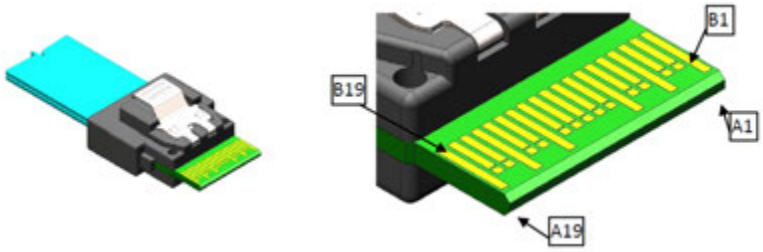


Figure 39 — SAS SlimLine 4i cable plug connector

Table 13 and table 14 (see 5.4.3.3.4.5) define the pin assignments for the SlimLine SAS 4i cable plug connector. This connector plugs into the SAS SlimLine 4i receptacle connector (see 5.4.3.3.4.3).

5.4.3.3.4.2 SAS SlimLine 8i cable plug connector

The SAS SlimLine 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8654.

Figure 35 shows the SAS SlimLine 8i cable plug connector.

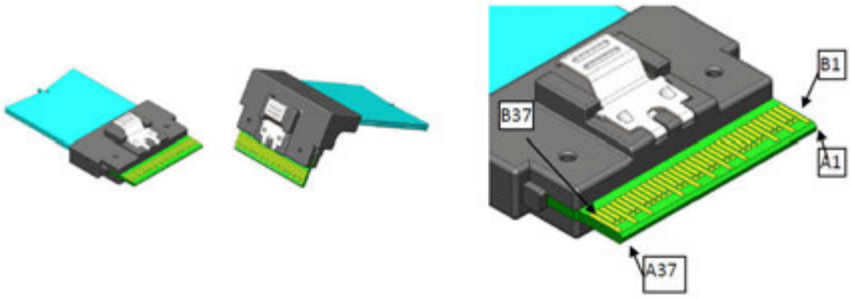


Figure 40 — SimLine SAS 8i cable plug connector

Table 15 and table 16 (see 5.4.3.3.4.5) define the pin assignments for the SAS SlimLine 8i cable plug connector. This connector plugs into the SAS SlimLine 8i receptacle connector (see 5.4.3.3.4.4).

5.4.3.3.4.3 SAS SlimLine 4i receptacle connector

The SAS SlimLine 4i receptacle connector is the four lane receptacle (fixed) connector defined in SFF-8654. Figure 41 shows the SAS SlimLine 4i receptacle connector.

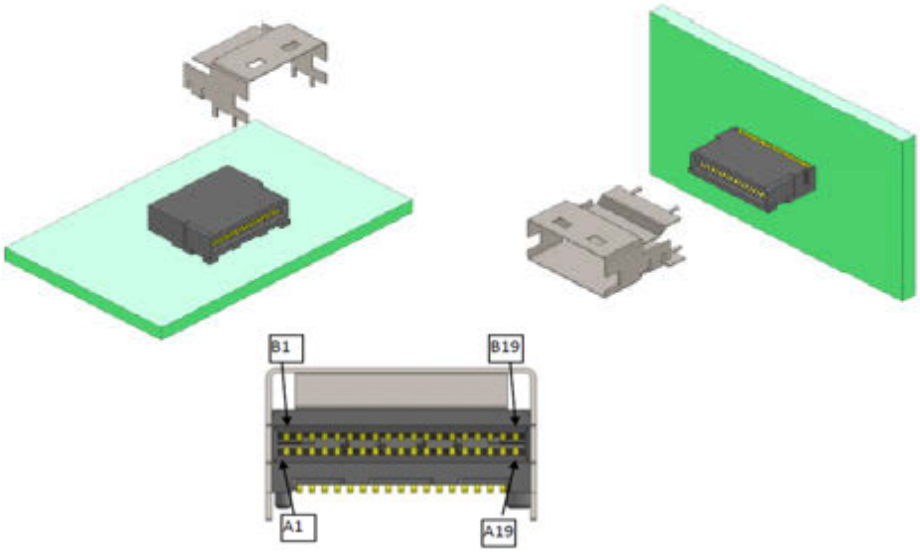


Figure 41 — SlimLine SAS 4i receptacle connector

Table 13 and table 14 (see 5.4.3.3.4.5) define the pin assignments for the SAS SlimLine 4i receptacle connector. This connector accepts the SAS SlimLine 4i cable plug connector (see 5.4.3.3.4.1).

5.4.3.3.4.4 SAS SlimLine 8i receptacle connector

The SAS SlimLine 8i receptacle connector is the four lane receptacle (fixed) connector defined in SFF-8654. Figure 36 shows the SAS SlimLine 8i receptacle connector.

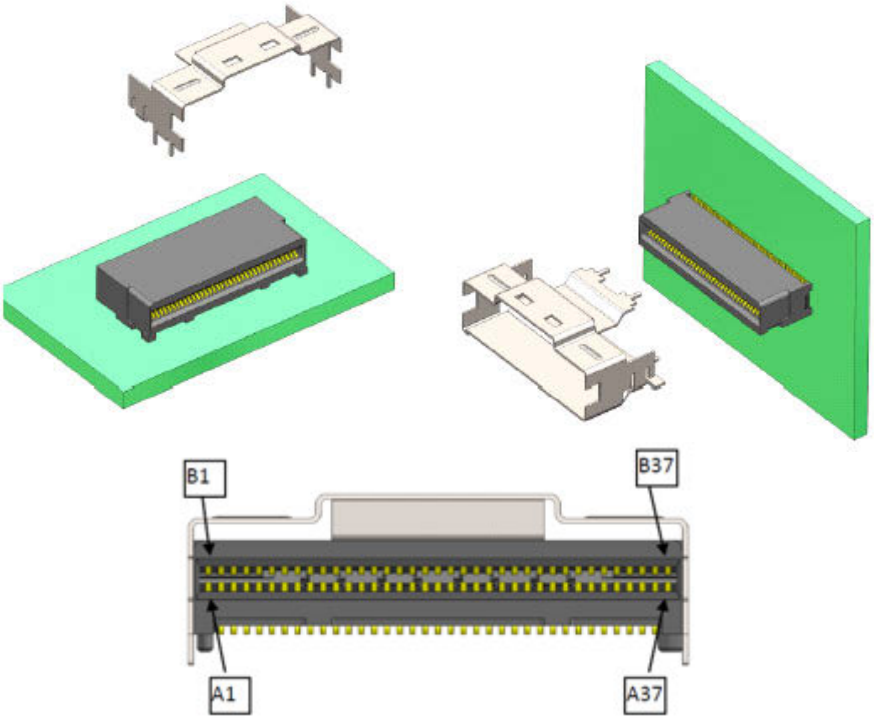


Figure 42 — SlimLine SAS 8i receptacle connector

Table 15 and table 16 (see 5.4.3.3.4.5) define the pin assignments for the SAS SlimLine 8i receptacle connector. This connector accepts the SAS SlimLine 8i cable plug connector (see 5.4.3.3.4.2).

5.4.3.3.4.5 SAS SlimLine connector pin assignments

Table 13 defines the pin assignments for SAS SlimLine 4i cable plug connectors (see 5.4.3.3.4.1) and SAS SlimLine 4i receptacle connectors (see 5.4.3.3.4.3) for controller applications using one, two, three, or four of the physical links.

Table 13 — Controller SAS SlimLine4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 7	A8	A8	A8	A8	Third
SIDEBAND 3	A9	A9	A9	A9	
SIDEBAND 9	A10	A10	A10	A10	
SIDEBAND 4	A11	A11	A11	A11	
SIDEBAND 5	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	
RX 3+	N/C	N/C	N/C	A17	
RX 3-	N/C	N/C	N/C	A18	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 0	B8	B8	B8	B8	Third
SIDEBAND 1	B9	B9	B9	B9	
SIDEBAND 8	B10	B10	B10	B10	
SIDEBAND 2	B11	B11	B11	B11	
SIDEBAND 6	B12	B12	B12	B12	
TX 2+	N/C	N/C	B14	B14	Third
TX 2-	N/C	N/C	B15	B15	
TX 3+	N/C	N/C	N/C	B17	
TX 3-	N/C	N/C	N/C	B18	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, B1, B4, B7, B13, B16, B19				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

The use of the sideband signals is vendor specific.

Table 14 defines the pin assignments for SAS SlimLine 4i cable plug connectors (see 5.4.3.3.4.1) and SAS SlimLine 4i receptacle connectors (see 5.4.3.3.4.3) for backplane applications using one, two, three, or four of the physical links.

Table 14 — Backplane SAS SlimLine4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 0	A8	A8	A8	A8	Third
SIDEBAND 1	A9	A9	A9	A9	
SIDEBAND 8	A10	A10	A10	A10	
SIDEBAND 2	A11	A11	A11	A11	
SIDEBAND 6	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	
RX 3+	N/C	N/C	N/C	A17	
RX 3-	N/C	N/C	N/C	A18	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 7	B8	B8	B8	B8	Third
SIDEBAND 3	B9	B9	B9	B9	
SIDEBAND 9	B10	B10	B10	B10	
SIDEBAND 4	B11	B11	B11	B11	
SIDEBAND 5	B12	B12	B12	B12	
TX 2+	N/C	N/C	B14	B14	Third
TX 2-	N/C	N/C	B15	B15	
TX 3+	N/C	N/C	N/C	B17	
TX 3-	N/C	N/C	N/C	B18	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, B1, B4, B7, B13, B16, B19				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

The use of the sideband signals is vendor specific.

Table 15 defines the pin assignments for SAS SlimLine 8i cable plug connectors (see 5.4.3.3.4.2) and SAS SlimLine 8i receptacle connectors (see 5.4.3.3.4.4) for controller applications using one, two, three, four, five, six, seven, or eight of the physical links.

Table 15 — Controller SAS SlimLine 8i connector pin assignments and physical link usage (part 1 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
RX 0+	A2	A2	A2	A2	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	A5	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	A6	A6	A6	A6	
SIDEBAND 7A	A8	A8	A8	A8	A8	A8	A8	A8	Third
SIDEBAND 3A	A9	A9	A9	A9	A9	A9	A9	A9	
SIDEBAND 9A	A10	A10	A10	A10	A10	A10	A10	A10	
SIDEBAND 4A	A11	A11	A11	A11	A11	A11	A11	A11	
SIDEBAND 5A	A12	A12	A12	A12	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	A14	A14	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	A15	A15	A15	A15	
RX 3+	N/C	N/C	N/C	A17	A17	A17	A17	A17	
RX 3-	N/C	N/C	N/C	A18	A18	A18	A18	A18	
RX 4+	N/C	N/C	N/C	N/C	A20	A20	A20	A20	Third
RX 4-	N/C	N/C	N/C	N/C	A21	A21	A21	A21	
RX 5+	N/C	N/C	N/C	N/C	N/C	A23	A23	A23	
RX 5-	N/C	N/C	N/C	N/C	N/C	A24	A24	A24	
SIDEBAND 7B	A26	A26	A26	A26	A26	A26	A26	A26	Third
SIDEBAND 3B	A27	A27	A27	A27	A27	A27	A27	A27	
SIDEBAND 9B	A28	A28	A28	A28	A28	A28	A28	A28	
SIDEBAND 4B	A29	A29	A29	A29	A29	A29	A29	A29	
SIDEBAND 5B	A30	A30	A30	A30	A30	A30	A30	A30	
RX 6+	N/C	N/C	N/C	N/C	N/C	N/C	A32	A32	Third
RX 6-	N/C	N/C	N/C	N/C	N/C	N/C	A33	A33	
RX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A35	
RX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A36	

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

Table 15 — Controller SAS SlimLine 8i connector pin assignments and physical link usage (part 2 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
TX 0+	B2	B2	B2	B2	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	B5	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	B6	B6	B6	B6	
SIDEBAND 0A	B8	B8	B8	B8	B8	B8	B8	B8	Third
SIDEBAND 1A	B9	B9	B9	B9	B9	B9	B9	B9	
SIDEBAND 8A	B10	B10	B10	B10	B10	B10	B10	B10	
SIDEBAND 2A	B11	B11	B11	B11	B11	B11	B11	B11	
SIDEBAND 6A	B12	B12	B12	B12	B12	B12	B12	B12	
TX 2+	N/C	N/C	B14	B14	B14	B14	B14	B14	Third
TX 2-	N/C	N/C	B15	B15	B15	B15	B15	B15	
TX 3+	N/C	N/C	N/C	B17	B17	B17	B17	B17	
TX 3-	N/C	N/C	N/C	B18	B18	B18	B18	B18	
TX 4+	N/C	N/C	N/C	N/C	B20	B20	B20	B20	Third
TX 4-	N/C	N/C	N/C	N/C	B21	B21	B21	B21	
TX 5+	N/C	N/C	N/C	N/C	N/C	B23	B23	B23	
TX 5-	N/C	N/C	N/C	N/C	N/C	B24	B24	B24	
SIDEBAND 0B	B26	B26	B26	B26	B26	B26	B26	B26	Third
SIDEBAND 1B	B27	B27	B27	B27	B27	B27	B27	B27	
SIDEBAND 8B	B28	B28	B28	B28	B28	B28	B28	B28	
SIDEBAND 2B	B29	B29	B29	B29	B29	B29	B29	B29	
SIDEBAND 6B	B30	B30	B30	B30	B30	B30	B30	B30	
TX 6+	N/C	N/C	N/C	N/C	N/C	N/C	B32	B32	Third
TX 6-	N/C	N/C	N/C	N/C	N/C	N/C	B33	B33	
TX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B35	
TX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B36	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, A22, A25, A31, A34, A37, B1, B4, B7, B13, B16, B19, B22, B25, B31, B34, B37								First

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

The use of the sideband signals is vendor specific.

Table 16 defines the pin assignments for SAS SlimLine 8i cable plug connectors (see 5.4.3.3.4.2) and SAS SlimLine 8i receptacle connectors (see 5.4.3.3.4.4) for backplane applications using one, two, three, four, five, six, seven, or eight of the physical links

Table 16 — Backplane SAS SlimLine 8i connector pin assignments and physical link usage (part 1 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
RX 0+	A2	A2	A2	A2	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	A5	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	A6	A6	A6	A6	
SIDEBAND 0A	A8	A8	A8	A8	A8	A8	A8	A8	Third
SIDEBAND 1A	A9	A9	A9	A9	A9	A9	A9	A9	
SIDEBAND 8A	A10	A10	A10	A10	A10	A10	A10	A10	
SIDEBAND 2A	A11	A11	A11	A11	A11	A11	A11	A11	
SIDEBAND 6A	A12	A12	A12	A12	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	A14	A14	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	A15	A15	A15	A15	
RX 3+	N/C	N/C	N/C	A17	A17	A17	A17	A17	
RX 3-	N/C	N/C	N/C	A18	A18	A18	A18	A18	
RX 4+	N/C	N/C	N/C	N/C	A20	A20	A20	A20	Third
RX 4-	N/C	N/C	N/C	N/C	A21	A21	A21	A21	
RX 5+	N/C	N/C	N/C	N/C	N/C	A23	A23	A23	
RX 5-	N/C	N/C	N/C	N/C	N/C	A24	A24	A24	
SIDEBAND 0B	A26	A26	A26	A26	A26	A26	A26	A26	Third
SIDEBAND 1B	A27	A27	A27	A27	A27	A27	A27	A27	
SIDEBAND 8B	A28	A28	A28	A28	A28	A28	A28	A28	
SIDEBAND 2B	A29	A29	A29	A29	A29	A29	A29	A29	
SIDEBAND 6B	A30	A30	A30	A30	A30	A30	A30	A30	
RX 6+	N/C	N/C	N/C	N/C	N/C	N/C	A32	A32	Third
RX 6-	N/C	N/C	N/C	N/C	N/C	N/C	A33	A33	
RX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A35	
RX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A36	

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

Table 16 — Backplane SAS SlimLine 8i connector pin assignments and physical link usage (part 2 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
TX 0+	B2	B2	B2	B2	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	B5	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	B6	B6	B6	B6	
SIDEBAND 0A	B8	B8	B8	B8	B8	B8	B8	B8	Third
SIDEBAND 1A	B9	B9	B9	B9	B9	B9	B9	B9	
SIDEBAND 8A	B10	B10	B10	B10	B10	B10	B10	B10	
SIDEBAND 2A	B11	B11	B11	B11	B11	B11	B11	B11	
SIDEBAND 6A	B12	B12	B12	B12	B12	B12	B12	B12	
TX 2+	N/C	N/C	B14	B14	B14	B14	B14	B14	Third
TX 2-	N/C	N/C	B15	B15	B15	B15	B15	B15	
TX 3+	N/C	N/C	N/C	B17	B17	B17	B17	B17	
TX 3-	N/C	N/C	N/C	B18	B18	B18	B18	B18	
TX 4+	N/C	N/C	N/C	N/C	B20	B20	B20	B20	Third
TX 4-	N/C	N/C	N/C	N/C	B21	B21	B21	B21	
TX 5+	N/C	N/C	N/C	N/C	N/C	B23	B23	B23	
TX 5-	N/C	N/C	N/C	N/C	N/C	B24	B24	B24	
SIDEBAND 0B	B26	B26	B26	B26	B26	B26	B26	B26	Third
SIDEBAND 1B	B27	B27	B27	B27	B27	B27	B27	B27	
SIDEBAND 8B	B28	B28	B28	B28	B28	B28	B28	B28	
SIDEBAND 2B	B29	B29	B29	B29	B29	B29	B29	B29	
SIDEBAND 6B	B30	B30	B30	B30	B30	B30	B30	B30	
TX 6+	N/C	N/C	N/C	N/C	N/C	N/C	B32	B32	Third
TX 6-	N/C	N/C	N/C	N/C	N/C	N/C	B33	B33	
TX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B35	
TX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B36	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, A22, A25, A31, A34, A37, B1, B4, B7, B13, B16, B19, B22, B25, B31, B34, B37								First

[a] The mating level indicates the physical dimension of the contact (see SFF-8654).

The use of the sideband signals is vendor specific.

5.4.3.3.5 SAS MiniLink internal connectors

5.4.3.3.5.1 SAS MiniLink 4i cable plug connector

The SAS MiniLink 4i cable plug connector is the four lane cable (free) connector defined in SFF-8611. Figure 43 shows the SAS MiniLink 4i cable plug connector.

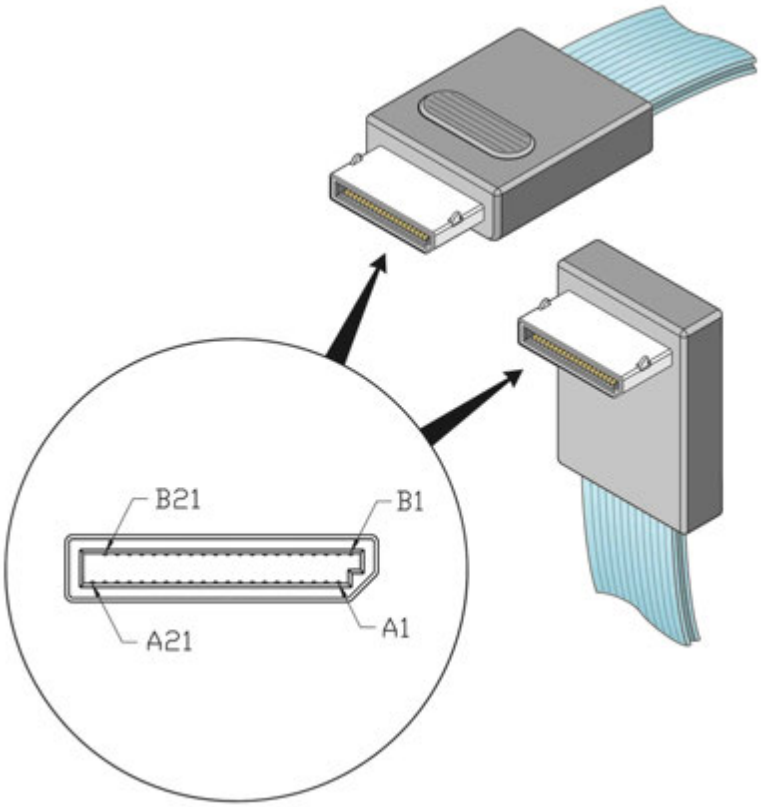


Figure 43 — SAS MiniLink 4i cable plug connector

Table 17 and table 18 (see 5.4.3.3.5.5) define the pin assignments for the SAS MiniLink 4i cable plug connector. This connector plugs into the SAS MiniLink 4i receptacle connector (see 5.4.3.3.5.3).

5.4.3.3.5.2 SAS MiniLink 8i cable plug connector

The SAS MiniLink 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8611.

Figure 44 shows the SAS MiniLink 8i cable plug connector.

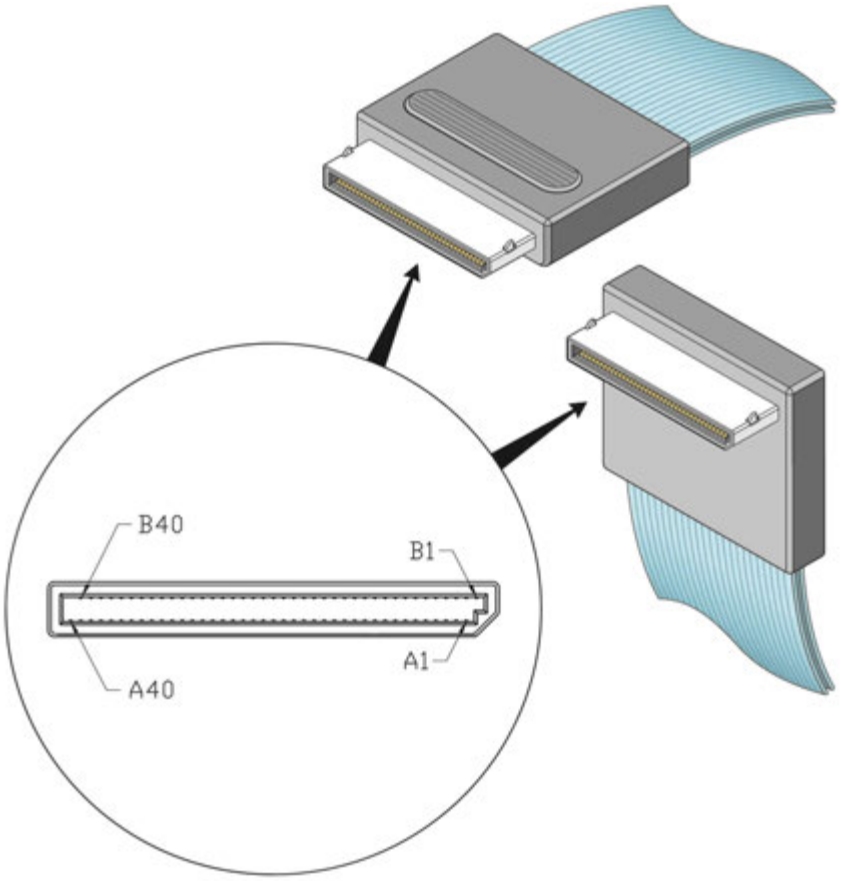


Figure 44 — SAS MiniLink 8i cable plug connector

Table 19and table 20 (see 5.4.3.3.5.5) define the pin assignments for the SAS MiniLink 8i cable plug connector. This connector plugs into the SAS MiniLink 8i receptacle connector (see 5.4.3.3.5.4).

5.4.3.3.5.3 SAS MiniLink 4i receptacle connector

The SAS MiniLink 4i receptacle connector is the four lane receptacle (fixed) connector defined in SFF-8612. Figure 45 shows the SAS MiniLink 4i receptacle connector.

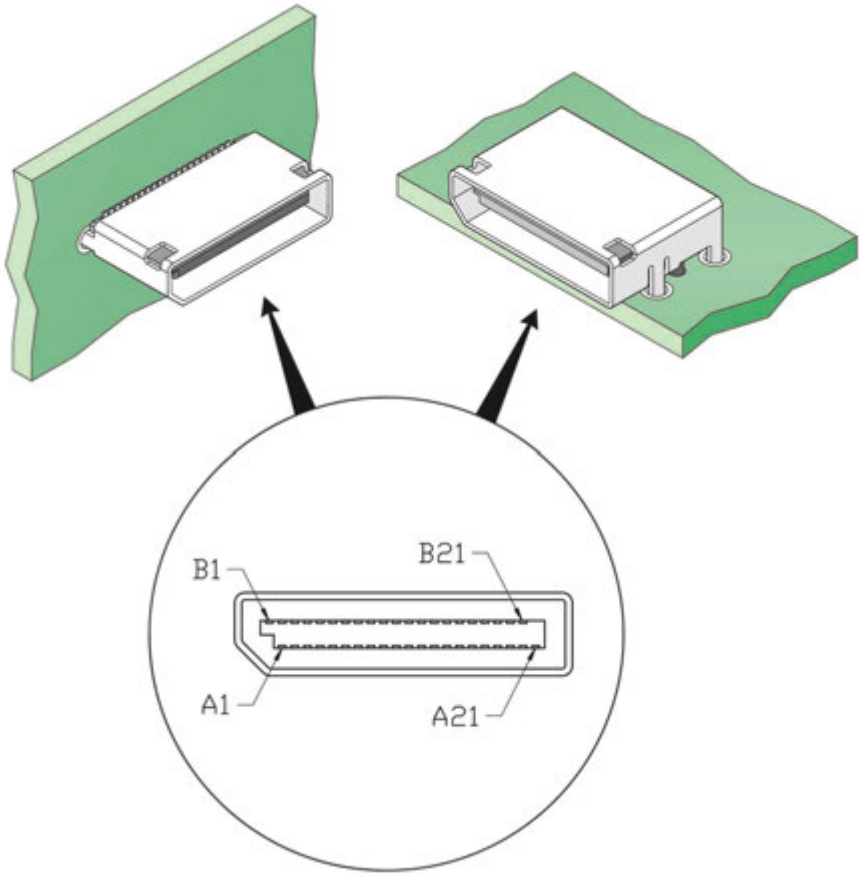


Figure 45 — SAS MiniLink 4i receptacle connector

Table 17 and table 18 (see 5.4.3.3.5.5) define the pin assignments for the SAS MiniLink 4i receptacle connector. This connector accepts the SAS MiniLink 4i cable plug connector (see 5.4.3.3.5.1).

5.4.3.3.5.4 SAS MiniLink 8i receptacle connector

The SAS MiniLink 8i receptacle connector is the eight lane receptacle (fixed) connector defined in SFF-8612. Figure 46 shows the SAS MiniLink 8i receptacle connector.

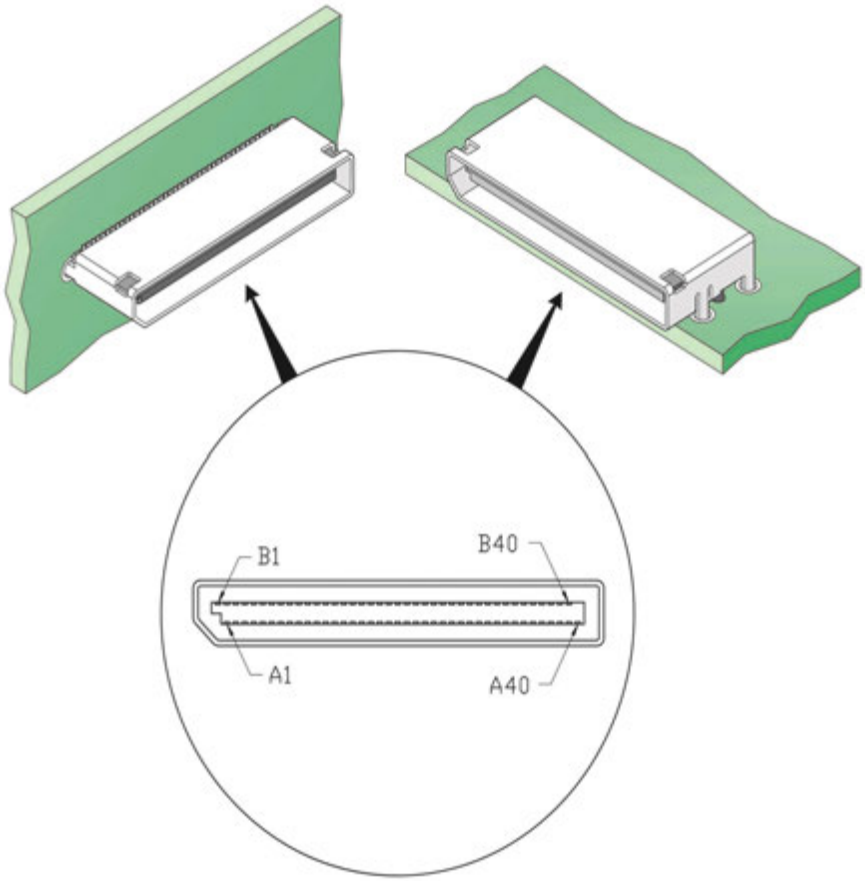


Figure 46 — SAS MiniLink 8i receptacle connector

Table 19and table 20 (see 5.4.3.3.5.5) define the pin assignments for the SAS MiniLink 8i receptacle connector. This connector accepts the SAS MiniLink 8i cable plug connector (see 5.4.3.3.5.2).

5.4.3.3.5.5 SAS MiniLink connector pin assignments

Table 17 defines the pin assignments for SAS MiniLink 4i cable plug connectors (see 5.4.3.3.5.1) and SAS MiniLink 4i receptacle connectors (see 5.4.3.3.5.3) for controller applications using one, two, three, or four of the physical links.

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Table 17 — Controller SAS MiniLink 4i pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A3	A3	A3	A3	Third
RX 0-	A4	A4	A4	A4	
RX 1+	N/C	A6	A6	A6	
RX 1-	N/C	A7	A7	A7	
SIDEBAND 7	A9	A9	A9	A9	Second
SIDEBAND 3	A10	A10	A10	A10	
SIDEBAND 9	A11	A11	A11	A11	
SIDEBAND 4	A12	A12	A12	A12	
SIDEBAND 5	A13	A13	A13	A13	
RX 2+	N/C	N/C	A15	A15	Third
RX 2-	N/C	N/C	A16	A16	
RX 3+	N/C	N/C	N/C	A18	
RX 3-	N/C	N/C	N/C	A19	
TX 0+	B3	B3	B3	B3	Third
TX 0-	B4	B4	B4	B4	
TX 1+	N/C	B6	B6	B6	
TX 1-	N/C	B7	B7	B7	
SIDEBAND 0	B9	B9	B9	B9	Second
SIDEBAND 1	B10	B10	B10	B10	
SIDEBAND 8	B11	B11	B11	B11	
SIDEBAND 2	B12	B12	B12	B12	
SIDEBAND 6	B13	B13	B13	B13	
TX 2+	N/C	N/C	B15	B15	Third
TX 2-	N/C	N/C	B16	B16	
TX 3+	N/C	N/C	N/C	B18	
TX 3-	N/C	N/C	N/C	B19	
SIGNAL GROUND	A2, A5, A8, A14, A17, A20, B2, B5, B8, B14, B17, B20				First
RESERVED	A1, A21, B1, B21				Third

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

The use of the sideband signals is vendor specific.

Table 18 defines the pin assignments for SAS MiniLink 4i cable plug connectors (see 5.4.3.3.5.1) and SAS MiniLink 4i receptacle connectors (see 5.4.3.3.5.3) for backplane applications using one, two, three, or four of the physical links.

Table 18 — Backplane SAS MiniLink 4i pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A3	A3	A3	A3	Third
RX 0-	A4	A4	A4	A4	
RX 1+	N/C	A6	A6	A6	
RX 1-	N/C	A7	A7	A7	
SIDEBAND 0	A9	A9	A9	A9	Second
SIDEBAND 1	A10	A10	A10	A10	
SIDEBAND 8	A11	A11	A11	A11	
SIDEBAND 2	A12	A12	A12	A12	
SIDEBAND 6	A13	A13	A13	A13	
RX 2+	N/C	N/C	A15	A15	Third
RX 2-	N/C	N/C	A16	A16	
RX 3+	N/C	N/C	N/C	A18	
RX 3-	N/C	N/C	N/C	A19	
TX 0+	B3	B3	B3	B3	Third
TX 0-	B4	B4	B4	B4	
TX 1+	N/C	B6	B6	B6	
TX 1-	N/C	B7	B7	B7	
SIDEBAND 7	B9	B9	B9	B9	Second
SIDEBAND 3	B10	B10	B10	B10	
SIDEBAND 9	B11	B11	B11	B11	
SIDEBAND 4	B12	B12	B12	B12	
SIDEBAND 5	B13	B13	B13	B13	
TX 2+	N/C	N/C	B15	B15	Third
TX 2-	N/C	N/C	B16	B16	
TX 3+	N/C	N/C	N/C	B18	
TX 3-	N/C	N/C	N/C	B19	
SIGNAL GROUND	A2, A5, A8, A14, A17, A20, B2, B5, B8, B14, B17, B20				First
RESERVED	A1, A21, B1, B21				Third

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

Table 19 defines the pin assignments for SAS MiniLink 8i cable plug connectors (see 5.4.3.3.5.2) and SAS MiniLink 8i receptacle connectors (see 5.4.3.3.5.4) for controller applications for using one, two, three, four, five, six, seven, or eight of the physical links.

Table 19 — Controller SAS MiniLink 8i connector pin assignments and physical link usage (part 1 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
RX 0+	A2	A2	A2	A2	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	A5	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	A6	A6	A6	A6	
SIDEBAND 7A	A8	A8	A8	A8	A8	A8	A8	A8	Third
SIDEBAND 3A	A9	A9	A9	A9	A9	A9	A9	A9	
SIDEBAND 9A	A10	A10	A10	A10	A10	A10	A10	A10	
SIDEBAND 4A	A11	A11	A11	A11	A11	A11	A11	A11	
SIDEBAND 5A	A12	A12	A12	A12	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	A14	A14	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	A15	A15	A15	A15	
RX 3+	N/C	N/C	N/C	A17	A17	A17	A17	A17	
RX 3-	N/C	N/C	N/C	A18	A18	A18	A18	A18	
RX 4+	N/C	N/C	N/C	N/C	A23	A23	A23	A23	Third
RX 4-	N/C	N/C	N/C	N/C	A24	A24	A24	A24	
RX 5+	N/C	N/C	N/C	N/C	N/C	A26	A26	A26	
RX 5-	N/C	N/C	N/C	N/C	N/C	A27	A27	A27	
SIDEBAND 7B	A29	A29	A29	A29	A29	A29	A29	A29	Third
SIDEBAND 3B	A30	A30	A30	A30	A30	A30	A30	A30	
SIDEBAND 9B	A31	A31	A31	A31	A31	A31	A31	A31	
SIDEBAND 4B	A32	A32	A32	A32	A32	A32	A32	A32	
SIDEBAND 5B	A33	A33	A33	A33	A33	A33	A33	A33	
RX 6+	N/C	N/C	N/C	N/C	N/C	N/C	A35	A35	Third
RX 6-	N/C	N/C	N/C	N/C	N/C	N/C	A36	A36	
RX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A38	
RX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A39	
TX 0+	B2	B2	B2	B2	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	B5	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	B6	B6	B6	B6	

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

Table 19 — Controller SAS MiniLink 8i connector pin assignments and physical link usage (part 2 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
SIDEBAND 0A	B8	B8	B8	B8	B8	B8	B8	B8	Third
SIDEBAND 1A	B9	B9	B9	B9	B9	B9	B9	B9	
SIDEBAND 8A	B10	B10	B10	B10	B10	B10	B10	B10	
SIDEBAND 2A	B11	B11	B11	B11	B11	B11	B11	B11	
SIDEBAND 6A	B12	B12	B12	B12	B12	B12	B12	B12	
TX 2+	N/C	N/C	B14	B14	B14	B14	B14	B14	Third
TX 2-	N/C	N/C	B15	B15	B15	B15	B15	B15	
TX 3+	N/C	N/C	N/C	B17	B17	B17	B17	B17	
TX 3-	N/C	N/C	N/C	B18	B18	B18	B18	B18	
TX 4+	N/C	N/C	N/C	N/C	B23	B23	B23	B23	Third
TX 4-	N/C	N/C	N/C	N/C	B24	B24	B24	B24	
TX 5+	N/C	N/C	N/C	N/C	N/C	B26	B26	B26	
TX 5-	N/C	N/C	N/C	N/C	N/C	B27	B27	B27	
SIDEBAND 0B	B29	B29	B29	B29	B29	B29	B29	B29	Third
SIDEBAND 1B	B30	B30	B30	B30	B30	B30	B30	B30	
SIDEBAND 8B	B31	B31	B31	B31	B31	B31	B31	B31	
SIDEBAND 2B	B32	B32	B32	B32	B32	B32	B32	B32	
SIDEBAND 6B	B33	B33	B33	B33	B33	B33	B33	B33	
TX 6+	N/C	N/C	N/C	N/C	N/C	N/C	B35	B35	Third
TX 6-	N/C	N/C	N/C	N/C	N/C	N/C	B36	B36	
TX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B38	
TX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B39	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, A22, A25, A28, A34, A 37, A40, B1 B4, B7, B13, B16, B19, B22, B25, B28, B28, B34, B37, B40								First
RESERVED	A20, A21, B20, B21								Third

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

The use of the sideband signals is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 20 defines the pin assignments for SAS MiniLink 8i cable plug connectors (see 5.4.3.3.5.2) and SAS MiniLink 8i receptacle connectors (see 5.4.3.3.5.4) for backplane applications for using one, two, three, four, five, six, seven, or eight of the physical links.

Table 20 — Backplane SAS MiniLink 8i connector pin assignments and physical link usage (part 1 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
RX 0+	A2	A2	A2	A2	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	A5	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	A6	A6	A6	A6	
SIDEBAND 0A	A8	A8	A8	A8	A8	A8	A8	A8	Third
SIDEBAND 1A	A9	A9	A9	A9	A9	A9	A9	A9	
SIDEBAND 8A	A10	A10	A10	A10	A10	A10	A10	A10	
SIDEBAND 2A	A11	A11	A11	A11	A11	A11	A11	A11	
SIDEBAND 6A	A12	A12	A12	A12	A12	A12	A12	A12	
RX 2+	N/C	N/C	A14	A14	A14	A14	A14	A14	Third
RX 2-	N/C	N/C	A15	A15	A15	A15	A15	A15	
RX 3+	N/C	N/C	N/C	A17	A17	A17	A17	A17	
RX 3-	N/C	N/C	N/C	A18	A18	A18	A18	A18	
RX 4+	N/C	N/C	N/C	N/C	A23	A23	A23	A23	Third
RX 4-	N/C	N/C	N/C	N/C	A24	A24	A24	A24	
RX 5+	N/C	N/C	N/C	N/C	N/C	A26	A26	A26	
RX 5-	N/C	N/C	N/C	N/C	N/C	A27	A27	A27	
SIDEBAND 0B	A29	A29	A29	A29	A29	A29	A29	A29	Third
SIDEBAND 1B	A30	A30	A30	A30	A30	A30	A30	A30	
SIDEBAND 8B	A31	A31	A31	A31	A31	A31	A31	A31	
SIDEBAND 2B	A32	A32	A32	A32	A32	A32	A32	A32	
SIDEBAND 6B	A33	A33	A33	A33	A33	A33	A33	A33	
RX 6+	N/C	N/C	N/C	N/C	N/C	N/C	A35	A35	Third
RX 6-	N/C	N/C	N/C	N/C	N/C	N/C	A36	A36	
RX 7+	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A38	
RX 7-	N/C	N/C	N/C	N/C	N/C	N/C	N/C	A39	

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

Table 20 — Backplane SAS MiniLink 8i connector pin assignments and physical link usage (part 2 of 2)

Signal	Pin usage based on number of physical links supported by the cable assembly								Mating level [a]
	One	Two	Three	Four	Five	Six	Seven	Eight	
TX 0+	B2	B2	B2	B2	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	B5	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	B6	B6	B6	B6	
SIDEBAND 7A	B8	B8	B8	B8	B8	B8	B8	B8	Third
SIDEBAND 3A	B9	B9	B9	B9	B9	B9	B9	B9	
SIDEBAND 9A	B10	B10	B10	B10	B10	B10	B10	B10	
SIDEBAND 4A	B11	B11	B11	B11	B11	B11	B11	B11	
SIDEBAND 5A	B12	B12	B12	B12	B12	B12	B12	B12	
TX 2+	N/C	B14	B14	B14	B14	B14	B14	B14	Third
TX 2-	N/C	B15	B15	B15	B15	B15	B15	B15	
TX 3+	N/C	B17	B17	B17	B17	B17	B17	B17	
TX 3-	N/C	B18	B18	B18	B18	B18	B18	B18	
TX 4+	N/C	B23	B23	B23	B23	B23	B23	B23	Third
TX 4-	N/C	B24	B24	B24	B24	B24	B24	B24	
TX 5+	N/C	B26	B26	B26	B26	B26	B26	B26	
TX 5-	N/C	B27	B27	B27	B27	B27	B27	B27	
SIDEBAND 7B	B29	B29	B29	B29	B29	B29	B29	B29	Third
SIDEBAND 3B	B30	B30	B30	B30	B30	B30	B30	B30	
SIDEBAND 9B	B31	B31	B31	B31	B31	B31	B31	B31	
SIDEBAND 4B	B32	B32	B32	B32	B32	B32	B32	B32	
SIDEBAND 5B	B33	B33	B33	B33	B33	B33	B33	B33	
TX 6+	N/C	B35	B35	B35	B35	B35	B35	B35	Third
TX 6-	N/C	B36	B36	B36	B36	B36	B36	B36	
TX 7+	N/C	B38	B38	B38	B38	B38	B38	B38	
TX 7-	N/C	B39	B39	B39	B39	B39	B39	B39	
SIGNAL GROUND	A1, A4, A7, A13, A16, A19, A22, A25, A28, A34, A 37, A40, B1 B4, B7, B13, B16, B19, B22, B25, B28, B28, B34, B37, B40								First
RESERVED	A20, A21, B20, B21								Third

[a] The mating level indicates the physical dimension of the contact (see SFF-8611 and SFF-8612).

5.4.3.4 SAS external connectors

5.4.3.4.1 Mini SAS 4x connectors

5.4.3.4.1.1 Mini SAS 4x cable plug connector

The Mini SAS 4x cable plug connector and the MiniSAS 4x active plug connector are the free (plug) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086. The Mini SAS 4x cable plug connector should not be used for rates greater than 6 Gbit/s.

Figure 47 shows the Mini SAS 4x cable plug connector.

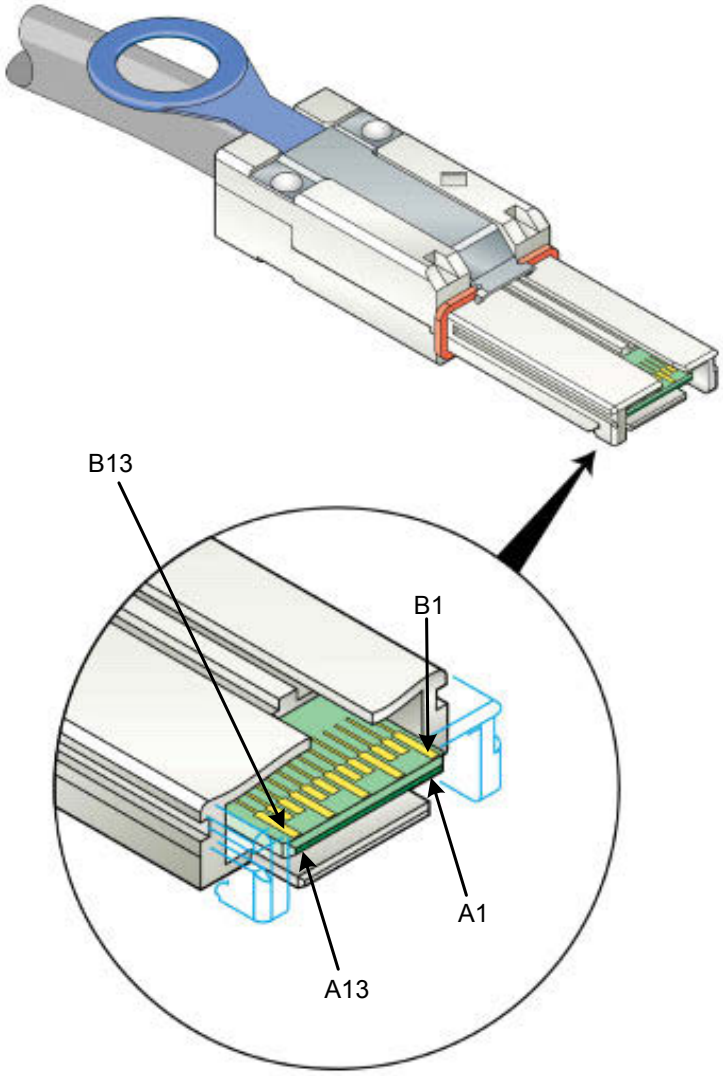


Figure 47 — Mini SAS 4x cable plug connector

If constructed with a pull tab as shown in figure 47, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 23 (see 5.4.3.4.1.3) and table 24 (see 5.4.3.4.1.3) define the pin assignments for the Mini SAS 4x cable plug connector.

Mini SAS 4x cable plug connectors shall include key slots to allow attachment to Mini SAS 4x receptacle connectors (see 5.4.3.4.1.2) with matching keys and key slots.

To ensure active cable assemblies are not intermateable with Mini SAS 4x receptacles that do not support active cable assemblies, differentiating keying shall be provided by having a blocking key on the plug

connector in addition to the key slots. Table 21 defines the icons that shall be placed on or near Mini SAS 4x cable plug connectors and the key slot and key positions (see SFF-8088) that shall be used by Mini SAS 4x cable plug connectors.

Table 21 — Mini SAS 4x cable plug connector and Mini SAS 4x active cable plug connector icons, key slot positions, and key positions

End of a SAS external cable		Icon	Key slot positions	Key positions	Reference
Electrical compliance	**Attaches to**				
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	Out or in [b]	Diamond and circle	2, 4, 6	none	Figure 48
	Out [c]	Diamond	2, 4	none	Figure 49
	In [d]	Circle	4, 6	none	Figure 50
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [e]	Out or in [b]	Two diamonds and two circles	2, 4, 6	3	Figure 51
	Out [c]	Two diamonds	2, 4	3	Figure 52
	In [d]	Two circles	4, 6	3	Figure 53
	Out or in [b]	Two triangles, diamond, and circle	2, 4, 6	5	Figure 54 [f]
	Out [c]	Two triangles and diamond	2, 4	5	Figure 55 [f]
	In [d]	Two triangles and circle	4, 6	5	Figure 56 [f]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Attaches to an end device, an enclosure out port, an enclosure in port, or an enclosure universal port.
[c] Attaches to an end device, an enclosure out port, or an enclosure universal port.
[d] Attaches to an end device, an enclosure in port, or an enclosure universal port.
[e] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[f] Mini SAS 4x active cable plug connector.

Figure 48 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 58,

figure 61, and figure 64 in 5.4.3.4.1.2), an enclosure out port (see figure 59, figure 62, and figure 65 in 5.4.3.4.1.2), or an enclosure in port (see figure 60, figure 63, and figure 66 in 5.4.3.4.1.2).

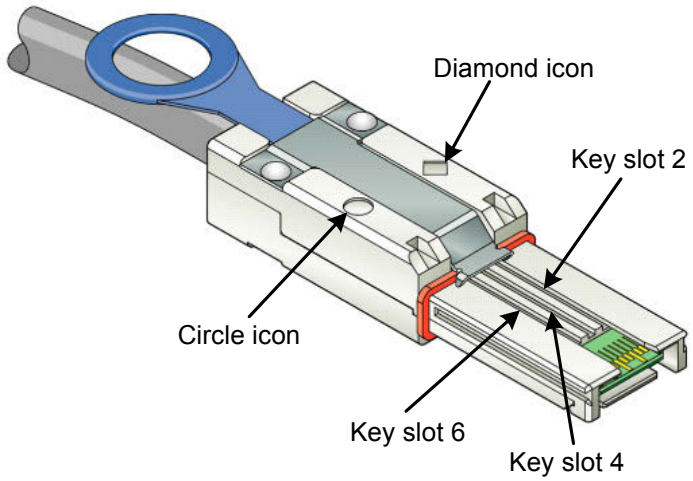


Figure 48 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 49 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 58, figure 61, and figure 64 in 5.4.3.4.1.2) or an enclosure out port (see figure 59, figure 62, and figure 65 in 5.4.3.4.1.2).

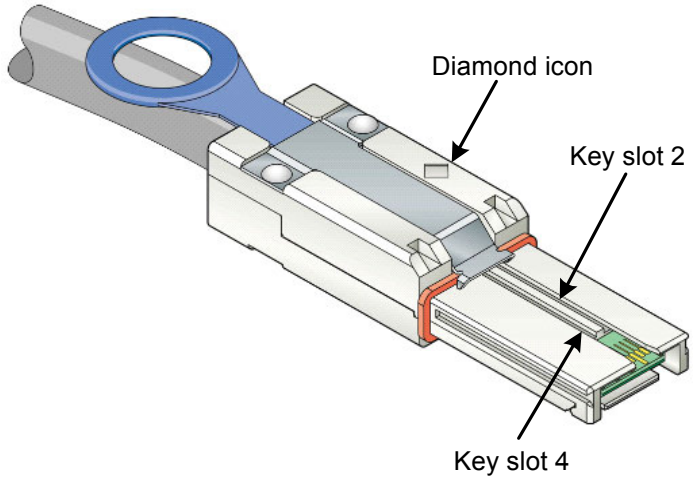


Figure 49 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port

Figure 50 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see

figure 58, figure 61, and figure 64 in 5.4.3.4.1.2) or an enclosure in port (see figure 60, figure 63, and figure 66 in 5.4.3.4.1.2).

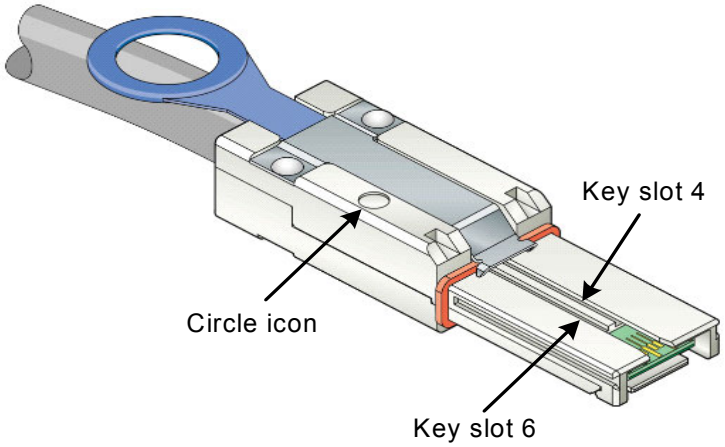


Figure 50 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure in port

Figure 51 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 61 and figure 64 in 5.4.3.4.1.2), an enclosure out port (see figure 62 and figure 65 in 5.4.3.4.1.2), or an enclosure in port (figure 63 and figure 66 in 5.4.3.4.1.2).

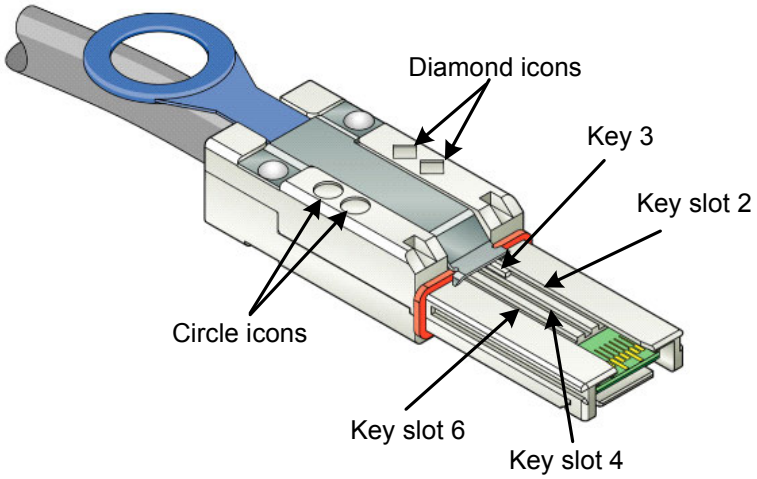


Figure 51 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 52 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal

port (see figure 61 and figure 64 in 5.4.3.4.1.2) or an enclosure out port (see figure 62 and figure 65 in 5.4.3.4.1.2).

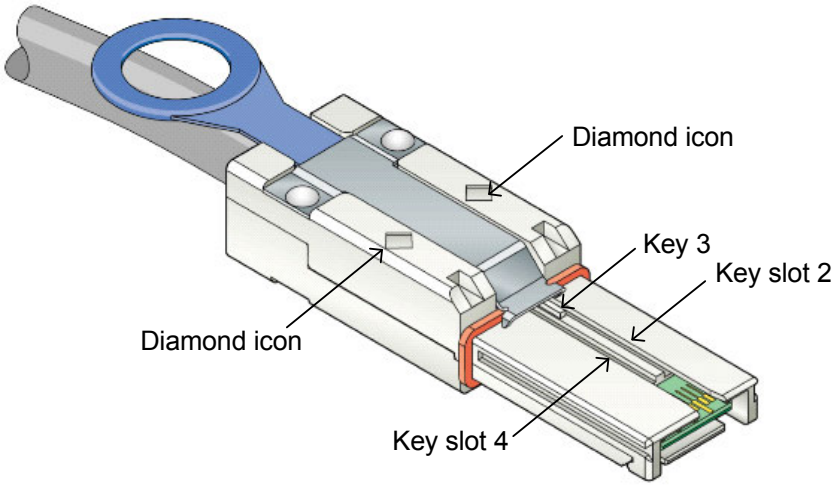


Figure 52 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port

Figure 53 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 61 and figure 64 in 5.4.3.4.1.2) or an enclosure in port (see figure 63 and figure 66 in 5.4.3.4.1.2).

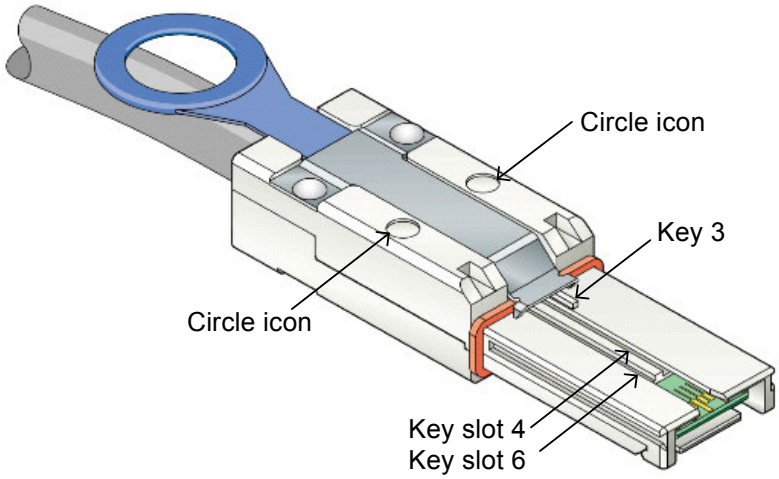


Figure 53 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure in port

Figure 54 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal

port (see figure 64 in 5.4.3.4.1.2), an enclosure out port (see figure 65 in 5.4.3.4.1.2), or an enclosure in port (see figure 66 in 5.4.3.4.1.2).

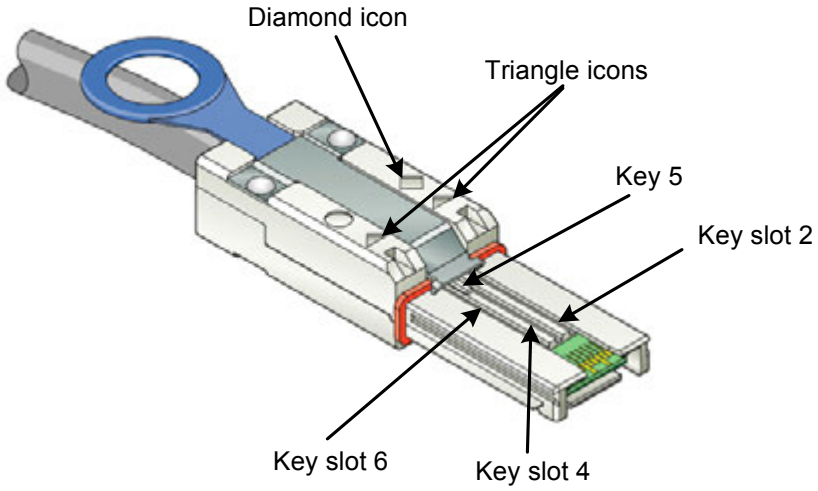


Figure 54 — Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 55 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 64 in 5.4.3.4.1.2) or enclosure out port (see figure 65 in 5.4.3.4.1.2).

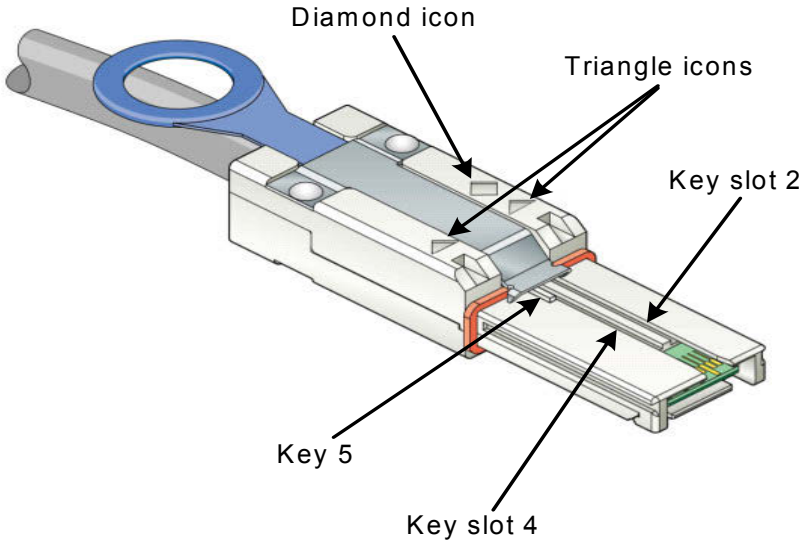


Figure 55 — Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port

Figure 56 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 64 in 5.4.3.4.1.2) or an enclosure in port (see figure 66 in 5.4.3.4.1.2).

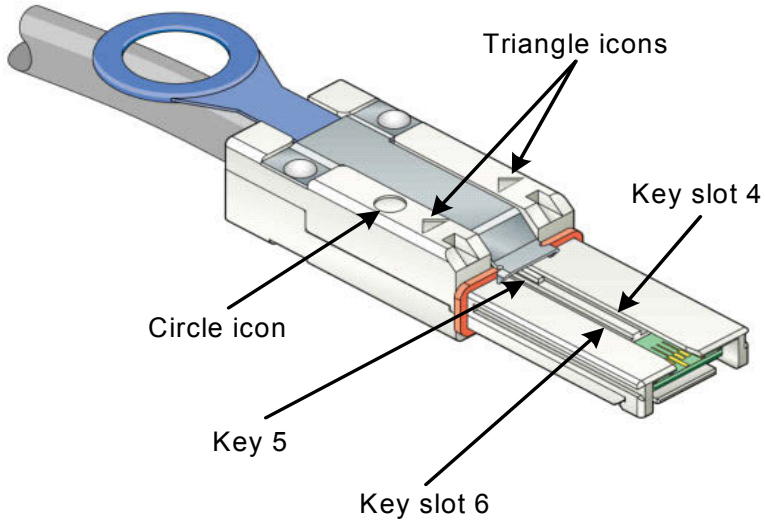


Figure 56 — Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure in port

5.4.3.4.1.2 Mini SAS 4x receptacle connector

The Mini SAS 4x receptacle connector is the fixed (receptacle) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086. The Mini SAS 4x receptacle connector should not be used for rates greater than 6 Gbit/s.

A Mini SAS 4x receptacle connector may be used by one or more SAS devices (e.g., one SAS device using physical links 0 and 3, another using physical link 1, and a third using physical link 2).

A Mini SAS 4x receptacle connector shall be used by no more than one expander device at a time, and all physical links shall be used by the same expander port (i.e., all the expander phys shall have the same routing attribute (e.g., subtractive or table) (see SPL-4)).

Figure 57 shows the Mini SAS 4x receptacle connector.

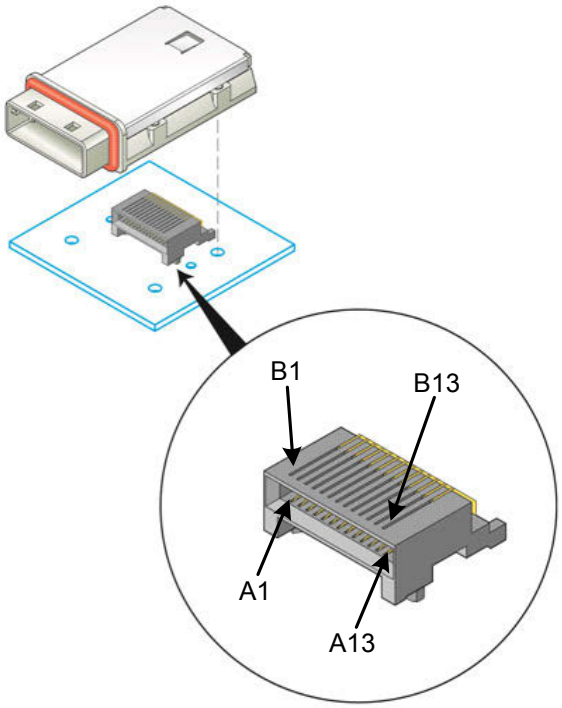


Figure 57 — Mini SAS 4x receptacle connector

Table 23 (see 5.4.3.4.1.3) and table 24 (see 5.4.3.4.1.3) define the pin assignments for the Mini SAS 4x receptacle connector.

Mini SAS 4x receptacle connectors and Mini SAS 4x active receptacle connectors shall include keys and key slots to prevent attachment to Mini SAS 4x cable plug connectors (see 5.4.3.4.1.1) without matching keys and key slots.

Table 22 defines the icons that shall be placed on or near Mini SAS 4x receptacle connectors and the key and key slot positions (see SFF-8088) that shall be used by Mini SAS 4x receptacle connectors.

Table 22 — Mini SAS 4x receptacle connector icons, key positions, and key slot positions

Electrical compliance	Use	Icons	Key position	Key slot position	Reference
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	End device or enclosure universal port	Diamond and circle	4	none	Figure 58
	Enclosure out port	Diamond	2	none	Figure 59
	Enclosure in port	Circle	6	none	Figure 60
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [b]	End device or enclosure universal port	Two diamonds and two circles	4	3	Figure 61
	Enclosure out port	Two diamonds	2	3	Figure 62
	Enclosure in port	Two circles	6	3	Figure 63
	End device or enclosure universal port	Two triangles, diamond, and circle	4	3, 5	Figure 64 [c]
	Enclosure out port	Two triangles and diamond	2	3, 5	Figure 65 [c]
	Enclosure in port	Two triangles and circle	6	3, 5	Figure 66 [c]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[c] Mini SAS 4x active receptacle.

Figure 58 shows the key on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 48, figure 49, and figure 50 (see 5.4.3.4.1.1) may be attached to this connector.

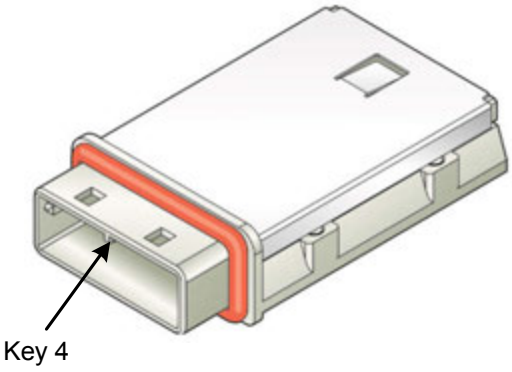


Figure 58 — Mini SAS 4x receptacle connector - end device or enclosure universal port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 59 shows the key on a Mini SAS 4x receptacle connector used by an enclosure out port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 48 and figure 49 (see 5.4.3.4.1.1) may be attached to this connector.

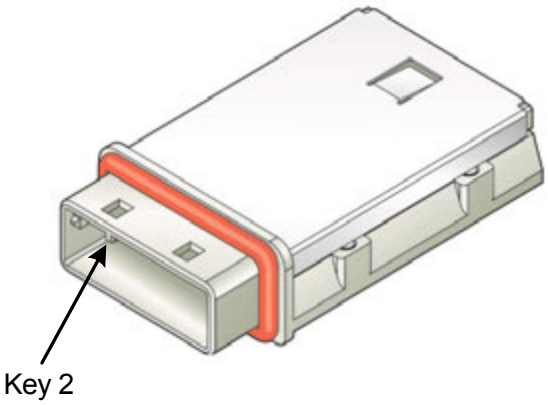


Figure 59 — Mini SAS 4x receptacle connector - enclosure out port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 60 shows the key on a Mini SAS 4x receptacle connector used by an enclosure in port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 48 and figure 50 (see 5.4.3.4.1.1) may be attached to this connector.

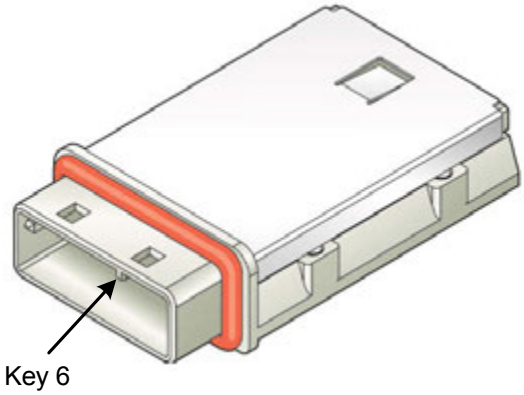


Figure 60 — Mini SAS 4x receptacle connector - enclosure in port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 61 shows the key and key slot on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 49, figure 50, figure 51, figure 52, and figure 53 (see 5.4.3.4.1.1) may be attached to this connector.

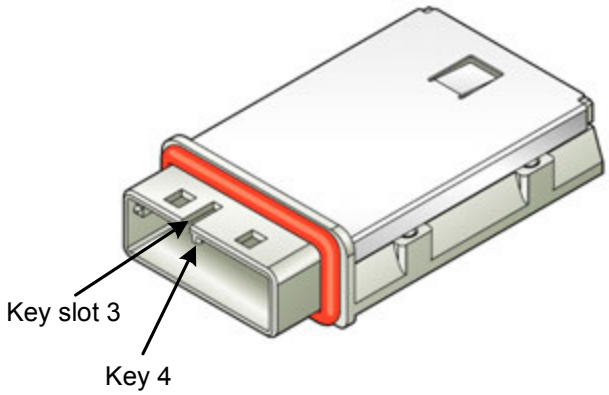


Figure 61 — Mini SAS 4x receptacle connector - end device or enclosure universal port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 62 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 49, figure 51, and figure 52, (see 5.4.3.4.1.1) may be attached to this connector.

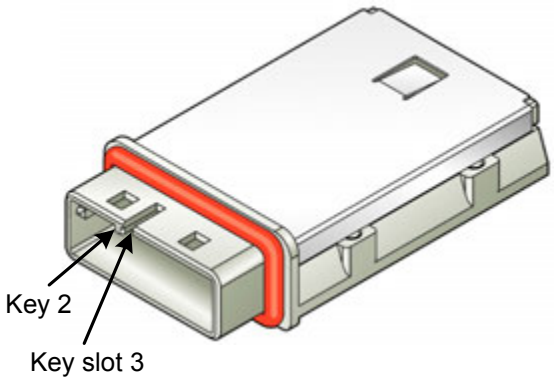


Figure 62 — Mini SAS 4x receptacle connector - enclosure out port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 63 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 50, figure 51, and figure 53 (see 5.4.3.4.1.1) may be attached to this connector.

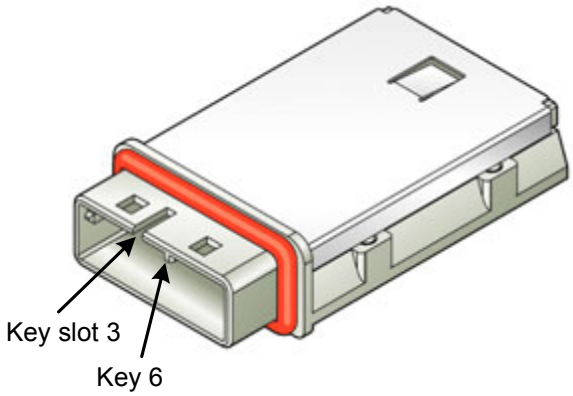


Figure 63 — Mini SAS 4x receptacle connector - enclosure in port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 64 shows a Mini SAS 4x active receptacle connector used by end devices or an enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 49, figure 50, figure 51, figure 52, figure 53, figure 54, figure 55, and figure 56 (see 5.4.3.4.1.1) may be attached to this connector.

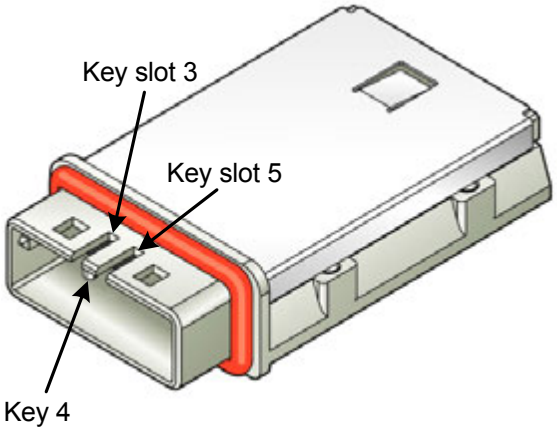


Figure 64 — Mini SAS 4x active receptacle connector - end device or enclosure universal port

Figure 65 shows an Mini SAS 4x active receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 49, figure 51, figure 52, figure 54, and figure 55 (see 5.4.3.4.1.1) may be attached to this connector.

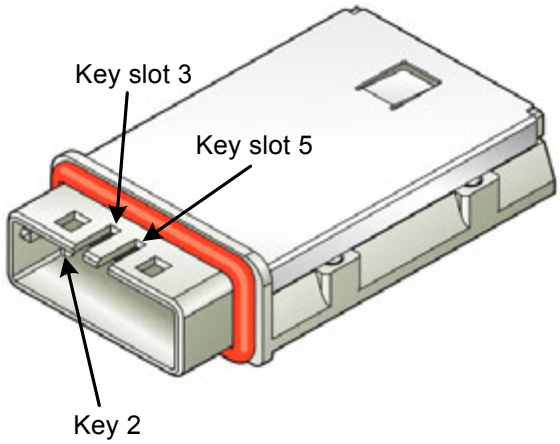


Figure 65 — Mini SAS 4x active receptacle connector - enclosure out port

Figure 66 shows an Mini SAS 4x active receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 48, figure 50, figure 51, figure 53, figure 54, and figure 56 (see 5.4.3.4.1.1) may be attached to this connector.

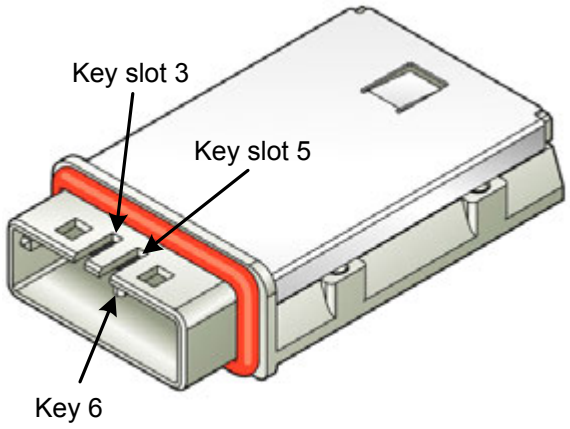


Figure 66 — Mini SAS 4x active receptacle connector - enclosure in port

5.4.3.4.1.3 Mini SAS 4x connector pin assignments

Table 23 defines the pin assignments for Mini SAS 4x cable plug connectors (see 5.4.3.4.1.1) and Mini SAS 4x receptacle connectors (see 5.4.3.4.1.2) for applications using one, two, three, or four of the physical links.

Table 23 — Mini SAS 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
RX 2+	N/C	N/C	A8	A8	
RX 2-	N/C	N/C	A9	A9	
RX 3+	N/C	N/C	N/C	A11	
RX 3-	N/C	N/C	N/C	A12	
TX 0+	B2	B2	B2	B2	
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
TX 2+	N/C	N/C	B8	B8	
TX 2-	N/C	N/C	B9	B9	
TX 3+	N/C	N/C	N/C	B11	
TX 3-	N/C	N/C	N/C	B12	
SIGNAL GROUND	A1, A4, A7, A10, A13 B1, B4, B7, B10, B13				First
CHASSIS GROUND	Housing				N/A

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.4.1.4 Mini SAS 4x active connector pin assignments

Table 24 defines the pin assignments for Mini SAS 4x active cable plug connectors (see 5.4.3.4.1.1) and Mini SAS 4x active receptacle connectors (see 5.4.3.4.1.2) for implementations using one, two, three, or four of the physical links.

Table 24 — Mini SAS 4x active connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
RX 2+	N/C	N/C	A8	A8	
RX 2-	N/C	N/C	A9	A9	
RX 3+	N/C	N/C	N/C	A11	
RX 3-	N/C	N/C	N/C	A12	
TX 0+	B2	B2	B2	B2	
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
TX 2+	N/C	N/C	B8	B8	
TX 2-	N/C	N/C	B9	B9	
TX 3+	N/C	N/C	N/C	B11	
TX 3-	N/C	N/C	N/C	B12	
SENSE [b]	B1				
V_{CC} [c]	B13				
SIGNAL GROUND	A1, A4, A7, A10, A13, B4, B7, B10				First
CHASSIS GROUND	Housing				

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).
[b] Electrical characteristics are defined in 5.4.3.4.1.5.
[c] Electrical characteristics are defined in 5.4.3.4.1.5.

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.4.1.5 Mini SAS 4x active cable power requirements

Mini SAS 4x active cable assemblies may contain integrated circuitry (e.g., drivers, repeaters, or equalizers). To enable the operation of circuitry inside the Mini SAS 4x active cable assemblies, Mini SAS 4x active receptacle connectors provide power when connected to a Mini SAS 4x active cable assembly (see 5.4.4.2.2). Mini SAS 4x active receptacle connectors shall be intermateable with Mini SAS 4x passive cable assemblies. To be intermateable, Mini SAS 4x active receptacle connectors define a pin (i.e., SENSE (see table 24) (see 5.4.3.4.1.4)) to allow control of power. Power shall only be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x active cable assembly is present. Power shall not be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x passive cable assembly or no cable assembly is present. An example of a power supply logic circuitry design is shown in Annex H.

The voltage and current requirements for the power supplied to the Mini SAS 4x active cable receptacle enable support for Mini SAS 4x active cable assemblies with power consumption of up to 1 W per each end of the cable assembly. These requirements are defined in table 25.

Table 25 — Mini SAS 4x active cable supplied power requirements

Characteristic	Units	Minimum	Nominal	Maximum
Supply voltage	V	3.135 [a]	3.3	3.465 [b]
Supply current	mA			319.4 [c]
Current consumption	mA			288.6 [d]
Power consumption	mW			1 000 [d e]

[a] At the maximum supply current.
[b] The power supply shall not exceed this value at any current.
[c] The power supply shall deliver this amount of current at the minimum voltage of 3.135 V.
[d] Maximum consumption for each end of the active cable assembly at the maximum voltage of 3.465 V.
[e] This is a derived quantity obtained from: (maximum supply voltage) x (maximum current consumption).

The Mini SAS 4x active cable assembly shall provide a connection of the SENSE pin to ground through a 5 kΩ resistor with a relative tolerance of ±5 %.

The active cable power circuitry shall enable power to the Mini SAS 4x receptacle connector only when the presence of the sense resistor is detected and power shall be disabled if the SENSE pin is open (i.e., no Mini SAS 4x cable assembly plugged in) or shorted to ground (i.e., Mini SAS 4x passive cable plugged in).

The active cable power circuitry shall have protection against the connection of the V_{CC} pin to ground or excessive current loading.

To support hot plugging, the active cable power circuitry shall be able to detect the sense resistor and provide full current within 50 ms of active cable assembly connection.

The active cable assembly and Mini SAS active cable receptacle power pins (i.e., the V_{CC} pin and SENSE pin) shall be coupled to ground via bypass capacitors so that they possess low impedance to ground from 100 MHz to 1.5 times the fundamental frequency of the maximum baud rate supported by the attached transmitter device and the attached receiver device.

The power planes of the printed circuit board on the receptacle side shall be coupled to ground.

In implementations where the circuitry in the Mini SAS 4x active cable assembly requires voltages other than the provided 3.3 V, voltage regulators may be located within the Mini SAS 4x active cable assembly.

5.4.3.4.2 Mini SAS HD external connectors

5.4.3.4.2.1 Mini SAS HD 4x cable plug connector

The Mini SAS HD 4x cable plug connector is the free (plug) 36-circuit connector defined in SFF-8644.

Figure 67 shows the Mini SAS HD 4x cable plug connector.

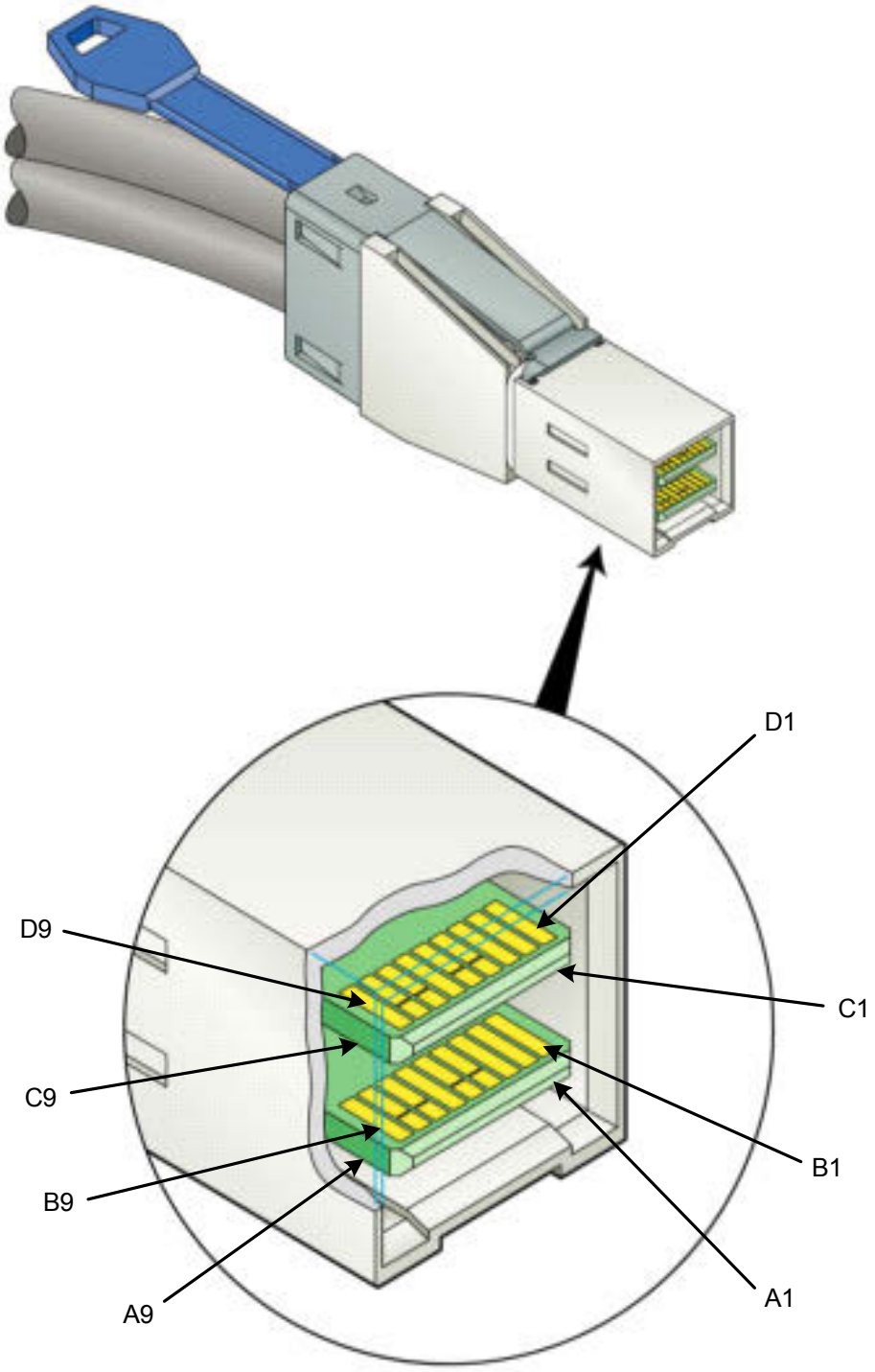


Figure 67 — Mini SAS HD 4x cable plug connector

If constructed with a pull tab as shown in figure 67, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 26 (see 5.4.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector.

The Mini SAS HD 4x cable plug connectors shall not include keying.

5.4.3.4.2.2 Mini SAS HD 8x cable plug connector

The Mini SAS HD 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8644. Figure 68 shows the Mini SAS HD 8x cable plug connector. This connector is a modular version of repeating Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1). Module labeling is shown in figure 68. See figure 67 (see 5.4.3.4.2.1) for pin designations. Mini SAS HD 8x cable plug connectors shall not include keying.

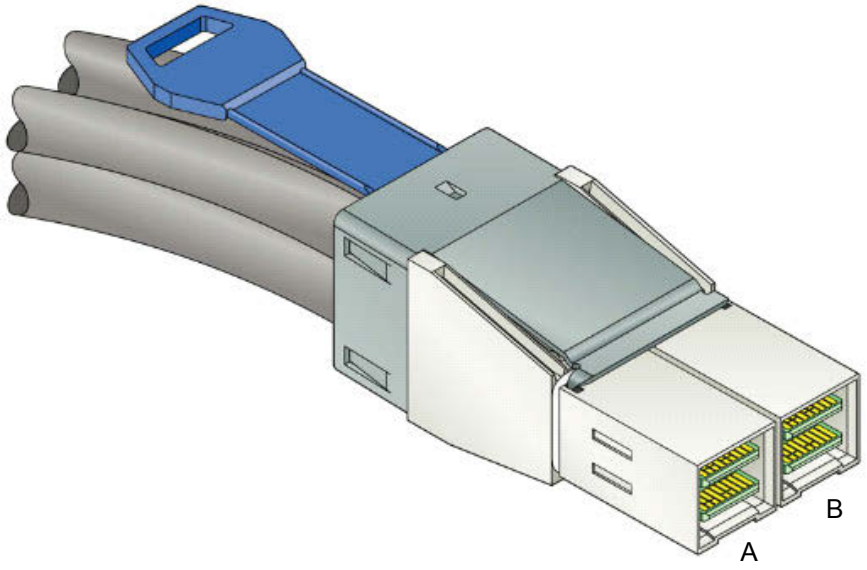


Figure 68 — Mini SAS HD 8x cable plug connector

Table 26 (see 5.4.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1). The pin assignments are repeated for each module of the Mini SAS 8x cable plug connector.

5.4.3.4.2.3 Mini SAS HD 4x receptacle connector

The Mini SAS HD 4x receptacle connector is the four-lane receptacle (fixed) connector defined in SFF-8644. Figure 69 shows the Mini SAS HD 4x receptacle connector.

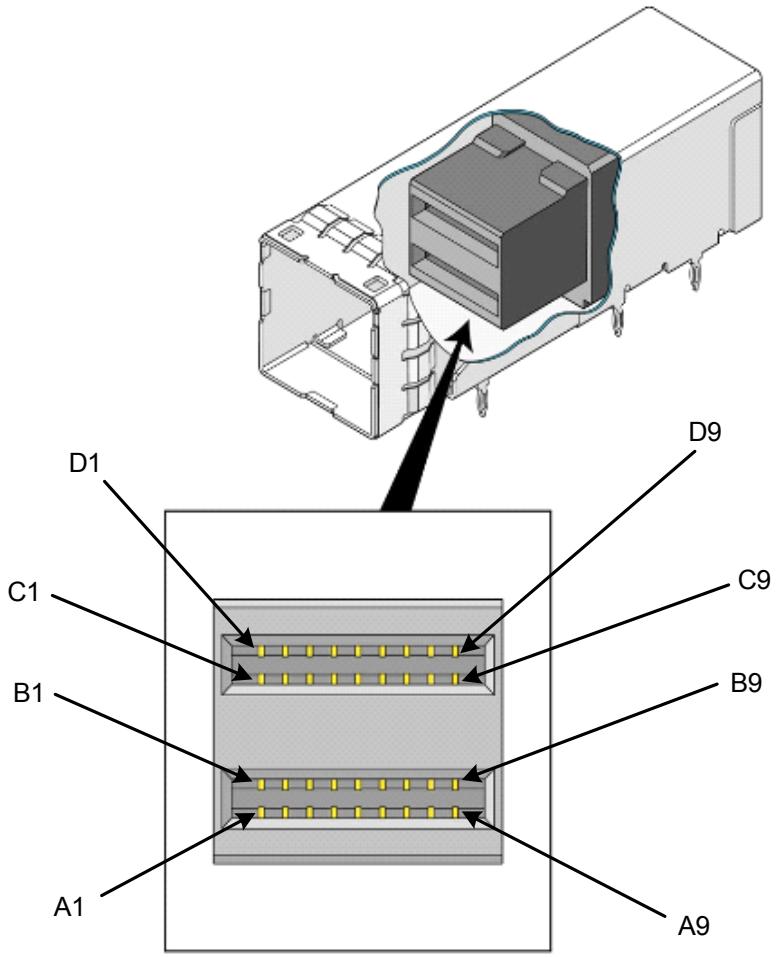


Figure 69 — Mini SAS HD 4x receptacle connector

Table 26 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 4x receptacle connector.

5.4.3.4.2.4 Mini SAS HD 8x receptacle connector

The Mini SAS HD 8x receptacle connector is a dual four-lane receptacle (fixed) connector defined in SFF-8644. Figure 70 shows the Mini SAS HD 8x receptacle connector. This connector is a modular version of

the Mini SAS HD 4x receptacle connector (see 5.4.3.4.2.3). Module labeling is shown in figure 70. See figure 69 (see 5.4.3.4.2.3) for pin designations.

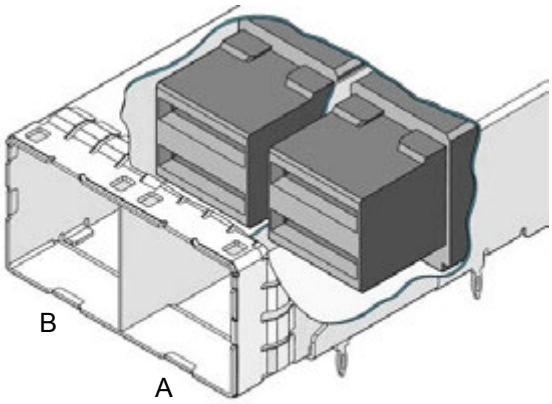


Figure 70 — Mini SAS HD 8x receptacle connector

Table 26 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 8x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.4.2.3). The Mini SAS HD 8x receptacle connector accepts one Mini SAS HD 8x plug connector (see 5.4.3.4.2.2) or one or two Mini SAS HD 4x plug connectors (see 5.4.3.4.2.1).

5.4.3.4.2.5 Mini SAS HD 16x receptacle connector

The Mini SAS HD 16x receptacle connector is a quad four-lane receptacle (fixed) connector defined in SFF-8644. Figure 71 shows the Mini SAS HD 16x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.4.3.4.2.3). Module labeling is shown in figure 71. See figure 69 (see 5.4.3.4.2.3) for pin designations.

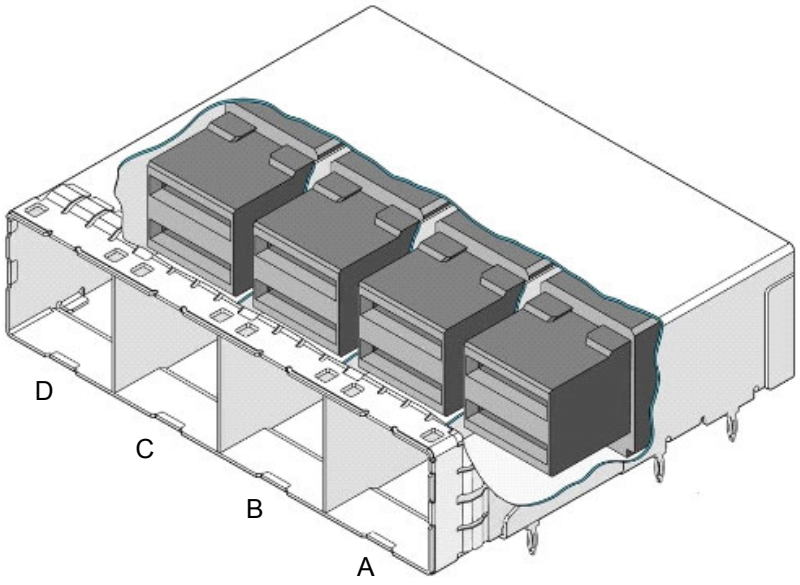


Figure 71 — Mini SAS HD 16x receptacle connector

Table 26 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 16x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.4.2.3). The Mini SAS HD 16x receptacle connector accepts:

a) one or two Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2);
b) one, two, three, or four Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1); or
c) a combination of one Mini SAS HD 8x cable plug connector (see 5.4.3.4.2.2) and one or two Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1).

A Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.4.3.4.2.6 Mini SAS HD 4x connector pin assignments

Table 26 defines the pin assignments for Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1) and Mini SAS HD 4x receptacle connectors (see 5.4.3.4.2.3) for controller applications using one, two, three, or four of the physical links.

Table 26 — Mini SAS HD 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0-	B5	B5	B5	B5	Third
RX 0+	B4	B4	B4	B4	
RX 1-	N/C	A5	A5	A5	
RX 1+	N/C	A4	A4	A4	
IntL [b]	A2	A2	A2	A2	Second
Reserved [b]	A1	A1	A1	A1	
ModPrsL [b]	B2	B2	B2	B2	
Vact [b]	B1	B1	B1	B1	
RX 2-	N/C	N/C	B8	B8	Third
RX 2+	N/C	N/C	B7	B7	
RX 3-	N/C	N/C	N/C	A8	
RX 3+	N/C	N/C	N/C	A7	
TX 0-	D5	D5	D5	D5	Third
TX 0+	D4	D4	D4	D4	
TX 1-	N/C	C5	C5	C5	
TX 1+	N/C	C4	C4	C4	
SDA [b]	C2	C2	C2	C2	Second
SCL [b]	C1	C1	C1	C1	
Vman [b]	D2	D2	D2	D2	
Vact [b]	D1	D1	D1	D1	
TX 2-	N/C	N/C	D8	D8	Third
TX 2+	N/C	N/C	D7	D7	
TX 3-	N/C	N/C	N/C	C8	
TX 3+	N/C	N/C	N/C	C7	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] The mating level indicates the physical dimension of the contact (see SFF-8644).
[b] Table 27 (see 5.4.3.4.2.7) defines the connection requirements of this signal.

5.4.3.4.2.7 Mini SAS HD external connector management interface

Each 4x module shall include a two-wire serial management interface to:

a) monitor circuitry residing in the cable assembly;
b) control circuitry residing in the cable assembly; and
c) obtain physical characteristics of the cable encoded in a non-volatile storage device located in the cable assembly.

Table 27 defines the connection requirements of the management interface signals. The following connectors shall support the signals in table 27 in each 4x module:

a) Mini SAS HD 4x receptacle connectors (see 5.4.3.4.2.3);
b) Mini SAS HD 8x receptacle connectors (see 5.4.3.4.2.4);
c) Mini SAS HD 16x receptacle connectors (see 5.4.3.4.2.5);
d) Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1); and
e) Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2).

See SFF-8449 and SFF-8636 for a complete signal definition, management interface memory map, and timing diagrams for the two-wire interface.

Table 27 — Management interface connection requirements

Signal	Connection requirements [a]
IntL	**Active Low Module Interrupt**: This pin shall be connected to Vman (see SFF-8449) on the receptacle side of the management interface. The source of the interrupt may be identified using the two-wire serial management interface. If the cable assembly supports interrupts, then the cable assembly shall assert this pin to indicate an interrupt bit has been set to one in the management interface memory map. If a cable assembly does not support interrupts, then all interrupt bits in the cable management interface memory map shall be set to zero and the cable assembly shall negate this pin (e.g., all interrupt bits of a passive cable assembly may be programmed to a clear state and the IntL pin not connected on the cable plug side of the management interface).
ModPrsL	**Active Low Module Present**: On the cable plug side of the management interface, ModPrsL shall be connected directly to the signal ground pins specified in table 26 (see 5.4.3.4.2.6). ModPrsL shall be connected to Vman (see SFF-8449) on the receptacle side of the management interface to negate this signal when the plug is not fully mated to the receptacle.
Reserved	This pin shall be not connected on the receptacle side and cable plug side of the management interface.
SCL	**Two-wire interface clock**: The receptacle side of the management interface shall connect this signal to Vman (see SFF-8449).
SDA	**Two-wire interface data**: The receptacle side of the management interface shall connect this signal to Vman (see SFF-8449).
Vact	**Active cable power**: If the receptacle side of the management interface supports active cable assemblies, then it shall provide all non-management interface power to the cable assembly on the Vact pins. To support equal loading, both Vact pins shall be connected together on the receptacle side of the management interface. If the receptacle side of the management interface does not support active cable assemblies, then the Vact pins should be not connected.
Vman	**Management interface power**: The receptacle side of the management interface shall provide power on the Vman pin to enable the management interface circuitry of the cable. Power may be removed to reset the management circuitry in the cable assembly.

[a] Electrical characteristics are defined in SFF-8449.

5.4.3.4.2.8 Mini SAS HD external connector memory map

SFF-8636 defines the Mini SAS HD external connector management interface memory map. The Mini SAS HD external cable assembly shall support the following management interface memory map registers:

a) supported SAS baud rate;
b) vendor name;
c) vendor part number;
d) vendor revision;
e) copper cable attenuation;
f) power class;
g) minimum operating voltage;
h) transmitter technology;
i) cable width; and
j) propagation delay.

5.4.3.4.3 QSFP+ connectors

5.4.3.4.3.1 QSFP+ cable plug

The QSFP+ cable plug connector is the free (plug) 38-circuit connector defined in SFF-8685. Figure 72 shows the QSFP+ cable plug connector.

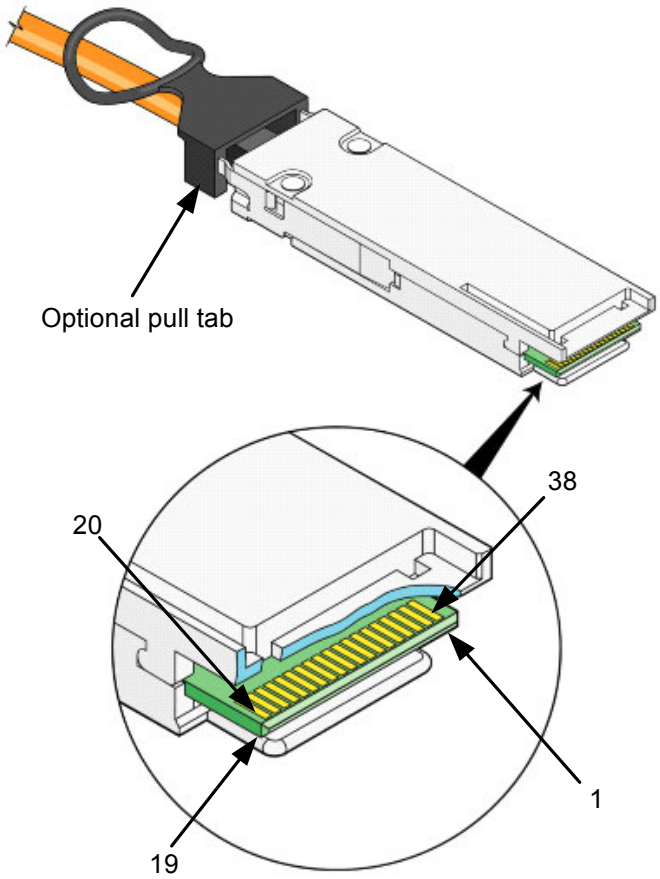


Figure 72 — QSFP+ cable plug connector

Table 28 (see 5.4.3.4.3.3) defines the pin assignments for the QSFP+ cable plug connector.

The QSFP+ cable plug connectors shall not include keying.

5.4.3.4.3.2 QSFP+ receptacle

The QSFP+ receptacle connector is the fixed (receptacle) 38-circuit connector defined in SFF-8685. Figure 73 shows the QSFP+ receptacle connector.

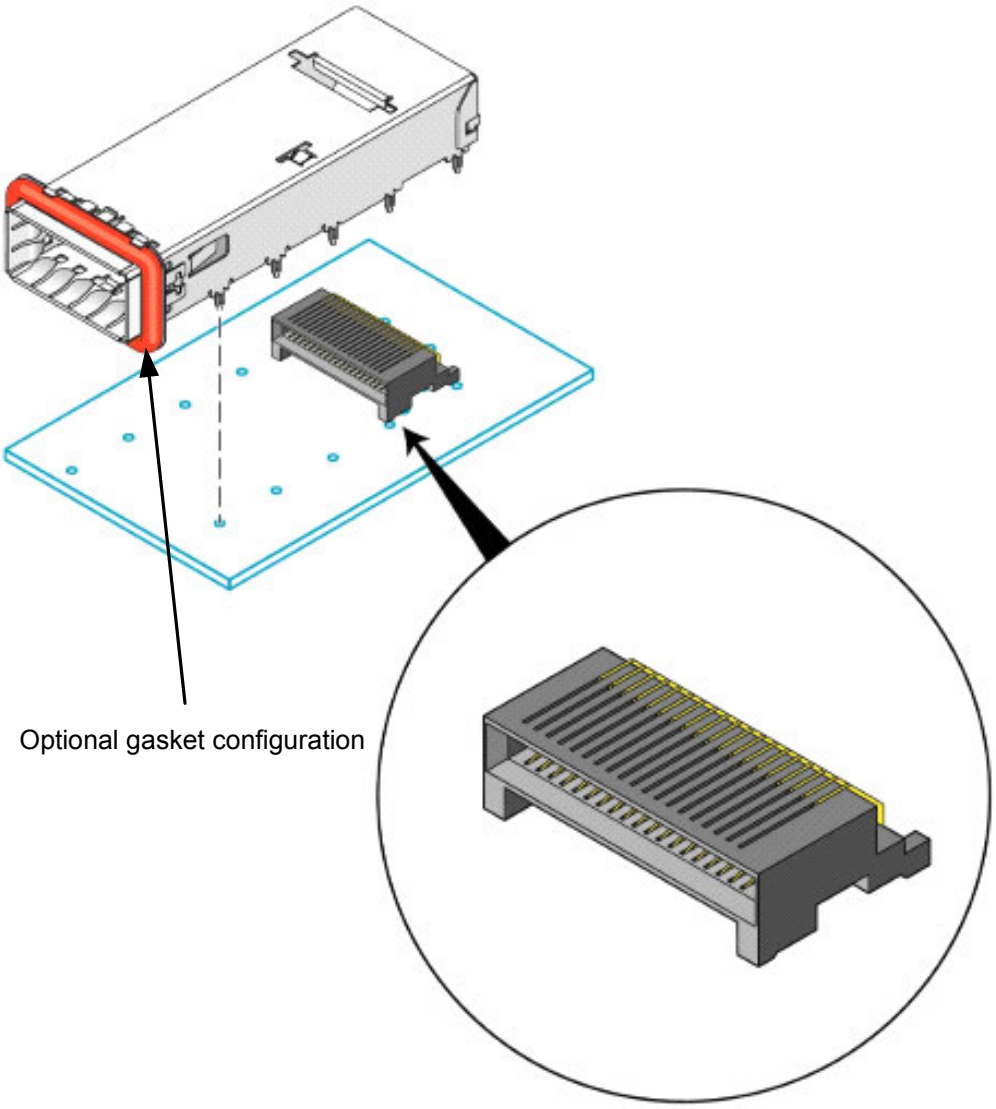


Figure 73 — QSFP+ receptacle connector

Table 28 (see 5.4.3.4.3.3) defines the pin assignments for the QSFP+ receptacle connector.

The QSFP+ receptacle connectors shall not include keying.

5.4.3.4.3.3 QSFP+ connector pin assignments

Table 28 defines the pin assignments for QSFP+ connectors (see 5.4.3.4.3.1 and 5.4.3.4.3.2). Specific pins are used to provide managed cable communication and power to the cable assembly.

Table 28 — QSFP+ connector pin assignments (part 1 of 2)

Pin	Signal	Description	Mating level [a]
1	GND [b]	Ground	First
2	Tx2n	Transmitter inverted data input	Third
3	Tx2p	Transmitter non-inverted data input	Third
4	GND [b]	Ground	First
5	Tx4n	Transmitter inverted data input	Third
6	Tx4p	Transmitter non-inverted data input	Third
7	GND [b]	Ground	First
8	ModSelL	Module select	Third
9	ResetL	Module reset	Third
10	Vcc Rx [c]	+3.3 V power supply receiver	Second
11	SCL	two-wire serial interface clock	Third
12	SDA	two-wire serial interface data	Third
13	GND [b]	Ground	First
14	Rx3p	Receiver non-inverted data output	Third
15	Rx3n	Receiver inverted data output	Third
16	GND [b]	Ground	First
17	Rx1p	Receiver non-inverted data output	Third
18	Rx1n	Receiver inverted data output	Third
19	GND [b]	Ground	First
20	GND [b]	Ground	First
21	Rx2n	Receiver inverted data output	Third
22	Rx2p	Receiver non-inverted data output	Third
23	GND [b]	Ground	First
24	Rx4n	Receiver inverted data output	Third
25	Rx4p	Receiver non-inverted data output	Third
26	GND [b]	Ground	First
27	ModPrsL	Module present	Third

[a] The mating level indicates the physical dimension of the contact. See SFF-8685.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

Table 28 — QSFP+ connector pin assignments (part 2 of 2)

Pin	Signal	Description	Mating level [a]
28	IntL	Interrupt	Third
29	Vcc Tx [c]	+3.3 V power supply transmitter	Second
30	Vcc1 [c]	+3.3 V power supply	Second
31	LPMode	Low power mode	Third
32	GND [b]	Ground	First
33	Tx3p	Transmitter non-inverted data input	Third
34	Tx3n	Transmitter inverted data input	Third
35	GND [b]	Ground	First
36	Tx1p	Transmitter non-inverted data input	Third
37	Tx1n	Transmitter inverted data input	Third
38	GND [b]	Ground	First

[a] The mating level indicates the physical dimension of the contact. See SFF-8685.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

5.4.3.4.3.4 QSFP+ memory map

The memory map for QSFP+ is used for identification information, cable characteristics, control functions, and digital monitoring. The two-wire serial interface is required for all QSFP+ devices. SFF-8636 defines the supported SAS baud rate codes. See SFF-8636 for register map details and the operation of the two-wire serial interface.

5.4.4 Cable assemblies

5.4.4.1 SAS internal cable assemblies

5.4.4.1.1 SAS Drive cable assemblies

A SAS Drive cable assembly is either:

a) a single-port SAS Drive cable assembly;
b) a dual-port SAS Drive cable assembly; or
c) a MultiLink SAS Drive cable assembly.

A SAS single-port Drive cable assembly or SAS dual-port Drive cable assembly has:

a) a SAS Drive cable receptacle connector (see 5.4.3.3.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL-4).

A SAS MultiLink Drive cable assembly has:

a) a SAS MultiLink Drive cable receptacle connector (see 5.4.3.3.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL-4).

The power, READY LED, and POWER DISABLE signal connection is vendor specific.

A SAS initiator device shall use a SATA host plug connector (see SATA) for connection to a SAS Drive cable assembly. The signal assignment for the SAS initiator device or expander device (see SPL-4) with this connector shall be the same as that defined for a SATA host (see SATA).

Figure 74 shows the Single-port SAS Drive cable assembly.

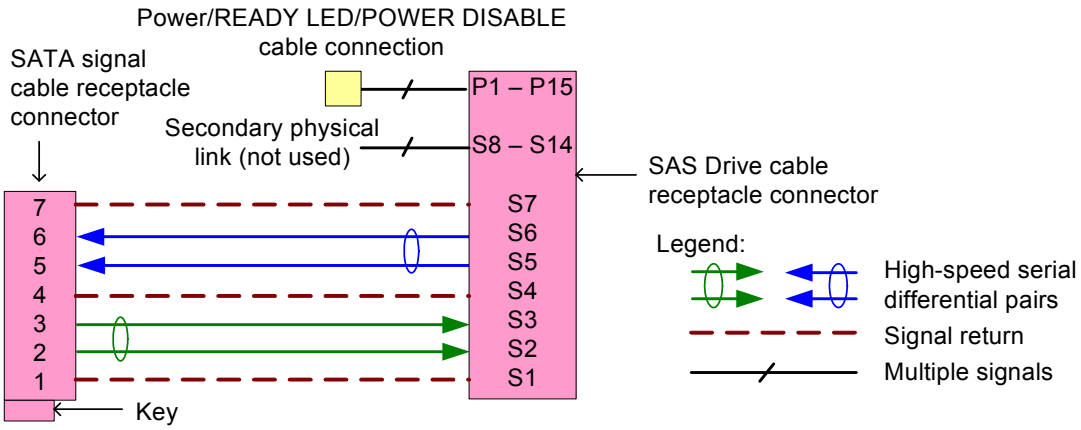


Figure 74 — Single-port SAS Drive cable assembly

Figure 75 shows the Dual-port SAS Drive cable assembly.

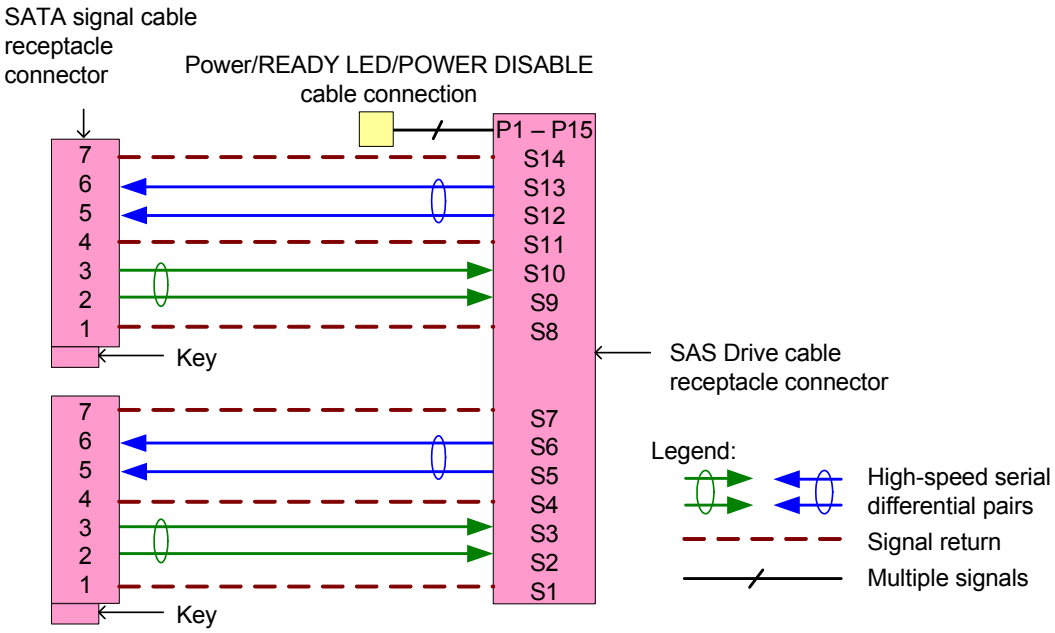


Figure 75 — Dual-port SAS Drive cable assembly

Figure 76 shows the MultiLink SAS Drive cable assembly.

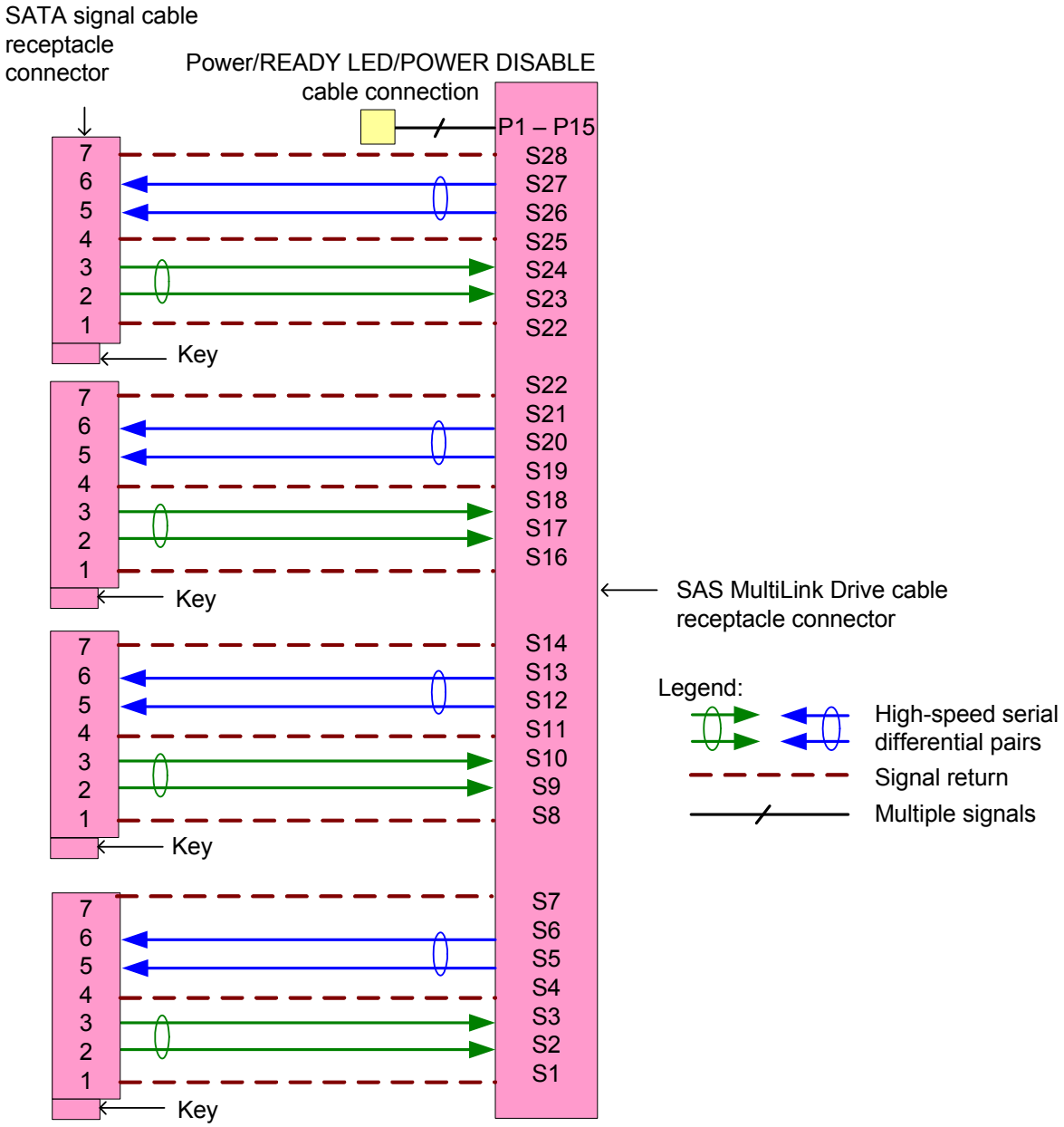


Figure 76 — MultiLink SAS Drive cable assembly

5.4.4.1.2 SAS internal symmetric cable assemblies

5.4.4.1.2.1 SAS internal symmetric cable assemblies overview

A SAS internal symmetric cable assembly has:

a) a Mini SAS 4i cable plug connector (see 5.4.3.3.2.1) on each end (see 5.4.4.1.2.2);
b) a Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1) on each end (see 5.4.4.1.2.3);
c) a Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) on each end (see 5.4.4.1.2.4);
d) a Mini SAS 4i cable plug connector (see 5.4.3.3.2.1) on one end and a Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1) on the other end (see 5.4.4.1.2.5);
e) a SAS SlimLine 4i cable plug connector (see 5.4.3.3.4.1) on each end (see 5.4.4.1.2.6);
f) a SAS SlimLine 4i cable plug connector (see 5.4.3.3.4.1) on one end and a Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1) on the other end (see 5.4.4.1.2.7);
g) a SAS SlimLine 4i cable plug connector (see 5.4.3.3.4.1) on one end and a Mini SAS 4i cable plug connector (see 5.4.3.3.2.1) on the other end (see 5.4.4.1.2.8);
h) a SAS SlimLine 8i cable plug connector (see 5.4.3.3.4.2) on each end (see 5.4.4.1.2.9);
i) a SAS SlimLine 8i cable plug connector (see 5.4.3.3.4.2) on one end and a Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) on the other end (see 5.4.4.1.2.10);
j) a SAS MiniLink 4i cable plug connector (see 5.4.3.3.4.1) on each end (see 5.4.4.1.2.11);
k) a SAS MiniLink 4i cable plug connector (see 5.4.3.3.4.1) on one end and a Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1) on the other end (see 5.4.4.1.2.12);
l) a SAS MiniLink 4i cable plug connector (see 5.4.3.3.4.1) on one end and a Mini SAS 4i cable plug connector (see 5.4.3.3.2.1) on the other end (see 5.4.4.1.2.13);
m) a SAS MiniLink 8i cable plug connector (see 5.4.3.3.4.2) on each end (see 5.4.4.1.2.14); or
n) a SAS MiniLink 8i cable plug connector (see 5.4.3.3.4.2) on one end and a Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2) on the other end (see 5.4.4.1.2.15).

In a SAS internal symmetric cable assembly, the TX signals on one end shall be connected to RX signals on the other end (e.g., a TX+ of one connector shall connect to an RX+ of the other connector). SAS internal symmetric cable assemblies should be labeled to indicate how many physical links are included (e.g., 1X, 2X, 3X, and 4X on each connector's housing).

In addition to the signal return connections shown in the figures, one or more of the signal returns may be connected together in the cable assemblies.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND 0 of the controller is attached to SIDEBAND 0 of the backplane). The SIDEBAND 8 and SIDEBAND 9 signals are not supported on the Mini SAS 4i cable plug connector (see 5.4.3.3.2.1), the Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1), or the Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND 0 of one controller is attached to SIDEBAND 7 of the other controller). The SIDEBAND 8 signal and SIDEBAND 9 signal are not supported on the Mini SAS 4i cable plug connector (see 5.4.3.3.2.1), the Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1), or the Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2).

5.4.4.1.2.2 SAS internal symmetric cable assembly - Mini SAS 4i

Figure 77 shows the SAS internal cable assembly with Mini SAS 4i cable plug connectors at each end.

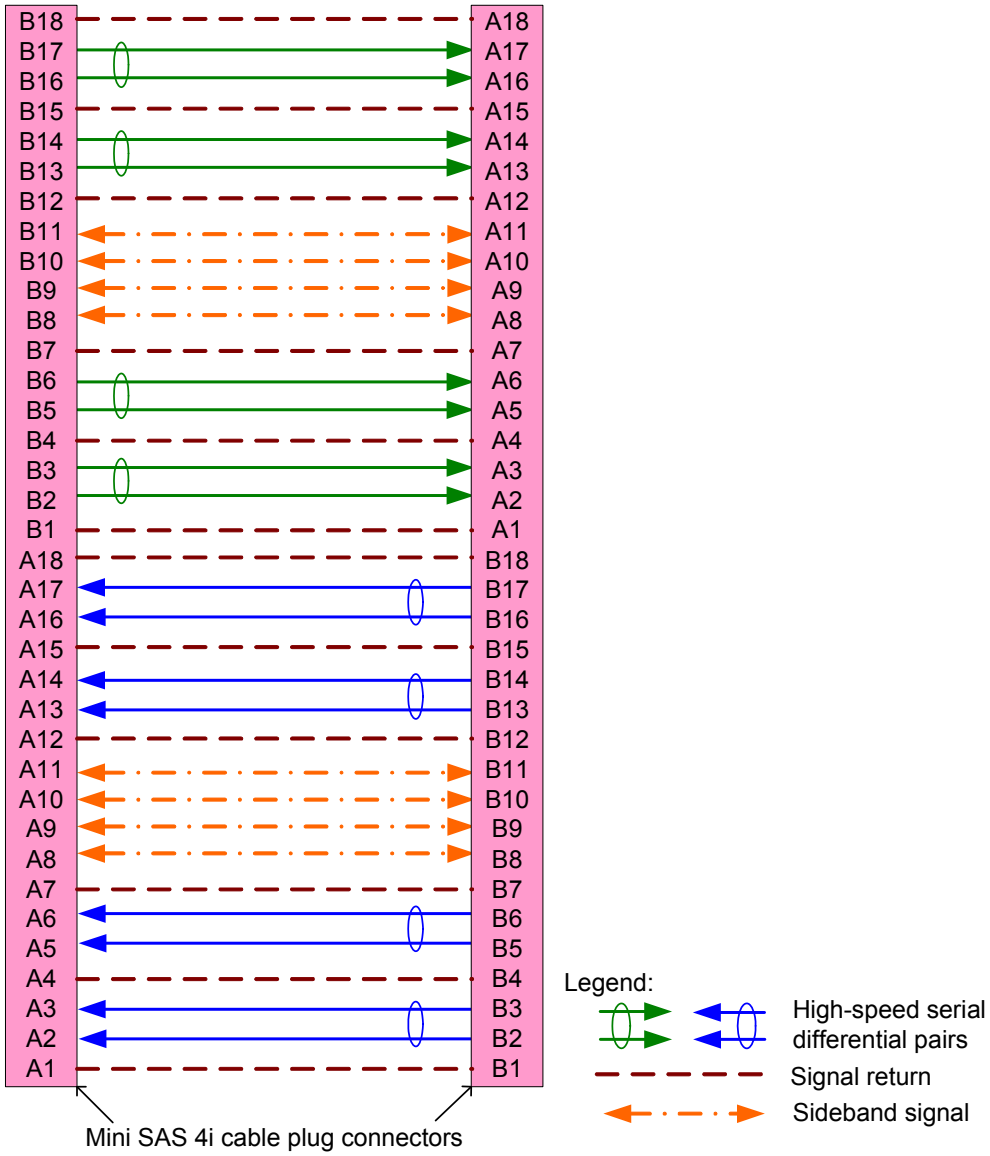


Figure 77 — SAS internal symmetric cable assembly - Mini SAS 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.3 SAS internal symmetric cable assembly - Mini SAS HD 4i

Figure 78 shows the SAS internal cable assembly with Mini SAS HD 4i cable plug connectors at each end.

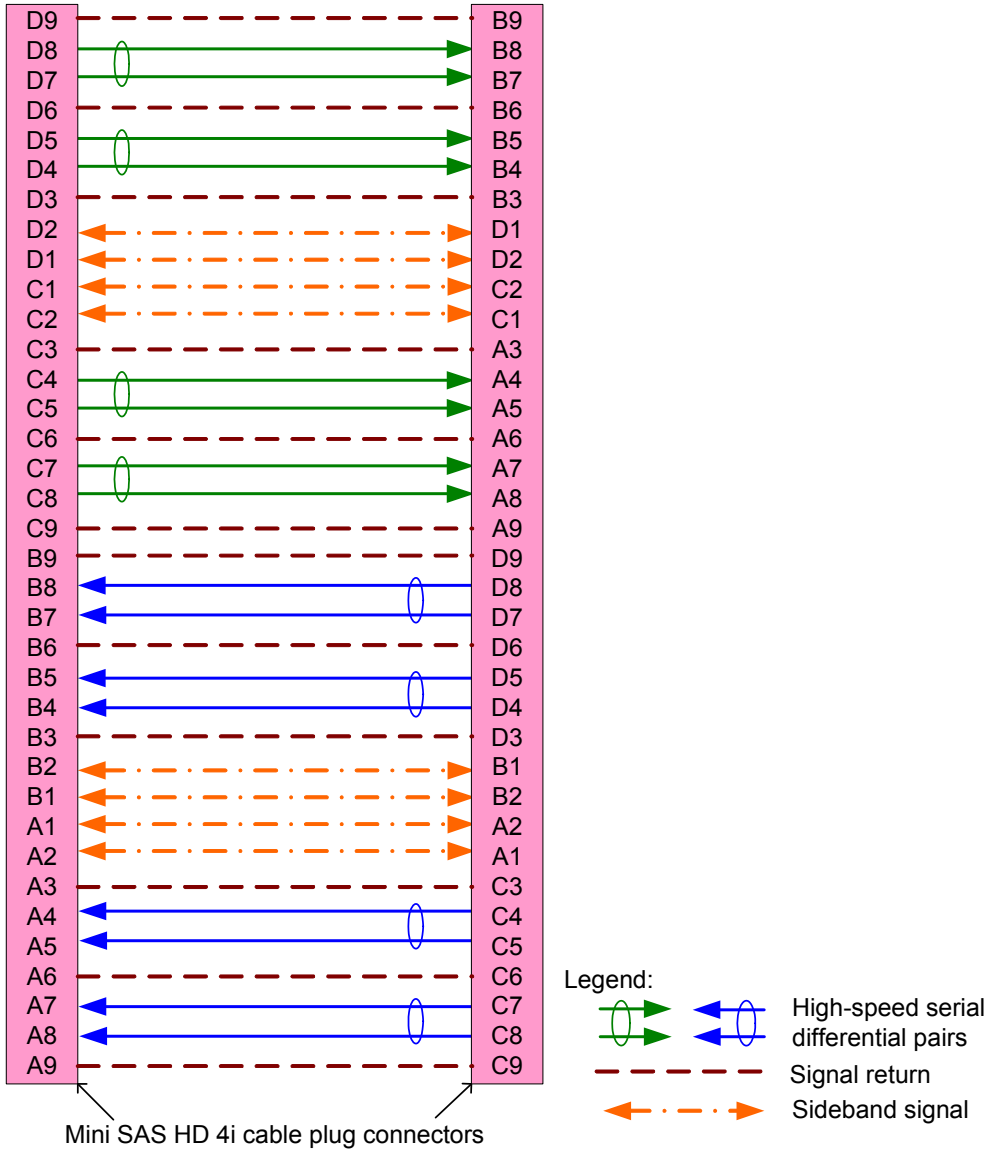


Figure 78 — SAS internal symmetric cable assembly - Mini SAS HD 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.4 SAS internal symmetric cable assembly - Mini SAS HD 8i

Figure 79 shows the SAS internal cable assembly with Mini SAS HD 8i cable plug connectors at each end.

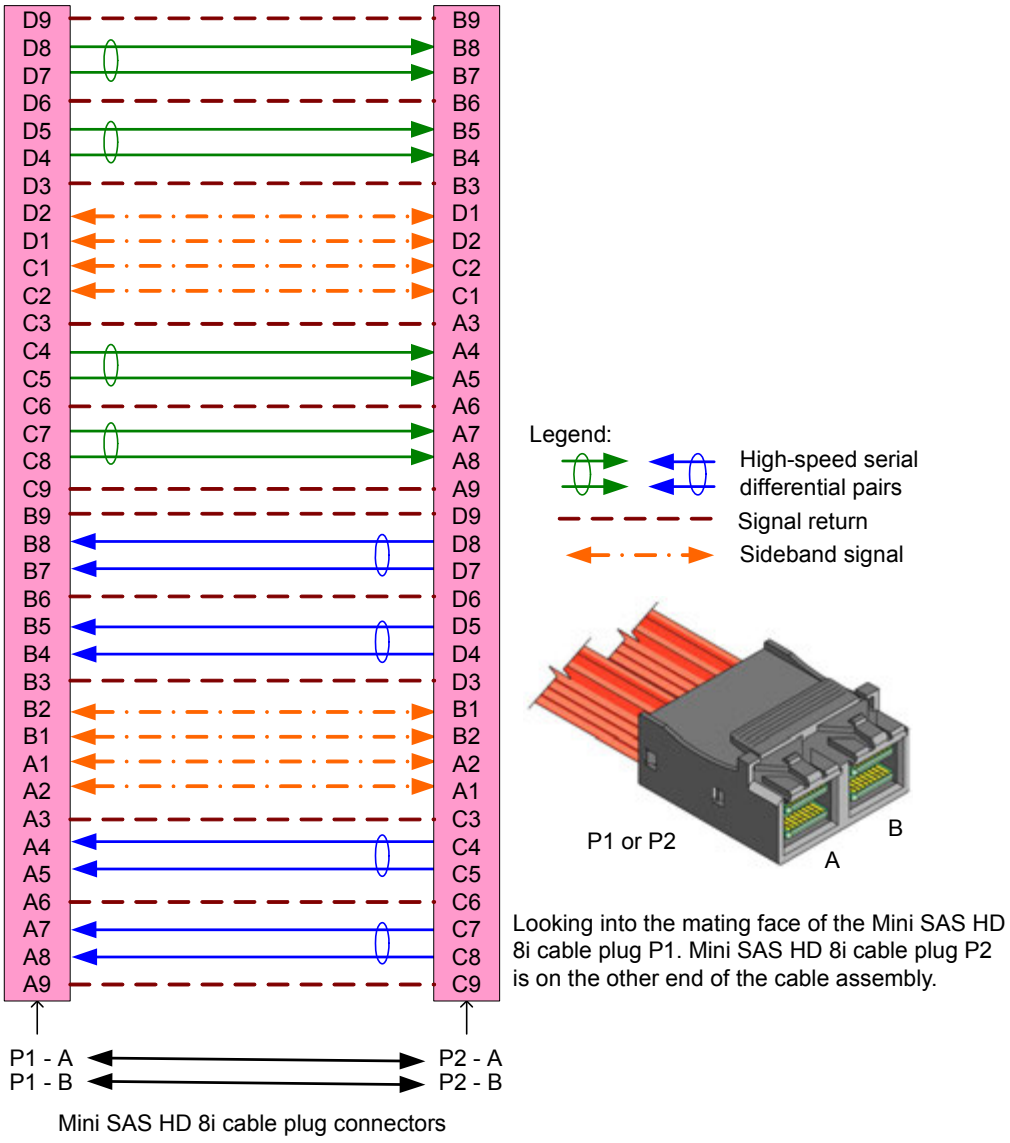


Figure 79 — SAS internal symmetric cable assembly - Mini SAS HD 8i

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.3.3.6 for connector module pin assignments.

5.4.4.1.2.5 SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

Figure 80 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable plug connector at one end and a Mini SAS HD 4i cable plug connector at the other end.

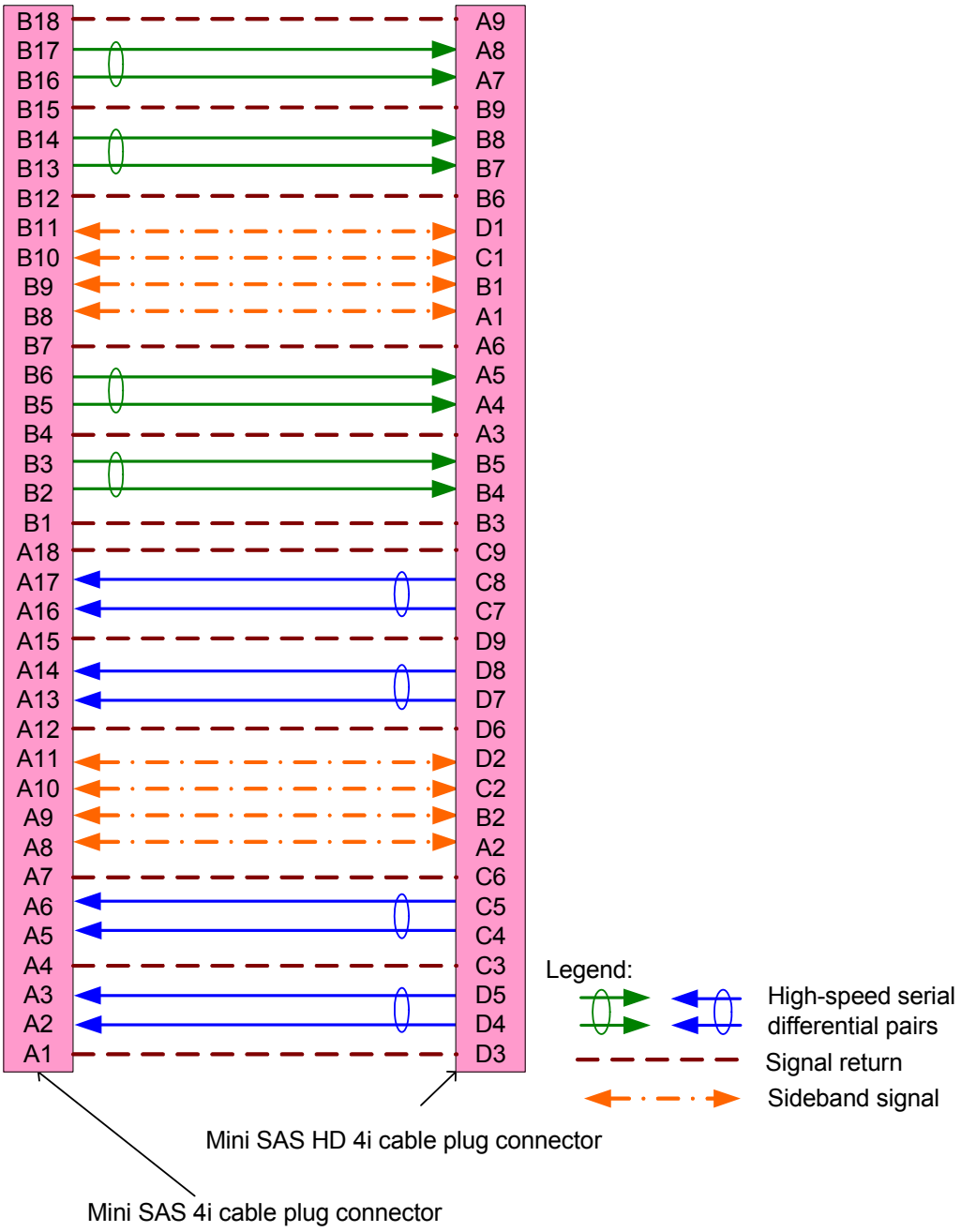


Figure 80 — SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.6 SAS internal symmetric cable assembly - SAS SlimLine 4i

Figure 81 shows the SAS internal cable assembly with SAS Slimline 4i cable plug connectors at each end.

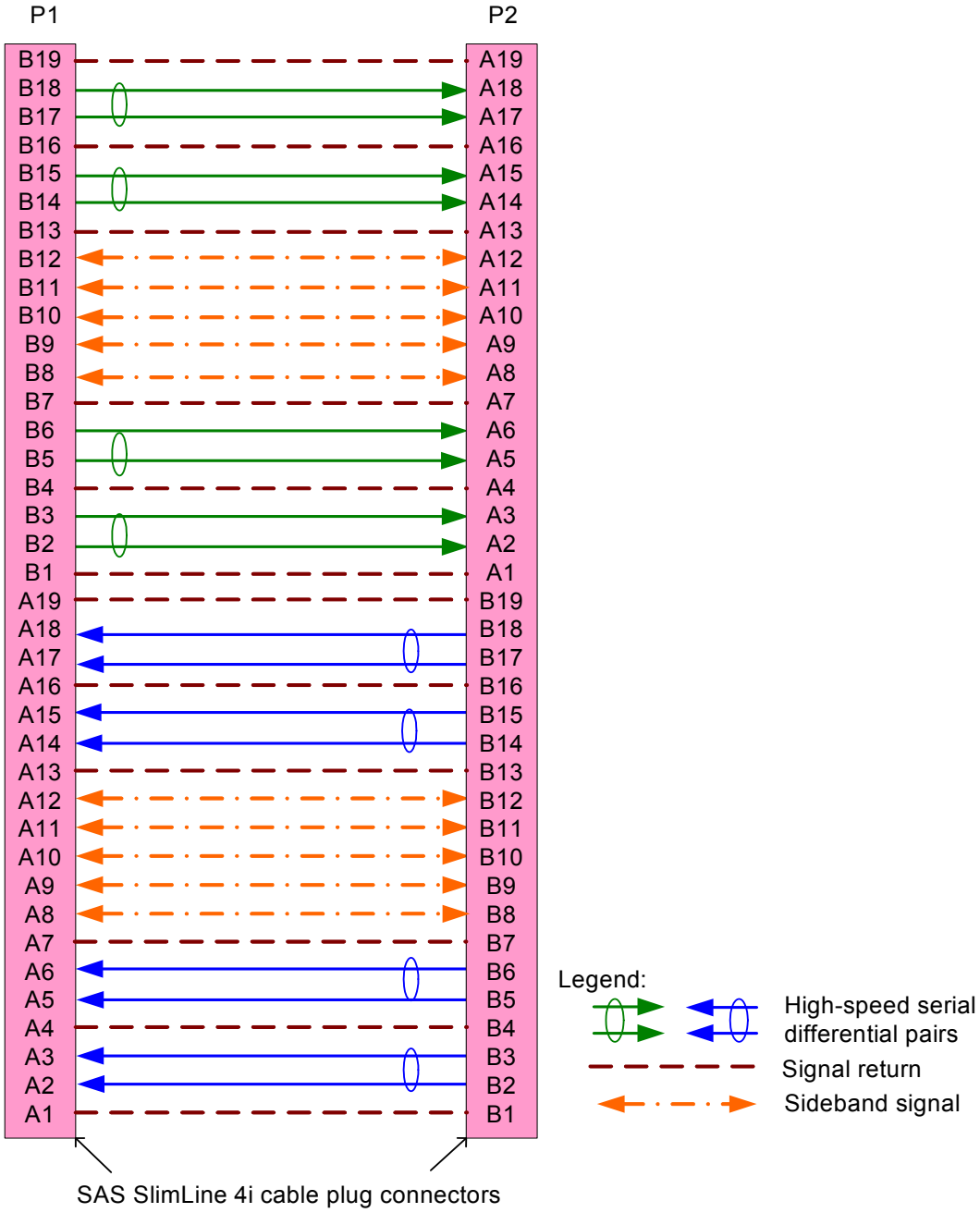


Figure 81 — SAS internal symmetric cable assembly - SAS SlimLine 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.7 SAS internal symmetric cable assembly - SAS SlimLine 4i to Mini SAS HD 4i

Figure 82 shows the SAS internal cable assembly with a SAS SlimLine 4i cable plug connector on one end and a Mini SAS HD 4i cable plug connector on the other end.

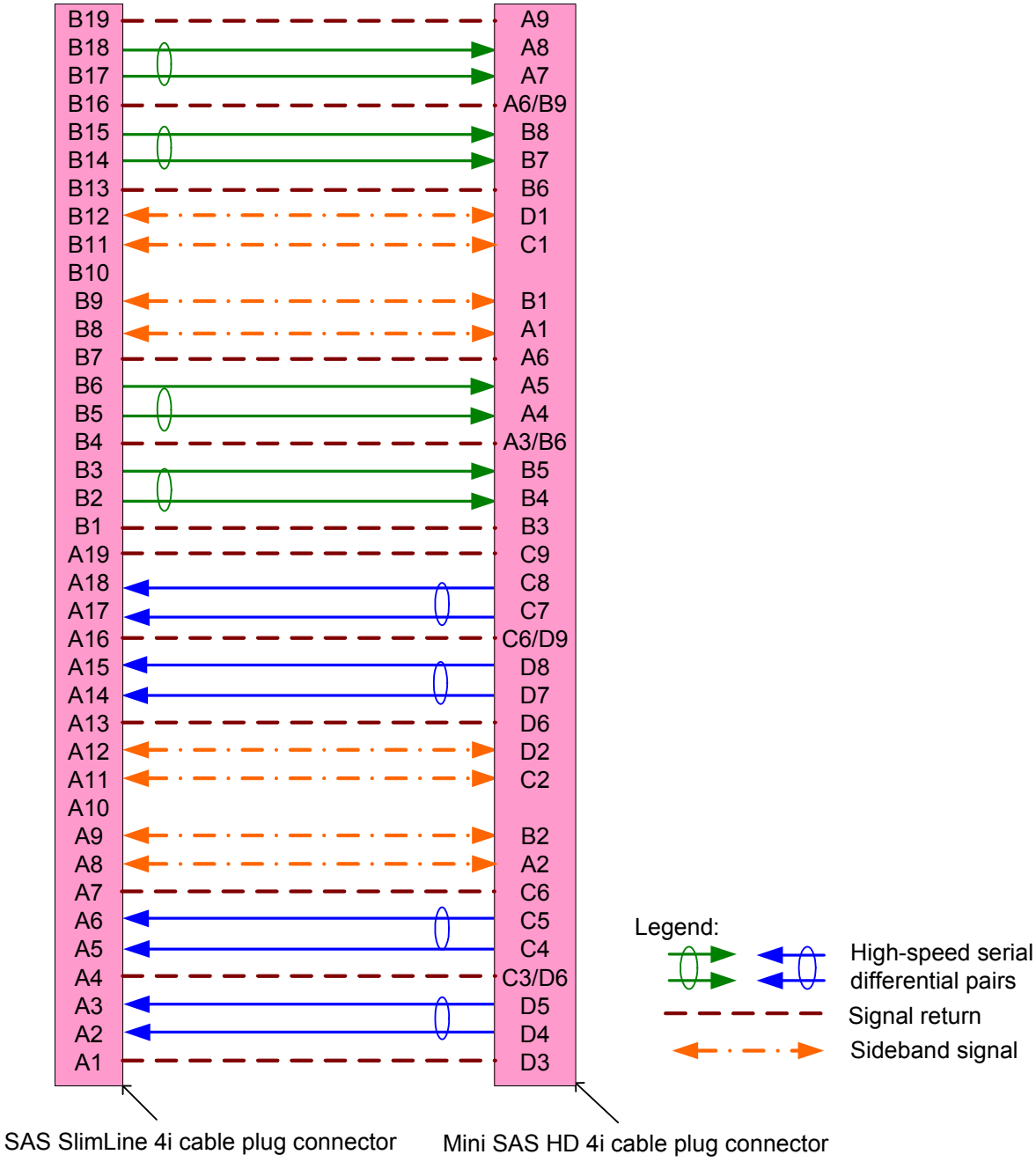


Figure 82 — SAS internal symmetric cable assembly - SAS SlimLine 4i to Mini SAS HD 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.8 SAS internal symmetric cable assembly - SAS SlimLine 4i to Mini SAS 4i

Figure 83 shows the SAS internal cable assembly with SAS Slimline 4i cable plug connector at one end and a Mini SAS 4i cable plug connector at the other end.

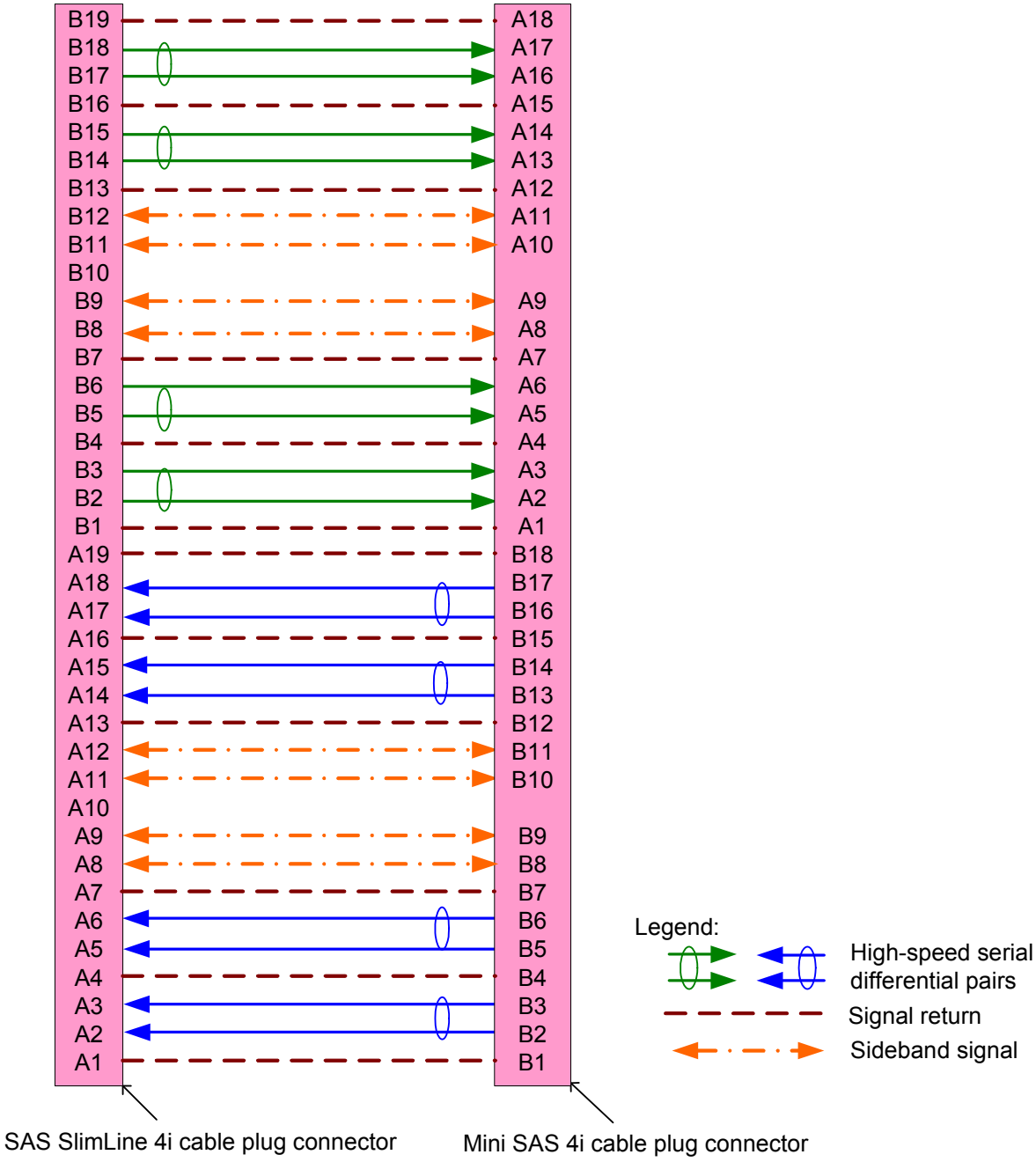


Figure 83 — SAS internal symmetric cable assembly - SAS SlimLine 4i to Mini SAS 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.9 SAS internal symmetric cable assembly - SAS SlimLine 8i

Figure 84 shows the SAS internal cable assembly with SAS Slimline 8i cable plug connectors at each end.

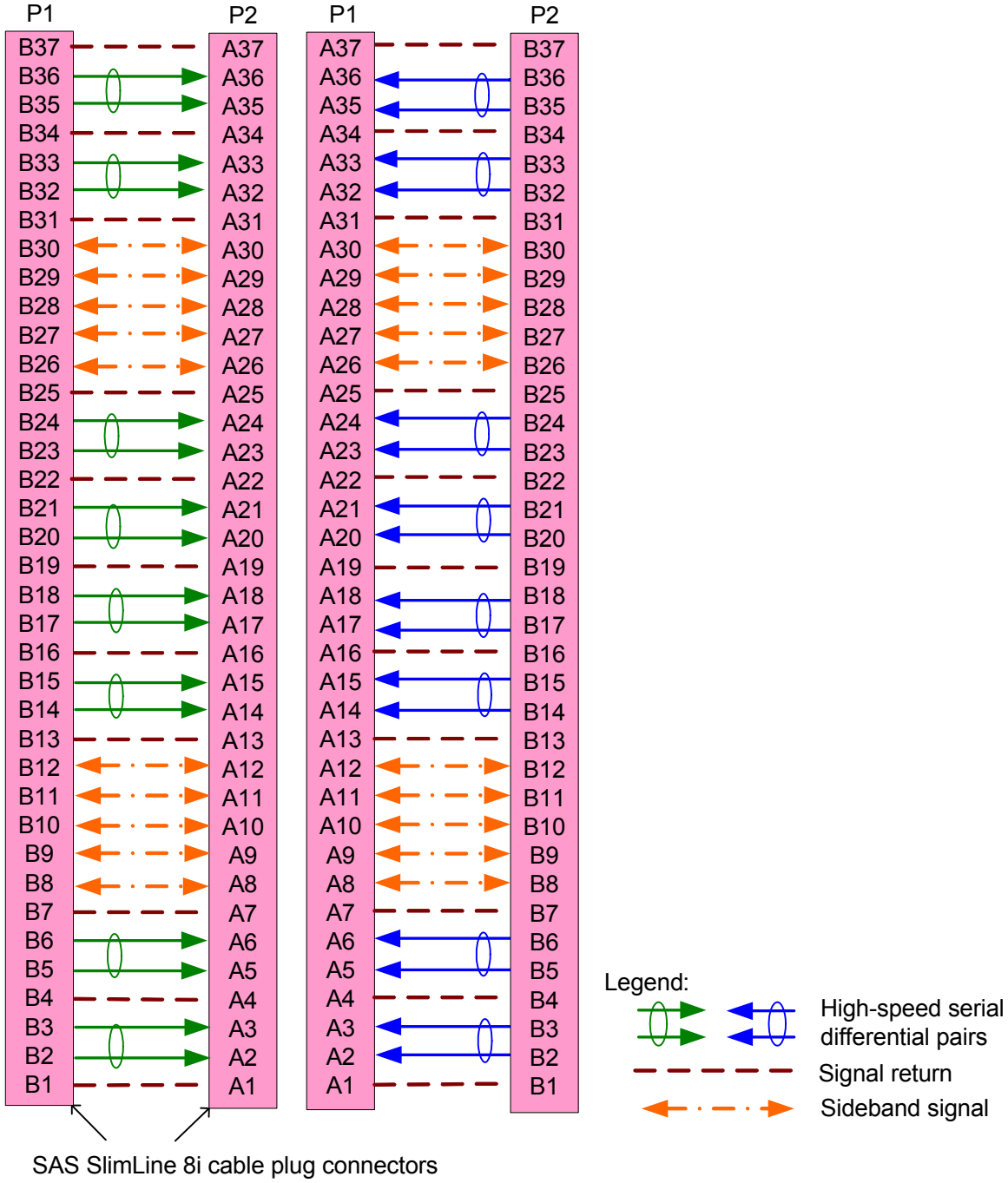


Figure 84 — SAS internal symmetric cable assembly - SAS SlimLine 8i

This cable assembly may support one to eight physical links.

5.4.4.1.2.10 SAS internal symmetric cable assembly - SAS SlimLine 8i to Mini SAS HD 8i

Figure 85 shows the SAS internal cable assembly with a SAS SlimLine 8i cable plug connector on one end and a Mini SAS HD 8i cable plug connector on the other end.

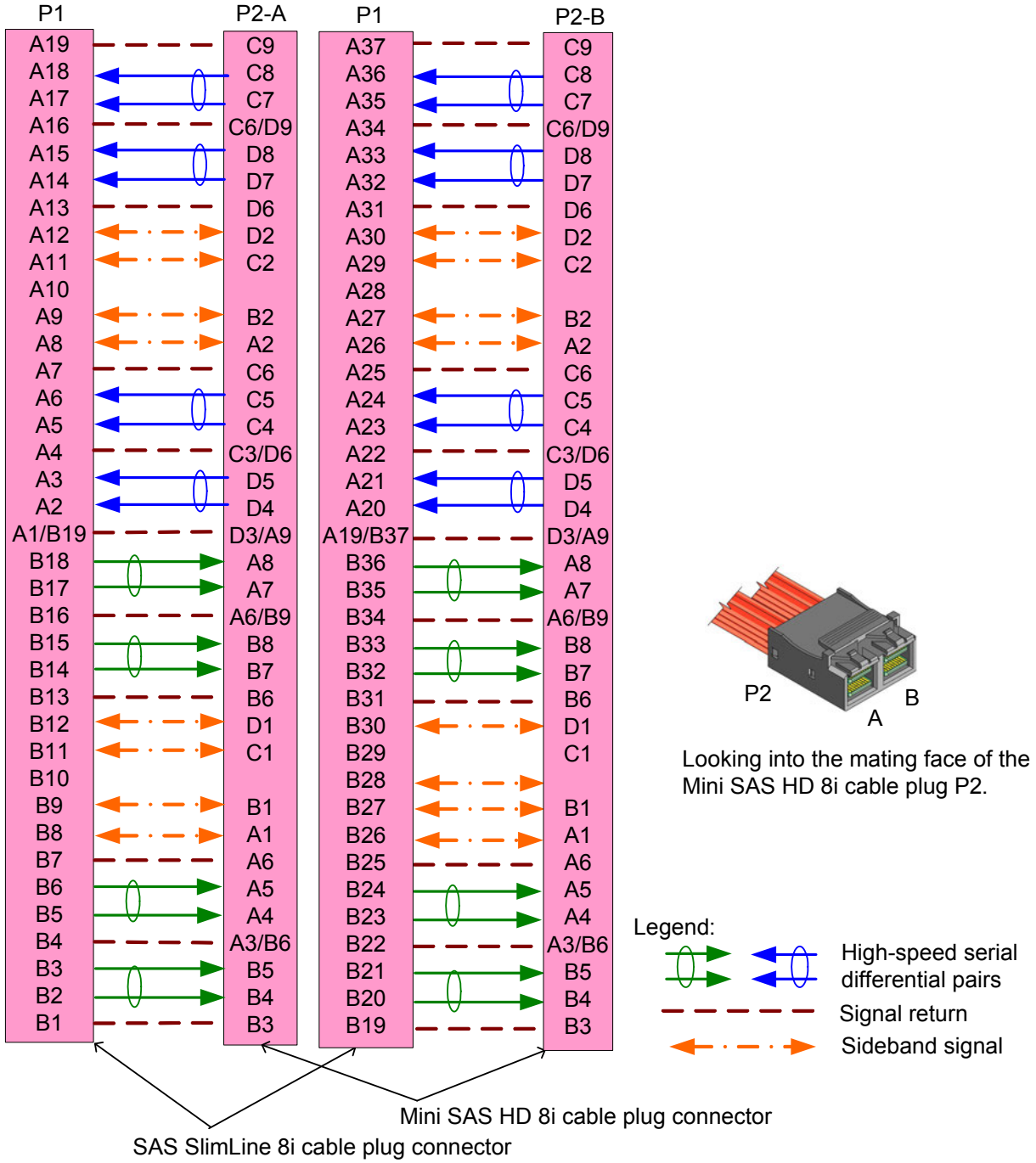


Figure 85 — SAS internal symmetric cable assembly - SAS SlimLine 8i to Mini SAS HD 8i

This cable assembly may support one to eight physical links.

5.4.4.1.2.11 SAS internal symmetric cable assembly - SAS MiniLink 4i

Figure 86 shows the SAS internal cable assembly with SAS MiniLink 4i cable plug connectors at each end.

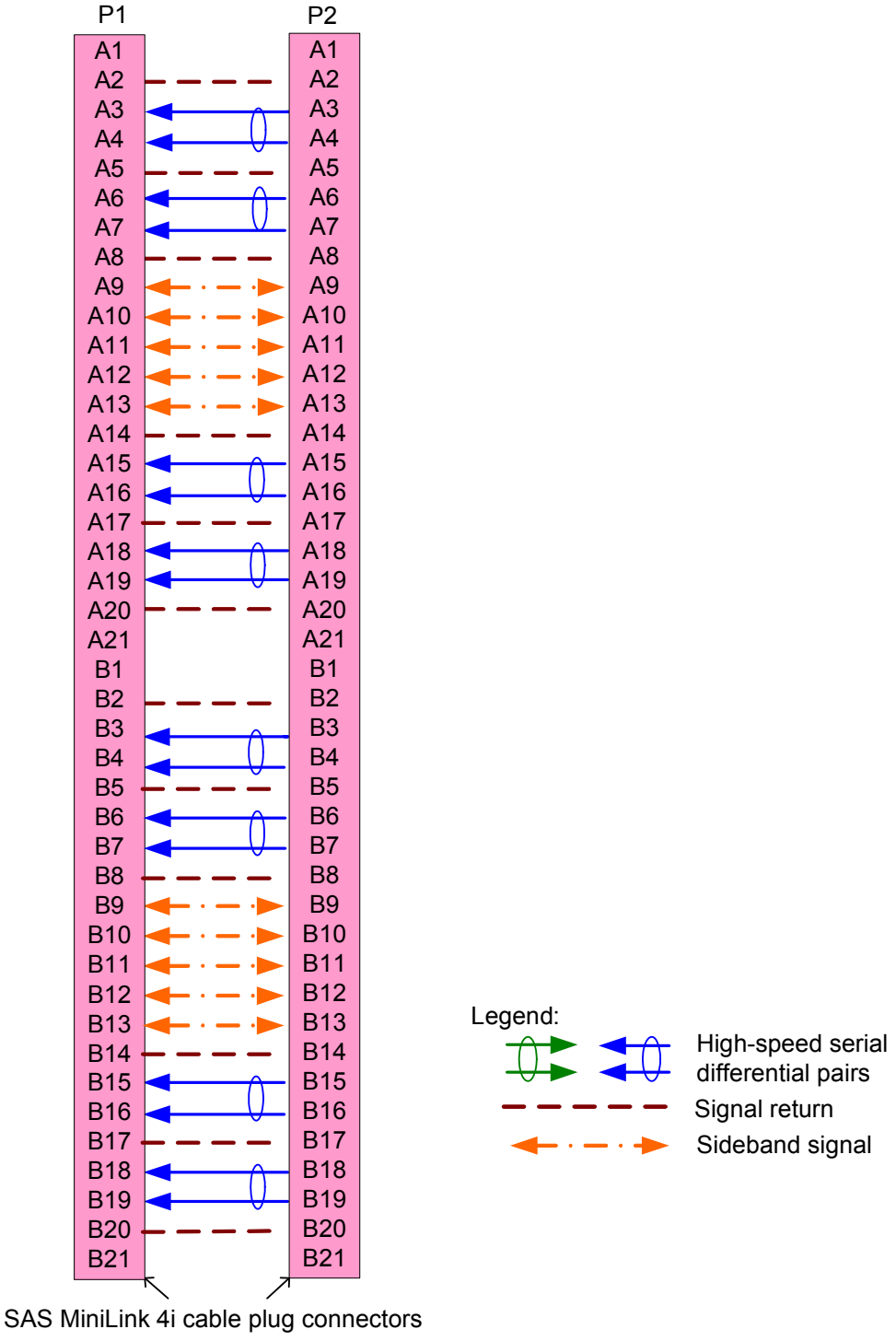


Figure 86 — SAS internal symmetric cable assembly - SAS MiniLink 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.12 SAS internal symmetric cable assembly - SAS MiniLink 4i to Mini SAS HD 4i

Figure 87 shows the SAS internal cable assembly with a SAS MiniLink 4i cable plug connector on one end and a Mini SAS HD 4i cable plug connector on the other end.

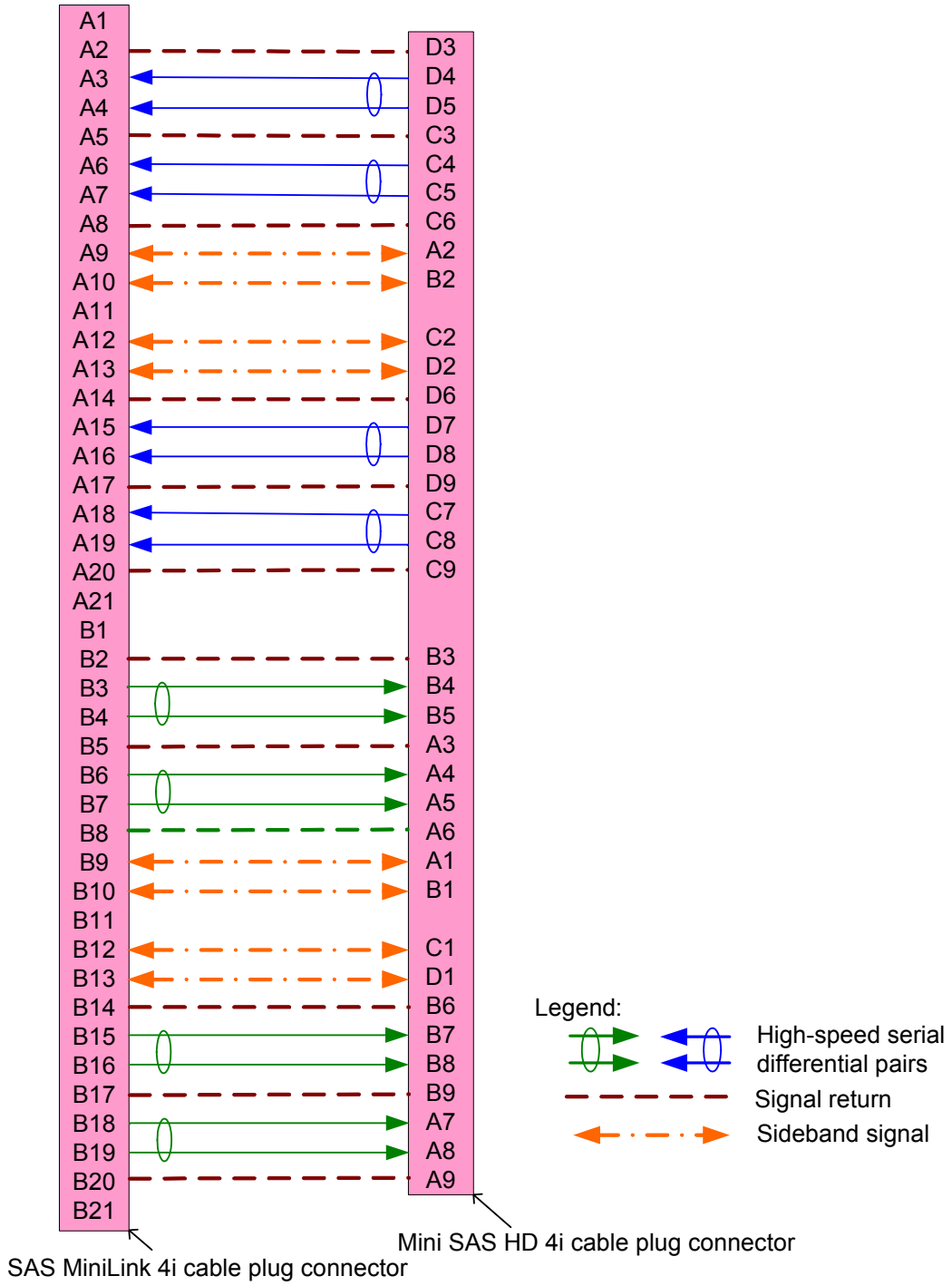


Figure 87 — SAS internal symmetric cable assembly - SAS MiniLink 4i to Mini SAS HD 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.13 SAS internal symmetric cable assembly - SAS MiniLink 4i to Mini SAS 4i

Figure 88 shows the SAS internal cable assembly with SAS MiniLink 4i cable plug connector at one end and a Mini SAS 4i cable plug connector at the other end.

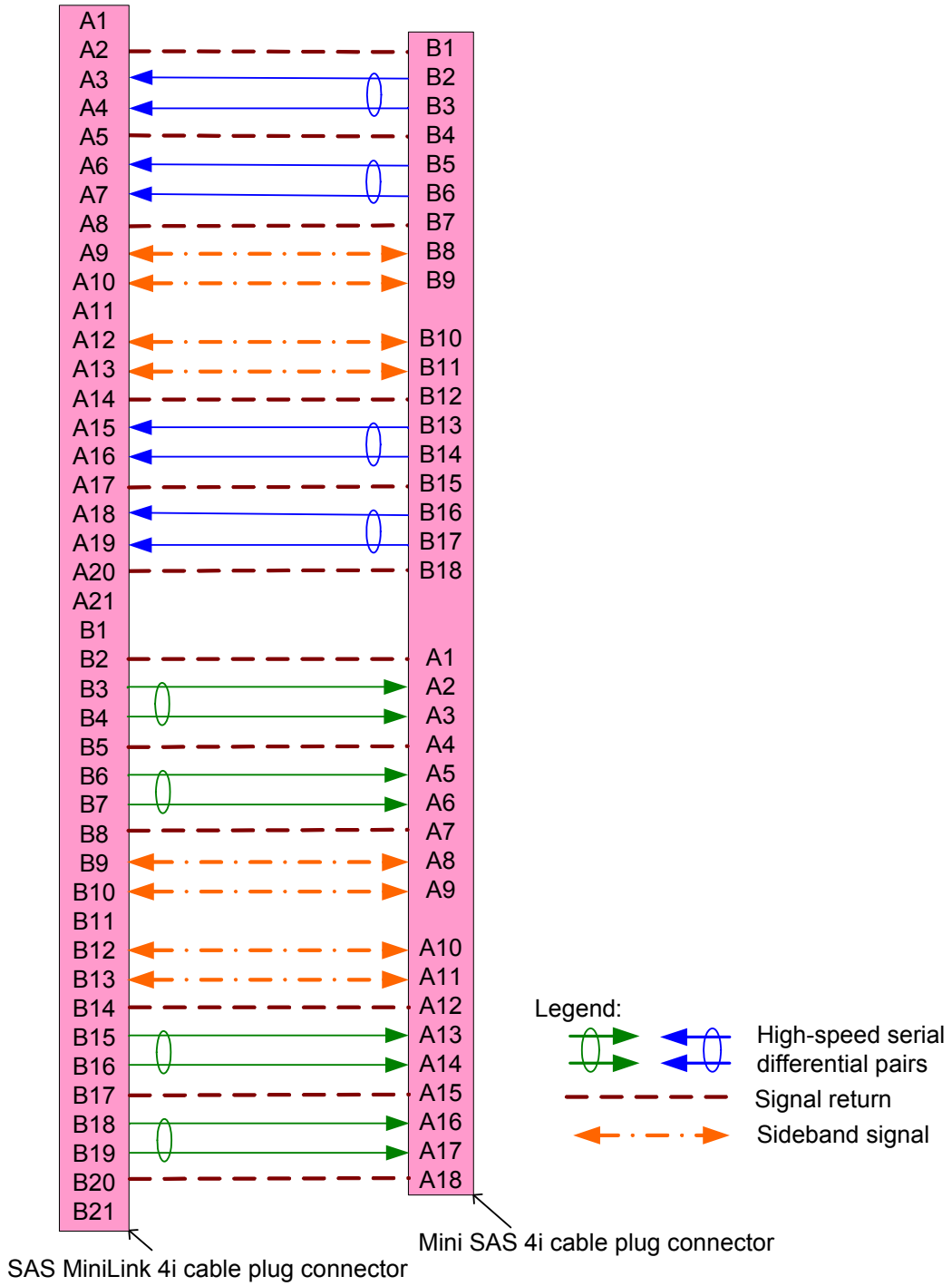


Figure 88 — SAS internal symmetric cable assembly - SAS MiniLink 4i to Mini SAS 4i

This cable assembly may support one to four physical links.

5.4.4.1.2.14 SAS internal symmetric cable assembly - SAS MiniLink 8i

Figure 89 shows the SAS internal cable assembly with SAS MiniLink 8i cable plug connectors at each end.

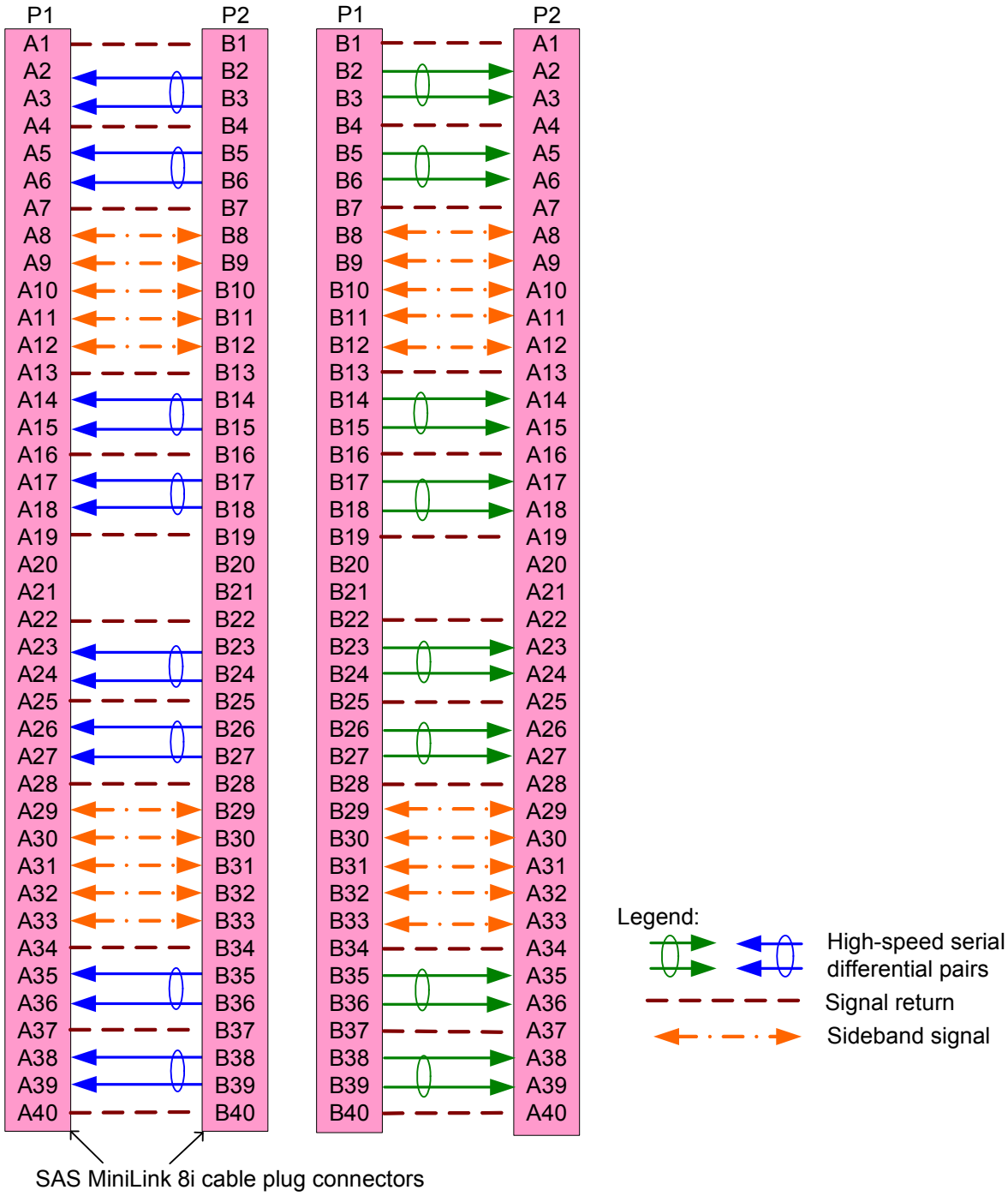


Figure 89 — SAS internal symmetric cable assembly - SAS MiniLink 8i

This cable assembly may support one to eight physical links.

5.4.4.1.2.15 SAS internal symmetric cable assembly - SAS MiniLink 8i to Mini SAS HD 8i

Figure 90 shows the SAS internal cable assembly with a SAS MiniLink 8i cable plug connector on one end and a Mini SAS HD 8i cable plug connector on the other end.

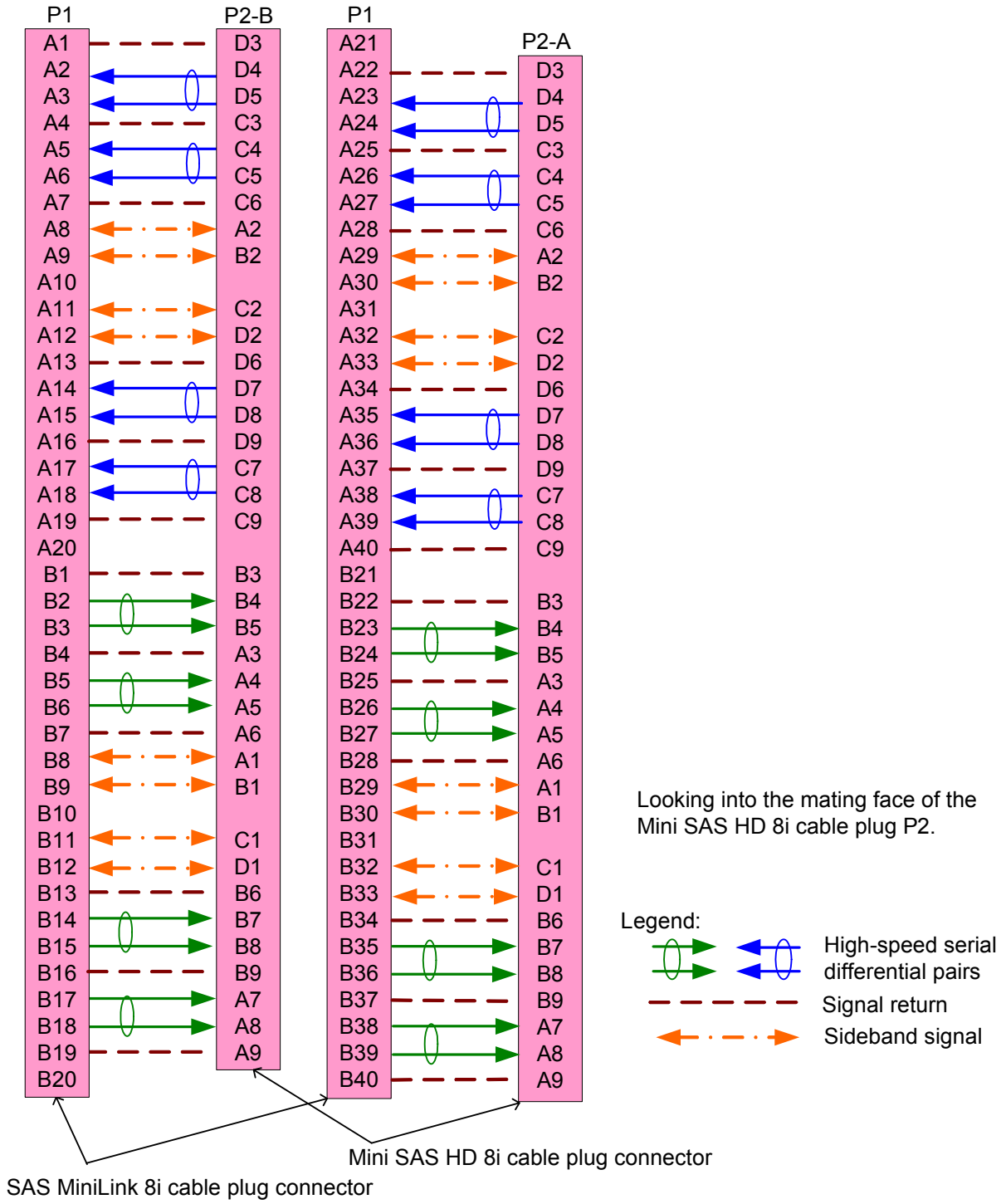


Figure 90 — SAS internal symmetric cable assembly - SAS MiniLink 8i to Mini SAS HD 8i

This cable assembly may support one to eight physical links.

5.4.4.1.3 SAS internal fanout cable assemblies

5.4.4.1.3.1 SAS internal fanout cable assemblies overview

A SAS internal fanout cable assembly is either:

a) a SAS internal controller-based fanout cable assembly with:
   A) a Mini SAS 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end (see 5.4.4.1.3.2);
   B) a Mini SAS HD 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end (see 5.4.4.1.3.3);
   C) a SAS SlimLine 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end (see 5.4.4.1.3.4);
   D) a SAS SlimLine 4i cable plug connector.on one end and four SATA signal cable receptacle connectors on the other end (see 5.4.4.1.3.5);
   E) a SAS SlimLine 8i cable plug connector (see 5.4.3.3.4.2) on one end and two SAS SlimLine 4i cable plug connectors (see 5.4.3.3.4.1) on the other end (see 5.4.4.1.3.6);
   F) a SAS SlimLine 8i cable plug connector (see 5.4.3.3.4.2) on one end and two Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1) on the other end (see 5.4.4.1.3.7);
   G) a SAS MiniLink 4i cable plug connector on one end and four SATA signal cable receptacle connectors on the other end (see 5.4.4.1.3.8);
   H) a SAS MiniLink 8i cable plug connector (see 5.4.3.3.4.2) on one end and two SAS MiniLink 4i cable plug connectors (see 5.4.3.3.4.1) on the other end (see 5.4.4.1.3.9);
   I) a SAS MiniLink 8i cable plug connector (see 5.4.3.3.4.2) on one end and two Mini SAS HD 4i cable plug connectors (see 5.4.3.3.3.1) on the other end (see 5.4.4.1.3.10); or
   J) a SAS MiniLink 8i cable plug connector (see 5.4.3.3.4.2) on one end and two Mini SAS 4i cable plug connectors (see 5.4.3.3.2.1) on the other end (see 5.4.4.1.3.11);

   or

b) a SAS internal backplane-based fanout cable assembly with:
   A) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS 4i cable plug connector on the other end (i.e., the backplane end) (see 5.4.4.1.3.12); or
   B) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS HD 4i cable plug connector on the other end (i.e., the backplane end) (see 5.4.4.1.3.13).

In a SAS internal fanout symmetric cable assembly, the TX signals on one end shall be connected to RX signals on the other end (e.g., a TX+ of one connector shall connect to an RX+ of the other connector).

Each signal return on one end of the cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in the cable assembly.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND 0 of the controller is attached to SIDEBAND 0 of the backplane). The SIDEBAND 8 and SIDEBAND 9 signals are not supported on the Mini SAS 4i cable plug connector (see 5.4.3.3.2.1), the Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1), or the Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2). No sidebands are supported on the SAS Drive cable receptacle connector or the SATA signal cable receptacle connector.

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND 0 of one controller is attached to SIDEBAND 7 of the other controller). The SIDEBAND 8 signal and SIDEBAND 9 signal are not supported on the Mini SAS 4i cable plug connector (see 5.4.3.3.2.1), the Mini SAS HD 4i cable plug connector (see 5.4.3.3.3.1), or the Mini SAS HD 8i cable plug connector (see 5.4.3.3.3.2). No sidebands are supported on the SAS Drive cable receptacle connector or the SATA signal cable receptacle connector.

5.4.4.1.3.2 SAS internal controller-based fanout cable assembly - Mini SAS 4i to SAS Drive

Figure 91 shows the SAS internal controller-based fanout cable assembly with a Mini SAS 4i cable plug connector at the controller end and four SAS Drive cable receptacle connectors on the other end.

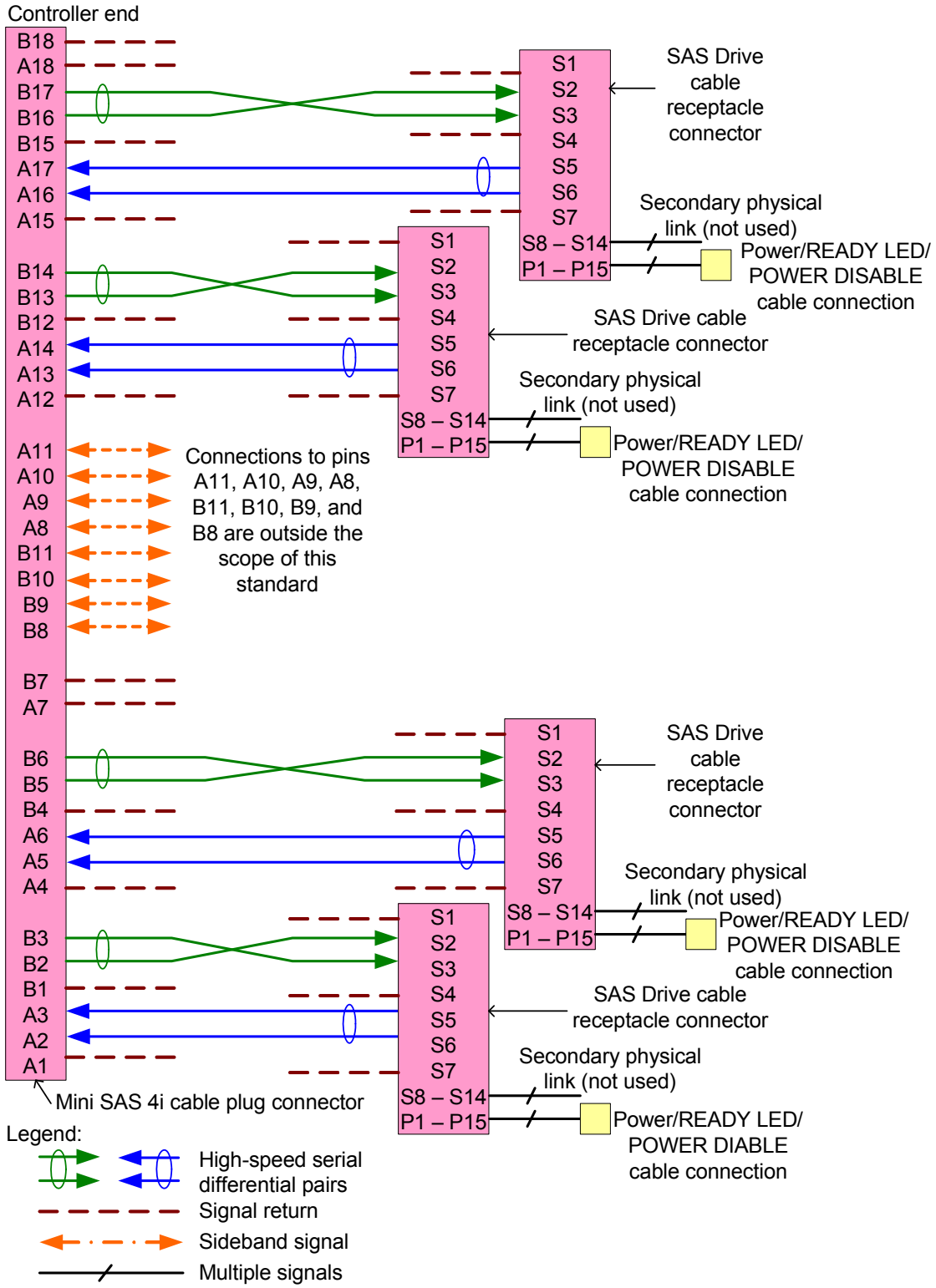


Figure 91 — SAS internal controller-based fanout cable assembly - Mini SAS 4i to SAS Drive

5.4.4.1.3.3 SAS internal controller-based fanout cable assembly - Mini SAS HD 4i to SAS Drive

Figure 92 shows the SAS internal controller-based fanout cable assembly with a Mini SAS HD 4i cable plug connector at the controller end and four SAS Drive cable receptacle connectors on the other end.

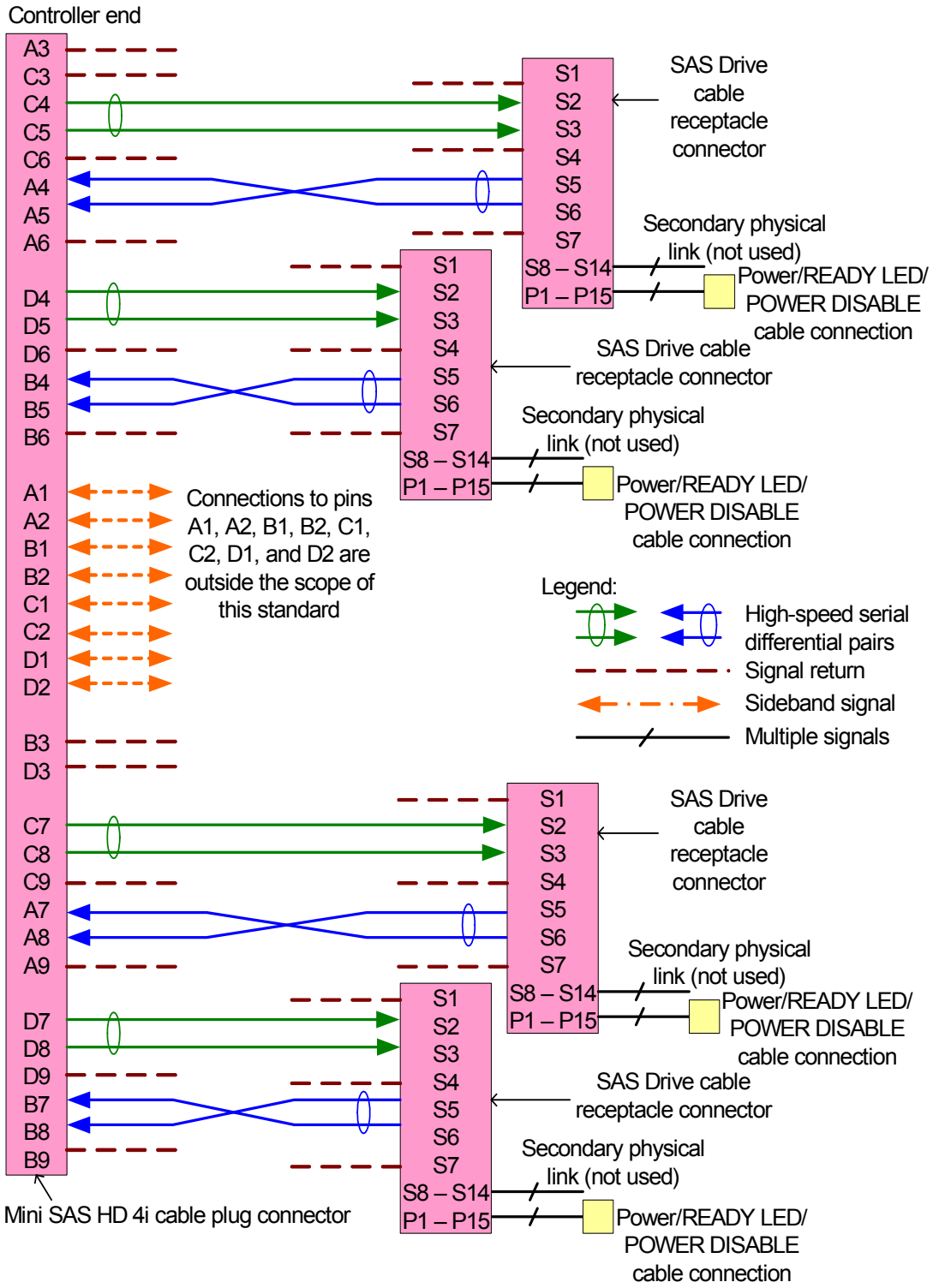


Figure 92 — SAS internal controller-based fanout cable assembly - Mini SAS HD 4i to SAS Drive

5.4.4.1.3.4 SAS internal controller-based fanout cable assembly - SAS SlimLine 4i to SAS Drive

Figure 93 shows the SAS internal controller-based fanout cable assembly with a SAS SlimLine 4i cable plug connector at the controller end and four SAS Drive cable receptacle connectors on the other end.

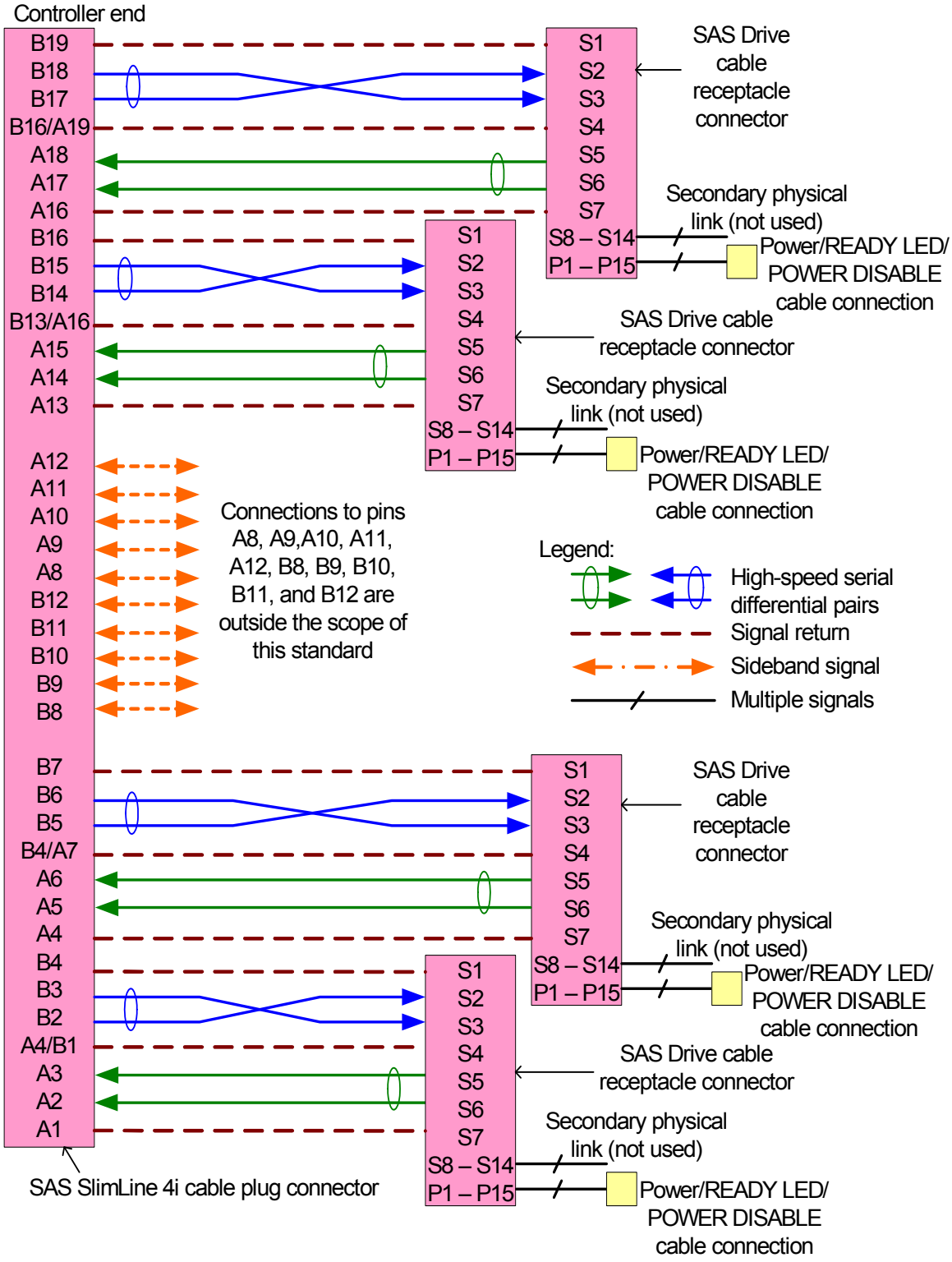


Figure 93 — SAS internal controller-based fanout cable assembly - SAS SlimLine 4i to SAS Drive

5.4.4.1.3.5 SAS internal controller-based fanout cable assembly - SAS SlimLine 4i to SATA signal

Figure 94 shows the SAS internal controller-based fanout cable assembly with the SAS SlimLine 4i cable plug connector at the controller end and four SATA signal cable receptacle connectors on the other end.

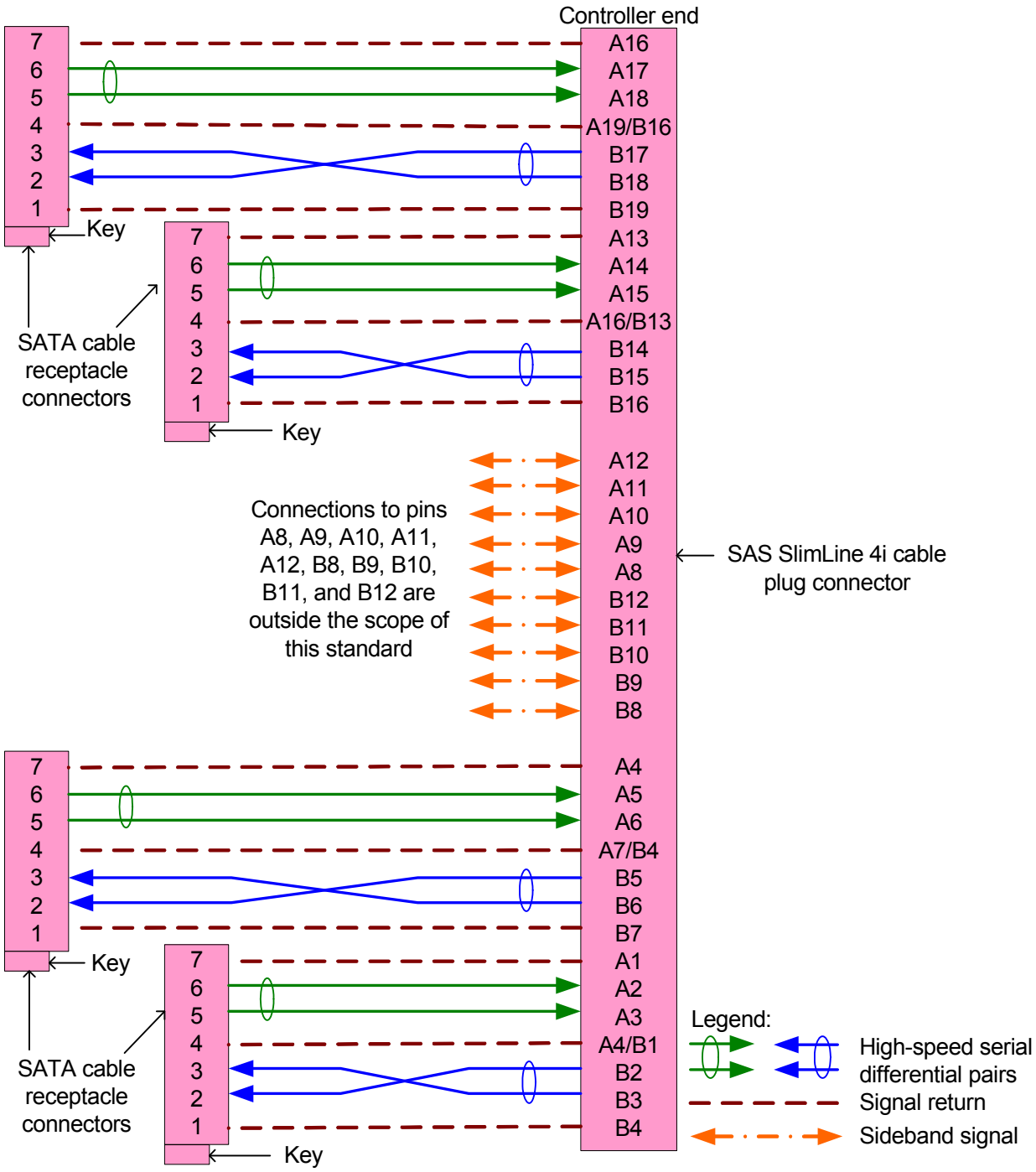


Figure 94 — SAS internal controller-based fanout cable assembly - SAS SlimLine 4i to SATA signal

5.4.4.1.3.6 SAS internal controller-based fanout cable assembly - SAS SlimLine 8i to SAS SlimLine 4i

Figure 95 shows the SAS internal controller-based fanout cable assembly with a SAS SlimLine 8i cable plug connector on one end and two SAS SlimLine 4i cable plug connectors on the other end.

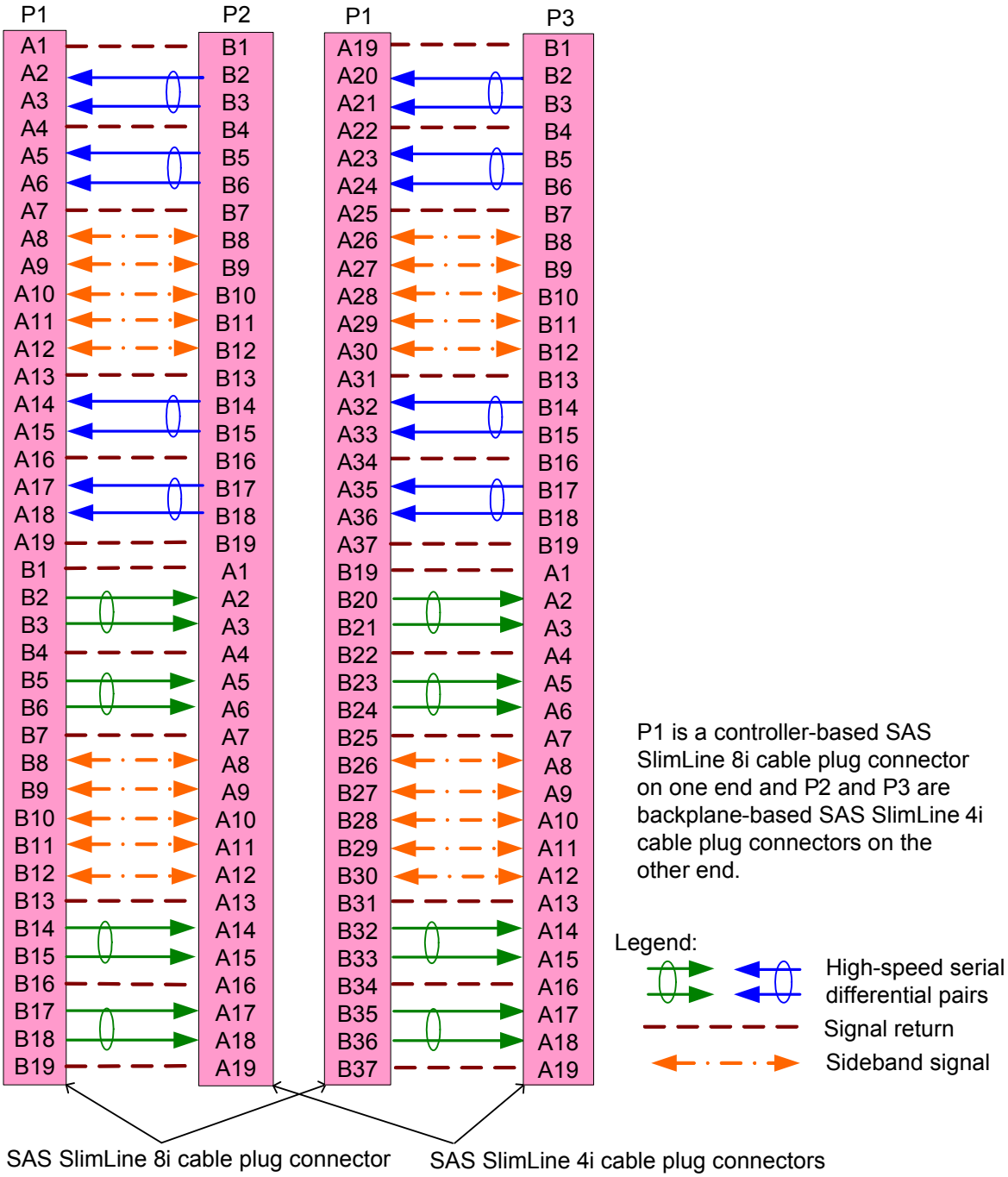


Figure 95 — SAS internal controller-based fanout cable assembly - SAS SlimLine 8i to SAS SlimLine 4i

5.4.4.1.3.7 SAS internal controller-based fanout cable assembly - SAS SlimLine 8i to Mini SAS HD 4i

Figure 96 shows the SAS internal controller-based fanout cable assembly with a SAS SlimLine 8i cable plug connector on one end and two Mini SAS HD 4i cable plug connectors on the other end.

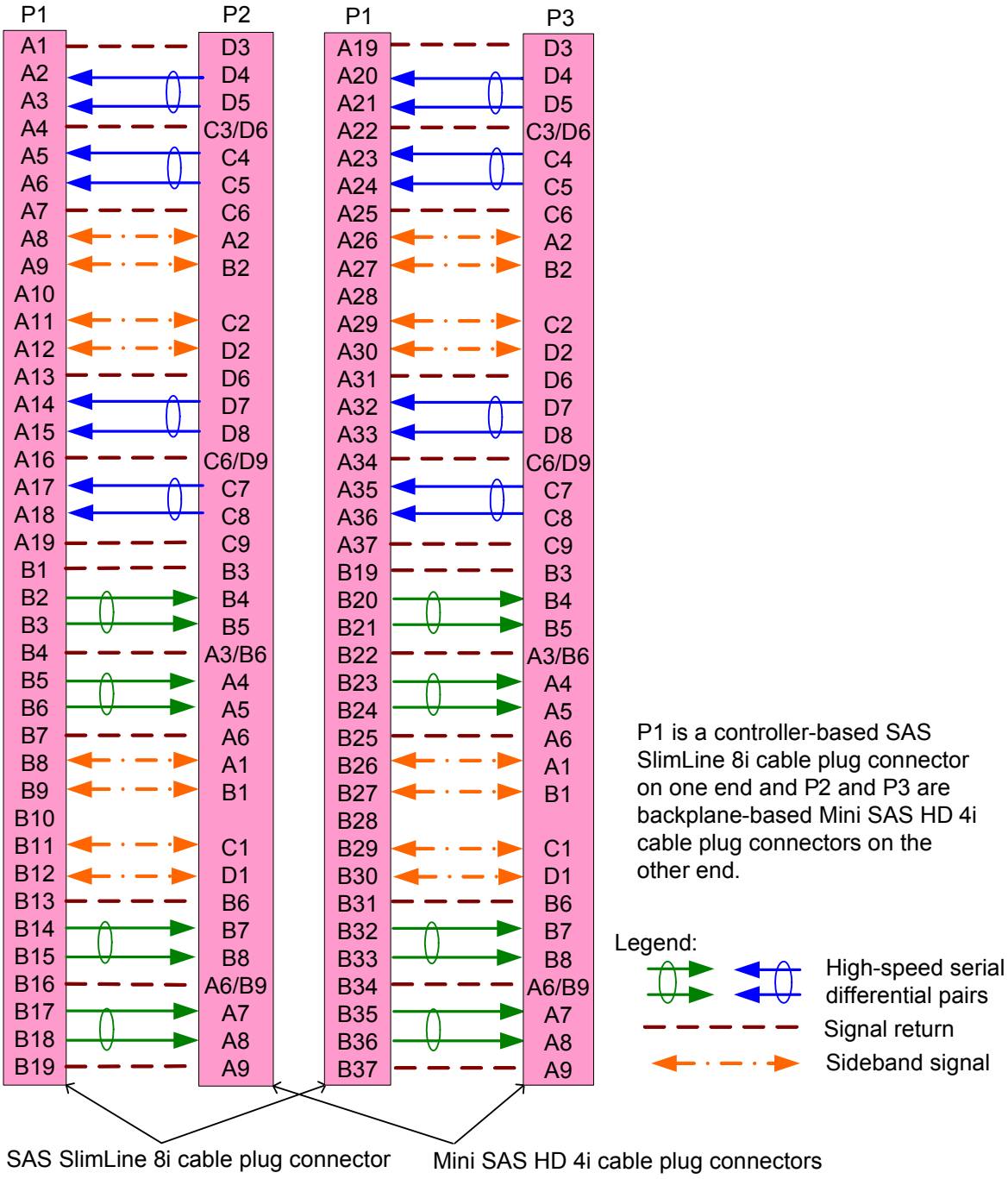


Figure 96 — SAS internal controller-based fanout cable assembly - SAS SlimLine 8i to Mini SAS HD 4i

5.4.4.1.3.8 SAS internal controller-based fanout cable assembly - SAS MiniLink 4i to SATA signal

Figure 97 shows the SAS internal controller-based fanout cable assembly with the SAS MiniLink 4i cable plug connector at the controller end and four SATA signal cable receptacle connectors on the other end.

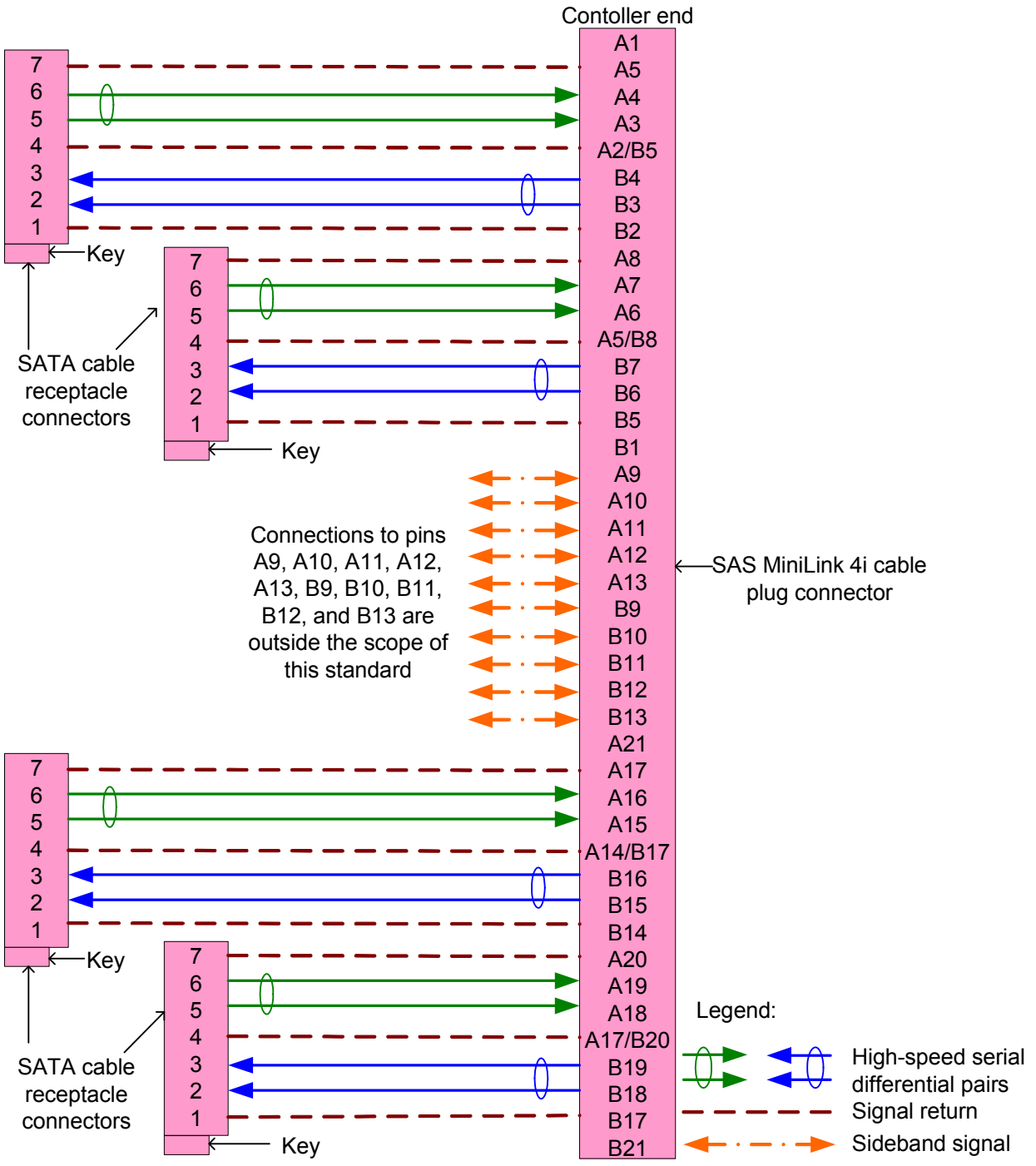


Figure 97 — SAS internal controller-based fanout cable assembly - SAS MiniLink 4i to SATA signal

5.4.4.1.3.9 SAS internal controller-based fanout cable assembly - SAS MiniLink 8i to SAS MiniLink 4i

Figure 98 shows the SAS internal controller-based fanout cable assembly with a SAS MiniLink 8i cable plug connector on one end and two SAS MiniLink 4i cable plug connectors on the other end.

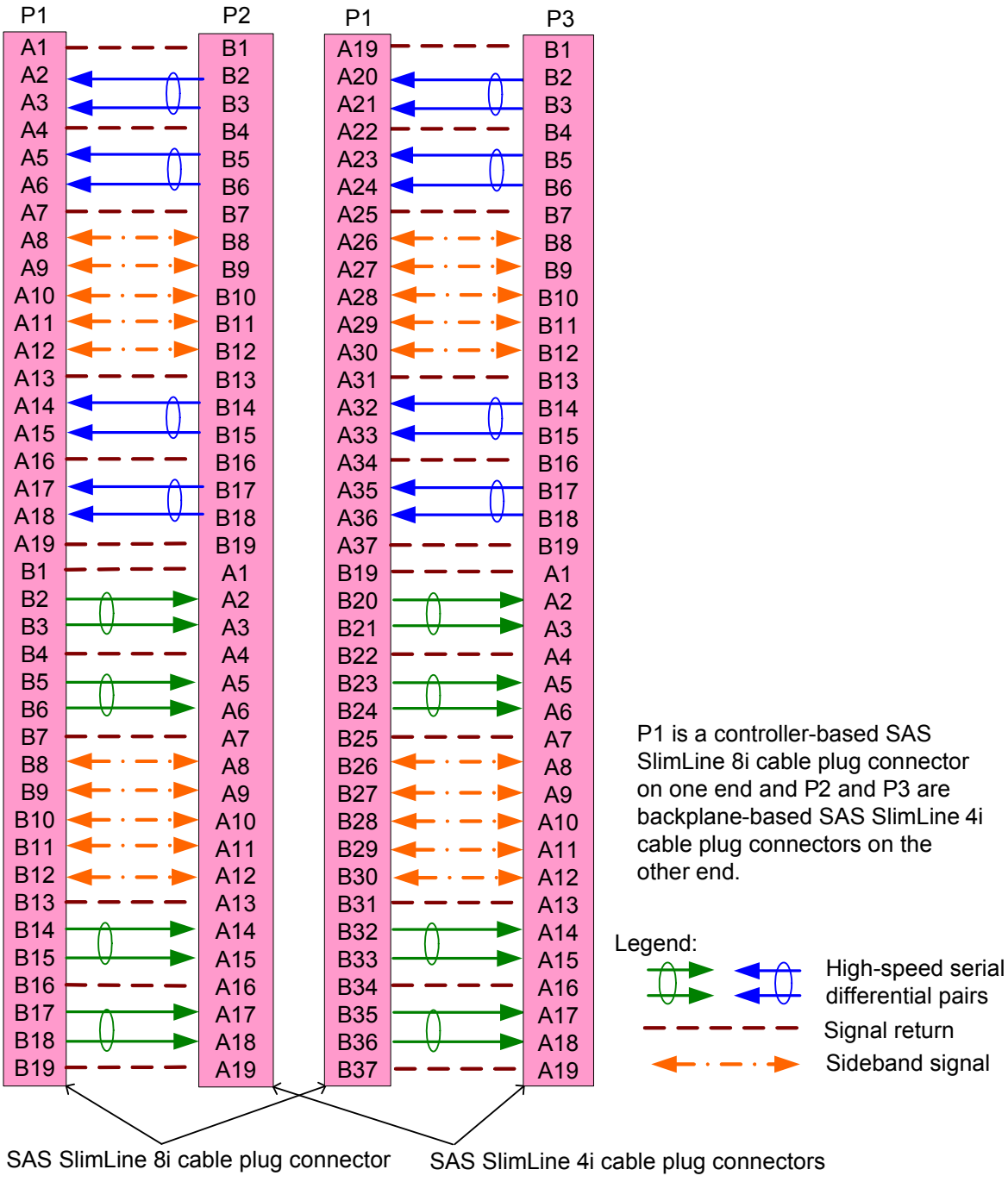


Figure 98 — SAS internal controller-based fanout cable assembly - SAS MiniLink 8i to SAS MiniLink 4i

5.4.4.1.3.10 SAS internal controller-based fanout cable assembly - SAS MiniLink 8i to Mini SAS HD 4i

Figure 99 shows the SAS internal controller-based fanout cable assembly with a SAS MiniLink 8i cable plug connector on one end and two Mini SAS HD 4i cable plug connectors on the other end.

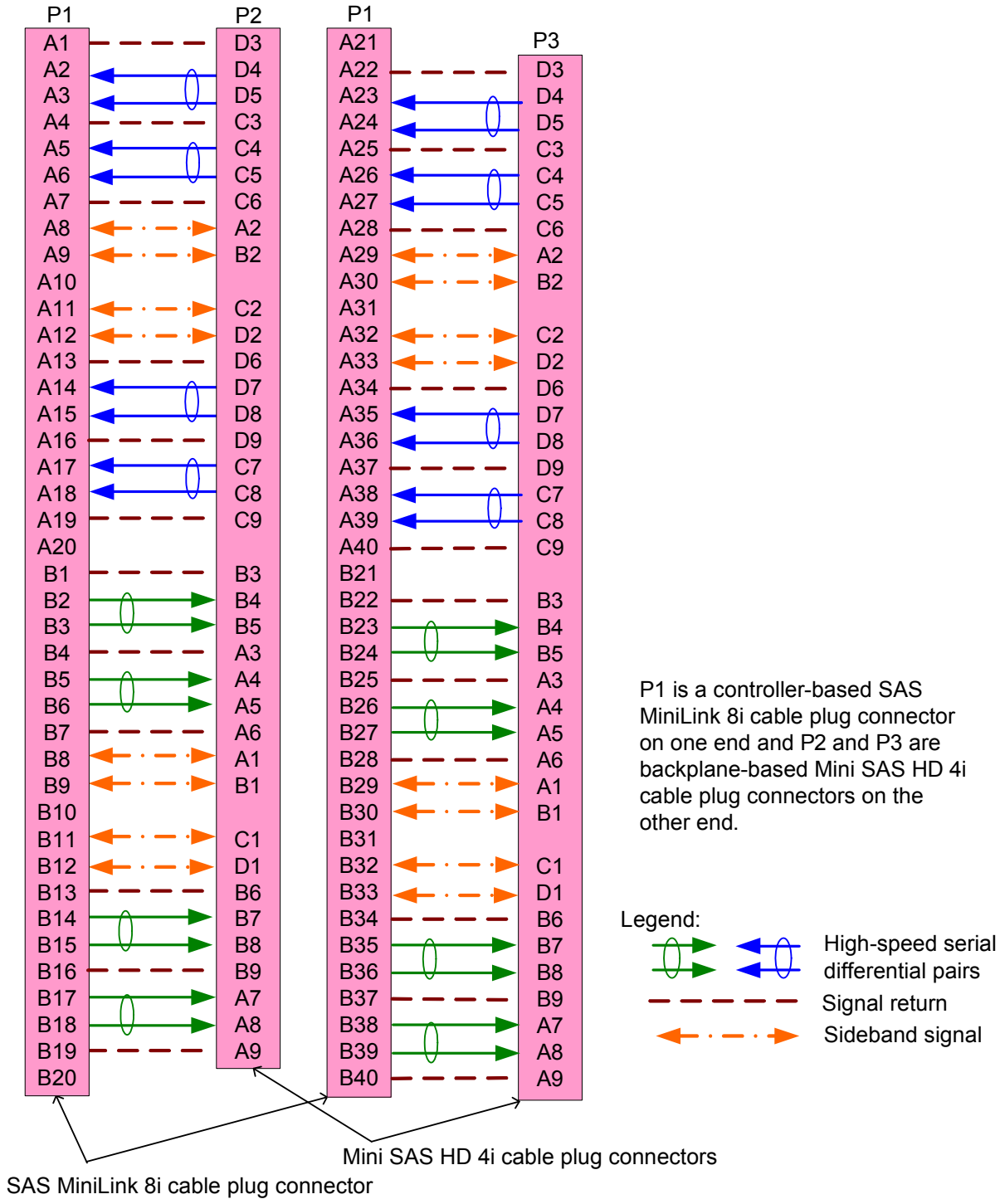


Figure 99 — SAS internal backplane-based fanout cable assembly - SAS MiniLink 8i to Mini SAS HD 4i

5.4.4.1.3.11 SAS internal controller-based fanout cable assembly - SAS MiniLink 8i to Mini SAS 4i

Figure 100 shows the SAS internal controller-based fanout cable assembly with a SAS MiniLink 8i cable plug connector on one end and two Mini SAS 4i cable plug connectors on the other end.

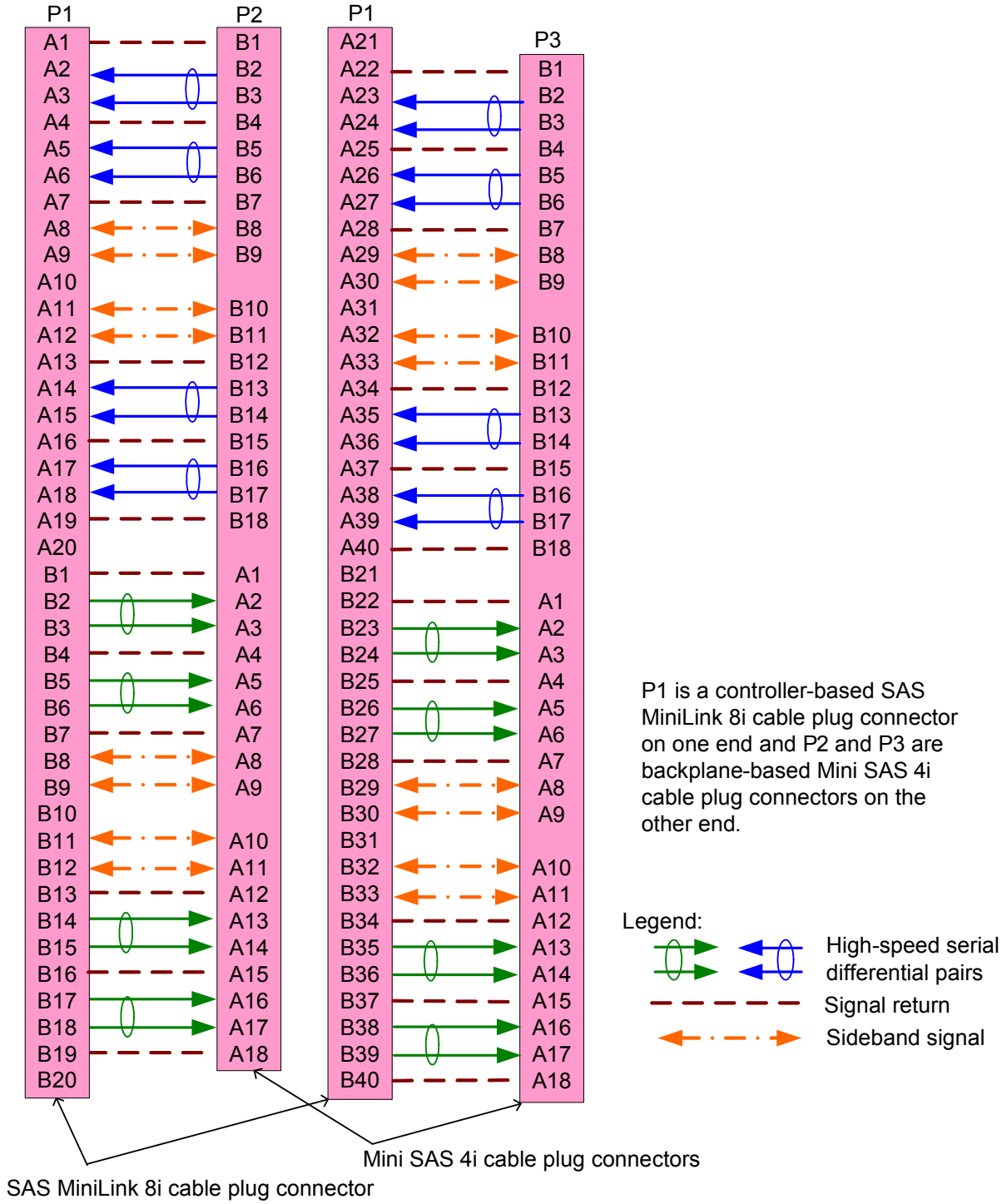


Figure 100 — SAS internal controller-based fanout cable assembly - SAS MiniLink 8i to Mini SAS 4i

5.4.4.1.3.12 SAS internal backplane-based fanout cable assembly - SATA signal to Mini SAS 4i

Figure 101 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS 4i cable plug connector.

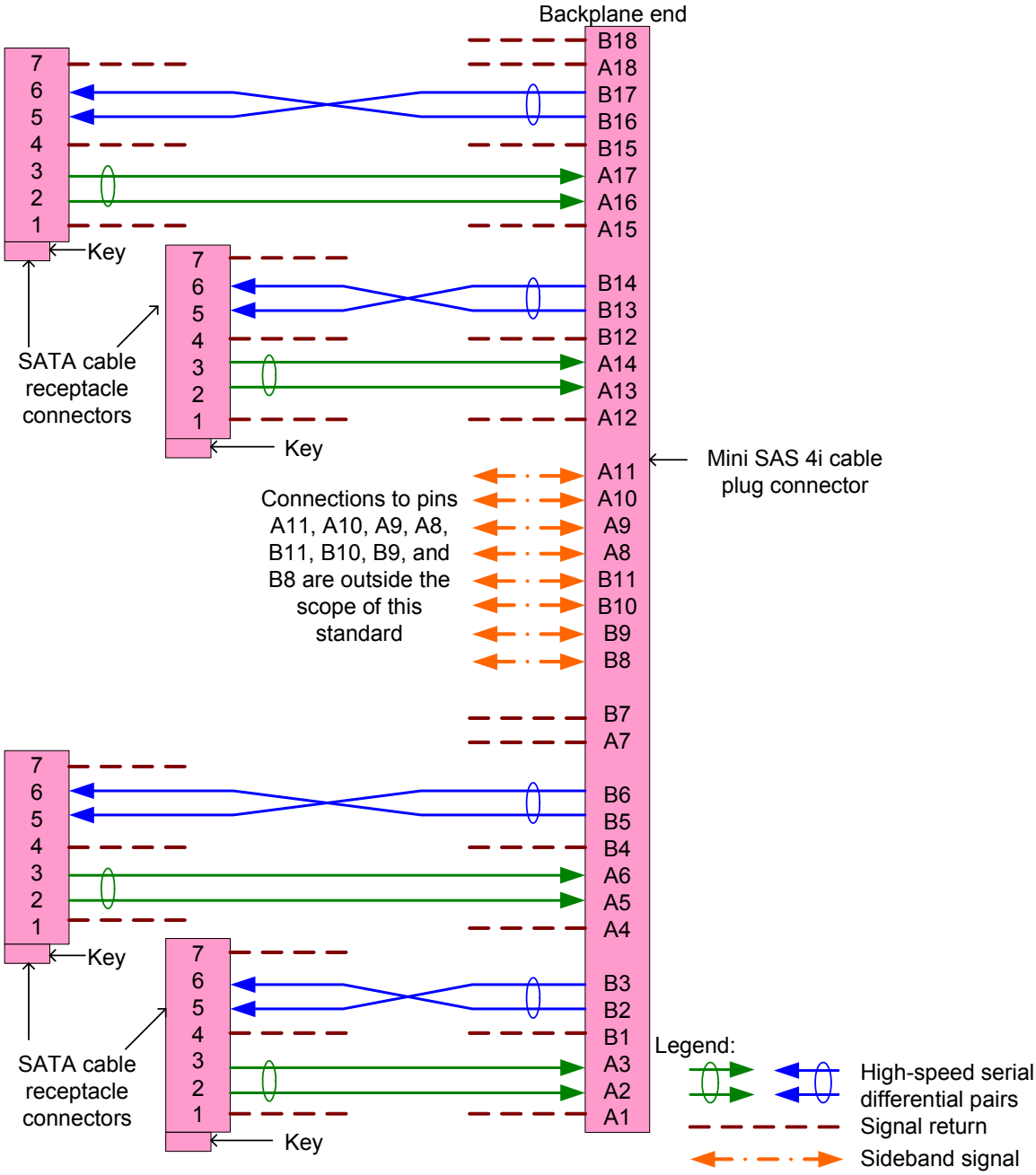


Figure 101 — SAS internal backplane-based fanout cable assembly - SATA signal to Mini SAS 4i

5.4.4.1.3.13 SAS internal backplane-based fanout cable assembly - SATA signal to Mini SAS HD 4i

Figure 102 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS HD 4i cable plug connector.

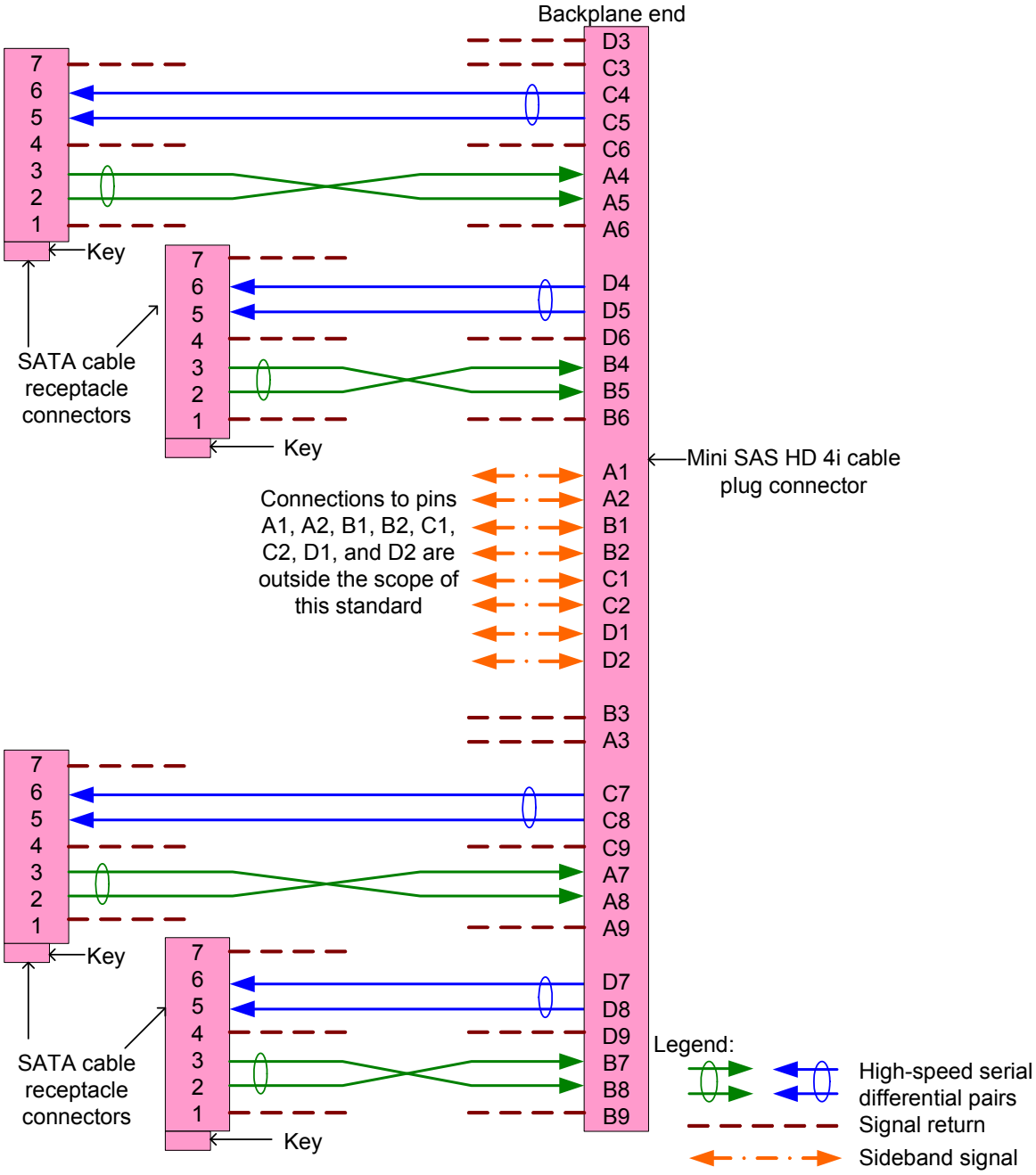


Figure 102 — SAS internal backplane-based fanout cable assembly - SATA signal to Mini SAS HD 4i

5.4.4.2 SAS external cable assemblies

5.4.4.2.1 SAS external cable assemblies overview

A SAS external cable assembly has:

a) a Mini SAS 4x cable plug connector (see 5.4.3.4.1.1) at each end (see 5.4.4.2.2);
b) a Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1) at each end (see 5.4.4.2.3);
c) a Mini SAS HD 8x cable plug connector (see 5.4.3.4.2.2) at each end (see 5.4.4.2.4);
d) a Mini SAS HD 8x cable plug connector (see 5.4.3.4.2.2) at one end and two Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1) at the other end (see 5.4.4.2.5);
e) a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end (see 5.4.4.2.6); or
f) a QSFP+ cable plug connector (see 5.4.3.4.3.1) at each end (see 5.4.4.2.7).

SAS external cable assemblies do not include power, the READY LED signal, or the POWER DISABLE signal.

Although the connector always supports four or eight physical links, a SAS external cable assembly may support one to eight physical links. SAS external cable assemblies should be labeled to indicate how many physical links are included (i.e., 1X, 2X, 3X, 4X, 5X, 6X, 7X, or 8X on each connector's housing).

The TX signals on one end shall be connected to the corresponding RX signals of the other end (e.g., TX0+ of one connector shall be connected to RX0+ of the other connector).

Signal returns shall not be connected to CHASSIS GROUND in the cable assembly.

In addition to the SAS icon (see Annex K), additional icons are defined for external connectors to guide users into making compatible attachments (i.e., not attaching expander device table routing phys to expander device table routing phys in externally configurable expander devices (see SPL-4), which is not allowed (see SPL-4)). Connectors that have one or more matching icons are intended to be attached together. Connectors that do not have a matching icon should not be attached together.

One end of the SAS external cable assembly shall support being attached to an end device, an enclosure out port, or an enclosure universal port. The other end of the SAS external cable assembly shall support being attached to an end device, an enclosure in port, or an enclosure universal port. If a Mini SAS 4x cable plug connector is used, then it shall include icons and key slots as defined in 5.4.3.4.1.1.

5.4.4.2.2 SAS external cable assembly - Mini SAS 4x

Figure 103 shows the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. This cable assembly should not be used for rates greater than 6 Gbit/s.

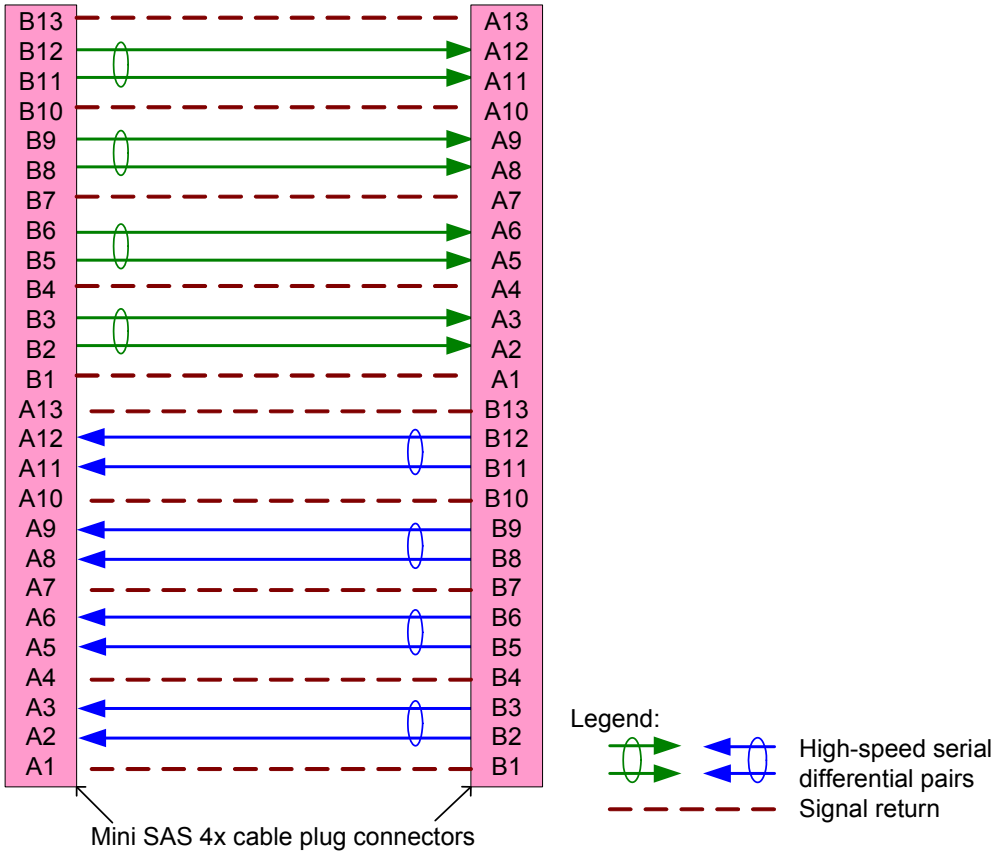


Figure 103 — Mini SAS 4x external cable assembly

In addition to the signal return connections shown in figure 103, one or more of the signal returns may be connected together in this cable assembly.

Figure 104 shows the SAS external cable assembly with Mini SAS 4x active cable assembly plug connectors at each end.

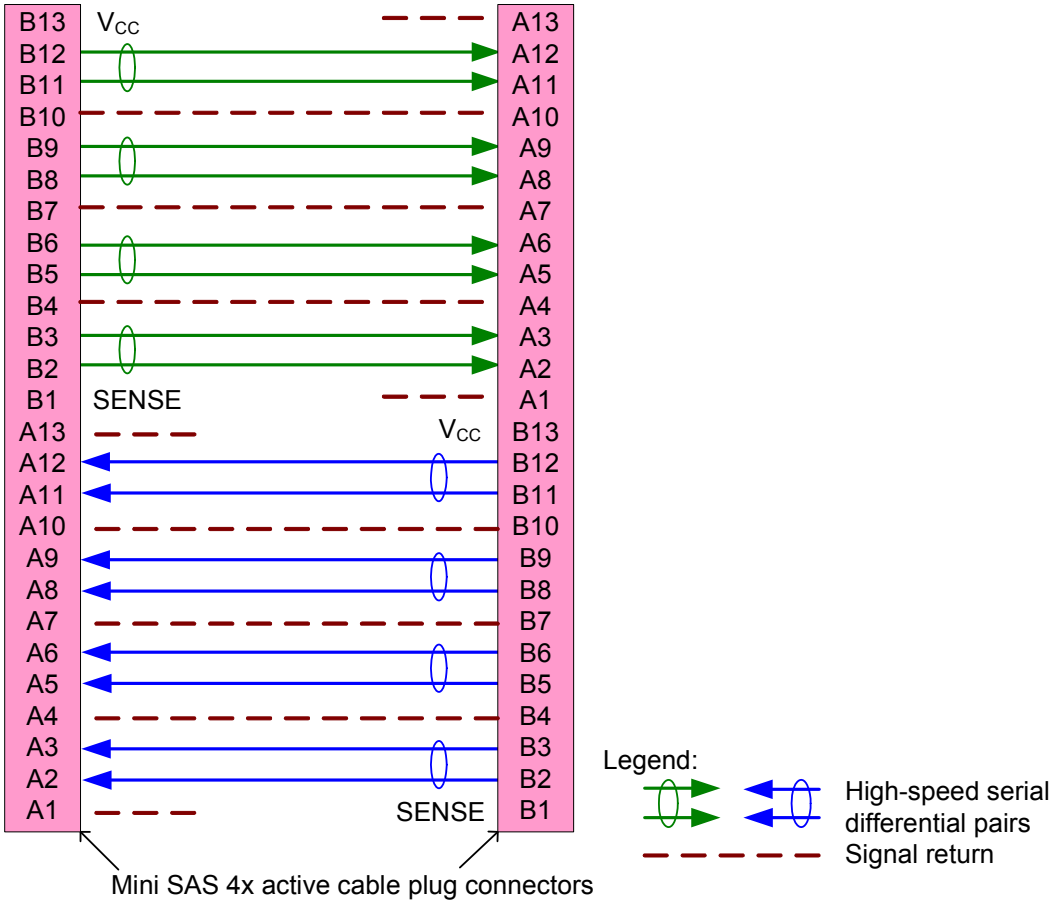


Figure 104 — Mini SAS 4x active external cable assembly

In addition to the signal return connections shown in figure 104, one or more of the signal returns may be connected together in this cable assembly.

Figure 105 shows an example cable with icons and key slots in the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. Depending on the cable configuration, the Mini SAS 4x cable connectors may also include different icon, key slot, and key combinations than shown in figure 105 (see 5.4.3.4.1.1).

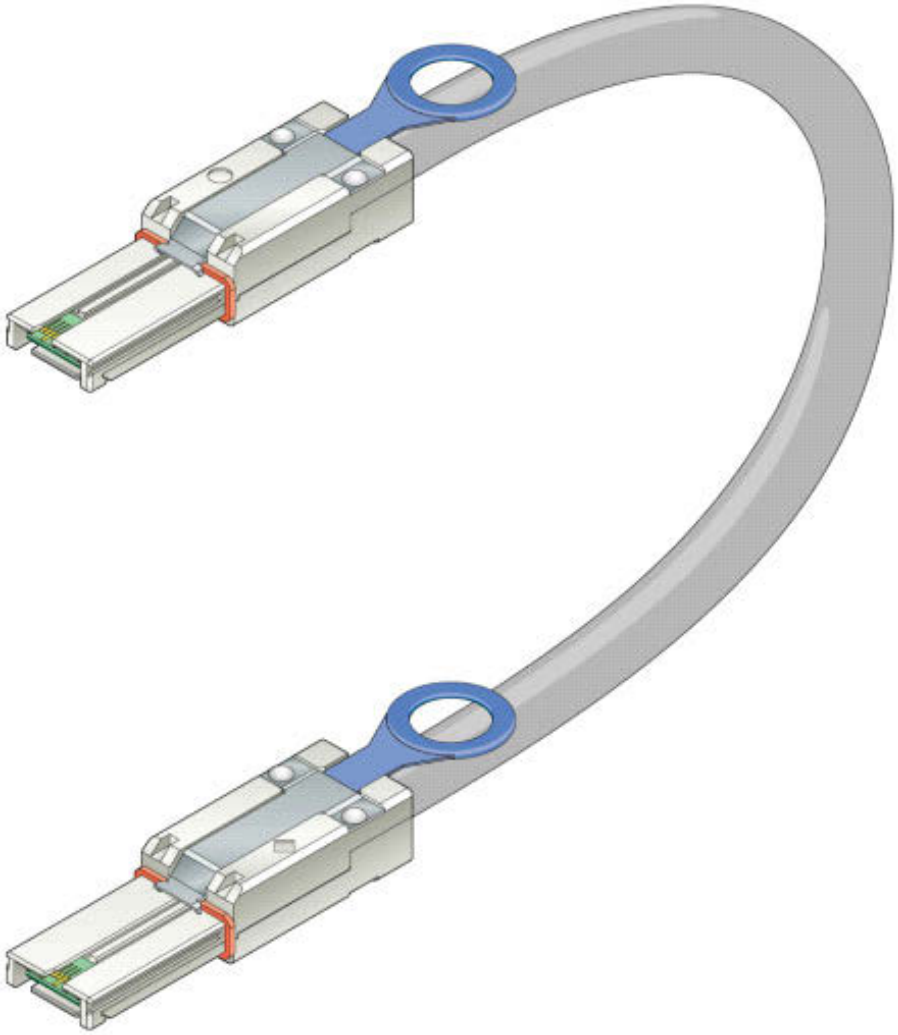


Figure 105 — SAS external cable assembly with Mini SAS 4x cable plug connectors

Although the topology is supported by this standard and SPL-4, a SAS external cable assembly with Mini SAS 4x cable plug connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL-4.

5.4.4.2.3 SAS external cable assembly - Mini SAS HD 4x

Figure 106 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

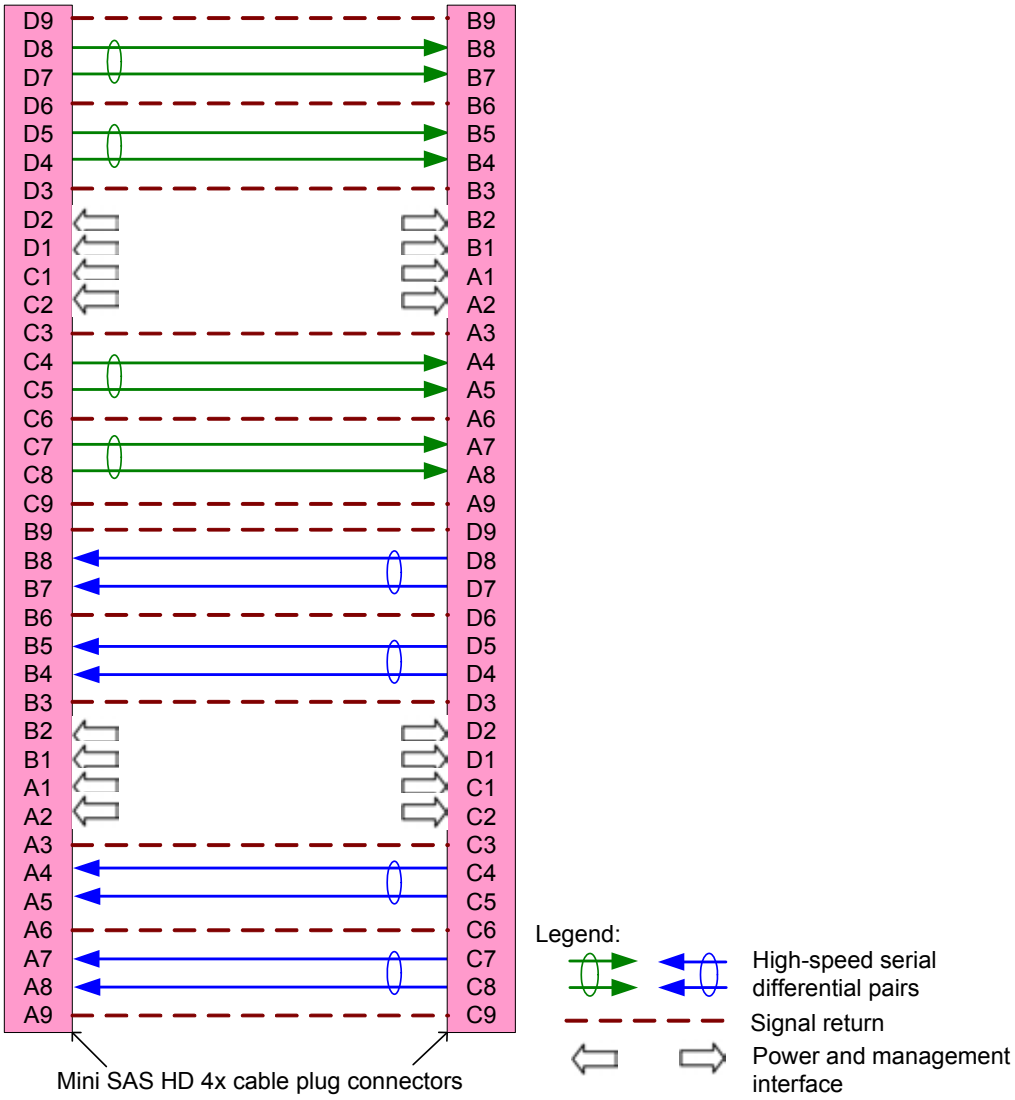


Figure 106 — SAS external cable assembly - Mini SAS HD 4x

In addition to the signal return connections shown in figure 106, one or more of the signal returns may be connected together in this cable assembly.

Figure 107 shows an example SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

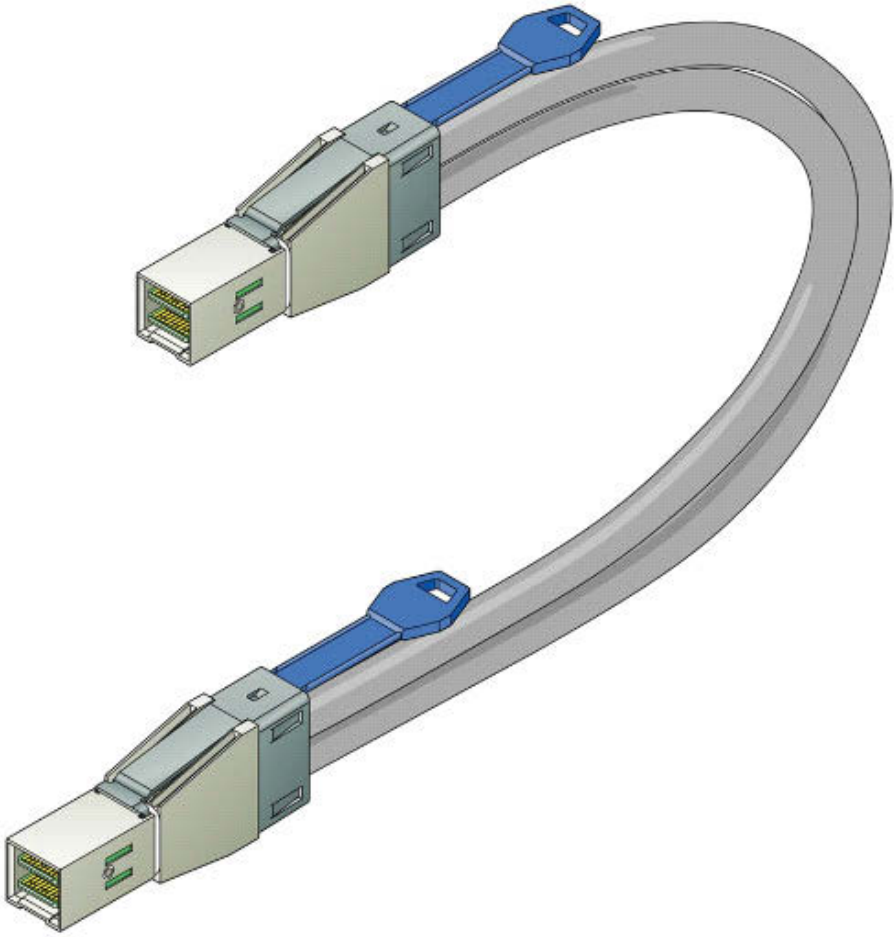


Figure 107 — SAS external cable assembly with Mini SAS HD 4x cable plug connectors

5.4.4.2.4 SAS external cable assembly - Mini SAS HD 8x

Figure 108 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

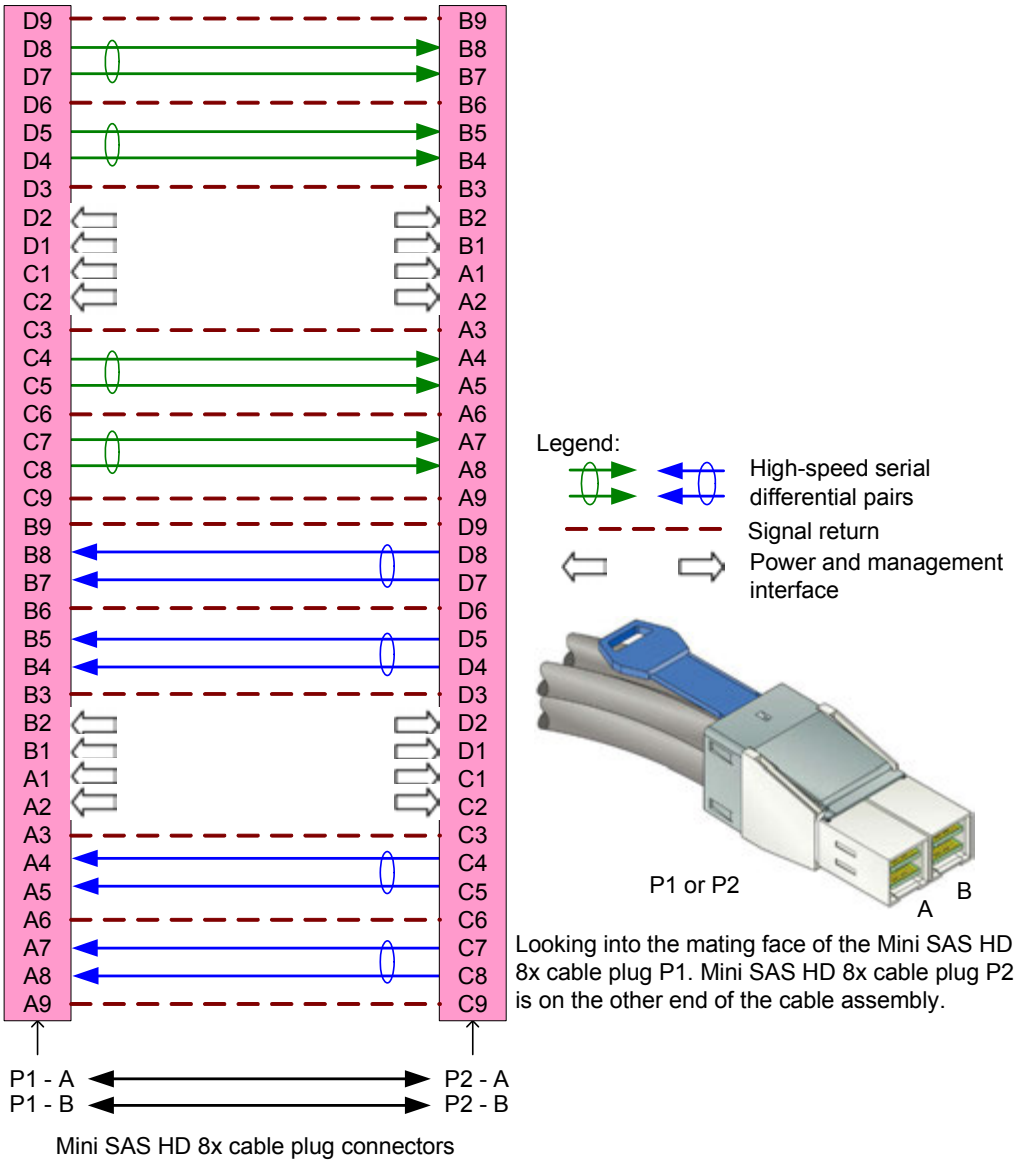


Figure 108 — SAS external cable assembly - Mini SAS HD 8x

In addition to the signal return connections shown in figure 108, one or more of the signal returns may be connected together in this cable assembly.

The cable assembly shown in figure 108 may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.4.2.6 for connector module pin assignments.

Figure 109 shows an example SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

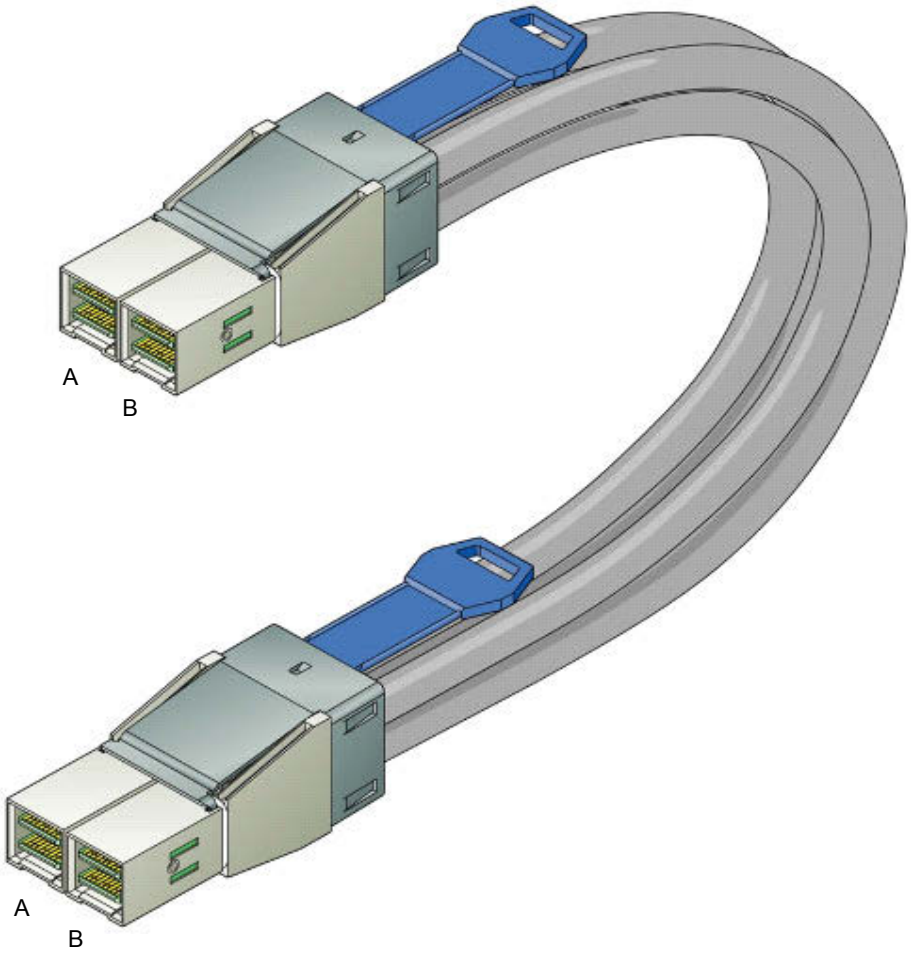


Figure 109 — SAS external cable assembly with Mini SAS HD 8x cable plug connectors

5.4.4.2.5 SAS external cable assembly - Mini SAS HD 8x to Mini SAS HD 4x

Figure 110 shows the SAS external cable assembly with a Mini SAS HD 8x cable plug connector at one end and two Mini SAS HD 4x cable plug connectors at the other end.

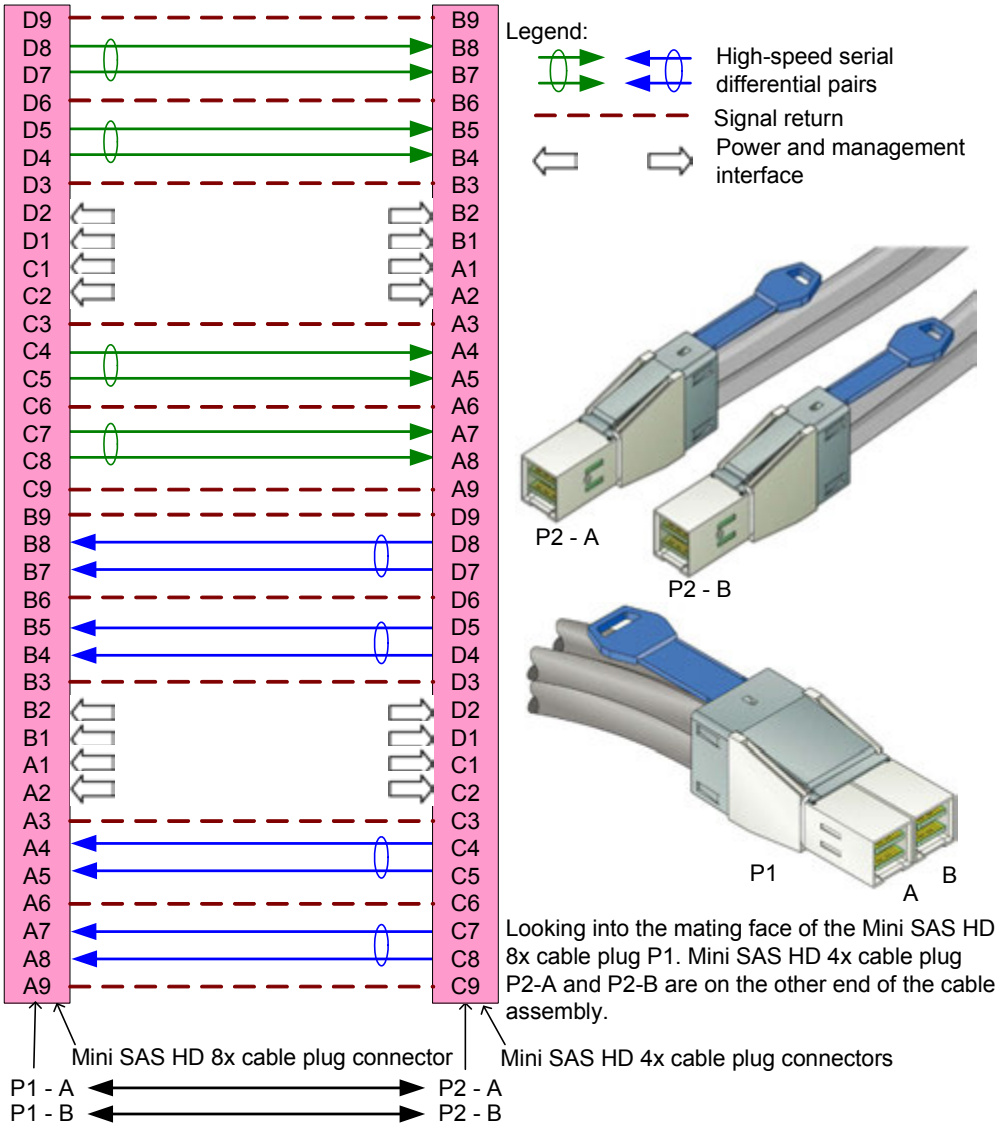


Figure 110 — SAS external cable assembly - Mini SAS HD 8x to Mini SAS HD 4x

In addition to the signal return connections shown in figure 110, one or more of the signal returns may be connected together in this cable assembly.

The cable assembly shown in figure 110 may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical links connected). See 5.4.3.4.2.6 for connector module pin assignments.

Figure 111 shows an example SAS external cable assembly with a Mini SAS HD 8x cable plug connector at one end and two Mini SAS HD 4x cable plug connectors at the other end.

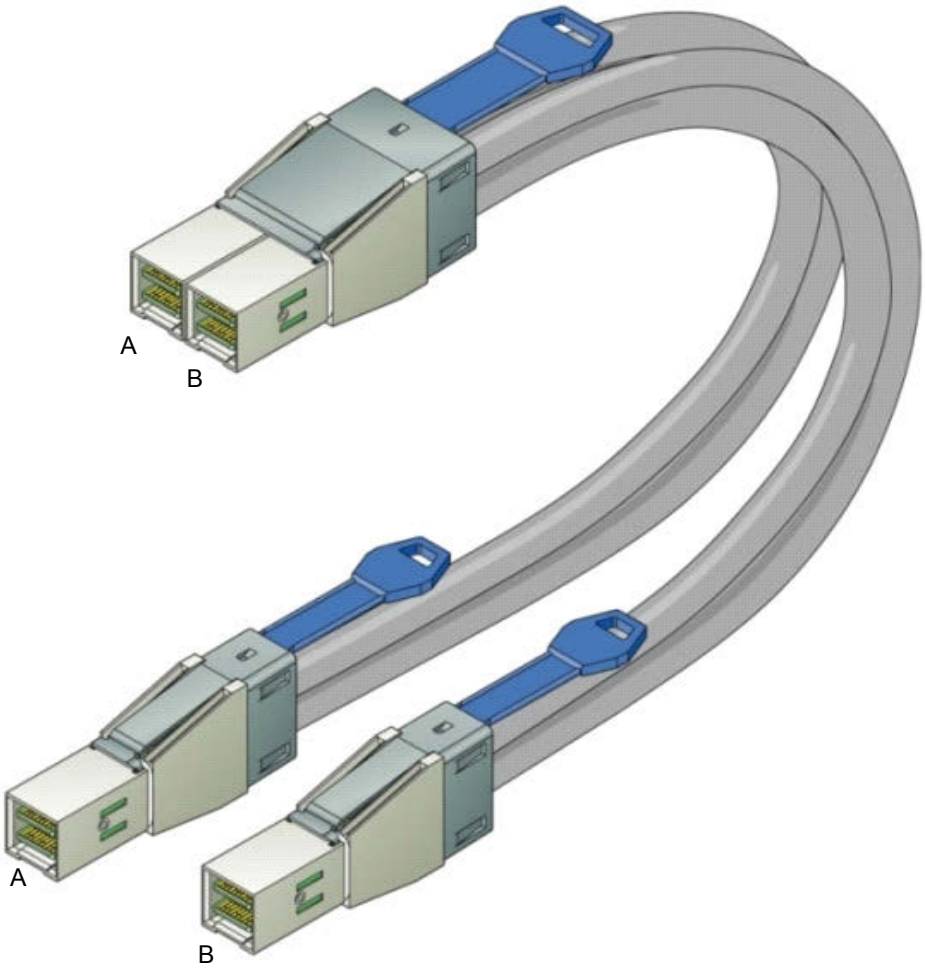


Figure 111 — SAS external cable assembly with a Mini SAS HD 8x cable plug connector and two Mini SAS HD 4x cable plug connectors

5.4.4.2.6 SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 112 shows the SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end. This cable assembly should not be used for rates greater than 6 Gbit/s.

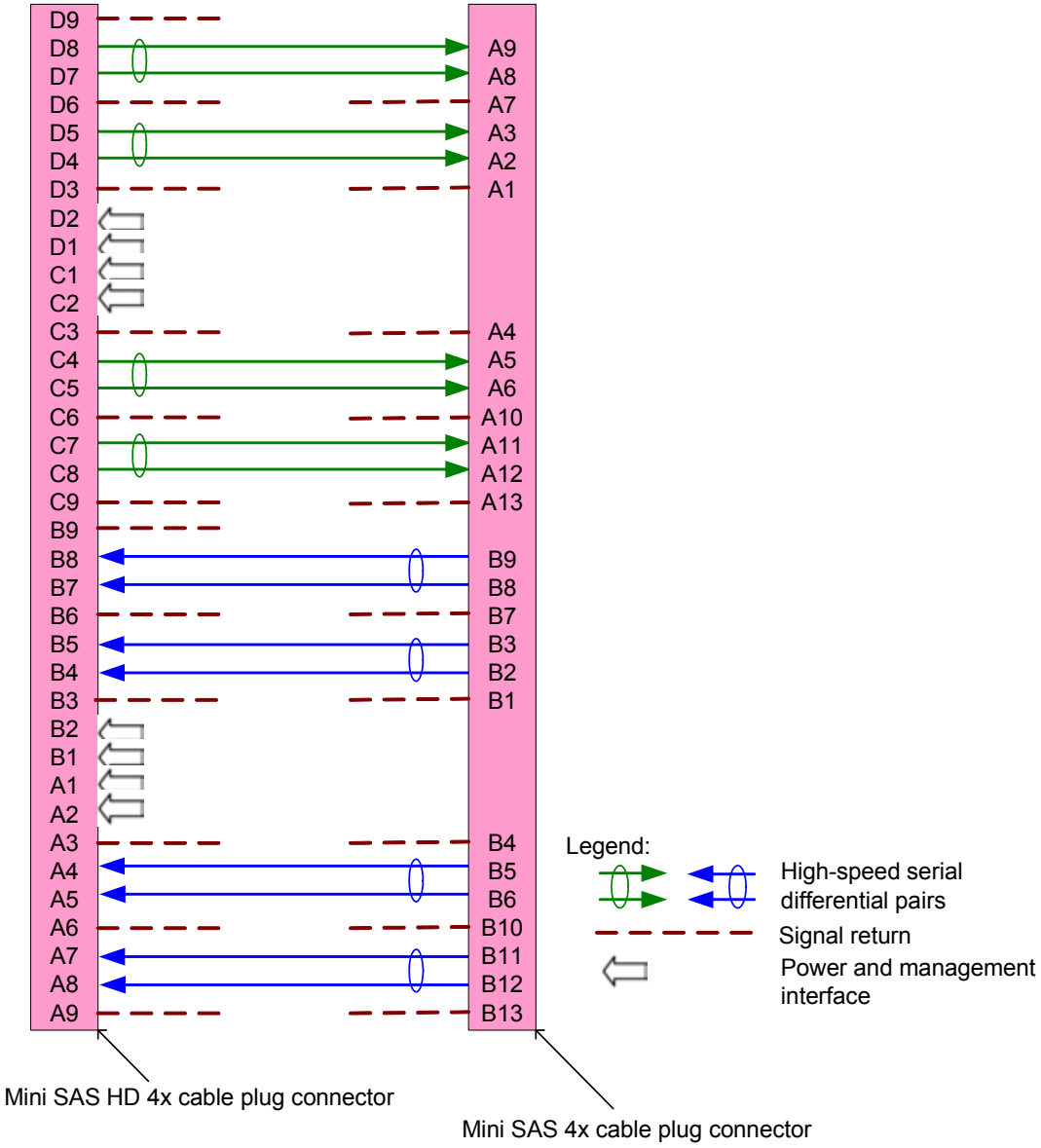


Figure 112 — SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 113 shows a example SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end.

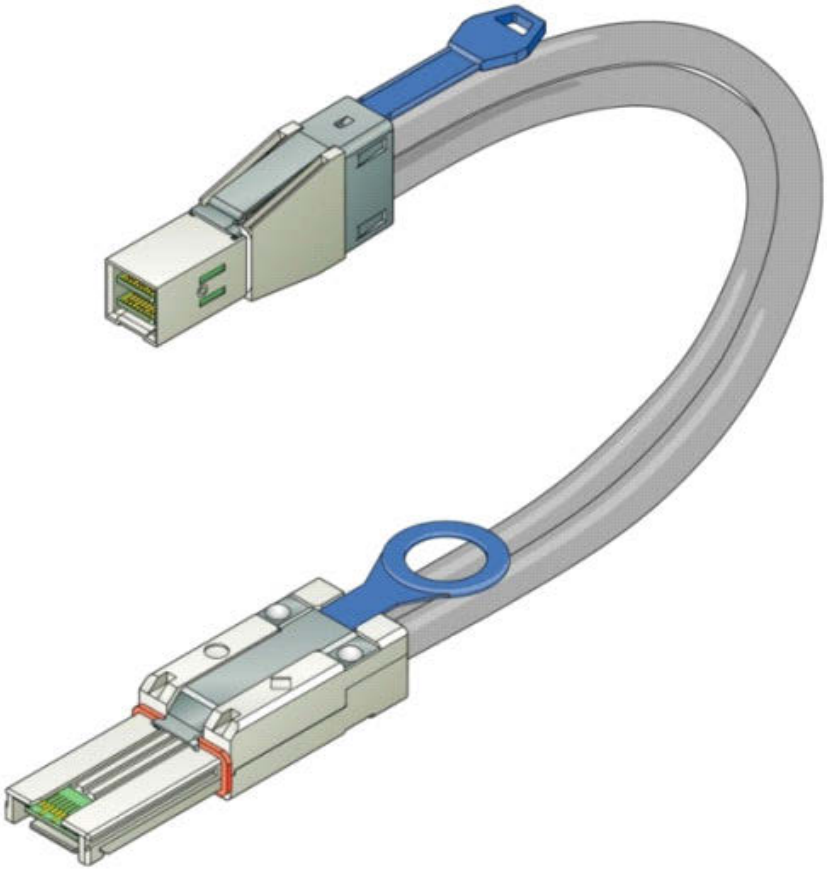


Figure 113 — SAS external cable assembly with a Mini SAS HD 4x cable plug connector and a Mini SAS 4x cable plug connector

Each signal return on one end of the cable assembly shown in figure 113 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.2.7 SAS external cable assembly - QSFP+

QSFP+ cable assemblies are defined in SFF-8685. QSFP+ cable assemblies for SAS shall comply with the TxRx connection characteristics specified in this standard (see 5.5).

5.5 TxRx connection characteristics

5.5.1 TxRx connection characteristics overview

Each TxRx connection shall support a bit error ratio (BER) that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits). The parameters specified in this standard support meeting this requirement under all conditions including the minimum input and output amplitude levels.

A TxRx connection may be constructed from multiple TxRx connection segments (e.g., backplanes and cable assemblies). It is the responsibility of the implementer to ensure that the TxRx connection is constructed from individual TxRx connection segments such that the overall TxRx connection requirements are met. Loss characteristics for individual TxRx connection segments are beyond the scope of this standard.

Each TxRx connection segment shall comply with the impedance requirements detailed in 5.5.2 for the conductive material from which they are formed. A passive equalizer network, if present, shall be considered part of the TxRx connection.

TxRx connections shall be applied only to homogeneous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

5.5.2 TxRx connection general characteristics

Table 29 defines the TxRx connection general characteristics.

Table 29 — TxRx connection general characteristics

Characteristic [a] [b]	Units	Value
Differential impedance (nominal)	Ω	100
Bulk cable or backplane:		
Differential characteristic impedance [d] [e]	Ω	100
Mated connectors:		
Differential characteristic impedance [f]	Ω	100
Passive cable assembly and backplane:		
Maximum propagation delay [c]	ns	53
Minimum $\|S_{DD21}\|$ for internal cable assemblies from 10 MHz to 4 500 MHz [g]	dB	-6
Minimum $\|S_{DD21}\|$ for internal cable assemblies from 4 500 MHz to 9 000 MHz [g] [h]	dB	-11
Minimum $\|S_{DD21}\|$ for external cable assemblies and backplanes	See 5.5	
Mini SAS 4x active cable assembly:		
Maximum propagation delay [i]	ns	133
Differential characteristic impedance [f]	Ω	100
Managed cable assembly:		
Maximum propagation delay [j]	ns	510
Differential characteristic impedance [f]	Ω	100

[a] All measurements are made through mated connector pairs.

[b] The equivalent maximum TDR rise time from 20 % to 80 % shall be 70 ps. Filtering may be used to obtain the equivalent rise time. The filter consists of the two-way launch/return path of the test fixture, the two-way launch/return path of the test cable, and the software or hardware filtering of the TDR scope. The equivalent rise time is the rise time of the TDR scope output after application of all filter components. When configuring software or hardware filters of the TDR scope to obtain the equivalent rise time, filtering effects of test cables and test fixtures shall be included.

[c] This is based on propagation delay for a 10 m Mini SAS 4x passive cable assembly. See SPL-4 for STP flow control details.

[d] The impedance measurement identifies the impedance mismatches present in the bulk cable or backplane when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the bulk cable or backplane, when present, but includes any intermediate connectors or splices.

[e] Where the bulk cable or backplane has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[f] The characteristic impedance is a measurement reference impedance for the test environment.

[g] An internal cable assembly may be a TxRx connection segment or a full TxRx connection. The full TxRx connection is required to comply with the requirements at intra-enclosure compliance points defined in 5.3 and 5.3.3.

[h] This requirement applies only for 12 Gbit/s passive cable assemblies.

[i] This is based on propagation delay for a 25 m Mini SAS 4x active cable assembly. TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-4 for STP flow control details.

[j] This is based on propagation delay for a 100 m optical cable. Managed cables shall report the propagation delay through the cable management interface (see 5.4.3.4.2.7). TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-4 for STP flow control details.

5.5.3 Passive TxRx connection S-parameter limits

S-parameters limits are calculated per the following formula:

$$\text{Measured value} < \max [L, \min [H, N + 13.3 \times \lg(f / 3\ \text{GHz})]]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 30 defines the maximum limits for S-parameter of the passive TxRx connection segment between IT_S and IR or CT_S and CR.

Table 30 — Maximum limits for S-parameters of the passive TxRx connection between IT_S and IR or CT_S and CR

Characteristic [a] [b] [c] [d]	L [e] (dB)	N [e] (dB)	H [e] (dB)	S [e] (dB / decade)	f_{min} [e] (MHz)	f_{max} [e] [f] (GHz)	f_{max} [e] [g] (GHz)
[20 × lg(|S_{CD21}|)] - [20 × lg(|S_{DD21}|)]	-10			0	100	6.0	9.0
Maximum near-end crosstalk (NEXT) for each receive signal pair [f] [h]	-26			0	100	6.0	
20 × lg(|S_{DD22}|)	-10	-7.9	-3.9	13.3	100	6.0	9.0
20 × lg(|S_{CD22}|)	-26	-12.7	-10	13.3	100	6.0	9.0
20 × lg(|S_{CD21}|)	-18			0	100	6.0	9.0
Insertion loss to crosstalk ratio (ICR(f)) [g] [h] [i] [j]	-15			0	100		6.0

[a] All measurements are made through mated connector pairs.

[b] Specifications apply to any combination of cable assemblies and backplanes that are used to form a passive TxRx connection.

[c] $|S_{CC22}|$ and $|S_{DC22}|$ are not specified.

[d] For 12 Gbit/s, these characteristics only apply to cable assemblies between CT_S and CR compliance points. 12 Gbit/s passive cable assemblies shall also comply with passive TxRx connection characteristics for trained 12 Gbit/s (see 5.5.6).

[e] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

[f] Only applies for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

[g] Only applies for 12 Gbit/s.

[h] Determine all near-end and far-end significant crosstalk sources. The sum of the crosstalk transfer ratios is measured in the frequency domain. The following equation details the summation process of the valid near-end crosstalk sources:

$$\mathrm{TotalNEXT}(f) = 10 \times \log \sum_{1}^{n} 10^{\langle \mathrm{NEXT}(f)/10 \rangle}$$

where:

f is frequency; and

n is the number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

The following equation details the summation process of the valid far-end crosstalk sources:

$$\mathrm{TotalFEXT}(f) = 10 \times \log \sum_{1}^{n} 10^{\langle \mathrm{FEXT}(f)/10 \rangle}$$

where:

f is frequency; and

n is the number of the far-end crosstalk source.

[i] All FEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

[j] The following equation defines the insertion loss to crosstalk ratio:

$$\mathrm{ICR}(f) = [10 \times \log(10^{\mathrm{TotalNEXT}(f)/10} + 10^{\mathrm{TotalFEXT}(f)/10})] - [\, 20 \times \lg(|S_{DD21}|) \,]$$

where:

f is frequency;

TotalNEXT(f)is near-end crosstalk;

TotalFEXT(f)is far-end crosstalk; and

$S_{DD21}$is insertion loss.

Figure 114 shows the passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits defined in table 30.

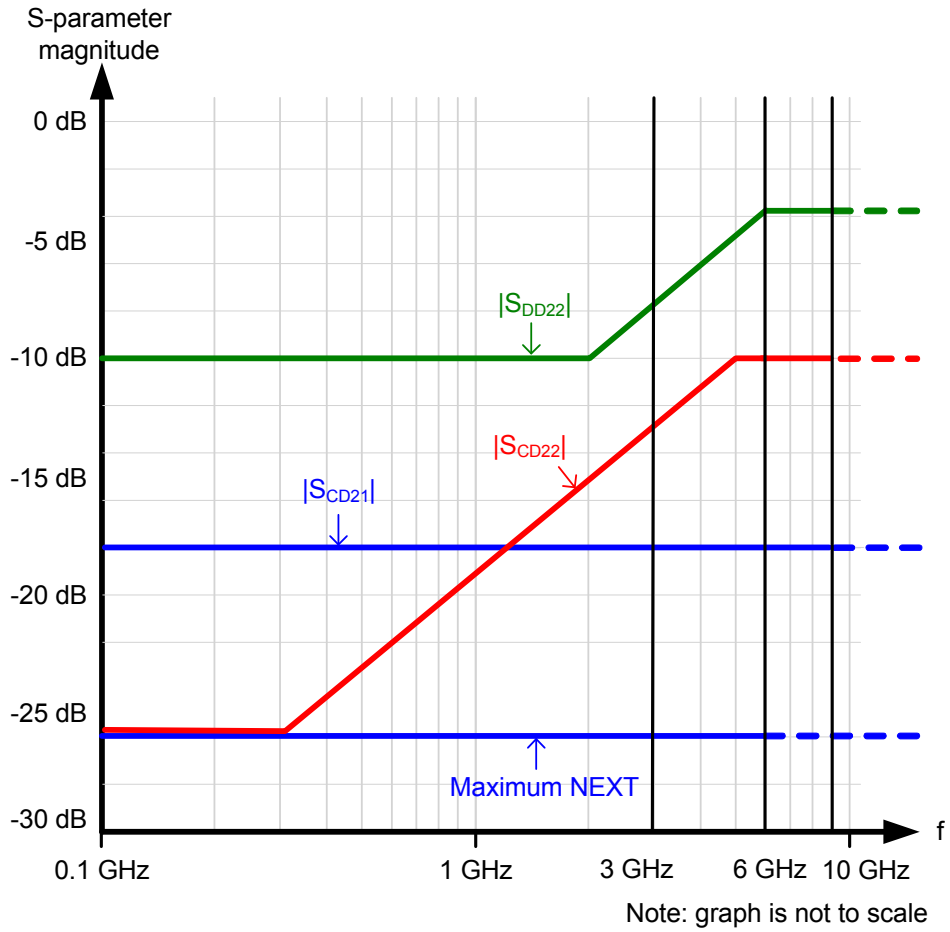


Figure 114 — Passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits

5.5.4 Passive TxRx connection characteristics for untrained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For untrained 1.5 Gbit/s and 3 Gbit/s, each external passive TxRx connection shall be designed such that its loss characteristics are less than the loss of the TCTF test load plus ISI at CT at 3 Gbit/s (see figure 125 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbit/s and 3 Gbit/s, each internal passive TxRx connection shall be designed such that its loss characteristics are less than:

a) the loss of the TCTF test load plus ISI at IT at 3 Gbit/s (see figure 124 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz; or
b) the loss of the low-loss TCTF test load plus ISI (see figure 129 in 5.6.4) over the frequency range of 50 MHz to 3 000 MHz if the system supports SATA devices using Gen2i levels (see SATA) and the receiver device does not support SATA Gen2i levels through the TCTF test load (see table 59 in 5.8.5.4).

For untrained 1.5 Gbit/s and 3 Gbit/s, each passive TxRx connection shall meet the delivered signal specifications in table 59 (see 5.8.5.4).

For untrained 6 Gbit/s (i.e., SATA devices using Gen3i levels (see SATA)), then the internal passive TxRx connection should be less than the CIC (see SATA). See SATA for delivered signal specifications.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included in the TxRx connection.

5.5.5 Passive TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the passive TxRx connection shall support a bit error ratio (BER) that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on simulation results using:

a) S-parameter measurements of the passive TxRx connection;
b) the reference transmitter device (see 5.8.4.6.5); and
c) the reference receiver device (see 5.8.5.7.3).

The simulation shall not include sources of crosstalk. Since simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 115 shows an example circuit for simulation. The specific simulation program used is not specified by this standard. Annex D includes the StatEye program from http://www.stateye.org, which is one such simulation program.

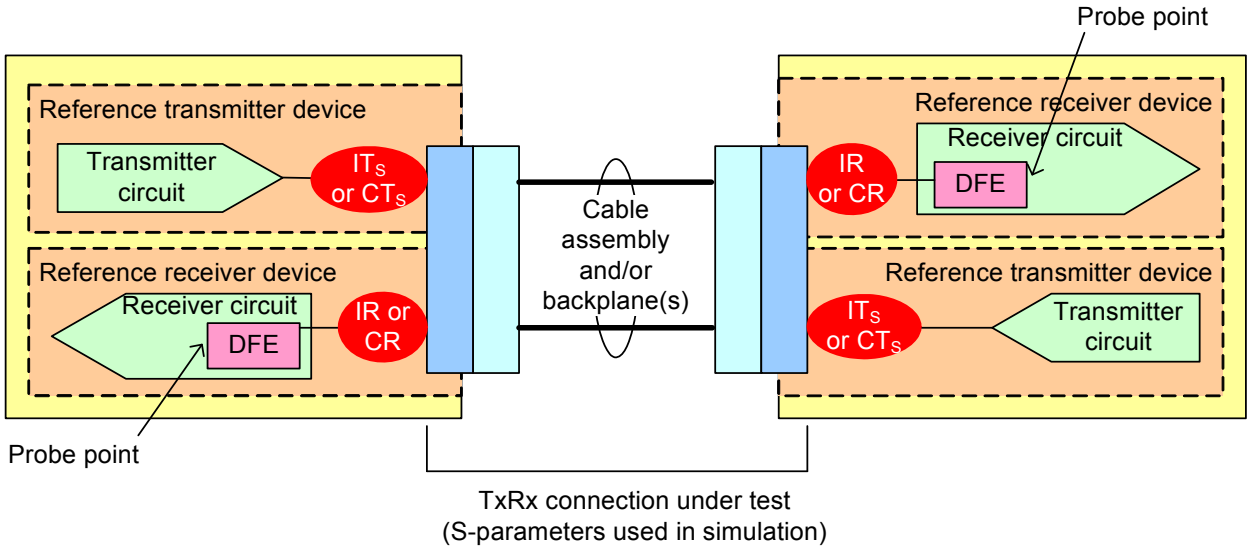


Figure 115 — Example passive TxRx connection compliance testing for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Table 31 defines the required passive TxRx connection characteristics.

Table 31 — Passive TxRx connection characteristics for trained 6 Gbit/s

Characteristic	Units	6 Gbit/s
Minimum voltage [a]	mV(P-P)	84
Maximum TJ [a]	UI	0.64

[a] As reported by simulation of the passive TxRx connection S-parameters with the reference transmitter device and the reference receiver device. Values are reported at a BER of 10^{-15} inside the reference receiver device after equalization at 6 Gbit/s. This standard does not define values for trained 3 Gbit/s and 1.5 Gbit/s. Passive TxRx connections that comply with the 6 Gbit/s characteristics are expected to operate correctly at slower physical link rates.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 10 m long, provided that no other TxRx connection segments are included in the TxRx connection.

A passive TxRx connection supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s may not support untrained 1.5 Gbit/s and 3 Gbit/s and may not support SATA. Trained transceiver devices incorporate features to allow them to operate over the following passive TxRx connections:

a) passive TxRx connections with higher loss than TxRx connections;
b) passive TxRx connections defined in this standard for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4); and
c) passive TxRx connections supporting SATA.

5.5.6 Passive TxRx connection characteristics for trained 12 Gbit/s

For trained 12 Gbit/s, the passive TxRx connection shall support a BER that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on end to end simulation results (see 5.7.1) using:

a) S-parameter measurements or model of the passive TxRx connection segment from CT_S to CR or IT_S to IR (see figure 13);
b) S-parameter measurements of the passive connection, S-parameter models of the passive connection, or reference S-parameter models (see C.2) from all significant crosstalk aggressors;
c) reference transmitter devices (see 5.8.4.7.3) providing signals to the through channel and crosstalk channels:
   A) using the reference transmitter device peak to peak voltage defined in table 52;
   B) using reference equalization coefficients (see 5.7.4); and
   C) generating no RJ or TJ;
d) the reference receiver device with optimal DFE weights (see 5.8.5.7.3 and table 32); and
e) reference S-parameter models to complete the simulation diagram (see figure 116), according to the appropriate usage model (see C.2.3).

The simulation shall include all significant crosstalk sources. The crosstalk sources shall be modeled as asynchronous to the TxRx connection segment under test (see C.1).

Simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 116 shows an example TxRx connection for trained 12 Gbit/s.The TxRx connection segment under test is the segment between CT_S and CR or IT_S and IR. XCS_n represents the crosstalk connection segments, where n is a numerical index identifying multiple crosstalk aggressors.

The specific simulation program used is not specified by this standard. See Annex C and Annex E.

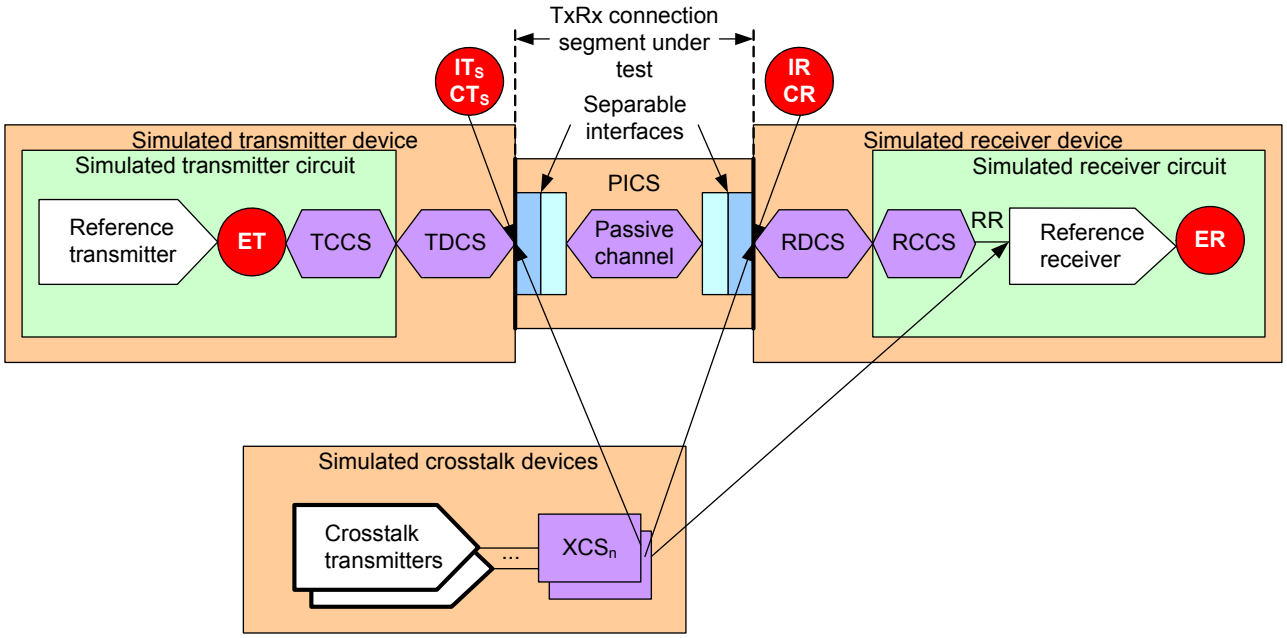


Figure 116 — Example passive TxRx connection compliance testing for trained 12 Gbit/s

The following reference through S-parameter files shall be used for this simulation, according to the appropriate usage model:

a) **<usage>_ET_ITs.s4p**: through between ET and CT_S or between ET and IT_S; and
b) **<usage>_CR_RR.s4p**: through between CR and RR or between IR and RR.

Labels beginning by <usage> indicate reference S-parameter files. <usage> represents a prefix that is set according to the selected usage model (see C.2.3). RR is the receiver die attachment point to RCCS.

Symmetrical models have the same through transfer function between ET and CT_S or between ET and IT_S as between CR and RR or between IR and RR. Symmetrical models shall use the same transfer function for both directions (i.e., **<usage>_ET_ITs.s4p**).

Asymmetrical models do not have the same through transfer function between ET and CT_S or between ET and IT_S as between CR and RR or between IR and RR. For asymmetrical models, the reverse transfer function between ET and CT_S or between ET and IT_S shall also be used (i.e., **<usage>_ET_ITs_rev.s4p**).

For each usage model, four types of crosstalk aggressor reference S-parameter files are defined for this simulation:

a) **<usage>_ET_ITs_FEXT.s4p**: crosstalk caused by elements between ET and CT_S or between ET and IT_S;
b) **<usage>_CR_RR_FEXT.s4p**: crosstalk caused by elements between CR and RR or between IR and RR;
c) **<usage>_CR_RR_NEXT.s4p**: crosstalk caused by elements between CR and RR or between IR and RR; and
d) **<usage>_ET_ITs_NEXT.s4p**: crosstalk caused by elements between ET and CT_S or between ET and IT_S.

Figure 117 shows the usage of the crosstalk and through files defined for the end to end simulation of TxRx connection segments between CT_S and CR or IT_S and IR. The boxes labeled PICS FEXT, PICS NEXT, PICS rev, and PICS indicate measured transfer functions (e.g., S-parameters). The boxes with a dashed boundary indicate reference S-parameter files. <usage> represents a prefix that is set according to the selected usage model (see C.2.3).

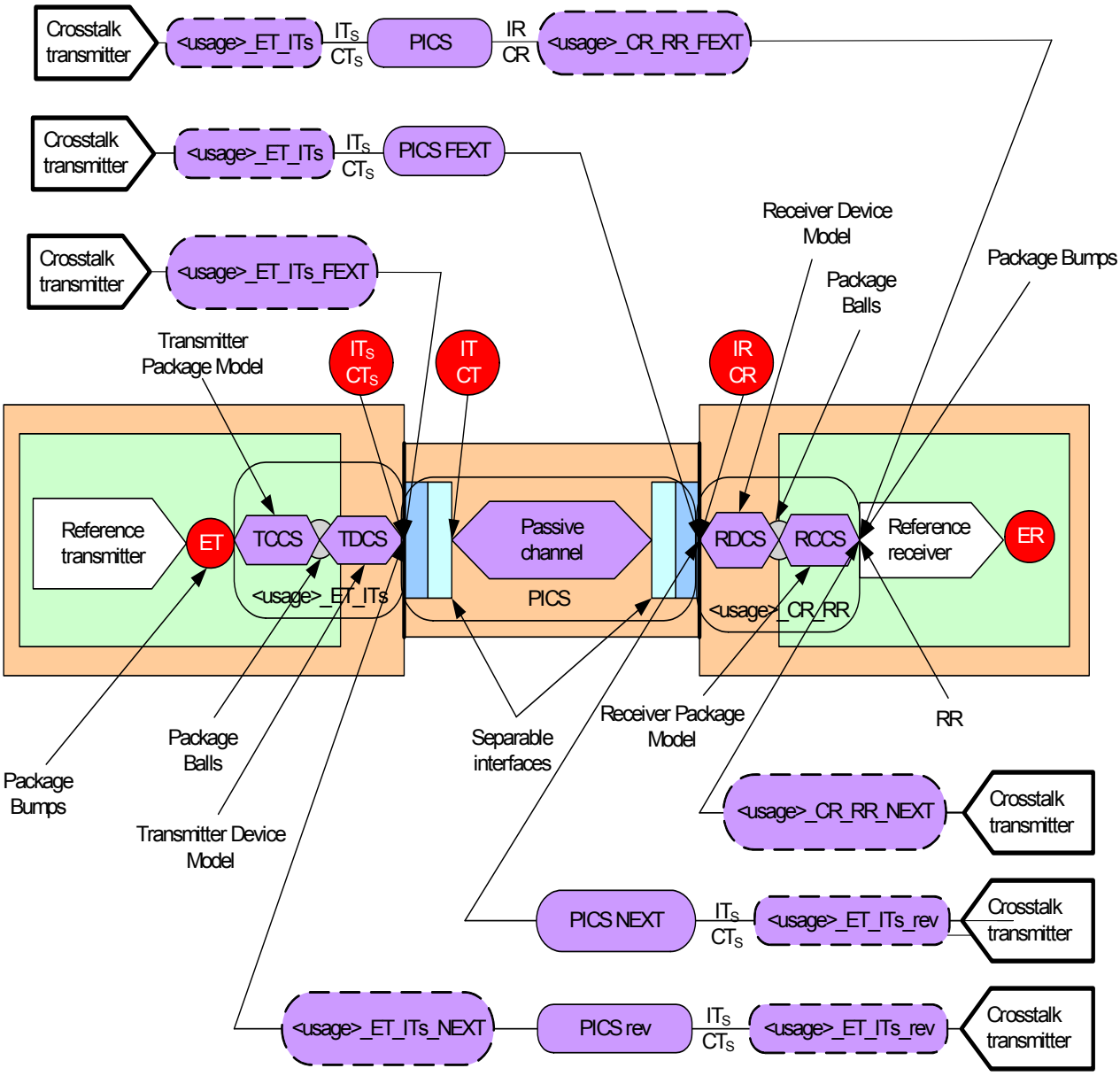


Figure 117 — Passive TxRx connection segment between CT_S and CR or IT_S and IR end to end simulation diagram for trained 12 Gbit/s

Table 32 defines the required passive TxRx connection characteristics. Refer to the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3) used in table 32.

Table 32 — Passive TxRx connection characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a] [b] [c]	V/V	-0.15	0	ET
VMA [d] [e]	mV(P-P)	80		ET
Coefficient 3 (i.e., C3) [a] [b] [f]	V/V	-0.3	0	ET
Reference pulse response cursor peak to peak amplitude [g]	mV(P-P)	135		ER
Vertical eye opening to reference pulse response cursor ratio [h] [i]	%	45		ER
DFE coefficient amplitude to reference pulse response cursor ratio [j]	%	-50	50	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then that coefficient is forced to its maximum limit and the other coefficients are recalculated.

[b] C2 = 1 - |C1| - |C3|.

[c] If C1 exceeds its minimum (negative) limit, then that coefficient is forced to its minimum limit and C3 is recalculated.

[d] VMA = $2K_0$ (C1 + C2 + C3)
where:
K_0 is the output gain;
C1 is coefficient 1 (see 5.8.4.7.3);
C2 is coefficient 2 (see 5.8.4.7.3); and
C3 is coefficient 3 (see 5.8.4.7.3).

[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3^2))^{0.5}$$

where:
C1' and C3' are values that satisfy the minimum VMA criterion.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 135.

[h] The vertical eye opening includes the effects of crosstalk (see C.1).

[i] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the transmitter device.

[j] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(di)) divided by the reference pulse response cursor) (see 5.8.5.7.3).

For external cable assemblies, these electrical requirements are consistent with using good quality passive Mini SAS HD cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included between CT_S and CR in the TxRx connection and the total ICR is below the limit specified in table 30.

Editor's Note 3: Add Passive TxRx connection characteristics for trained 22.5 Gbit/s

5.5.7 TxRx connection characteristics for active cable assemblies

5.5.7.1 Active cable assembly electrical characteristics for trained 6 Gbit/s overview

Active cable assemblies shall support a bit error ratio (BER) that is less than 10^{-12} when used with transmitter devices and trained receiver devices defined in 5.8.

In addition to complying with electrical characteristics necessary for the required BER performance, active cable assemblies shall comply with the OOB signaling defined in 5.11. The circuitry incorporated in unmanaged cable assemblies shall operate in the D.C. mode. Managed active cable assemblies supporting 6 Gbit/s operation may operate in the D.C. mode or in the optical mode (see 5.11). The circuitry incorporated in active cable assemblies shall preserve OOB signals with response times that support the OOB signal receiver device detection requirements in table 83 (see 5.11.3).

5.5.7.2 Active cable assembly output electrical characteristics for trained 6 Gbit/s

Table 33 defines active cable assembly output electrical characteristics for trained 6 Gbit/s.

Table 33 — Active cable assembly output electrical characteristics for trained 6 Gbit/s

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage	mV (P-P)	400		1 200
RJ [a b d]	UI			0.22
TJ [a c d]	UI			0.56

[a] Based on TX input per table 42 (see 5.8.4.6.1) and recommended TX interoperability settings per table 45 (see 5.8.4.6.4).
[b] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] The TJ measurement shall be performed with at least 58 dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC enabled.
[d] The measurement shall include the effects of the JTF (see 5.8.3.2).

For active cable assemblies, these characteristics are consistent with good quality half-active (i.e., with circuitry only on the receive end of the assembly) cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 25 m long, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbit/s and 3 Gbit/s. Active cables that comply with trained 6 Gbit/s characteristics should operate within the specified error rate at slower physical link rates.

5.5.7.3 Active cable assembly S-parameter limits for trained 6 Gbit/s and trained 12 Gbit/s

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × lg(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 34 defines the maximum limits for S-parameters of the active cable assembly.

Table 34 — Maximum limits for S-parameters for active cable assemblies

Characteristic [a] [b]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] [d] (GHz)	f_{max} [c] [e] (GHz)
$\|S_{CC22}\|$ [f]	-6.0	-5.0	-1.0	13.3	100	6.0	9.0
$\|S_{DD11}\|$, $\|S_{DD22}\|$ [f]	-10	-7.9	-3.9	13.3	100	6.0	9.0
$\|S_{CD11}\|$, $\|S_{CD22}\|$ [f]	-20	-12.7	-10	13.3	100	6.0	9.0

[a] Power shall be applied to the active cable assembly during these measurements.
[b] $|S_{CC11}|$, $|S_{DC11}|$ and $|S_{DC22}|$ are not specified.
[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.
[d] Applies for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[e] Applies for 12 Gbit/s.
[f] For $|S_{CC22}|$, $|S_{DD22}|$ and $|S_{CD22}|$ measurements, the transmitter device attached to the active cable assembly under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See F.11.4.4 and F.11.4.5.

Figure 118 shows the active cable assembly $|S_{CC22}|$, $|S_{DD11}|$, $|S_{DD22}|$, $|S_{CD11}|$, and $|S_{CD22}|$ limits defined in table 34.

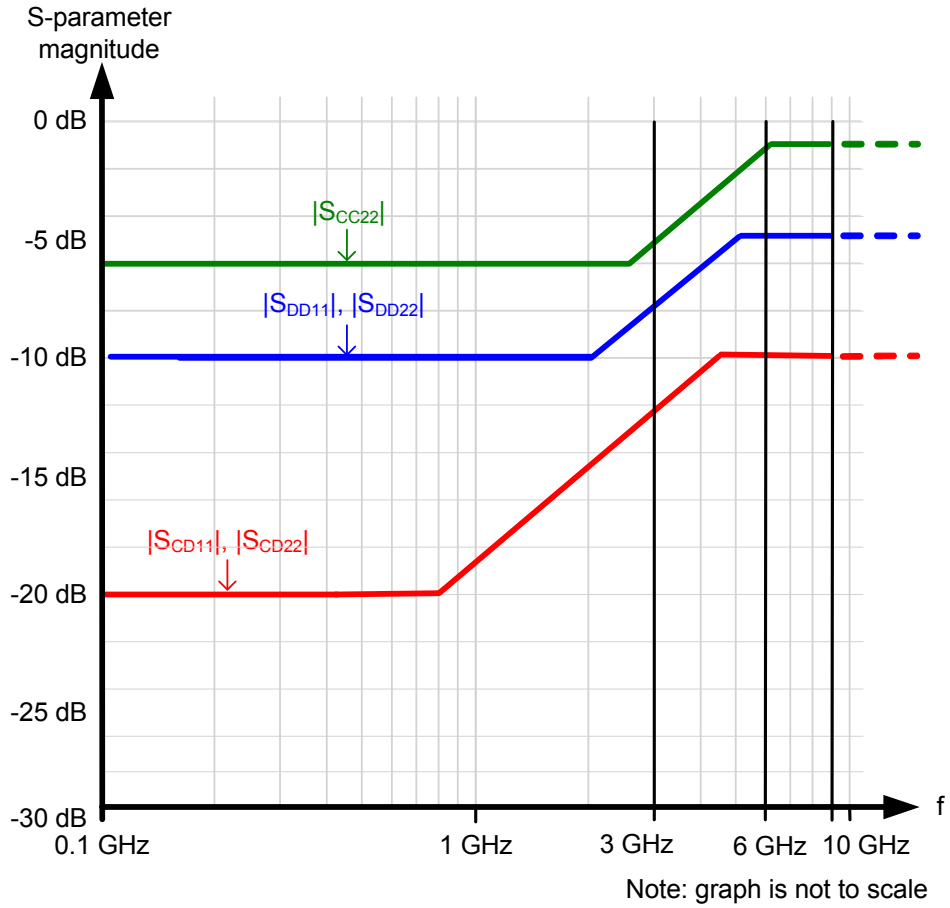


Figure 118 — Active cable S-parameter limits

5.5.7.4 Active cable assembly electrical characteristics overview for 12 Gbit/s

Active cable assemblies supporting 12 Gbit/s operation shall comply with OOB in the optical mode (see 5.11) and shall support pass through of SSC. The optical mode does not support transmitter training. The circuitry incorporated in these cable assemblies preserves OOB signals with response times that support the OOB signal receiver device detection requirements in table 83 (see 5.11.3).

5.5.7.5 Active cable assembly electrical characteristics for 12 Gbit/s

Figure 119 describes the eye mask used to calibrate the input in an active cable assembly at CT_S (see figure 14) to test the output of an active cable assembly at CR (see figure 14) for 12 Gbit/s.

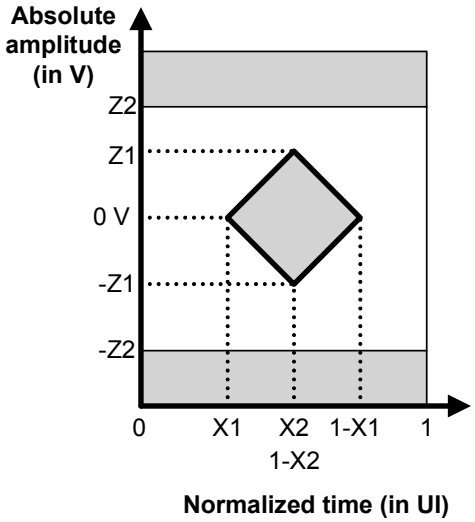


Figure 119 — Active cable eye mask for 12 Gbit/s

Table 35 defines the signal input and output characteristics for an active cable assembly for 12 Gbit/s.

Table 35 — Active cable assembly electrical characteristics for 12 Gbit/s

Signal characteristic	Units	CT_S [a]	CR
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 119) [b c d]	mV(P-P)	1 200	1 200
Minimum eye opening (i.e., 2 × Z1 in figure 119) [b c e]	mV(P-P)	200	360
Maximum half of TJ (i.e., X1 in figure 119) [b c e f]	UI	0.175	0.35
Maximum RJ [b d f g]	UI	0.15	0.45
Center of bit time (i.e., X2 in figure 119)	UI	0.5	0.5

[a] This column represents signal input characteristics to a cable assembly under test.
[b] All crosstalk sources shall be active with representative traffic during the measurement.
[c] Maximum TJ at CT_S and maximum RJ at CT_S shall be applied during this measurement.
[d] The maximum peak to peak voltage measurement and RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[e] The minimum eye opening measurement and TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC enabled for a period of at least $33.\overline{3}$ µs (i.e., a full SSC cycle).
[f] The measurement shall include the effects of the JTF (see 5.8.3.2).
[g] The maximum RJ at CT_S shall be applied during this measurement.

For active cable assemblies, these characteristics are consistent with good quality full-active cable assemblies (i.e., with circuitry on both ends of each differential signal pair of the cable assembly) constructed with shielded twinaxial cable with 26 AWG solid wire up to 15 m or optical cable assemblies up to 100 m, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbit/s and 3 Gbit/s. Active cable assemblies that comply with active cable assembly electrical characteristics for 12 Gbit/s characteristics should also comply with active cable assembly electrical characteristics for 6 Gbit/s (see 5.5.7) with optical mode enabled and should operate within the specified bit error ratio at slower physical link rates.

Editor's Note 4: Add active cable characteristics for 22.5 Gbit/s.

5.6 Test loads

5.6.1 Test loads overview

This standard uses a test load methodology to specify transmitter device signal output characteristics (see 5.8.4.4 and 5.8.4.5) and delivered signal characteristics (see 5.8.5.4). This methodology specifies the signal as measured at specified probe points in specified test loads.

For untrained 1.5 Gbit/s and 3 Gbit/s (e.g., the physical link rate is negotiated in Final-SNW (see SPL-4) or the physical link is SATA), the test loads used by the methodology are:

a) zero-length test load (see 5.6.2): used for testing transmitter device compliance points and receiver device compliance points;
b) transmitter compliance transfer function (TCTF) test load (see 5.6.3): used for testing transmitter device compliance points;
c) low-loss TCTF test load (see 5.6.4): used for testing transmitter device compliance points if SATA devices using Gen2i levels (see SATA) are supported and the SAS receiver device does not support the signal levels received through a full TCTF test load (see 5.6.3); and
d) CIC (see SATA): used for testing transmitter device compliance points if SATA devices using Gen3i levels (see SATA) are supported.

For trained (e.g., the physical link rate is negotiated in Train_Rx-SNW (see SPL-4)) 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the test loads used by the methodology are:

a) zero-length test load (see 5.6.2) used for:
   A) testing transmitter device compliance points;
   B) testing receiver device compliance points; and
   C) used with a reference receiver device (see 5.8.5.7.3) in simulation to determine the delivered signal;

   and
b) reference transmitter test load (see 5.6.5) is used with a reference receiver device (see 5.8.5.7.3) in simulation to determine the delivered signal.

For 12 Gbit/s, the zero-length test load (see 5.6.2) test load is used for:

a) testing transmitter device compliance points;
b) testing receiver device compliance points;
c) measuring crosstalk; and
d) capturing signals for use in simulation.

In addition to measurement with the zero-length test load, 12 Gbit/s may use end to end simulation and, depending on the usage model, use reference transfer functions to determine the delivered signal. See 5.7 and Annex C.

Physical positions denoted as probe points identify the position in the test load where the signal properties are measured, but do not imply that physical probing is used for the measurement. Physical probing may be disruptive to the signal and should not be used unless verified to be non-disruptive.

5.6.2 Zero-length test load

Figure 120 shows the zero-length test load as used for testing a transmitter device compliance point.

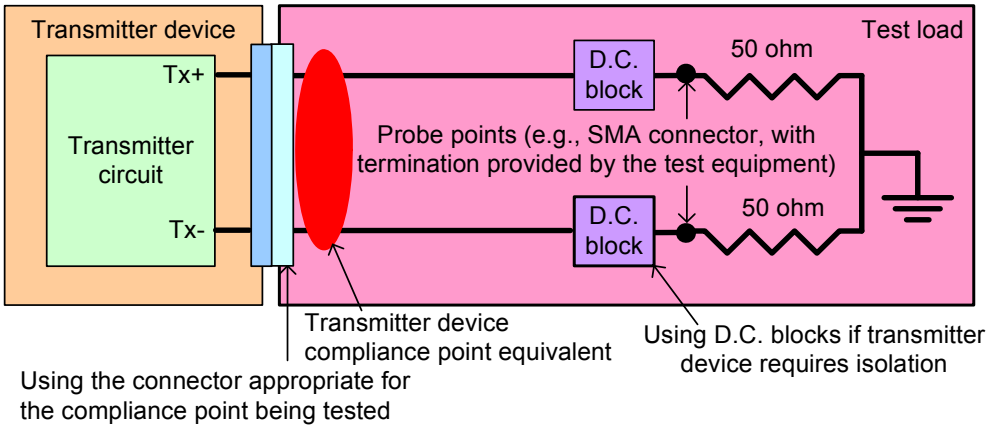


Figure 120 — Zero-length test load for transmitter device compliance point

Figure 121 shows the zero-length test load as used for testing a receiver device compliance point.

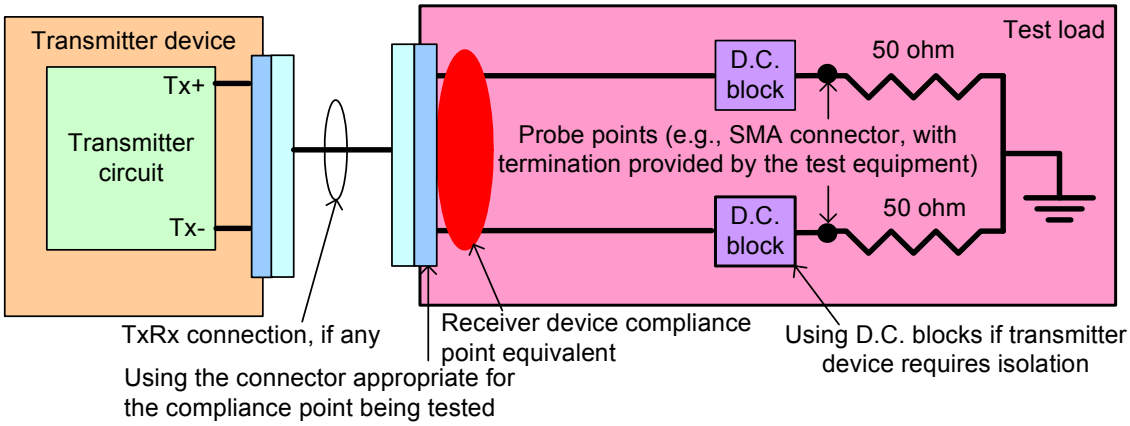


Figure 121 — Zero-length test load for receiver device compliance point

Figure 120 and figure 121 show ideal designs. Implementations may include:

a) insertion loss between the compliance and probe points; and
b) return loss due to one or more impedance mismatches between the compliance point and 50 Ω termination points.

Not shown are non-ideal effects of the test equipment raw measurements (e.g., additional insertion loss and return loss). For de-embedding methods to remove non-ideal effects, see Annex F.

Usage of fixturing and test equipment shall comply with the requirements defined in this subclause. The requirements in this subclause include the combined effects of the fixturing and test equipment.

The zero-length test load is defined by a set of S-parameters (see F.11). Only the magnitude of $S_{DD21}(f)$ and the magnitude of $S_{DD11}(f)$ are specified by this standard.

The zero-length test load, including all fixturing and instrumentation required for the measurement, shall comply with the following equations:

For 50 MHz < f ≤ 6.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log(e) \times ((1.0 \times 10^{-6} \times \sqrt{f}) + (2.8 \times 10^{-11} \times f) + (5.3 \times 10^{-21} \times f^2)) - 0.2\text{dB}$$

$$|S_{DD11}(f)| \leq \text{-15 dB}$$

where:

$|S_{DD21}(f)|$ is themagnitude of $S_{DD21}(f)$;

$|S_{DD11}(f)|$ is the magnitude of $S_{DD11}(f)$; and

f is the signal frequency in Hz.

Figure 122 shows the allowable $|S_{DD21}(f)|$ of a zero-length test load and the $|S_{DD21}(f)|$ of a sample zero-length test load.

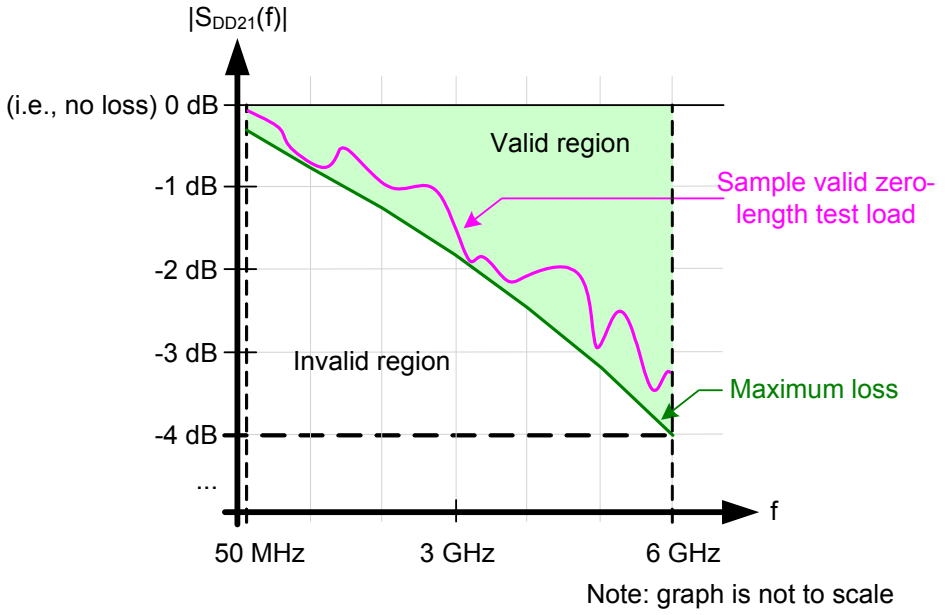


Figure 122 — Zero-length test load $|S_{DD21}(f)|$ requirements

5.6.3 TCTF test load

Figure 123 shows the TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

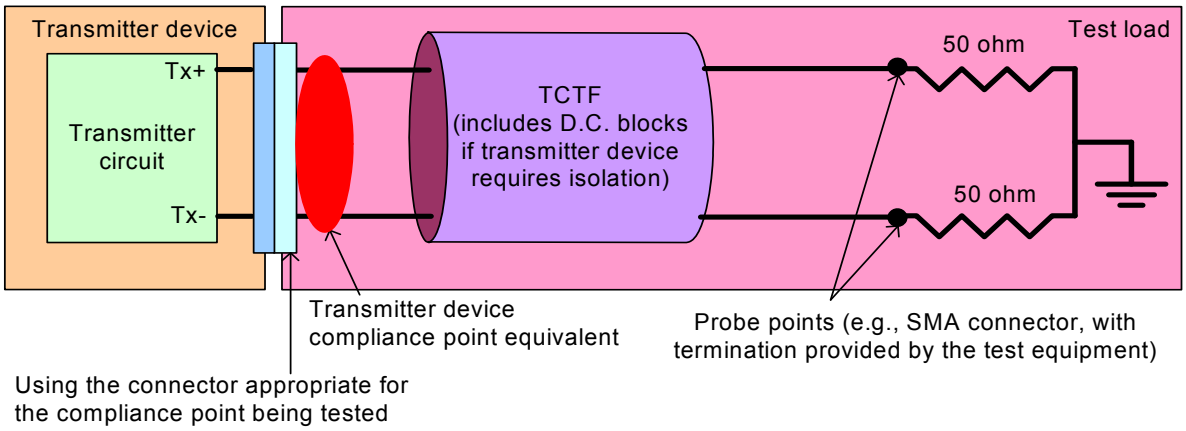


Figure 123 — TCTF test load

The TCTF test load shall meet the requirements in 5.5.2. The nominal impedance shall be the target impedance.

The TCTF test load is defined by a set of S-parameters (see F.11). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

For testing an untrained 3 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$\left|S_{DD21}(f)\right| \leq -20 \times \log(e) \times ((6.5 \times 10^{-6} \times \sqrt{f}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^2))\text{dB}$$

and for 3.0 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq$ -10.9 dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 300\text{ MHz})|$ - $|S_{DD21}(f = 1\,500\text{ MHz})| >$ 3.9 dB

where:

$|S_{DD21}(f)|$ is the magnitude of $S_{DD21}(f)$; and

f is the signal frequency in Hz.

Figure 124 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 3 Gbit/s.

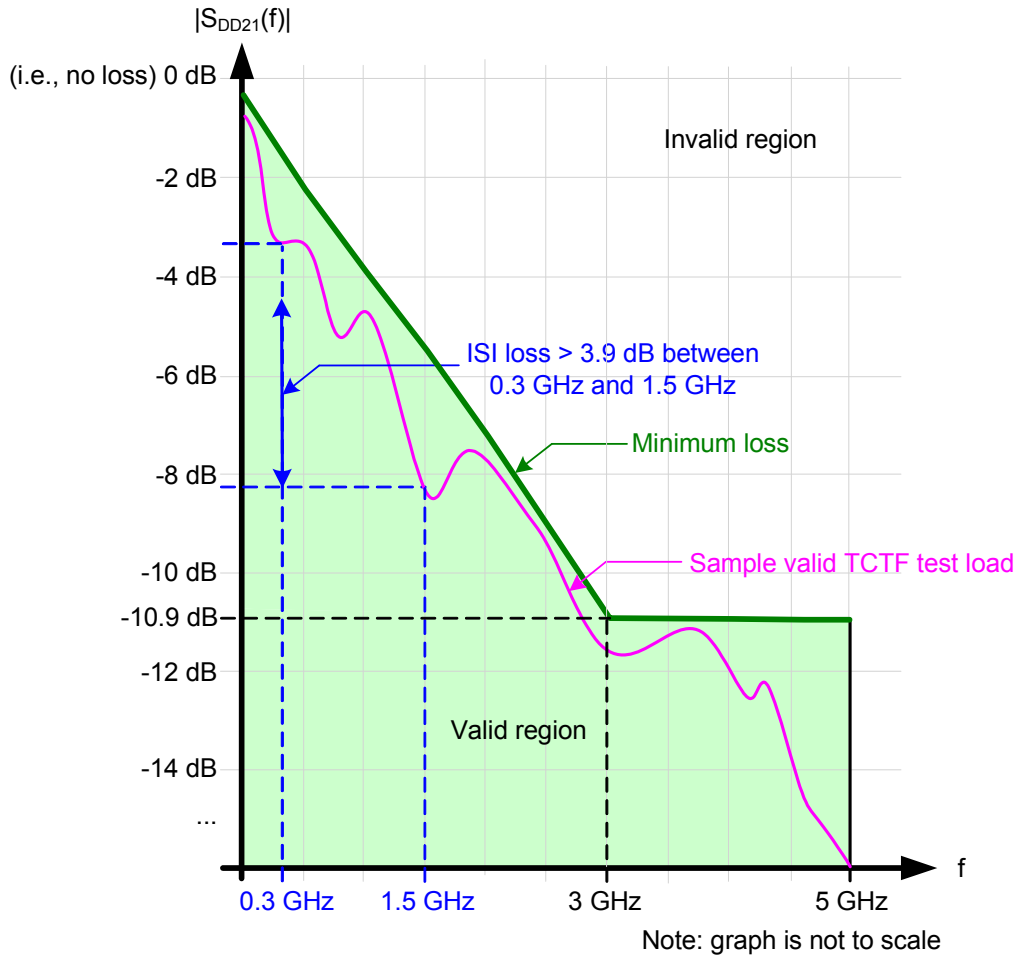


Figure 124 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 3 Gbit/s

For testing an untrained 3 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log(e) \times ((1.7 \times 10^{-5} \times \sqrt{f}) + (1.0 \times 10^{-10} \times f))\text{dB}$$

and for 3.0 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq$ -10.7 dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 300\text{ MHz})| - |S_{DD21}(f = 1\,500\text{ MHz})| > 3.9$ dB

where:

$|S_{DD21}(f)|$ is the magnitude of $S_{DD21}(f)$; and

f is the signal frequency in Hz.

Figure 125 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 3 Gbit/s.

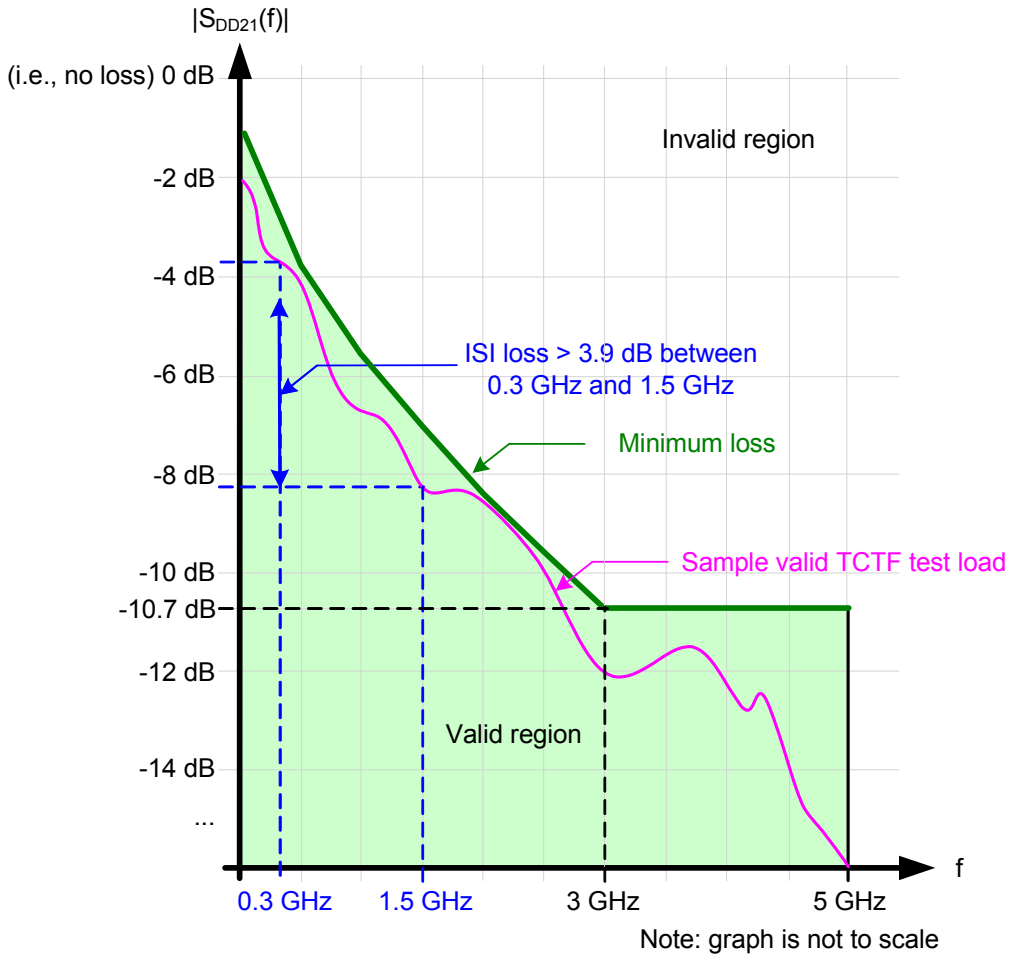


Figure 125 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 3 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log(e) \times ((6.5 \times 10^{-6} \times \sqrt{f}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^2))\text{dB}$$

and for 1.5 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq$ -5.4 dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 150\text{ MHz})| - |S_{DD21}(f = 750\text{ MHz})| >$ 2.0 dB

where:

$|S_{DD21}(f)|$ is the magnitude of $S_{DD21}(f)$; and

f is the signal frequency in Hz.

Figure 126 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 1.5 Gbit/s.

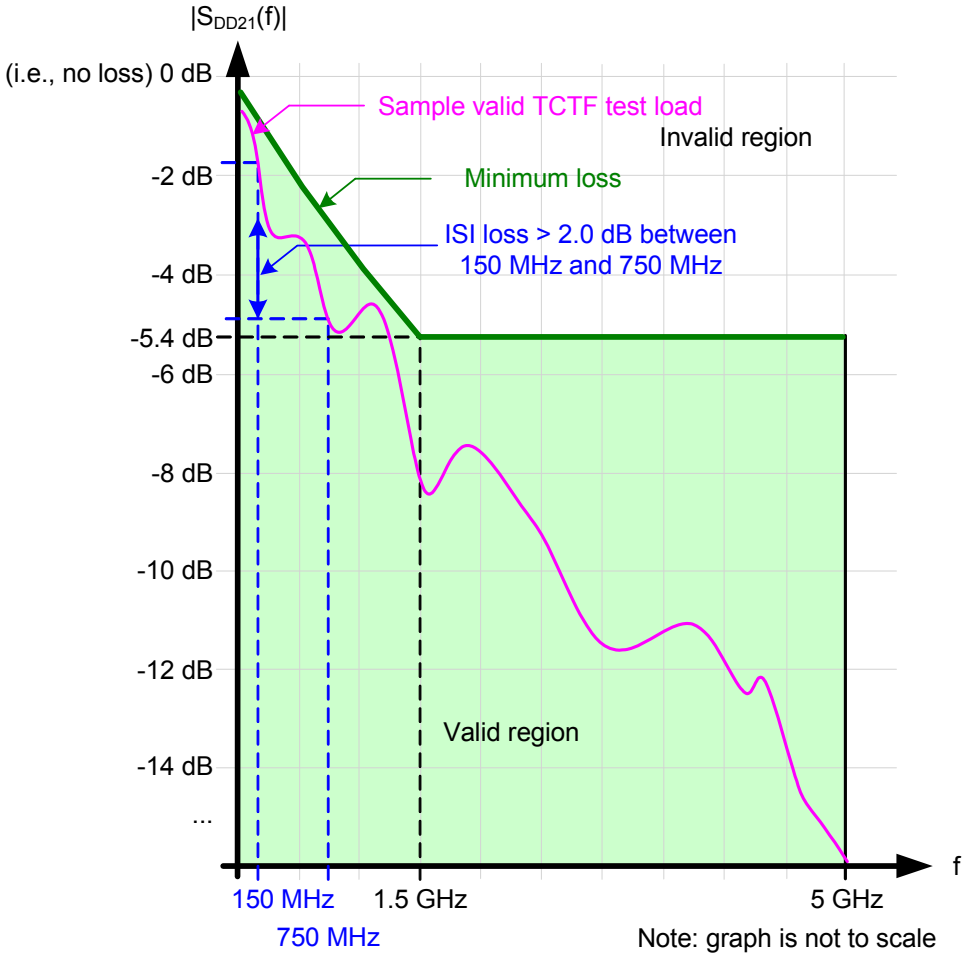


Figure 126 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 1.5 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log(e) \times ((1.7 \times 10^{-5} \times \sqrt{f}) + (1.0 \times 10^{-10} \times f))\text{dB}$$

and for 1.5 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq$ -7.0 dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 150\text{ MHz})| - |S_{DD21}(f = 750\text{ MHz})| >$ 2.0 dB

where:

$|S_{DD21}(f)|$ is the magnitude of $S_{DD21}(f)$; and

f is the signal frequency in Hz.

Figure 127 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 1.5 Gbit/s.

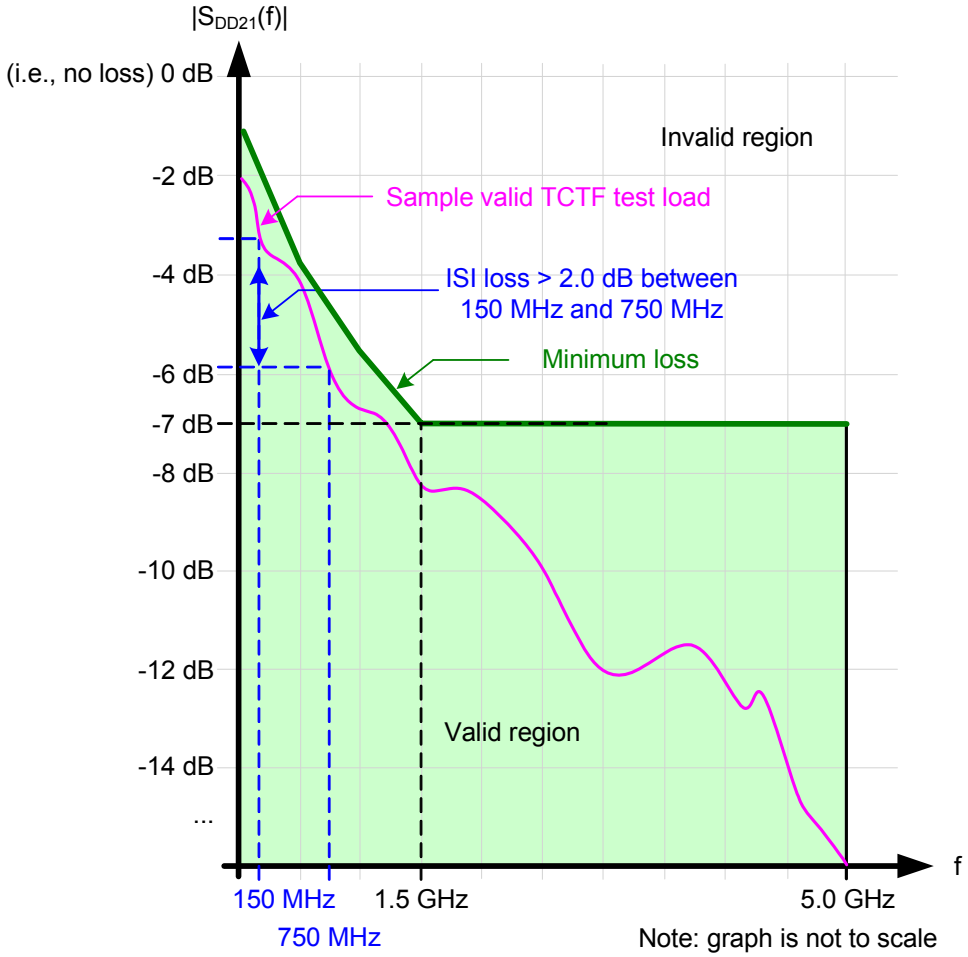


Figure 127 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 1.5 Gbit/s

5.6.4 Low-loss TCTF test load

Figure 128 shows the low-loss TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

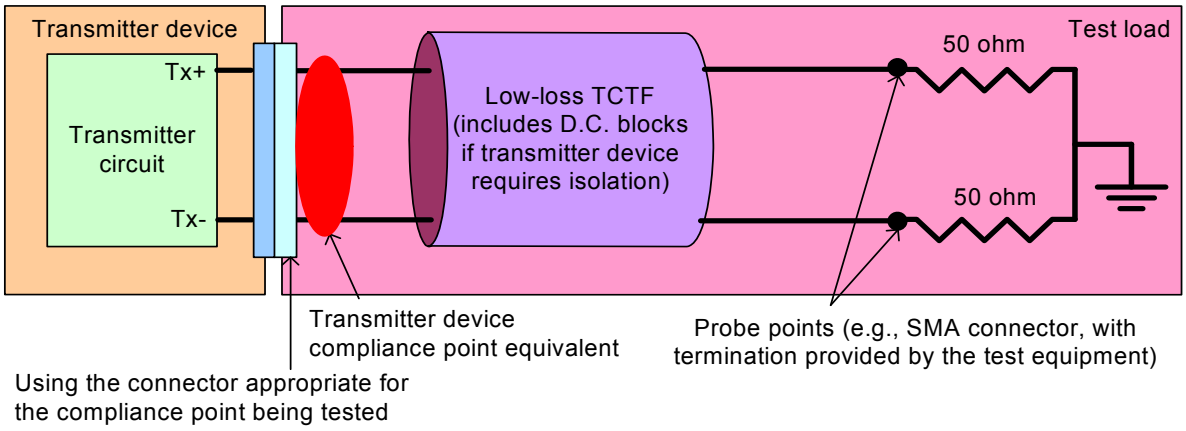


Figure 128 — Low-loss TCTF test load

The low-loss TCTF test load shall meet the requirements defined in 5.5.2. The nominal impedance shall be the target impedance.

The low-loss TCTF test load is defined by a set of S-parameters (see F.11). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

The low-loss TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$\left|S_{DD21}(f)\right| \leq -20 \times \log(e) \times ((2.2 \times 10^{-6} \times \sqrt{f}) + (6.9 \times 10^{-11} \times f) + (1.1 \times 10^{-20} \times f^2))\text{dB}$$

for 3.0 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq$ -3.7 dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 300\text{ MHz})| - |S_{DD21}(f = 1\,500\text{ MHz})| >$ 1.3 dB

where:

$|S_{DD21}(f)|$ is the magnitude of $S_{DD21}(f)$; and

f is the signal frequency in Hz.

Figure 129 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a low-loss TCTF test load and the $|S_{DD21}(f)|$ of a sample low-loss TCTF test load.

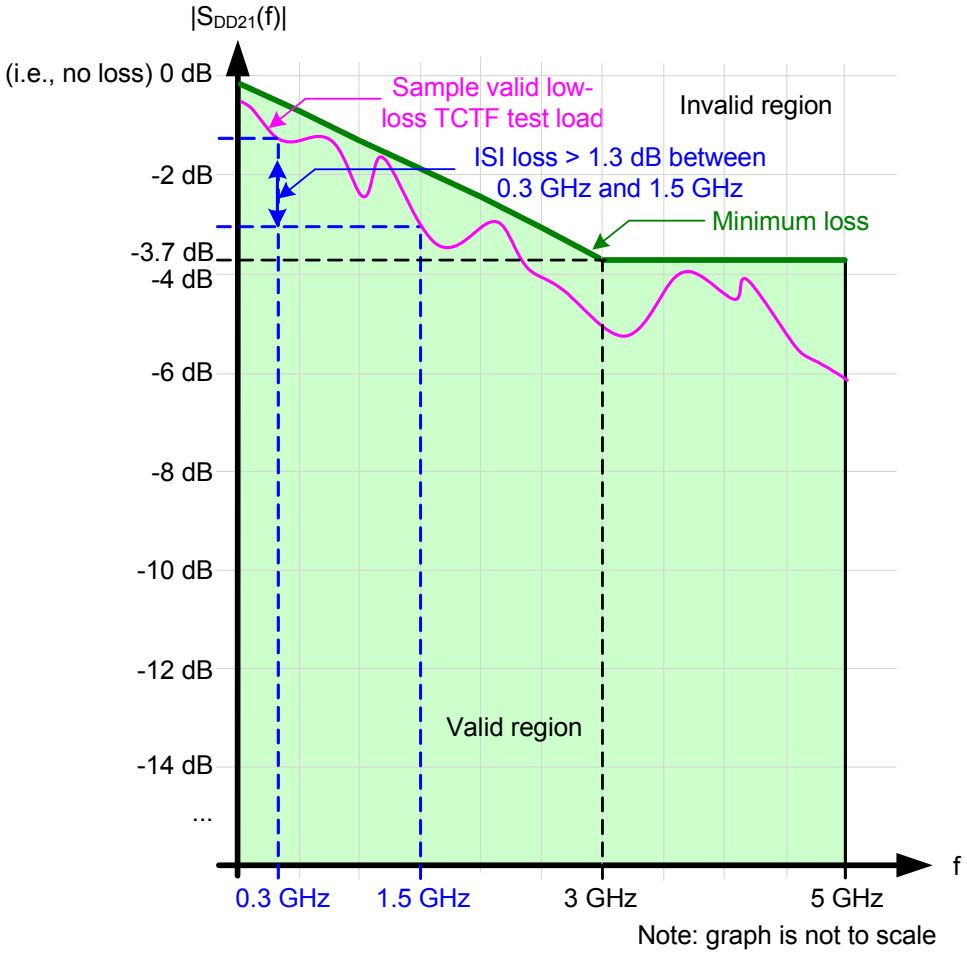


Figure 129 — Low-loss TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements

5.6.5 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load

The reference transmitter test load for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is a set of parameters defining the electrical performance characteristics of a 10 m Mini SAS 4x cable assembly, used:

a) in simulation to determine compliance of a transmitter device (see 5.8.4.6); and
b) as a representative component of an ISI generator used to determine compliance of a receiver device (see 5.8.5.7.6).

The following Touchstone model of the reference transmitter test load is included with this standard:

a) SAS2_transmittertestload.s4p.

See Annex G for a description of how the Touchstone model was created.

Figure 130 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

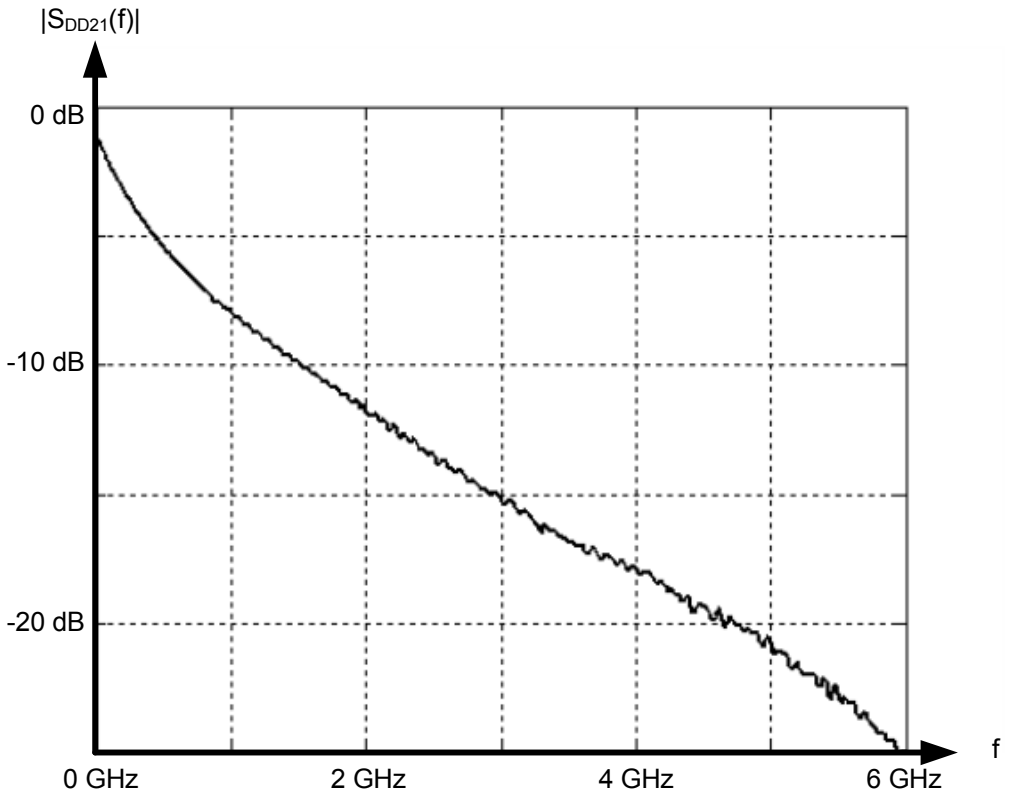


Figure 130 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz

Figure 131 shows the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load pulse response.

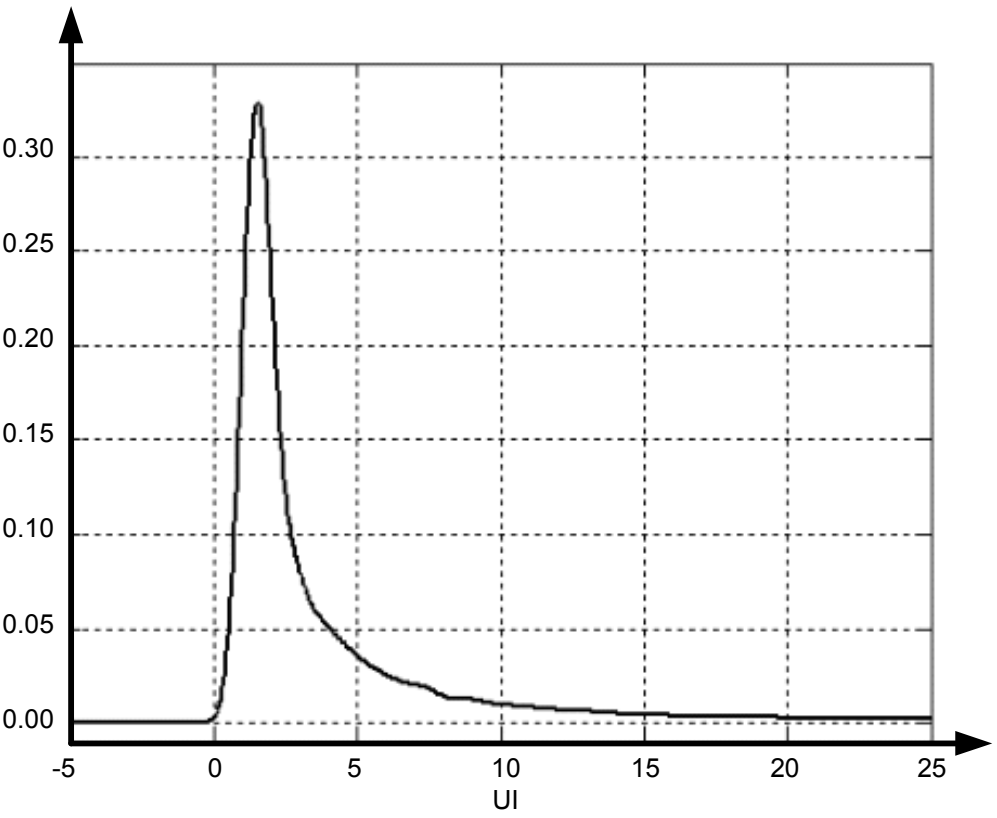


Figure 131 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load pulse response

The following impulse response model of the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load is included with this standard:

a) sas2_stressor_6g0_16x.txt.

Figure 132 shows the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load impulse response found in the sas2_stressor_6g0_16x.txt.

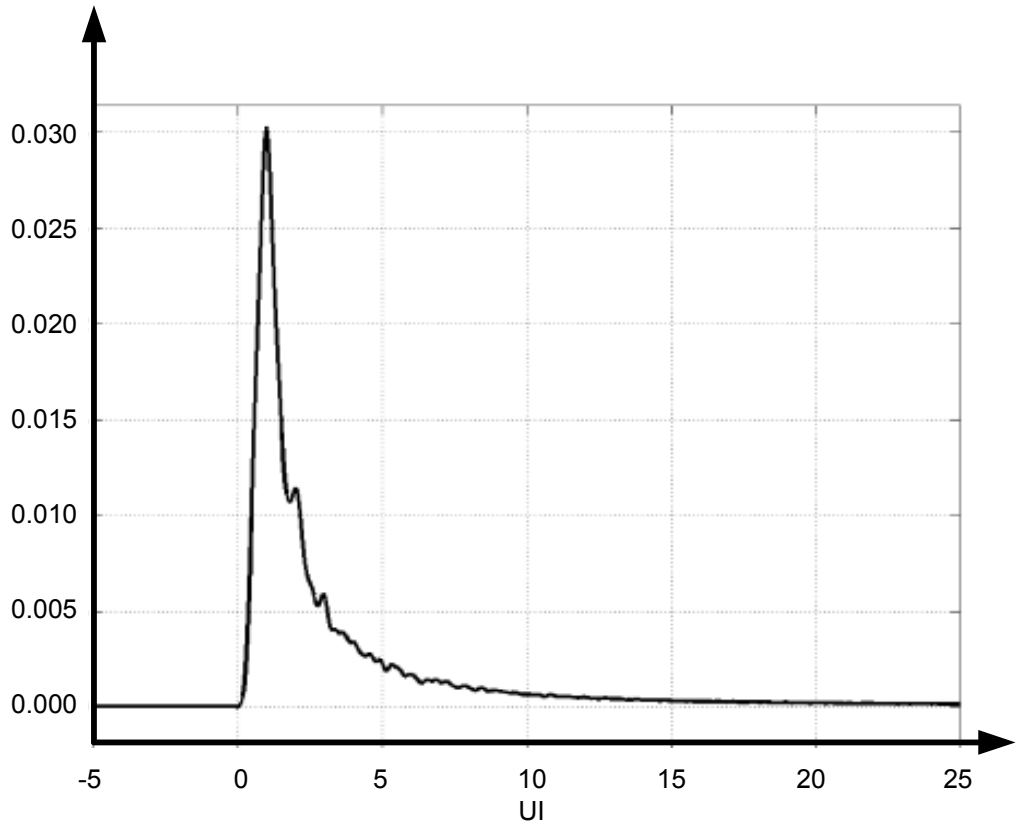


Figure 132 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load impulse response for 6 Gbit/s

Figure 133 shows the trained 1.5 Gbit/s, 3 Gbit/s, an 6 Gbit/s reference transmitter test load repeating 0011b pattern or 1100b pattern (e.g., D24.3) response.

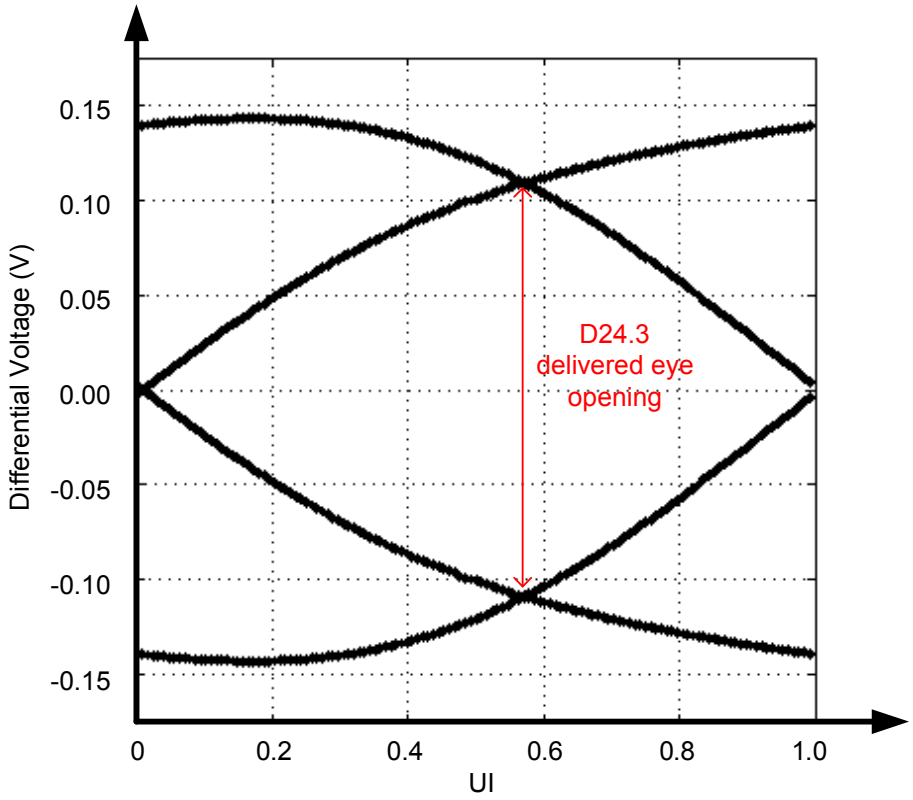


Figure 133 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load D24.3 response

5.7 End to end simulation for trained 12 Gbit/s

5.7.1 End to end simulation for trained 12 Gbit/s overview

End to end simulation shall be used to verify characteristics of:

a) transmitter devices connected to passive TxRx connections (see 5.8.4.7.4);
b) passive TxRx connections (see 5.5.6); and
c) ISI generators providing the stressed receiver signal input for receiver devices connected to passive TxRx connections (see 5.8.5.7.6.6).

The specific end to end simulation procedures defined in 5.8.4.7.4, 5.5.6, and 5.8.5.7.6.6 follow this sequence:

1) capture the signal from a transmitter device with no equalization and without SSC into a zero-length test load or model the transmitter using the reference transmitter (see 5.8.4.7.3);
2) connect passive TxRx connection segments, crosstalk, reference transmitter, and reference receiver according to the reference end to end simulation diagram (see 5.7.2 and C.2);
3) in the simulator, set the transmitter reference equalization (see 5.7.3 and figure 164) and set the receiver reference DFE equalization (see 5.8.5.7.3); and
4) perform a linear simulation, including the effects of edge rates, ISI, and crosstalk (see C.1).

The end to end simulation uses a reference transmitter with RJ and TJ set to zero. RJ and TJ and non-linear behavior present in the captured signal used for simulation are removed by the simulation process. Margins for these effects are provided in the required simulation characteristics. The simulation characteristics are processed at a BER of 10^{-15}.

Crosstalk transmitters are simulated using reference transmitters. These reference transmitters shall be set to the characteristics of table C.1. The crosstalk transmitters shall be asynchronous to the data sent to the channel under test.

Characteristics are measured from the simulation at specified measurement points for the usage model and characterization type (see table 53, table 32, and table 68).

5.7.2 Usage models for end to end simulation for trained 12 Gbit/s

A set of transfer functions is required to complement the measured S-parameter or captured signal to provide an end to end simulation model. C.2 describes the different S-parameter files that shall be used for each usage model, with their associated measurement points.

Each transmitter device, receiver device, or passive TxRx connection segment shall be simulated with the appropriate usage model (see C.2).

The S-parameter files provided in SAS3.zip use the port mapping of F.11.3. The FEXT S-parameters and NEXT S-parameters are extracted as shown in figure 134.

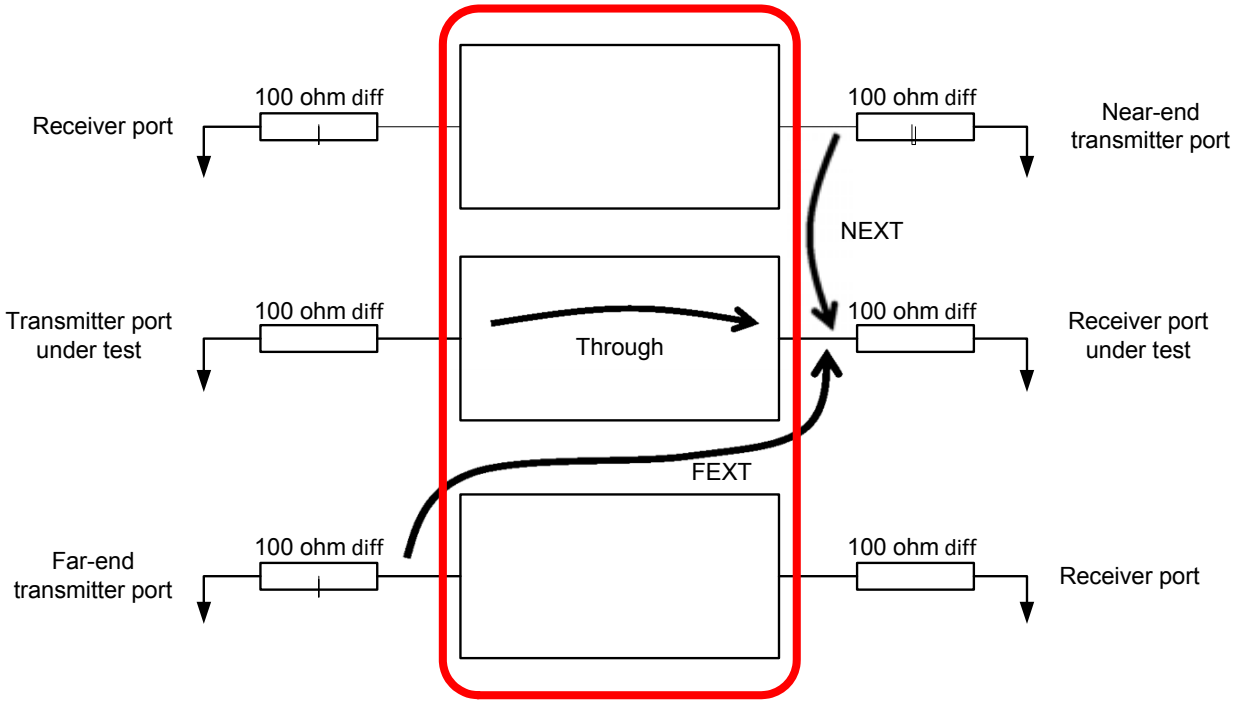


Figure 134 — NEXT and FEXT measurement definition

See Annex C for a description of the procedure that shall be used for end to end simulations. See E.1 for additional information regarding the S-parameter for 12 Gbit/s simulations.

5.7.3 Reference transmitter equalization for trained 12 Gbit/s

The reference transmitter equalization shall be calculated using the procedure described in this subclause, which requires the unequalized pulse response of the TxRx connection between ET and the input of the reference receiver (i.e., RR) (see C.2). Extraction of pulse responses from captured signals or transfer functions is beyond the scope of this standard, however, an example is provided in SAS3_EYEOPENING (see SAS3.zip).

The reference transmitter equalization procedure is as follows:

1) compute the reference sampling instant from the un-equalized pulse response between ET and RR (see figure 135);
2) set coefficient 2 (i.e., C2) of a reference transmitter to one and K_0 to one;
3) provide the un-equalized pulse response between ET and RR as the input of the reference transmitter, and compute the coefficient 1 (i.e., C1) and coefficient 3 (i.e., C3) that result in a pulse response with the smallest sum of squared error to an ideal pulse, at instants separated from the reference sampling instant by integer multiples of a one UI period (see figure 136);
4) calculate an equalized pulse response by convolving the coefficients obtained in steps (2) and (3) with the un-equalized pulse response between ET and RR;
5) calculate the reference sampling instant from the equalized pulse response;
6) repeat steps (2) through (5) until the coefficients and sampling point converge (see figure 137); and
7) normalize the final coefficients found in steps (3) and (4) by dividing them by (|C1| + |C3| + 1).

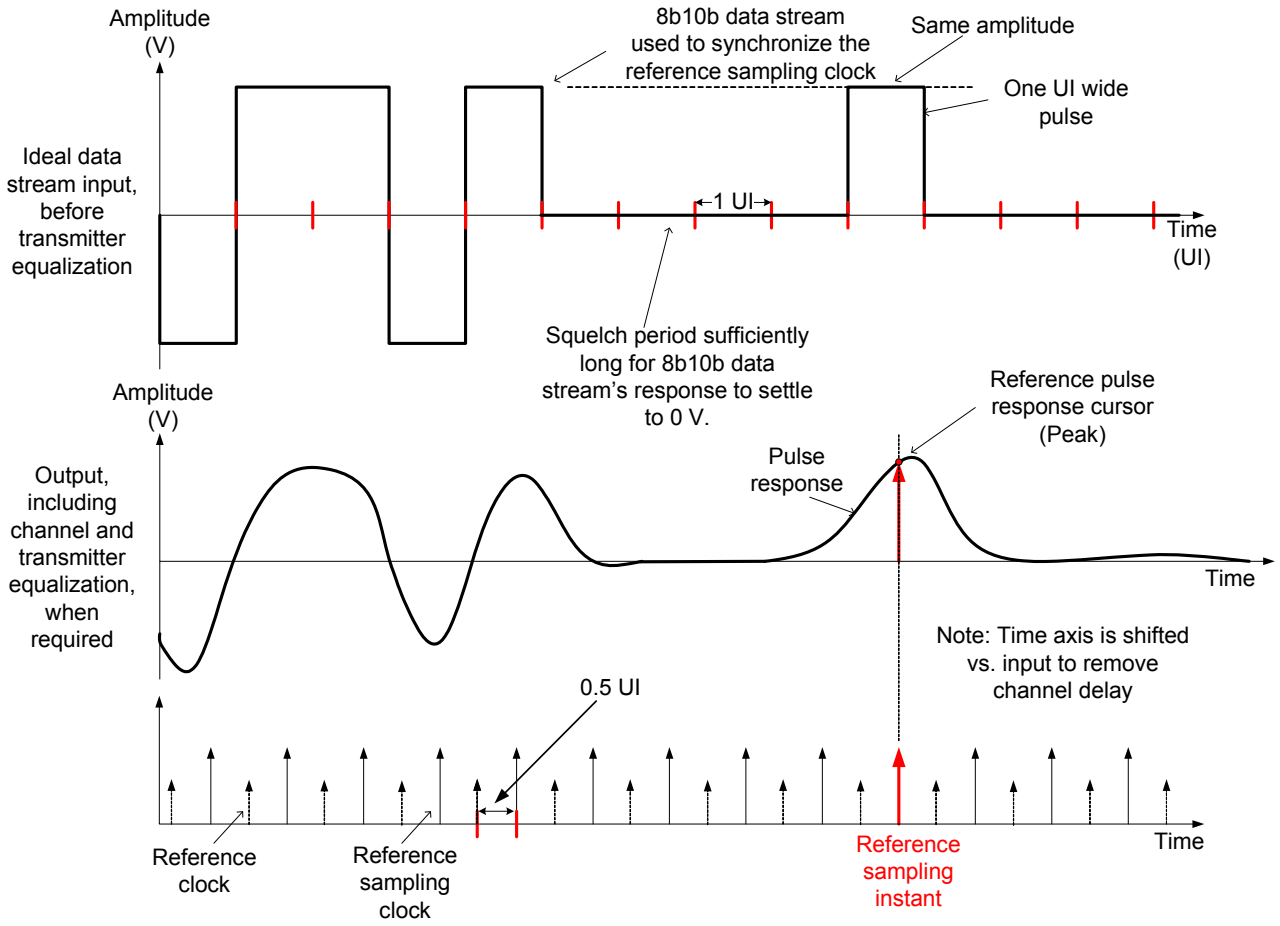


Figure 135 — Reference sampling point and reference pulse response cursor

Figure 136 shows the computations of step 3). A one UI spaced filter of coefficients [C1, C2 = 1, C3] is convolved with the extracted end to end pulse response. Coefficient 1 and coefficient 3 are computed to produce an equalized pulse response that has the smallest sum of squared errors at the sampling instants defined by a reference sampling clock.

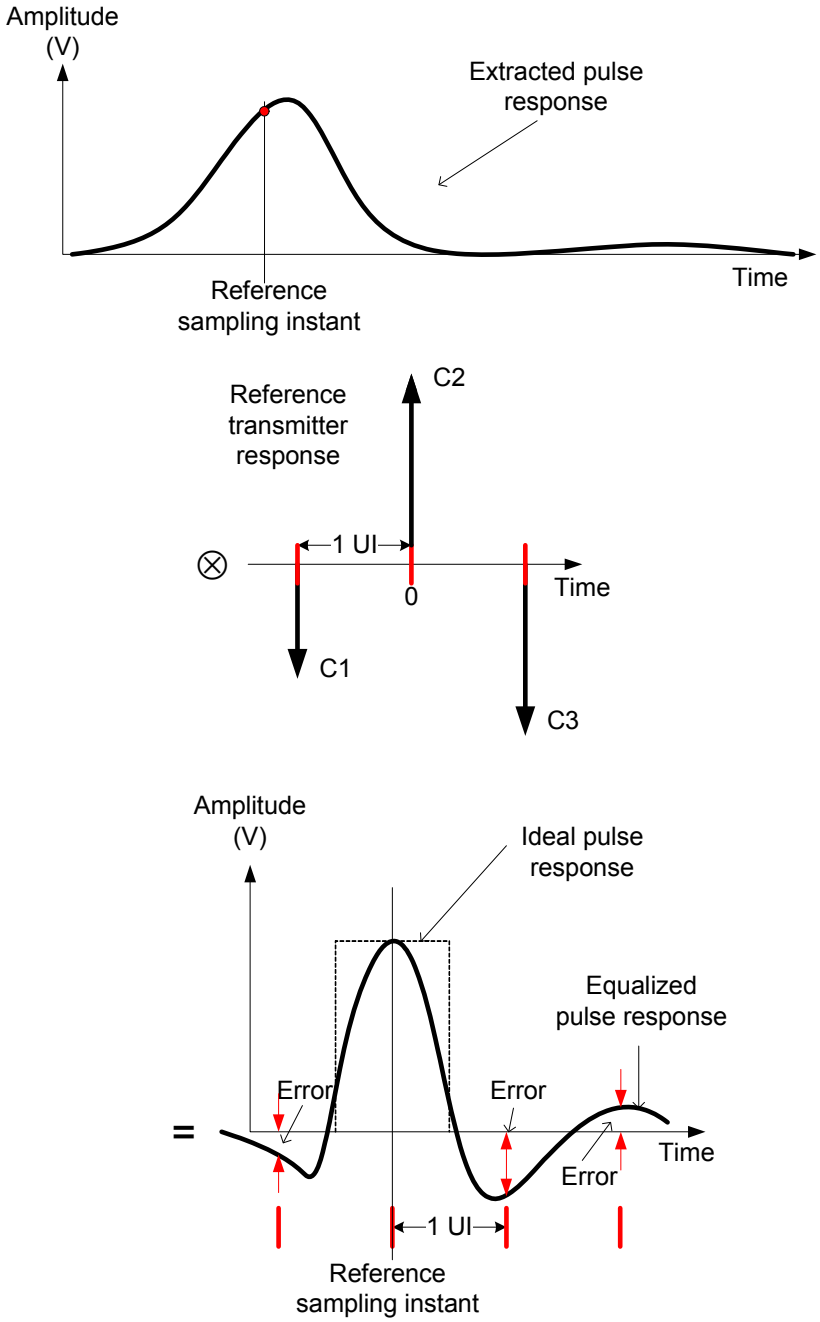


Figure 136 — Reference transmitter coefficient error computation

The reference sampling instant is computed from:

1) the un-equalized pulse response from ET to RR, for the first iteration; and
2) the equalized pulse response using transmitter coefficients from the previous iteration, for other iterations.

The reference sampling instant changes when the coefficients from the current iteration are used to compute the equalized pulse response. As shown in figure 137, the process of calculating C1 and C3 is repeated with the reference sampling instant computed from the last equalized pulse response, until the coefficients and reference sampling instant converge to stable values.

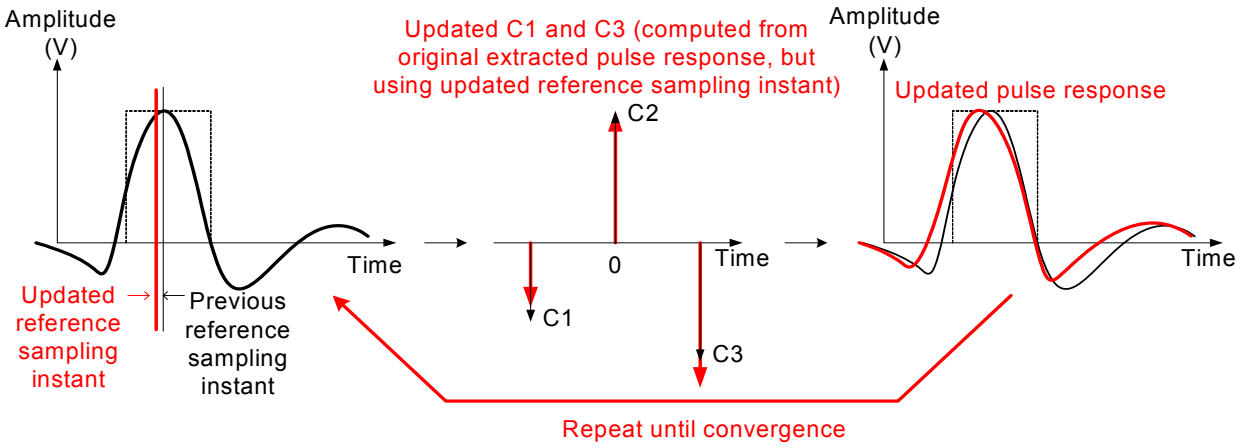


Figure 137 — Convergence of reference transmitter equalization

If either coefficient 1 (i.e., C1) or coefficient 3 (i.e., C3) takes a positive value during this procedure, its value is forced to zero and only the other coefficient is computed. The procedure stops if both coefficients need to be forced to zero.

5.7.4 Crosstalk measurement for end to end simulations and 12 Gbit/s jitter tolerance

End to end channel simulation shall include crosstalk. Crosstalk shall be measured using:

a) crosstalk transfer functions (e.g., S-parameters, see F.11); or
b) total peak to peak crosstalk measurement.

The following procedure shall be used to measure total peak to peak crosstalk:

1) calculate the reference transmitter equalization for the TxRx connection segment under test (see 5.7.3);
2) terminate the TxRx connection segment under test on the transmitter end;
3) connect 12 Gbit/s transmitters to the source of all or a subset of crosstalk channels;
4) set the crosstalk transmitters to transmit asynchronous IDLE dwords (see SPL-4) using the characteristics in table C.1;
5) measure the asynchronous amplitude histogram at the end of the TxRx connection segment under test, into a zero-length test load, with an acquisition bandwidth of at least 9 GHz, and a capture of at least 2 x 10^7 UI;
6) repeat steps (2) through (4) until all crosstalk sources have been measured;
7) when multiple measurements are made, convolve the histograms to obtain the total crosstalk histogram; and
8) from the total crosstalk histogram evaluate the crosstalk amplitude that is met or exceeded at a cumulative probability of 10^{-6} using the following procedure:
    1) separate positive samples from negative samples, ensuring at least 10^7 samples are collected for each type;
    2) calculate the vertical histogram for the positive samples;
    3) from the histogram, compute the crosstalk voltage that is met or exceeded at a probability of 10^{-6};
    4) calculate the vertical histogram for the opposite of the negative samples (i.e., zero minus the samples);
    5) from the histogram, calculate the crosstalk voltage that is met or exceeded at a probability of 10^{-6}; and
    6) sum the peak crosstalk voltages calculated in steps (3) and (5).

To provide a variety of pattern combinations for the crosstalk measurement, the digital IDLE dwords should be aligned differently one crosstalk channel to another and the transmission frequencies of the crosstalk transmitters should be different one from another.

The channel under test shall be terminated with the characteristics of the transmitter device termination (see table 39) on the transmitter end. The termination should be implemented using:

a) a high-bandwidth termination having impedance close to the nominal differential impedance (see table 29), for TxRx connection segments; or
b) a transmitter device set to transmit D.C. idle while maintaining the characteristics of table 39 for transmitter circuits and ISI generators.

Active circuits create noise when transmitting signals, including D.C. idle. By measuring the crosstalk with active circuits connected, the crosstalk value reported includes this noise. This is representative of the noise generated when the active circuit is transmitting data. When multiple crosstalk measurements are performed, this noise may however be overestimated in the final crosstalk amplitude calculation. Appropriate measurement techniques should be used to minimize these effects.

For transmitter device characterization, the crosstalk transmitters shall set coefficient 1 (i.e., C1) to zero, set coefficient 3 (i.e., C3) to zero, and set maximum peak to peak voltage.

For receiver ISI stress generators, the crosstalk is measured into a zero-length test load, and shall not include crosstalk from the receiver under test. A crosstalk generator channel should be selected to provide signal characteristics as close as possible to the required crosstalk signal characteristics (see table C.5), with the crosstalk generator characteristics defined by table C.1. Peak to peak voltage should then be adjusted to meet the required crosstalk characteristics.

5.8 Transmitter device and receiver device electrical characteristics

5.8.1 General electrical characteristics

Table 36 defines the general electrical characteristics, which apply to both transmitter devices and receiver devices.

Table 36 — General electrical characteristics

Characteristic	Units	1.5 Gbit/s (i.e., G1)	3 Gbit/s (i.e., G2)	6 Gbit/s (i.e., G3)	12 Gbit/s (i.e., G4)	22.5 Gbit/s (i.e., G5)
Physical link rate (nominal)	MBps	150	300	600	1 200	2 400
Unit interval (UI) (nominal) [a]	ps	$666.\overline{6}$	$333.\overline{3}$	$166.\overline{6}$	$83.\overline{3}$	$44.\overline{4}$
Baud rate (f_{baud}) (nominal)	Gigasymbols/s	1.5	3	6	12	22.5
Minimum A.C. coupling capacitor [b] [c]	nF	N/A				167
Maximum A.C. coupling capacitor [b] [c]	nF	12				265
Maximum noise during OOB idle time [d] [e]	mV(P-P)	120				

[a] $666.\overline{6}$ (i.e., 2 000 / 3), $333.\overline{3}$ (i.e., 1 000 / 3), $166.\overline{6}$ (i.e., 500 / 3), $83.\overline{3}$ (i.e., 250 / 3), and $44.\overline{4}$ (i.e., $133.\overline{3}$ / 3).

[b] The coupling capacitor value for A.C. coupled transmit and receive pairs. See 5.8.4.2 for coupling requirements for transmitter devices. See 5.8.5.2 for coupling requirements for receiver devices. The equivalent series resistance at 3 GHz should be less than 1 Ω.

[c] The G5 coupling capacitor value may be used at rates of 1.5 Gbt/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s when 22.5 Gbit/s is supported.

[d] With a measurement bandwidth of 1.5 × f_{baud} (e.g., 18 GHz for 12 Gbit/s), no signal level during the idle time shall exceed the specified maximum differential amplitude.

[e] This is not applicable when optical mode is enabled.

5.8.2 Transmitter device and receiver device transients

Transients may occur at transmitter devices or receiver devices as a result of changes in supply power conditions or mode transitions.

A mode transition is an event that may result in a measurable transient due to the response of the transmitter device or receiver device. The following conditions constitute a mode transition:

a) enabling or disabling driver circuitry;
b) enabling or disabling receiver common mode circuitry;
c) hot plug event;
d) adjusting driver amplitude;
e) enabling or disabling de-emphasis; and
f) adjusting terminator impedance.

Transmitter device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 138 during all power state and mode transitions. Receiver device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 139 during all power state and mode transitions. Test conditions shall include power supply power on and power off conditions, voltage sequencing, and mode transitions.

Figure 138 shows the test circuit attached to IT or CT to test transmitter device transients.

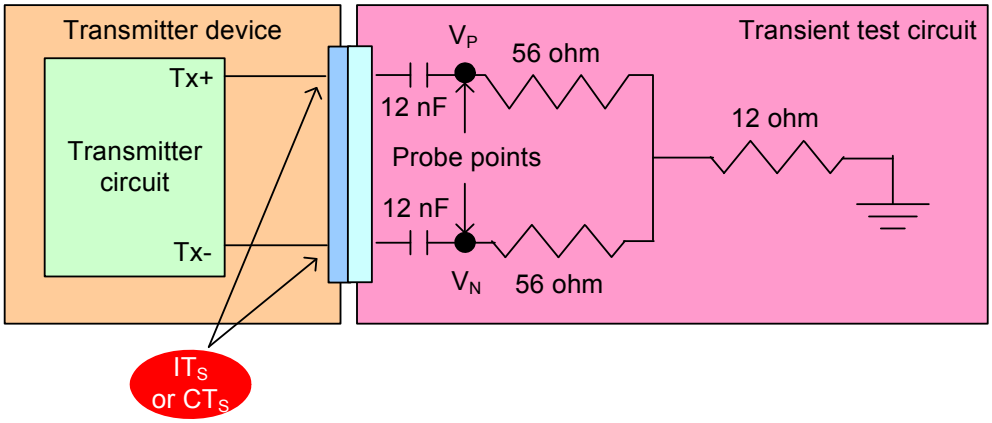


Figure 138 — Transmitter device transient test circuit

Figure 139 shows the test circuit attached to IR or CR to test receiver device transients.

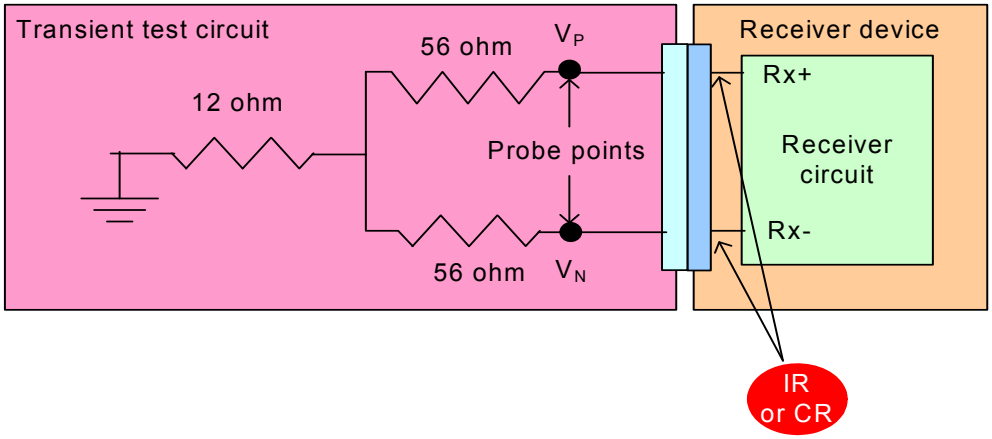


Figure 139 — Receiver device transient test circuit

5.8.3 Eye masks and the JTF

5.8.3.1 Eye masks overview

The eye masks shown in 5.8.3 shall be interpreted as graphical representations of the voltage and time limits of the signal. The eye mask boundaries define the eye contour of:

a) the 10^{-12} jitter population for untrained 1.5 Gbit/s and 3 Gbit/s measured eyes; and
b) the 10^{-15} jitter population for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s simulated eyes.

For untrained 1.5 Gbit/s and 3 Gbit/s, equivalent time sampling oscilloscope technology is not practical for measuring compliance to the eye masks. See MJSQ for methods that are suitable for verifying compliance to these eye masks.

CJTPAT (see Annex A) shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and provides information regarding special considerations for running disparity (see SPL-4) and scrambling (see SPL-4).

5.8.3.2 JTF

With the possible presence of SSC, the application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667) as specified in SAS-1.1 does not separate the SSC component from the actual jitter and thus may overstate the transmitter device jitter. To differentiate between allowable timing variation due to SSC and jitter, the frequency-weighting JTF shall be applied to the signal at the compliance point when determining the eye mask.

The jitter measurement device shall comply with the JTF. The reference clock characteristics are controlled by the resulting JTF characteristics obtained by taking the time difference between the PLL output (i.e., the reference clock) and the data stream sourced to the PLL. The PLL's closed loop transfer function's -3 dB corner frequency and other adjustable parameters (e.g., peaking) are determined by the value required to meet the requirements of the JTF.

The JTF shall have the characteristics specified in table 37 for a repeating 0011b pattern or 1100b pattern (e.g., D24.3). See the phy test patterns in the Protocol Specific diagnostic page in SPL-4.

The JTF -3 dB corner frequency and the magnitude peaking requirements shall be measured with SJ applied, with a peak to peak amplitude of 0.3 UI, with a relative tolerance of ± 10 %. The relative attenuation at 30 kHz shall be measured with sinusoidal phase (i.e., time) modulation applied, with a peak to peak amplitude of 20.8 ns with a relative tolerance of ± 10 %. See Annex F for the calibration procedure.

A proportional decrease of the JTF -3 dB corner frequency should be observed for a decrease in pattern transition density compared to a 0.5 transition density. If a JMD shifts the JTF -3 dB corner frequency in a manner that does not match this characteristic, or does not shift at all, then measurements of jitter with patterns with transition densities different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3 dB corner frequency that is closest to the proportional characteristic of the reference transmitter test load (see 5.6.5) shall be considered correct. This characteristic may be measured with the conditions defined above for measuring the -3 dB corner frequency but substituting other patterns with different transition densities.

Table 37 — JTF parameters

Characteristic	Without SSC support					With SSC support				
	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s	22.5 Gbit/s	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s	22.5 Gbit/s
JTF -3 dB point (kHz) [a] [b]	900 ± 500	1 800 ± 500	3 600 ± 500	3 600 ± 500	3 600 ± 500	1 300 ± 500	1 838 ± 500	2 600 ± 500	2 600 ± 500	2 600 ± 500
JTF slope (dB/decade)	20	20	20	20	20	40	40	40	40	40
Attenuation at 30 kHz ± 1 % (dB) [c]	N/A	N/A	N/A	N/A	N/A	61.5 ± 1.5	67.5 ± 1.5	73.5 ± 1.5	73.5 ± 1.5	73.5 ± 1.5
Maximum Peaking (dB)	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5

Key:

N/A = not applicable

[a] For untrained or trained without SSC support this value equals f_{baud}/1 667 ± 500 kHz for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s and 22.5 Gbit/s use the value for 6 Gbit/s.

[b] For untrained or trained with SSC support this value equals $(f_{baud})^{0.5}$ x 33.566 x $Hz^{0.5}$ ± 500 kHz for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s and 22.5 Gbit/s use the value for 6 Gbit/s.

[c] For untrained or trained with SSC support this value equals 73.5 dB + [20 x log(f_{baud} / 6 x 10^9 Hz)] dB ± 1.5 dB for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s and 22.5 Gbit/s use the value for 6 Gbit/s.

[d] For the above equations, f_{baud} is expressed in Hz (i.e., 1.5 GHz for 1.5 Gbit/s, 3.0 GHz for 3 Gbit/s, and 6.0 GHz for 6 Gbit/s). 12 Gbit/s and 22.5 Gbit/s use the value for 6 Gbit/s.

5.8.3.3 Transmitter device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 140 describes the eye mask used for testing the signal output of the transmitter device at IT and CT for untrained 1.5 Gbit/s and 3 Gbit/s (see table 41 in 5.8.4.5) and OOB signals (see table 55 in 5.8.4.8). This eye mask applies to jitter after the application of the JTF (see 5.8.3.2).

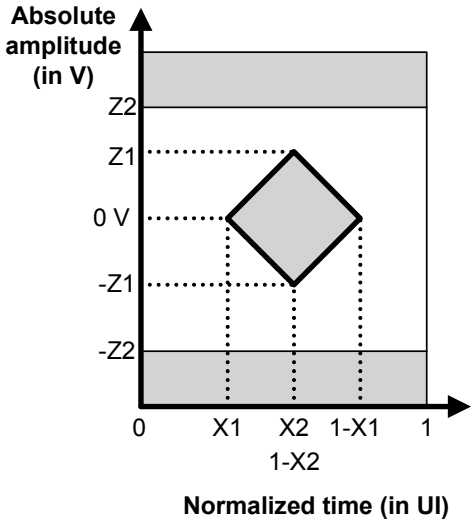


Figure 140 — Transmitter device eye mask

Verifying compliance with the limits represented by the transmitter device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.8.3.4 Receiver device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 141 describes the eye mask used for testing the signal delivered to the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 59 in 5.8.5.4). This eye mask applies to jitter after the application of the JTF (see 5.8.3.2). This requirement accounts for the low frequency tracking properties and response time of the CDR circuitry in receiver devices.

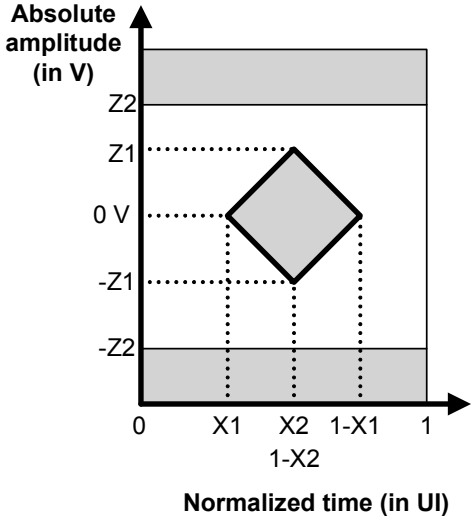


Figure 141 — Receiver device eye mask

Verifying compliance with the limits represented by the receiver device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.8.3.5 Receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 142 describes the eye mask used to test the jitter tolerance of the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 59 in 5.8.5.4). For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, jitter tolerance is included in the delivered signal specifications for stressed receiver device jitter tolerance testing (see 5.8.5.7.6).

The eye mask shall be constructed as follows:

a) X2 and Z2 shall be the values for the delivered signal listed in table 59 (see 5.8.5.4);
b) $X1_{OP}$ shall be half the value of TJ for maximum delivered jitter listed in table 60 (see 5.8.5.5); and
c) $X1_{TOL}$ shall be half the value of TJ for receiver device jitter tolerance listed in table 61 (see 5.8.5.6), for applied SJ frequencies above (f_{baud} / 1 667).

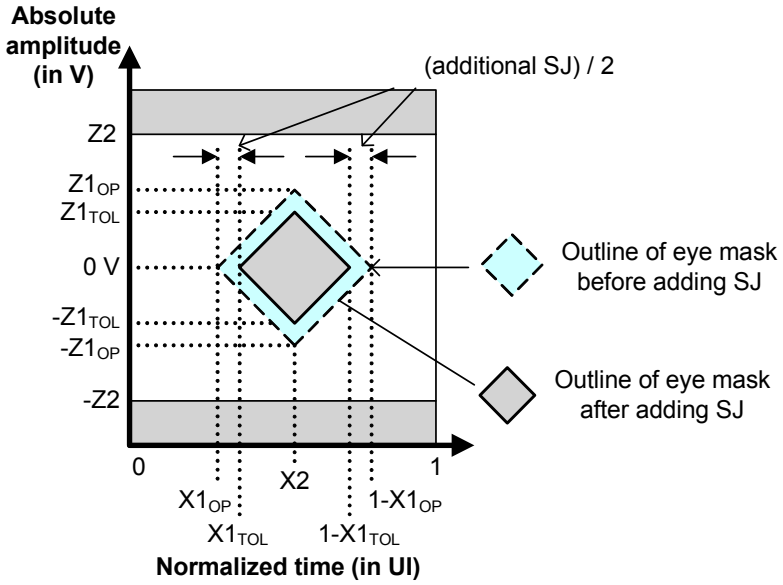


Figure 142 — Deriving a receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

The leading and trailing edge slopes of the receiver device eye mask in figure 141 (see 5.8.3.4) shall be preserved. As a result, the amplitude value of Z1 is less than that given for the delivered signal in table 59 (see 5.8.5.4), and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2 - \left(\frac{ASJ}{2}\right) - X1_{OP}}{X2 - X1_{OP}}$$

where:

$Z1_{TOL}$	is the value for Z1 to be used for the receiver device jitter tolerance eye mask;
$Z1_{OP}$	is the Z1 value for the delivered signal in table 59;
$X1_{OP}$	is the X1 value for the delivered signal in table 59;
X2	is the X2 value for the delivered signal in table 59; and
ASJ	is the additional SJ for applied SJ frequencies above (f_{baud} / 1 667) (see figure 156 in 5.8.5.6).

The X1 points in the receiver device jitter tolerance eye mask (see figure 142) are greater than the X1 points in the receiver device eye mask (see figure 141) due to the addition of SJ.

5.8.4 Transmitter device characteristics

5.8.4.1 Transmitter device characteristics overview

Transmitter devices operating at 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s may or may not incorporate de-emphasis (i.e., pre-emphasis) and other forms of compensation. The transmitter device operating at 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s shall use the same settings (e.g., de-emphasis and voltage swing) with both the zero-length test load and the appropriate TCTF test load or reference transmitter test load (see 5.6). Transmitter devices operating at 6 Gbit/s should use the transmitter equalization settings provided in table 45. Transmitter devices operating at 12 Gbit/s and 22.5 Gbit/s shall support transmitter training (see SPL-4) unless the transmitter device is operating in the optical mode.

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

See F.7 for a methodology for measuring transmitter device signal output.

5.8.4.2 Transmitter device coupling requirements

Coupling requirements for transmitter devices are as follows:

a) transmitter devices using inter-enclosure TxRx connections (i.e., attached to CT compliance points) should be D.C. coupled, however, may be A.C. coupled to the interconnect through a transmission network; or
b) transmitter devices using intra-enclosure TxRx connections (i.e., attached to IT compliance points) should be D.C. coupled, however, may be A.C. coupled.

If the transmitter device is attached to an IT compliance point supporting SATA, then the coupling requirements of Gen1i devices (see SATA) should be considered regarding its impact to the implementation.

If the transmitter device is attached to an IT compliance point supporting a PCIe SFF-8639 Module, then the coupling requirements of PCIe devices (see PCIe) should be considered regarding its impact to the implementation.

See table 36 (see 5.8.1) for the coupling capacitor value.

5.8.4.3 Transmitter device general electrical characteristics

Table 38 defines the transmitter device general electrical characteristics.

Table 38 — Transmitter device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s	22.5 Gbit/s
Physical link rate accuracy [a] at IT and CT	ppm	± 100				
Physical link rate SSC modulation at IT and CT	ppm	See table 73, table 74, and table 75 in 5.8.6				
Maximum transmitter device transients [b]	V	± 1.2				

[a] Physical link rate accuracy shall be measured over a minimum of 1 x 10^6 UI and should be measured using a minimum resolution of 100 Hz.
[b] See 5.8.2 for transient test circuits and conditions.

Table 39 defines the transmitter device termination characteristics.

Table 39 — Transmitter device termination characteristics

Characteristic	Units	Untrained 1.5 Gbit/s and 3 Gbit/s	Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s	Trained 12 Gbit/s	Trained 22.5 Gbit/s
Differential impedance [a]	Ω	60 minimum 115 maximum	See 5.8.4.6.1	See 5.8.4.7.1	tbd
Maximum differential impedance imbalance [a] [b]	Ω	5	See 5.8.4.6.3 [c]	See 5.8.4.7.2 [c]	tbd
Common mode impedance [b]	Ω	15 minimum 40 maximum	See 5.8.4.6.1	See 5.8.4.7.1	tbd

[a] All transmitter device termination measurements are made through mated connector pairs.
[b] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.
[c] Measurement replaced by S_{CD22} specifications (i.e., differential to common mode conversion).

5.8.4.4 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load

Table 40 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load (see 5.6.2) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.8.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 40 — Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load at IT and CT

Signal characteristic [a]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Maximum intra-pair skew [b]	ps	20	15
Maximum transmitter device off voltage [c] [d]	mV(P-P)	50	
Maximum (i.e., slowest) rise/fall time [e]	ps	273	137
Minimum (i.e., fastest) rise/fall time [e]	ps	41.6	
Maximum transmitter output imbalance [f]	%	10	

[a] All tests in this table shall be performed with zero-length test load (see 5.6.2).

[b] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the TX+ and TX- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the TX+ signal and the TX- signal.

[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[d] This is not applicable when optical mode is enabled.

[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link.

[f] The maximum difference between the V+ and V- A.C. rms transmitter device amplitudes measured with CJTPAT (see Annex A) into the zero-length test load shown in figure 120 (see 5.6.2), as a percentage of the average of the V+ and V- A.C. rms amplitudes.

5.8.4.5 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load

Table 41 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load (i.e., the zero-length test load (see 5.6.2) and either the TCTF test load (see 5.6.3) or the low-loss TCTF test load (see 5.6.4)) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.8.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 41 — Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load at IT and CT

Signal characteristic	Units	IT, untrained		CT, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 140) if SATA is not supported	mV(P-P)	1 200			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 140) if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 140), if SATA is not supported	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 140), if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Maximum DJ [b c d]	UI	0.35			
Maximum half of TJ (i.e., X1 in figure 140) [b c d e f g h]	UI	0.275			
Center of bit time (i.e., X2 in figure 140)	UI	0.50			
Maximum intra-pair skew [i]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] All DJ and TJ values are level 1 (see MJSQ).

[c] The values for jitter in this table are measured at the average signal amplitude point.

[d] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.

[e] TJ is specified at a CDF level of 10^{-12}.

[f] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.

Jitter peak to peak measured < (maximum TJ - |asymmetry|).

[g] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability, direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[h] The value for X1 is also half the value of TJ for maximum delivered jitter listed in table 60 (see 5.8.5.5). The test or analysis shall include the effects of the JTF (see 5.8.3.2).

[i] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the TX+ and TX- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the TX+ signal and the TX- signal at the probe points.

5.8.4.6 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.8.4.6.1 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s overview

Table 42 specifies the signal output characteristics for the transmitter device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s as measured with the zero-length test load (see 5.6.2), unless otherwise specified, attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements except for common mode measurements.

Table 42 — Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s at IT and CT

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage [b] [c]	mV(P-P)			50
Rise/fall time [d]	ps	41.6		
Reference differential impedance [e]	Ω		100	
Reference common mode impedance [e]	Ω		25	
Common mode voltage limit (rms) [f]	mV			30
RJ [g] [h]	UI			0.15 [i]
TJ [h] [j]	UI			0.25 [k]
WDP at 6 Gbit/s [l]	dB			13
WDP at 3 Gbit/s [l]	dB			7
WDP at 1.5 Gbit/s [l]	dB			4.5

[a] See 5.8.4.6.6 for the V_{P-P} measurement method.
[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[c] This is not applicable when optical mode is enabled.
[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link.
[e] See 5.8.4.6.3 for transmitter device S-parameters characteristics.
[f] This is a broadband limit. For additional limits on spectral content, see figure 143 and table 43.
[g] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.
[h] The measurement shall include the effects of the JTF (see 5.8.3.2).
[i] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[j] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.
[k] 0.25 UI is 41.6 ps at 6 Gbit/s, 83.3 ps at 3 Gbit/s, and 166.6 ps at 1.5 Gbit/s.
[l] See 5.8.4.6.2 for the transmitter device test procedure.

Table 43 defines the transmitter device common mode voltage limit characteristics.

Table 43 — Transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] (dBmV) [b]	N [a] (dBmV) [b] [c]	S [a] (dBmV/decade) [b]	f_{min} [a] (MHz)	f_{max} [a] (GHz)
Spectral limit of common mode voltage [d]	Figure 143	12.7	26.0	13.3	100	6.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 Ω (i.e., the reference impedance for common mode voltage) which is 20 × lg(158) = +44 dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at the Nyquist frequency (i.e., 3 GHz) (see figure 143).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 143 shows the transmitter device common mode voltage limit defined in table 43.

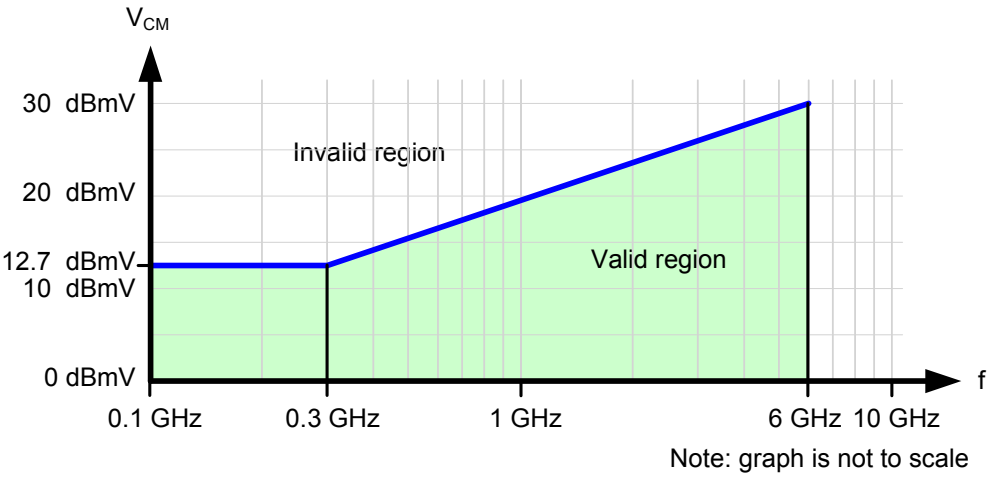


Figure 143 — Transmitter device common mode voltage limit

5.8.4.6.2 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device test procedure

The transmitter device test procedure is as follows:

1) attach the transmitter device to a zero-length test load, where its signal output is captured by an oscilloscope;
2) configure the transmitter device to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4);
3) configure the transmitter device to minimize DCD and BUJ;
4) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Use averaging to minimize RJ; and
5) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to ‘SAS2_TWDP’.

The WDP value is a characterization of the signal output within the reference receiver device (see 5.8.5.7.3) after equalization. WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5.8.4.6.3 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × lg(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 44 defines the maximum limits for S-parameters of the transmitter device.

Table 44 — Maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\|S_{CC22}\|$	-6.0	-5.0	-1.0	13.3	100	6.0
$\|S_{DD22}\|$	-10	-7.9	-3.9	13.3	100	6.0
$\|S_{CD22}\|$	-26	-12.7	-10	13.3	100	6.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). The amplitude applied by the test equipment shall be less than -4.4 dBm (i.e., 190 mV zero to peak) per port (see F.11.4.2).

[b] $|S_{DC22}|$ is not specified.

[c] See figure 4 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 144 shows the transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 44.

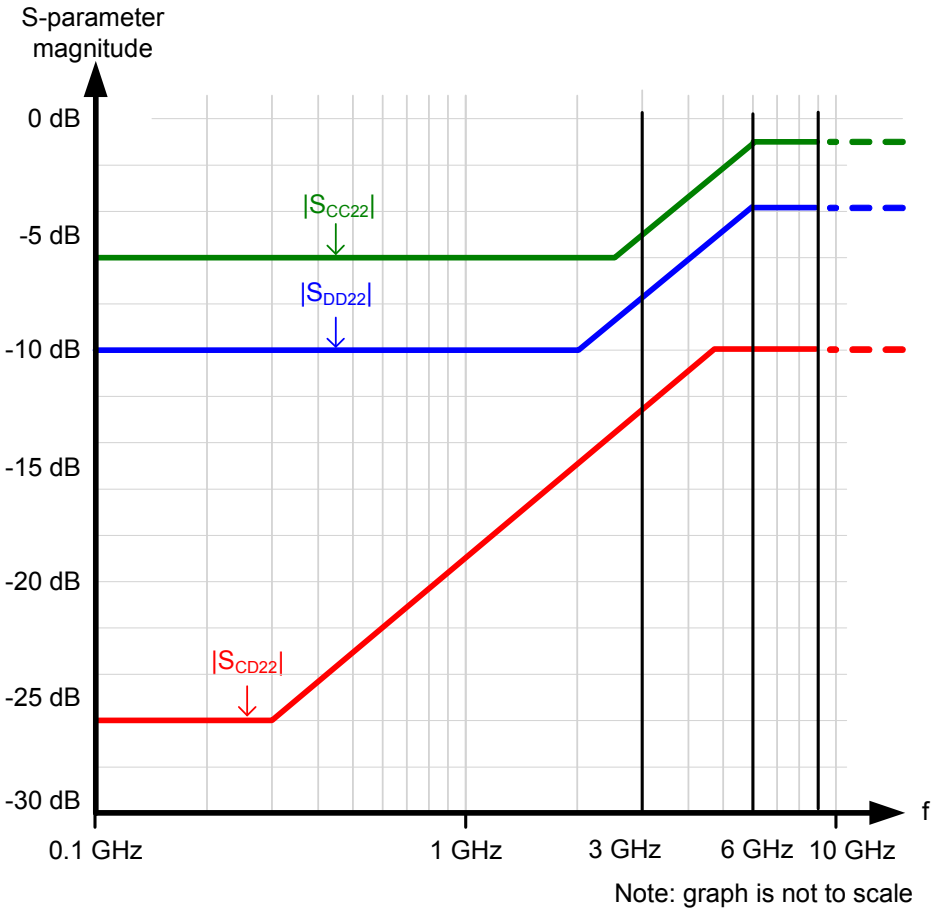


Figure 144 — Transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.8.4.6.4 Recommended trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device settings for interoperability

Table 45 defines recommended values for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter devices to provide interoperability with a broad range of implementations utilizing compliant TxRx connections and compliant receiver devices. The values are based on the evaluation of simulations with a variety of characterized physical hardware. Use of the recommended values does not guarantee that an implementation is capable of achieving a specific BER.

Specific implementations may obtain increased margin by deviating from the recommended values, however, such implementations are beyond the scope of this standard.

Table 45 — Recommended trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device settings at IT and CT

Characteristic	Units	Minimum	Nominal	Maximum
Differential voltage swing (mode) (VMA) [a]	mV	600	707	
Transmitter equalization [a]	dB	2	3	4
[a] See 5.8.4.6.6 for measurement method.				

5.8.4.6.5 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics

The trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device is a set of parameters defining the electrical performance characteristics of a transmitter device used in simulation to determine compliance of a TxRx connection (see 5.5.5).

Figure 145 shows a trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device.

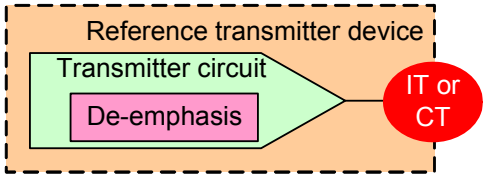


Figure 145 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device

Table 46 defines the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics.

Table 46 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics at IT and CT

Characteristic	Units	Value
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850
Transmitter equalization [a]	dB	2
Maximum (i.e., slowest) rise/fall time [b]	UI	0.41 [c]
RJ	UI	0.15 [d]
BUJ	UI	0.10 [e]

[a] See 5.8.4.6.6 for measurement method.
[b] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4).
[c] 0.41 UI is 68.$\overline{3}$ ps at 6 Gbit/s, 136.$\overline{6}$ ps at 3 Gbit/s, and 273.$\overline{3}$ ps at 1.5 Gbit/s.
[d] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[e] 0.10 UI is 16.$\overline{6}$ ps at 6 Gbit/s, 33.$\overline{3}$ ps at 3 Gbit/s, and 66.$\overline{6}$ ps at 1.5 Gbit/s.

The following Touchstone model of the reference transmitter device termination is included with this standard:

a) SAS2_TxRefTerm.s4p.

Figure 146 shows the S-parameters of the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device termination model.

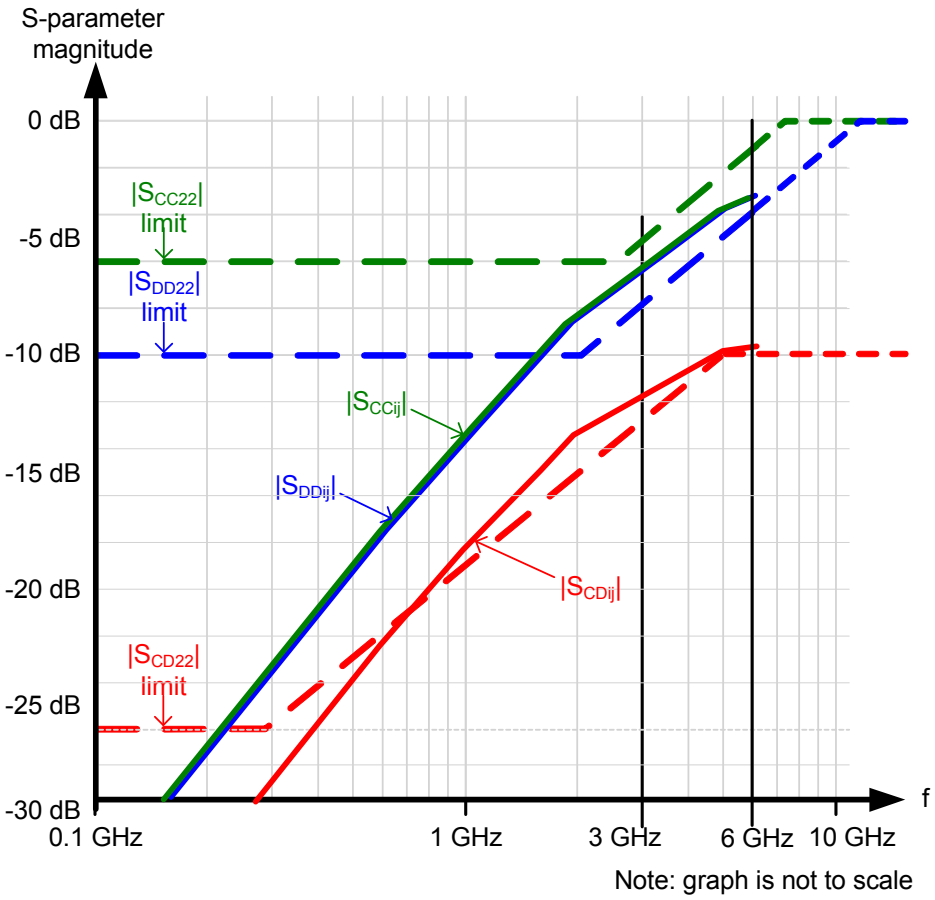


Figure 146 — Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device termination S-parameters

The Touchstone model does not exactly match the $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in 5.8.4.6.3 at all frequencies, however, it is a reasonable approximation for use in simulations. See Annex G for a description of how the Touchstone model was created.

5.8.4.6.6 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s Transmitter equalization, VMA, and V_{P-P} measurement

The trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter equalization measurement shall be based on the following values:

a) VMA: a mode (i.e., the most frequent value of a set of data) measurement; and
b) V_{P-P}: a peak to peak measurement with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4).

The VMA and V_{P-P} measurements shall be made with the transmitter device terminated through the interoperability point into a zero-length test load (see 5.6.2).

The VMA and V_{P-P} measurements shall be made using an equivalent time sampling scope with a histogram function with the following or an equivalent procedure:

1) calibrate the sampling scope for measurement of a 3 GHz signal; and
2) determine VMA and V_{P-P} as shown in figure 147. A sample size of 1 000 minimum to 2 000 maximum histogram hits for VMA shall be used to determine the values. The histogram is a combination of two histograms (i.e., an upper histogram for TX+ and a lower histogram for TX-). The histograms on the left represent the test pattern signal displayed on the right. VMA and V_{P-P} are determined by adding the values measured for TX+ and TX-.

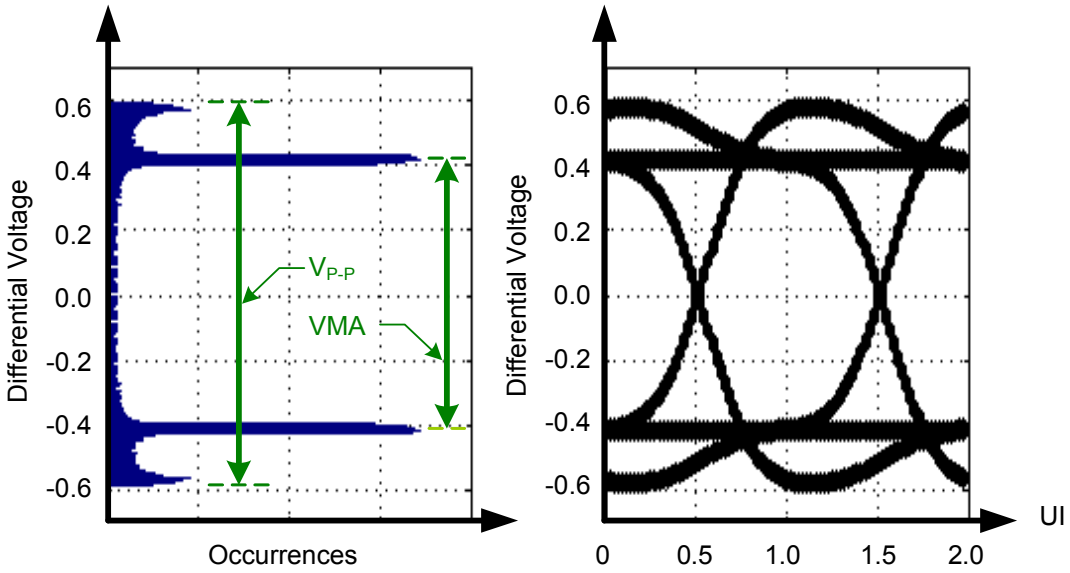


Figure 147 — Transmitter equalization measurement

The following formula shall be used to calculate the transmitter equalization value:

Transmitter equalization = 20 × lg (V_{P-P} / VMA) dB

where:

V_{P-P} is the peak to peak value; and

VMA is the mode value.

5.8.4.7 Transmitter device signal output characteristics for trained 12 Gbit/s

5.8.4.7.1 Transmitter device signal output characteristics for trained 12 Gbit/s overview

Table 47 specifies the signal output characteristics for the transmitter device for trained 12 Gbit/s.

Table 47 — Transmitter device signal output characteristics for trained 12 Gbit/s at ET, IT, and CT
(part 1 of 2)

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage at IT or CT [b] [c]	mV(P-P)			50
Rise/fall time at IT or CT [d]	ps	20.8		
Reference differential impedance at IT or CT [e]	Ω		100	
Reference common mode impedance at IT or CT [e]	Ω		25	

[a] The V_{P-P} measurement shall be made with the transmitter device set to no equalization (see table 50) and amplitude set to maximum. The minimum value applies at ET (see 5.3.3) and the maximum value applies at IT (see 5.3.3) or CT (see 5.3.3). The measurement is made with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). If using SAS3_EYEOPENING or equivalent tool for the measurement at ET, then IDLE dwords (see SPL-4) may be used for the test pattern.

[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[c] If optical mode is enabled the transmitter device off voltage is not applicable.

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link.

[e] See 5.8.4.7.2 for transmitter device S-parameters characteristics.

[f] Ratio measured with post cursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-4 and figure 151). When both precursor and post cursor equalization are active the maximum observed R_{pre} may be as high as 3.8 at the VMA limit.

[g] If a simulation tool (e.g., SAS3_EYEOPENING) is used, then this measurement may be performed with IDLE dwords (see SPL-4) as the test pattern.

[h] Ratio measured with precursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-4 and figure 151). When both precursor and post cursor equalization are active the maximum observed R_{post} may be as high as 5.5 at the VMA limit.

[i] Measured as v_2 - v_5 (see figure 151) with a repeating TRAIN_DONE primitive (see SPL-4).

[j] This is a broadband limit. For additional limits on spectral content, see figure 149 and table 48.

[k] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[l] The measurement shall include the effects of the JTF (see 5.8.3.2).

[m] RJ and TJ are measured at IT (see 5.3.3) or CT (see 5.3.3).

[n] 0.15 UI is 12.5 ps at 12 Gbit/s.

[o] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[p] 0.25 UI is 20.8 ps at 12 Gbit/s.

Table 47 — Transmitter device signal output characteristics for trained 12 Gbit/s at ET, IT, and CT
(part 2 of 2)

Signal characteristic	Units	Minimum	Nominal	Maximum
Precursor equalization ratio R_{pre} [f] [g]	V/V	1		$1.6\overline{6}$
Post cursor equalization ratio R_{post} [g] [h]	V/V	1		$3.3\overline{3}$
VMA [g] [i]	mV(P-P)	80		
Common mode voltage limit (rms) [j]	mV			30
RJ [k] [l] [m]	UI			0.15 [n]
TJ [l] [m] [o]	UI			0.25 [p]

[a] The V_{P-P} measurement shall be made with the transmitter device set to no equalization (see table 50) and amplitude set to maximum. The minimum value applies at ET (see 5.3.3) and the maximum value applies at IT (see 5.3.3) or CT (see 5.3.3). The measurement is made with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). If using SAS3_EYEOPENING or equivalent tool for the measurement at ET, then IDLE dwords (see SPL-4) may be used for the test pattern.

[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[c] If optical mode is enabled the transmitter device off voltage is not applicable.

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link.

[e] See 5.8.4.7.2 for transmitter device S-parameters characteristics.

[f] Ratio measured with post cursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-4 and figure 151). When both precursor and post cursor equalization are active the maximum observed R_{pre} may be as high as 3.8 at the VMA limit.

[g] If a simulation tool (e.g., SAS3_EYEOPENING) is used, then this measurement may be performed with IDLE dwords (see SPL-4) as the test pattern.

[h] Ratio measured with precursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-4 and figure 151). When both precursor and post cursor equalization are active the maximum observed R_{post} may be as high as 5.5 at the VMA limit.

[i] Measured as $v_2 - v_5$ (see figure 151) with a repeating TRAIN_DONE primitive (see SPL-4).

[j] This is a broadband limit. For additional limits on spectral content, see figure 149 and table 48.

[k] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[l] The measurement shall include the effects of the JTF (see 5.8.3.2).

[m] RJ and TJ are measured at IT (see 5.3.3) or CT (see 5.3.3).

[n] 0.15 UI is 12.5 ps at 12 Gbit/s.

[o] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[p] 0.25 UI is 20.8 ps at 12 Gbit/s.

In addition to table 47, figure 148 specifies the transmitter coefficient ranges when the transmitter peak to peak voltage is maximum. The coefficients are defined according to the reference transmitter (see 5.8.4.7.3). The bottom left area of the minimum and maximum ranges in figure 148 are limited by VMA and vary according to V_{P-P}_noeq. V_{P-P}_noeq is the amplitude at ET measured with the no_equalization setting as specified in table 50.

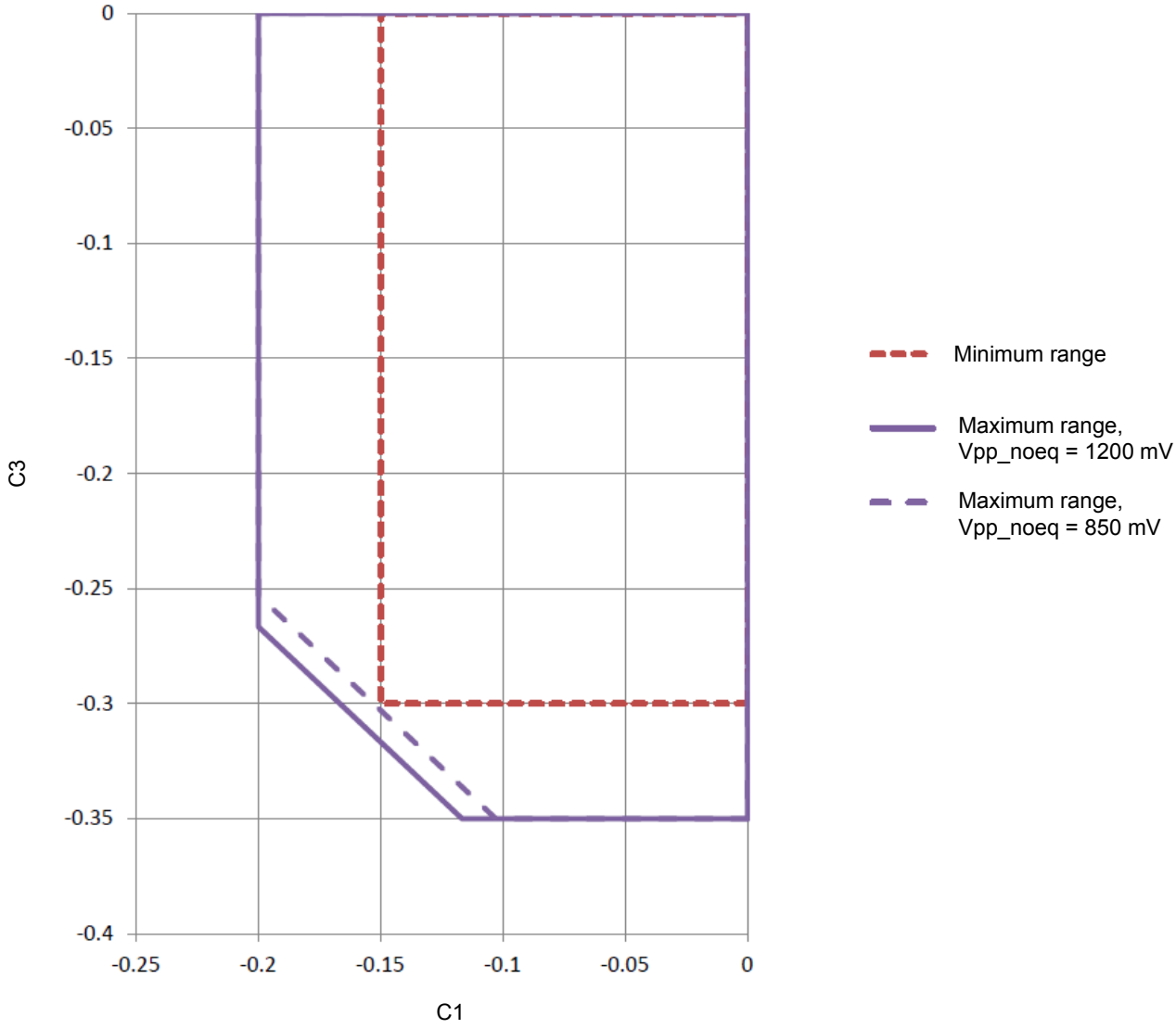


Figure 148 — Minimum and maximum coefficient ranges at maximum peak to peak voltage

Table 48 defines the transmitter device common mode voltage limit characteristics.

Table 48 — 12 Gbit/s transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] (dBmV) [b]	N [a] (dBmV) [b] [c]	S [a] (dBmV/decade) [b]	H [a] (dBmV) [b]	f_{min} [a] (MHz)	f_{max} [a] (GHz)
Spectral limit of common mode voltage [d]	Figure 149	12.7	26.0	13.3	30.0	100	9.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 Ω (i.e., the reference impedance for common mode voltage) which is 20 × lg(158) = +44 dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at 3 GHz (see figure 149).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 149 shows the transmitter device common mode voltage limit defined in table 48.

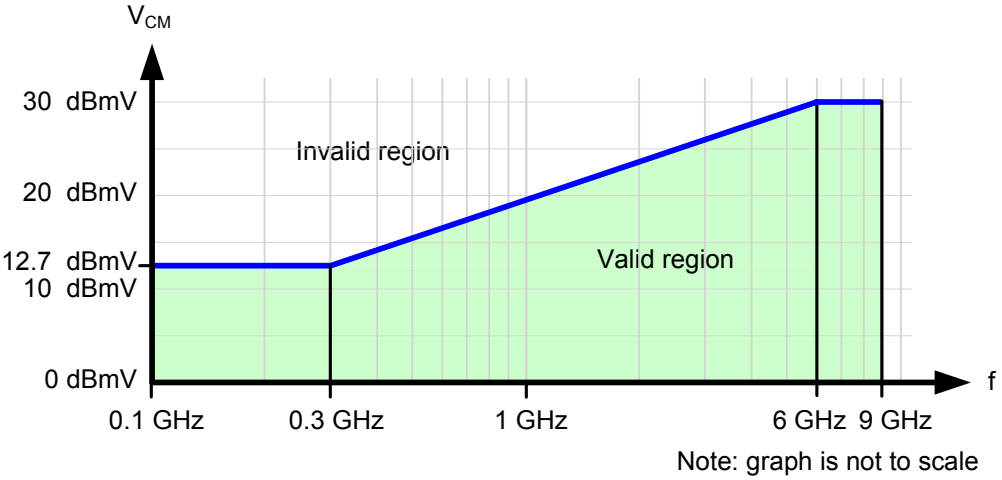


Figure 149 — 12 Gbit/s transmitter device common mode voltage limit

Transmitter equalization coefficient adjustments are controlled using the protocol defined in SPL-4. Transmitter circuits that support 12 Gbit/s, if not operating in optical mode, shall:

a) support the coefficient requests shown in table 49; and
b) provide equalization equivalent to the reference transmitter device (see 5.8.4.7.3).

The algorithm for optimizing the transmitter coefficient is beyond the scope of this standard.

Table 49 — Transmitter coefficient requests and corresponding transmitter circuit response

Coefficient 1 request	Coefficient 2 request	Coefficient 3 request	Description	$v_{HL}(k+1)$- $v_{HL}(k)$ (mV(P-P))	$v_1(k+1)$ - $v_1(k)$ (mV)	$v_2(k+1)$ - $v_2(k)$ (mV)	$v_3(k+1)$ - $v_3(k)$ (mV)
hold	hold	hold	Hold peak to peak voltage and hold equalization	-20 to +20 [a]	-10 to +10 [a]	-10 to +10 [a]	-10 to +10 [a]
dec	dec	hold	Increase precursor and hold peak to peak voltage	-20 to +20	-40 to -10	-40 to -10	-10 to +10
inc	inc	hold	Decrease precursor and hold peak to peak voltage	-20 to +20	+40 to +10	+40 to +10	-10 to +10
hold	dec	dec	Increase post cursor and hold peak to peak voltage	-20 to +20	-10 to +10	-40 to -10	-40 to -10
hold	inc	inc	Decrease post cursor and hold peak to peak voltage	-20 to +20	-10 to +10	+40 to +10	+40 to +10
hold	dec	hold	Decrease peak to peak voltage and hold equalization	-40 to -10	-20 to -5	-20 to -5	-20 to -5
hold	inc	hold	Increase peak to peak voltage and hold equalization	+40 to +10	+20 to +5	+20 to +5	+20 to +5
dec	hold	hold	Increase precursor and increase peak to peak voltage	+40 to +10	-20 to -5	-20 to -5	+20 to +5
inc	hold	hold	Decrease precursor and decrease peak to peak voltage	-40 to -10	+20 to +5	+20 to +5	-20 to -5
hold	hold	dec	Increase post cursor and increase peak to peak voltage	+40 to +10	+20 to +5	-20 to -5	-20 to -5
hold	hold	inc	Decrease post cursor and decrease amplitude	-40 to -10	-20 to -5	+20 to +5	+20 to +5

Key:

hold = Requests no change be made to the coefficient. Equivalent to hold in SPL-4.
dec = Request to make the coefficient more negative. Equivalent to decrement in SPL-4.
inc = Request to make the coefficient more positive. Equivalent to increment in SPL-4.

[a] The peak to peak voltage and equalization voltage differences between the initial condition and following any single or consecutive hold/hold/hold command shall not be greater than the specified range.

The transmitter circuit responses specified in table 49 shall be measured with a zero-length test load as shown in figure 150. The test fixture is de-embedded back to output of the transmitter circuit ET. D.C. losses are not de-embedded. For de-embedding methods see F.5.

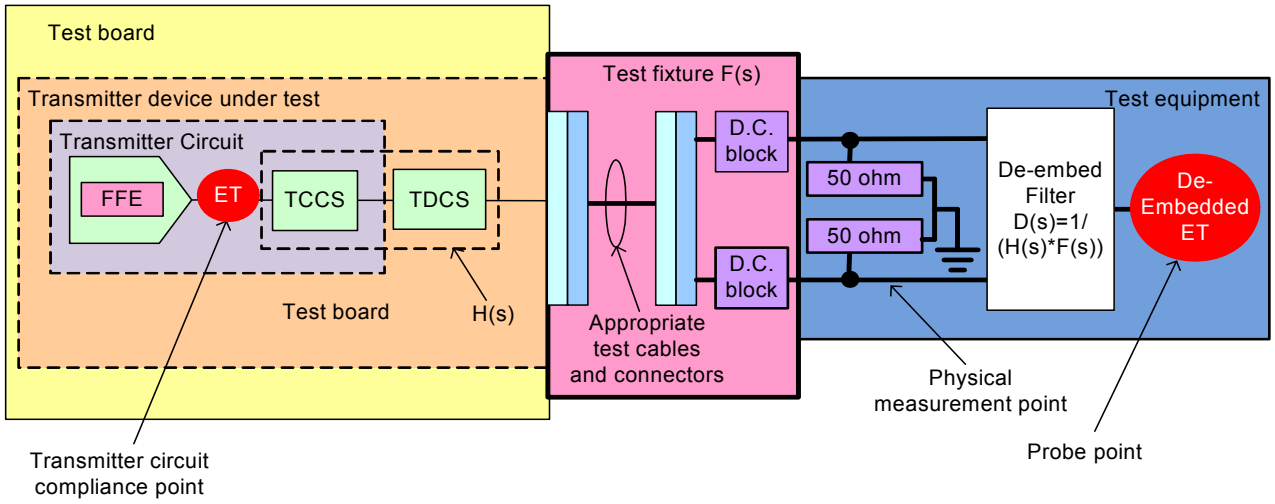


Figure 150 — Transmitter circuit compliance test configuration

All response specifications are based on differential measurements.The output waveform for a TRAIN_DONE primitive (see SPL-4) is shown in figure 151 where:

a) T is the symbol period;
b) t_1 is the zero-crossing point of the rising edge of the positive 5 UI CID;
c) t_2 is the zero-crossing point of the falling edge of the positive 5 UI CID;
d) t_3 is the zero-crossing point of the falling edge of the negative 5 UI CID;
e) t_4 is the zero-crossing point of the rising edge of the negative 5 UI CID;
f) v_1 is the maximum voltage measured in the interval t_1 to t_1 + T;
g) v_2 is the average voltage measured in the interval t_1 + 2T to t_1 + 3T;
h) v_3 is the maximum voltage measured in the interval t_2 - T to t_2;
i) v_4 is the minimum voltage measured in the interval t_3 to t_3 + T;
j) v_5 is the average voltage measured in the interval t_3 + 2T to t_3 + 3T;
k) v_6 is the minimum voltage measured in the interval t_4 - T to t_4;
l) VMA is v_2 - v_5; and
m) v_{HL} is the peak to peak voltage measured in the interval t_1 to t_1 + 80T.

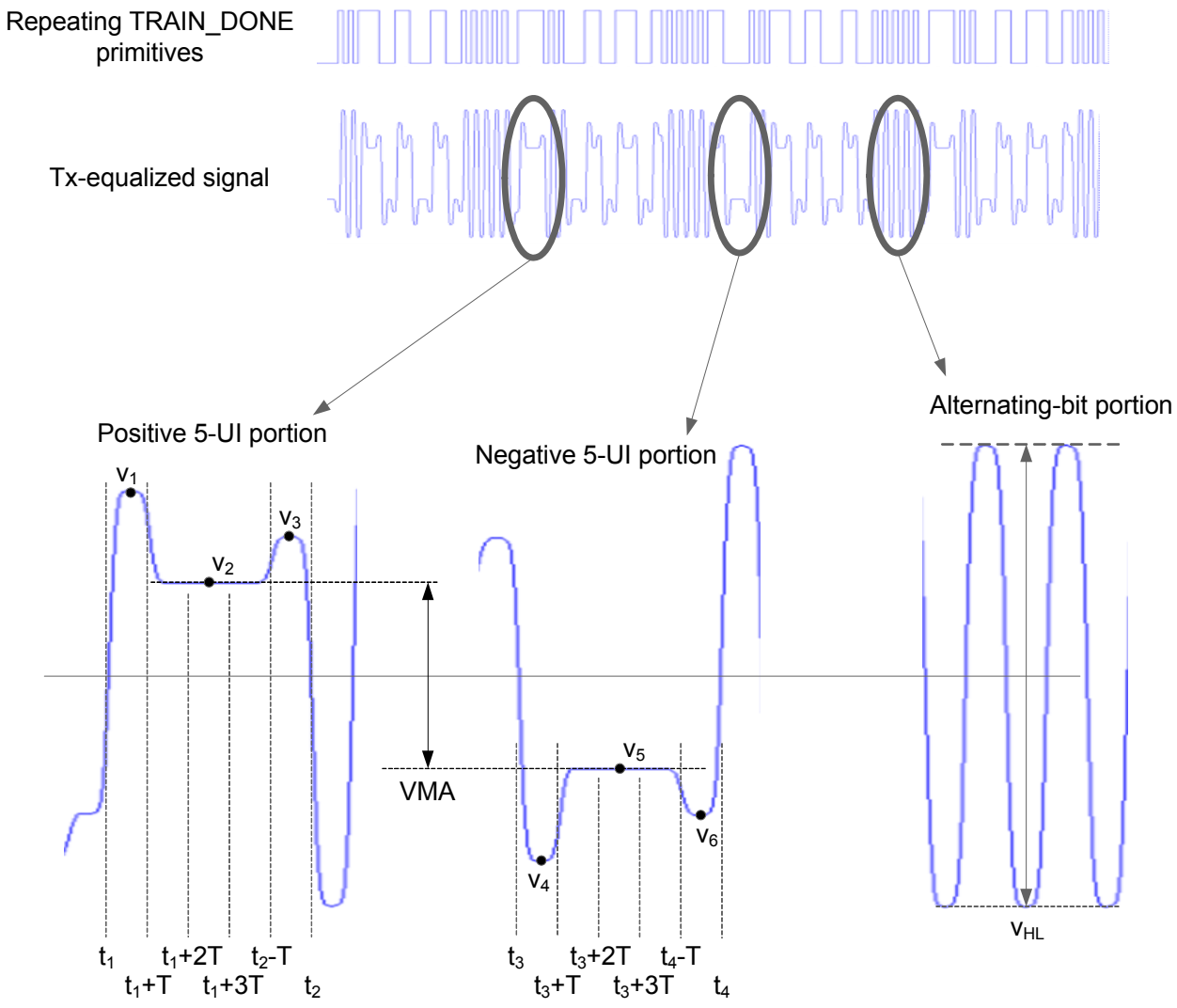


Figure 151 — 12 Gbit/s transmitter circuit output waveform

Equalization ratios are defined based on these voltages,

$$R_{post} = \frac{v_1}{v_2}$$

$$R_{pre} = \frac{V_3}{V_2}$$

Transmitter coefficient presets may be requested using a protocol that is defined in the SPL-4 standard. Transmitter circuits that support 12 Gbit/s shall:

a) support the coefficient settings shown in table 50; and
b) provide equalization equivalent to the reference transmitter device (see 5.8.4.7.3).

Table 50 — Transmitter circuit coefficient presets at ET

Coefficient settings [a]	R_{pre} (V/V) [b]			R_{post} (V/V) [b]		
	Min	Nom	Max	Min	Nom	Max
normal [c]						
reference_1 [d] [e]	2.10	2.52	2.97	2.94	3.52	4.16
reference_2 [e] [f]	1.05	1.26	1.49	1.19	1.43	1.68
no_equalization [e] [g]	0.84	1.00	1.19	0.84	1.00	1.19

Key:

Max = Maximum
Min = Minimum
Nom = Nominal

[a] The coefficient setting field in the TTIU (see SPL-4).
[b] All measurements are performed with a repeating TRAIN_DONE primitive (see SPL-4 and figure 150). If a simulation tool (e.g., SAS3_EYEOPENING) is used then this measurement may be performed with IDLE dwords (see SPL-4) as the test pattern.
[c] See SPL-4.
[d] Equivalent to the reference transmitter setting transmitter circuit coefficient 1 (i.e., C1) set to -0.15, coefficient 2 (i.e., C2) set to 0.6, and coefficient 3 (i.e., C3) set to -0.25 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[e] The reference_1, reference_2, and no_equalization presets shall set the transmitter to its maximum peak to peak voltage (V_{P-P}).
[f] Equivalent to the reference transmitter setting transmitter circuit C1 set to -0.075, C2 set to 0.8, and C3 set to -0.125 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[g] Equivalent to the reference transmitter setting transmitter circuit C1 set to zero, C2 set to one, and C3 set to zero with a ± 1.5 dB tolerance on R_{pre} and R_{post}.

5.8.4.7.2 12 Gbit/s Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × lg(f / 3 GHz)]]

where:

L is the minimum value (i.e., the low frequency asymptote);
H is the maximum value (i.e., the high frequency asymptote);
N is the value at 3 GHz;

f is the frequency of the signal in Hz;

max [A, B] is the maximum of A and B; and

min [A, B] is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 51 defines the maximum limits for S-parameters of the 12 Gbit/s transmitter device.

Table 51 — 12 Gbit/s maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\|S_{CC22}\|$	-6.0	-5.0	-1.0	13.3	100	9.0
$\|S_{DD22}\|$	-10	-7.9	-3.9	13.3	100	9.0
$\|S_{CD22}\|$	-26	-12.7	-10	13.3	100	9.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-4). The amplitude applied by the test equipment shall be less than -4.4 dBm (i.e., 190 mV zero to peak) per port (see F.11.4.2).

[b] $|S_{DC22}|$ is not specified.

[c] See figure 4 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 152 shows the 12 Gbit/s transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 51.

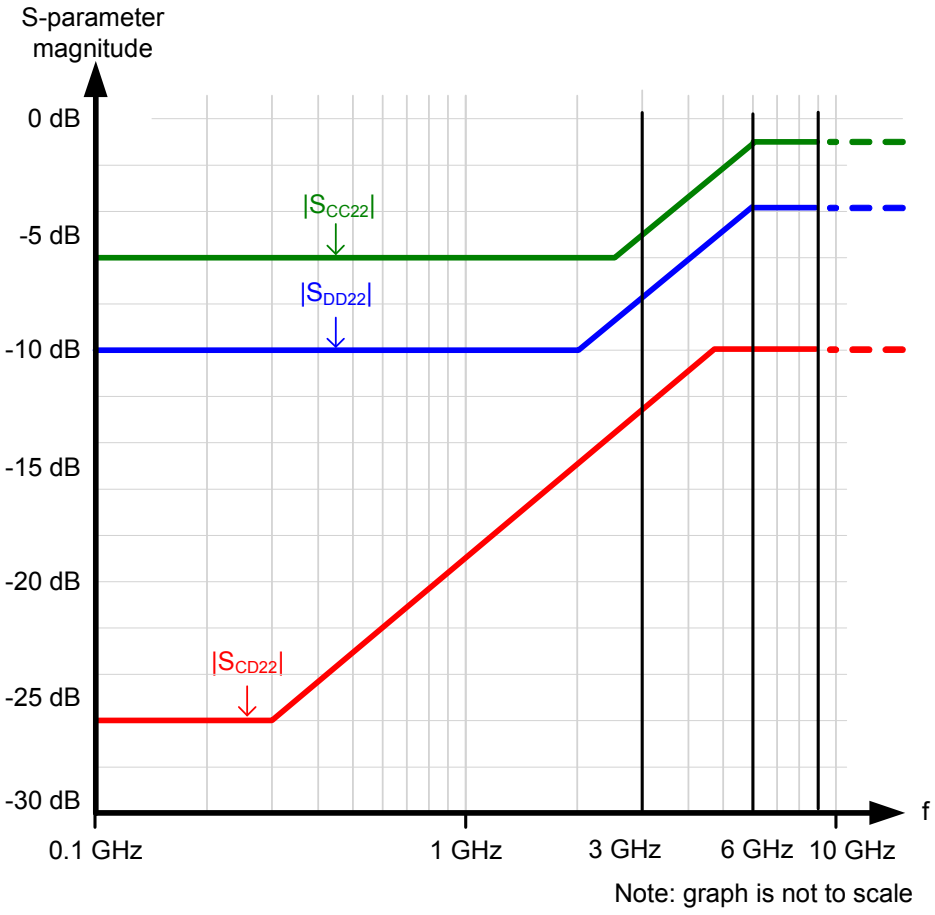


Figure 152 — 12 Gbit/s transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.8.4.7.3 12 Gbit/s reference transmitter device

The 12 Gbit/s reference transmitter device is a set of parameters and equalization filters defining the electrical performance characteristics of a transmitter circuit used in simulation. Figure 153 illustrates the reference transmitter device.

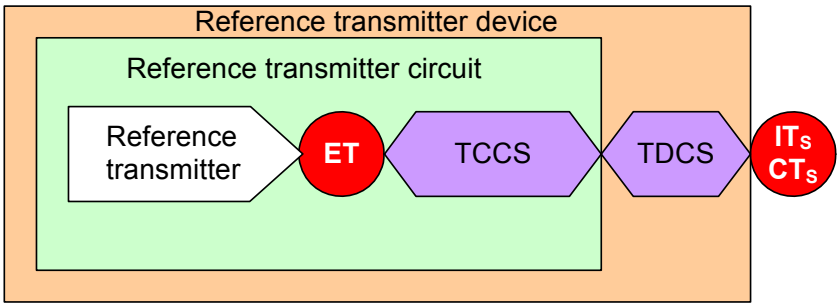


Figure 153 — 12 Gbit/s reference transmitter device

Figure 154 shows the reference transmitter generating the signal at ET. Passive TxRx connection segments TCCS and TDCS simulate the reference TxRx connection segment between ET and CT_S or ET and IT_S. See C.2 for the description of the reference TxRx connection segments.

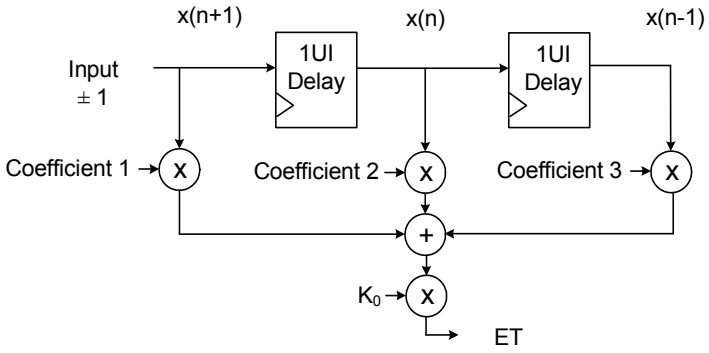


Figure 154 — 12 Gbit/s reference transmitter

During 12 Gbit/s end to end simulations (see 5.7), the reference transmitter device parameters are optimized to maximize the eye opening at the output of the reference receiver device (5.8.5.7.3) using the procedure defined in 5.7.3. Table 52 defines the reference transmitter device characteristics. The reference transmitter device shall use the minimum peak to peak voltage and minimum rise/fall time. The input is a unitless stream of pulses representing transmitted data. The amplitude of these pulses reach +1 or -1. The stream of pulses contain the jitter and rise/fall time characteristics defined in table 52.

Table 52 — 12 Gbit/s reference transmitter device characteristics at ET

Signal characteristic	Units	Minimum	Nominal	Maximum
Output gain (K_0)	V/V	0.425		
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		
Precursor coefficient (i.e., coefficient 1) [a]	V/V	-0.15		0
VMA [b]	mV(P-P)	80		
Post cursor coefficient (i.e., coefficient 3) [a]	V/V	-0.3		0
Rise/fall time [c]	ps	25		
RJ [d] [e]	UI			0.15
DJ [f]	UI			0.1

[a] V_{P-P} is constrained in the reference transmitter device by
C2 = 1 - |C1| - |C3|
where:
C1 = coefficient 1;
C2 = coefficient 2; and
C3 = coefficient 3.

[b] VMA = $2K_0$ (C1 + C2 + C3) V.

[c] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4).

[d] 0.15 UI is 12.5 ps at 12 Gbit/s.

[e] RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.

[f] 0.1 UI is 8.3 ps at 12 Gbit/s.

5.8.4.7.4 Transmitter device end to end simulation characteristics for trained 12 Gbit/s

The end to end simulation procedure for transmitter devices connected to passive TxRx connections is as follows:

1) set the transmitter to output IDLE dwords (see SPL-4);
2) set the transmitter to the no_equalization coefficient setting (see SPL-4);
3) capture the signal at IT (see 5.3.3) or CT (see 5.3.3) into a zero-length test load (see 5.6.2);
4) measure the total crosstalk amplitude (see 5.7.4) or extract crosstalk transfer functions (e.g., S-parameters);
5) connect TxRx connection segments, crosstalk segments, reference transmitter and reference receiver according to the reference end to end simulation diagram (see 5.7.2, C.2.1 and C.2.2);
6) set the reference transmitter equalization (see 5.7.3) and reference receiver DFE equalization (see 5.8.5.7.3); and
7) perform a linear simulation, including the effects of edge rates, ISI and crosstalk (see C.1).

The characteristics of the signal at specified points in the simulation are defined in table 53. See the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3).

Table 53 — Transmitter device characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a] [b] [c]	V/V	-0.15	0	ET
VMA [d] [e]	mV(P-P)	80		ET
Coefficient 3 (i.e., C3) [a] [b] [f]	V/V	-0.3	0	ET
Reference pulse response cursor peak to peak amplitude [g]	mV(P-P)	135		ER
Vertical eye opening to reference pulse response cursor ratio [h] [i]	%	45		ER
DFE coefficient amplitude to reference pulse response cursor ratio [j]	%	-50	50	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[b] C2 = 1 - |C1| - |C3|.

[c] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[d] VMA = $2K_0$ (C1 + C2 + C3) V. See 5.8.4.7.3.

[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3)^2)^{0.5}$$

where:

C1' and C3' are values that satisfy the minimum VMA criterion.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] The average amplitude of the eye for an IDLE pattern (see SPL-4) digital input at the compliance point may be used for this measurement. See figure 135.

[h] The vertical eye opening includes the effects of crosstalk (see C.1).

[i] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the transmitter device.

[j] The maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(d_i)) divided by the reference pulse response cursor (see 5.8.5.7.3).

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter-free reference transmitter with K_0 set to one (i.e., unit-less value) at the output of the transmitter device (see 5.8.4.7.3), using the transmitter device output as the input of the reference transmitter instead of the +1/-1 digitized stream (see figure 155). For non-separable TxRx connection segments, the reference simulation channel (i.e., <usage>_IR_RR) does not include the reference PICS.

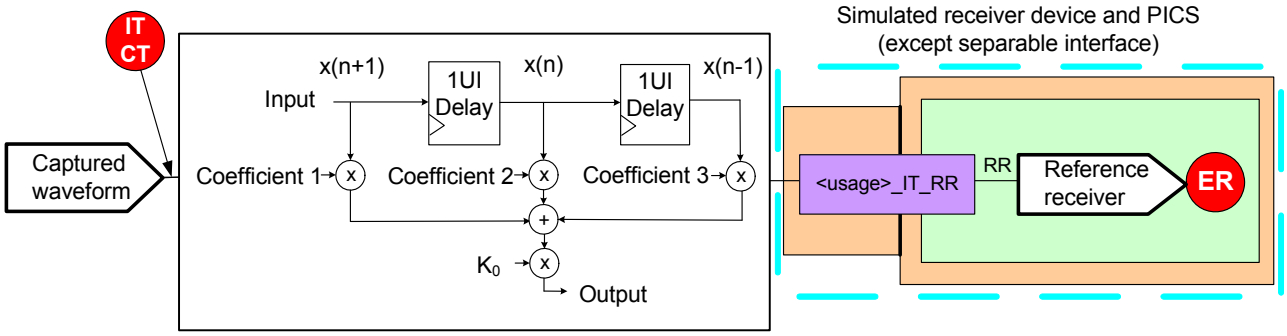


Figure 155 — Simulation of the reference transmitter from a captured signal

5.8.4.7.5 Transmitter device signal output characteristics at CT_S for 12 Gbit/s when an active cable is connected

Transmitter devices supporting trained 12 Gbit/s that are connected to an external cable connector shall support the signal characteristics specified in table 54 at CT_S when an active cable is connected.

Table 54 — Transmitter device signal output characteristics for 12 Gbit/s at CT_S when an active cable is connected

Signal characteristic	Units	CT_S
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 119) [a] [b]	mV(P-P)	1 200
Minimum eye opening (i.e., 2 × Z1 in figure 119) [a] [c]	mV(P-P)	200
Maximum half of TJ (i.e., X1 in figure 119) [a] [c] [d]	UI	0.175
Maximum RJ [a] [b] [d]	UI	0.15
Center of bit time (i.e., X2 in figure 119)	UI	0.5

[a] All crosstalk sources shall be active with representative traffic during the measurement.
[b] The maximum peak to peak voltage measurement and RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] The minimum eye opening measurement and TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) with SSC enabled for a period of at least 33.3 µs (i.e., a full SSC cycle).
[d] The measurement shall include the effects of the JTF (see 5.8.3.2).

5.8.4.8 Transmitter device signal output characteristics for OOB signals

Transmitter devices supporting SATA shall use SATA Gen1i, Gen2i, or Gen3i signal output levels (see SATA) during the first OOB sequence (see SPL-4) after a power on or hard reset. If the phy does not receive COMINIT within a hot-plug timeout (see SPL-4), then the transmitter device shall increase its transmit levels to the OOB signal output levels specified in table 55 and perform the OOB sequence again. If no COMINIT is

received within a hot-plug timeout of the second OOB sequence, then the transmitter device shall initiate another OOB sequence using SATA Gen1i, Gen2i, or Gen3i signal output levels. The transmitter device shall continue alternating between transmitting COMINIT using SATA Gen1i, Gen2i, or Gen3i signal output levels and transmitting COMINIT with SAS signal output levels until the phy receives COMINIT.

If the phy both transmits and receives COMSAS (i.e., a SAS phy or expander phy is attached), then the transmitter device shall set its transmit levels to the SAS signal output levels (see 5.8.4.4, 5.8.4.5, and 5.8.4.6) prior to beginning the SAS speed negotiation sequence (see SPL-4). If transmitter device had been using SATA Gen1i, Gen2i, or Gen3i signal output levels, this mode transition (i.e., output voltage change) may result in a transient (see 5.8.2) during the idle time between COMSAS and the SAS speed negotiation sequence.

If the transmitter device is using SAS signal output levels and the phy does not receive COMSAS (i.e., a SATA phy is attached), then the transmitter device shall set its transmit levels to the SATA Gen1i, Gen2i, or Gen3i signal output levels and restart the OOB sequence.

Transmitter devices that do not support SATA or that have optical mode enabled shall transmit OOB signals using SAS signal output levels. In phy low power conditions (see SPL-4) the output common mode specification OOB common mode delta (see table 55) is relaxed to enable transmitter device power savings. During phy low power conditions, the transmitter device should reduce its output swing level to save power. Before exiting a phy low power condition the transmitter device shall wait for its common mode to settle.

Table 55 defines the transmitter device signal output characteristics for OOB signals.

Table 55 — Transmitter device signal output characteristics for OOB signals

Characteristic	Units	IT	CT
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 140)	mV(P-P)	1 200	
OOB offset delta [a] [b]	mV	± 25	
OOB common mode delta [b] [c]	mV	± 50	
Minimum OOB burst amplitude [d], if SATA is not supported	mV(P-P)	240 [e]	
Minimum OOB burst amplitude [d], if SATA is supported	mV(P-P)	240 [e] [f]	N/A

[a] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.
[b] This is not applicable when optical mode is enabled or in phy low power conditions.
[c] The maximum difference in the average of the common mode voltage between the burst times and the idle times of an OOB signal.
[d] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst as measured with each test load at IT and CT.
[e] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see SPL-4 and SATA).
[f] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.8.5 Receiver device characteristics

5.8.5.1 Receiver device characteristics overview

The receiver device shall operate within the required BER (see 5.5.1) when a signal with valid voltage and timing characteristics is delivered to the receiver device compliance point from a nominal 100 Ω source. The received signal shall be considered valid if it meets the voltage and timing limits specified in table 59 (see 5.8.5.4) for untrained 1.5 Gbit/s and 3 Gbit/s and table 63 (see 5.8.5.7.1) for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) receiver device requirements.

Additionally, for untrained 1.5 Gbit/s and 3 Gbit/s the receiver device shall operate within the required BER when the signal has additional SJ present as specified in table 61 (see 5.8.5.6) with the common mode signal V_{CM} as specified in table 56 (see 5.8.1). Jitter tolerance for receiver device compliance points is shown in figure 142 (see 5.8.3.5). Figure 142 assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver device, the additional 0.1 UI of SJ may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiver device. The additional jitter reduces the eye opening in both voltage and time. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s the additional jitter is included in the stressed receiver device jitter tolerance test (see 5.8.5.7.6).

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

See F.10 for a methodology for measuring receiver device signal tolerance.

A receiver device shall provide equivalent performance to the reference receiver device (see 5.8.5.7.3) and shall operate within the required BER when attached to:

a) any transmitter device compliant with this standard (see 5.8.4); and
b) any TxRx connection compliant with this standard (see 5.5).

5.8.5.2 Receiver device coupling requirements

Coupling requirements for receiver devices are as follows:

a) all receiver devices (i.e., attached to IR (see 5.3) or CR (see 5.3) compliance points) shall be A.C. coupled to the interconnect through a receive network.

See table 36 (see 5.8.1) for the coupling capacitor value.

5.8.5.3 Receiver device general electrical characteristics

Table 56 defines the receiver device general electrical characteristics.

Table 56 — Receiver device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s
Physical link rate accuracy [a] tolerance at IR if SATA is not supported	ppm	± 100			
Physical link rate accuracy [a] tolerance at IR if SATA is supported	ppm	± 350			
Physical link rate SSC modulation tolerance at IR and CR	ppm	See table 76 in 5.8.6.3			
Maximum receiver device transients [b]	V	± 1.2			
Minimum receiver A.C. common mode voltage tolerance V_{CM} [c d]	mV(P-P)	150			
Receiver A.C. common mode frequency tolerance range F_{CM} [c]	MHz	2 to 200			

[a] Physical link rate accuracy shall be measured over a minimum of 1 x 10^6 UI and should be measured using a minimum resolution of 100 Hz.
[b] See 5.8.2 for transient test circuits and conditions.
[c] Receiver devices shall tolerate sinusoidal common mode noise components within the peak to peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[d] The measurement shall be made with a channel equivalent to the channel used in the zero-length test load (see figure 122) (see 5.6.2).

The common mode frequency tolerance range for 6 Gbit/s and 12 Gbit/s is extended to include the effects of duty cycle distortion. Measurement methods for testing the extended frequency ranges for AC common mode tolerance are not defined by this standard; therefore the common mode signal characteristics defined in table 57 are recommended design guidelines for receiver devices supporting 6 Gbit/s and 12 Gbit/s.

Table 57 — Recommended receiver device common mode tolerance for 6 Gbit/s, and 12 Gbit/s

Characteristic	Units	6 Gbit/s	12 Gbit/s
Minimum receiver A.C. common mode voltage tolerance V_{CM} [a b]	mV(P-P)	150	
Receiver A.C. common mode frequency tolerance range F_{CM} [b]	MHz	2 to 3 000	2 to 6 000

[a] Receiver devices should be designed to tolerate sinusoidal common mode noise components within the peak to peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[b] The value represents the signal characteristic at IR or CR when the channel between the transmitter device and IR or CR is equivalent to the channel used in the zero-length test load (see figure 122) (see 5.6.2).

Table 58 defines the receiver device termination characteristics.

Table 58 — Receiver device termination characteristics

Characteristic	Units	Untrained		Trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s
		1.5 Gbit/s	3 Gbit/s	
Differential impedance [a b c]	Ω	100 ± 15		See 5.8.5.7.1
Maximum differential impedance imbalance [a b c d]	Ω	5		See 5.8.5.7.2 [e]
Maximum receiver termination time constant [a b c]	ps	150	100	N/A
Common mode impedance [a b]	Ω	20 minimum 40 maximum		See 5.8.5.7.1

[a] All receiver device termination measurements are made through mated connector pairs.

[b] The receiver device termination impedance specification applies to all receiver devices in a TxRx connection and covers all time points between the connector nearest the receiver device, the receiver device, and the transmission line terminator. This measurement shall be made from that connector.

[c] At the time point corresponding to the connection of the receiver device to the transmission line, the input capacitance of the receiver device and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. With impedance measured using amplitude in units of ρ (i.e., the reflection coefficient, a dimensionless unit) and duration in units of time, the area of the impedance dip caused by this capacitance is the receiver termination time constant. The receiver termination time constant shall not be greater than the values shown in this table.

An approximate value for the receiver termination time constant is given by the following equation:

RTTC = amp × width

where:

RTTC receiver termination time constant in seconds;

amp amplitude of the dip in units of ρ (i.e., the difference between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point); and

width width of the dip in units of time, as measured at the half amplitude point.

The value of the receiver device excess input capacitance is given by the following equation:

$$C = \frac{RTTC}{(R_0 \parallel R_R)}$$

where:

C receiver device excess input capacitance in farads;

RTTC receiver termination time constant in seconds;

R_0 transmission line characteristic impedance in Ω;

R_R termination resistance at the receiver device in Ω; and

$(R_0 \parallel R_R)$ parallel combination of R_0 and R_R.

[d] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.

[e] Measurement replaced by S_{CD11} specifications (i.e., differential to common mode conversion).

5.8.5.4 Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s

Table 59 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. These also serve as the required signal tolerance characteristics of the receiver device. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, see 5.8.5.7.

Table 59 — Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load at IR and CR

Signal characteristic	Units	IR, untrained		CR, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 141) if a SATA phy is not attached	mV(P-P)	1 200		1 200	
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 141) if a SATA phy is attached	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 141), if a SATA phy is not attached	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 141), if a SATA phy using Gen1i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	225 [a]	N/A	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 141), if a SATA phy using Gen2i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	N/A	175 [a]	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 141), if a SATA phy is attached and the TxRx connection is characterized with the low-loss TCTF test load (see 5.6.4)	mV(P-P)	275 [a]		N/A	
Jitter tolerance (see figure 142 in 5.8.3.5) [b] [c]	N/A	See table 61 in 5.8.5.6			
Maximum half of TJ (i.e., X1 in figure 141) [d]	UI	0.275			
Center of bit time (i.e., X2 in figure 141)	UI	0.50			
Maximum intra-pair skew [e]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[c] SSC shall be enabled if the receiver device supports being attached to SATA. Jitter setup shall be performed prior to application of SSC.

[d] The value for X1 shall be half the value given for TJ in table 60. When SSC is disabled, the test or analysis shall include the effects of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667).

[e] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal at the probe points.

5.8.5.5 Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s

Table 60 defines the maximum jitter the system shall deliver to the receiver device at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s see 5.8.5.7.6.

Table 60 — Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic [a] [b]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Deterministic jitter (DJ) [c]	UI	0.35	
Total jitter (TJ) [c] [d] [e]	UI	0.55	

[a] All DJ and TJ values are level 1 (see MJSQ).
[b] The values for jitter in this table are measured at the average signal amplitude point.
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] TJ is specified at a CDF level of 10^{-12}.
[e] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.
Jitter peak to peak measured < (maximum TJ - |Asymmetry|)

5.8.5.6 Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s

Table 61 defines the amount of jitter the receiver device shall tolerate at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. Receiver device jitter testing shall be performed with the maximum (i.e., slowest) rise/fall times, minimum signal amplitude, and maximum TJ, and should be performed with normal activity in the receiver device (e.g., with other transmitter circuits and receiver circuits on the same board as the receiver device performing normal activity) with SSC enabled if SSC is supported by the receiver device. Jitter setup shall be performed prior to application of SSC. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s see 5.8.5.7.6.

Table 61 — Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Applied sinusoidal jitter (SJ) from f_c to f_{max} [a]	UI	0.10 [e]	0.10 [f]
Deterministic jitter (DJ) [b] [c]	UI	0.35 [g]	0.35 [h]
Total jitter (TJ) [b] [c] [d]	UI	0.65	

[a] The jitter values given are normative for a combination of applied SJ, DJ, and TJ that receiver devices shall be able to tolerate without exceeding the required BER (see 5.5.1). Receiver devices shall tolerate applied SJ of progressively greater amplitude at lower frequencies than f_c, according to figure 156, with the same DJ and RJ levels as were used from f_c to f_{max}.
[b] All DJ and TJ values are level 1 (see MJSQ).
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.4. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] No value is given for RJ. For compliance with this standard, the actual RJ amplitude shall be the value that brings TJ to the stated value at a probability of 10^{-12}. The additional 0.1 UI of applied SJ is added to ensure the receiver device has sufficient operating margin in the presence of external interference.
[e] Applied sinusoidal swept frequency for 1.5 Gbit/s: 900 kHz to 5 MHz.
[f] Applied sinusoidal swept frequency for 3 Gbit/s: 1 800 kHz to 7.5 MHz.
[g] The measurement bandwidth for 1.5 Gbit/s shall be 900 kHz to 750 MHz.
[h] The measurement bandwidth for 3 Gbit/s shall be 1 800 kHz to 1 500 MHz.

Figure 156 defines the applied SJ for table 61.

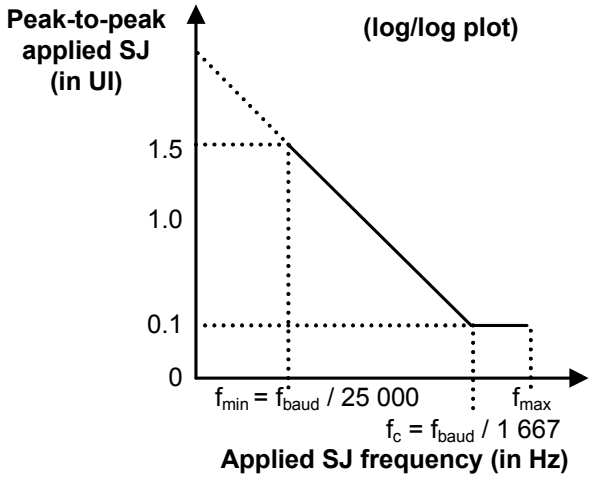


Figure 156 — Applied SJ for untrained 1.5 Gbit/s and 3 Gbit/s

Table 62 defines f_{min}, f_c, and f_{max} for figure 156. f_{baud} is defined in table 36 (see 5.8.1).

Table 62 — f_{min}, f_c, and f_{max} for untrained 1.5 Gbit/s and 3 Gbit/s

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz

5.8.5.7 Receiver device and delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s

5.8.5.7.1 Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s

Table 63 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2), unless otherwise specified, attached at the receiver device compliance point (i.e., IR (see 5.3) or CR (see 5.3)) for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s. These also specify the required signal tolerance characteristics of the receiver device. All specifications are based on differential measurements unless otherwise stated.

Table 63 — Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s at IR and CR

Characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s [a] [b] [c]	mV(P-P)			1 200
Non-operational input voltage	mV(P-P)			2 000
Reference differential impedance [d]	Ω		100	
Reference common mode impedance [d]	Ω		25	

[a] See 5.8.4.6.6 for the measurement method for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[b] See table 47 for the measurement method for 12 Gbit/s.
[c] During OOB, SNW-1, SNW-2, and SNW-3 (see SPL-4), the untrained 1.5 Gbit/s and 3 Gbit/s specifications in 5.8.5.4 apply.
[d] For receiver device S-parameter characteristics, see 5.8.5.7.2.

5.8.5.7.2 Receiver device S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [L, \min [H, N + 13.3 \times \lg(f / 3\ \text{GHz})]]$$

where:

L is the minimum value (i.e., the low frequency asymptote);
H is the maximum value (i.e., the high frequency asymptote);
N is the value at 3 GHz;
f is the frequency of the signal in Hz;
max [A, B] is the maximum of A and B; and
min [A, B] is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 64 defines the maximum limits for S-parameters of the receiver device.

Table 64 — Maximum limits for S-parameters at IR or CR

Characteristic [a]	L [b] (dB)	N [b] (dB)	H [b] (dB)	S [b] (dB / decade)	f_{min} [b] (MHz)	f_{max} [b] [c] (GHz)	f_{max} [d] (GHz)
$\|S_{CC11}\|$	-6.0	-5.0	-1.0	13.3	100	6.0	9.0
$\|S_{DD11}\|$	-10	-7.9	-3.9	13.3	100	6.0	9.0
$\|S_{CD11}\|$	-26	-12.7	-10	13.3	100	6.0	9.0

[a] $|S_{DC11}|$ is not specified.
[b] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.
[c] Applies only for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[d] Applies only for 12 Gbit/s.

Figure 157 shows the receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in table 64.

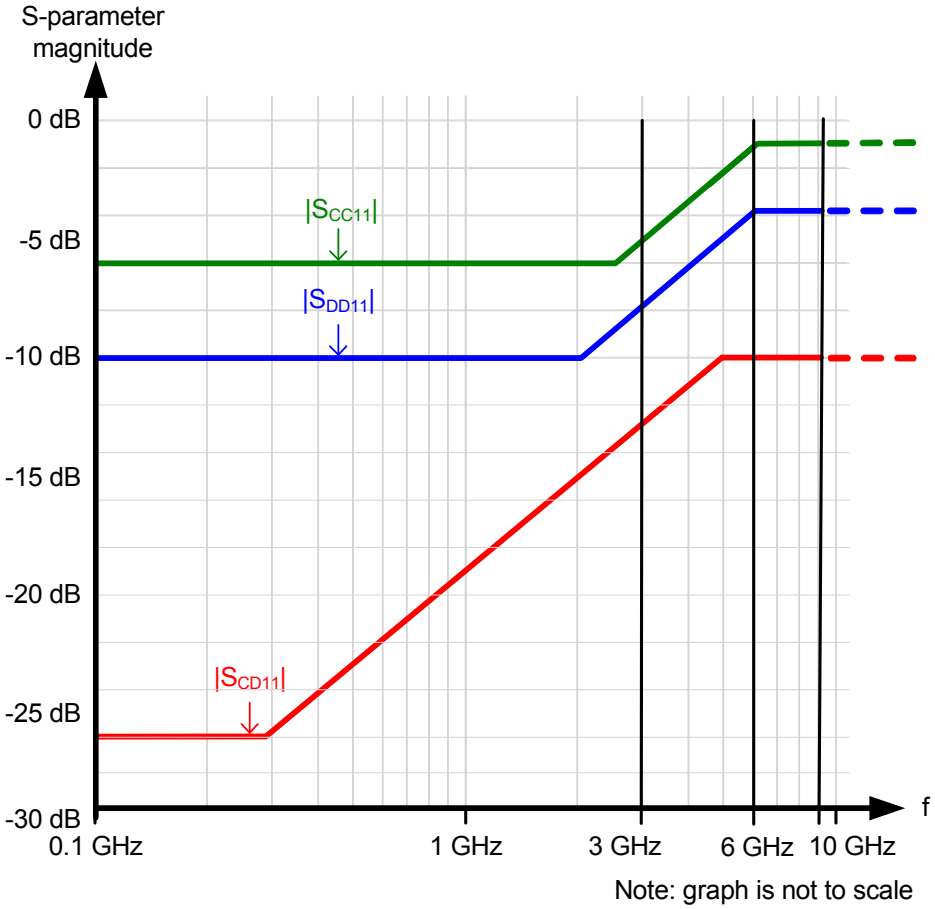


Figure 157 — Receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits

5.8.5.7.3 Reference receiver device characteristics

5.8.5.7.3.1 Reference receiver device overview

The reference receiver device is a set of parameters defining the electrical performance characteristics of a receiver device used in simulation to:

a) determine compliance of a transmitter device (see 5.8.4.6 and 5.8.4.7); and
b) determine compliance of a TxRx connection (see 5.5.5 and 5.5.6).

Figure 158 shows the reference receiver device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

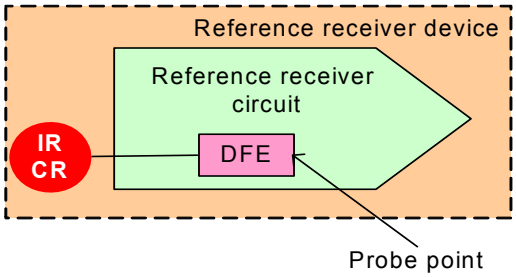


Figure 158 — Reference receiver device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Figure 159 shows the reference receiver device for trained 12 Gbit/s. Passive TxRx connection segments RDCS and RCCS simulate the reference TxRx connection segment between IR and RR or CR and RR. See C.2 for the description of the reference TxRx connection segments.

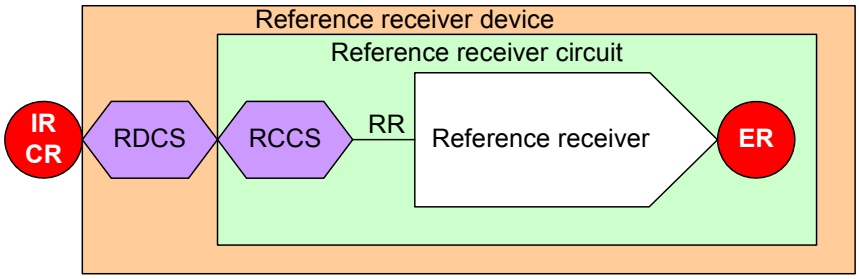


Figure 159 — Reference receiver device for trained 12 Gbit/s

For trained 1.5 Gbit/s, 3 Gbit/s and 6 Gbit/s, the reference receiver circuit performs the reference DFE equalization at the center of the eye.

For trained 12 Gbit/s, the reference receiver device:

1) applies the reference receiver equalization (see 5.8.5.7.3.3);
2) samples the incoming data according to a reference sampling clock (see 3.1.82); and
3) performs the reference DFE equalization.

The signal at the probe point or at ER is an analog signal.

5.8.5.7.3.2 Reference receiver device DFE

The reference receiver device includes a multiple tap DFE with infinite precision taps and unit interval tap spacing. The reference coefficient adaptation algorithm is the LMS algorithm. The DFE may be modeled at the reference sampling instants as:

$$y_k = x_k - \sum_{i=1}^{N_{dfe}} d_i \times \mathrm{sgn}(y_{k-i})$$

where:

y	is the equalizer differential output voltage;
x	is the equalizer differential input voltage;
d	is the equalizer feedback coefficient;
k	is the sample index in UI; and
N_{dfe}	is the number of equalizer DFE taps. N_{dfe} = 3 for the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference receiver device. N_{dfe} = 5 for the 12 Gbit/s reference receiver device.

The trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s reference receiver device feedback coefficients (i.e., d_i) have absolute magnitudes that are less than 0.5 times the peak of the equivalent pulse response of the reference receiver device.

NOTE 8 - For more information on DFE and LMS, see John R. Barry, Edward A. Lee, and David G. Messerschmitt. *Digital Communication - Third Edition*. Kluwer Academic Publishing, 2003. See http://users.ece.gatech.edu/~barry/digital.

5.8.5.7.3.3 Reference receiver device equalization for trained 12 Gbit/s

The reference receiver applies a filter composed of three cascaded identical equalization stages. Each of these stages has the characteristics described in table 65. The frequency response of each stage is of the form:

$$H(s) = (1 + s/(2\pi \times fz_0)) / [(1 + s/(2\pi \times fp_0)) \times (1 + s/(2\pi \times fp_1))]$$

where:

s	represents $2\pi \times f \times (-1)^{0.5}$;
fz_0	is the zero corner frequency;
fp_0	is the first pole corner frequency; and
fp_1	is the second pole corner frequency.

Table 65 — Reference receiver equalization stage characteristics for trained 12 Gbit/s

Characteristic	Units	Value
Zero corner frequency (fz_0)	GHz	2.5
First pole corner frequency (fp_0)	GHz	4
Second pole corner frequency (fp_1)	GHz	10

5.8.5.7.4 Reference receiver device termination characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The following Touchstone model of the reference receiver device termination is included with this standard:

a) SAS2_RxRefTerm.s4p.

Figure 160 shows the S-parameters of the reference receiver device termination model for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

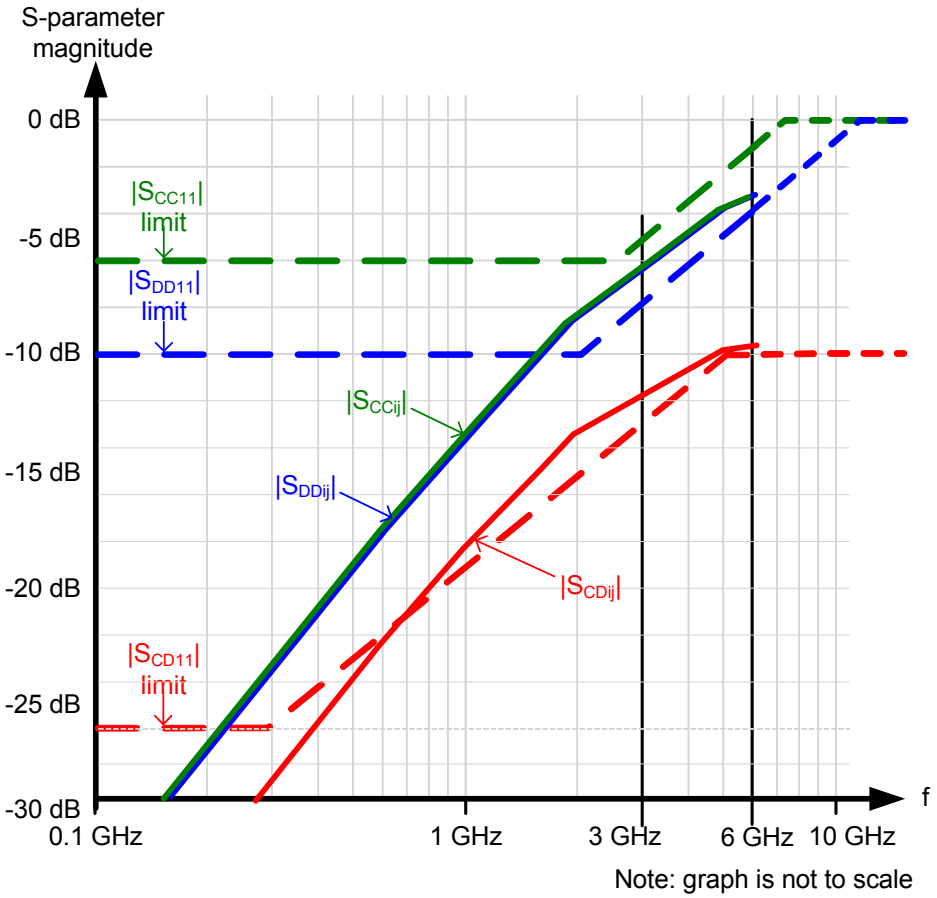


Figure 160 — Reference receiver device termination S-parameters for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The Touchstone model does not exactly match the $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in 5.8.5.7.2 at all frequencies, however, it is a reasonable approximation for use in simulations. See Annex G for a description of how the Touchstone model was created.

5.8.5.7.5 Reference receiver device termination characteristics for trained 12 Gbit/s

The termination characteristics of the reference receiver device for trained 12 Gbit/s are determined by the reference TxRx connection segments used in the simulations (see C.2). The reference transmitter presents an ideal termination at RR.

5.8.5.7.6 Stressed receiver device jitter tolerance test

5.8.5.7.6.1 Stressed receiver device jitter tolerance test overview for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

A receiver device shall pass the stressed receiver device jitter tolerance test described in this subclause.

The stressed receiver device jitter tolerance test for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s shall be applied at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) as a means to perform physical validation of predicted performance of the receiver device. Any implementation of the stressed signal generation hardware is permitted for the stressed receiver signal as long as it provides the ISI-stressed signal with jitter and noise as defined in this subclause.

Figure 161 shows the block diagram of the stressed receiver device jitter tolerance test.

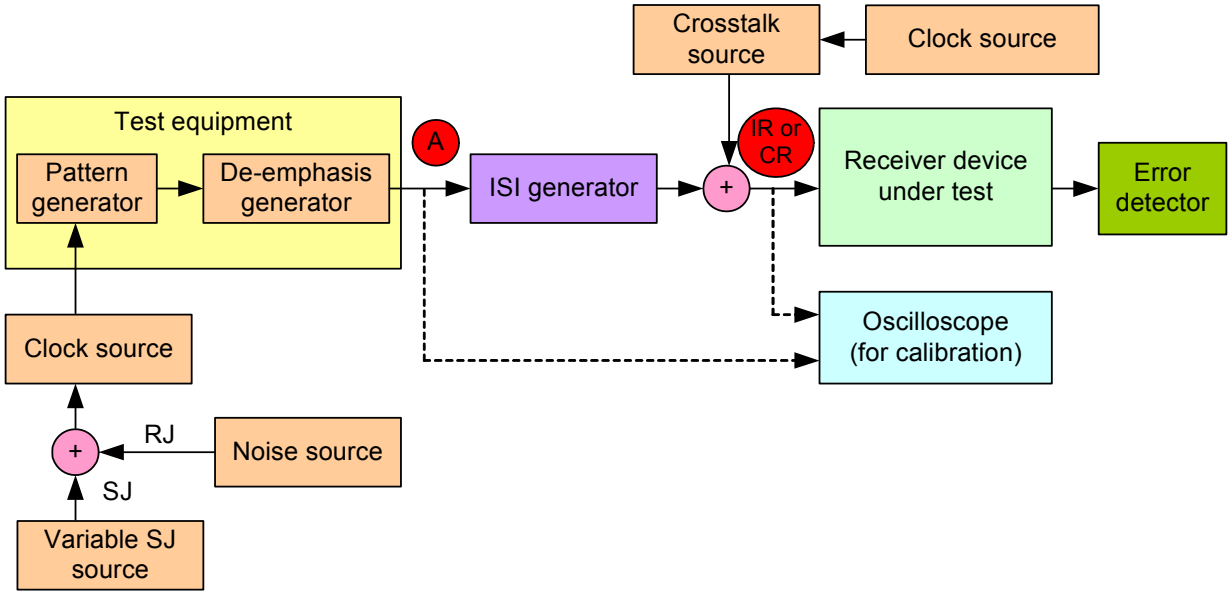


Figure 161 — Stressed receiver device jitter tolerance test block diagram for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The ISI generator shall be representative of, and at least as stressful as, the reference transmitter test load (see 5.6.5). The reference transmitter test load (see 5.6.5), with a nominal $|S_{DD21}|$ of -15 dB at (f_{baud} / 2), may be used as a component of the ISI generator.

The receiver device under test demonstrates its ability to compensate for channel intersymbol interference (ISI) representative of the reference transmitter test load (see 5.6.5) while subjected to the budgeted jitter and crosstalk sources.

Table 66 defines the stressed receiver device jitter tolerance test characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. Unless otherwise noted, characteristics are measured at IR (see 5.3.2) or CR (see 5.3.2) in figure 161.

Table 66 — Stressed receiver device jitter tolerance test characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Characteristic	Units	Minimum	Nominal	Maximum	Reference
TX peak to peak voltage [a]	mV(P-P)		850		5.8.4.6.1
Transmitter equalization [a]	dB		2		5.8.4.6.6
TX RJ [b] [c] [d]	UI	0.135 [e]	0.150 [f]	0.165 [g]	5.8.4.6.1
TX SJ [c]	UI	See figure 165 and figure 166			5.8.5.7.6.9
WDP at 6 Gbit/s [b] [h]	dB	13		14.5	
WDP at 3 Gbit/s [b] [h]	dB	7		8.5	
WDP at 1.5 Gbit/s [b] [h]	dB	4.5		6	
D24.3 eye opening [b] [i]	mV(P-P)	200	215	230	5.8.3.4
NEXT offset frequency [i] [j] [k]	ppm	2 500			
Total crosstalk amplitude [i] [k]	mV_{rms}	4			
Receiver device configuration [l]					

[a] For a characteristic with only a nominal value, the test setup shall be configured to be as close to that value as possible while still complying with other characteristics in this table.

[b] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.

[c] Measured at point A in figure 161.

[d] Measured after application of the JTF (see 5.8.3.2).

[e] 0.135 UI is 22.5 ps at 6 Gbit/s, 45 ps at 3 Gbit/s, and 90 ps at 1.5 Gbit/s.

[f] 0.150 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.

[g] 0.165 UI is 27.5 ps at 6 Gbit/s, 55 ps at 3 Gbit/s, and 110 ps at 1.5 Gbit/s.

[h] This value is obtained by simulation with SASWDP (see Annex B). BUJ and RJ shall be minimized for WDP simulations. The WDP value is a characterization of the signal output within the reference receiver device (see 5.8.5.7.3) after equalization.

[i] The repeating 0011b pattern or 1100b pattern (e.g., D24.3) eye opening pertains to the delivered signal at IR or CR. Figure 162 defines this value in an eye diagram.

[j] The NEXT source may use SSC modulation rather than have a fixed offset frequency.

[k] Observed with a histogram of at least 1 000 samples. Additional pseudo-random crosstalk shall be added, if needed, to meet the total crosstalk amplitude specification.

[l] All transmitter devices and receiver devices adjacent to the receiver device under test shall be active with representative traffic with their maximum amplitude and maximum frequency of operation.

Figure 162 shows the stressed receiver device jitter tolerance test repeating 0011b pattern or 1100b pattern (e.g., D24.3) eye opening for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

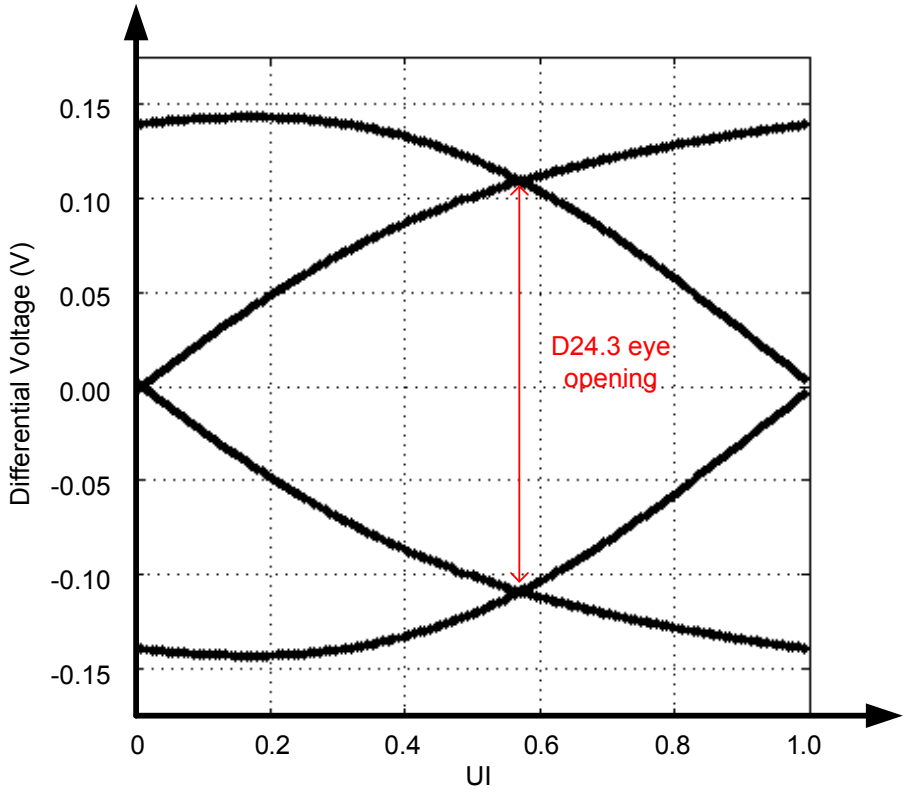


Figure 162 — Stressed receiver device jitter tolerance test D24.3 eye opening for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.8.5.7.6.2 Stressed receiver device jitter tolerance test procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The stressed receiver device jitter tolerance test procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.8.5.7.6.3;
2) calibrate the crosstalk source as specified in 5.8.5.7.6.4;
3) attach the test equipment and ISI generator and the crosstalk source to the receiver device under test;
4) configure the pattern generator to transmit a Train_Rx-SNW pattern (see SPL-4);
5) allow the receiver device to complete the Train_Rx-SNW;
6) configure the applied SJ as specified in 5.8.5.7.6.9;
7) configure the pattern generator to transmit CJTPAT (see Annex A); and
8) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

This procedure requires the receiver under test to train during Train_Rx-SNW as specified in SPL-4. This training may be performed by:

a) using the mechanisms defined in SPL-4; or
b) using an equivalent procedure.

The use of an equivalent procedure is outside the scope of this standard.

Table 67 defines the number of bits that shall be received with a certain number of errors to have a confidence level of 95 % that the BER is less than 10^{-12}.

Table 67 — Number of bits received per number of errors for desired BER

Number of errors	Number of bits
0	3.00×10^{12}
1	4.74×10^{12}
2	6.30×10^{12}
3	7.75×10^{12}
4	9.15×10^{12}
5	1.05×10^{13}

5.8.5.7.6.3 Test equipment and ISI generator calibration for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The test equipment and ISI generator calibration procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) ensure that the ISI generator has an $|S_{DD21}|$ comparable to that of the reference transmitter test load (see 5.6.5). $|S_{DD21}|$ delivered by the ISI generator shall be measured by observing the D24.3 eye opening at IR or CR as defined in table 66;
2) attach the test equipment and ISI generator to a zero-length test load, where its signal output is captured by an oscilloscope;
3) disable the crosstalk source;
4) disable the variable SJ source and the random noise source;
5) configure the pattern generator to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4);
6) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Waveform averaging shall be used to minimize the impact of measurement noise and jitter on the WDP calculations;
7) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to ‘SAS2_LDP’; and
8) adjust the ISI generator until the WDP is within the range defined in table 66 (see 5.8.5.7.6.1).

WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5.8.5.7.6.4 Crosstalk source calibration for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The crosstalk source calibration procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) attach the test equipment and ISI generator and the crosstalk source to a zero-length test load, where its signal output is captured by an oscilloscope;
2) disable the pattern generator;
3) enable the crosstalk source;
4) set the center frequency of the crosstalk source to be frequency offset from the pattern generator to sweep all potential relative phase alignments between the crosstalk source and the signal from the ISI generator;
5) generate a histograph of the signal delivered to the test equipment; and
6) adjust the crosstalk source until the crosstalk amplitude complies with table 66 (see 5.8.5.7.6.1).

5.8.5.7.6.5 Stressed receiver device jitter tolerance test procedure for trained 12 Gbit/s

The stressed receiver device jitter tolerance test procedure for 12 Gbit/s is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.8.5.7.6.6;
2) calibrate the crosstalk source as specified in 5.8.5.7.6.7;
3) attach the test equipment and ISI generator and the crosstalk generator to the receiver device under test;
4) configure the devices on the receiver device board to transmit and receive representative traffic, including the transmitter device associated with the receiver device under test;
5) configure the pattern generator to transmit a Train_Tx-SNW pattern (see SPL-4);
6) allow the receiver to complete the Train_Tx-SNW;
7) configure the pattern generator to transmit a Train_Rx-SNW pattern (see SPL-4);
8) allow the receiver to complete the Train_Rx-SNW;
9) configure the applied RJ as specified in 5.8.5.7.6.8;
10) configure the applied SJ as specified in 5.8.5.7.6.9;
11) configure the pattern generator to transmit CJTPAT (see Annex A); and
12) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

The configuration of the transmitter device associated with the receiver device under test may be performed after the receiver training completes.

This procedure requires the receiver under test to train during Train_Tx-SNW and Train_Rx-SNW as specified in SPL-4 (see figure 163). This training may be performed by:

a) using the mechanisms defined in SPL-4; or
b) using an equivalent procedure.

The test equipment shall be capable of adjusting its transmitter coefficients as requested by the receiver under test. The use of an equivalent procedure is outside the scope of this standard.

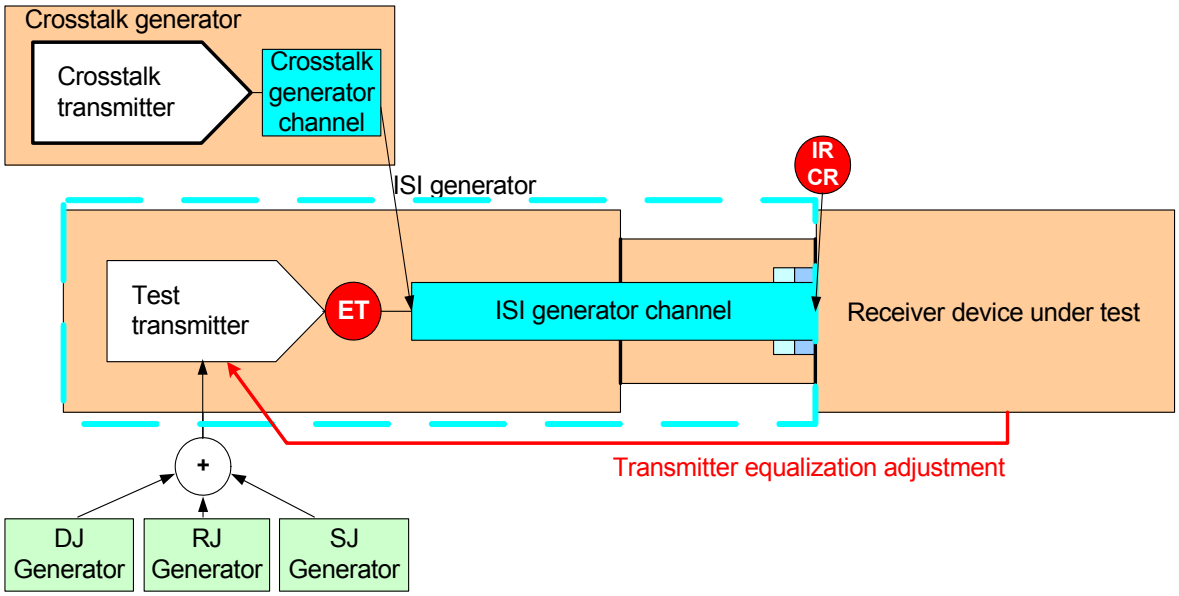


Figure 163 — Stressed receiver transmitter equalization adjustment for 12 Gbit/s

5.8.5.7.6.6 ISI generator calibration for trained 12 Gbit/s

The delivered signal for stressed receiver device jitter tolerance test for 12 Gbit/s (see 5.8.5.7.6) shall provide ISI characteristics defined in table 68.

The characteristics at ER shall be measured using end to end simulations (see 5.7.1 and Annex C).

To simplify de-embedding to ET, the peak to peak voltage may be measured from the output of the ISI generator's transmitter, if the ISI channel has insertion loss less than 1.5 dB at 10 MHz (e.g.,10 MHz represents effective D.C., excluding A.C. coupling). Using this method, the peak to peak voltage is computed by scaling down the measured amplitude by the loss of the ISI channel at 10 MHz. This simplified de-embedding method requires verification of the ISI channel insertion loss.

The effective ISI generator's transmitter output may include attenuators or power combiners. The characteristics of the ISI generator's transmitter, including transmitter circuit response to coefficient steps and coefficient preset settings, are measured including the attenuators or power combiners.

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter free reference transmitter with K_0 set to 1 (unit-less value) at the output of the ISI generator, using the ISI generator's output as the input of the reference transmitter, instead of the +1/-1 digitized stream (see figure 164).

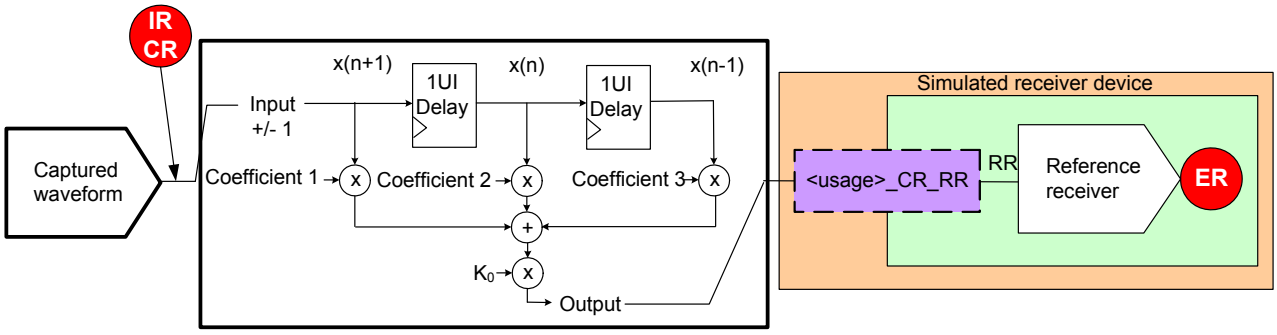


Figure 164 — Simulation of the reference transmitter from a captured signal

The ISI generator's transmitter device shall have the trained 12 Gbit/s transmitter characteristics (see 5.8.4.7). The ISI generator shall be capable of changing its equalization in response to the attached receiver device's back channel requests (see SPL-4). This may be performed using a duplex link as defined in SPL-4, or through the use of an equivalent procedure. The use of an equivalent procedure is outside the scope of this standard.

The ISI generator calibration procedure is as follows:

1) set the transmitter of the ISI generator to output no equalization (i.e., coefficient 1 set to zero, coefficient 2 set to one, coefficient 3 set to zero);
2) attach the test equipment and ISI generator to a zero-length test load;
3) disable:
   A) the crosstalk source;
   B) the RJ source;
   C) the DJ source;
   D) the SSC source; and
   E) the variable SJ source;
4) configure the pattern generator to transmit a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4);
5) set the transmitter peak to peak voltage to the characteristics of table 68;
6) configure the pattern generator to transmit IDLE dwords (see SPL-4);
7) capture the signal at IR or CR;
8) simulate signal characteristics and reference transmitter characteristics (see C.1), using reference <usage>_CR_RR channel models of the appropriate usage model (see C.2); and
9) adjust the ISI generator channel for end to end simulation characteristics defined in table 68.

Table 68 defines the characteristics measured in end to end simulation of the delivered signal for trained 12 Gbit/s stressed receiver device jitter tolerance test.

See the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3) used in table 68.

Table 68 — ISI generator characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Peak to peak voltage [a] [b]	mV(P-P)	850	1 000	ET (see 5.3.3)
Coefficient 1 (i.e., C1) [c] [d] [e]	V/V	-0.15	0	ET
Coefficient 3(i.e., C3) [c] [d] [f]	V/V	-0.3	0	ET
VMA [g] [h]	mV(P-P)	80		ET
Reference pulse response cursor peak to peak amplitude [i] [j]	mV(P-P)	125	145	ER (see 5.3.3)
Vertical eye opening to reference pulse response cursor ratio [j] [k] [l]	%	65	80	ER
DFE coefficient magnitude to reference pulse response cursor ratio [m]	%	5	50	ER

[a] The measurement shall be made with the ISI generator transmitter set to no equalization and a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4).

[b] The peak to peak voltage is adjusted as close as possible to the minimum limit.

[c] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[d] C2 = 1 - |C1| - |C3|.

[e] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] VMA = $2K_0$ (C1 + C2 + C3) V. See 5.8.4.7.3.

[h] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3)^2)^{0.5}$$

where:

C1’ and C3’ are values that satisfy the minimum VMA criterion.

[i] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 135.

[j] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the ISI generator’s transmitter.

[k] The vertical eye opening does not include crosstalk. Crosstalk representing FEXT is calibrated as specified in 5.8.5.7.6.7, while representative traffic is present during the test to provide NEXT crosstalk (see 5.8.5.7.6.5).

[l] The ISI generator is adjusted as close as possible to the maximum reference pulse response cursor and vertical eye opening to reference pulse response cursor ratio limits.

[m] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(d_i)) divided by the reference pulse response cursor (see 5.8.5.7.3)).

5.8.5.7.6.7 Crosstalk calibration for trained 12 Gbit/s stressed receiver device jitter tolerance test

Total peak to peak crosstalk noise shall be measured as defined in 5.7.4 at IR (see 5.3.3) or CR (see 5.3.3). The crosstalk is added to the simulation as a measured peak to peak amplitude at a cumulative probability of 10^{-6} (see 5.7.4). The characteristics of the crosstalk amplitude are defined in table C.5. The crosstalk shall be generated by a single transmitter with:

a) a minimum fixed offset frequency of 1 000 ppm; or
b) using SSC modulation rather than the fixed offset frequency.

5.8.5.7.6.8 Applied RJ for trained 12 Gbit/s stressed receiver device jitter tolerance test

The delivered signal for stressed receiver device jitter tolerance test (see 5.8.5.7.6.5) shall provide RJ characteristics defined in table 69.

Table 69 — RJ charateristics for trained 12 Gbit/s stressed receiver device tolerance test

Characteristic	Units	Minimum	Nominal	Maximum
RJ [a b c d]	UI	0.135 [e]	0.150 [f]	0.165 [g]

[a] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.
[b] Measured at ER, IR, or CR as shown in figure 164.
[c] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[d] Measured after application of the JTF (see 5.8.3.2).
[e] 0.135 UI is 11.25 ps at 12 Gbit/s.
[f] 0.150 UI is 12.5 ps at 12 Gbit/s.
[g] 0.165 UI is 13.75 ps at 12 Gbit/s.

5.8.5.7.6.9 Applied SJ

Figure 165 defines the applied SJ for trained receiver devices that do not support SSC.

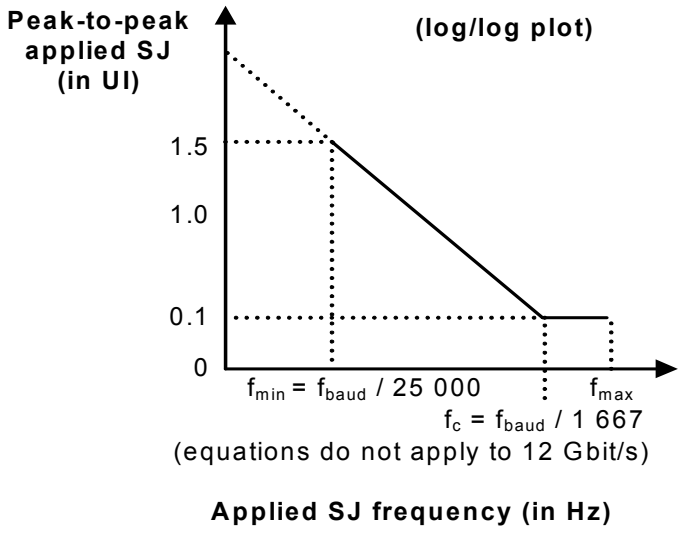


Figure 165 — Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s without SSC support

Table 70 defines f_{min}, f_c, and f_{max} for figure 165. f_{baud} is defined in table 36 (see 5.8.1).

Table 70 — f_{min}, f_c, and f_{max} for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s without SSC support

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz
6 Gbit/s	240 kHz	3 600 kHz	15 MHz
12 Gbit/s	240 kHz	3 600 kHz	15 MHz

Figure 166 defines the applied SJ for trained receiver devices that support SSC.

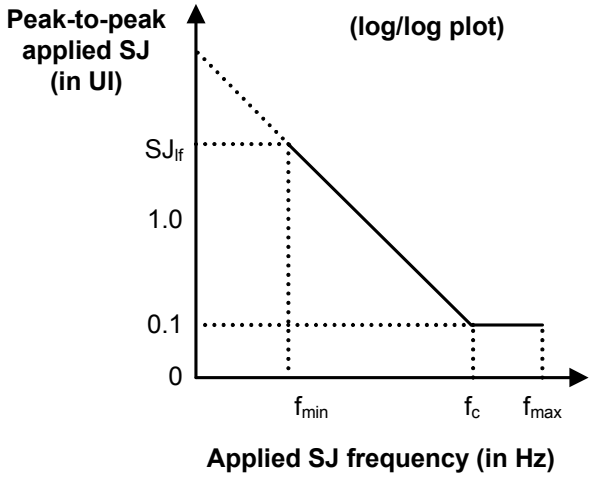


Figure 166 — Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s and 12 Gbit/s with SSC support

Table 71 defines f_{min}, f_c, f_{max}, and SJ_{lf} for figure 166.

Table 71 — f_{min}, f_c, f_{max}, and SJ_{lf} for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s with SSC support

Physical link rate	f_{min}	f_c	f_{max}	SJ_{lf}
1.5 Gbit/s	97 kHz	1.03 MHz	5 MHz	11.3 UI
3 Gbit/s	97 kHz	1.46 MHz	7.5 MHz	22.6 UI
6 Gbit/s	97 kHz	2.06 MHz	15 MHz	45.3 UI
12 Gbit/s	111 kHz	2.06 MHz	15 MHz	34.6 UI

5.8.5.8 Delivered signal characteristics for OOB signals

Table 72 defines the amplitude requirements of the OOB signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR (see 5.3) or CR (see 5.3)). These also serve as the required signal tolerance characteristics of the receiver device.

Table 72 — Delivered signal characteristics for OOB signals

Characteristic	Units	IR	CR
Minimum OOB burst amplitude [a], if SATA is not supported	mV(P-P)	240 [b]	
Minimum OOB burst amplitude [a], if SATA is supported	mV(P-P)	225 [c] [d]	N/A

[a] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst.
[b] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see ~~SPL-3~~SPL-4).
[c] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3) or 1.5 Gbit/s ALIGN (0) primitives (see SPL-4 and SATA).
[d] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.8.6 Spread spectrum clocking (SSC)

5.8.6.1 SSC overview

Spread spectrum clocking (SSC) is the technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions.

Phys transmit with SSC as defined in 5.8.6.2 and receive with SSC as defined in 5.8.6.3.

Table 73 defines the SSC modulation types.

Table 73 — SSC modulation types

SSC modulation type	Maximum SSC frequency deviation (SSC_{tol}) [a]				
	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s	22.5 Gbit/s
Center-spreading	+2 300 / -2 300 ppm			+1 000 / -1 000 ppm	+500 / -500 ppm
No-spreading	+0 / -0 ppm			+0 / -0 ppm	+0 / -0 ppm
Down-spreading	+0 / -2 300 ppm			+0 / -1 000 ppm	+0 / -500 ppm
SATA down-spreading [b]	+0 / -5 000 ppm			N/A	N/A

[a] This is in addition to the physical link rate accuracy and tolerance defined in table 38 (see 5.8.4.3) and table 56 (see 5.8.5.3).
[b] This is only used as a receiver parameter.

A phy may transmit with a different SSC modulation type than it receives (e.g., a phy may transmit with center-spreading while it receives with down-spreading).

If the SSC modulation type is not no-spreading, then the phy shall transmit within the specified maximum SSC frequency deviation with an SSC modulation frequency that is a minimum of 30 kHz and a maximum of 33 kHz.

The SSC modulation profile (e.g., triangular) is vendor specific, but should provide the maximum amount of EMI reduction. For center-spreading, the average amount of up-spreading (i.e., > 0 ppm) in the SSC modulation profile shall be the same as the average amount of down-spreading (i.e., < 0 ppm). The amount of asymmetry in the SSC modulation profile shall be less than 288 ppm.

NOTE 9 - 288 ppm is the rate of deletable primitives (see SPL-4) that are left over after accounting for the physical link rate accuracy. It is calculated as the deletable primitive rate defined in the SAS standard of 1 / 2 048 (i.e., 488 ppm) minus the width between the extremes of the physical link rate accuracy of +100 ppm to -100 ppm (i.e., 200 ppm).

SSC induced jitter is included in TJ at the transmitter output.

The slope of the frequency deviation should not exceed 850 ppm/µs when computed over any 0.27 µs ± 0.01 µs interval of the SSC modulation profile, after filtering of the transmitter device jitter output by a second order Butterworth low pass filter with a cutoff frequency of 3.7 MHz ± 0.2 MHz.

The slope is computed from the difference equation:

slope = (f(t) - f(t - 0.27 µs)) / 0.27 µs

where:

f(t) is the SSC frequency deviation expressed in ppm.

A ± 2 300 ppm triangular SSC modulation profile has a slope of approximately 310 ppm/µs and meets the informative slope specification. Other SSC modulation profiles (e.g., exponential) may not meet the slope requirement. A modulation profile that has a slope of ± 850 ppm/µs over 0.27 µs creates a residual jitter of approximately 16.7 ps (i.e., 0.10 UI at 6 Gbit/s) after filtering by the JTF. This consumes the total BUJ budget of the transmitter device, which does not allow the transmitter device to contribute any other type of BUJ.

Activation or deactivation of SSC on a physical link that is not OOB idle or negotiation idle (see SPL-4) shall be done without violating TJ at the transmitter device output after application of the JTF.

5.8.6.2 Transmitter SSC modulation

A SAS phy transmits with the SSC modulation types defined in table 74.

Table 74 — SAS phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Mandatory	Optional
While attached to a phy that does not support SSC	No-spreading	
While attached to a phy that supports SSC	No-spreading	Down-spreading

[a] SAS phys compliant with SAS-1.1 only transmitted with an SSC modulation type of no-spreading.

An expander phy transmits with the SSC modulation types defined in table 75.

Table 75 — Expander phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Mandatory	Optional
While attached to a SAS phy or expander phy that does not support SSC	No-spreading	
While attached to a SAS phy or expander phy that supports SSC	No-spreading	Center-spreading
While attached to a SATA phy	No-spreading	Down-spreading

[a] Expander phys compliant with SAS-1.1 only transmitted with an SSC modulation type of no-spreading.

A SAS device (see SPL-4) or expander device (see SPL-4) should provide independent control of SSC on each transmitter device. However, a SAS device or expander device may implement a common SSC transmit clock in which multiple transmitter devices do not have independent controls to enable and disable SSC. In such implementations, SSC may be disabled on a transmitter device that is already transmitting with SSC enabled if another transmitter device sharing the same common SSC transmit clock is required to perform SNW-1, SNW-2, SNW-3, or Final-SNW (see SPL-4) or SAS speed negotiation (see SPL-4).

If any transmitter device sharing a common SSC transmit clock enters a non-SSC transmission state (e.g., SNW-1, SNW-2, Final-SNW, Train_Tx-SNW, or Train_Rx-SNW with SSC disabled (see SPL-4)), then any transmitter device sharing that common SSC transmit clock may disable SSC. These transmitter devices are compliant with the SSC requirements even if the transmitter device has negotiated SSC enabled but its transmit clock has SSC disabled, provided that the transmitted signal does not exceed the maximum SSC frequency deviation limits specified in table 73.

The disabling and enabling of SSC may occur at any time (see 5.8.6.1) except during SNW-1, SNW-2, and Final-SNW (see SPL-4).

5.8.6.3 Receiver SSC modulation tolerance

SAS phys and expander phys support (i.e., tolerate) receiving with SSC modulation types defined in table 76.

Table 76 — Receiver SSC modulation types tolerance

Type of phys	SSC modulation type(s) [a] [b]	
	Mandatory	Optional [c]
Phys that support being attached to SATA phys	No-spreading and SATA down-spreading	Center-spreading and down-spreading
Phys that do not support being attached to SATA phys	No-spreading	Center-spreading and down-spreading

[a] This is in addition to the physical link rate accuracy tolerance defined in table 56 (see 5.8.5.3).
[b] Phys compliant with SAS-1.1 that do not support being attached to SATA devices were only required to tolerate an SSC modulation type of no-spreading. Phys compliant with SAS-1.1 that support being attached to SATA devices were only required to tolerate SSC modulation types of no-spreading and SATA down-spreading.
[c] If either the SSC modulation type of center-spreading or down-spreading is supported, then both shall be supported.

5.8.6.4 Expander device center-spreading tolerance buffer

Expander devices supporting the SSC modulation type of center-spreading shall support a center-spreading tolerance buffer for each connection with the buffer size defined in table 77. The expander device uses this buffer to hold any dwords that it receives during the up-spreading portions of the SSC modulation period that expander device is unable to forward as a result of:

a) the ECR (see SPL-4) and/or the transmitting expander phy is slower than the receiving expander phy; and
b) the dword stream does not include enough deletable primitives (see SPL-4).

The expander device unloads the center-spreading tolerance buffer during the down-spreading portions of the SSC modulation period when the receiving expander phy is slower than the ECR and the transmitting expander phy.

Table 77 — Expander device center-spreading tolerance buffer

Physical link rate	Minimum buffer size
22.5 Gbit/s	4 SPL packets
12 Gbit/s	14 dwords
6 Gbit/s	14 dwords
3 Gbit/s	8 dwords
1.5 Gbit/s	4 dwords

NOTE 10 - The minimum buffer size is based on the number of dwords or SPL packets that ~~may~~are ~~-~~allowed to be transmitted during half of the longest allowed SSC modulation period (i.e., half of the period indicated by 30 kHz) at the maximum physical link rate (i.e., +2 400 ppm for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; +1 100 ppm for 12 Gbit/s; or +600 ppm for 22.5 Gbit/s) minus the number that ~~may~~are ~~-~~allowed to be transmitted at the minimum physical link rate (i.e., -2 400 ppm for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; -1 100 ppm for 12 Gbit/s; or -600 ppm for 22.5 Gbit/s). This accounts for forwarding dwords in a connection (see SPL-4) that originated from a phy compliant with SAS-1.1 (i.e., a phy with an SSC modulation type of no-spreading and inserting deletable primitives at a rate supporting only the frequency accuracy).

Figure 167 shows an example of center-spreading tolerance buffer usage.

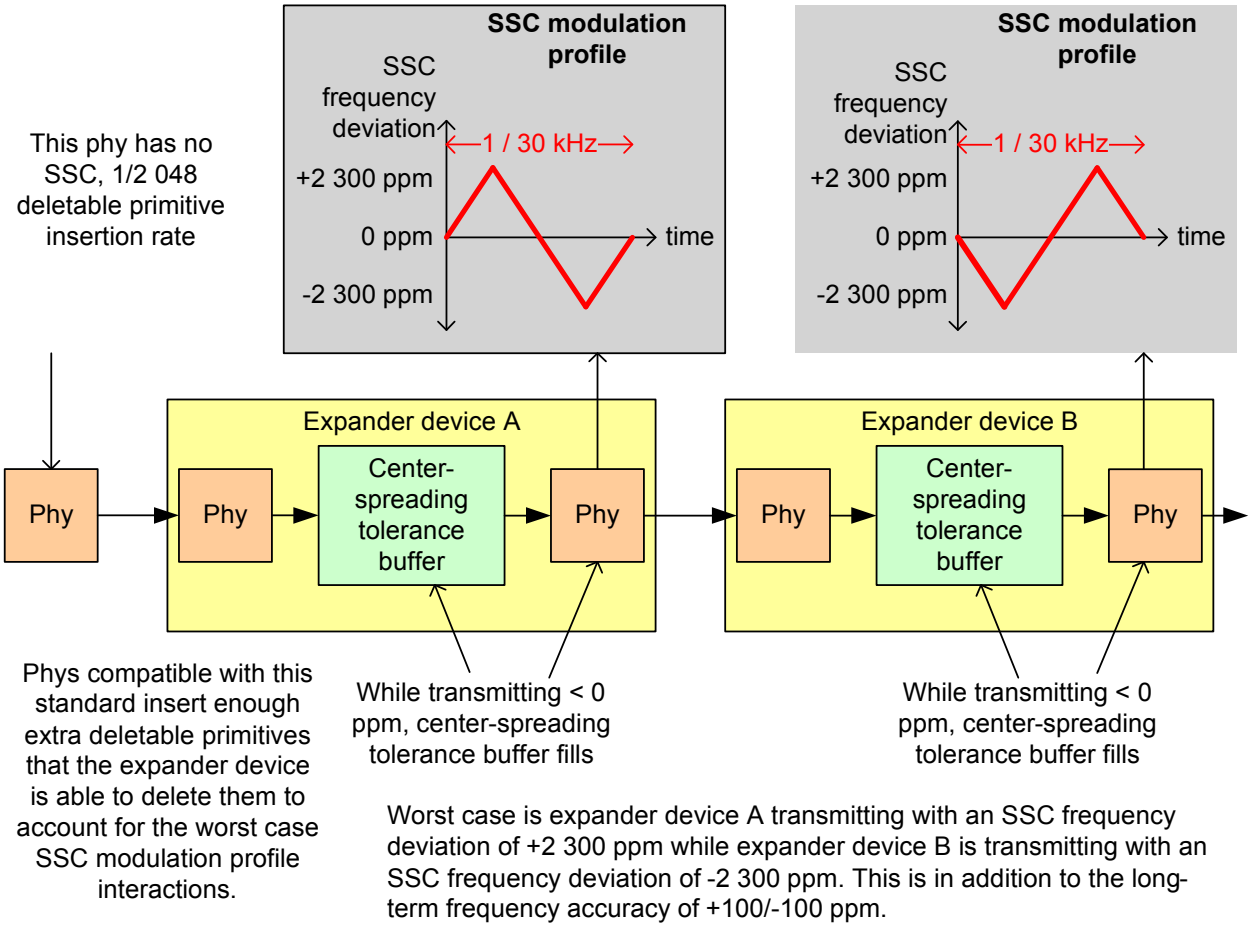


Figure 167 — Center-spreading tolerance buffer

5.8.7 Non-tracking clock architecture

Transceivers shall be designed with a non-tracking clock architecture (i.e., the receive clock derived from the bit stream received by the receiver device shall not be used as the transmit clock by the transmitter device).

Receiver devices that support SATA shall tolerate clock tracking by the SATA device. Receiver devices that do not support SATA are not required to tolerate clock tracking by the SATA device.

5.9 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices (see SPL-4) using the SAS Drive plug connector (see 5.4.3.3.1.1) or SAS MultiLink Drive plug connector (see 5.4.3.3.1.5) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 78 describes the output characteristics of the READY LED signal.

Table 78 — Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0 V \leq V_{OH} \leq 3.6 V$	$-100 \mu A < I_{OH} < 100 \mu A$
Asserted (LED on)	$I_{OL} = 15 mA$	$0 \leq V_{OL} \leq 0.225 V$

The READY LED signal behavior is defined in SPL-4.

NOTE 11 - SATA devices use the pin used by the READY LED signal (i.e., P11) for activity indication and disable staggered spin-up (see SATA). The output characteristics differ from those in table 78.

5.10 POWER DISABLE signal electrical characteristics

The POWER DISABLE signal, if implemented, may be used to disable power to the SAS target device circuitry.

If the POWER DISABLE signal is supported by a SAS target device with the SAS Drive plug connector (see 5.4.3.3.1.1) or SAS MultiLink Drive plug connector (see 5.4.3.3.1.5), then the SAS target device shall:

a) indicate that the POWER DISABLE signal is supported on the Protocol Specific Port Information VPD page and the IDENTFY address frame (see SPL-4);
b) allow power to be applied to the SAS target device circuitry if the POWER DISABLE signal is not connected on the SAS Drive backplane receptacle (see 5.4.3.3.1.3), SAS Drive cable receptacle (see 5.4.3.3.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.3.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.3.1.6);
c) allow power to be applied to the SAS target device circuitry if the POWER DISABLE signal is negated as defined in table 79;
d) disable power applied to the SAS target device circuitry if:
    1) the minimum negated hold time in table 79 is met; and
    2) the POWER DISABLE signal is asserted as defined in table 79;
e) perform the actions defined for power on (see SPL-4) if:
    1) the minimum negated hold time in table 79 is met;
    2) the POWER DISABLE signal is asserted as defined in table 79; and
    3) the POWER DISABLE signal transitions from asserted to negated;
    and
f) not respond to a change of the POWER DISABLE signal from negated to asserted or asserted to negated until the POWER DISABLE signal is held at the asserted or negated level for a minimum of 1 μs.

Table 79 describes the characteristics of the POWER DISABLE signal applied to the SAS target device.

Table 79 — Characteristics of the POWER DISABLE signal applied to the SAS target device

Characteristic	Units	Minimum	Typical	Maximum
Absolute maximum input voltage range	V	-0.5		3.6
Negated voltage (power enabled) [a] [b]	V	-0.5		0.7
Asserted voltage (power disabled) [c]	V	2.1		3.6
Driver sink/source current capability [b] [c]	μA	100		
POWER DISABLE asserted hold time [d] [e]	s	5.0		
POWER DISABLE negated hold time [d] [e]	s	30.0		

[a] The SAS target device shall allow power to be applied to the SAS target device circuitry if P3 is not connected on the SAS Drive backplane receptacle (see 5.4.3.3.1.3), SAS Drive cable receptacle (see 5.4.3.3.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.3.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.3.1.6).

[b] The POWER DISABLE signal should be actively negated. If the POWER DISABLE signal is not actively negated (e.g., open), then the specified values for POWER DISABLE signal negated voltage and driver sink current capability applied to the SAS target device do not apply.

[c] The POWER DISABLE signal shall be actively asserted.

[d] The hold time is the length of time the POWER DISABLE signal is asserted or negated. The length of time after the POWER DISABLE signal is asserted or negated until the disabling or allowing of power application to the SAS target device circuitry is vendor specific.

[e] The POWER DISABLE signal should not transition from negated to asserted or asserted to negated for the negated hold time:

a) after power is applied to the SAS Drive backplane receptacle (see 5.4.3.3.1.3), SAS Drive cable receptacle (see 5.4.3.3.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.3.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.3.1.6); or

b) after the detection of a hot plug event.

5.11 Out of band (OOB) signals

5.11.1 OOB signals overview

If D.C. mode is enabled, then OOB signals are low-speed signal patterns that do not appear in normal data streams. If optical mode is enabled, then OOB signals consist of a defined series of dwords. OOB signals consist of defined amounts of idle time followed by defined amounts of burst time. During the idle time, the physical link carries OOB idle. During the burst time, the physical link carries dwords. The signals are differentiated by the length of idle time between the burst times. OOB signals are not decoded unless dword synchronization has been lost (see SPL-4). Once high-speed data transfers are underway, the data pattern amplitude may fall to levels that are falsely detected as OOB signals. A phy shall either have D.C. mode enabled or optical mode enabled. The method to enable D.C. mode or optical mode is outside the scope of this standard.

SATA defines two OOB signals (i.e., COMINIT/COMRESET and COMWAKE). COMINIT and COMRESET are used in this standard interchangeably. Phys compliant with this standard identify themselves with an additional SAS specific OOB signal called COMSAS.

Table 80 defines the timing specifications for OOB signals.

Table 80 — OOB signal timing specifications

Parameter	Minimum	Nominal	Maximum	Comments
OOB Interval (OOBI) [a]	665.0$\overline{6}$ ps [b]	666.$\overline{6}$ ps [c]	668.2$\overline{6}$ ps [d]	The time basis for burst times and idle times used to create OOB signals.
COMSAS detect timeout	13.686 µs [e]			The minimum time a receiver device shall allow to detect COMSAS after transmitting COMSAS.

[a] OOBI is different than UI(OOB) defined in SATA (e.g., SAS has tighter physical link rate accuracy and different SSC frequency deviation). OOBI is based on:
A) 1.5 Gbit/s UI (see table 36 in 5.8.1);
B) physical link rate accuracy (see table 38 in 5.8.4.3); and
C) center-spreading SSC (see table 73 in 5.8.6.1).

[b] 665.0$\overline{6}$ ps equals 666.$\overline{6}$ ps × (1 - 0.002 4).

[c] 666.$\overline{6}$ ps equals 2 000 ps / 3.

[d] 668.2$\overline{6}$ ps equals 666.$\overline{6}$ ps × 1.002 4.

[e] 13.686 µs is 512 × 40 × Maximum OOBI.

To interoperate with interconnects compliant with SAS-1.1, phys should create OOB burst times and idle times based on the UI for 1.5 Gbit/s without SSC modulation. SAS-1.1 defined OOBI based on the nominal UI for 1.5 Gbit/s (see table 36 in 5.8.1) with physical link rate accuracy (see table 38 in 5.8.4.3) but not with SSC modulation (see table 73 in 5.8.6.1). Interconnects compliant with SAS-1.1 may have assumed phys had that characteristic.

5.11.2 Transmitting OOB signals

Table 81 describes the OOB signal transmitter requirements for the burst time, idle time, negation times, and signal times that are used to form each OOB signal.

Table 81 — OOB signal transmitter device requirements

Signal	Burst time	Idle time	Negation time	Signal time [a]
COMWAKE	160 OOBI [b]	160 OOBI [b]	280 OOBI [c]	2 200 OOBI [g]
COMINIT/COMRESET	160 OOBI [b]	480 OOBI [d]	800 OOBI [e]	4 640 OOBI [i]
COMSAS	160 OOBI [b]	1 440 OOBI [f]	2 400 OOBI [h]	12 000 OOBI [j]

[a] A signal time is six burst times plus six idle times plus one negation time.
[b] 160 OOBI is nominally 106.$\overline{6}$ ns (see table 80 in 5.11.1).
[c] 280 OOBI is nominally 186.$\overline{6}$ ns.
[d] 480 OOBI is nominally 320 ns.
[e] 800 OOBI is nominally 533.$\overline{3}$ ns.
[f] 1 440 OOBI is nominally 960 ns.
[g] 2 200 OOBI (e.g., COMWAKE) is nominally 1 466.$\overline{6}$ ns.
[h] 2 400 OOBI is nominally 1 600 ns.
[i] 4 640 OOBI (e.g., COMINIT/COMRESET) is nominally 3 093.$\overline{3}$ ns.
[j] 12 000 OOBI (e.g., COMSAS) is nominally 8 000 ns.

If D.C. mode is enabled, then an OOB idle consists of the transmission of D.C. idle.

If optical mode is enabled, then an OOB idle consists of repetitions of the following steps:

1) transmission of six OOB_IDLE primitives with either starting disparity at 3 Gbit/s; and
2) transmission of up to 512 data dwords (e.g., two data dwords for COMWAKE idle time, 18 data dwords for COMINIT/COMRESET idle time, and 66 data dwords for COMSAS idle time) set to 0000_0000h that are 8b10b encoded, scrambled, and transmitted at 3 Gbit/s.

An OOB burst consists of:

a) if D.C. mode is enabled, then transmission of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) or ALIGN (0) primitives with either starting disparity. The OOB burst should consist of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at 1.5 Gbit/s; or
b) if optical mode is enabled, then transmission of ALIGN (3) primitives with either starting disparity at 3 Gbit/s.

To transmit an OOB signal, the transmitter device shall:

1) transmit OOB idle for an idle time;
2) transmit an OOB burst for a burst time; and
3) repeat steps 1) and 2) five additional times.

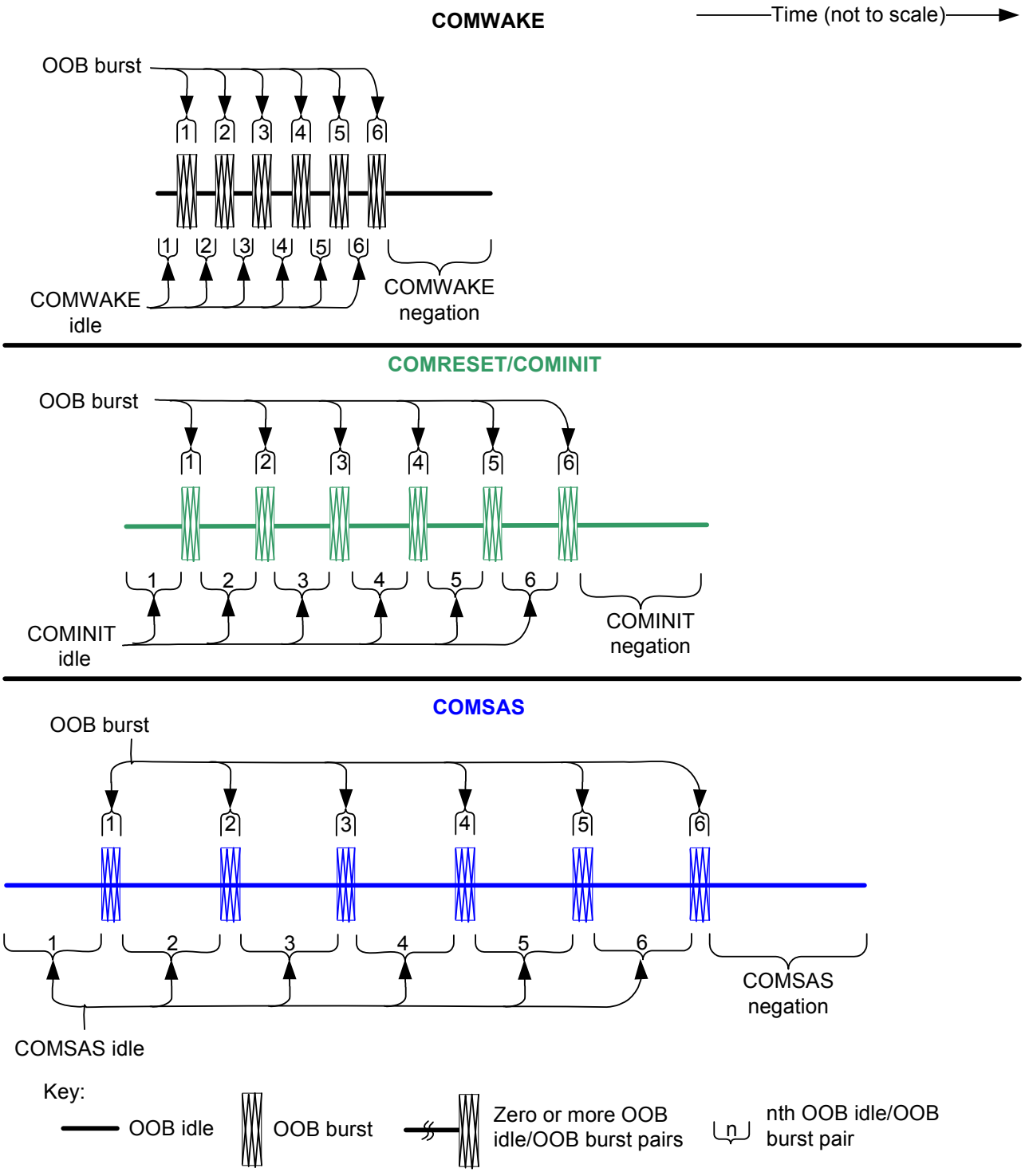
The transmitter device shall then transmit OOB idle for an OOB signal negation time.

The transmitter device shall use signal output levels during burst time and idle time as described in 5.8.4.8.

If D.C. mode is enabled, then the repeating 0011b pattern or 1100b pattern (e.g., D24.3) or ALIGN (0) primitives (see SPL-4) used in OOB signals shall be transmitted and the OOB burst is only required to generate an envelope for the detection circuitry, as required for any signaling that may be A.C. coupled. A burst of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at 1.5 Gbit/s is equivalent to a square wave pattern that has a one for two OOBI and a zero for two OOBI. A transmitter may use this square wave pattern for the OOB burst. The start of the pattern may be one or zero. The signal rise and fall times:

a) shall be greater than (i.e., slower) or equal to the minimum (i.e., fastest) rise and fall times allowed by the fastest supported physical link rate of the transmitter device (see table 40 in 5.8.4.4); and
b) shall be less than (i.e., faster) or equal to the maximum (i.e., slowest) rise and fall times allowed at 1.5 Gbit/s.

Figure 168 describes OOB signal transmission.



Note: OOB idle is shown here as a neutral signal for visual clarity only.

Figure 168 — OOB signal transmission

5.11.3 Receiving OOB signals

Table 82 describes the OOB signal receiver device requirements for detecting burst times, assuming T_{burst} is the length of the detected burst time. The burst time is not used to distinguish between signals.

Table 82 — OOB signal receiver device burst time detection requirements

Signal [a]	may detect	shall detect
COMWAKE	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns
COMINIT/COMRESET	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns
COMSAS	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns

[a] Each burst time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 81 in 5.11.2).

Table 83 describes the OOB signal receiver device requirements for detecting idle times, assuming T_{idle} is the length of the detected idle time.

Table 83 — OOB signal receiver device idle time detection requirements

Signal	may detect	shall detect	shall not detect
COMWAKE [a]	35 ns ≤ T_{idle} < 175 ns	101.3 ns ≤ T_{idle} ≤ 112 ns	T_{idle}< 35 ns or $T_{idle} \geq$ 175 ns
COMINIT/ COMRESET [b]	175 ns ≤ T_{idle} < 525 ns	304 ns ≤ T_{idle} ≤ 336 ns	T_{idle} < 175 ns or $T_{idle} \geq$ 525 ns
COMSAS [c]	525 ns ≤ T_{idle} < 1 575 ns	911.7 ns ≤ T_{idle} ≤ 1 008 ns	T_{idle} < 525 ns or $T_{idle} \geq$ 1 575 ns

[a] COMWAKE idle time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 81 in 5.11.2).
[b] COMINIT/COMRESET idle time is transmitted as 480 OOBI, which is nominally 320 ns.
[c] COMSAS idle time is transmitted as 1 440 OOBI, which is nominally 960 ns.

Table 84 describes the OOB signal receiver device requirements for detecting negation times, assuming T_{idle} is the length of the detected idle time.

Table 84 — OOB signal receiver device negation time detection requirements

Signal	shall detect
COMWAKE [a]	T_{idle} > 175 ns
COMINIT/COMRESET [b]	T_{idle} > 525 ns
COMSAS [c]	T_{idle} > 1 575 ns

[a] COMWAKE negation time is transmitted as 280 OOBI, which is nominally 186.$\overline{6}$ ns (see table 81 in 5.11.2).
[b] COMINIT/COMRESET negation time is transmitted as 800 OOBI, which is nominally 533.$\overline{3}$ ns.
[c] COMSAS negation time, which is transmitted as 2 400 OOBI, which is nominally 1 600 ns.

If D.C. mode is enabled, then a SAS receiver device shall detect OOB bursts formed from any of the following:

a) D24.3 characters (see SPL-4) at 1.5 Gbit/s;
b) ALIGN (0) primitives (see SPL-4) at 1.5 Gbit/s; or
c) ALIGN (0) primitives at 3 Gbit/s.

NOTE 12 - Detection of ALIGN (0) primitives at 3 Gbit/s provides interoperability with transmitter devices compliant with SAS-1.1.

If D.C. mode is enabled, then a SAS receiver device shall not qualify the OOB burst based on the characters received.

If optical mode is enabled, then a SAS receiver device shall detect OOB bursts formed from ALIGN (3) primitives at 3 Gbit/s.

5.11.4 Transmitting the SATA port selection signal

The SATA port selection signal shown in figure 169 causes the attached SATA port selector (see SPL-4) to select the attached phy (i.e., one of the SATA port selector's host phys) as the active phy (see SATA).

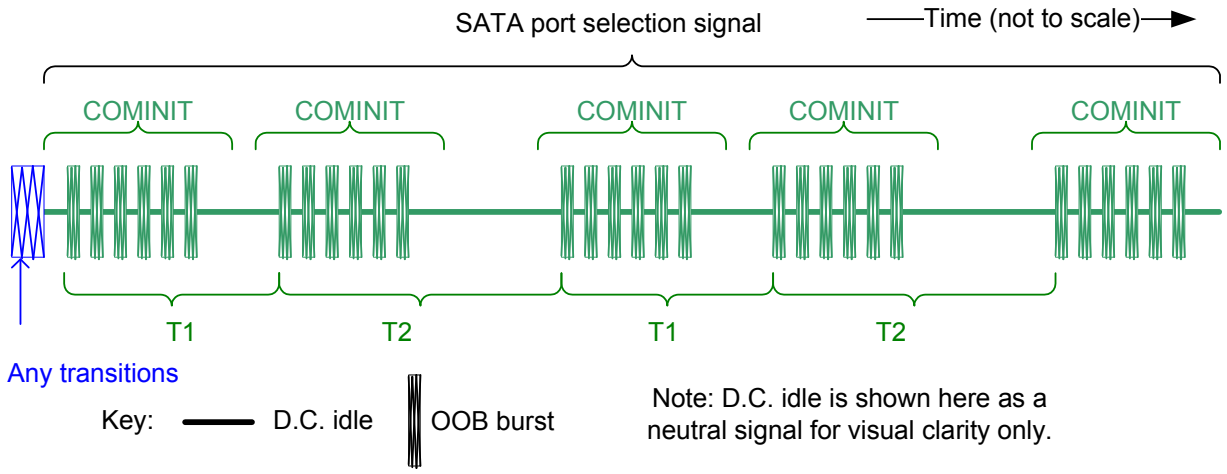


Figure 169 — SATA port selection signal

The SATA port selection signal shall be composed of five COMINIT signals, each starting a specified time interval, T1 or T2, as shown in figure 169, after the start of the OOB burst portion of the previous COMINIT signal. The values of T1 and T2 shall be as shown in table 85.

Table 85 — SATA port selection signal transmitter device requirements

Parameter	Time
T1	3×10^6 OOBI [a]
T2	12×10^6 OOBI [b]

[a] 3×10^6 OOBI is nominally 2 ms (see table 80 in 5.11.1).
[b] 12×10^6 OOBI is nominally 8 ms.

See SPL-4 for information on usage of the SATA port selection signal.

Annex A
(normative)

Jitter tolerance pattern (JTPAT)

The jitter tolerance pattern (JTPAT) consists of:

1) a long run of low transition density pattern;
2) a long run of high transition density pattern; and
3) another short run of low transition density pattern.

The transitions between the pattern segments stress the receiver. The JTPAT is designed to contain the phase shift in both polarities, from zero to one and from one to zero. The critical pattern sections with the phase shifts are underlined in table A.1 and table A.2.

Table A.1 shows the JTPAT when there is positive running disparity (RD+) (see SPL-4) at the beginning of the pattern. The 8b and 10b values of each character (see SPL-4) are shown.

Table A.1 — JTPAT for RD+

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD+
		10 0001 1100b	01 1110 0011b	10 0001 1100b	01 1110 0011b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D20.3 (74h)	RD-
		10 0001 1100b	01 1110 0011b	10 0001 1100b	00 1011 1100b	
	The above dword containing phase shift 111 0000 1011b is sent one time					
42	RD-	D30.3 (7Eh)	D11.5 (ABh)	D21.5 (B5h)	D21.5 (B5h)	RD+
		01 1110 0011b	11 0100 1010b	10 1010 1010b	10 1010 1010b	
	The above dword containing phase shift 000 1111 0100b is sent one time					
43 to 54	RD+	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	RD+
		10 1010 1010b	10 1010 1010b	10 1010 1010b	10 1010 1010b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD+	D21.5 (B5h)	D30.2 (5Eh)	D10.2 (4Ah)	D30.3 (7Eh)	RD+
		10 1010 1010b	10 0001 0101b	01 0101 0101b	01 1110 0011b	
	The above dword containing phase shift 0101 0000b and 1010 1111b is sent one time					

If the same 8b characters specified in table A.1 are used when there is negative running disparity (RD-) at the beginning of the pattern, then the resulting 10b pattern is different than the positive running disparity for the same 8b character and does not provide the critical phase shifts. To achieve the same phase shift effects with RD-, a different 8b pattern is required. Table A.2 shows the JTPAT when there is negative running disparity (RD-) at the beginning of the pattern. The 8b and 10b values of each character are shown.

Table A.2 — JTPAT for RD-

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD-
		01 1110 0011b	10 0001 1100b	01 1110 0011b	10 0001 1100b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D11.3 (6Bh)	RD+
		01 1110 0011b	10 0001 1100b	01 1110 0011b	11 0100 0011b	
	The above dword containing phase shift 000 1111 0100b is sent one time					
42	RD+	D30.3 (7Eh)	D20.2 (54h)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		10 0001 1100b	00 1011 0101b	01 0101 0101b	01 0101 0101b	
	The above dword containing phase shift 111 0000 1011b is sent one time					
43 to 54	RD-	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		01 0101 0101b	01 0101 0101b	01 0101 0101b	01 0101 0101b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD-	D10.2 (4Ah)	D30.5 (BEh)	D21.5 (B5h)	D30.3 (7Eh)	RD-
		01 0101 0101b	01 1110 1010b	10 1010 1010b	10 0001 1100b	
	The above dword containing phase shift 10101111b and 01010000b is sent one time					

The compliant jitter tolerance pattern (CJTPAT) is the JTPAT for RD+ (see table A.1) and RD- (see table A.2) included as the payload in an SSP DATA frame or an SMP frame. A phy or test equipment transmitting CJTPAT outside connections may transmit it with fixed content. See SPL-4.

Annex B
(normative)

SASWDP

SASWDP is a MATLAB program used for transmitter device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.8.4.6.1) and for receiver device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.8.5.7.6). Several files including SASWDP.m and SASWDP_testcase.m are included in the SAS2_1. zip directory of SAS4.zip. SASWDP.m includes comments within the file explaining input requirements and outputs of the script. Equivalent simulation programs may be used if they lead to the same results.

Annex C
(normative)

End to end simulation for trained 12 Gbit/s

C.1 Detailed end to end simulation procedure description for trained 12 Gbit/s

The trained 12 Gbit/s simulation model is based on a die to die insertion loss of approximately 24 dB as shown in .

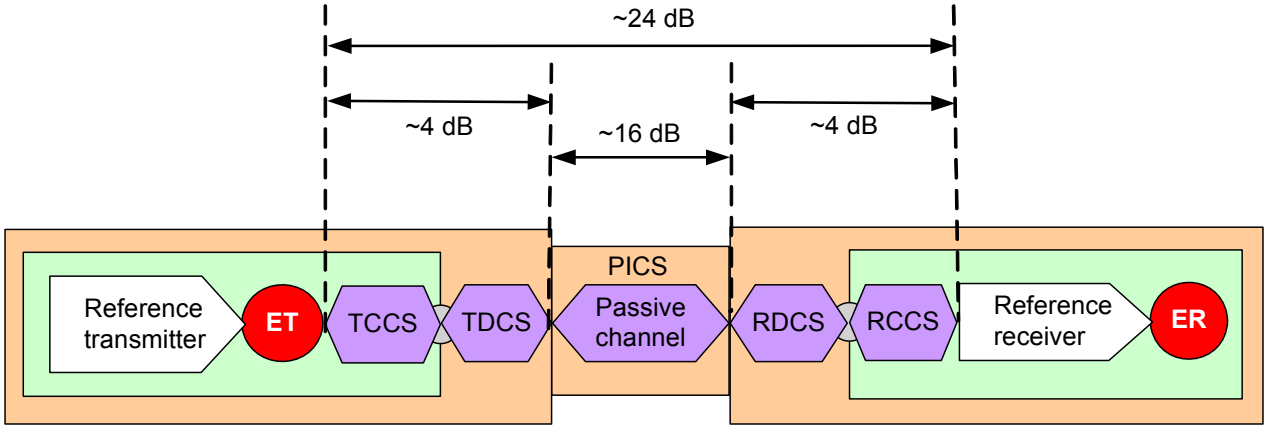


Figure C.1 — Trained 12Gbit/s die to die insertion loss model

The following procedure describes the end to end simulation process:

1) extract the un-equalized pulse response between ET (see 5.3.3) and RR (see 5.5.6) from:
   a) the captured signal into a zero-length test load or measured transfer function; and
   b) the reference transfer functions of the appropriate end to end simulation diagram (see C.2);
2) compute the reference transmitter equalization (see 5.7.3);
3) compute reference receiver DFE equalization (see 5.8.5.7.3);
4) compute an equalized pulse response by applying the reference transmitter equalization and the reference receiver DFE equalization to the un-equalized pulse response between ET and RR;
5) compute the vertical eye opening at the sampling instants defined by a reference sampling clock (see figure 135), for a BER of 10^{-15} assuming 8b10b data, using the equalized pulse response and the asynchronous crosstalk from all significant crosstalk sources;
6) measure the peak to peak reference pulse response cursor from the equalized pulse response (see figure 135); and
7) compute the vertical eye opening to reference pulse response cursor ratio.

Crosstalk information is provided as:

a) crosstalk transfer functions; or
b) a crosstalk signal amplitude that is met or exceeded at a cumulative probability of 10^{-6} (see 5.7.2).

When crosstalk information is provided as crosstalk transfer functions, the vertical eye opening is simulated at a BER of 10^{-15}, using the following procedure:

1) connect asynchronous reference transmitters to generate crosstalk according to the appropriate end to end simulation diagram (see C.2);
2) set the characteristics of the crosstalk transmitters per table C.1;
3) simulate the resulting amplitude due to crosstalk; and
4) compute the vertical eye opening at a BER of 10^{-15}.

Table C.1 — Crosstalk transmitter characteristics

Characteristic	Units	Value
Minimum peak to peak voltage (V_{P-P})	mV(P-P)	850 [a]
Output gain (K_0)	V/V	0.425 [a]
Rise/fall time [b]	ps	25 [a]
Differential impedance (nominal)	Ω	100
Common mode impedance (nominal)	Ω	25
Coefficient 1	V/V	See [a]
Coefficient 2	V/V	See [a]
Coefficient 3	V/V	See [a]

[a] Peak to peak voltage, rise/fall time, and coefficients should match the characteristics of the transmitter device used for the TxRx connection segment under test after reference transmitter equalization (see 5.7.3).

[b] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-4).

If crosstalk information is provided as a signal amplitude at a cumulative probability of 10^{-6}, then the vertical eye opening is computed by summing:

a) the simulated ISI not equalized by the transmitter equalization and receiver DFE equalization, at a BER of 10^{-15} assuming 8b10b data; and
b) the total crosstalk at a cumulative probability of 10^{-6}, scaled by the maximum gain of the TxRx connection segment between the crosstalk measurement point and the reference receiver input.

The maximum gain of the TxRx connection segment between the crosstalk measurement point and the reference receiver input is computed by simulation using the following procedure:

1) connect a reference transmitter to the TxRx connection segment between the crosstalk measurement point and the reference receiver input;
2) terminate the TxRx connection segment on the receiver end;
3) set the reference transmitter coefficient 1 to zero, coefficient 2 to one, coefficient 3 to zero and K_0 (see 5.8.4.7.3) to 0.5; and
4) compute the maximum gain as the maximum peak to peak voltage at the output of the TxRx connection segment, assuming 8b10b data.

C.2 Trained 12 Gbit/s usage models, S-parameter files, and crosstalk amplitude

C.2.1 Transmitter device connected to a separable passive TxRx connection segment

Table C.2 defines the S-parameter files for a transmitter device connected to a separable passive TxRx connection.

Table C.2 — S-parameter files for transmitter devices connected to a separable TxRx connection segment

End to end simulation type	S-parameter files [a] [b] [c]	Description of S-parameter files	Measurement point
Transmitter device connected to a separable TxRx connection segment (from SAS target device)	LongPassiveD2H_ITs_IR.s4p LongPassiveD2H_CR_RR.s4p	TxRx connection channel Rx initiator/expander device channel	IT, IT_S, CT, or CT_S
	LongPassiveD2H_ET_ITs_rev.s4p LongPassiveD2H_ITs_IR_NEXTx.s4p LongPassiveD2H_ITs_IR_FEXTx.s4p LongPassiveD2H_CR_RR_NEXTx.s4p LongPassiveD2H_CR_RR_FEXTx.s4p	Rx initiator/expander device NEXT Tx channel TxRx connection NEXT channels TxRx connection FEXT channels Rx initiator/expander device NEXT channels Rx initiator/expander device FEXT channels	
Transmitter device connected to a separable TxRx connection segment (to SAS target device)	LongPassiveH2D_ITs_IR.s4p LongPassiveH2D_CR_RR.s4p	TxRx connection channel Rx target device channel	IT, IT_S, CT, or CT_S
	LongPassiveH2D_ET_ITs_rev.s4p LongPassiveH2D_ITs_IR_NEXTx.s4p LongPassiveH2D_ITs_IR_FEXTx.s4p LongPassiveH2D_CR_RR_NEXTx.s4p LongPassiveH2D_CR_RR_FEXTx.s4p	Rx target device NEXT Tx channel TxRx connection NEXT channels TxRx connection FEXT channels Rx target device NEXT channels Rx target device FEXT channels	

[a] NEXTx and FEXTx indicate multiple aggressor channels.
[b] See figure 134 for a description of the NEXT and FEXT extraction.
[c] The <usage>_ET_ITs_rev.s4p transfer function may be calculated by de-embedding (see F.6)

Figure C.2 shows the usage models for a transmitter device connected to a separable passive TxRx connection.

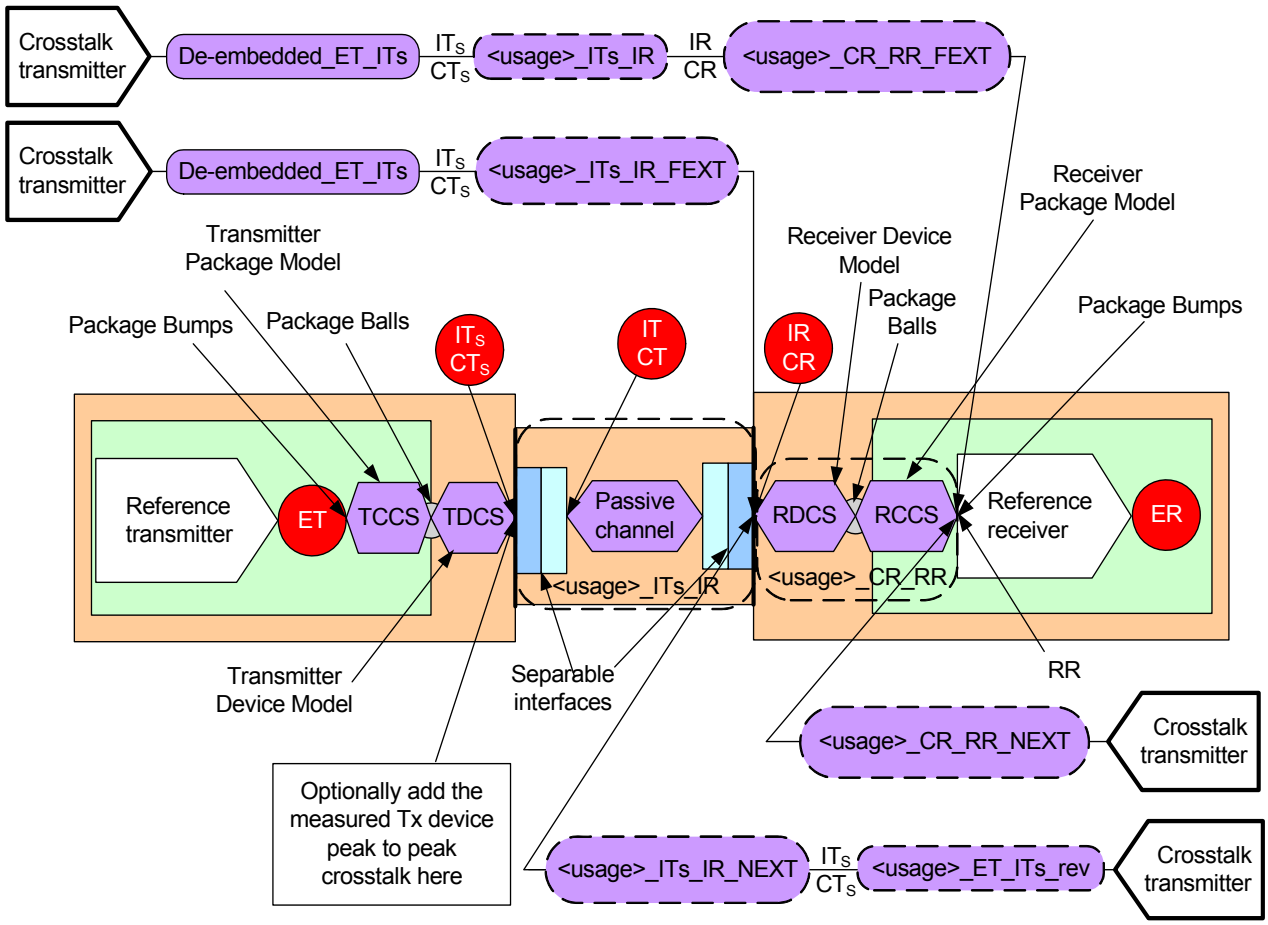


Figure C.2 — Transmitter device end to end simulation diagram that includes a separable TxRx connection segment

C.2.2 Transmitter device connected to a non-separable passive TxRx connection segment

Table C.3 defines the S-parameter files for a transmitter device connected to a non-separable passive TxRx connection.

Table C.3 — S-parameter files for transmitter devices connected to a non-separable TxRx connection segment

End to end simulation type	S-parameter files [a] [b] [c]	Description of S-parameter files	Measurement point
Transmitter device connected to a non-separable TxRx connection segment (from SAS target device) [d]	LongPassiveD2H_IR_RR.s4p	Rx initiator/expander device channel	IT, IT_S, CT, or CT_S
	LongPassiveD2H_IR_RR_NEXTx.s4p LongPassiveD2H_IR_RR_FEXTx.s4p	Rx initiator/expander device NEXT channels Rx initiator/expander device FEXT channels	
Transmitter device connected to a non-separable TxRx connection segment (to SAS target device) [e]	LongPassiveH2D_CR_RR.s4p	Rx target device channel	IT, IT_S, CT, or CT_S
	LongPassiveH2D_CR_RR_NEXTx.s4p LongPassiveH2D_CR_RR_FEXTx.s4p	Rx target device NEXT channels Rx target device FEXT channels	

[a] NEXTx and FEXTx indicate multiple aggressor channels.
[b] See figure 134 for a description of the NEXT and FEXT extraction.
[c] The <usage>_ET_ITs_rev.s4p transfer function may be calculated by de-embedding (see F.6)
[d] See figure C.3.
[e] See figure C.4.

Figure C.3 shows the target device to initiator device and target device to expander device usage models (i.e., from target device usage model) for a transmitter device connected to a non-separable passive TxRx connection.

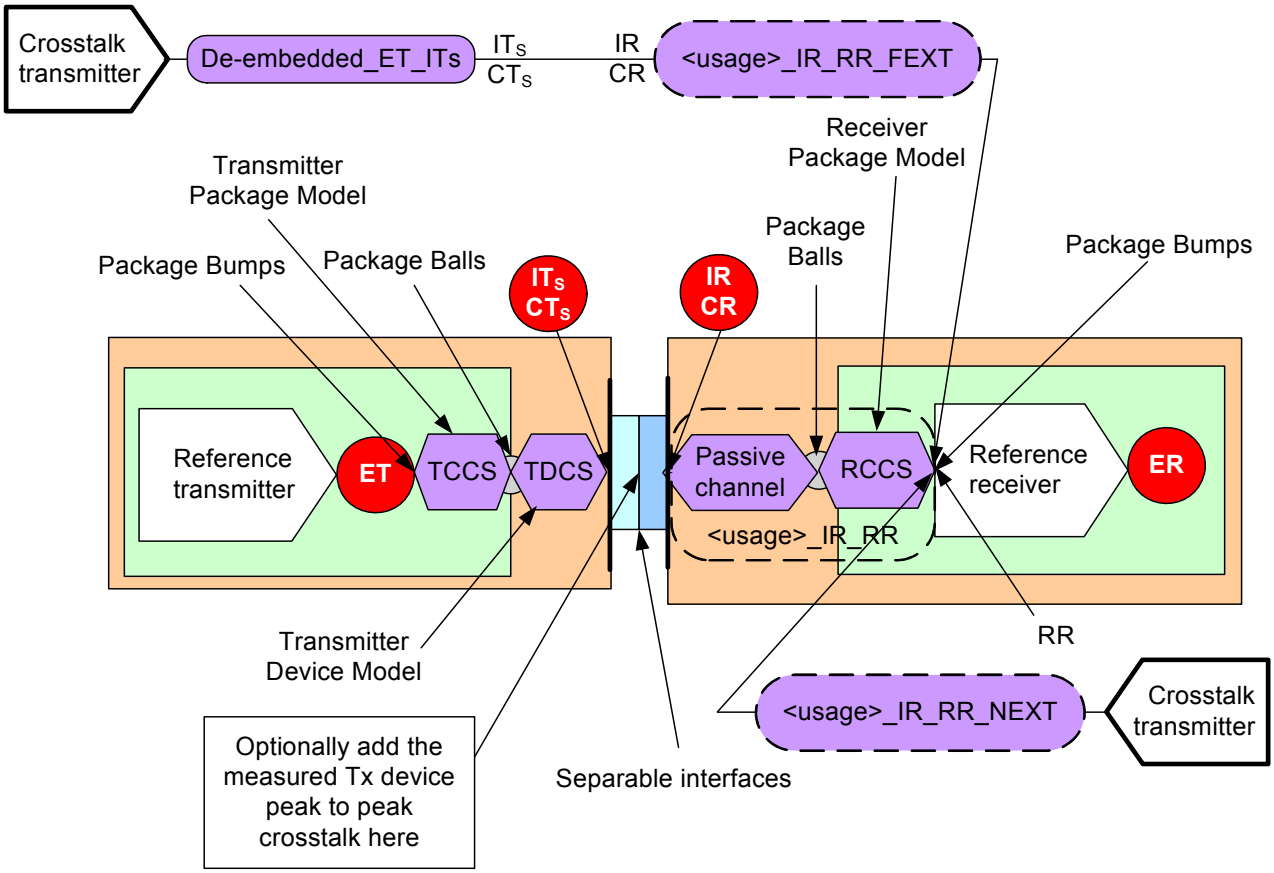


Figure C.3 — End to end simulation diagram of the from target device usage model for a transmitter device connected to a non-separable TxRx connection segment

Figure C.4 shows the initiator device to target device and expander device to target device usage models (i.e., to target device usage model) for a transmitter device connected to a non-separable passive TxRx connection.

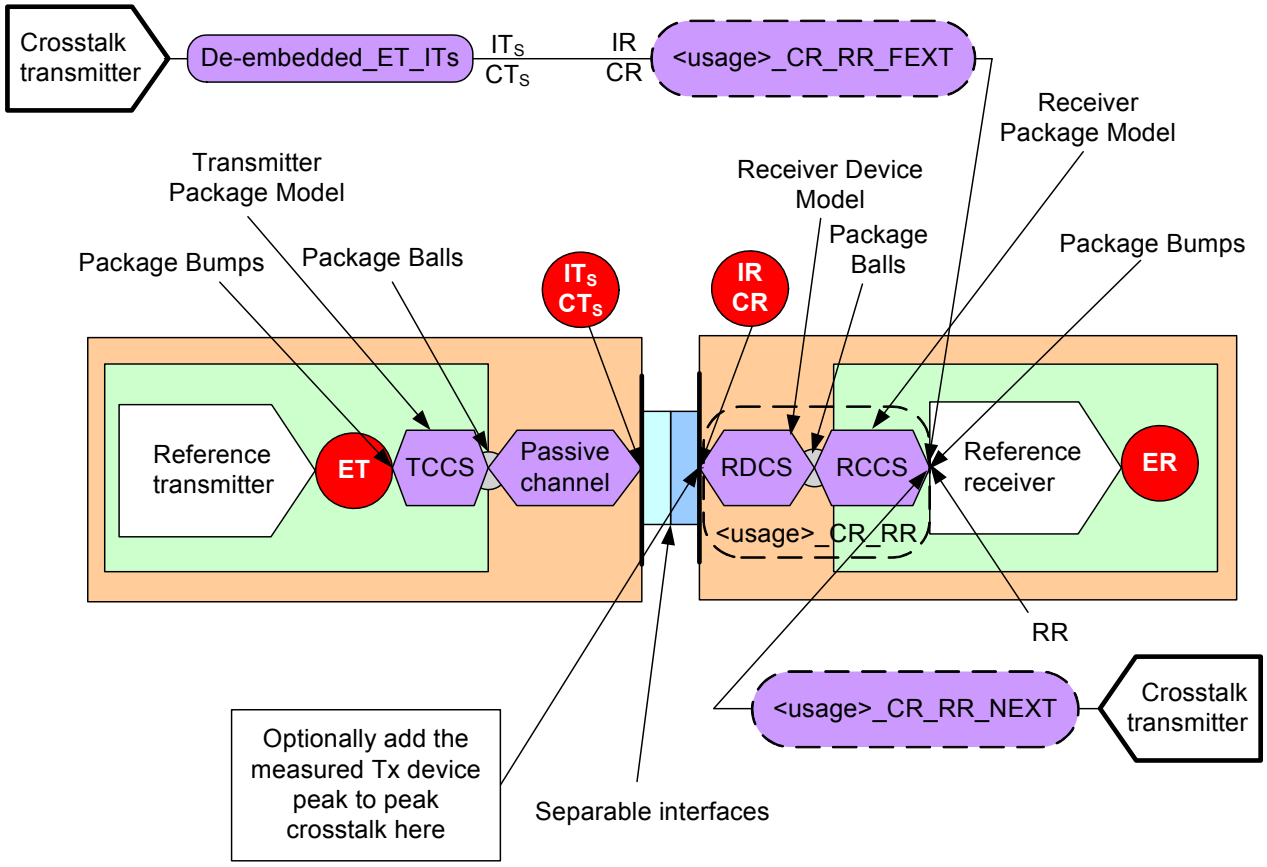


Figure C.4 — End to end simulation diagram of the to target device usage model for a transmitter device connected to a non-separable TxRx connection segment

C.2.3 TxRx connection segment

Table C.4 defines the S-parameter files to verify compliance of a TxRx connection segment.

Table C.4 — S-parameter files for a TxRx connection segment

End to end simulation type [a]	S-parameter files [a] [b] [c]	Description of S-parameter files
TxRx connection segment (SAS target device to SAS initiator device or SAS target device to SAS expander device)	LongPassiveD2H_ET_ITs.s4p LongPassiveD2H_CR_RR.s4p	Tx target device channel Rx initiator/expander device channel
	LongPassiveD2H_ET_ITs_NEXTx.s4p LongPassiveD2H_ET_ITs_FEXTx.s4p LongPassiveD2H_CR_RR_NEXTx.s4p LongPassiveD2H_CR_RR_FEXTx.s4p LongPassiveD2H_ET_ITs_rev.s4p	Tx target device NEXT channels Tx target device FEXT channels Rx initiator/expander device NEXT channels Rx initiator/expander device FEXT channels Rx initiator/expander device NEXT Tx channel
TxRx connection segment (SAS initiator device to SAS target device or SAS expander device to SAS target device)	LongPassiveH2D_ET_ITs_rev.s4p LongPassiveH2D_CR_RR.s4p	Tx initiator/expander device channel Rx target device channel
	LongPassiveH2D_ET_ITs_NEXTx.s4p LongPassiveH2D_ET_ITs_FEXTx.s4p LongPassiveH2D_CR_RR_NEXTx.s4p LongPassiveH2D_CR_RR_FEXTx.s4p LongPassiveH2D_ET_ITs_rev.s4p	Tx initiator/expander device NEXT channels Tx initiator/expander device FEXT channels Rx target device NEXT channels Rx target device FEXT channels Rx target device NEXT Tx channel

[a] If multiple through files are provided, then the first one used shall be before the PICS under test (i.e. between ET and the first measurement point), and the second one used shall be after the PICS under test (i.e. between the second measurement point and RR) (see 5.5.6).
[b] NEXTx and FEXTx indicate multiple aggressor channels.
[c] See figure 134 for a description of the NEXT and FEXT extraction.

Figure 117 shows the end to end simulation diagram for passive TxRx connection segments between IT_S and IR or between CT_S and CR for trained 12 Gbit/s.

C.2.4 Stressed Receiver device delivered signal calibration end to end simulation diagram

Figure C.5 shows the end to end simulation diagram for the stressed receiver device delivered signal calibration for trained 12 Gbit/s (see 5.8.5.7.6.6). For calibration, noise sources (i.e., DJ, RJ, SJ, and SSC) shall not be activated.

The crosstalk from the crosstalk transmitter represents FEXT and should be applied closer to ET than to IR or CR to optimize the amplitude distribution. Equivalent configurations are allowed.

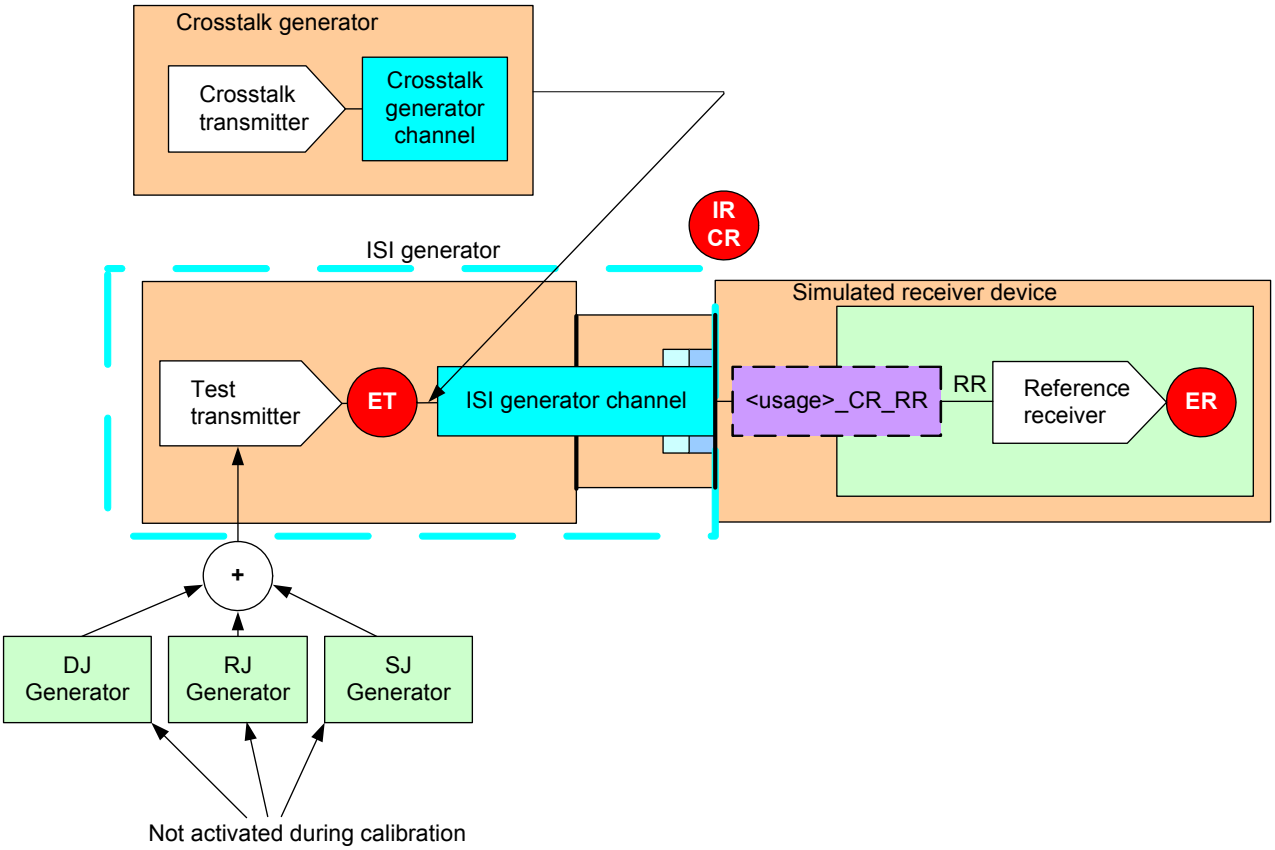


Figure C.5 — Stressed receiver device delivered signal calibration end to end simulation diagram

Table C.5 defines the S-parameter files for stressed receiver device delivered signal calibration.

Table C.5 — S-parameter files for stressed receiver device delivered signal calibration

End to end simulation type	S-parameter files	Description of S-parameter files	Measurement point	Crosstalk amplitude [a]	
				Minimum	Maximum
Stressed receiver device (SAS target device to SAS initiator device or SAS target device to SAS expander device)	LongPassiveD2H_CR_RR.s4p	Rx initiator/expander device channel	IR or CR	15 mV_{P-P}	20 mV_{P-P}
Stressed receiver device (SAS initiator device to SAS target device or SAS expander device to SAS target device)	LongPassiveH2D_CR_RR.s4p	Rx target device channel	IR or CR	10 mV_{P-P}	15 mV_{P-P}

[a] The peak to peak amplitude of the crosstalk that is met or exceeded with a cumulative probability of 10^{-6} (see 5.8.4).

Annex D
(informative)

StatEye

StatEye is a Python program that may be used for simulating TxRx connection compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5). Equivalent simulation programs may be used if they lead to the same results.

The SAS4.zip file includes a directory named SAS2_1.zip. The files in the SAS2_1. zip directory may be used to run StatEye on the SAS-2 reference channel with the appropriate reference transmitter and receiver settings. Python files included in the SAS2_1.zip directory and their function are listed in table D.1.

Table D.1 — Python files included in SAS2_1.zip

File name	Function
analysis.py	This file loads pattern measurement files, and is not used for txRx connection compliance simulations.
cdr.py	This file extracts the clock from a pattern measurement and is not used for TxRx connection compliance simulations.
extractJitter.py	This file extracts jitter from a pattern measurement and is not used for TxRx connection compliance simulations.
penrose.py	This file extracts the step response from a pattern measurement and is not used for TxRx connection compliance simulations.
portalocker.py	This file locks files for exclusive access. (See the ActiveState Code web site at http://aspn.activestate.com/ASPN/Cookbook/Python/Recipe/65203 for information about the portalocker code recipe.)
stateye.py	This file computes the statistical eye.
testcase.py	This file runs a single StatEye simulation.
testall.py	This file runs a set of StatEye simulations.

A file named Stateye_readme.pdf is included in the SAS2_1.zip file to aid the user in setting up and verifying the installation of StatEye.

NOTE 13 - See http://www.stateye.org for more information on StatEye.

Annex E
(informative)

12 Gbit/s S-parameters and end to end simulation

E.1 S-parameters for 12 Gbit/s simulation

E.1.1 Measurement procedure

Figure E.1 shows the connections that are made to a four port VNA to measure S-parameters. The following procedure describes the recommended measurement method:

1) connect the through channel as shown in figure E.1;
2) measure the S-parameters between 50 MHz to 20 GHz with a maximum step size of 10 MHz;
3) repeat step 2) for NEXT of the link under test; and
4) repeat step 2) for NEXT and FEXT of each aggressor link.

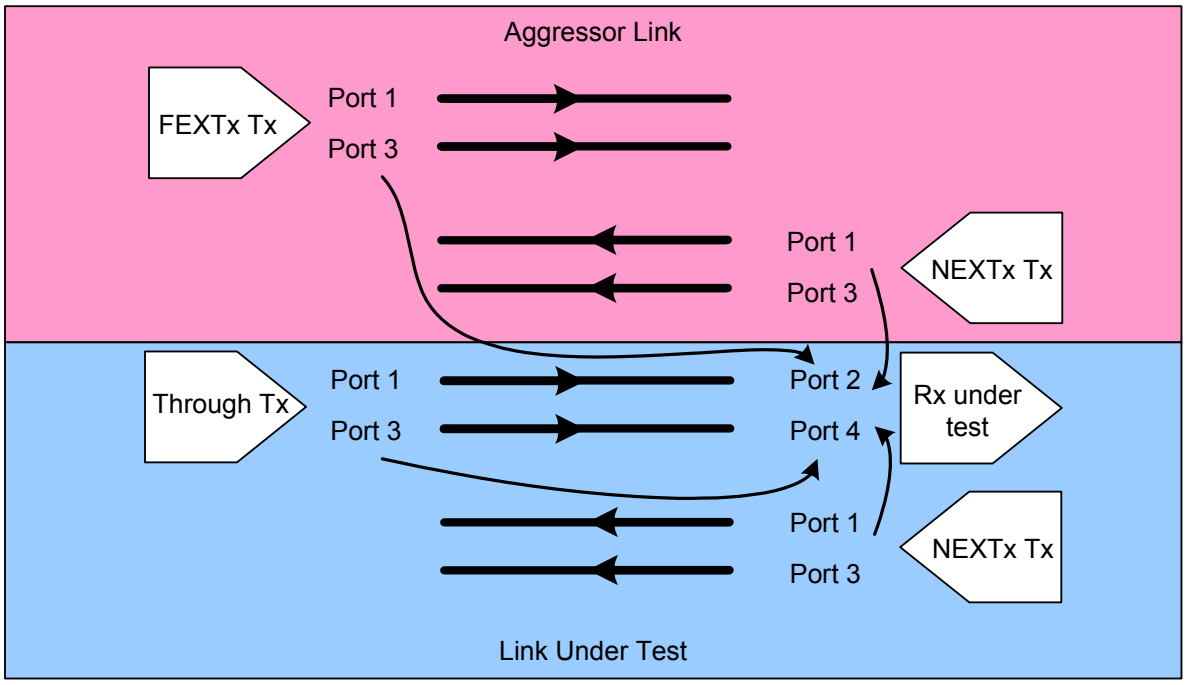


Figure E.1 — S-parameter measurement connections for a four port VNA

E.1.2 Multiple channel segments

If the channel consists of multiple segments, then the complete through channel and crosstalk channels are not directly measurable. One method of computing a channel consisting of multiple measured segments is by cascading the S-parameters in order.

For example a three TxRx connection segment SAS environment is shown in figure E.2.

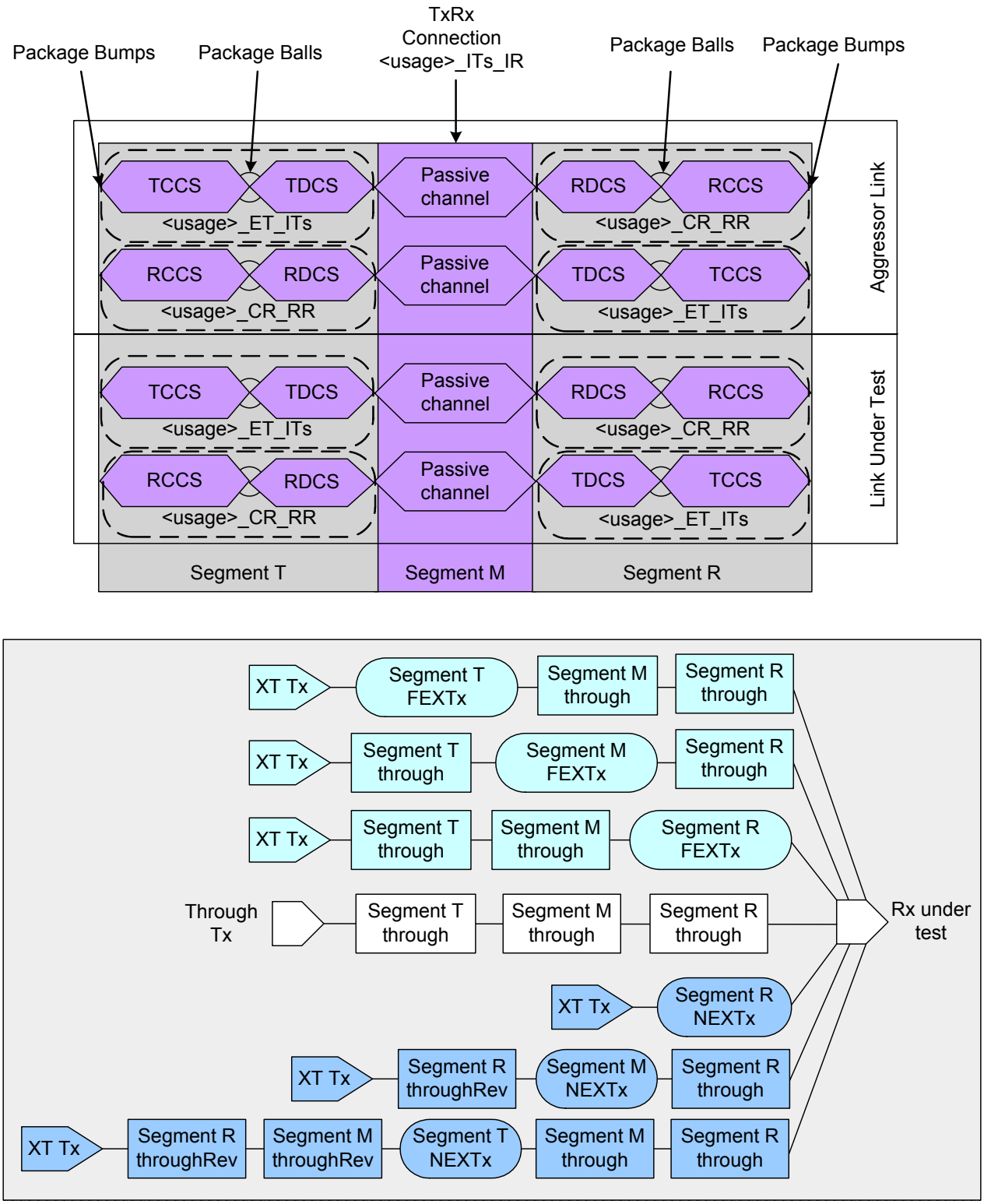


Figure E.2 — Example of a SAS three TxRx connection segment

E.2 End to end simulation using SAS3_EYEOPENING

The SAS3_EYEOPENING Octave/Matlab script may be used for end-to-end simulations and trained 12 Gbit/s transmitter device characterization (see 5.8.4.7). The script and its documentation (i.e., SAS3_EYEOPENING_Usage_Guide) are included in the SAS4.zip file. A wrapper script (i.e., SAS3_Usage) is included in the SAS4.zip file for running the end-to-end simulation described in Annex C. This wrapper script may be run in either interactive mode or batch mode. See SAS3_EYEOPENING_Usage_Guide for full details.

Annex F
(informative)

Signal performance measurements

F.1 Signal performance measurements overview

This annex describes methodologies for making electrical performance measurements, including signal output, signal tolerance, and return loss. Standard loads are used in all cases so that independent specification of connection components and transportability of the measurement results are possible.

F.2 Glossary

F.2.1 port: In this annex, the physical input or output connection of an instrument or device.

F.3 Simple physical link

F.3.1 Simple physical link overview

The physical link consists of the following component parts:

a) the transmitter device;
b) the interconnect; and
c) the receiver device.

Each of these components is connected by a separable connector. On a TxRx connection, signals travel in opposite directions down the same nominal path.

Figure F.1 shows a physical link and the location of the connectors.

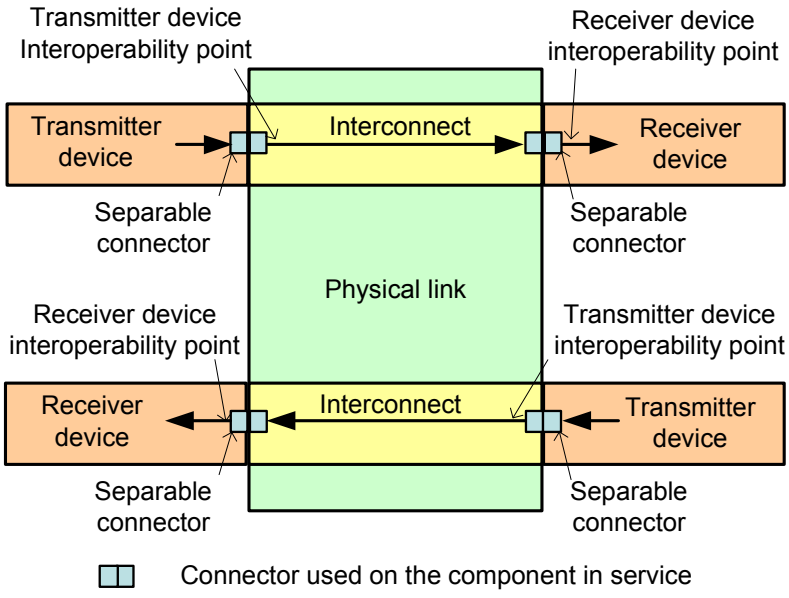


Figure F.1 — A simple physical link

Since connectors are always used in the mated condition, the only practical access to the signals is before the signal enters the mated connector (i.e., upstream) or after the signal exits the connector (i.e., downstream). Even if signals were able to be accessed at the point of mating within the connector, such access may disturb the connector to the point that the measurement of the signal is compromised (e.g., attempting to access the unmated connector with probes does not provide valid results because the connector is not in the same

condition when unmated as when mated and the probe contact points are not at the same location as the connector contact points).

In this annex, signal outputs are always measured downstream of the mated connector (see figure F.1) so that the contribution of the mated connector to the signal properties is included in the measurement. This approach assigns a portion of the connector losses to the upstream component, but it also makes the signal measurement conservative. If the connectors on both ends of the interconnect are the same, then the additional loss at the downstream connector is offset by the reduced loss at the upstream connector.

F.3.2 Assumptions for the structure of the transmitter device and the receiver device

Figure F.2 shows the details of a transmitter device.

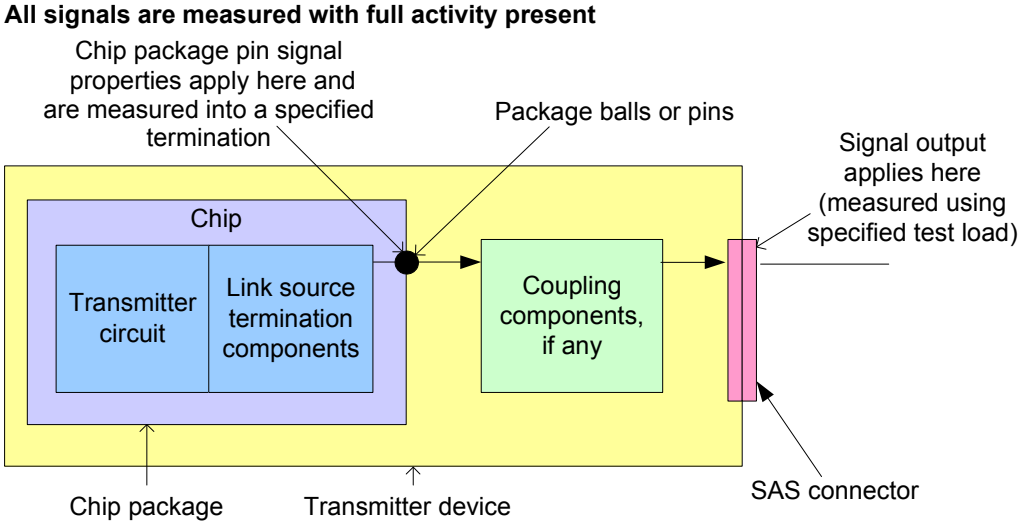


Figure F.2 — Transmitter device details

As figure F.2 shows, any of the following internal parts of this transmitter device may be labeled as the transmitter:

a) the transmitter circuit in the chip;
b) the chip itself; or
c) the chip and its associated chip package.

The term *transmitter* is therefore not well defined and is not used in the terminology without a modifier.

The transmitter device contains:

a) a connector (i.e., half a mated pair);
b) coupling components, if any;
c) PCB traces and vias;
d) the chip package;
e) ESD protection devices, if any;
f) the source termination; and
g) the transmitter circuit.

It is assumed that the source termination is contained within the chip package.

Although interoperability points are defined at the chip package pins in some standards (e.g., Ethernet XAUI), this standard does not define requirements at chip package pins.

Figure F.3 shows the details of a receiver device. It is similar to the transmitter device.

All signals measured with full activity present

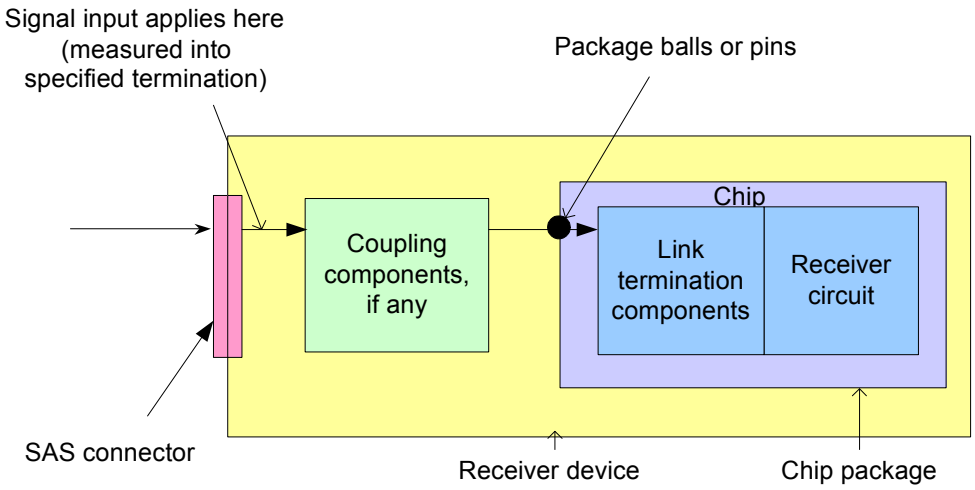


Figure F.3 — Receiver device details

As figure F.3 shows, any of the following internal parts of this receiver device may be labeled as the receiver:

a) the receiver circuit in the chip;
b) the chip itself; or
c) the chip and its associated chip package.

The term *receiver* is therefore not well defined and is not used in the terminology without a modifier.

The receiver device contains:

a) a connector (i.e., half a mated pair);
b) coupling components, if any;
c) PCB traces and vias;
d) the chip package;
e) ESD protection devices, if any;
f) the physical link termination; and
g) the receiver circuit.

It is assumed that the physical link termination is contained within the chip package.

F.3.3 Definition of receiver sensitivity and receiver device sensitivity

The term *receiver sensitivity* is not well defined and is therefore not used in this standard. A related term applicable to the receiver device input signal is *receiver device sensitivity*. While these two terms are related, they are significantly different because of the noise environment assumed. The description in this subclause is used to define these terms with the understanding that this standard discourages usage of either term.

For 1.5 Gbit/s and 3 Gbit/s, receiver device sensitivity is defined as the minimum vertical inner eye opening measured at the signal output point for the input to the receiver device at which the receiver chip (i.e., the receiver circuit in the chip package on the board containing the receiver device interoperability point as shown in figure F.3) delivers the required BER (see 5.8.1) with:

a) the minimum horizontal eye opening;
b) all activity expected in the application for the receiver circuit present (i.e., not quiesced as for the receiver sensitivity definition); and
c) the CJTPAT pattern being received (see Annex A).

For 6 Gbit/s, receiver device sensitivity is defined as the minimum vertical inner eye opening determined by simulation. The signal measured at the input to the receiver device is processed in a manner to simulate the additional interconnect losses (e.g., board traces, chip package). Then, the equalization function provided by the receiver circuit is applied to determine the resulting eye opening.

F.10 describes special test conditions to measure these sensitivities.

For 12 Gbit/s, receiver device sensitivity is verified to achieve the specified BER by testing the receiver device with a stressed signal equivalent to the reference transmitter and reference TxRx connection applied to the receiver device. See 5.8.5.7.6.5 for the test procedure.

This standard uses the term *signal tolerance* instead of *receiver device sensitivity*.

F.4 Signal measurement architecture

F.4.1 General

Signal specifications are only meaningful if the signals are able to be measured with practical instrumentation and if different laboratories making measurements on the same signal get the same results within acceptable measurement error (i.e., the measurements need to be accessible, verifiable, and transportable).

Some of the elements necessary for practical, verifiable, and transportable signal measurements are included in this standard.

Having signal specifications at interoperability points that do not depend on the actual properties of the other physical link components not under test requires that specified known test loads be used for the signal measurements. In service, the load presented to the interoperability point is that of the actual component and environment.

Interfacing with practical instruments requires that specified impedance environments be used. This forces a signal measurement architecture where the impedance environment is 50 Ω single ended (i.e., 100 Ω differential) and also forces the requirement for instrumentation quality loads of the correct value.

Instrumentation quality loads are readily available for simple transmission line termination. However, no instrumentation quality loads are available for more complex loads that include specified propagation time, insertion loss properties, crosstalk properties, and jitter creation properties.

For signal tolerance measurements, the signal is calibrated before applying it to the interoperability point under test. This signal calibration is done by adjusting the properties of the specified signal source system as measured into a laboratory quality test load until the desired signal tolerance specifications are met. The signal source system is then disconnected from the laboratory quality test load and connected to the interoperability point under test. It is assumed that any changes to the signal from the calibration state to the measurement state are caused by the interoperability point under test and are therefore part of the performance sought by the measurement.

F.4.2 Relationship between signal compliance measurements at interoperability points and operation in systems

The signal measurements in this standard apply under specified test conditions that simulate some parts of the conditions existing in service (e.g., this simulation includes full-duplex traffic on all phys and under all applicable environmental conditions). Other features existing in service (e.g., non-ideal return loss in parts of the physical link that are not present when measuring signals in the specified test conditions) may be included in the signal specifications themselves. This methodology results in signal performance requirements for each side of the interoperability point that do not depend on knowing the properties of the other side.

Measuring signals in an actual functioning system at an interoperability point does not verify compliance for the components on either side of the interoperability point, although it does verify that the specific combination of components in the system at the time of the measurement produces compliant signals. Interaction between components on either side of the interoperability point may allow the signal measured to be compliant, but this compliance may have resulted because one component does not meet the signal specifications while the other exceeds the signal specifications.

Additional margin should be allowed when performing signal compliance measurements to account for conditions existing in service that may not have been accounted for in the specified measurements and signal specifications.

F.5 De-embedding connectors in test fixtures

Connectors are part of the test fixtures (e.g. test loads) needed for obtaining access to the interoperability points. This is intrinsic for most practical measurements because the connectors used on the service components are different from those used on the instrumentation.

The effects of the portions of the connector used on the test fixture are taken into account when measurements are made using the fixture so that the results of interoperability point under test are not influenced by the performance of the test fixture connector. This accounting process is termed de-embedding.

Figure F.4 shows two cases that apply.

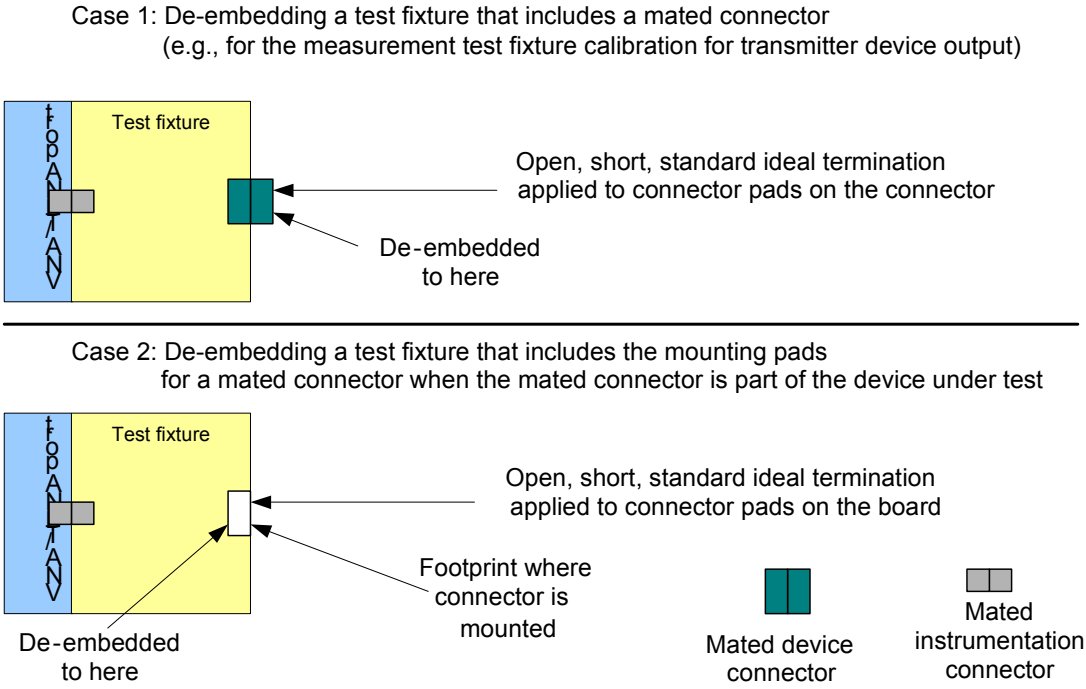


Figure F.4 — De-embedding of connectors in test fixtures

The de-embedding process assumes that the test fixture is linear and that S-parameter methodologies (see F.11) are used. An S-parameter model for the test fixture with or without the connector in place is the result. Knowing this model for the test fixture, with or without the connector in place, allows simulation of the impact of the test fixture on the signal measurement.

F.6 De-embedding test fixture for 12 Gbit/s transmitter compliance

Connectors and board traces are part of the test fixtures (e.g., test loads) needed for obtaining access to the transmitter compliance point ET (see 5.3.3). The effects of the test fixture and test board de-embedding by creation of a de-embedding filter to cancel their effects on the measurements.

Figure F.5 shows the test fixture for a 12 Gbit/s transmitter compliance test.

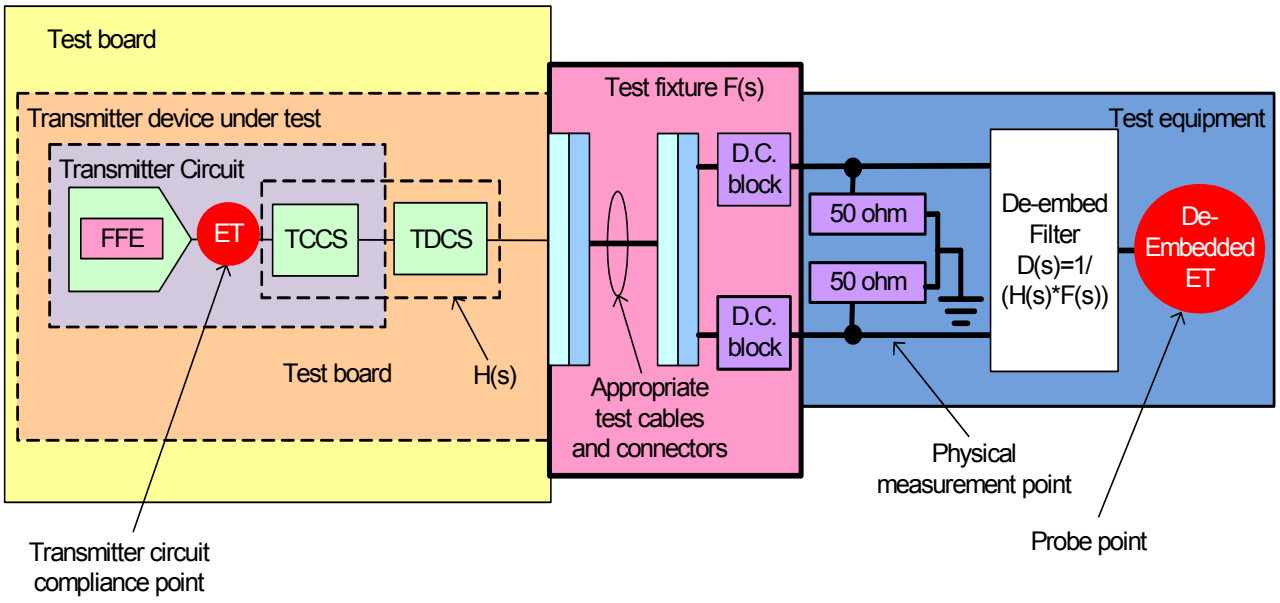


Figure F.5 — De-embedding to ET for 12 Gbit/s transmitter compliance

Figure F.6 shows a test structure for measuring the channel to be de-embedded.

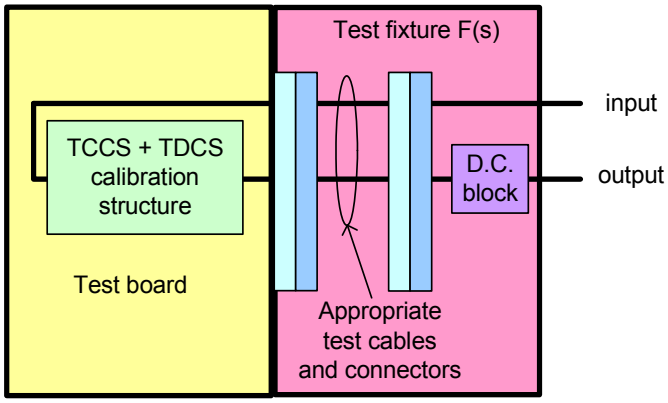


Figure F.6 — De-embedding calibration test structure

The de-embedding process consist of the following steps:

1) measure a de-embedding test structure equivalent to the TCCS and TDCS H(s) and test fixture F(s);
2) compute an appropriate de-embedding filter D(s); and
3) exercise the transmitter to demonstrate compliance observed at the output of the de-embedding filter.

F.7 Measurement conditions for signal output at the transmitter device

The measurement conditions for a differential transmitter device signal output are shown in figure F.7. Figure F.7 applies to the following cases the transmitter device:

a) is directly attached to the zero-length test load (see 5.6.2); and
b) is attached to the TCTF test load (see 5.6.3).

To simulate the properties of the interconnect assembly, instrumentation quality test loads as shown in figure F.8 are used.

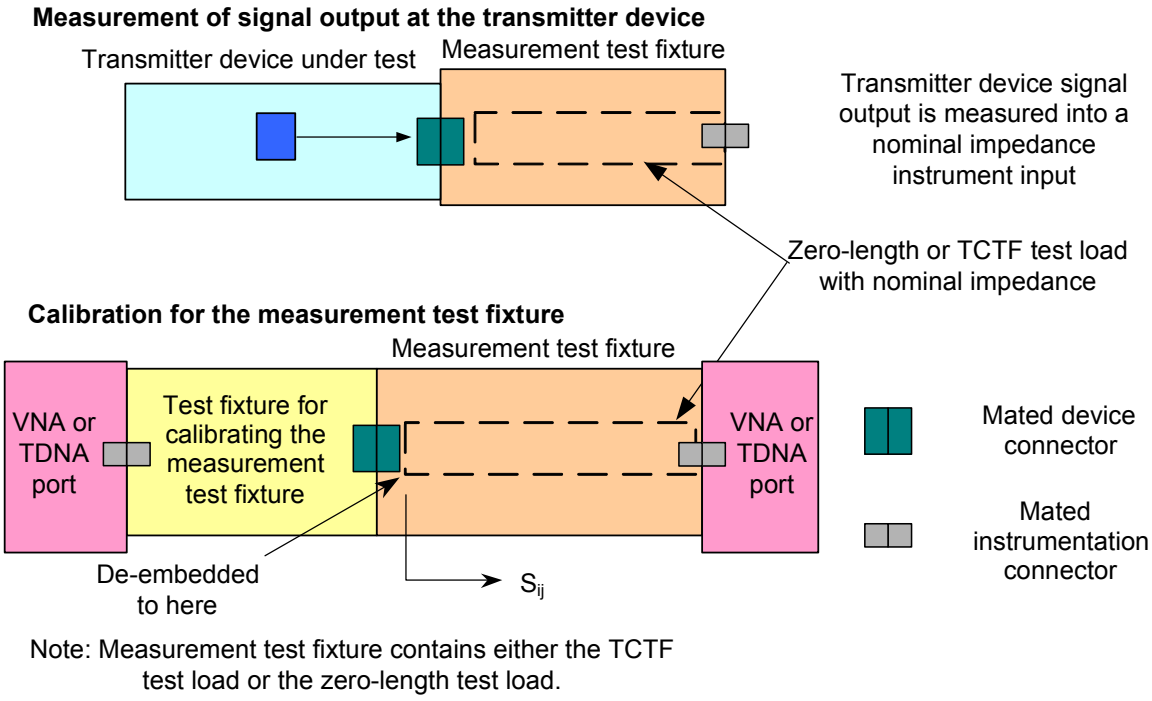


Figure F.7 — Measurement conditions for signal output at the transmitter device

An instrumentation quality cable assembly connects the measurement test fixture to the instrumentation port. This cable assembly is considered part of the instrumentation and is not specifically shown in figure F.7, figure F.8, figure F.9, figure F.10, figure F.11, figure F.12, and figure F.13.

A measurement test fixture may be constructed from an instrumentation quality TCTF test load with instrumentation quality connectors and a connector adapter as shown in figure F.8. This method may be useful when using multiple device connector types but adds extra components that may increase loss and delay. For best accuracy, this method is not recommended. Extra components make it more difficult for the transmitter device to meet the required output specifications.

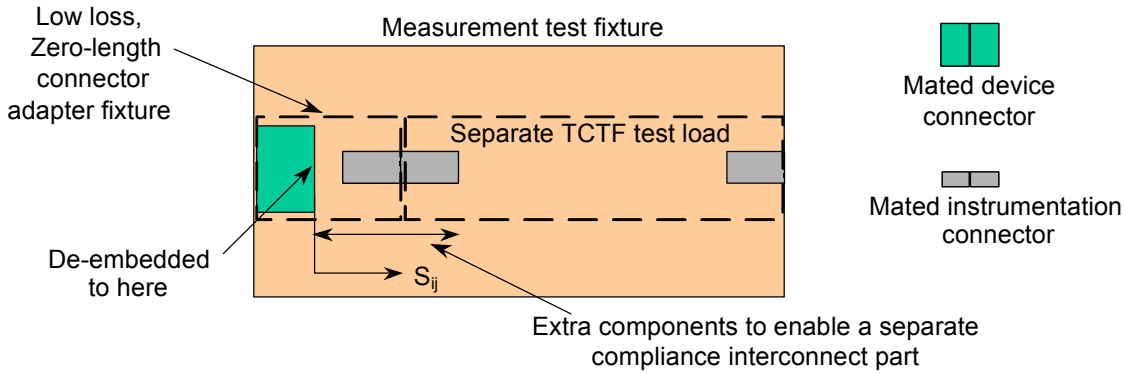


Figure F.8 — Transmitter device signal output measurement test fixture details

F.8 Measurement conditions for signal tolerance at the transmitter device

The measurement conditions for the signal tolerance at the differential transmitter device interoperability point are shown in figure F.9. Figure F.9 shows the test signal is launched into the interconnect assembly (e.g., cable assembly or PCB) that is attached to the receiver device.

This standard does not specify this performance requirement. It is included here for completeness.

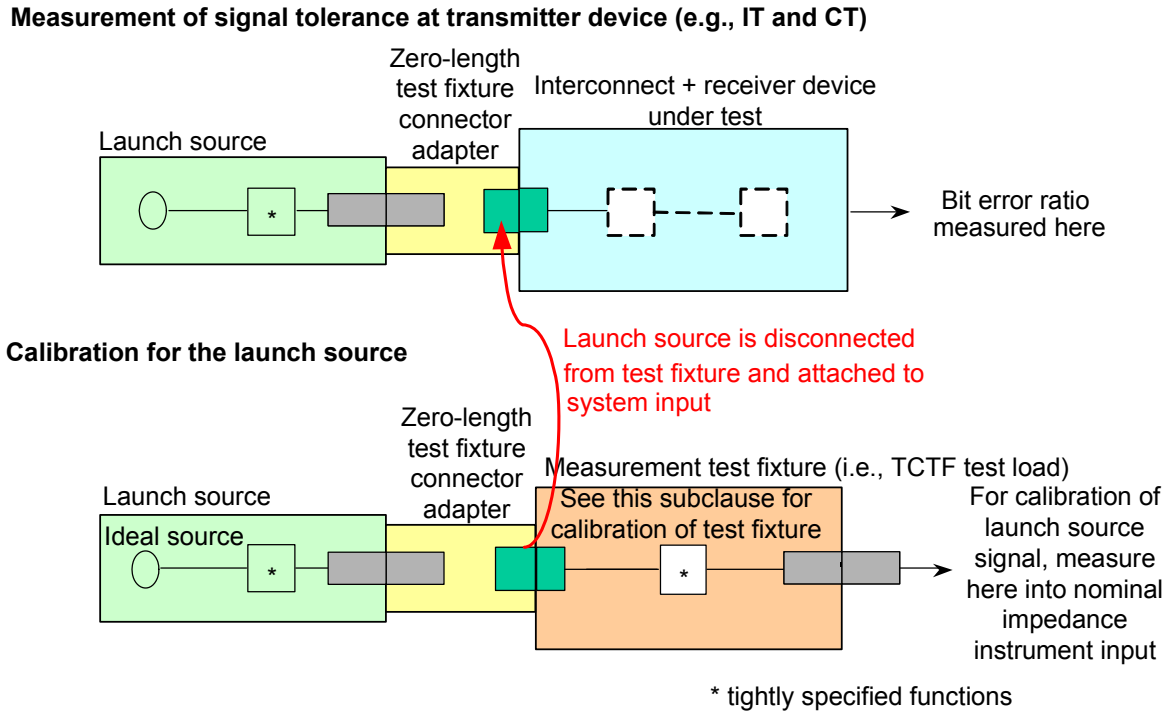


Figure F.9 — Measurement conditions for signal tolerance at the transmitter device

Figure F.10 shows calibration of the measurement test fixture.

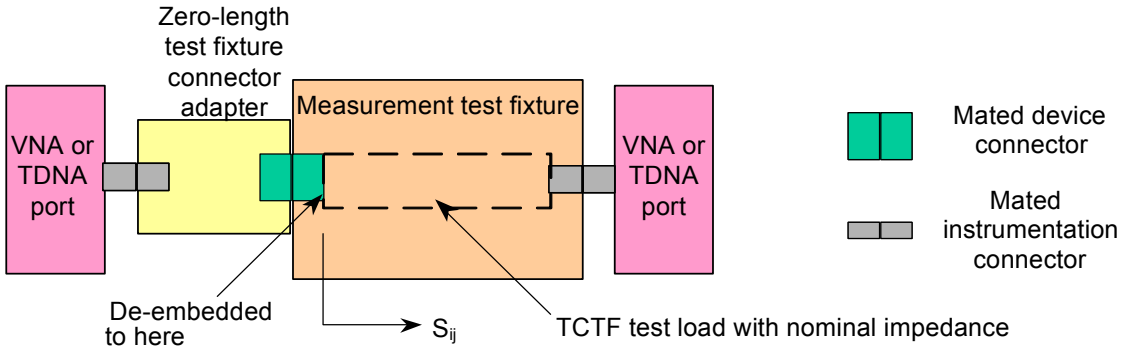


Figure F.10 — Calibration of test fixture for signal tolerance at the transmitter device

F.9 Measurement conditions for signal output at the receiver device

Figure F.11 shows the measurement conditions for the signal output at the receiver device.

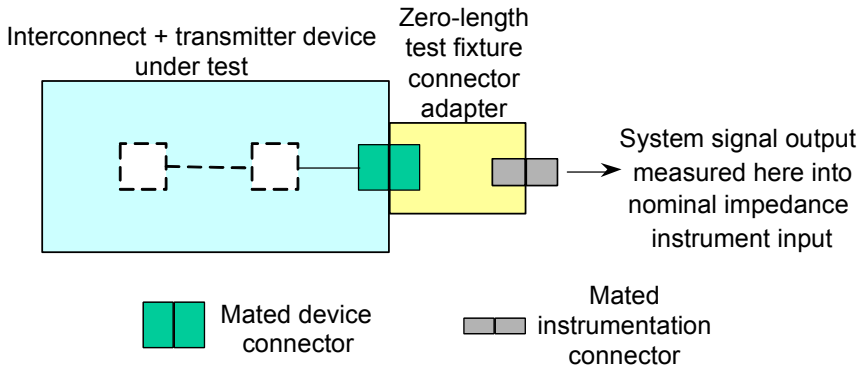


Figure F.11 — Measurement conditions for signal output at the receiver device

The interconnect may be the zero-length connector adaptor where the transmitter device is connected directly to the receiver device.

F.10 Measurement conditions for signal tolerance at the receiver device

Figure F.12 shows the measurement conditions for the signal tolerance at the differential receiver device interoperability point (see 5.8.5.4).

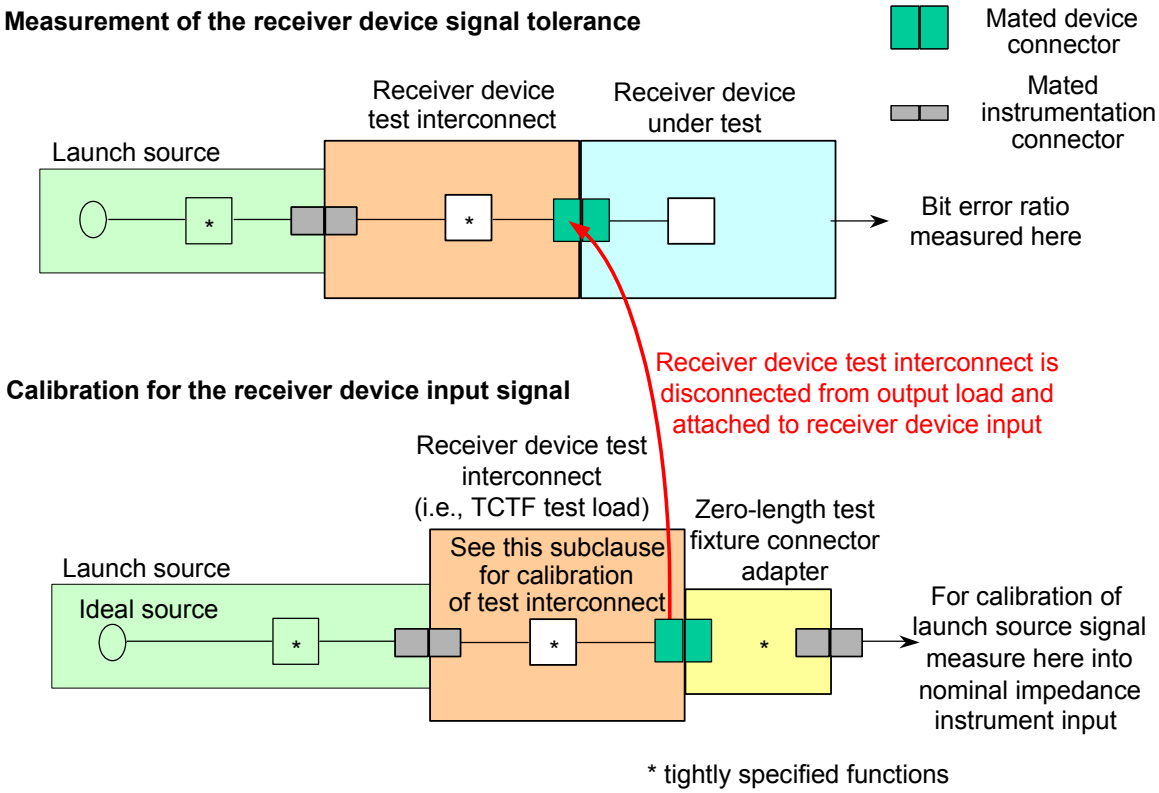
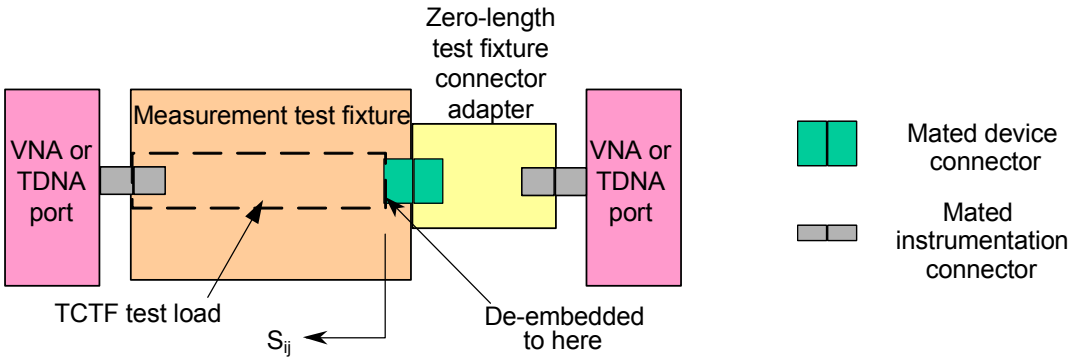


Figure F.12 — Measurement conditions for signal tolerance at the receiver device

Figure F.13 shows calibration of the measurement test fixture.



NOTE 1 - This is not identical to the measurement test fixture used for the transmitter output signal even though the connector genders are the same. The pins used in the SAS connector are for the Rx (i.e., not the Tx) signals and the signals flow the other way. The S_{22} measurement here is the same as the S_{11} measurement for the transmitter output signal but on different pins.

NOTE 2 - The S_{21} and S_{12} are used to create the desired jitter in this application and are not as critical.

Figure F.13 — Calibration of test fixture for signal tolerance at the receiver device

F.11 S-parameter measurements

F.11.1 S-parameter overview

Properties of physical link elements that are linear may be represented by S-parameter (i.e., scattering parameter) spectra.

S-parameters are the preferred method of capturing the linear properties of physical link elements. A frequency domain spectrum output is used for all S-parameters and specifying pass/fail limits to such a spectrum may overconstrain the system because some peaks and properties are benign to the application.

There are two problematic areas when applying S-parameters to differential electrical physical links:

a) naming conventions (see F.11.2); and
b) use of single ended vector network methods on differential and common mode systems (see F.11.3).

F.11.4 describes using special test fixtures to make S-parameter measurements.

F.11.2 S-parameter naming conventions

There are two types of measurements performed with S-parameters:

a) return loss from the same port of the element; and
b) insertion loss across the element.

Each S-parameter is a function of frequency returning complex numbers and is expressed with:

a) a magnitude component, usually expressed in dB; and
b) a phase component.

For a two port linear element having ports i and j with the signals being either differential or common mode, S_{ij} is the ratio of the signal coming out of the ith port (i.e., the response) to the signal coming into the jth port (i.e., the stimulus).

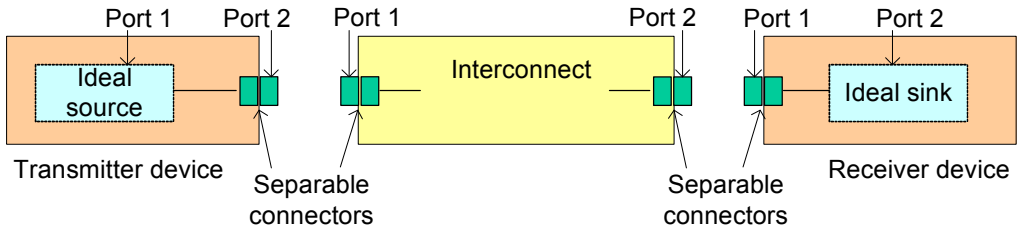
A port number convention is used where the downstream port is always port 2 and the upstream port is always port 1. The stream direction is determined by the direction of the primary signal launched from the transmitter device to the receiver device (e.g., in this standard, since each differential pair carries a signal in

only one direction, the port nearest the transmitter device is port 1 and the port nearest the receiver device is port 2).

There are four combinations of ports for a two ported system yielding the following S-parameters:

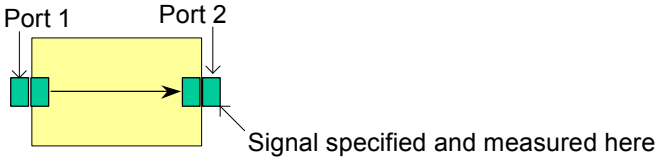
a) S_{11} (i.e., negative return loss): measured at port 1;
b) S_{21} (i.e., negative insertion loss): measured at port 1;
c) S_{22} (i.e., negative upstream return loss): measured at port 2 of the element. The measurement is the same kind of measurement that is done at port 1 to measure S_{11}; and
d) S_{12} (i.e., negative upstream insertion loss): measured at port 2 of the element. The measurement is the same kind of measurement that is done at port 1 to measure S_{21}.

Figure F.14 shows the port naming conventions for physical link elements, loads, and where those elements exit.



The transmitter device port 1 and receiver device port 2 are internal and are not defined.

Port definitions for loads used for signal output testing and S-parameter measurements in multiline configurations



This load has ideal differential and common mode properties

Figure F.14 — S-parameter port naming conventions

F.11.3 Use of single ended instrumentation in differential applications

There are four categories of S-parameters for a differential system:

a) $\mathbf{S_{DDij}}$, differential stimulus, differential response;
b) $\mathbf{S_{CDij}}$, differential stimulus, common mode response (i.e., mode conversion causing emissions);
c) $\mathbf{S_{DCij}}$, common mode stimulus, differential response (i.e., mode conversion causing susceptibility); and
d) $\mathbf{S_{CCij}}$, common mode stimulus, common mode response.

Figure F.15 shows the connections that are made to a four port VNA or TDNA for measuring S-parameters on a four single ended port black box device.

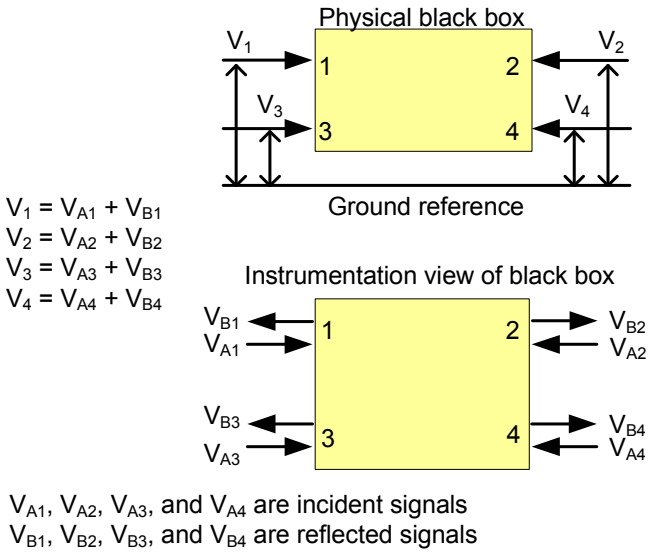
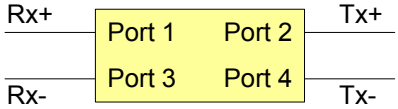


Figure F.15 — Four single ended port or two differential port element

Since VNA ports are all single ended, the differential and common mode properties for differential ports are calculated internal to the VNA or are mathematically derived. If using a TDNA, consult the details for the specific instrument. Four analyzer ports are needed to measure the properties of two differential ports.

Figure F.16 shows the set of S-parameters for a single ended system and for a differential system.

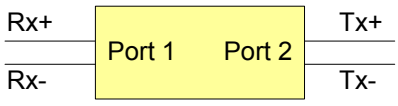
Single ended



S-parameters

	Stimulus	
Response	S_{11} S_{12} S_{13} S_{14}	
	S_{21} S_{22} S_{23} S_{24}	
	S_{31} S_{32} S_{33} S_{34}	
	S_{41} S_{42} S_{43} S_{44}	

Differential



S-parameters

		Stimulus: Differential	Stimulus: Common-mode
Response	Differential	S_{DD11} S_{DD12}	S_{DC11} S_{DC12}
		S_{DD21} S_{DD22}	S_{DC21} S_{DC22}
	Common-mode	S_{CD11} S_{CD12}	S_{CC11} S_{CC12}
		S_{CD21} S_{CD22}	S_{CC21} S_{CC22}

Converting single ended to mixed-mode

$$S_{mm} = 0.5 \times \begin{bmatrix} S_{11} - S_{13} - S_{31} + S_{33} & S_{12} - S_{14} - S_{32} + S_{34} & S_{11} + S_{13} - S_{31} - S_{33} & S_{12} + S_{14} - S_{32} - S_{34} \\ S_{21} - S_{23} - S_{41} + S_{43} & S_{22} - S_{24} - S_{42} + S_{44} & S_{21} + S_{23} - S_{41} - S_{43} & S_{22} + S_{24} - S_{42} - S_{44} \\ S_{11} - S_{13} + S_{31} - S_{33} & S_{12} - S_{14} + S_{32} - S_{34} & S_{11} + S_{13} + S_{31} + S_{33} & S_{12} + S_{14} + S_{32} + S_{34} \\ S_{21} - S_{23} + S_{41} - S_{43} & S_{22} - S_{24} + S_{42} - S_{44} & S_{21} + S_{23} + S_{41} + S_{43} & S_{22} + S_{24} + S_{42} + S_{34} \end{bmatrix}$$

S_{DD11}, S_{DC11}, S_{CD11}, S_{CC11}

Figure F.16 — S-parameters for single ended and differential systems

See SFF-8416 for details on differential S-parameter measurements.

F.11.4 Measurement configurations for physical link elements

F.11.4.1 Measurement configuration overview

Special test fixtures are needed to make S-parameter measurements partly because the connectors used on real physical link elements are different from those used on instrumentation. The goal is for these test fixtures to be as invisible as possible.

All of the measurements in this annex are of S_{11} or S_{22}. A more complete set of S-parameters is used as part of the calibration process for test fixtures.

F.11.4.2 Transmitter device S_{22} measurements

Figure F.17 shows the configuration to be used for the transmitter device S_{22} measurements.

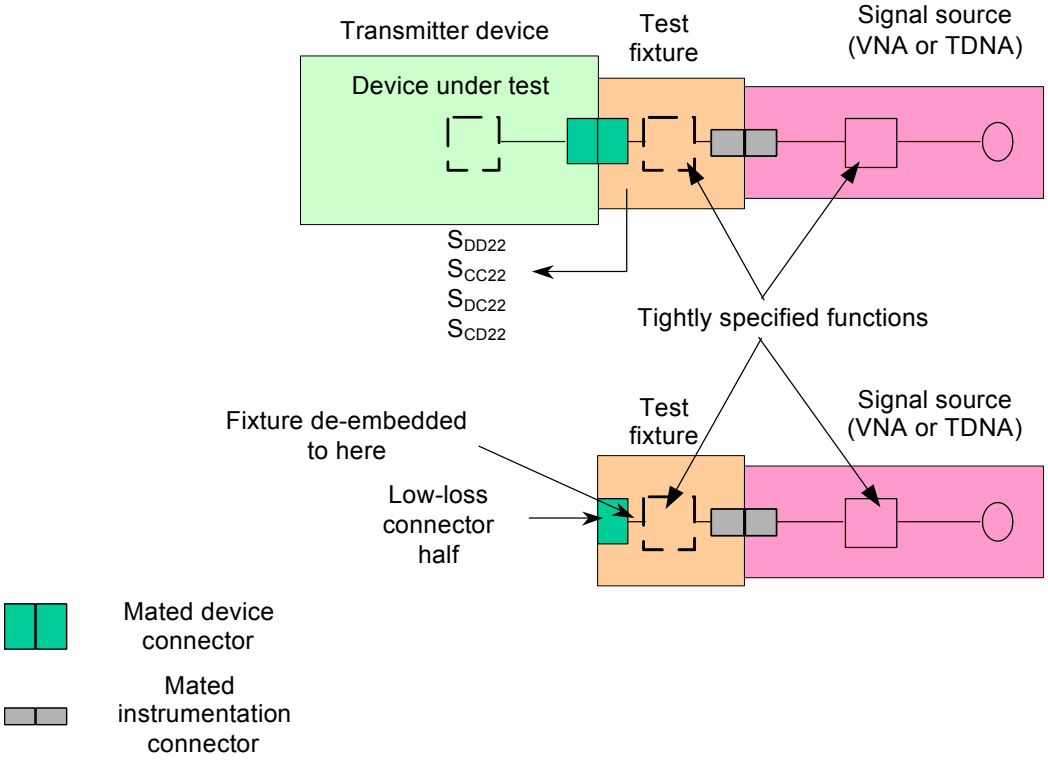


Figure F.17 — Measurement conditions for S_{22} at the transmitter device connector

The test fixture in figure F.17 uses low loss connectors to avoid penalizing the transmitter device under test for the test fixture half of the connector.

The test fixture losses up to the mounting points for the device connector are de-embedded using the methods described in figure F.4.

F.11.4.3 Receiver device S_{11} measurements

Figure F.18 shows the configuration to be used for the receiver device S_{11} measurements.

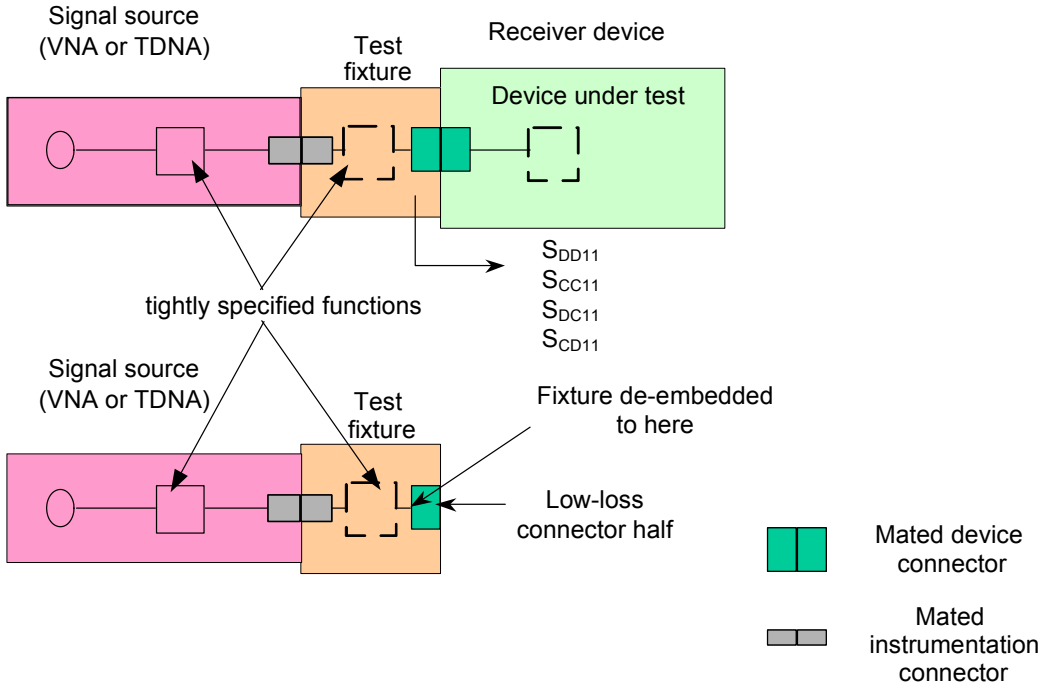


Figure F.18 — Measurement conditions for S_{11} at the receiver device connector

The test fixture in figure F.18 uses low loss connectors to avoid penalizing the receiver device under test for the test fixture half of the connector.

The test fixture losses up to the mounting points for the device connector are de-embedded using the methods described in figure F.4.

F.11.4.4 TxRx connection S_{11} measurements at IT or CT

Figure F.19 shows the conditions for making S_{11} measurements of the interconnect attached to the transmitter device.

This measurement, like the signal tolerance measurement at the transmitter device connector, has both the interconnect and the receiver device in place when the combination is measured. If the receiver device is replaced by an ideal load, then S_{11} does not represent in-service conditions. If the interconnect is very lossy, then the effects of the load on the far end (i.e., where the receiver device is located) are not significant and an ideal load may be used. However, if the interconnect is not very lossy (e.g., the zero-length test load), then the measured S_{11} may be dominated by the properties of the receiver device and not the properties of the interconnect.

For short physical links, S_{11} performance may be the limiting factor for the entire physical link due to severe unattenuated reflections that create large DJ.

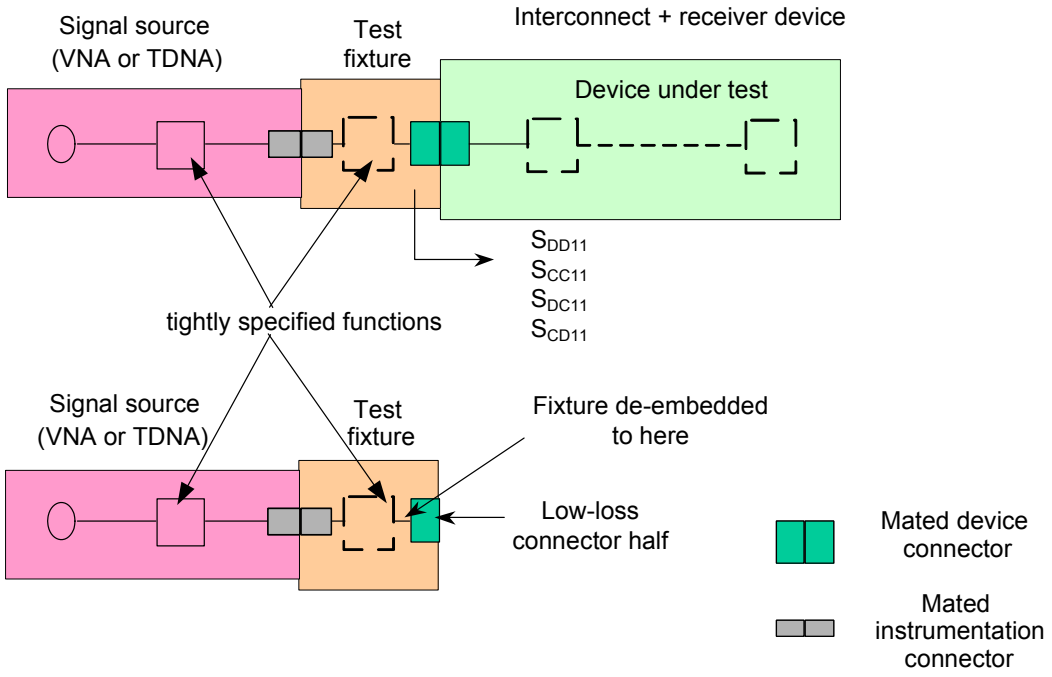


Figure F.19 — Measurement conditions for S_{11} at IT or CT

F.11.4.5 TxRx connection S_{22} measurements at IR or CR

Figure F.20 shows the conditions for making S_{22} measurements of the interconnect attached to the receiver device.

This measurement has both the interconnect and the transmitter device in place when the combination is measured. This may be considered a reverse direction signal tolerance measurement. If the transmitter device is replaced by an ideal load, then S_{22} does not represent in-service conditions. If the interconnect is very lossy, then the effects of the load on the far end (i.e., where the transmitter device is located) are not significant and an ideal load may be used. However, if the interconnect is not very lossy (e.g., the zero-length test load), then the measured S_{22} may be dominated by the properties of the transmitter device and not the properties of the interconnect.

For short physical links, S_{22} may be the limiting factor for the entire physical link due to severe unattenuated reflections that create large DJ.

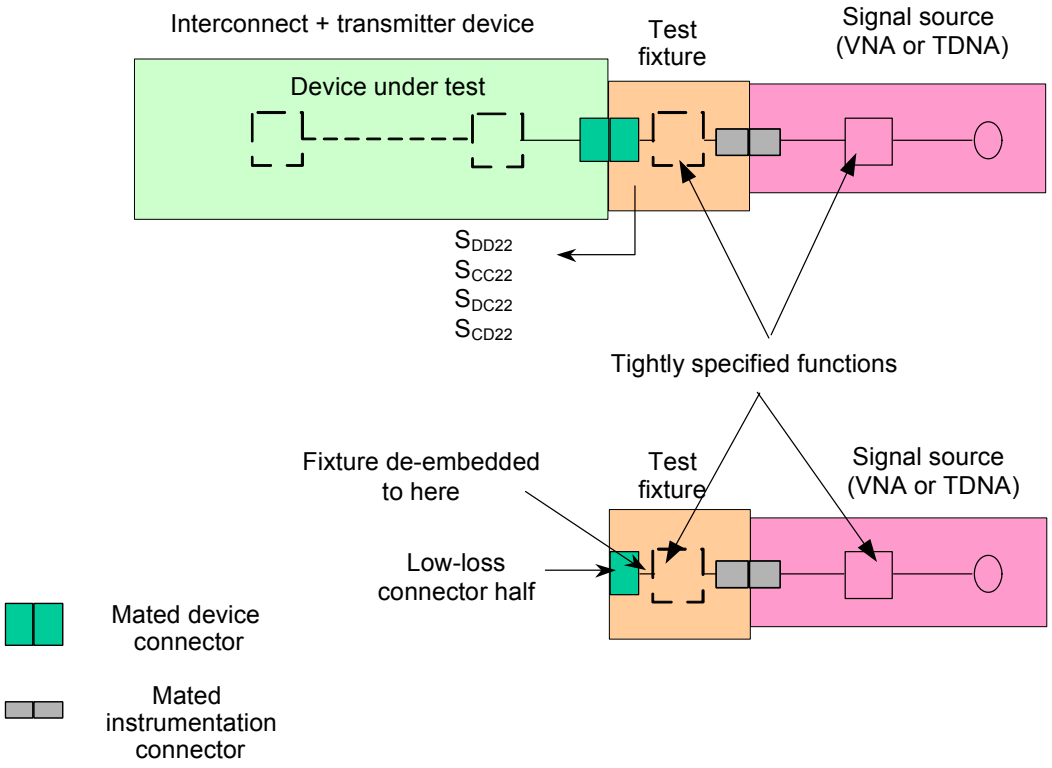


Figure F.20 — Measurement conditions for S_{22} at IR or CR

F.12 Calibration of JMDs

F.12.1 Calibration of JMDs overview

F.12.1.1 Purpose of JMD calibration

The response of a JMD to known jitter levels is calibrated and verified in two frequency bands:

a) the lower frequency band; and
b) the frequency band around the -3 dB frequency and the peak frequency of the JTF.

By calibrating the JMD to these two bands, the response to jitter is calibrated and allows for improved correlation among JMDs.

The test sequence for all measurements removes the baseline DJ, the DJ of the source, and the DJ of the JMD so that the measurement only reports the added test jitter.

F.12.1.2 Overview of low frequency calibration for SSC configurations

For configurations supporting SSC, the lower frequency band requirement is tested with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) on which a sinusoidal phase modulation of 30 kHz with a relative tolerance of 1 % is added. The amplitude of this modulation is 20.83 ns peak to peak. The ratio of the reported jitter to the amount applied is the attenuation (see 5.8.3.2).

This calibration procedure ensures that the measurement equipment responds properly to the fundamental characteristics of the JTF.

For any SSC modulation, there are three important characteristics that affect the response of the JMD and the ability to generate jitter:

a) the peak to peak phase excursion experienced through an SSC cycle;
b) the extreme instantaneous frequency modulation; and
c) the extreme instantaneous frequency modulation rate.

The peak to peak phase excursion experienced through an SSC cycle is an important parameter for jitter generating equipment.

The extreme instantaneous frequency modulation stresses the ability of the JMD to track large frequency modulation. All systems have practical limitations beyond which the response changes shape (e.g. the system response becomes 20 dB/decade instead of 40 dB/decade). The amplitude of the peak to peak frequency modulation under which the JMD maintains a 40 dB/decade response indicates the JMD's limitation to behave as a linear system.

The extreme instantaneous frequency modulation rate (e.g., the minimal negative and maximal positive) stresses the ability of the JMD to respond with the 40 dB/decade low frequency JTF slope specified by this standard. The remaining jitter, after being filtered by the JTF, is proportional to the extreme frequency modulation rate. The maximal amount of remaining jitter a JMD reports is a direct indication of its linear performance in the expected 40 dB/decade response region.

An example of an SSC profile is a balanced triangular SSC waveform (e.g., ± 2 300 ppm).

In this calibration procedure, a sinusoidal phase modulation is applied. Even though this modulation is defined as a phase modulation, its variation in time makes it equivalent to a frequency modulation having comparable characteristics to that of a triangular SSC profile.

The triangular SSC profile is defined by the following equations.

For $k/f_m \leq t < (k+0.5)/f_m$:

$$\Delta f(t) = f_{baud} \times mod\_max \times (-1 + modulo(t,1/f_m) \times f_m \times 4) \text{ Hz}$$

and for $(k+0.5)/f_m \leq t < (k+1)/f_m$:

$$\Delta f(t) = f_{baud} \times mod\_max \times (3 - modulo(t,1/f_m) \times f_m \times 4) \text{ Hz}$$

where:

$\Delta f(t)$	is the frequency deviation in Hz;
f_{baud}	is the baud rate (e.g., 6 GHz for 6 Gbit/s) (see 5.8.1);
mod_max	is the peak excursion of the frequency modulation as a ratio of the current baud rate (e.g., 2.3×10^{-3} for a ± 2 300 ppm modulation);
modulo(t,1/f_m)	modulo operator, the result is x modulo y and limited to range [0,y];
f_m	is the modulation frequency in Hz; and
k	is an integer.

The bit transitions are expected to happen for t where the following equation reaches any integer value m:

$$(f_{baud} + \Delta f(t)) \times t = m$$

where the characteristics for this pattern are:

a) peak to peak phase excursion = $2 \times \pi \times mod\_max \times f_{baud} / (4 \times f_m)$ radians (or peak to peak time excursion = $mod\_max / (4 \times f_m)$ seconds);
b) extreme instantaneous frequency modulation = $\pm\ mod\_max \times f_{baud}$ Hz; and
c) extreme instantaneous frequency modulation rate = $\pm\ 4 \times mod\_max \times f_m \times f_{baud}$ Hz/s (or $\pm\ 4 \times mod\_max \times f_m$ ppm/µs).

A sinusoidal phase modulation is defined by:

$$PJ(t) = A_{ppu}/2 \times \sin(2 \times \pi \times f_{ms} \times t) \text{ UI}$$

where:

A_{ppu} is the peak to peak modulation in UI; and

f_{ms} is the frequency of the phase modulation in Hz.

This is equivalent to A_{pps}, the peak to peak time modulation in seconds, knowing that:

$$A_{pps} = A_{ppu}/f_{baud}$$

The bit transitions are expected to happen for t where the following equation reaches any integer value n:

$$f_{baud} \times t + PJ(t) = n$$

where the characteristics for this pattern are:

a) peak to peak phase excursion = $2 \times \pi \times A_{pps} \times f_{baud}$ radians (or Appu UI);
b) extreme instantaneous frequency modulation = $\pm \pi \times A_{pps} \times f_{baud} \times f_{ms}$ Hz; and
c) extreme instantaneous frequency modulation rate = $\pm 2 \times (\pi \times f_{ms})^2 \times A_{pps} \times f_{baud}$ Hz/s (or $\pm 2 \times (\pi \times f_{ms})^2 \times A_{pps}$ ppm/µs).

The JMD calibration procedure uses sinusoidal phase modulation where:

a) A_{pps} = 20.83 ns; and
b) f_{ms} = 30 kHz.

By comparing the equations of the characteristics, it is possible to compute the parameters of the equivalent triangular SSC profile to the prescribed sinusoidal phase modulation. Defining that $f_m = f_{ms}$ = 30 kHz the equivalent:

a) peak to peak phase excursion of the sinusoidal phase modulation (i.e., 20.83 ns) corresponds to a triangular SSC profile having a mod_max parameter of ± 2 500 ppm;
b) extreme instantaneous frequency modulation of the sinusoidal phase modulation (i.e., 11.78 UI/µs) to a triangular SSC profile having a mod_max parameter of ± 1 963 ppm; and
c) extreme instantaneous frequency modulation rate of the sinusoidal phase modulation (i.e., 370 ppm/µs) corresponds to a triangular SSC profile having a mod_max parameter of ± 3 084ppm.

As a result, using a sinusoidal jitter with a 20.83 ns peak to peak excursion at 30 kHz produces a modulation with fundamental parameters balanced around the specified maximal ± 2 300 ppm amplitude of the SSC profile at a modulation rate of 30 kHz.

F.12.1.3 Overview of low frequency calibration for non-SSC configurations

For configurations not supporting SSC, the lower frequency band requirement is tested with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at the desired baud rate on which sinusoidal phase modulation is added. The ratio of the jitter applied to the jitter reported is the attenuation.

Unlike the SSC supported cases, there is no specific frequency defined for this measurement. It is recommended to verify the attenuation using PJ at a frequency 10 times below the -3 dB frequency (e.g., 90 kHz for 1.5 Gbit/s, 180 kHz for 3 Gbit/s, 360 kHz for 6 Gbit/s, or 720 kHz for 12 Gbit/s). The phase modulation amplitude used for these tests is calibrated to be 3 UI peak to peak at the current baud rate, which is 20 dB more than the 0.3 UI used at high frequency (see F.12.1.4).

F.12.1.4 High frequency calibration

The calibration described in this subclause applies for all configurations, independent of SSC support.

To do a high frequency calibration, two tests are performed in the higher frequency band:

a) adjustment of the -3 dB bandwidth of the JTF; and
b) verification of the peaking (see 5.8.3.2).

Both of these tests use a repeating 0011b pattern or 1100b pattern (e.g., D24.3) with sinusoidal periodic phase modulation or PJ that has been independently verified to produce 0.3 UI with a relative tolerance of 10 % peak to peak at the baud rate being tested over a frequency range of 0.5 MHz to 50 MHz. This corresponds to the values in table F.1.

Table F.1 — High frequency jitter source amplitudes

Baud rate (Gbit/s)	Peak to peak jitter for high frequency test (ps)	Tolerance (ps)	Range (MHz)
1.5	200	± 20	0.5 to 50
3	100	± 10	0.5 to 50
6	50	± 5	0.5 to 50
12	25	± 2.5	0.5 to 50

The programmed source PJ level may vary over the frequency range in order to keep the generated PJ at 0.3 UI with a relative tolerance of 10 %.

There are two typical JMD adjustments for clock recovery:

a) loop bandwidth; and
b) peaking (i.e., damping).

These adjustments may refer to the closed loop response or be specific to a particular design, so they are not used directly to ensure the JTF response to jitter. The loop bandwidth is initially adjusted with the peaking fixed. If both the low frequency band requirements and the high frequency band requirements are not able to be simultaneously met, then the peaking is adjusted to modify the JTF shape in the upper band. In the case of hardware based reference clocks, moderate levels of peaking may be needed to achieve the proper attenuation at 30 kHz. The peaking setting is usually specific to the JMD. With software based clock recovery, the suggested starting peaking level may be low, close to the critically damped condition of peaking of 0.707.

F.12.2 JMD calibration procedure

F.12.2.1 General characteristics and equipment

This calibration procedure is based on the JTF characteristics defined in 5.8.3.2 for:

a) the -3 dB corner frequency of the JTF;
b) the magnitude peaking of the JTF;
c) the attenuation at 30 kHz when SSC is supported; and
d) the low frequency attenuation when SSC is not supported.

The required JMD calibration equipment for configurations supporting SSC is as follows:

a) a pattern generator for SAS signals;
b) a sine wave source of 30 kHz;
c) test cables; and
d) a JMD.

The JMD calibration equipment is as follows:

a) a pattern generator for SAS signals;
b) a sine wave source covering the range from 90 kHz to 360 kHz;
c) a sine wave source covering the range from 0.5 MHz to 50 MHz;
d) test cables; and
e) a JMD.

The response to jitter of the JMD is measured with three different jitter modulation frequencies corresponding to the three cases:

a) low frequency jitter (i.e., the JMD fully tracks);

b) high-frequency jitter (i.e., the JMD does not track); and
c) the boundary between low-frequency jitter and high-frequency jitter.

The jitter source is independently verified by separate means to ensure that the jitter response of the JMD is reproducible across different test setups.

The JMD calibration pattern is a square wave at 0.25 × f_{baud} with a relative tolerance of 0.01 % (i.e., a repeating 0011b pattern or 1100b pattern (e.g., D24.3)) with rise time longer than 0.25 UI measured from 20 % to 80 % of the transition.

When testing 6 Gbit/s or 12 Gbit/s, a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at 6 Gbit/s is used. When testing 3 Gbit/s or 1.5 Gbit/s, a repeating 0011b pattern or 1100b pattern (e.g., D24.3) is used at 3 Gbit/s or 1.5 Gbit/s, respectively. This applies to all jitter frequencies.

An independent, separate means of verification of the JMD calibration pattern is used to ensure that the level of the modulation is correct.

F.12.2.2 Calibration of the JMD for testing SSC configurations

This procedure checks the JTF attenuation and the JTF bandwidth for testing configurations with training and SSC support.

The following test procedure is performed for each baud rate tested (e.g., 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s as applicable):

1) set the pattern generator to output the JMD calibration pattern with a sinusoidal phase modulation of 20.8 ns with a relative tolerance of 10 % peak to peak at 30 kHz with a relative tolerance of 1 %;
2) verify the level of modulation meets the requirements and record the peak to peak level as DJ_SSC (e.g., the independent, separate means of verification of the 30 kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator) measured with:
   A) a time interval error plot with constant frequency clock on a real time oscilloscope;
   B) an equivalent time oscilloscope; or
   C) a frequency demodulator;
3) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_SSCOFF;
4) turn on the sinusoidal phase modulation. Record the reported DJ as DJ_SSCON;
5) calculate and record the reported DJ as DJ_MSSC by subtracting the DJ with modulation off from DJ with modulation on (i.e., DJ_MSSC = DJ_SSCON - DJ_SSCOFF), calculate the jitter attenuation by 20 × lg(DJ_MSSC / DJ_SSC), adjust the JMD settings so the value falls within the range specified in 5.8.3.2 for the selected baud rate;
6) set the pattern generator to output the JMD calibration pattern with sinusoidal phase modulation of 0.3 UI with a relative tolerance of 10 % peak to peak over a frequency range of 0.5 MHz to 50 MHz for the selected baud rate (see table F.1);
7) verify the level of modulation meets the requirements and record the peak to peak level as DJ_M (e.g., the independent verification of the 50 MHz test signal is a jitter measurement by separate means from the JMD under calibration) measured with:
   A) a time interval error plot with constant frequency clock on a real time oscilloscope;
   B) an equivalent time oscilloscope with histogram and constant frequency clock;
   C) a bit error rate tester (BERT) using a constant frequency clock; or
   D) a spectral analysis with the Bessel expansion of angle modulated sidebands;
8) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_MOFF;
9) turn on the sinusoidal phase modulation, record the reported DJ as DJ_MON;
10) calculate the following:
   A) the difference in reported DJ (i.e., DJ_MM = DJ_MON - DJ_MOFF); and
   B) the -3 dB value (i.e., DJ_3DB = DJ_MM × 0.707);
11) adjust the frequency of the PJ source to the specified -3 dB frequency for the baud rate being tested per table 37 (5.8.3.2), measure the reported DJ difference between PJ on versus PJ off (i.e., DJ = DJ_ON - DJ_OFF) and compare DJ to DJ_3DB. Shift the frequency of the PJ source until the

reported DJ difference between PJ on and PJ off is equal to DJ_3DB. The PJ frequency is the -3 dB bandwidth of the JTF, record this value as F_3DB;
12) adjust the JMD settings to bring F_3DB to the corner frequency specified in table 37 (5.8.3.2) for the baud rate being tested;
13) repeat steps (4) through (12) until both the jitter attenuation and -3 dB frequency are in the acceptable ranges;
14) check the peaking of the JTF, set the pattern generator to output the JMD calibration pattern with sinusoidal phase modulation of 0.3 with a relative tolerance of 10 % UI peak to peak at F_3DB, increase the frequency of the modulation to find the maximum reported DJ (i.e., it is not necessary to increase beyond 20 MHz), measure the reported DJ difference between PJ on versus PJ off as DJ_PK = DJ_PKON - DJ_PKOFF; and
15) calculate the JTF Peaking value: 20 × lg (DJ_PK / DJ_MM), verify that the peaking is below the limits set in 5.8.3.2, if peaking is above the limits repeat the procedure until all specifications are met.

F.12.2.3 Calibration of the JMD for testing non-SSC configurations

This test procedure verifies the JTF attenuation and the JTF bandwidth for SAS devices that:

a) support training with no SSC support; or
b) do not support training.

This procedure is performed for each baud rate tested (e.g., 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s as applicable):

1) set the pattern generator to output the JMD calibration pattern with a sinusoidal phase modulation of 1.5 UI with a relative tolerance of 10 % peak to peak at f_{baud}/33.333 kHz (see table F.2);
2) verify the level of modulation meets the requirements and record the peak to peak level as DJ_LF (e.g., the independent, separate means of verification of the low frequency test signal is equivalent to a frequency demodulator or wide range phase demodulator), measured with:
   A) continuously gated frequency counter;
   B) a time interval error plot with constant frequency clock on a real time oscilloscope;
   C) an equivalent time oscilloscope; or
   D) a frequency demodulator;
3) apply the test signal to the JMD, turn off the sinusoidal phase modulation, record the reported DJ as DJ_LFOFF;
4) turn on the sinusoidal phase modulation, record the reported DJ as DJ_LFON;
5) calculate and record the reported DJ as DJ_MLF by subtracting the DJ with modulation off from DJ with modulation on (i.e., DJ_MLF = DJ_LFON - DJ_LFOFF), calculate the jitter attenuation by 20 × lg (DJ_MLF / DJ_LF), adjust the JMD settings so the attenuation value falls within the range specified in table F.3; and
6) continue with the high frequency tests of the corner frequency and peaking by following steps (6) through (15) of in F.12.2.2, repeat the this procedure until all specifications are met.

Table F.2 — Low frequency jitter source calibration amplitudes

Baud rate (Gbit/s)	Phase modulation frequency (kHz)	Peak to peak modulation (UI)	Peak to peak modulation (ns)	Modulation tolerance
1.5	45	1.5	1.0	± 0.15
3	90	1.5	0.5	± 0.15
6	180	1.5	0.25	± 0.15
12	360	1.5	0.125	± 0.15

Table F.3 — Low frequency jitter attenuation targets

Baud rate (Gbit/s)	Phase modulation frequency (kHz)	Peak to peak modulation (UI)	Target attenuation (dB) [a] [b]	Target attenuation tolerance (dB)
1.5	45	1.5	26	± 1.5
3	90	1.5	26	± 1.5
6	180	1.5	26	± 1.5
12	360	1.5	26	± 1.5

[a] Target Attenuation = 20 × lg ((f / fc) / (1+ (f / fc)^{2})$^{0.5}$), where fc is the -3 dB frequency.
[b] This is derived from a nominal first-order frequency response.

Annex G
(informative)

Description of the included Touchstone models for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

G.1 Description of the included Touchstone models for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s overview

Touchstone models for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s are included with this standard to represent:

a) reference transmitter device termination (see 5.8.4.6.5 and G.2);
b) reference receiver device termination (see 5.8.5.7.3 and G.3); and
c) reference transmitter test load (see 5.6.5 and G.5).

Figure G.1 shows the circuit models used to create the Touchstone models of reference transmitter device termination and reference receiver device termination.

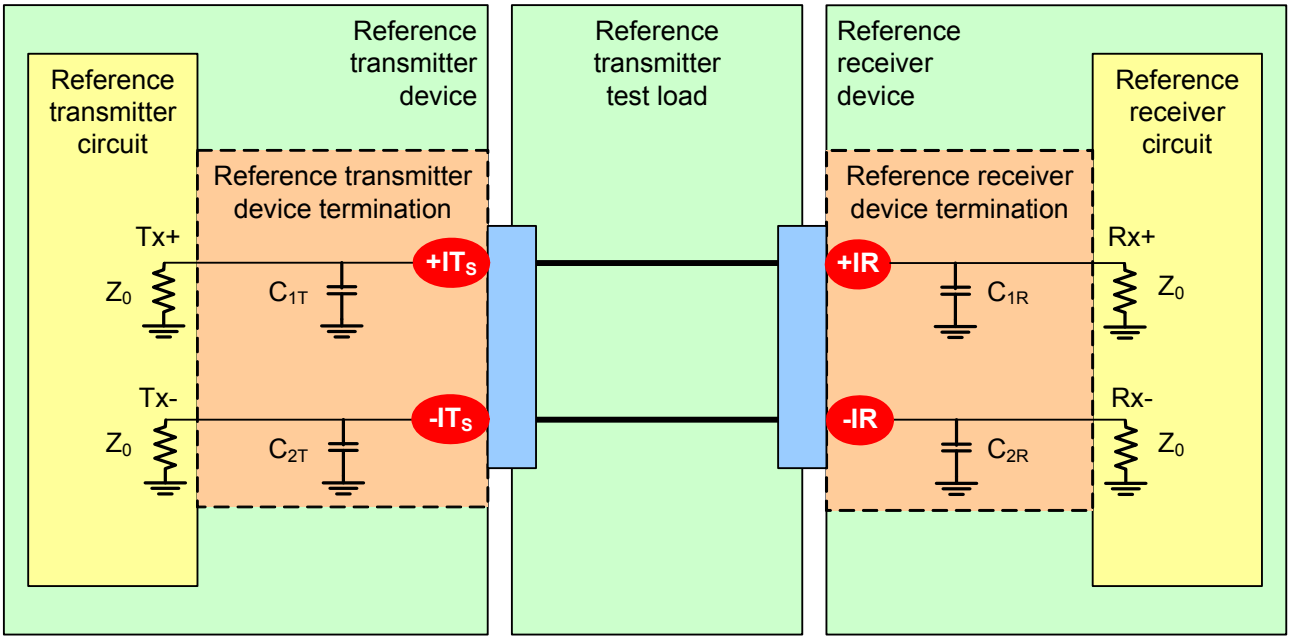


Figure G.1 — Reference transmitter device and reference receiver device termination circuit model

G.2 Reference transmitter device termination model for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

From the circuit model shown in figure G.1 (see G.1), the S-parameters of the reference transmitter device termination for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s were derived using the following calculations:

$$\tau_1 = \frac{Z_0 \times C_{1T}}{2}$$

$$\tau_2 = \frac{Z_0 \times C_{2T}}{2}$$

$$S_{11} = \frac{-s \times \tau_1}{1 + (s \times \tau_1)}$$

$$S_{12} = 0$$

$$S_{22} = \frac{-s \times \tau_2}{1 + (s \times \tau_2)}$$

$$S_{DDij} = S_{CCij} = \frac{S_{11} + S_{22}}{2}$$

$$S_{CDij} = S_{DCij} = \frac{S_{11} - S_{22}}{2}$$

where:

τ_1	is the Tx+ termination time constant;
τ_2	is the Tx- termination time constant;
Z_0	is the impedance as specified by this standard (i.e., 50 Ω);
C_{1T}	is the Tx+ termination capacitance; and
C_{2T}	is the Tx- termination capacitance.

Figure 146 (see 5.8.4.6.5) shows the graph of the S-parameters based on the following values:

a) Z_0 is set to 50 Ω;
b) C_{1T} is set to 0.5 pF, so τ_1 becomes 12.5 ps; and
c) C_{2T} is set to 2 pF, so τ_2 becomes 50 ps.

G.3 Reference receiver device termination model for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

From the circuit model shown in figure G.1 (see G.1), the S-parameters of the reference receiver device termination for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s were derived using the following calculations:

$$\tau_1 = \frac{Z_0 \times C_{1R}}{2}$$

$$\tau_2 = \frac{Z_0 \times C_{2R}}{2}$$

$$S_{11} = \frac{-s \times \tau_1}{1 + (s \times \tau_1)}$$

$$S_{12} = 0$$

$$S_{22} = \frac{-s \times \tau_2}{1 + (s \times \tau_2)}$$

$$S_{DDij} = S_{CCij} = \frac{S_{11} + S_{22}}{2}$$

$$S_{CDij} = S_{DCij} = \frac{S_{11} - S_{22}}{2}$$

where:

τ_1 is the Rx+ termination time constant;

τ_2 is the Rx- termination time constant;

Z_0 is the impedance as specified by this standard (i.e., 50 Ω);

C_{1R} is the Rx+ termination capacitance; and

C_{2R} is the Rx- termination capacitance.

Figure 160 (see 5.8.5.7.3) shows the graph of the S-parameters based on the following values:

a) Z_0 is set to 50 Ω;
b) C_{1R} is set to 2 pF, so τ_1 becomes 50 ps; and
c) C_{2R} is set to 0.5 pF, so τ_2 becomes 12.5 ps.

G.4 Generic return loss circuit model for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Figure G.2 shows a generic circuit model for return loss for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, upon which the circuit models for transmitter device termination in G.2 and receiver device termination in G.3 are based.

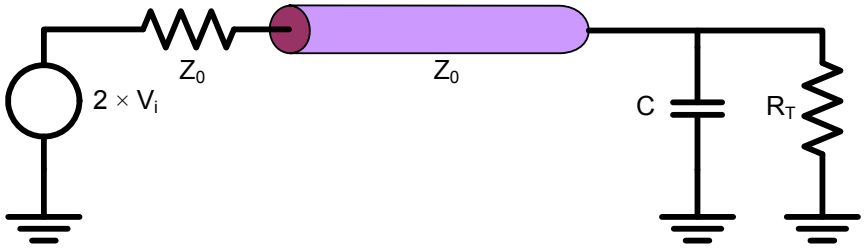


Figure G.2 — Generic return loss circuit model

$|S_{11}|$ (i.e., negative return loss) may be derived by defining points on a curve using the following calculations:

$$LF = 20 \times \log_{10}\left(\frac{tol}{2 + tol}\right)$$

$$R_T = Z_0 \times (1 + tol)$$

$$F_{zero} = \frac{tol}{(2 \times \pi \times R_T \times C \times (1 + tol))}$$

$$F_{pole} = \frac{2 + tol}{(2 \times \pi \times R_T \times C \times (1 + tol))}$$

where:

LF is the low frequency asymptote of $|S_{11}|$;

tol is the tolerance of R_T;

Z_0 is the impedance specified by this standard (i.e., 50 Ω);

R_T is the far end load;

C is the far end capacitance;

F_{zero} is the frequency at which a 20 dB/decade asymptote intersects the LF asymptote; and

F_{pole} is the frequency at which a 20 dB/decade asymptote intersects the 0 dB asymptote.

Because the effects of the far end load are not significant, the equations may be simplified as follows:

$$LF \sim 20 \times \log_{10}\left(\frac{tol}{2}\right)$$

$$F_{zero} \sim \frac{tol}{(2 \times \pi \times R_T \times C)}$$

$$F_{pole} \sim \frac{1}{(\pi \times R_T \times C)}$$

Using the simplified equations, $|S_{11}|$ may be derived from LF, F_{zero}, and F_{pole} as shown in figure G.3.

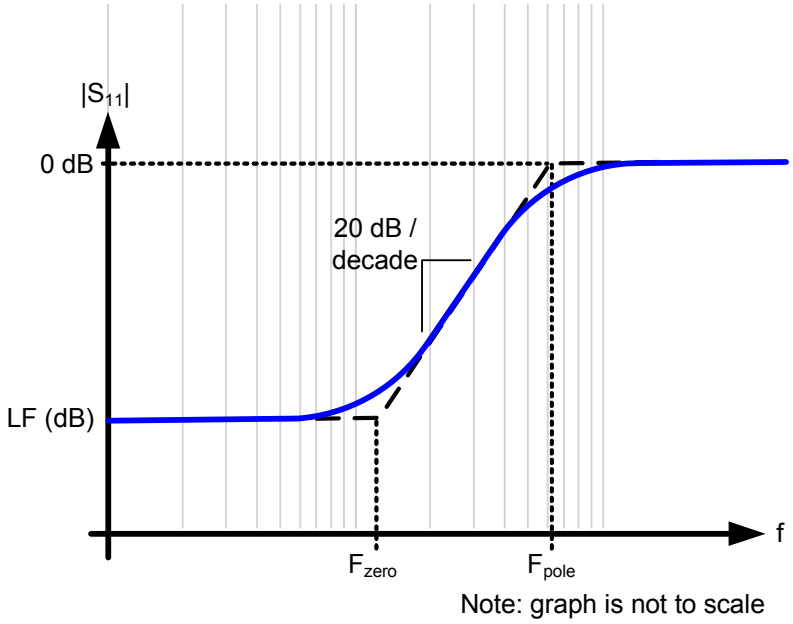


Figure G.3 — Generic return loss model $|S_{11}|$

G.5 Reference transmitter test load for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The Touchstone model of the reference transmitter test load for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.6.5) is based on physical measurements.

The following components of a TxRx connection were measured:

a) an etch length of 50.8 mm with an etch width of 177.8 µm between IT_S (see 5.3.6.5.4) and the Mini SAS 4x cable plug in a Nelco® 4000-13 material environment. This etch is part of the transmitter device;
b) a 10 m Mini SAS 4x cable assembly using 24 AWG solid wire from pin B5 to pin A5 and from pin B6 to pin A6 (see 5.4.3.4.1.3); and
c) an etch length of 50.8 mm with an etch width of 177.8 µm between IR (see 5.3.7.4.3) and the Mini SAS 4x cable plug in a Nelco® 4000-13 material environment. This etch is part of the receiver device.

NOTE 14 - Nelco® 4000-13 material is a product supplied by Park Electrochemical Corporation. This information is given for the convenience of users of this standard and does not constitute an endorsement by ANSI or ISO. Equivalent products ~~may be used~~are ~~-~~acceptable if they lead to the same results.

Although the etches between the transmission points and probe points add extra loss to the TxRx connection, they are considered to be an acceptable amount of loss for simulation purposes.

The following list of equipment was used to perform the measurement:

a) Agilent N1957B Physical Layer Test System (PLTS), including:
   A) Agilent E8364B PNA Network Analyzer (10 MHz to 50 GHz);
   B) Agilent N4421B S-parameter Test Set (10 MHz to 50 GHz); and
   C) Agilent N1930B Physical Layer Test System Software version 3.01;

   and

b) Molex 26-circuit External iPass™ Test Fixture (PCB 73931-2540).

NOTE 15 - The Agilent Technologies® Corporation and Molex® equipment are examples of a suitable product(s) available commercially. iPass™ is a product supplied by Molex Incorporated. This information is given for the convenience of users of this standard and does not constitute an endorsement by ANSI or ISO of these products. Equivalent products ~~may be used~~are ~~-~~acceptable if they lead to the same results.

The equipment was interconnected as shown in figure G.4.

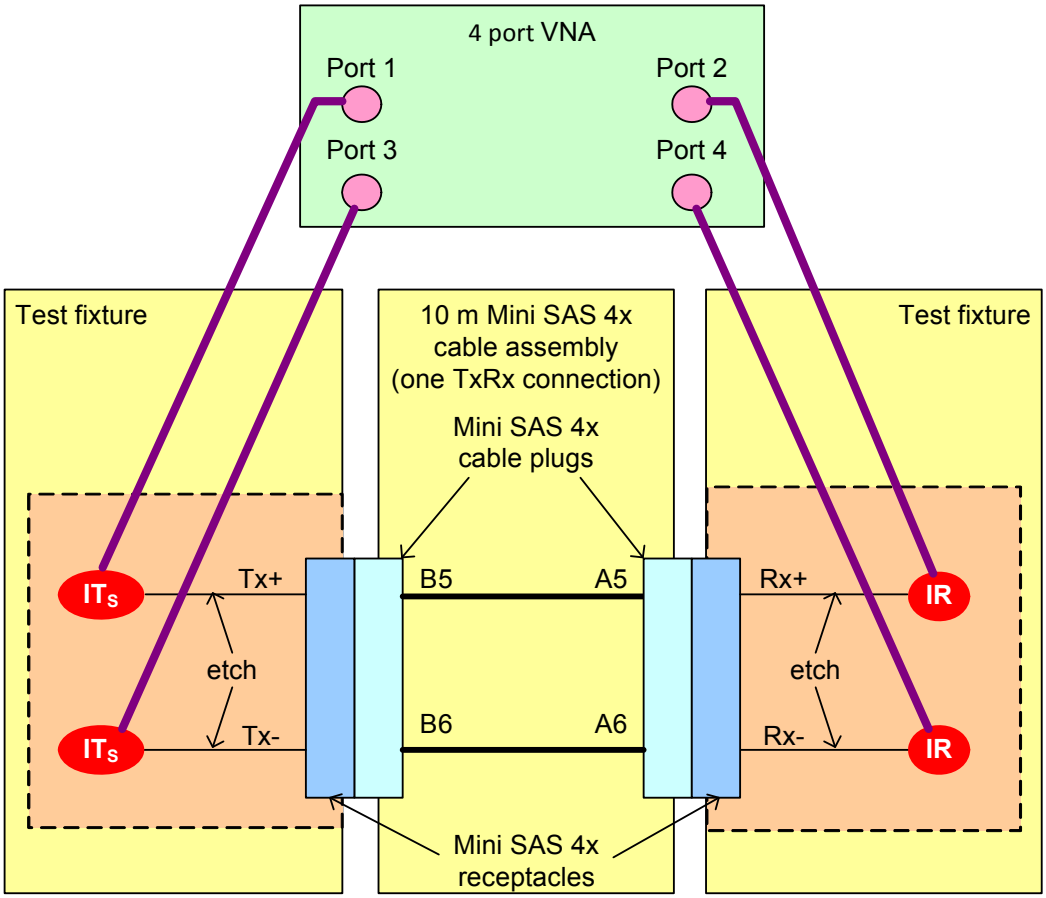


Figure G.4 — Reference transmitter test load measurement setup

The Short-Open-Load-Through (SOLT) calibration procedure should be run before generating the S-parameters.

Samples were taken from 10 MHz to 20 GHz in 1 MHz steps.

Figure 130 (see 5.6.5) shows the graph of the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

Figure G.5 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 20 GHz.

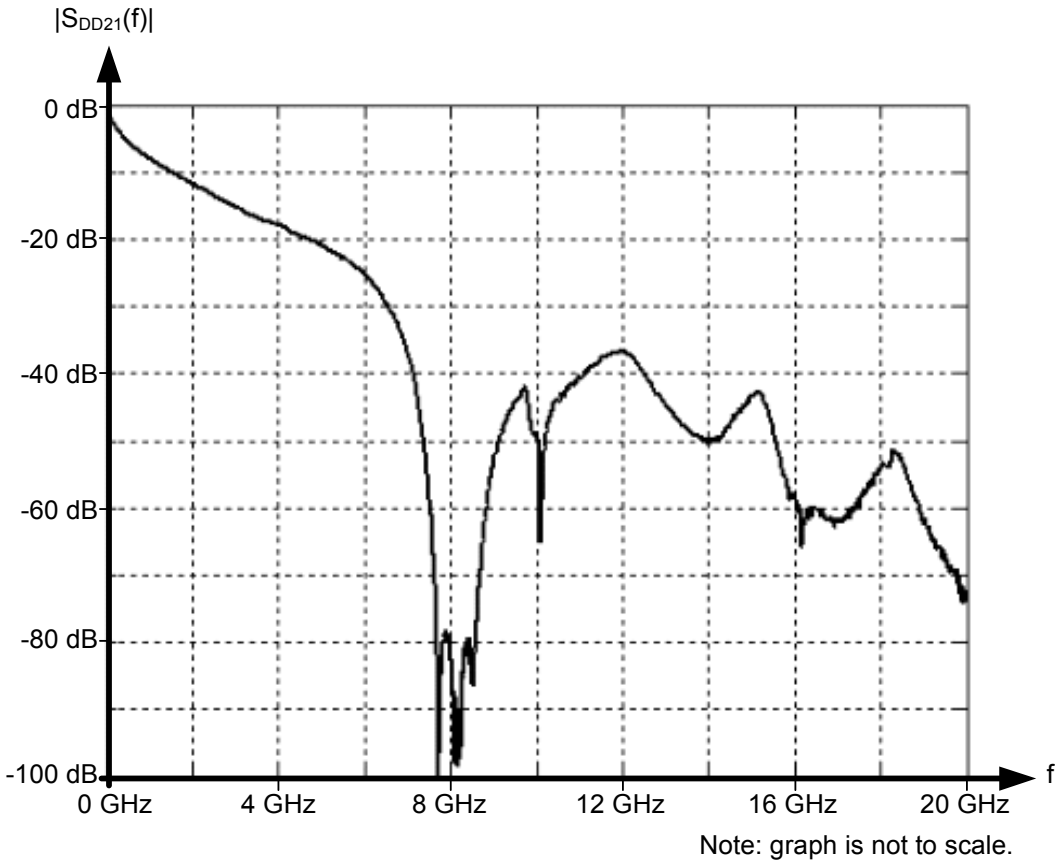


Figure G.5 — Reference transmitter test load $|S_{DD21}(f)|$ up to 20 GHz

Annex H
(informative)

Mini SAS 4x active cable assembly power supply and voltage detection circuitry

SAS devices and expander devices with Mini SAS 4x active receptacle connectors should operate with Mini SAS 4x passive cables which have the Vcc pin tied to ground. There should be a mechanism that turns on the power to the receptacle only when active cable assembly presence is detected to avoid shorting power to ground. A SENSE pin is provided (see 5.4.3.4.1.5) to detect if an active cable assembly is present. This pin may also be used to detect the status of a specific port or to implement other features within a switch device.

Figure H.1 is an example design utilizing a dual comparator to determine from the SENSE pin on the active cable assembly plug. If an active cable assembly is present, then the circuit supplies power to the receptacle upon detection of an active cable assembly. For proper function during hot plug, B1 and B13 should be mated to the Mini SAS 4x cable plug connector (see 5.4.3.4.1.1) simultaneously.

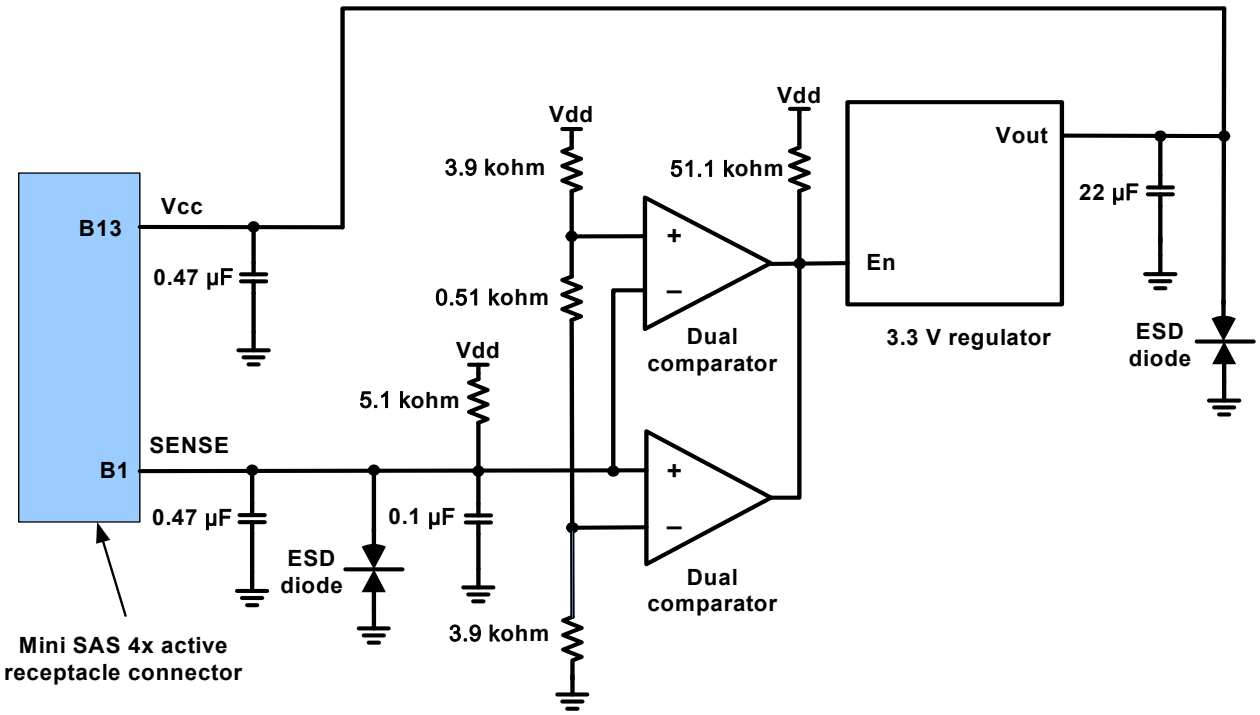


Figure H.1 — Dual comparator design for active cable assembly detection

The power supply characteristics are specified in table 25 (see 5.4.3.4.1.5). The type of power supply may either be a switching regulator or a linear regulator.

Annex I
(informative)

Recommended electrical performance limits for mated connector pairs supporting rates of 12 Gbit/s

The recommended electrical performance limits for connector mated pairs supporting rates of 12 Gbit/s are defined in table I.1 and shown in figure I.1. The TxRx connection shall meet the requirements of 5.5.6 or 5.5.7 for 12 Gbit/s applications.

Table I.1 — Recommended electrical performance limits for mated connector pairs supporting rates of 12 Gbit/s

Characteristic [c] [d]	Units	Value
Maximum near-end crosstalk (NEXT) for each signal pair [e] [f]	dB	-39
Maximum far-end crosstalk (FEXT) for each signal pair [e] [f]	dB	-39
Maximum S_{DD22}	dB	-12
Maximum S_{CC22}	dB	-3.0
Minimum S_{DD21}	dB	-1.0

[c] All measurements apply to connector mated pairs supporting rates of 12 Gbit/s and include the mounting footprint or wire termination.

[d] All characteristic values apply to the frequency range from 100 MHz to 6 000 MHz. The measurement output should include results to a minimum of 20 GHz.

[e] Determine all near-end and far-end significant crosstalk transfer modes. The sum of the crosstalk transfer ratios is measured in the frequency domain. The following equation details the summation process of the valid near-end crosstalk sources:

$$TotalNEXT(f) = 10 \times \log \sum_{1}^{n} 10^{\langle NEXT(f)/10 \rangle}$$

where:

f frequency; and

n number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

The following equation details the summation process of the valid far-end crosstalk sources:

$$TotalFEXT(f) = 10 \times \log \sum_{1}^{n} 10^{\langle FEXT(f)/10 \rangle}$$

where:

f frequency; and

n number of the far-end crosstalk source.

All FEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

[f] Total TxRx connection crosstalk should be at least 15 dB less than its total insertion loss. A total TxRx connection crosstalk of -39 dB implies an acceptable TxRx connection total insertion loss of 24 dB as shown in figure C.1.

Figure I.1 shows the recommended $|S_{DD21}|$, $|S_{CC22}|$, $|S_{DD22}|$, NEXT, and FEXT limits for connector mated pairs supporting rates of 12 Gbit/s.

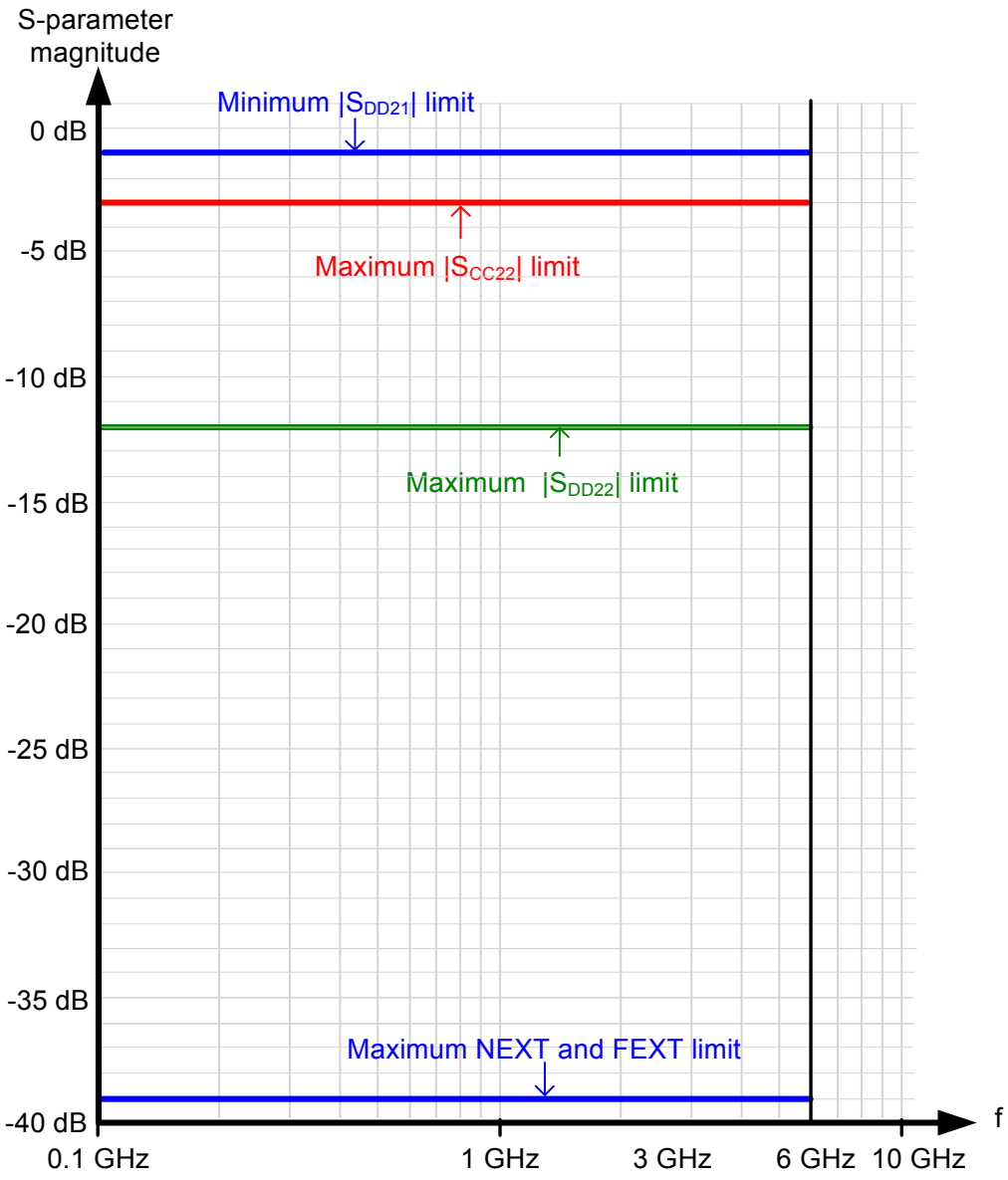


Figure I.1 — Recommended $|S_{DD21}|$, $|S_{CC22}|$, $|S_{DD22}|$, NEXT, and FEXT limits for connector mated pairs supporting rates of 12 Gbit/s

Annex J
(informative)

Recommended electrical performance limits for mated connector pairs supporting rates of 22.5 Gbit/s

Recommended electrical characteristics for connector mated pairs supporting rates of 22.5 Gbit/s are defined in table J.1 and table J.2, and illustrated in figure J.1, figure J.2, figure J.3, and figure J.4. The characteristics include the test fixtures in addition to the mated connector pair. The test fixtures should comply with the electrical characteristics defined in table J.3. The TxRx connection shall meet the requirements of tbd for 22.5 Gbit/s applications.

A weighting function is used to scale the magnitude of electrical characteristic equations to provide an approximation of the spectral content of a signal up to the baud rate. The weighting function is defined by the following equation:

$$W(f) = \mathrm{sinc}^2\left(\frac{f}{f_b}\right)\left[\frac{1}{1+\left(\frac{f}{f_t}\right)^4}\right]\left[\frac{1}{1+\left(\frac{f}{f_r}\right)^8}\right]$$

where:

$$f_t = \frac{0.2365}{T_t}$$

and:

sinc*(x)* is $\frac{\sin(\pi x)}{\pi x}$;

f is the frequency of the signal in Hz;

f_b is the baud rate (i.e., 22.5 GHz);

f_r is the 3dB reference receiver bandwidth = $\frac{3}{4}f_b$ (i.e., 16.9 GHz); and

T_t is the rise time.

Insertion Loss Deviation is the difference between the measured insertion loss (S_{DD21}) and the fitted insertion loss ($S_{DD21\ fit}$) as defined by the following equations:

$$ILD(f) = S_{DD21}(f) - S_{DD21\ fit}(f)$$

where:

$$S_{DD21fit}(f) = a_0 + a_1\sqrt{\frac{f}{f_b}} + a_2\frac{f}{f_b} + a_4\left(\frac{f}{f_b}\right)^2 \mathrm{dB}$$

where:

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = \langle F^T F \rangle^{-1} F^T [|S_{DD21}| \times S_{DD21}]$$

and

$$F = \begin{bmatrix} |S_{DD21}(f_1)| & |S_{DD21}(f_1)|\sqrt{\frac{f_1}{f_b}} & |S_{DD21}(f_1)|\frac{f_1}{f_b} & |S_{DD21}(f_1)|\left(\frac{f_1}{f_b}\right)^2 \\ |S_{DD21}(f_2)| & |S_{DD21}(f_2)|\sqrt{\frac{f_2}{f_b}} & |S_{DD21}(f_2)|\frac{f_2}{f_b} & |S_{DD21}(f_2)|\left(\frac{f_2}{f_b}\right)^2 \\ \cdots & \cdots & \cdots & \cdots \\ |S_{DD21}(f_N)| & |S_{DD21}(f_N)|\sqrt{\frac{f_N}{f_b}} & |S_{DD21}(f_N)|\frac{f_N}{f_b} & |S_{DD21}(f_N)|\left(\frac{f_N}{f_b}\right)^2 \end{bmatrix}$$

Table J.1 defines the recommended electrical characteristics for connector mated pairs supporting rates of 22.5 Gbit/s.

Table J.1 — Recommended electrical characteristic limits for mated connector pairs supporting rates of 22.5 Gbit/s

Characteristic [a]	Equation	Units	Range
Minimum $S_{DD21}(f)$ [b]	$-0.08\sqrt{f/1\times10^9} - 0.336(f/1\times10^9)$	dB	$50\text{MHz} \le f \le \frac{3}{4}f_b$
Maximum $S_{DD21}(f)$ [b]	$-0.12 - 0.475\sqrt{f/1\times10^9} - 0.364(f/1\times10^9)$	dB	$50\text{MHz} \le f \le \frac{3}{4}f_b$
Maximum $S_{DD22}(f)$ [c]	$-20\log[W(f)^{0.353}] - 12$	dB	$50\text{MHz} \le f \le \frac{3}{4}f_b$
Maximum $S_{CD21}(f)$ [d]	$\begin{cases} -25 + 20\left(\frac{f}{f_b}\right) \\ -18 + 6\left(\frac{f}{f_b}\right) \end{cases}$	dB	$\begin{cases} 50\text{MHz} \le f \le \frac{f_b}{2} \\ \frac{f_b}{2} < f \le \frac{3}{4}f_b \end{cases}$
Maximum $S_{CD22}(f)$ [e]	$\begin{cases} -25 + 20\left(\frac{f}{f_b}\right) \\ -18 + 6\left(\frac{f}{f_b}\right) \end{cases}$	dB	$\begin{cases} 50\text{MHz} \le f \le \frac{f_b}{2} \\ \frac{f_b}{2} < f \le \frac{3}{4}f_b \end{cases}$

[a] These characteristics apply to all Tx pairs.
[b] See figure J.1.
[c] See figure J.2.
[d] See figure J.3.
[e] See figure J.4.

Figure J.1 shows the recommended $|S_{DD21}|$ limits for connector mated pairs supporting rates of 22.5 Gbit/s.

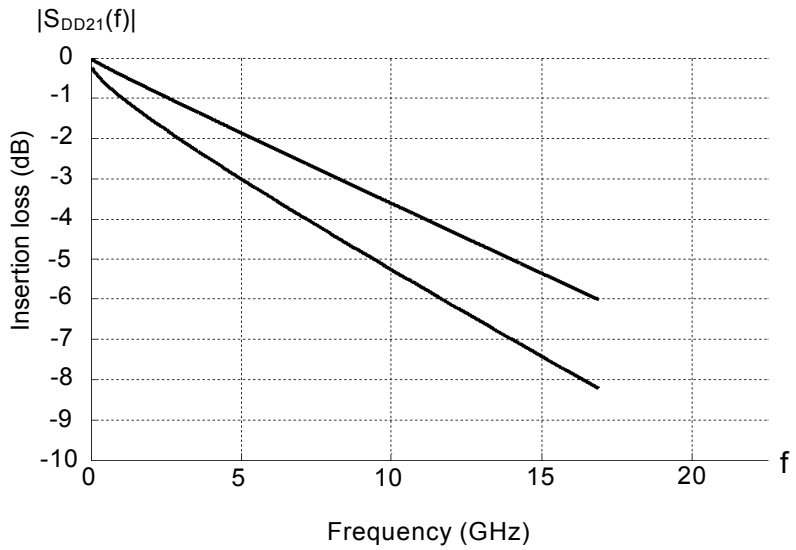


Figure J.1 — Recommended $|S_{DD21}|$ limits for connector mated pairs supporting rates of 22.5 Gbit/s

Figure J.2 shows the recommended $|S_{DD22}|$ limit for connector mated pairs supporting rates of 22.5 Gbit/s.

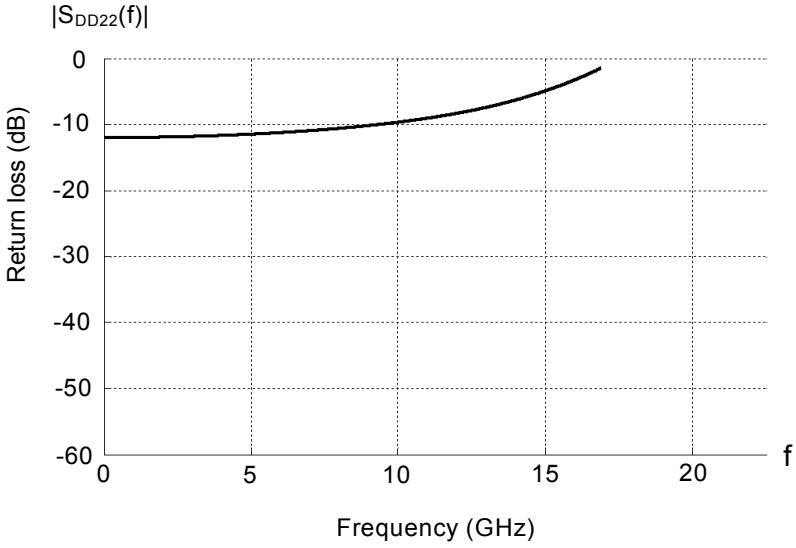


Figure J.2 — Recommended $|S_{DD22}|$ limit for connector mated pairs supporting rates of 22.5 Gbit/s

Figure J.3 shows the recommended $|S_{CD21}|$ limit for connector mated pairs supporting rates of 22.5 Gbit/s.

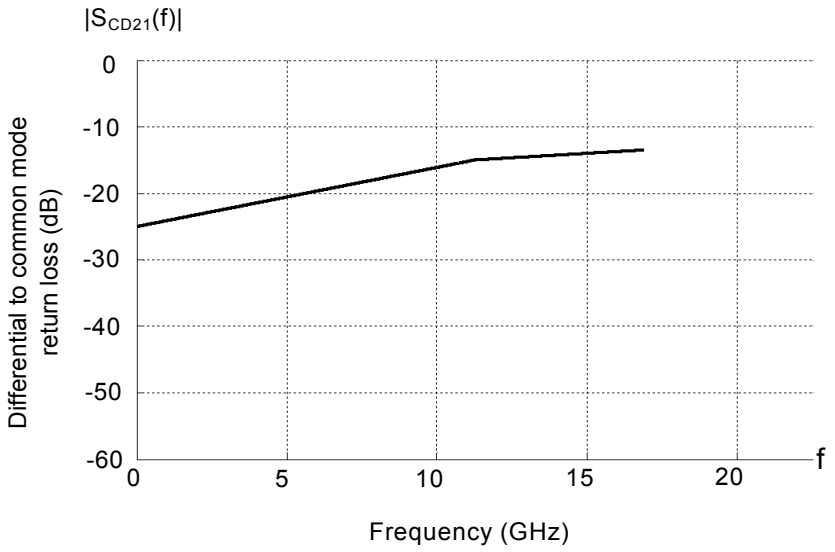


Figure J.3 — Recommended |SCD21| limit for connector mated pairs supporting rates of 22.5 Gbit/s

Figure J.4 shows the recommended $|S_{CD22}|$ limit for connector mated pairs supporting rates of 22.5 Gbit/s.

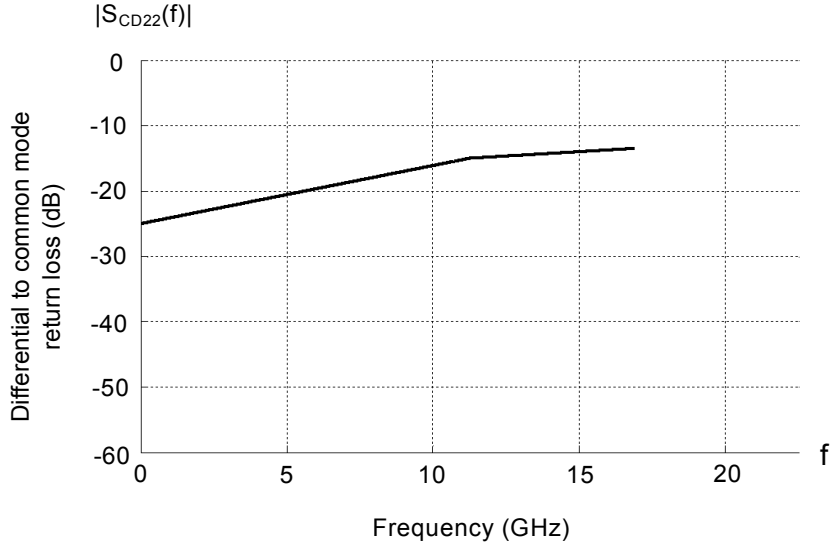


Figure J.4 — Recommended |SCD22| limit for connector mated pairs supporting rates of 22.5 Gbit/s

ICN is the weighted RMS value of multi-disturber near/far-end crosstalk loss (MDNEXT/MDFEXT, respectively). ICN is defined by the following equations:

$$ICN = \sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2}$$

$$\sigma_{nx} = \sqrt{2\Delta f \sum_n W_{nt}(f_n) 10^{-MDNEXT(f_n)/10}}$$

$$\sigma_{fx} = \sqrt{2\Delta f \sum_{n} W_{ft}(f_n) 10^{-\mathrm{MDFEXT}(f_n)/10}}$$

$$\mathrm{MDNEXT}(f) = -10\log\left(\sum_{\mathrm{NEXTaggressors}} 10^{-\frac{\mathrm{NEXT}(f)}{10}}\right)\mathrm{dB}$$

$$\text{for } 50\mathrm{MHz} \le f \le \frac{3}{4} f_b$$

$$\mathrm{MDFEXT}(f) = -10\log\left(\sum_{\mathrm{FEXTaggressors}} 10^{-\frac{\mathrm{FEXT}(f)}{10}}\right)\mathrm{dB}$$

$$\text{for } 50\mathrm{MHz} \le f \le \frac{3}{4} f_b$$

$$W_{nt}(f) = \left(\frac{A_{nt}^2}{4 f_b}\right) \mathrm{sinc}^2\left(\frac{f}{f_b}\right) \left[\frac{1}{1+\left(\frac{f}{f_{nt}}\right)^4}\right] \left[\frac{1}{1+\left(\frac{f}{f_r}\right)^8}\right]$$

$$W_{ft}(f) = \left(\frac{A_{ft}^2}{4 f_b}\right) \mathrm{sinc}^2\left(\frac{f}{f_b}\right) \left[\frac{1}{1+\left(\frac{f}{f_{ft}}\right)^4}\right] \left[\frac{1}{1+\left(\frac{f}{f_r}\right)^8}\right]$$

where:

$$f_{nt} = f_{ft} = f_t = \frac{0.2365}{T_{nt}} = \frac{0.2365}{T_{ft}}$$

and

f is the frequency of the signal in Hz;

f_b is the baud rate (i.e., 22.5 GHz);

T_{nt} is the near end rise time;

T_{ft} is the far end rise time;

A_{nt} is the near end Tx peak to peak voltage (i.e., 1200 mV); and

A_{ft} is the far endTx peak to peak voltage (i.e., 1200 mV).

Table J.2 defines the recommended ICN limits for mated connector pairs supporting rates of 22.5 Gbit/s.

Table J.2 — Recommended ICN limits for mated connector pairs supporting rates of 22.5 Gbit/s

Connector type [a]	Value [b]	Frequency range
SAS Drive connectors	3.5 mV	$50\text{MHz} \le f \le \frac{3}{4} f_b$
All other SAS connectors	3 mV	$50\text{MHz} \le f \le \frac{3}{4} f_b$

[a] See table 4 for the list of SAS connectors by connector type.
[b] Applies to all Rx pairs.

Test fixtures should comply with the electrical characteristics defined in table J.3.

Table J.3 — Recommended test fixture electrical characteristics

Characteristic	Units	Value
Maximum material relative dielectric constant at 10 GHz		4.0
Maximum material loss tangent at 10 GHz		0.01
Minimum footprint via length (press fit connectors only)	mm	1.0
Minimum signal trace routing width	mm	0.114

Annex K
(informative)

SAS icons

A SAS icon should be included on or near all connectors used by devices compliant with both this standard and SPL-4. Icons indicating support of 12 Gbit/s are shown. If only speeds slower than 12 Gbit/s are supported, then contact the SCSI Trade Association for the appropriate icons.

NOTE 16 - Contact the SCSI Trade Association (see http://www.scsita.org) for versions of the SAS icons in various graphics formats.

Figure K.1 shows the primary SAS icon.

Figure K.1 — SAS primary icon

Figure K.2 shows an alternate SAS icon that may be used instead of the primary SAS icon when the area for the icon is small.

Figure K.2 — SAS alternate icon

Figure K.3 shows the MultiLink SAS icon.

Figure K.3 — MultiLink SAS icon

Editor's Note 5: Update to 24 Gbit/s

Annex L
(informative)

Standards bodies contact information

Table L.1 shows standards bodies and their web sites.

Table L.1 — Standards bodies

Abbreviation	Standards body	Web site
ANSI® [a]	American National Standards Institute	http://www.ansi.org
DIN	German Institute for Standardization	http://www.din.de
IEC® [b]	International Electrotechnical Commission	http://www.iec.ch
IEEE® [c]	Institute of Electrical and Electronics Engineers	http://www.ieee.org
INCITS	International Committee for Information Technology Standards	http://www.incits.org
ISO® [d]	International Organization for Standardization	http://www.iso.ch
ITIC	Information Technology Industry Council	http://www.itic.org
JIS	Japanese Industrial Standards Committee	http://www.jisc.co.jp
T10	INCITS T10 SCSI storage interfaces	http://www.t10.org
T11	INCITS T11 Fibre Channel interfaces	http://www.t11.org
T13	INCITS T13 ATA storage interface	http://www.t13.org

[a] ANSI is a registered trademark of the American National Standards Institute.
[b] IEC is a registered trademark of the International Electrotechnical Commission.
[c] IEEE is a registered trademark of the Institute of Electrical Electronics Engineers, Inc.
[d] ISO is a registered trademark of the International Organization for Standardization.

Bibliography

ANSI INCITS 451-2008, *Information technology - AT Attachment-8 ATA/ATAPI Architecture Model (ATA8-AAM).*

ANSI INCITS 467-2011, *SCSI Stream Commands - 3 (SSC-3).*

ISO/IEC 14776-223, *Fiber Channel Protocol - 3 (FCP-3).*

ISO/IEC 14776-323, *SCSI Block Commands - 3 (SBC-3)* (T10/1799-D) (under consideration).

ISO/IEC 14776-922, *SCSI/ATA Translation - 3 (SAT-3)* (T10/2126-D) (under consideration).

ISO/IEC 14776-115, *SCSI Paralell Interfdace - 5 (SPI-5)* (T10/1525-D).

ISO/IEC 24739-201*, ATA/ATAPI Command Set - 2 (ACS-2)*.

John R. Barry, Edward A. Lee, and David G. Messerschmitt, *Digital Communication - Third Edition*. Kluwer Academic Publishing, 2003.