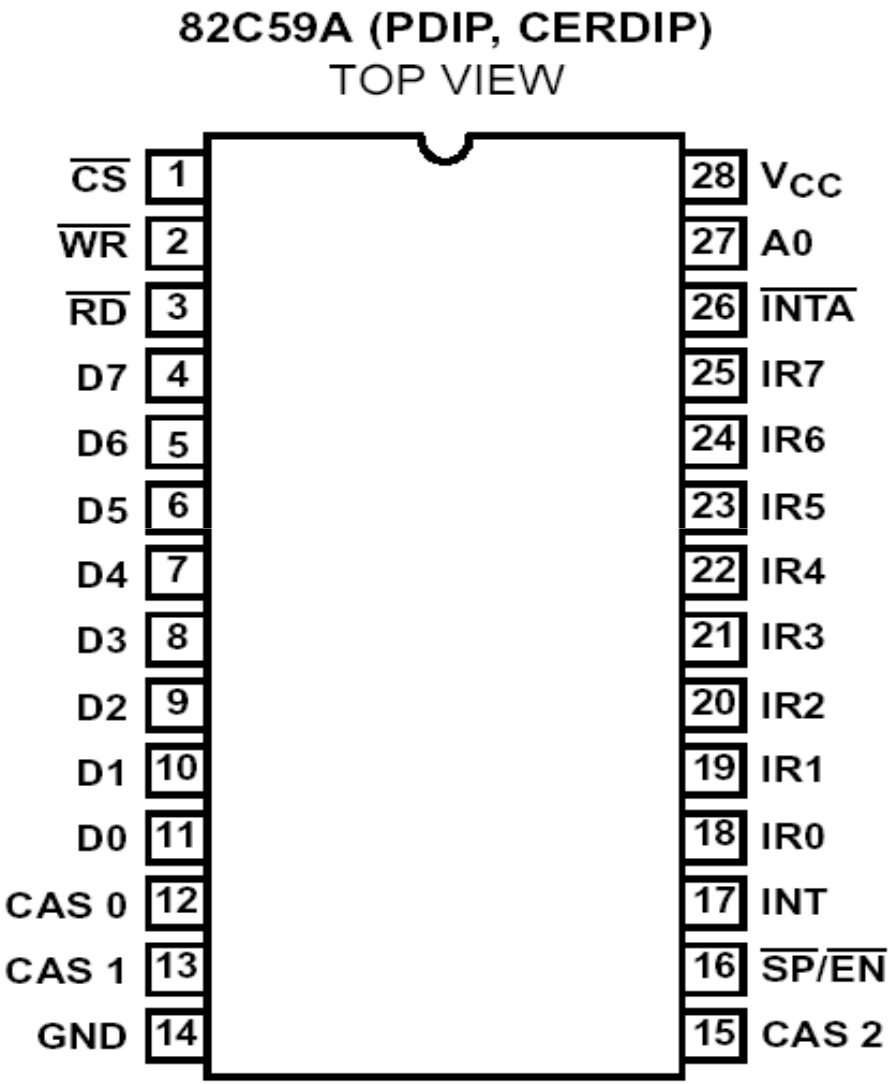
8259

Programmable Interrupt Controller

8259 Features

- 8259 is **Programmable Interrupt Controller (PIC)**
- It is a tool **for managing the interrupt requests**.
- 8259 is a very **flexible** peripheral controller chip:
  - PIC can deal with **up to 64 interrupt inputs**
  - interrupts can be **masked individually**.
  - **various priority schemes** can also programmed.

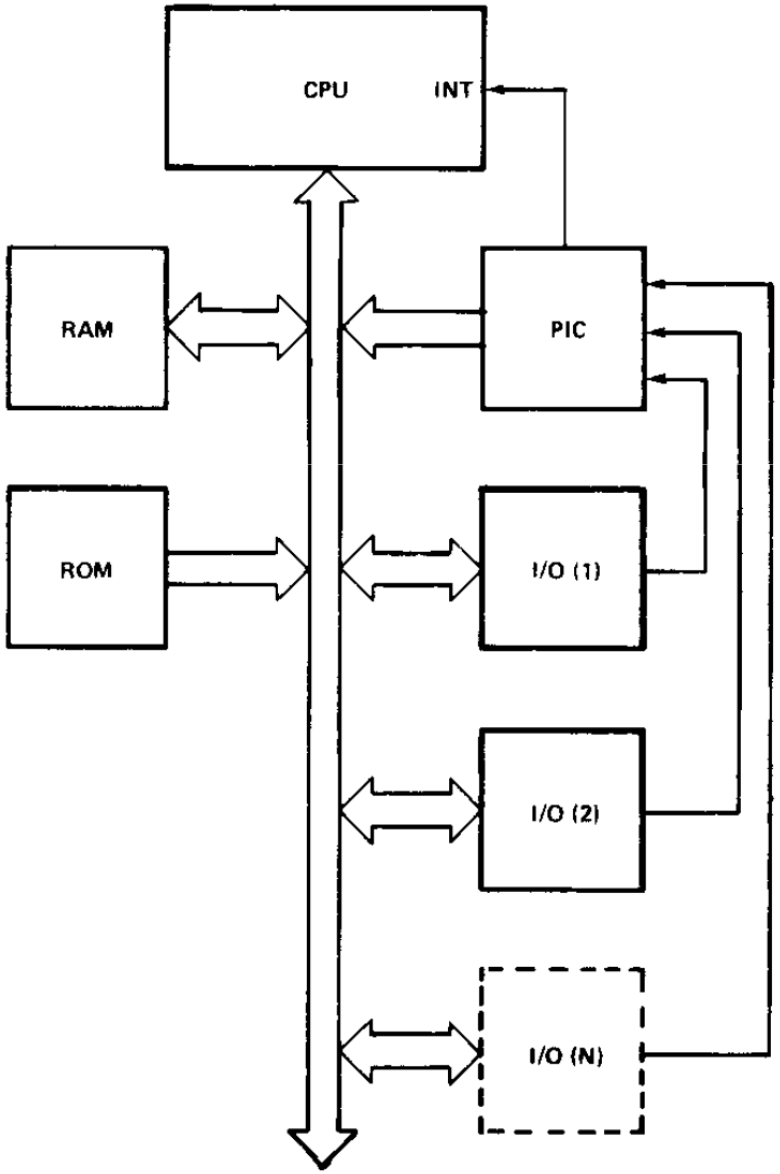
8259 Pin Diagram

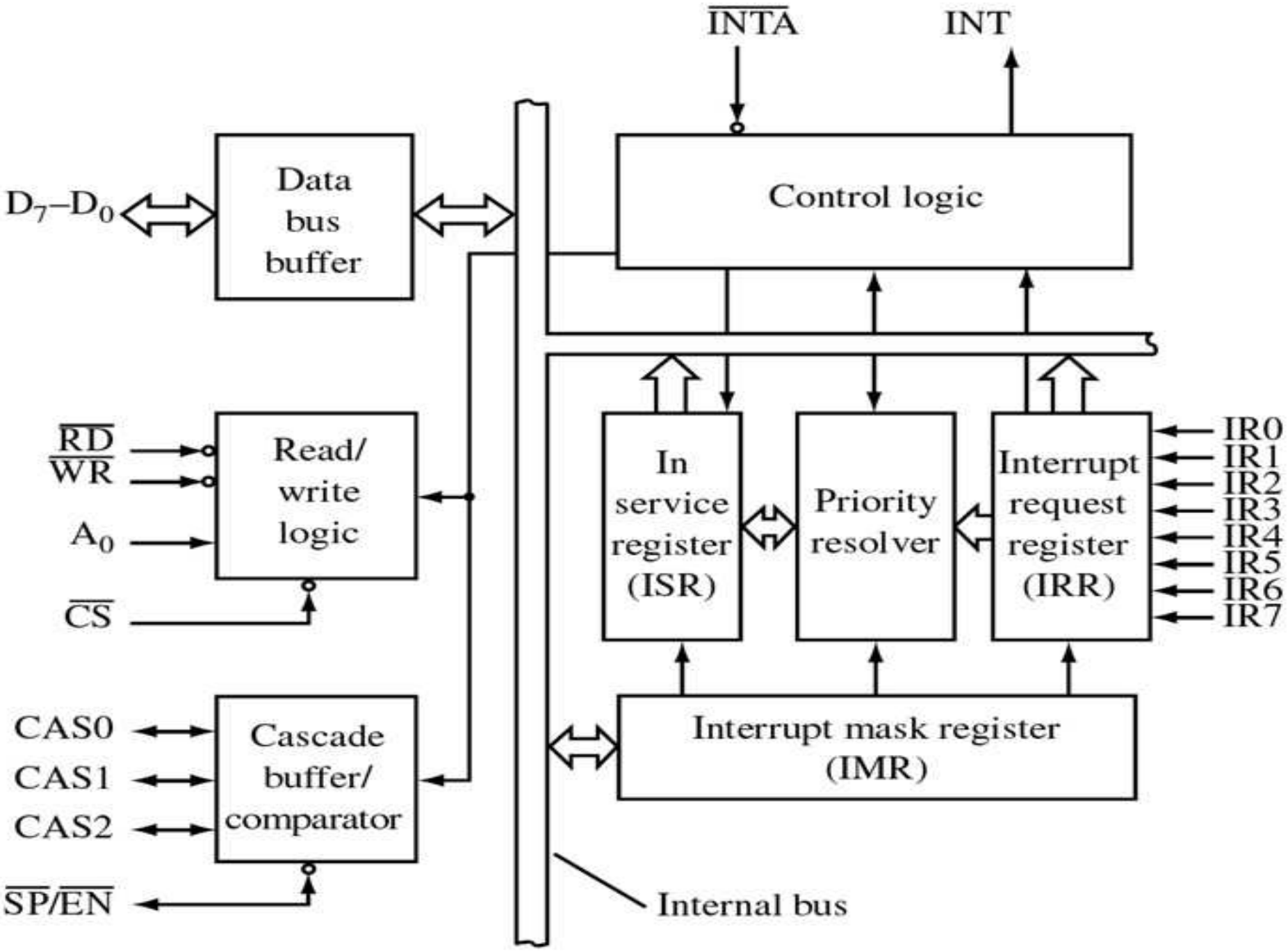


Pin Details

Symbol	Pin No.	Type	Name and Function
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

Interfacing 8259




INTA
INT
Data bus buffer
D7–D0
Control logic
RD
WR
A0
CS
Read/ write logic
In service register (ISR)
Priority resolver
Interrupt request register (IRR)
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS0
CAS1
CAS2
Cascade buffer/ comparator
SP/EN
Interrupt mask register (IMR)
Internal bus

Working of 8259

1. One or more of the **INTERRUPT REQUEST** lines (IR0 – IR7) are raised high, setting the corresponding IRR bit(s).

2. The 8259A evaluates these requests, and sends an **INT to the CPU**, if appropriate.

3. The CPU acknowledges the INT and responds with an **INTA*** pulse.

4. Upon receiving an INTA* from the CPU group, the **highest priority ISR bit is set and the corresponding IRR bit is reset**.

Working of 8259

5. Then 8086 will send **one more INTA** pulse to 8259.

   - **On this second interrupt acknowledge cycle, 8259 will send an interrupt vector byte of data to the CPU, which is a pointer of the interrupt to be processed.**

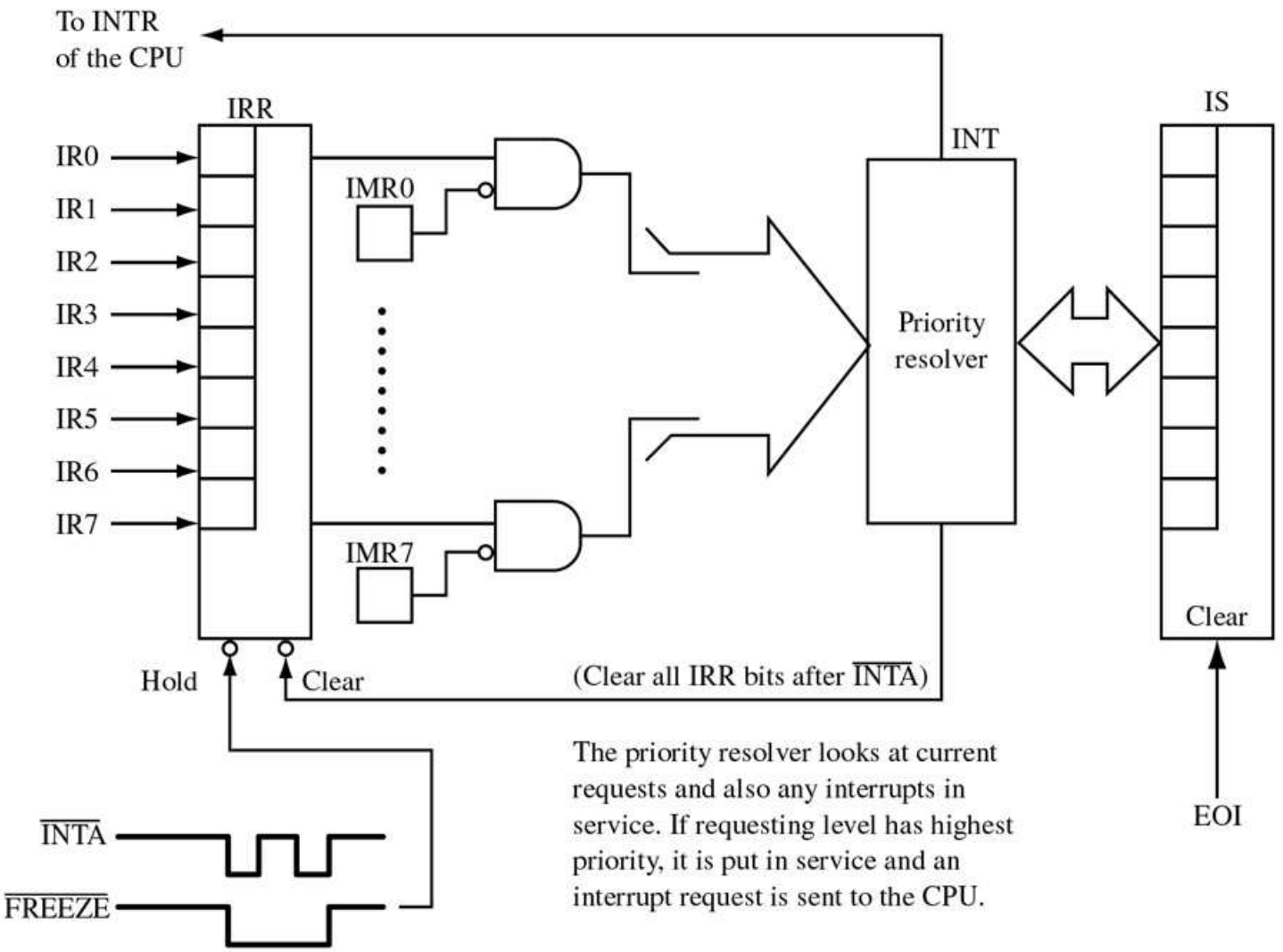
5. This **completes** the interrupt cycle.

6. The **ISR bit is reset** at the end of the **3rd** INTA pulse.

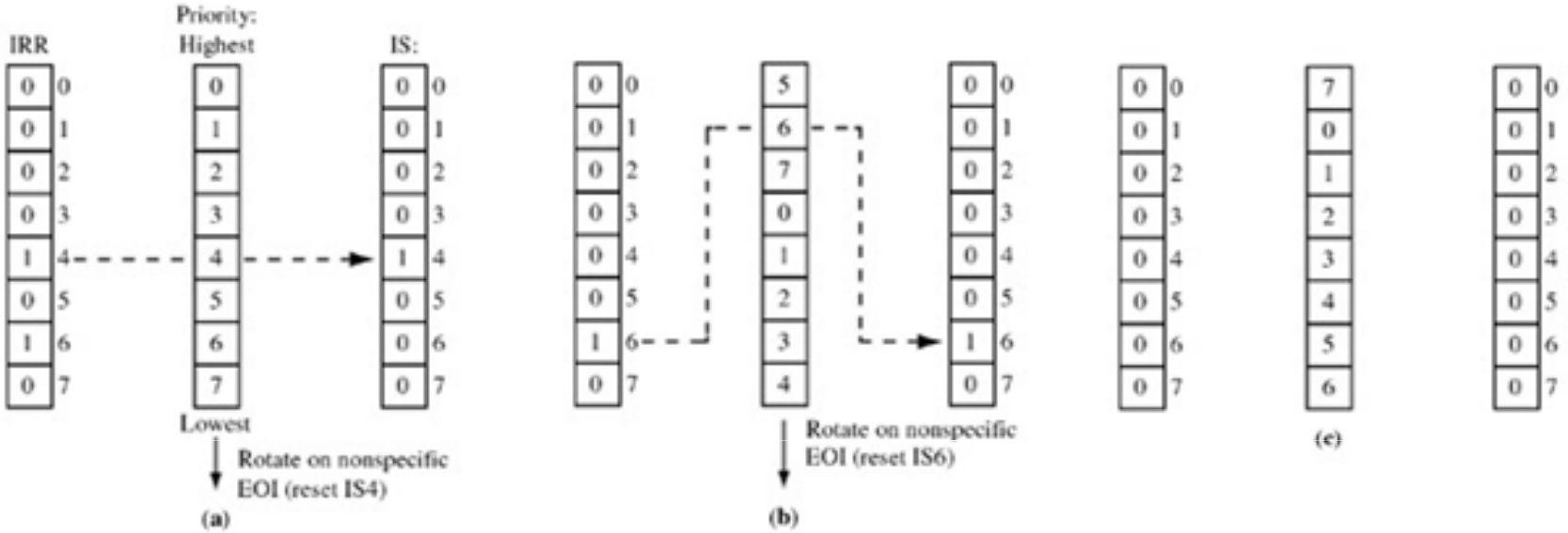
Interrupt vector byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Work flow inside 8259



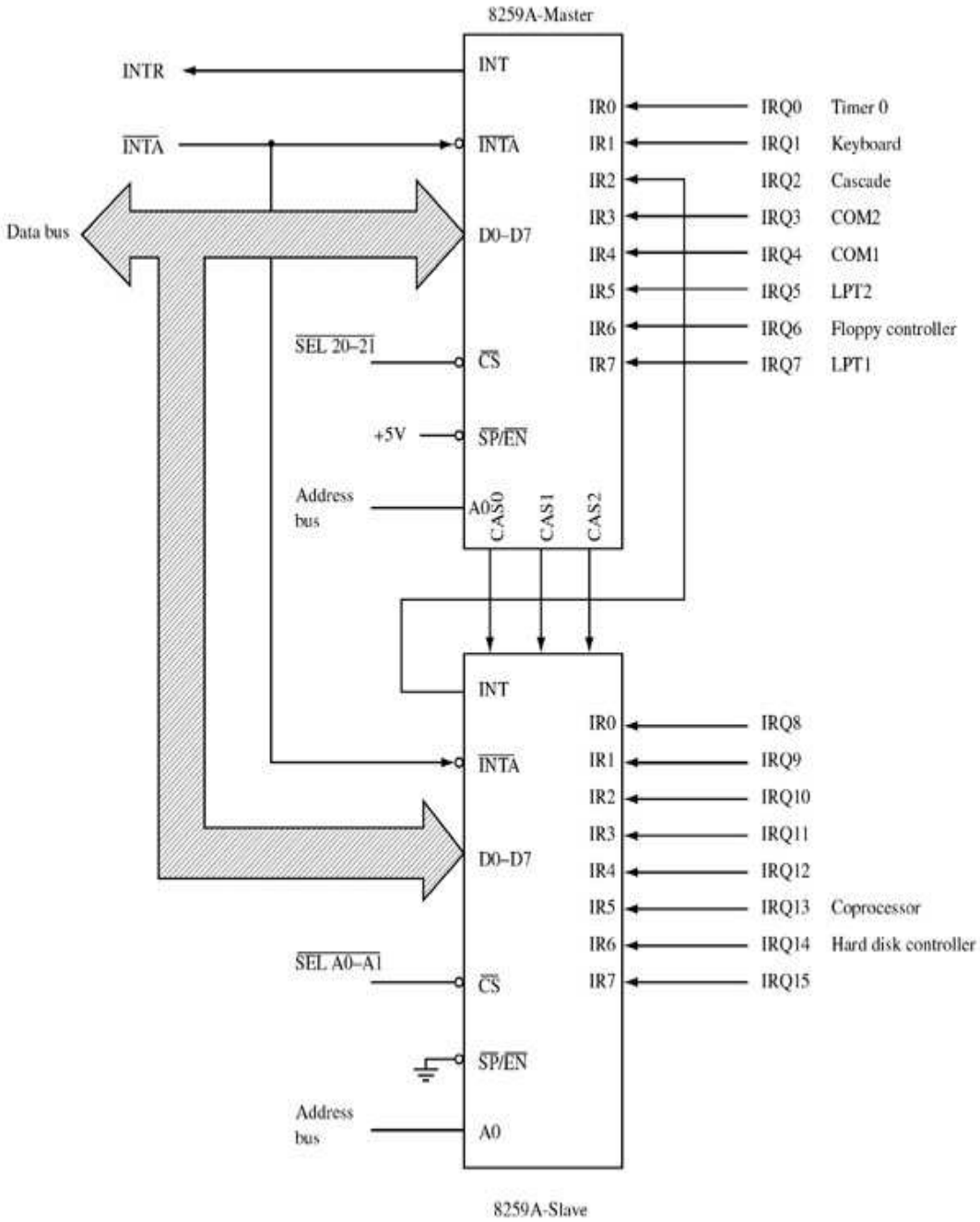
8259 Priority Resolver



(a) Simultaneous interrupt requests arrive on IR4 and IR6. IR4 has highest priority and its IS bit is set as the IR4 service routine is put in service.

(b) The IR4 service routine issues a rotate-on-nonspecific-EOI command, resetting IS4 and assigning it lowest priority. IR6 is now placed in service.

(c) The IR6 service routine issues a rotate-on-nonspecific-EOI command, resetting IS6 and assigning it lowest priority.


8259A-Master
INT
INTR
IR0
IRQ0
Timer 0
INTA
INTA
IR1
IRQ1
Keyboard
IR2
IRQ2
Cascade
Data bus
D0–D7
IR3
IRQ3
COM2
IR4
IRQ4
COM1
IR5
IRQ5
LPT2
IR6
IRQ6
Floppy controller
SEL 20–21
CS
IR7
IRQ7
LPT1
+5V
SP/EN
Address bus
A0
CAS0
CAS1
CAS2
INT
IR0
IRQ8
INTA
IR1
IRQ9
IR2
IRQ10
IR3
IRQ11
D0–D7
IR4
IRQ12
IR5
IRQ13
Coprocessor
IR6
IRQ14
Hard disk controller
SEL A0–A1
CS
IR7
IRQ15
SP/EN
Address bus
A0
8259A-Slave

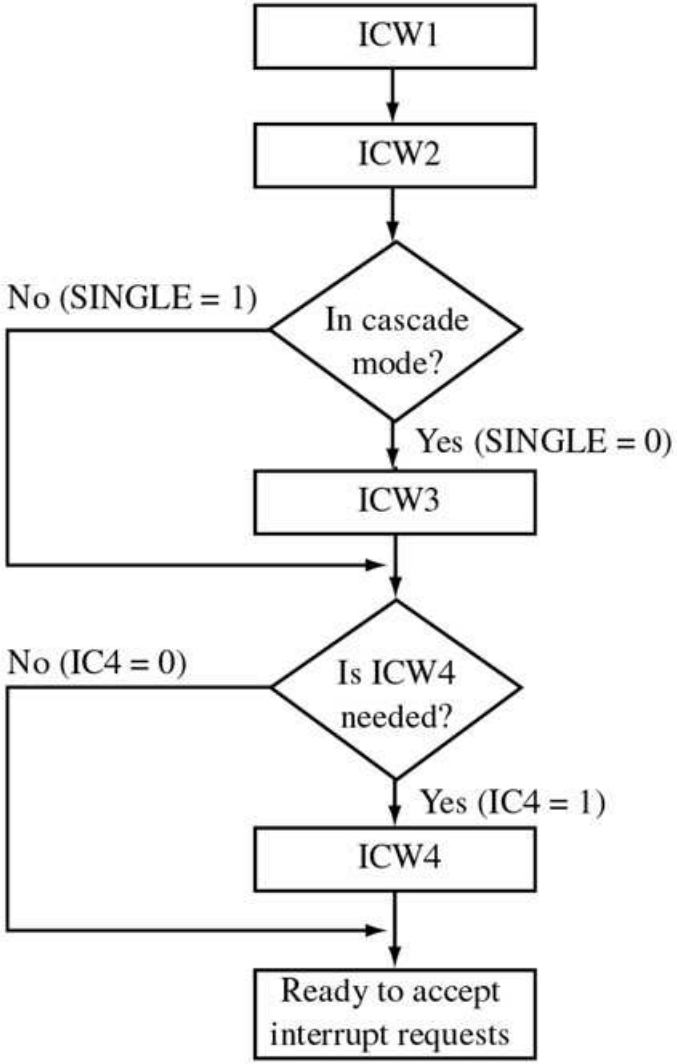
8259 Command Words

- There are 2 Command Words in 8259.

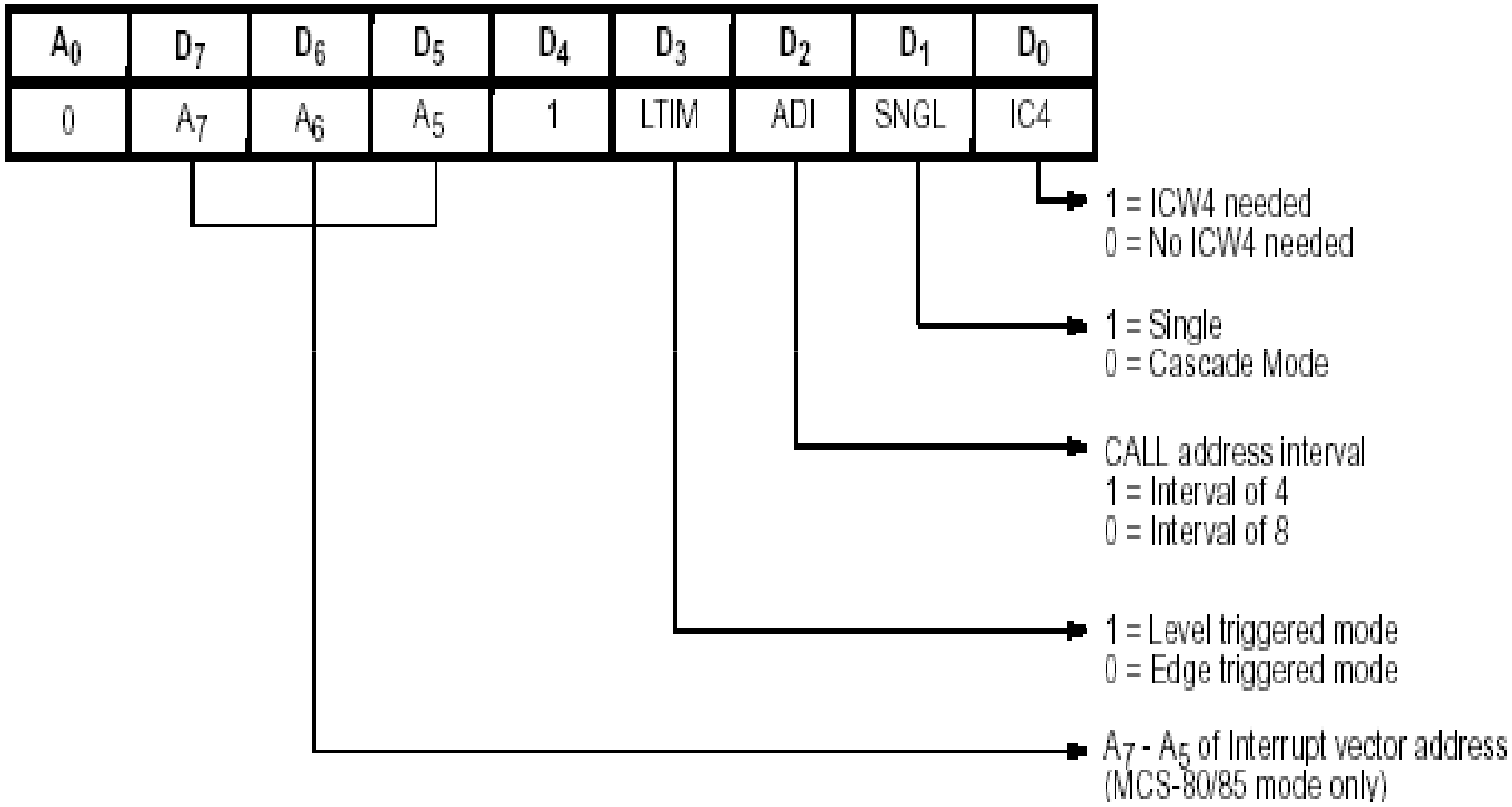
1. **Initialization Command Words (ICWs):** Before normal operation can begin, each 82C59A in the system must be brought to a starting point using these command words.
   - There are **4 ICWs** in 8259.

2. **Operation Command Words (OCWs):** These are the command words which command the 82C59A to operate in various interrupt modes.
   - There are **3 OCWs** in 8259

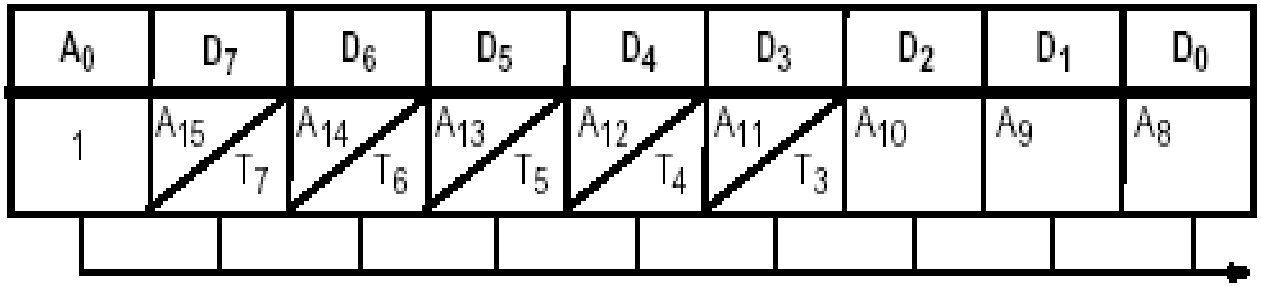
8259A initialization sequence



ICW1 Format


A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 LTIM ADI SNGL IC4
1 = ICW4 needed
0 = No ICW4 needed
1 = Single
0 = Cascade Mode
CALL address interval
1 = Interval of 4
0 = Interval of 8
1 = Level triggered mode
0 = Edge triggered mode
A7 - A5 of Interrupt vector address
(MCS-80/85 mode only)

ICW2 Format



A_{15} - A_8 of interrupt vector address (MCS80/85 mode)

T_7 - T_3 of interrupt vector address (8086/8088 mode)

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

ICW3 Format

- This word is read only when **there is more than one 8259** in the system and cascading is used, in which case **SNGL = 0 in ICW1**.

ICW3 (Master device)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

This register is treated as a mask, with 1's indicating the IRQ channels connected to master/slave 8259As.

0 = IR Input has a slave
1 = IR Input does not have a slave

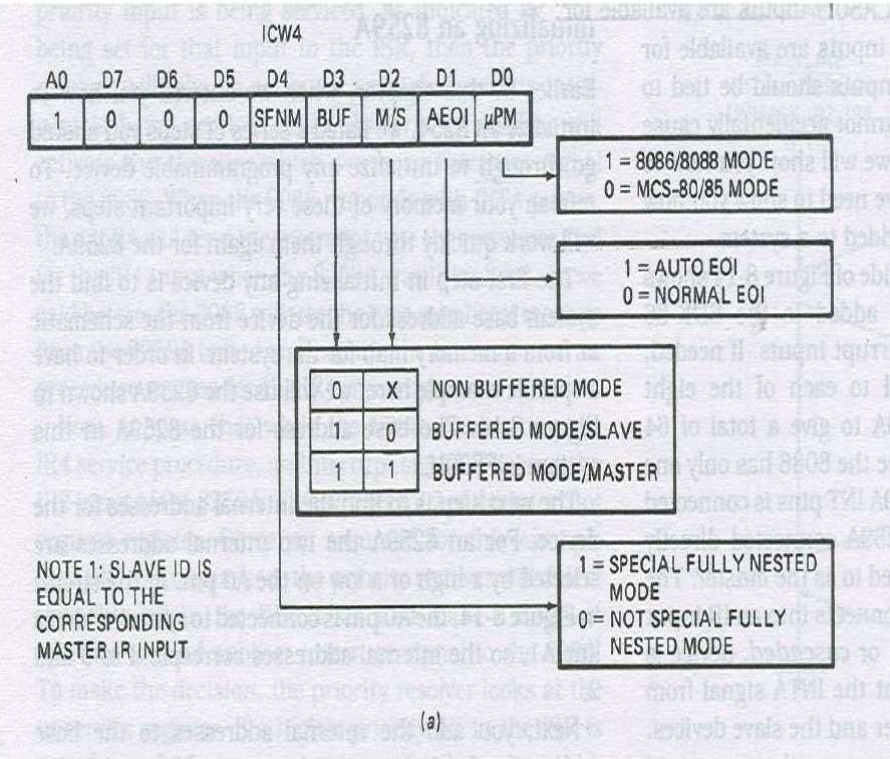
ICW3 (SLAVE DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

SLAVE ID (NOTE)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW4 Format



SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

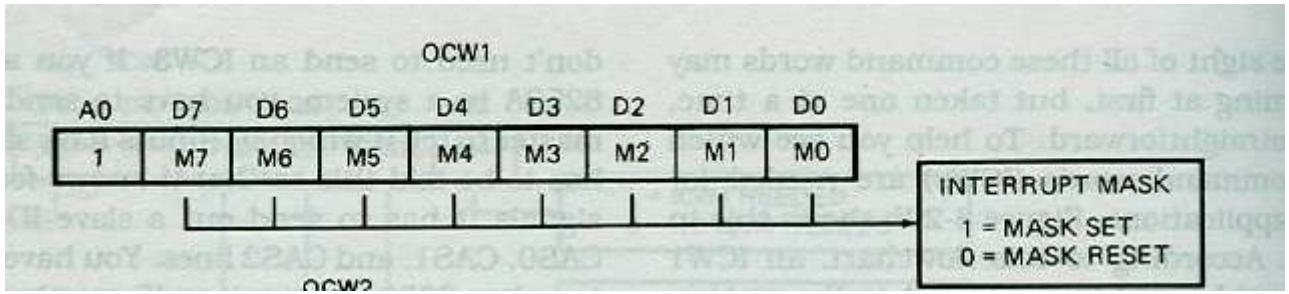
μPM: Microprocessor mode: μPM = 0 sets the 82C59A for 8080/85 system operation, μPM = 1 sets the 82C59A for 80C86/88/286 system operation.

Operation Command Words (OCWs)

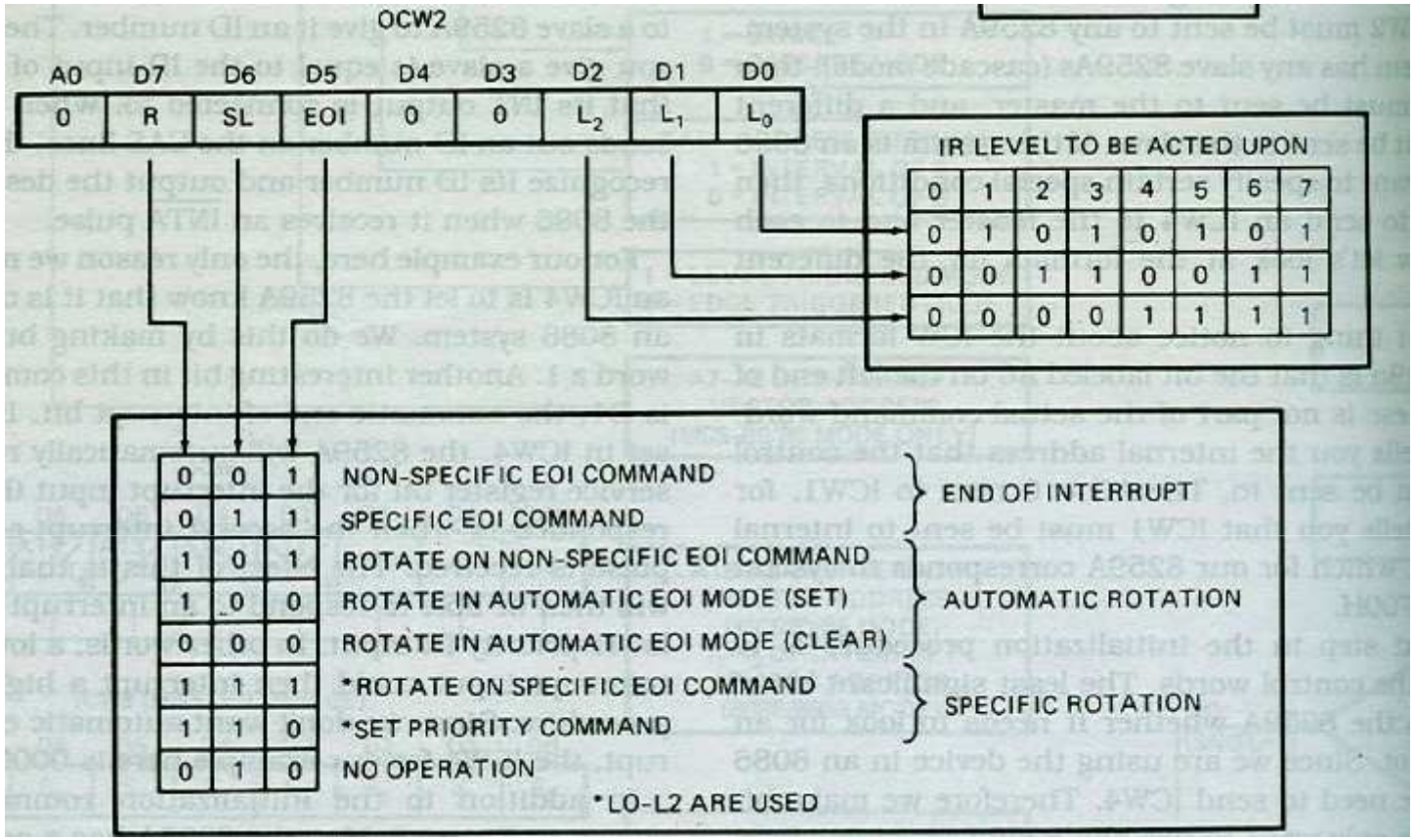
- After the **Initialization Command Words (ICWs)** are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines.

- However, during the 8259A operation, a selection of algorithms can command the **8259A to operate in various modes** through the Operation Command Words (OCWs).

OCW1 Format


OCW1
A0
D7
D6
D5
D4
D3
D2
D1
D0
1
M7
M6
M5
M4
M3
M2
M1
M0
INTERRUPT MASK
1 = MASK SET
0 = MASK RESET

OCW2 Format



R, SL, EOI: These three bits control the Rotate and End of Interrupt modes and combinations of the two.

L2, L1, L0: These bits determine the interrupt level acted upon when the SL bit is active.

OCW3 Format

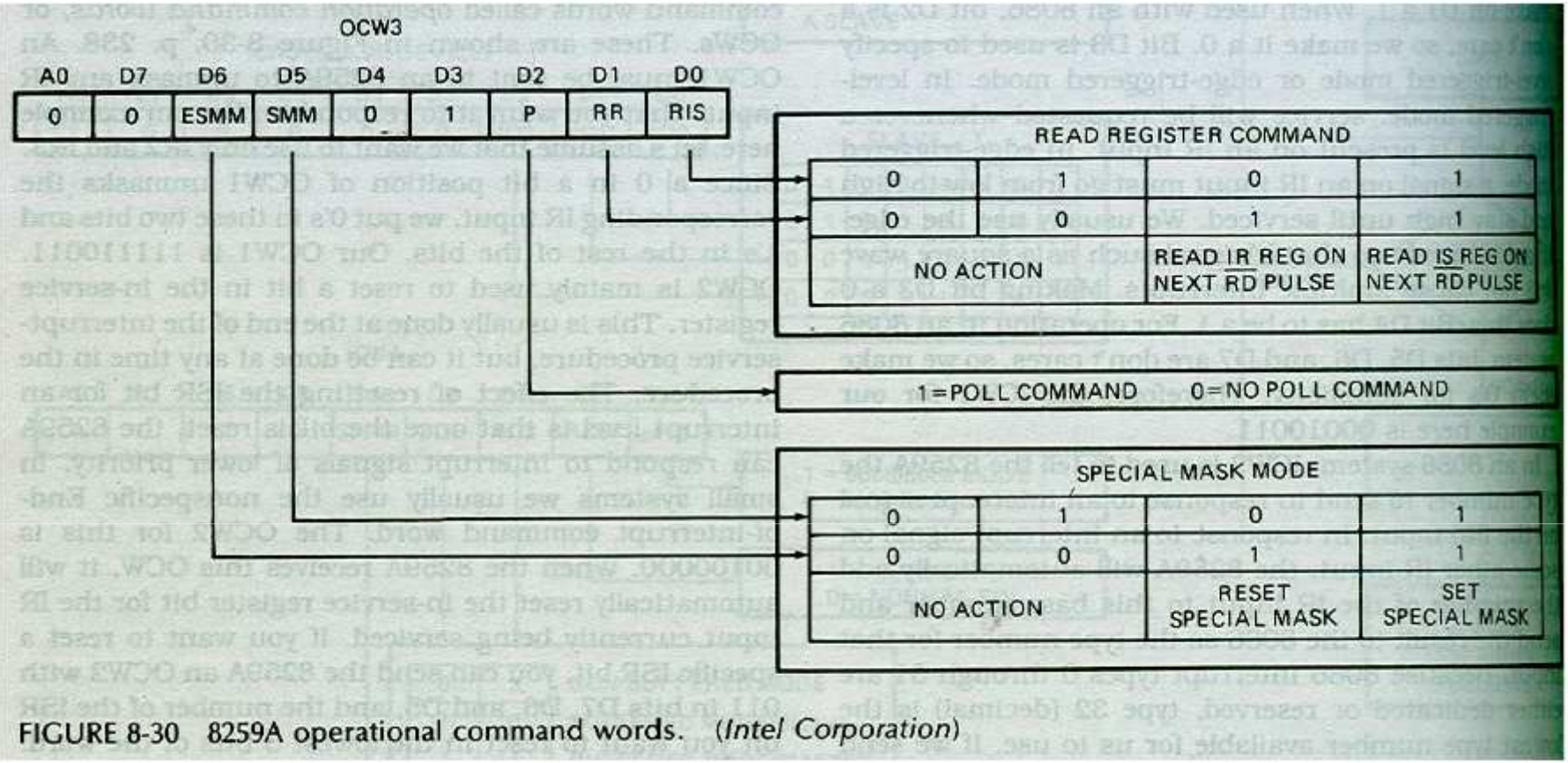


FIGURE 8-30 8259A operational command words. (*Intel Corporation*)

ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a "don't care".

SMM - Special Mask Mode. If ESMM = 1 and SMM = 1, the 82C59A will enter Special Mask Mode. If ESMM = 1 and SMM = 0, the 82C59A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

8259 Working Modes

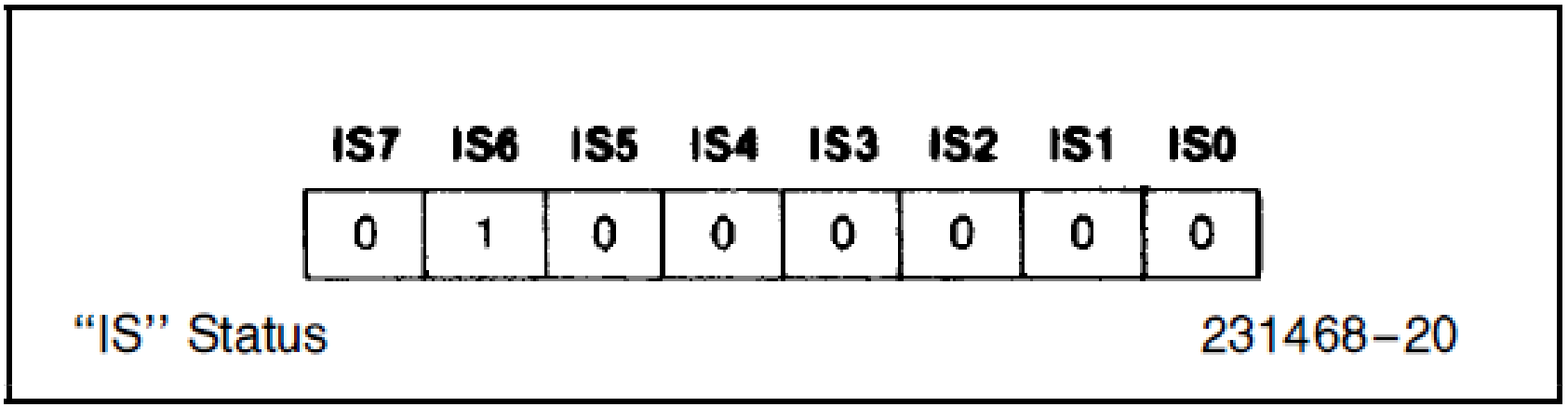
- There are 4 different modes for 8259.

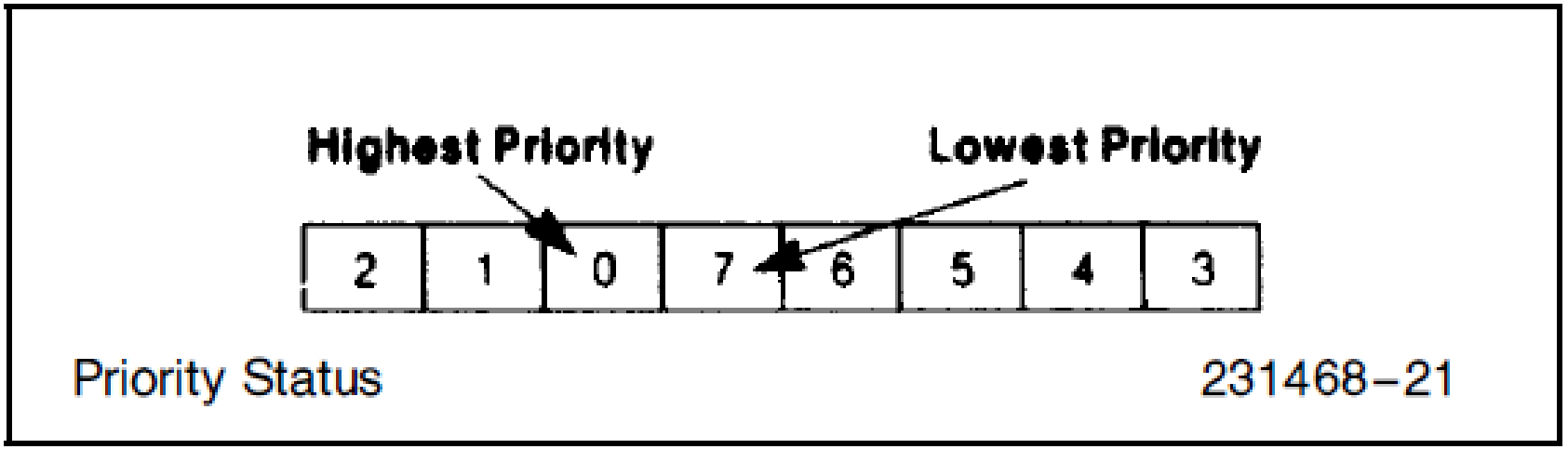
1. **Fully nested mode.**
2. **Rotating priority mode.**
3. **Special mask mode.**
4. **Polled mode.**

Fully nested mode

- This mode is entered after initialization unless another mode is programmed.
- The interrupt requests are ordered in priority from 0 through 7 (0 highest).
- When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus.
- Additionally, a bit of the Interrupt Service register (ISO-7) is set.
- This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine
- If AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA.

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)





Special mask mode

- Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control.
- For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.
- That is where the Special Mask Mode comes in.
- In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.
- Thus, any interrupts may be selectively enabled by loading the mask register.

Polled mode

- In Polled mode the INT output functions as it normally does.
- The microprocessor should ignore this output.
- This can be accomplished either by not connecting the INT output or by masking interrupts within the microprocessor, thereby disabling its interrupt input.
- Service to devices is achieved by software using a Poll command.
- The Poll command is issued by setting P = 1 in OCW3.