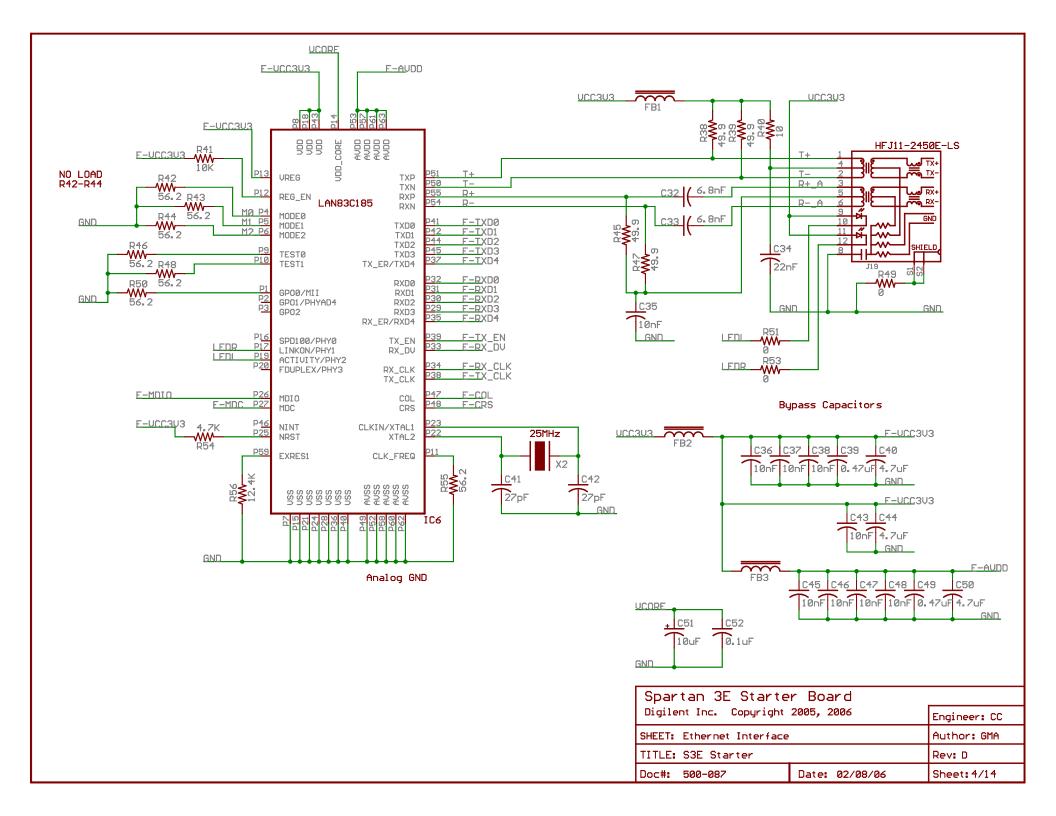
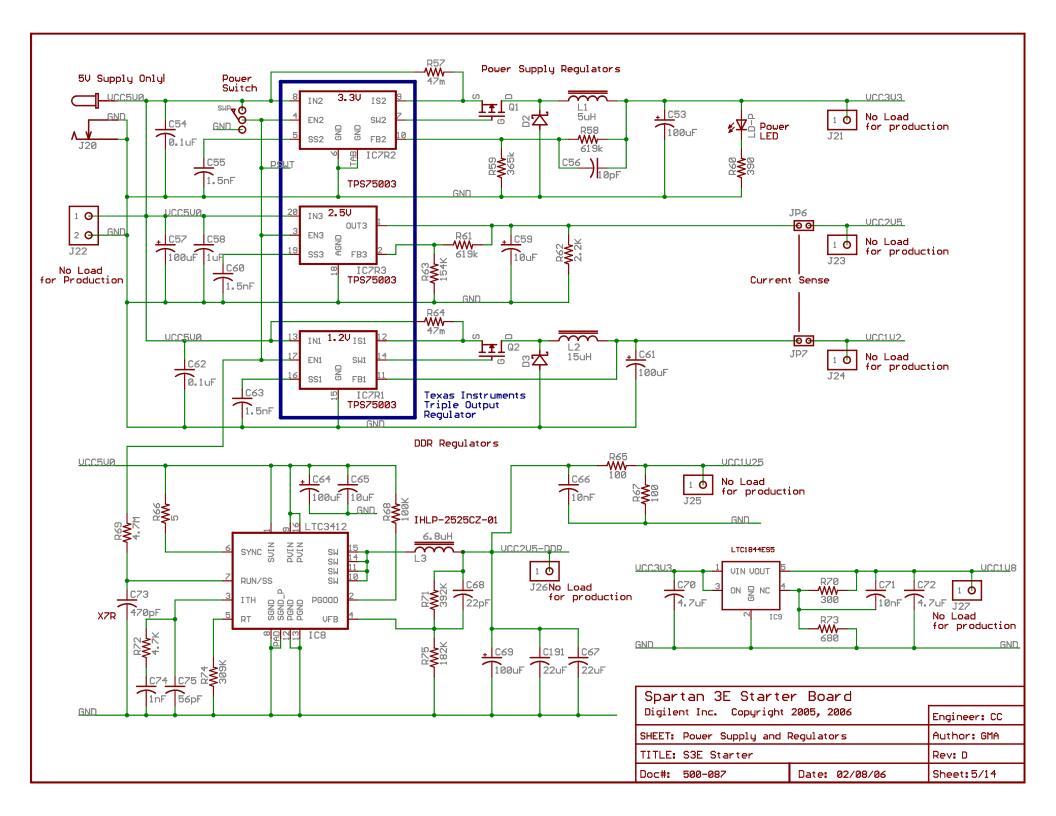
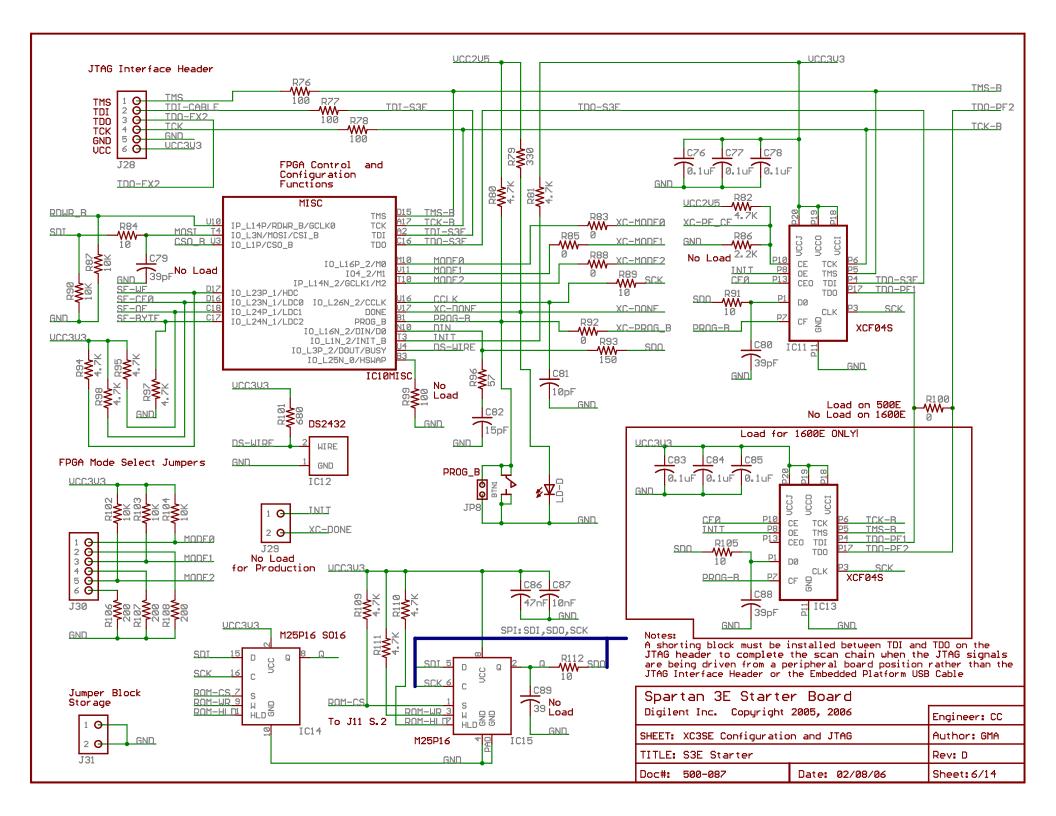


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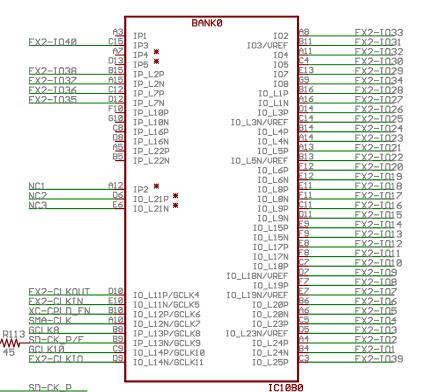
(This page outlines the Xilinx ® proprietary USB 2.0 layout/interface.)





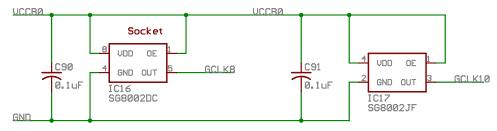






VCC for Bank 1 = 3.3V

	VCC TOT Bank 1 -	0100		
	BANK1	¥ 10 1 00N	E16	
SF-STS B18	IP1	* IO_L22N * IO2	E17	XC-CPLD_EN
AMP-DO E18	IB3	* 102	P16	
ROT-B G18		101	P15	E-TX EN
EAST H13	IP4	100	U18	SF-A16
SOUTH K17	IP5	IO_L1P/A16	T17	SF-A15
WEST D18	IP6	IO_L1N/A15	R18	SF-A14
ROT-A K18	IP7/UREF	IO_L2P/A14	T18	SF-A13
SWØ L13	IP8	IO_L2N/A13	R15	SF-D8
SW1 L14	IP9	IO_L3P	R16	SF-D9
SU2 H18		IO_L3N/VREF	M1 4	TXD
SU3 N17	IP11/VREF	IO_L5P	M13	TXD-A
XC-TRIG R17		IO_L5N/VREF	P17	SF-D10
AL-IRIU NII	IP14	IO_L6P	P18	XC-CMD0
		IO_L6N	M15	SF-D11
		IO_L7P	M16	SF-D12
		IO_L7N	N18	XC-CMD1
NC4 N15	TO 14D *	IO_L8P	M18	LCD F
NC5 N14	IU_LTP	IO_L8N	L16	SF-A12
NC6 E15	IU_LTN	IO_L9P/A12	L15	SF-A11
NLD LIS	IO_L22P *	IO_L9N/A11	L18	LCD RS
		IO_L10P	L17	I CD RW
	I	O_L10N/VREF	J12	SF-A2
		IO_L15P/A2	J13	SF-HZ SF-A1
		IO_L15N/A1	H16	XC-GCK0
		IO_L16P	H17	SF-AA
		IO_L16N/A0	H1 4	UGA-RED
OF A10 K13		IO_L17P	H15	
SF-A10 K13 SF-A9 K12	IO_L11P/A10/RHCLK0	IO_L17N	G15	UGA-GRN
	IO_L11N/A9/RHCLK1	IO_L18P	G16	UGA-BLUE
	IO_L12P/A8/RHCLK2	IO_L18N	F18	XC-DØ
SF-A7 K14	IO_L12N/A7/RHCLK3/TRDY:	I IO_L19P	F18	<u>XC-D1</u>
SF-A6 J17	IO_L13P/A6/RHCLK4/IRDY1	. IO_L19N		XC-D2
SF-A5 J16	IO_L13N/A5/RHCLK5	IO_L20P	G14	PS2C
SF-A4 J15	IO_L14P/A4/RHCLK6	IO_L20N	G13	PS2D
SF-A3 J14	IO_L14N/A3/RHCLK7	IO_L21P	F15	UGA-HS
	_	IO_L21N	F1 <u>4</u>	UGA-US
		T01001	_	
		IC10B1		



AD - A/D Converter (11) AMP - Gain Amplifier (11) DAC - D/A converter (11) E- Ethernet (4)

FX2 - Hirose FX2 Connector (1) ROM - M25P16 (6)

SD- SD RAM (12) SF - StrataFlash (12)

ST - Soft Touch Connector (1)

U - USB (3) XC - XC9572 (10)

*	Notes	are	for	pins	that	very	between	500/1200/1600	dies

Spartan 3E Starter Board			
Digilent Inc. Copyright 2005, 2006		Engineer: CC	
SHEET: XC3SE Banks 0 and 1, Clock ICs		Author: GMA	
TITLE: S3E Starter		Rev: D	
Doc#: 500-087	Date: 02/08/06	Sheet:7/14	

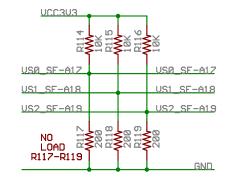
Vcc for Bank 2 = 3.3V

VCC vor Bank 3 = 2.5V DDR

	RANK2		1
E-RX_DU U2 CFNTFR V16 F-COL U6 F-CRS U13 NORTH U4 F-RX_CLK U3 F-TX_CLK T7 RXD R7 RXD-A U8 F-RXDD U8 F-RXDD U8 F-RXDD U11 F-RXD2 U11 F-RXD3 U14 F-RXD4 U14	BANK2 IP1 IP2 IP3 * IP4 * IP4 * IP_L2P IP_L2N IP_L2N IP_L8P IP_L8N IP_L11P IP_L11N/UREF IP_L17P IP_L17N IP_L23P IP_L23N	I01/VREF I02/D5 I03 I05 I06/VREF I0_L4P I0_L5P I0_L5N I0_L7P I0_L7P I0_L7N I0_L9P I0_L9N I0_L10P	U5 F-MDIO R9 SF-D5 P9 F-MDC R11 F-TXD0 T15 F-TXD1 R5 F-TXD2 T5 F-TXD3 R6 F-TXD4 P6 SF-D13 N7 AMP-CS P7 AMP-SHDN P8 DAC-CLR N8 DAC-CS R8 SF-D14 T8 SF-D15
NCZ VZ NC8 V5 NC9 V6 NC10 N12 NC11 P12	IO4 * IO_L6P * IO_L6N/VPEF * IO_L21P * IO_L21N *	IO_L18P IO_L18N IO_L19P IO_L19N/VREF IO_L20P IO_L20N	P11 AD—CONV N11 SF/XC—A23 V12 SF/XC—A22 V13 SF/XC—A21 T12 SF/XC—A20 R12 SFI
SF-DZ N9 SF-D6 M9 SF-D4 U9 SF-D3 U9 SF-D2 R10 SF-D1 P10	IO_L12P/D7/GCLK12 IO_L12N/D6/GCLK13 IO_L13P/D4/GCLK14 IO_L13N/D3/GCLK15 IO_L15P/D2/GCLK2 IO_L15N/D1/GCLK3	IO_L22P/A23 IO_L22N/A22 IO_L24P/A21 IO_L24N/A20 IO_L25P/US2/A19 IO_L25N/US1/A18 IO_L26P/US0/A17	P13 R13 T14 R14 U15 US2_SF-A19 U15 US1_SF-A18 T16 US0_SF-A17
		IC10B2	

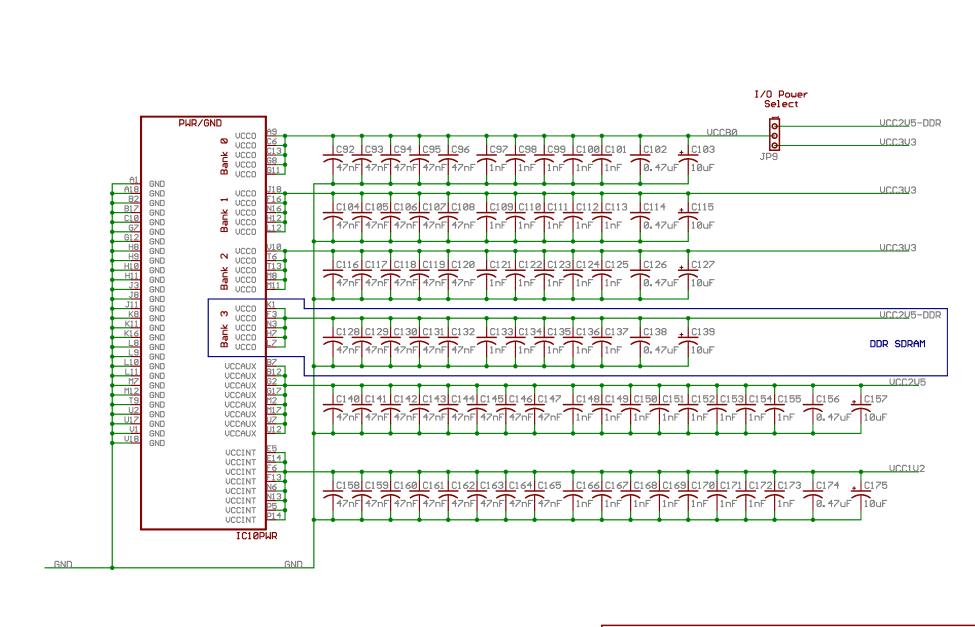
	BANK3	* 101	D4	NC15
D3	IDI	* IO2	F4 .	SD-A4
F5	100	* IO L4P	E4	
<u>UCC1U25</u> J6	ID4/UDEE	* I03/VREF	R4	<u>UCC1U</u> 25
6 <u>1</u> J <i>7</i> K <u>2</u> K <u>7</u> M <u>1</u> N <u>1</u>	IP5	IO_L1P	C1	<u>SD-</u> RAS
<u>J7</u>	IP6	IO LIN	C2	SD-CAS
<u>K2</u>	IP7	IO_L2P	D1	SD-WE
<u>K7</u>	IP8	IO_L2N/VREF	D2	<u>UCC1U</u> 25
<u>M1</u>	IP9	IO_L3P	E2	SD-DQ8
<u>N1</u>	IP10	IO_L3N	E1	SD-DQ9
N <u>2</u>	IP11	IO_L5P	F1 F2	<u>SD-</u> DQ10
<u>R1</u> U1	IP12	IO_L5N	63	SD-DQ11
<u>01</u>	IP13	IO_L6P	G3 G4	SD-UDQS
		IO_L6N/VREF	G6	<u>UCC1U</u> 25 SD-DQ12
		IO_L7P	G5	SD-DQ13
		IO_L7N	H6	SD-DQ14
		IO_L8P	H5	SD-DQ15
		IO_L8N	H4	SD=A5
NC12 E3	TO 14N *	IO_L9P	H3	SD-A6
NC13 P3	IU_LTN	IO_L9N	H2	SD-A8
NC14 P4	IU_LZZP	IO_L10P	H1	SD-AZ
Net 1	IO_L22N *	IO_L10N	L1	SD-DQ1
		IO_L15P	L2	SD-DQ0
		IO_L15N	L3	SD-DQ2
		IO_L16P	L4	SD-DQ3
		IO_L16N	L6	SD-L DQS
		IO_L17P IO_L17N/VREF	L5	UCC1U25
		IO_L18P	M4	SD-DQ5
		IO_L18N	M3	SD-DQ4
		IO_L19P	M5	SD-DQ6
SD-CK_P J5		IO_L19N	M6	SD-DQ7
SD-CK_N J4	IO_L11N/LHCLK1	IO_L20P	N4	<u>SD-</u> A9
SD-UDM J1	IO_L12P/LHCLK2	IO_L20N	N5	<u>SD-</u> A11
SD-LDM J2	TO 1 12N /1 HCL V2 /TDDV2	IO_L21P	P2	<u>SD-</u> A12
SD-CKE K3	IN 112071 HOLK4/TDDV2	IO_L21N	P1	SD-A3
SD-CS K4	IO L13N/LHCLK5	IO_L23P	R3	SD-A1
SD-BA1 K6	IO_L14P/LHCLK6	IO_L23N	R2	SD-A2
SD-BAO K5	IO_L14N/LHCLK7	I0_L24P	T2	<u>SD-</u> A10/AP
		IO_L24N	T1	<u>SD-</u> A0
		IC10B3	_	

AD - A/D Converter (11) AMP - Gain Amplifier (11) DAC - D/A converter (11) E- Ethernet (4) FX2 - Hirose FX2 Connector (1) ROM - M25P16 (6) SD- SD RAM (12) SF - StrataFlash (12) ST - Soft Touch Connector (1) U - USB (3) XC - XC9572 (10)

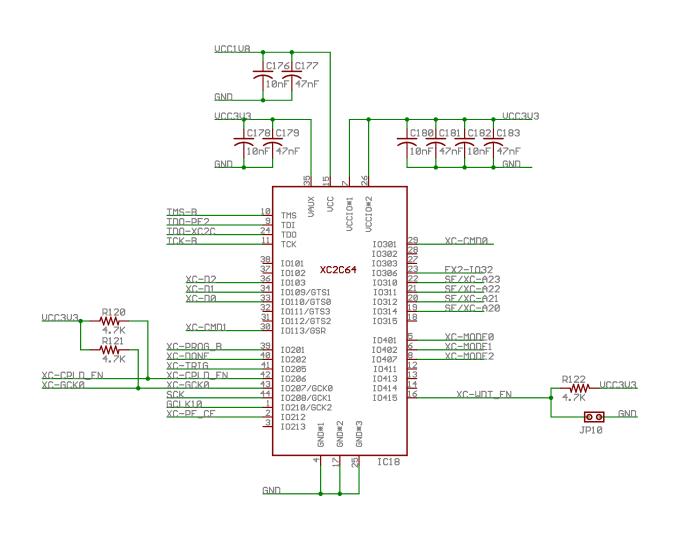


* Notes are for pins that very between 500/1200/1600 dies

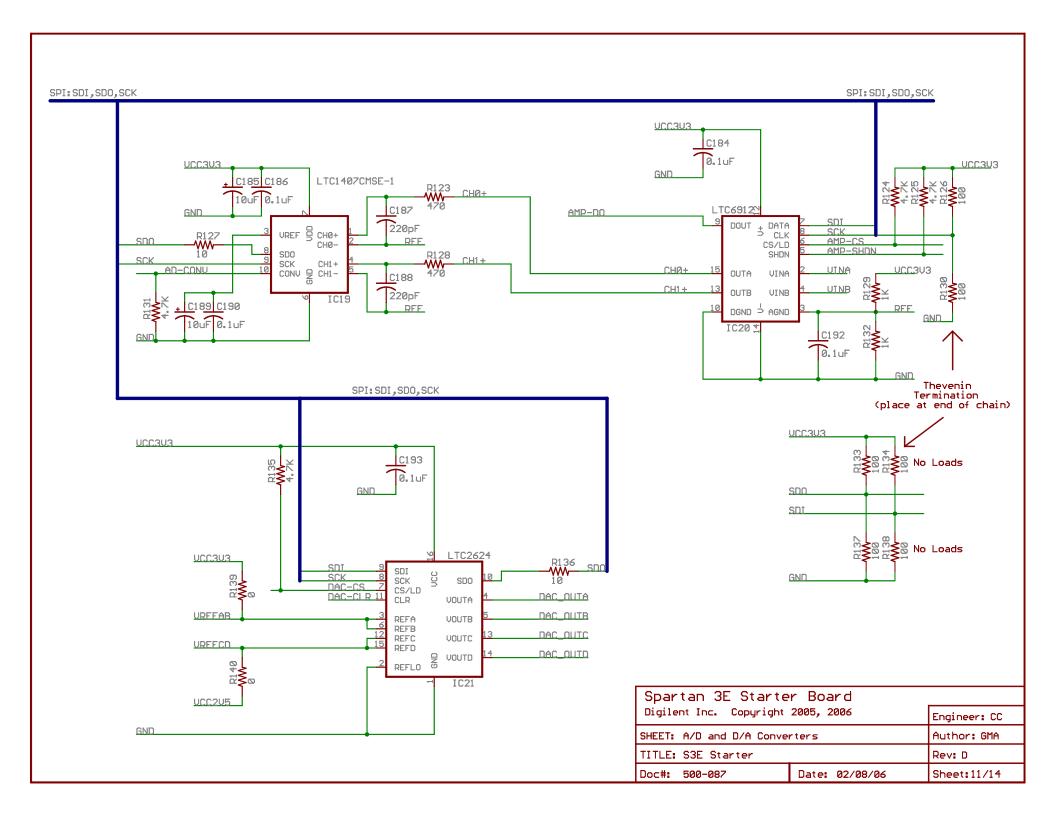
Spartan 3E Starter Board			
Digilent Inc. Copyright	2005, 2006	Engineer: CC	
SHEET: XC3SE Banks 2 and 3		Author: GMA	
TITLE: S3E Starter		Rev: D	
Doc#: 500-087	Date: 02/08/06	Sheet: 8/14	

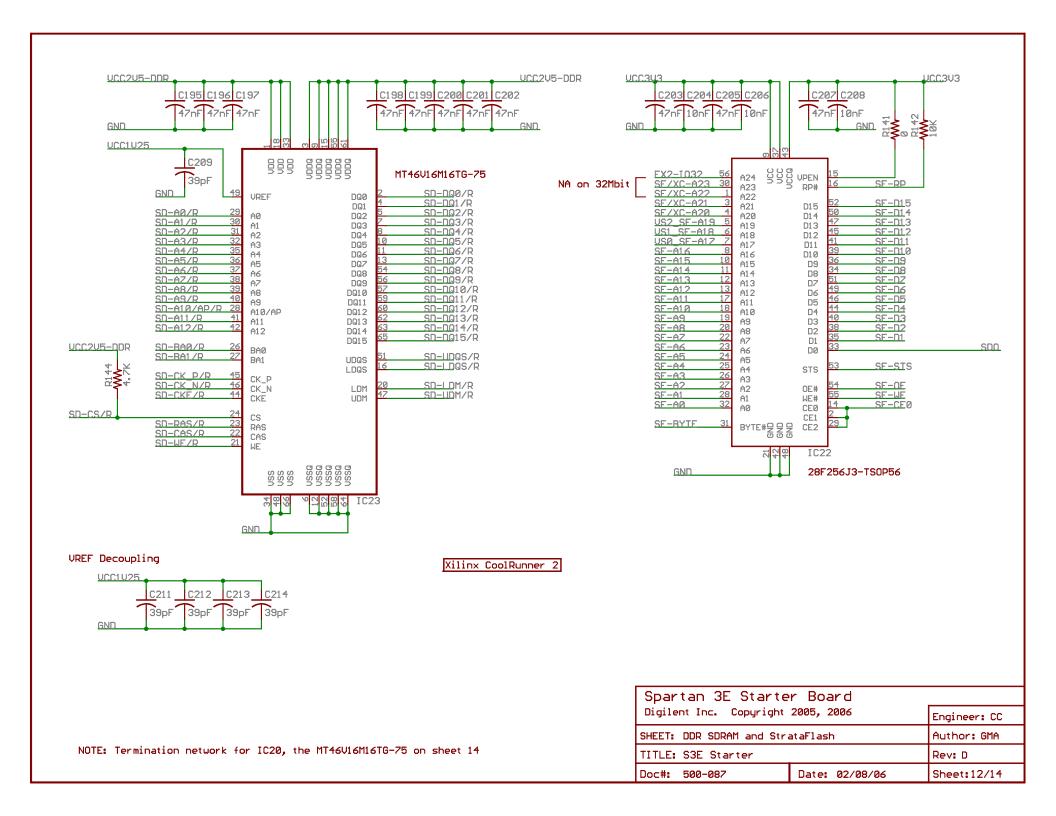


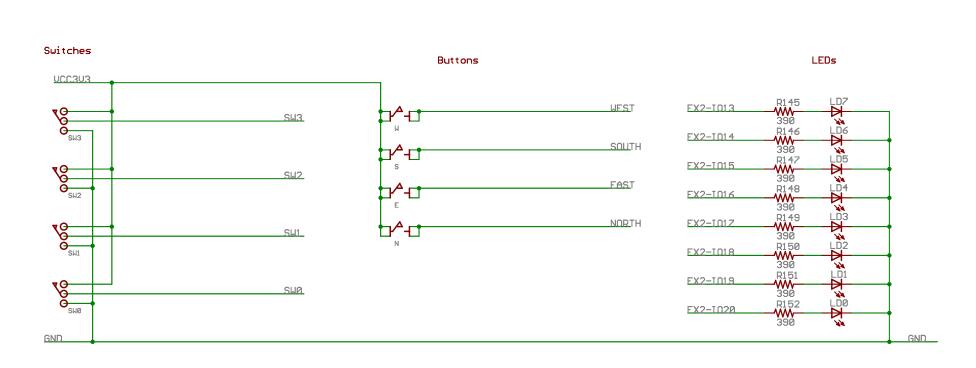
Spartan 3E Starter Board		
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SHEET: XC3SE Power Decoupling		Author: GMA
TITLE: S3E Starter		Rev: D
Doc#: 500-087	Date: 02/08/06	Sheet: 9/14

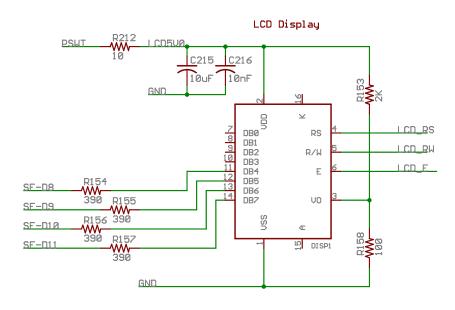


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SHEET: XC2C64 CPLD		Author: GMA	
TITLE: S3E Starter		Rev: D	
Doc#: 500-087	Date: 02/08/06	Sheet:10/14	

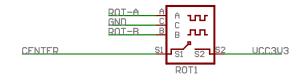








Pushbutton/Rotary Encoder



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SHEET: LCD and General IOs		Author: GMA	
TITLE: S3E Starter		Rev: D	
Doc#: 500-087	Date: 02/08/06	Sheet:13/14	



FX2 Differential Termination Not Loaded

	NOT LOGGEG	
EX2-I017	R202	FX2-I018
FX2-I019	100 R203 	FX2-I020
FX2-I021	100 R204	FX2-I022
FX2-I023	100 R205	FX2-I024
FX2-I025	100 R206	FX2-I026
FX2-I027	100 R207	FX2-I028
EX2-I035	100 R208	FX2-1036
EX2-I037	100 R209	FX2-1038
EX2-CLKIN		FX2-CLKOUT
	100	

Spartan 3E Starter Board			
Digilent Inc. Copyright 2005, 2006		Engineer: CC	
SHEET: DDR Memory Signals		Author: GMA	
TITLE: S3E Starter		Rev: D	
Doc#: 500-087	Date: 02/08/06	Sheet:14/14	