Dual AWR2243 Cascade Board Design

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Background

This board has been designed during a group-project at the University of Southampton, in collaboration with Roke.

The design task was to create a radar system to lower the cost of imaging radar systems. During this project I have designed a PCB to interface a Texas Instruments radar development board to a Raspberry Pi Compute Module 4, as well as breakout other useful functions. This allows data capture and onboard computation at a low cost – TI provides an FPGA based solution for data collection only – costing $600.

The aim of the board in this document is to replace the TI development board (AWR2243Boost), which costs $349. The dev board centres around a single AWR2243 IC, and contains many unused (by us) features.

Since the AWR2243 IC by itself costs $30 in single units, a saving could be made, prompting the development of a new board. In fact, the new board combines two of these ICs in a cascade configuration, allowing more complex imaging techniques.

This document will detail my design choices and workflow; I would be very grateful for any feedback you have on any of my choices. The PCB has been developed in KiCad; I am unsure if this is software you use, so I have uploaded both the project files and the Gerbers.

The board is 6 layers, with each layer labelled in the top right with a number from 1-6.

Board Layout

The board layout followed the priority of:

- Off Board Connectors and mounting holes (set positions)
- 2 AWR2243 (radar) ICs
- AWR2243's decoupling capacitors
- Power rail filtering
- Buck Converter Circuitry
- Low speed (40MHz) Clock circuitry
- Misc IO, resistor pullup/downs etc.

The ffc connectors have a set position, as they have been designed into the CM4 interface board. Being ffc connectors, their position is not technically impossible to

move, due to the flexible nature of the cables, but I feel their positions aren't interfering with the design much. The ffc's were chosen over hard mounted connectors to allow versatile mounting.

The 10 pin header in the bottom left has a fixed position.

The two AWR2243 (radar) ICs have been placed at the front, in the middle of the board, with antennas above and below them. There is a 20GHz sync signal which runs between the two chips, which prompted the chips being as close together as possible.

I have extended the board at the top and bottom to allow the antennas to move further up and down, and out of the way of neighbouring components.

The radar ICs are in a BGA package, so I placed all required through-hole vias to break out the whole IC before placing the decoupling capacitors, to ensure I wouldn't run into issues with placement later down the line. They were placed mostly on the rear, directly under the relevant pin's via, to ensure the lowest impedance path to the IC.

7.5 Power Supply Specifications

Table 7-1 describes the four rails from an external power supply block of the AWR2243 device.

Table 7-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)(1)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in Table 7-2 are defined to meet a target spur level of –105dBc (RF Pin = –15dBm) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a ~1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

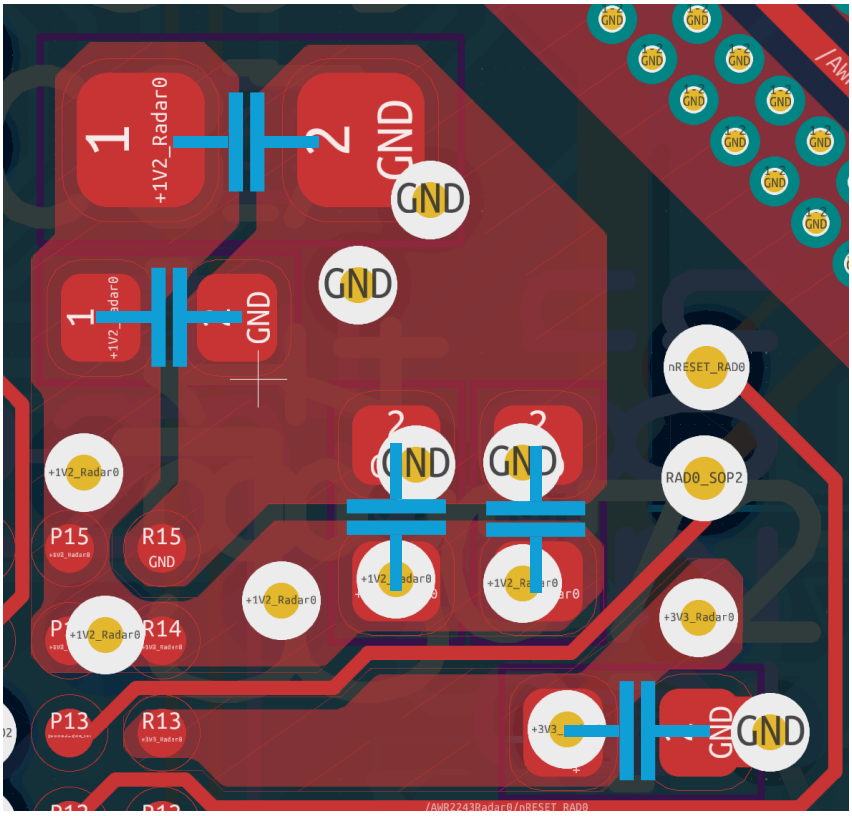
Table 7-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

Power supply specifications from TI AWR2243 Datasheet (page 17)

https://www.ti.com/lit/ds/symlink/awr2243.pdf

Priority was given the 1V0 RF rails, which require the lowest noise, followed by the 1V8, 1V2 and finally 3V3 rail. A few of the power pins were on the outermost layer of balls, so their decoupling was placed on the top layer, so the path didn't have to go through one via to the power plane, then a second via to the power pin.



Example of decoupling capacitors on front side, when the ball (P14/15, R14, R13) is on the outer layer of BGA.

Each power rail is produced by a switching regulator, so has another LC filter closer to the radar chip. These are placed in close proximity, although are placed in a way to not affect any decoupling, or important IO signals. The best positioning mostly comes out to be extending from the corners of the IC, on the bottom.

One key design issue was not the routing of the power plane, but allowing enough area to supply enough of a path to supply the return currents. Especially with these filters, being quite bulky, I found myself blocking many ground plane entrances into the underside of the radar ICs. This does mean that there is perhaps a slightly better placement of these filter components from a power point of view, although there would be so little ground area entering the IC, it would perform worse. Another issue is the placement of ground vias near these filter circuits. Because some of them are placed under the >GHz signals and waveguide, there is not enough room to place the through

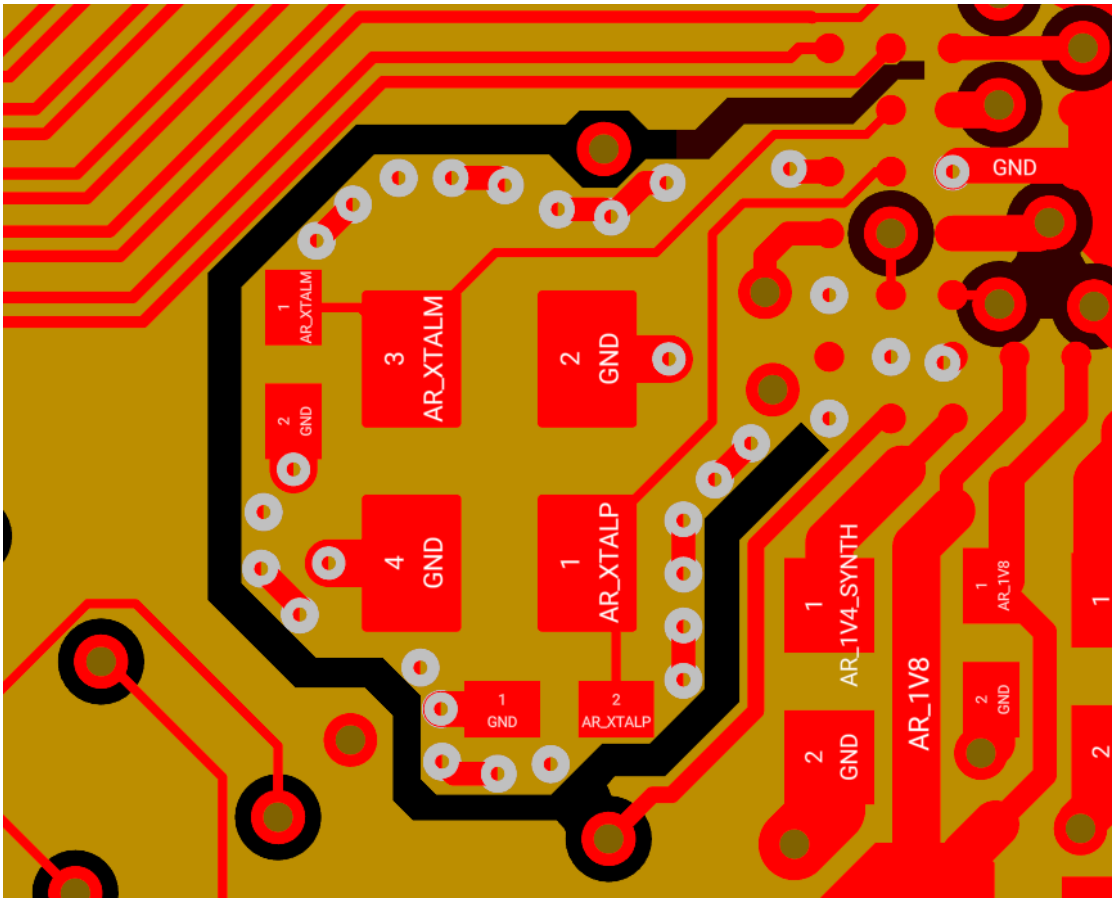
hole vias. I have chosen to place these components in non-optimal positions along the borders

This step especially couples closely to the routing of the various voltage rails. I aimed to keep as much of this power routing to one layer, extending into multiple polygons. This power plane layer is chosen to be layer 4, which was selected for its proximity to the 5th Layer, a ground plane. The proximity creates a capacitive effect, improving decoupling.

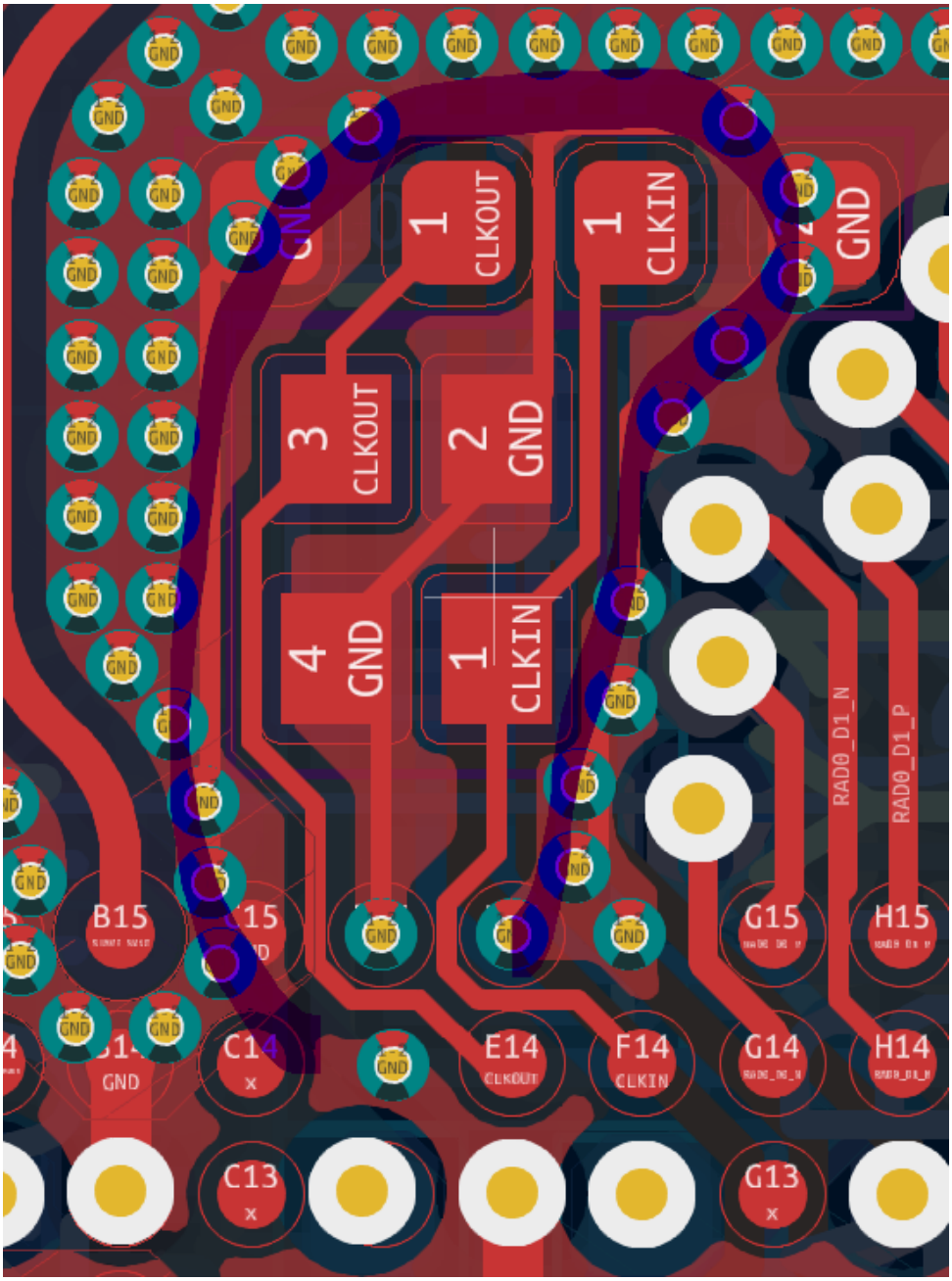
Again, priority was given to the higher power layers, namely 1V0. The maximum width of these 1V0 copper polygons are also replicated on the bottom layer to lower the resistance, and hence improve power supply quality. Via stitching in key areas means these planes are closely coupled. I used a PCB toolkit calculator to calculate the minimum viable trace width and ensured these polygons far surpass that value.

The buck converter is placed off to the left of the board. This ensures there is minimal interference with the antennas, as well as an intentional placement of the voltage rail outputs. This allows every high-power rail to be routable in only the power plane layer (4).

The low frequency clock (40MHz) supplies the master radar IC, which it then distributes to the slave IC. The crystal has been protected by a guard ring, which has been closely via stitched. On the reference design, they split the 2nd Layer ground at this point, which I have not done, as that is quite a crucial ground return path from the 1V2 and 1V8 Lines. Also, the reference design does not have to route the 20GHz sync signal near the clock, as it is only a single radar IC, not cascaded. Let me know your thoughts on this.



The reference design (AWR2243BOOST) contains a split ground plane under the clock.

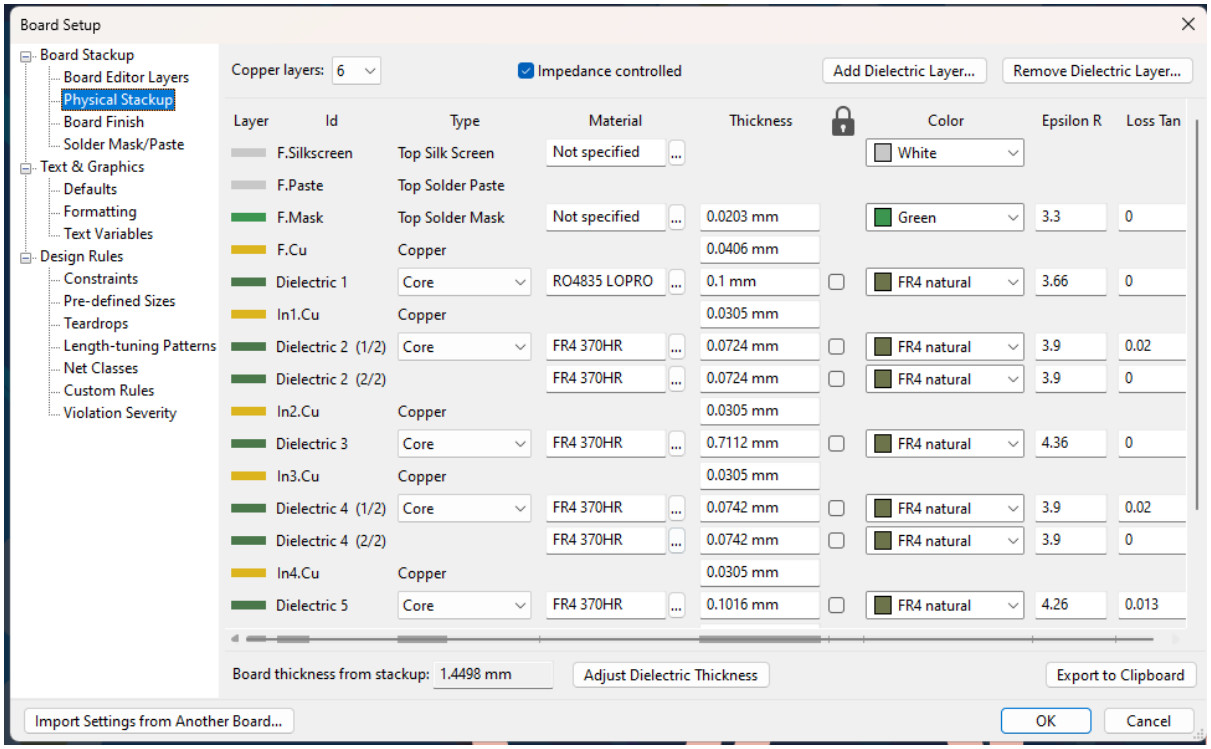


The clock has a guard ring surrounding it.

Last priority was the various pullup/down resistors, LEDs, testpoints etc. Most of the traces were routed first, before placing those components.

PCB Stackup

The stackup used is one of the recommended designs, as used in the AWR2243BOOST board. There is only one layer of HF specific dielectric, the Rogers RO4835 LOPRO. This is between layers 1 and 2. All RF routing is done on layer 1, and stiched closely to the GND plane on layer 2.



Single-ended, and differential impedance for specific traces were calculated and regulated using a microstrip impedance calculator.

Routing Topology

Routing followed a similar priority tiering to that of component placement, with the change of there not being any mandatory routing like there was with placement.

The routing rules were defined from the Texas Instruments AWR2243BOOST board, since that is the stackup I have used. Clearance and trace width minimum trace width are both 0.1mm, ~4mils. The smallest mechanical vias are 0.25 (hole)/0.55mm (diameter), and the microvias used for the waveguides are blind, layer 1->2 0.15/0.35mm. These blind vias allow a tight coupling to layer 2 ground, without disturbance to traces internal to the board and components on the bottom layer.

During non-RF routing I first laid out a basic plan of the traces, before going back over and increasing their width, and in general neatening them. MIPI CSI2 lanes were routed multiple times to ensure the correct spacing, trace width and length/skew matching.

RF Antenna Layout

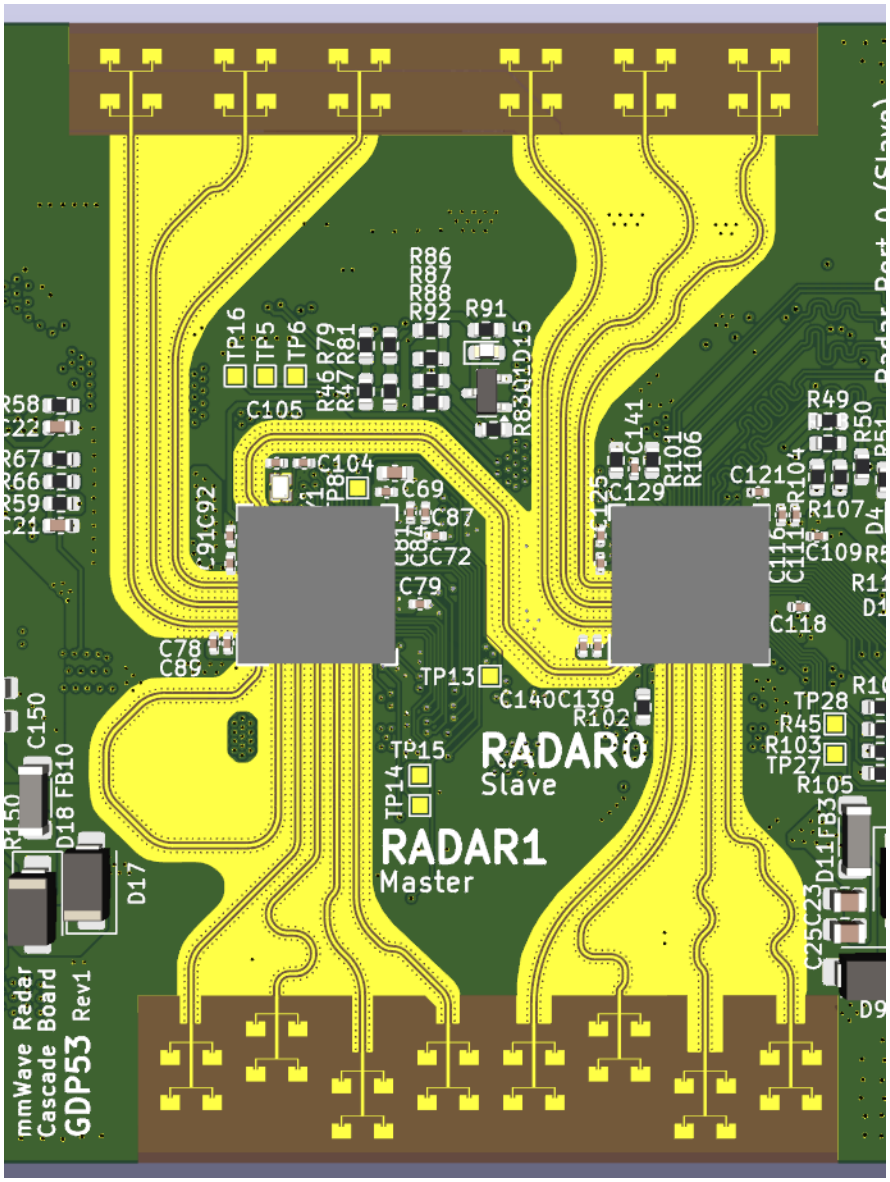
The antenna design was devised by another student, Quinn, and although I did help at times, I cannot claim their design. However, the placement on the board was my doing. I used a spreadsheet to come up with a MIMO array, dependant on the positions of the

antennas on the board. This is somewhat limited by board area, and in hindsight should have been calculated prior to laying out any other components.

I am not from a radar background unfortunately, so the calculation of the MIMO array could be incorrect.

The layout depends on the Tx Antennas being spaced apart by 2xLambda, with a gap of 3xLambda between the two sets of three Tx Antennas.

The Rx Antennas are all spaced 3/2*Lambda apart in the horizontal plane, but repetitively spaced +-1/2*Lambda in the vertical plane. This gives a wide MIMO array.



Tx Antennas at the top of the board, Rx Antennas at the bottom.

A have also attached the excel spreadsheet defining the MIMO array details.

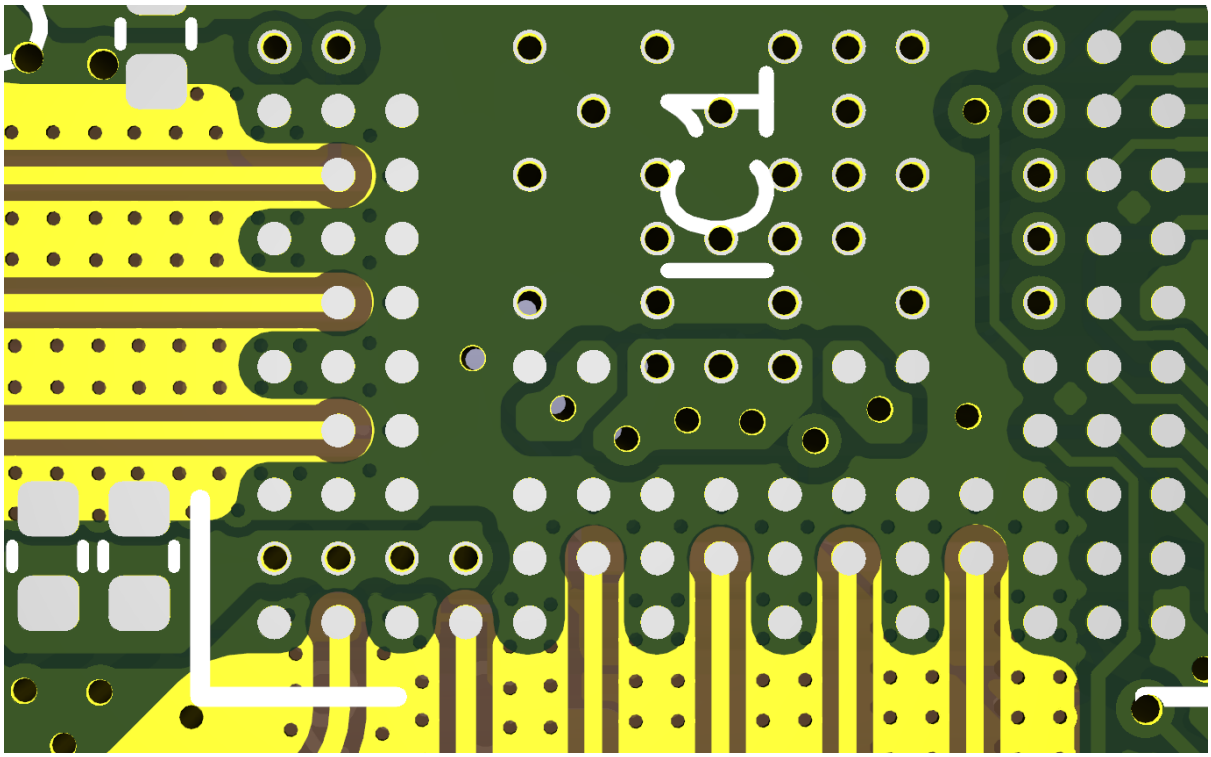
RF Routing

Each RF trace (Rx, Tx, Sync) has other corresponding traces which have been length matched. Every RX has been matched to the other RX's, to within 0.0001mm, as have the TX's, and Sync signals.

Each of these high speed signals have been routed using a curve tool, to minimise the RF attenuation. Unfortuately, I could not find a good tool to length match these curved traces programatically, so I had to tweak each trace by itself until the lengths matched.

A similar issue arose when placing the microvias to create the waveguide. All the tools only work with throughhole vias, and not blind ones. The best solution I could think of was to manually place them; student labour I think is the technical term! The microvias are placed 0.4-0.45mm apart, which translates to 1/8*lambda.

I have placed a soldermask-cutout to ensure that the soldermask does not interfere with the antennas. Similarly, I have stopped the copper ground pour from surrounding the antennas. I have selected a gold plated finish to prevent corrosion occuring on the soldermask-less areas, hindering the RF propogation. I have also ensured the solder mask is removed all the way under the radar ICs, as shown in the picture below.



The lack of soldermask extends under the BGA IC.