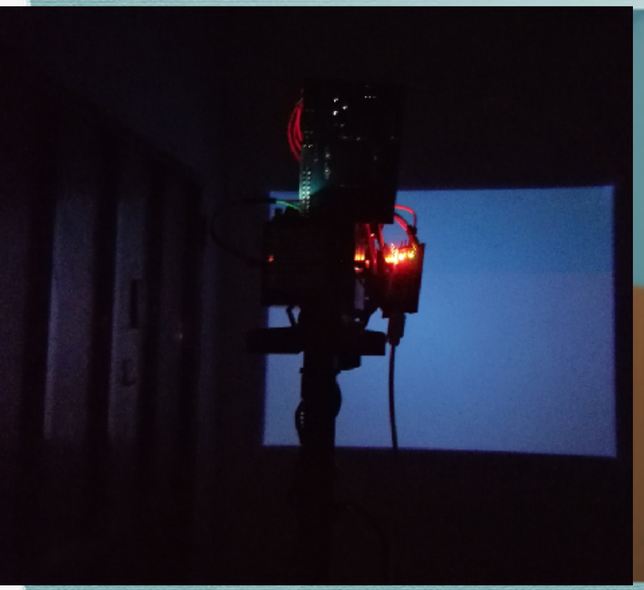
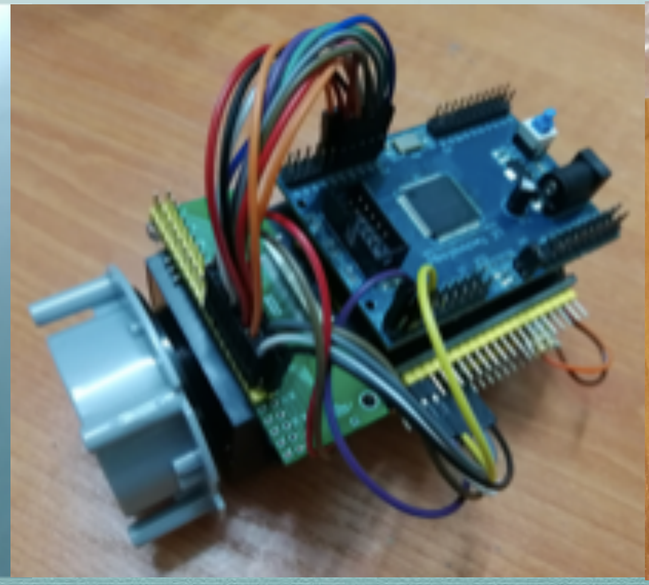
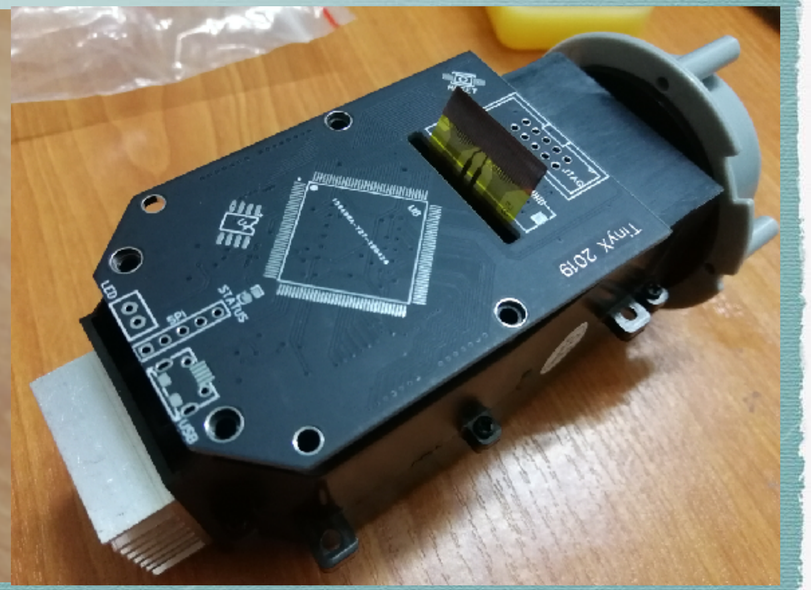
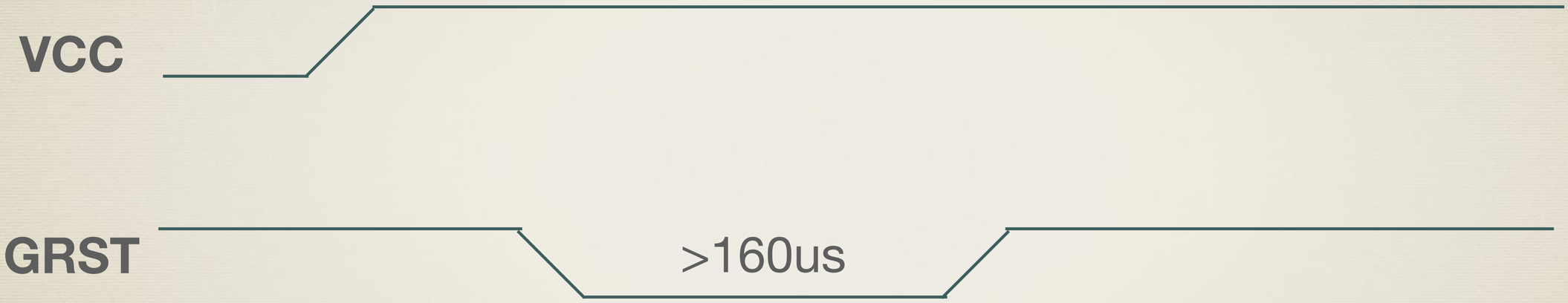
9.98投影时序分析

DIY迷你投影群号:210177425



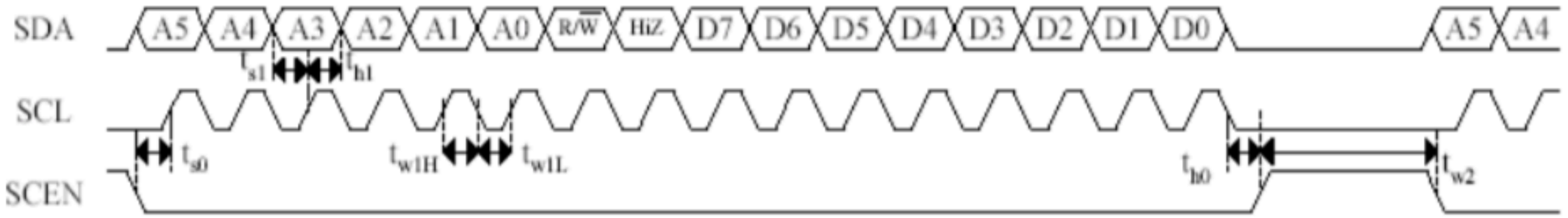



1.复位



2.配置模式（通信协议）

3 wires Serial data transfer format:



Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDA Setup Time	t_{s0}	SCEN to SCL	150			ns
	t_{s1}	SDA to SCL	150			ns
SDA Hold Time	t_{h0}	SCEN to SCL	150			ns
	t_{h1}	SDA to SCL	150			ns
Pulse Width	t_{w1L}	SCL pulse width	160			ns
	t_{w1H}	SCL pulse width	160			ns
	t_{w2}	SCEN pulse width	1.0			us
Clock duty			40	50	60	%

2.配置模式（Through mode）

```
data = spi_read(0x2);//读出R2的值
data &= ~(0x3 << 0);//清零[1:0]位
data |= 0x2; //through mode//设置相应bit位
spi_write(0x2, data);//写入配置
if(spi_read(0x2) == data)//回读判断是否写入成功
{
    printf("through mode ok !\r\n");
}
else
{
    printf("through mode failed !\r\n");
}
```

R02[1:0]	0	1(Default)	2
Input Format	RGBDummy	YUV	Through mode

2.配置模式（Non-interlace）

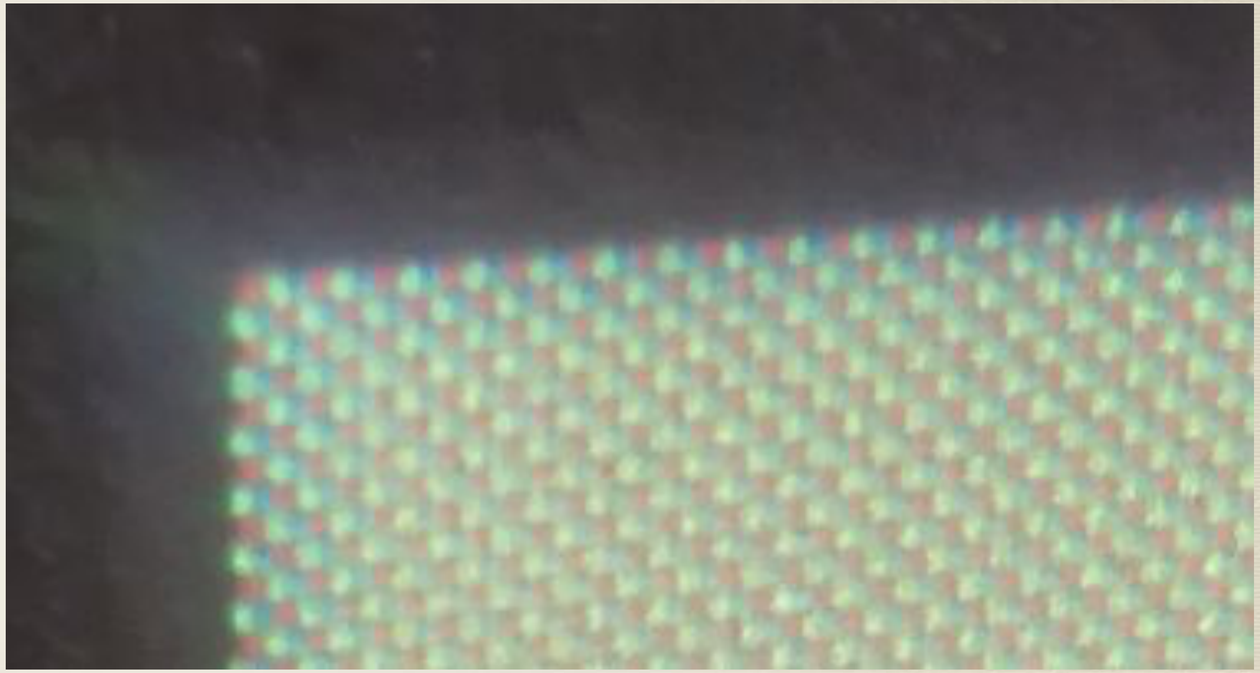
```
data = spi_read(0x3);
data &= ~(0x1 << 0);
data |= 0x1; //Non-interlace
spi_write(0x3, data);
if(spi_read(0x3) == data)
{
    printf("Non-interlace ok !\r\n");
}
else
{
    printf("Non-interlace failed !\r\n");

}
```

R03[0]	0(Default)	1
Interlace Mode	Interlace	Non-interlace

3.发送数据

VD：场同步，回到场的开始坐标
HD：行同步，开始新一行
DIN[7:0]：当前点的亮度
DCLK：一个时钟传输一个点的亮度

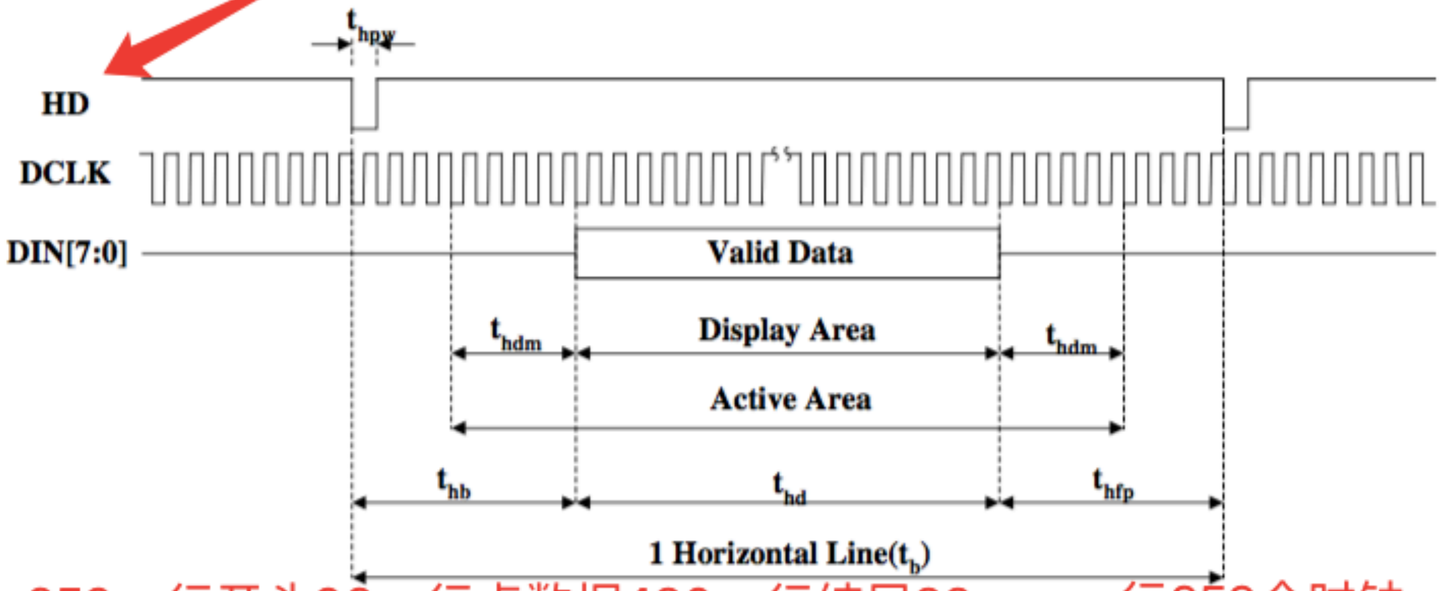
奇行：红绿蓝
偶行：绿蓝红



3.发送数据

12 Through mode

--Horizontal-- 行同步以DCLK为单位

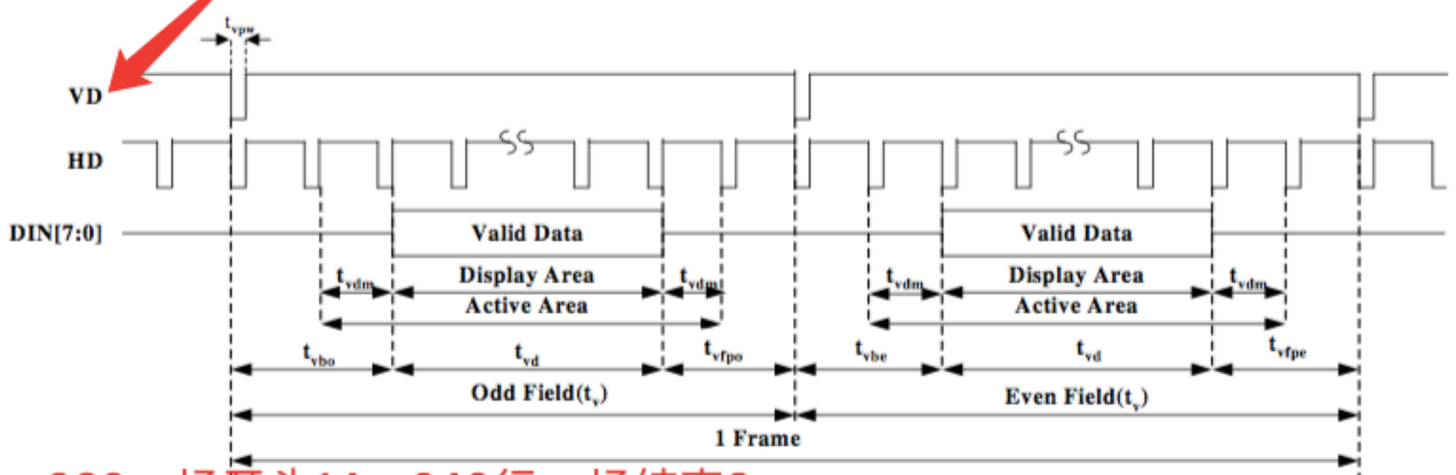


659 = 行开头96 + 行点数据480 + 行结尾83　　一行659个时钟

Parameter		Symbol	Panel Resolution			Unit
DCLK Frequency		f_{clk}	10.36	12.90	18.42	MHz
Horizontal valid data		t_{hd}	480	640	960	DCLK
1 Horizontal Line		t_h	659	820	1171	DCLK
HSYNC Pulse Width	Min.	t_{hpw}	1			DCLK
	Typ.		1			
	Max.		--			
Hsync blanking		t_{hb}	96	117	152	DCLK
Hsync front porch		t_{hfp}	83	63	59	DCLK
Horizontal dummy time		t_{hdm}	0	4	0	MCLK

3.发送数据

Non-interlace 场同步以一行为时钟单位



262 = 场开头14 + 240行 + 场结束8

一场有262个行时钟

Parameter		Symbol	Interlace	Non-interlace	Unit
Vertical valid data		t_{vd}	240	240	H
1 Vertical field		t_v	262.5	262	H
Vsync pulse width	Min.	t_{vpw}	1	1	H
	Typ.		1	1	H
	Max.		-	-	H
Vsync blanking	Odd field	t_{vbo}	14	14	H
	Even field	t_{vbe}	14.5	14	H
Vsync front porch	Odd field	t_{vfpo}	8.5	8	H
	Even field	t_{vfpe}	8	8	H
Vertical dummy time		t_{vdm}	0	0	H