

CMES Exam

a) Model Checking - promela implementation

toyFactory.pml

```
/*
Actors: ProductionDepartment (PD), RequestDepartment (RD)
Signals: PD to RD ( stop ), RD to PD ( car, doll, musicalInstrument )
*/

mtype = {sigPDtoRD, sigRDtoPD};
chan signal = [0] of {mtype};
byte toysToProduce=12;
byte toysProduced=0;

bool production_ended = false;
bool requests_ended = false;

active proctype PD() {
    waiting:
        signal?sigRDtoPD -> atomic {
            if
            :: toysProduced == toysToProduce -> atomic {
                signal!sigPDtoRD;
                goto ready;
            }
            :: else -> atomic {toysProduced++; goto waiting;};
            fi;
        };

    ready: {
        production_ended = true;
    };
}

active proctype RD() {
    sending: atomic {
        if
        :: signal?sigPDtoRD -> atomic {printf("Stop \n"); goto ready;};
        :: toysProduced <= toysToProduce -> atomic {printf("Make Car \n"); signal!sigRDtoPD; goto
sending;};
        :: toysProduced <= toysToProduce -> atomic {printf("Make Doll \n"); signal!sigRDtoPD; goto
sending;};
        :: toysProduced <= toysToProduce -> atomic {printf("Make Musical Instrument \n");
signal!sigRDtoPD; goto sending;};
}
```

```
        fi;
    };
    ready: {
        requests_ended = true;
    };
}

/*
LTL formulas

[] (toysProduced <= toysToProduce)
<> (toysProduced == toysToProduce)
*/
```

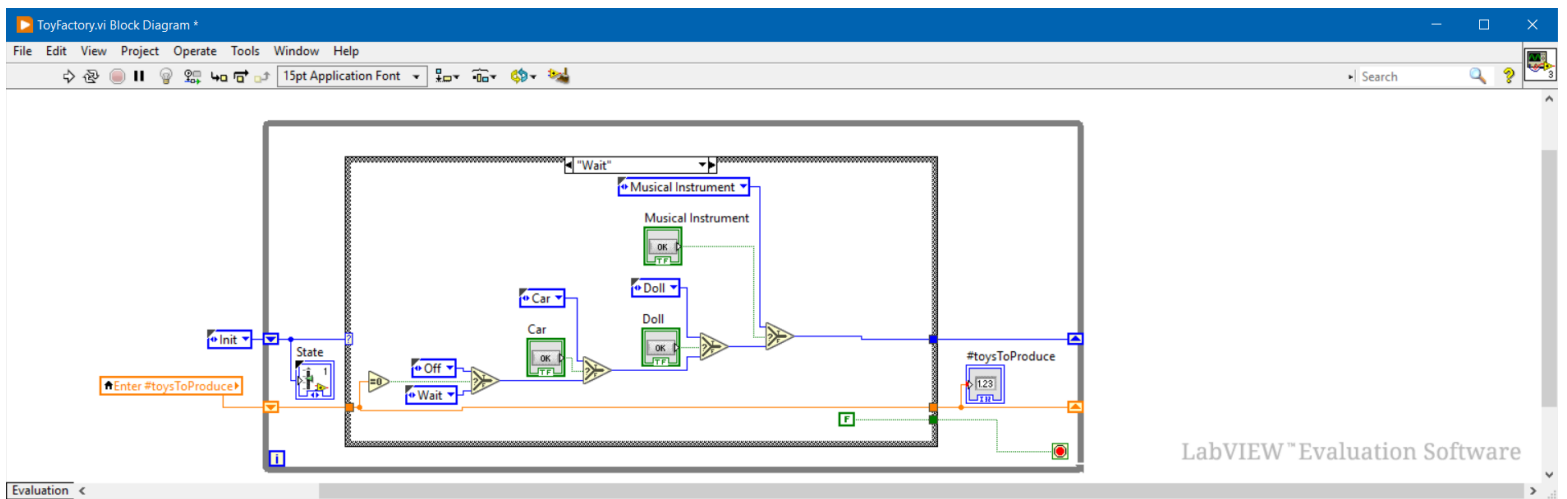
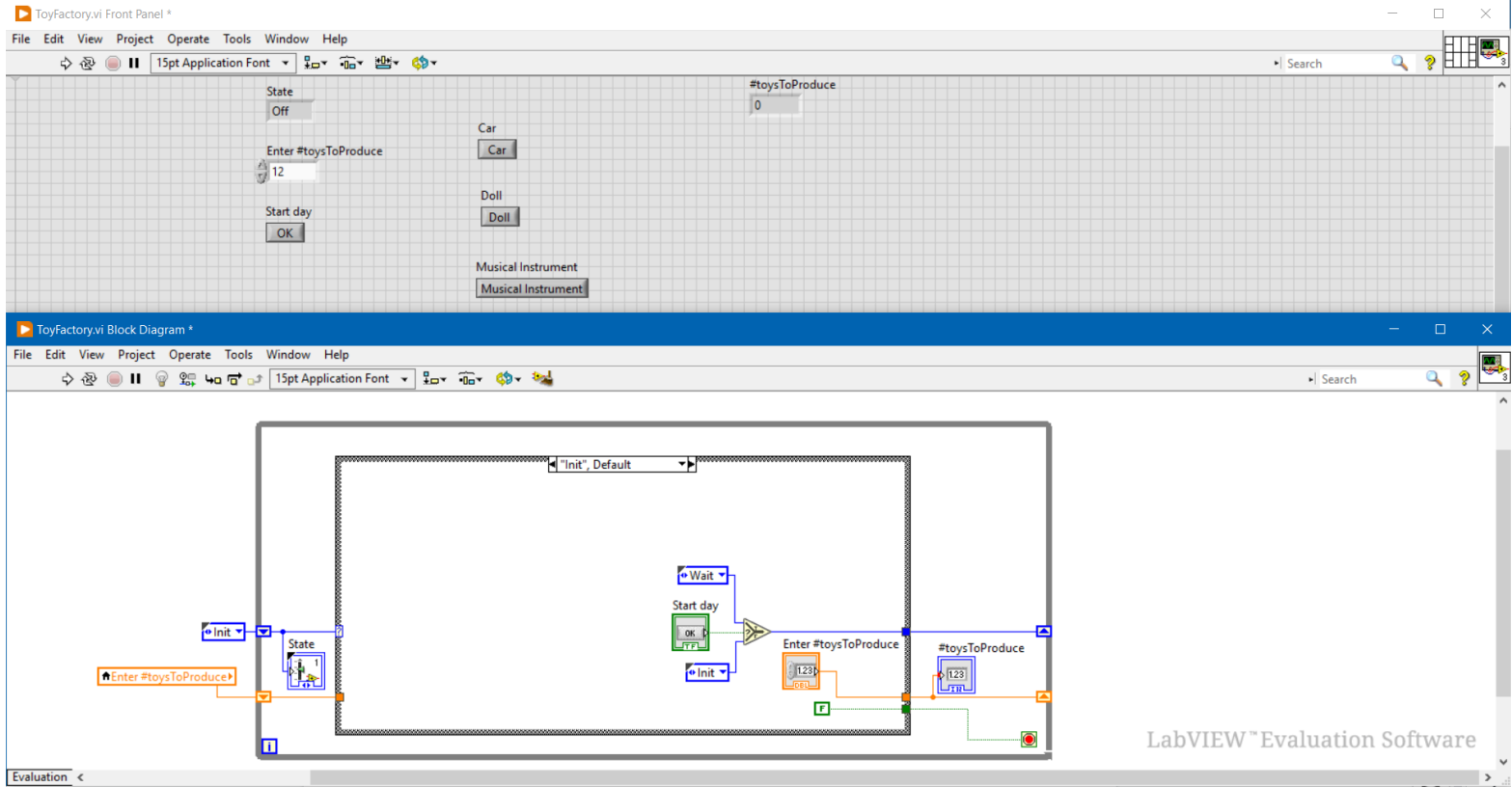
Output:

```
0:      proc - (:root:) creates proc 0 (PD)
0:      proc - (:root:) creates proc 1 (RD)
1 RD 33 toysProduced<=
Make Car
1 RD 36 printf('Make C
1 RD 36 signal!sigRDto
0 PD 16 signal?sigRDto
1 RD 36 values: !sigR
0 PD 16 values: !?sigR
0 PD 17 else
0 PD 22 toysProduced =
Process Statement      toysProduc
1 RD 33 toysProduced<= 1
Make Musical Instrument
1 RD 38 printf('Make M 1
1 RD 38 signal!sigRDto 1
0 PD 16 signal?sigRDto 1
1 RD 38 values: !sigR 1
0 PD 16 values: !?sigR 1
0 PD 17 else      1
0 PD 22 toysProduced = 1
1 RD 33 toysProduced<= 2
Make Car
1 RD 36 printf('Make C 2
1 RD 36 signal!sigRDto 2
0 PD 16 signal?sigRDto 2
1 RD 36 values: !sigR 2
0 PD 16 values: !?sigR 2
0 PD 17 else      2
0 PD 22 toysProduced = 2
1 RD 33 toysProduced<= 3
Make Doll
1 RD 37 printf('Make D 3
1 RD 37 signal!sigRDto 3
0 PD 16 signal?sigRDto 3
Process Statement      toysProduc
1 RD 37 values: !sigR 3
```

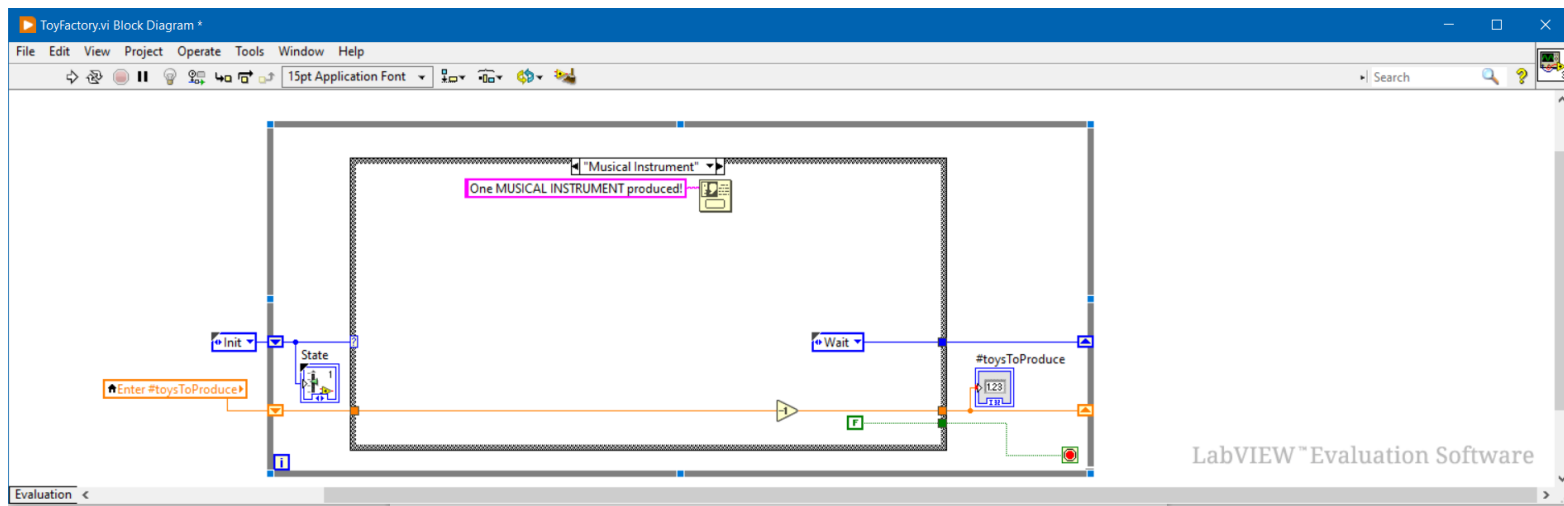
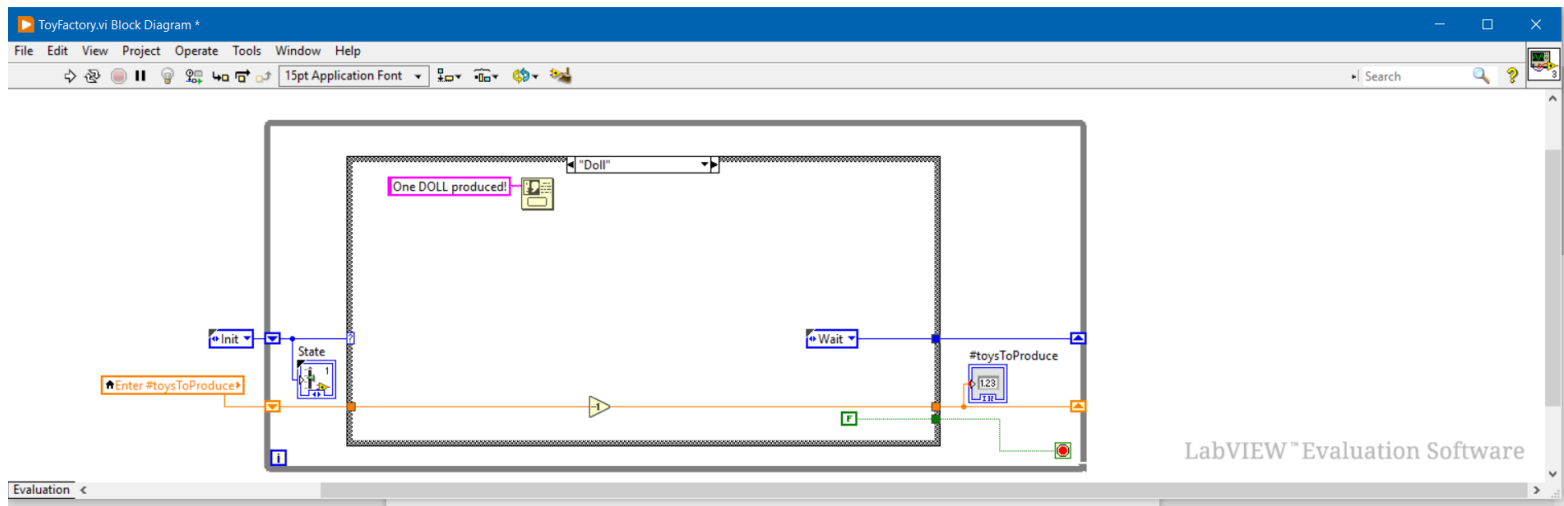
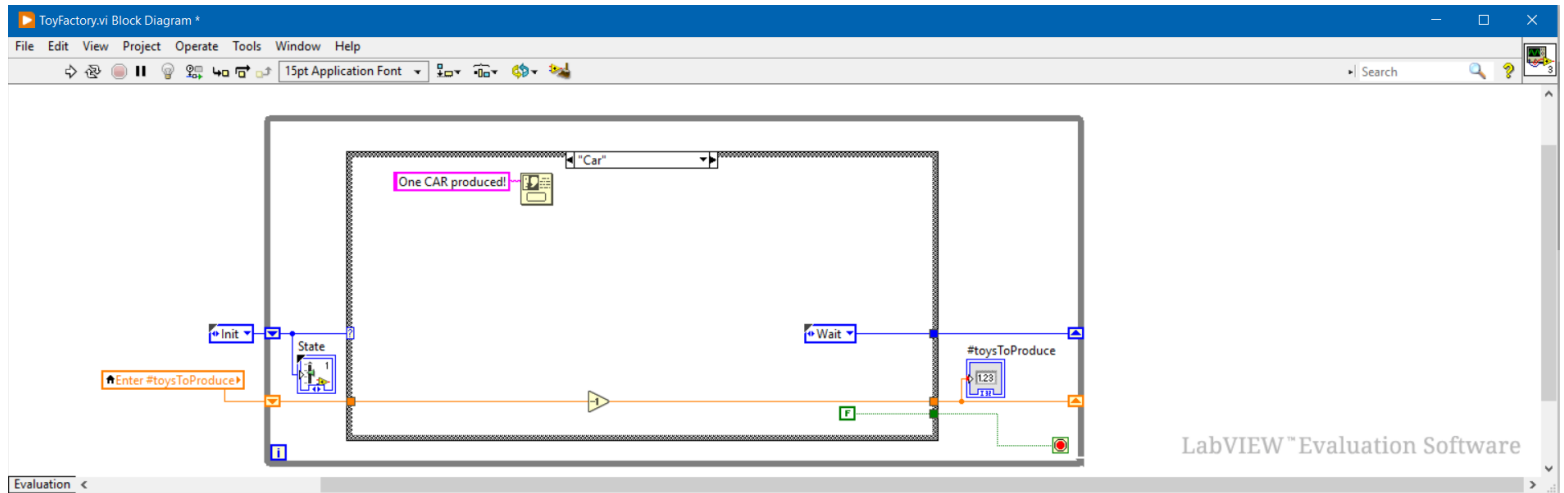
```
0 PD 16 values: 1?sigR 3
0 PD 17 else 3
0 PD 22 toysProduced = 3
1 RD 33 toysProduced<= 4
Make Doll
1 RD 37 printf('Make D 4
1 RD 37 signal!sigRDto 4
0 PD 16 signal?sigRDto 4
1 RD 37 values: 1!sigR 4
0 PD 16 values: 1?sigR 4
0 PD 17 else 4
0 PD 22 toysProduced = 4
1 RD 33 toysProduced<= 5
Make Car
1 RD 36 printf('Make C 5
1 RD 36 signal!sigRDto 5
0 PD 16 signal?sigRDto 5
1 RD 36 values: 1!sigR 5
0 PD 16 values: 1?sigR 5
0 PD 17 else 5
0 PD 22 toysProduced = 5
Process Statement toysProduc
1 RD 33 toysProduced<= 6
Make Doll
1 RD 37 printf('Make D 6
1 RD 37 signal!sigRDto 6
0 PD 16 signal?sigRDto 6
1 RD 37 values: 1!sigR 6
0 PD 16 values: 1?sigR 6
0 PD 17 else 6
0 PD 22 toysProduced = 6
1 RD 33 toysProduced<= 7
Make Car
1 RD 36 printf('Make C 7
1 RD 36 signal!sigRDto 7
0 PD 16 signal?sigRDto 7
1 RD 36 values: 1!sigR 7
0 PD 16 values: 1?sigR 7
0 PD 17 else 7
0 PD 22 toysProduced = 7
1 RD 33 toysProduced<= 8
Make Car
1 RD 36 printf('Make C 8
1 RD 36 signal!sigRDto 8
0 PD 16 signal?sigRDto 8
Process Statement toysProduc
1 RD 36 values: 1!sigR 8
0 PD 16 values: 1?sigR 8
0 PD 17 else 8
0 PD 22 toysProduced = 8
1 RD 33 toysProduced<= 9
Make Doll
1 RD 37 printf('Make D 9
```

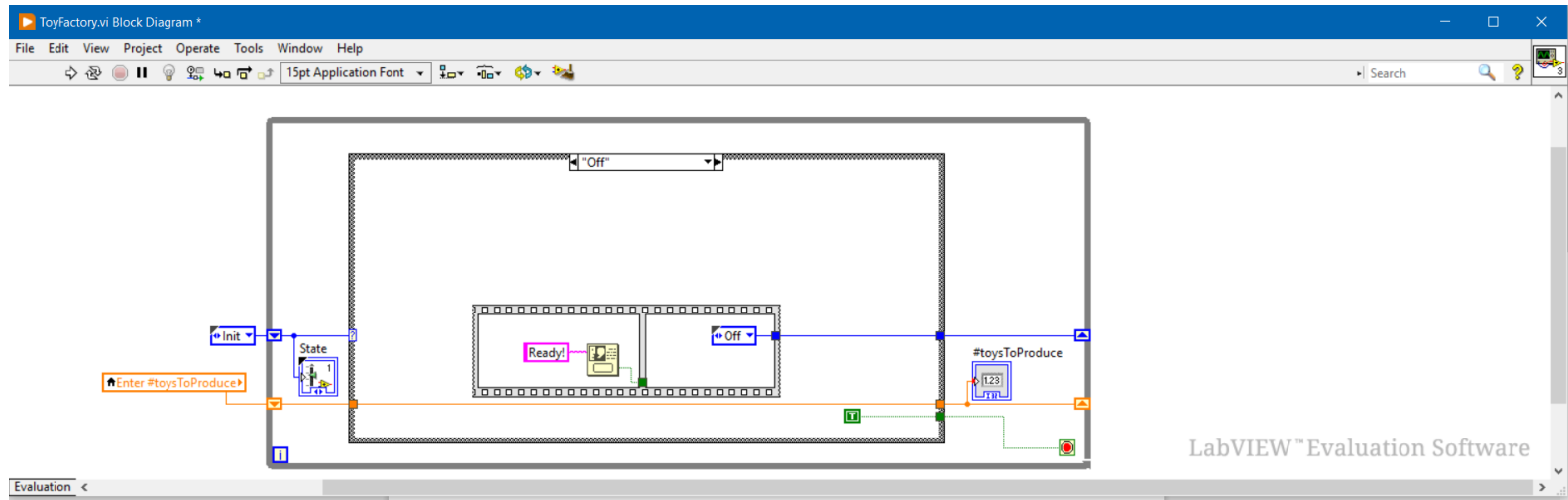
```
1 RD 37 signal!sigRDto 9
0 PD 16 signal?sigRDto 9
1 RD 37 values: !sigR 9
0 PD 16 values: !sigR 9
0 PD 17 else 9
0 PD 22 toysProduced = 9
1 RD 33 toysProduced<= 10
Make Car
1 RD 36 printf('Make C 10
1 RD 36 signal!sigRDto 10
0 PD 16 signal?sigRDto 10
1 RD 36 values: !sigR 10
0 PD 16 values: !sigR 10
0 PD 17 else 10
0 PD 22 toysProduced = 10
Process Statement toysProduc
1 RD 33 toysProduced<= 11
Make Doll
1 RD 37 printf('Make D 11
1 RD 37 signal!sigRDto 11
0 PD 16 signal?sigRDto 11
1 RD 37 values: !sigR 11
0 PD 16 values: !sigR 11
0 PD 17 else 11
0 PD 22 toysProduced = 11
1 RD 33 toysProduced<= 12
Make Musical Instrument
1 RD 38 printf('Make M 12
1 RD 38 signal!sigRDto 12
0 PD 16 signal?sigRDto 12
1 RD 38 values: !sigR 12
0 PD 16 values: !sigR 12
0 PD 17 toysProduced== 12
0 PD 19 signal!sigPDto 12
1 RD 35 signal?sigPDto 12
0 PD 19 values: !sigP 12
1 RD 35 values: !sigP 12
Stop
1 RD 35 printf('Stop \ 12
Process Statement toysProduc
0 PD 28 production_end 12
Process Statement production toysProduc
1 RD 43 requests_ended 1 12
68: proc 1 (RD) terminates
68: proc 0 (PD) terminates
2 processes created
```

b) LabView implementation



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c) Petri net representation

