Alexandria University
Faculty of Engineering
Computer and Systems Engineering Department
CS 401 – Graduation Project



# Graduation Project General-Purpose Computer and Game Console

MIPS-I Instruction Set Architecture

#### Student:

- Mostafa Abd El-Aziz (65)

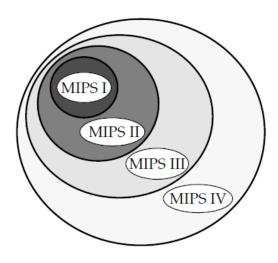
### **Supervisor:**

- Prof. Dr. Layla Abo Hadid

#### Introduction:

This document contains a summary for MIPS-I instruction set, as well as pointers to related parts in "MIPS IV Instruction Set."

There are several versions of MIPS, as MIPS-I ISA was extended three times. The newer MIPS instruction sets are backward compatible with MIPS-I instruction set, as seen in the figure below.



MIPS Architecture Extensions

# **Instruction Set:**

Instructions are divided into several groups:

- Load and Store
- ALU
- Jump and Branch
- Miscellaneous
- Coprocessor

Following is a listing for instructions with references to pages in "MIPS IV Instruction Set" that describe the instructions.

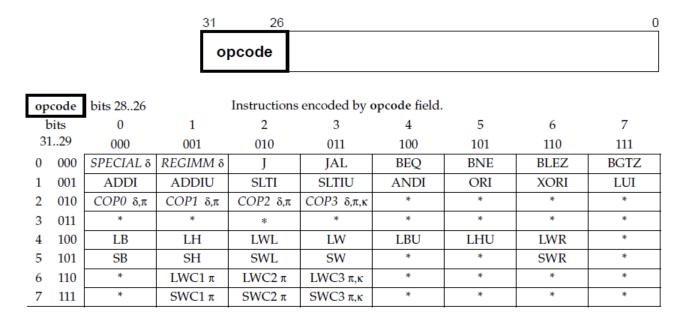
Load and Store Instructions						
Mnemonic	Description	Page				
LB	Load Byte	A-80				
LBU	Load Byte Unsigned	A-81				
SB	Store Byte	A-123				
LH	Load Halfword	A-91				
LHU	Load Halfword Unsigned	A-92				
SH	Store Halfword	A-139				
LW	Load Word	A-98				
SW	Store Word	A-152				
LWL	Load Word Left	A-101				
LWR	Load Word Right	A-104				
SWL	Store Word Left	A-155				
SWR	Store Word Right	A-158				
	ALU Instructions	·				
Mnemonic	Description	Page				
ADDI	Add Immediate Word	A-29				
ADDIU	Add Immediate Unsigned Word	A-30				
SLTI	Set on Less Than Immediate	A-143				
SLTIU	Set on Less Than Immediate Unsigned	A-144				
ANDI	And Immediate	A-33				
ORI	Or Immediate	A-119				
XORI	Exclusive OR Immediate	A-179				

LUI	Load Upper Immediate	A-97			
ADD	Add Word	A-28			
ADDU	Add Unsigned Word	A-31			
SUB	Subtract Word	A-150			
SUBU	Subtract Unsigned Word	A-151			
SLT	Set on Less Than	A-142			
SLTU	Set on Less Than Unsigned	A-145			
AND	And	A-32			
OR	Or	A-118			
XOR	Exclusive Or	A-178			
NOR	Nor	A-117			
SLL	Shift Word Left Logical	A-140			
SRL	Shift Word Right Logical	A-148			
SRA	Shift Word Right Arithmetic	A-146			
SLLV					
SRLV	-				
SRAV	Shift Word Right Arithmetic Variable	A-147			
MULT	Multiply Word	A-115			
MULTU	Multiply Unsigned Word	A-116			
DIV	Divide Word	A-60			
DIVU	Divide Unsigned Word	A-62			
MFHI	Move From HI	A-109			
MTHI	Move To HI	A-113			
MFLO	Move From LO	A-110			
MTLO	Move To LO	A-114			
	Jump and Branch Instructions				
Mnemonic Description					
J	Jump	A-76			
JAL	Jump and Link	A-77			
JR	Jump Register	A-79			
JALR	Jump and Link Register	A-78			
BEQ	Branch on Equal	A-34			
BNE	Branch on Not Equal	A-50			

BLEZ	Branch on Less Than or Equal To Zero	A-43				
BGTZ	Branch on Greater Than Zero	A-41				
BLTZ	Branch on Less Than Zero	A-45				
BGEZ	Branch on Greater Than or Equal To Zero	A-36				
BLTZAL	Branch on Less Than Zero and Link	A-46				
BGEZAL	Branch on Greater Than or Equal To Zero and Link	A-37				
Miscellaneous Instructions						
Mnemonic	Description	Page				
SYSCALL	System Call	A-165				
BREAK	Breakpoint	A-52				

# **Instruction Encoding:**

Page A-177 summarizes CPU instruction encoding for MIPS-I instruction set. Instructions are grouped in three classes based on their opcode.



Class A Instructions

;	31 26	5	0
	opcode = SPECIAL	function	1

fun	function bits 20 Instructions encoded by function field when opcode field = SPECIAL.								ECIAL.
bits 0		1	2	3	4	5	6	7	
53		000	001	010	011	100	101	110	111
0	000	SLL	*	SRL	SRA	SLLV	*	SRLV	SRAV
1	001	JR	JALR	*	*	SYSCALL	BREAK	*	*
2	010	MFHI	MTHI	MFLO	MTLO	*	*	*	*
3	011	MULT	MULTU	DIV	DIVU	*	*	*	*
4	100	ADD	ADDU	SUB	SUBU	AND	OR	XOR	NOR
5	101	*	*	SLT	SLTU	*	*	*	*
6	110	*	*	*	*	*	*	*	*
7	111	*	*	*	*	*	*	*	*

## Class B Instructions

31 26	20 ′	<u>16</u> 0
opcode = REGIMM	rt	

	rt	bits 1816		Instructions encoded by the rt field when opcode field = REGIMM.					
bits		0	1	2	3	4	5	6	7
2019		000	001	010	011	100	101	110	111
0	00	BLTZ	BGEZ	†	†	†	†	†	†
1	01	†	†	†	†	†	†	†	†
2	10	BLTZAL	BGEZAL	†	†	†	†	†	†
3	11	†	†	†	†	†	†	†	†

Class C Instructions