



Graduation Project Proposal

General-Purpose Computer and Game Console

Design and Implementation for Hardware and Operating System

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Supervisor:

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Description:

The main target of the project is to design and implement a digital computer system (both hardware and software sides) that will be based on **MIPS I** instruction set architecture. The general-purpose computer system shall also be able to run games and programs written for **Sony Playstation 1 (PS1)**, which was based on a MIPS microprocessor.

Quafios will be introduced as the main operating system for this computer. We may introduce extra components for Quafios as part of this project, like TCP/IP stack. If we fail to run Quafios on the new system, we might rewrite a smaller clone of Quafios.

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Quafios text editor (Command mode) - /home/COPYING
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Version 3, 29 June 2007

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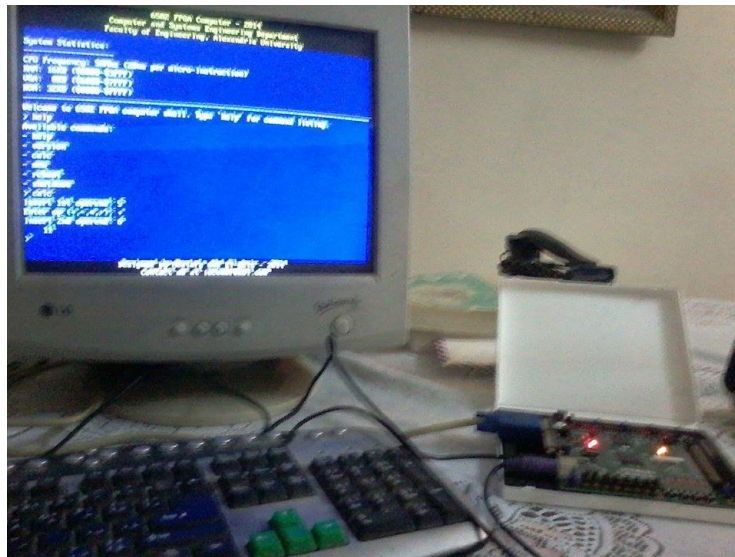
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Quafios operating system (on IBM-compatible PC)

We are not sure if we will be able to implement a real Playstation-compatible computer using the **FPGA** and hardware devices we currently have. So, in case we are not able to support PS1, a backup plan is to support **6502**-based **Nintendo Entertainment System** (NES, also known as Famicom in Japan) games. We might also implement both PS1 and NES!

Hardware Components:

- **CPU**: it is going to be a pipelined implementation for the MIPS I architecture. Mostly, the CPU core will be compatible with **R3000A** chip, developed by *MIPS Computer Systems*. The R3000 chip contains an additional “control processor”, which includes an MMU and a TLB to implement virtual memory. An instruction cache and a data cache will be implemented.
- **RAM**: 16MB SDRAM will be used.
- **ROM**: 16MB Flash ROM will be used to store BIOS.
- **GPU**: I have already designed a video adapter on FPGA. The adapter supports text-mode only (with resolution of 640x480 pixels → 30 rows * 80 columns). I can use it temporarily until I design a clone of Sony Playstation's GPU, which will need an external micro-controller and 1MB SRAM.



FPGA computer with 6502 microprocessor and a text-mode VGA

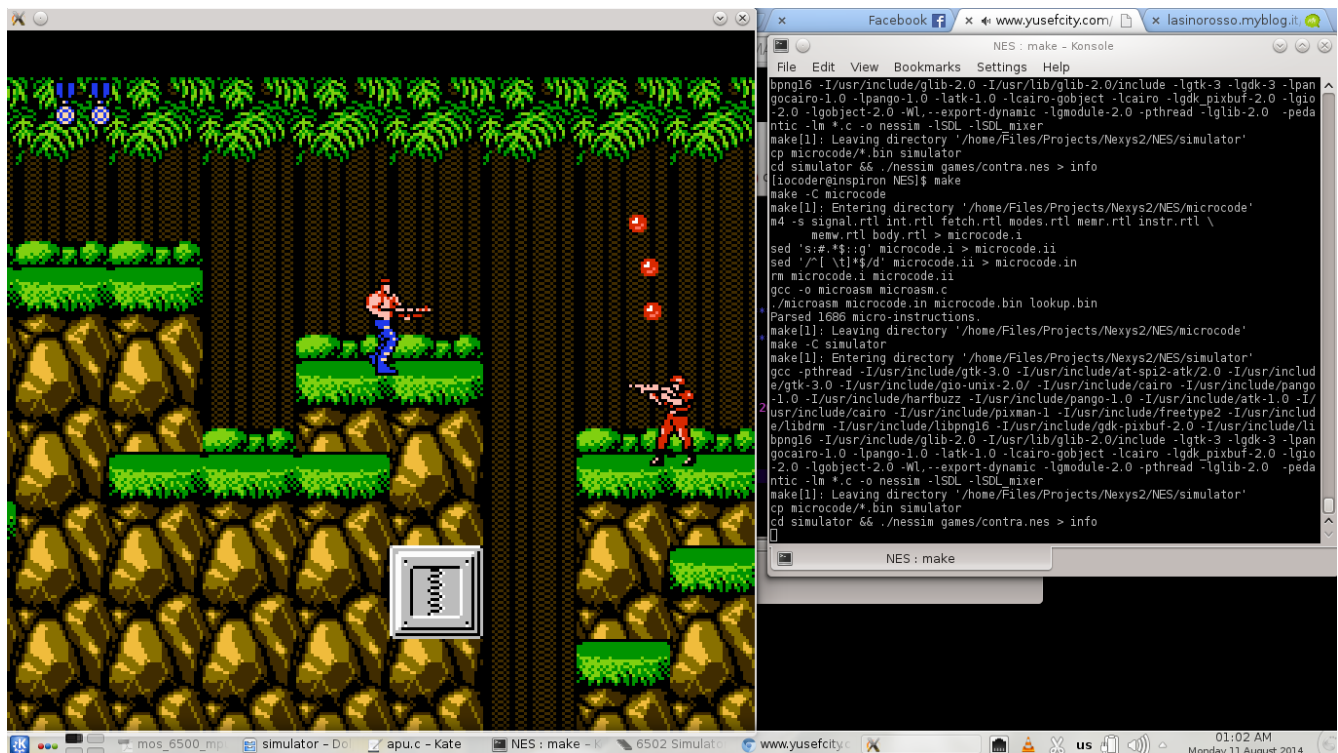
- **SPU** (Sound processing unit): I intend to use an external Z80 chip to process sound. It will mostly be compatible with PS1's SPU.
- **CD-ROM controller**: PS1 uses CD-ROMs to store games.
- **SDCard slot**: to interface the SDCard that stores Quafios.
- **PS/2 controller**: to interface keyboard.
- **Programmable Timer**.
- **Ethernet controller (optional)**.

Software Components:

- **BIOS:** Firmware for the computer.
- **Operating System:** Quafios.

Nintendo Entertainment System:

For NES, I am not sure if I am going to implement an additional 6502 microprocessor to run NES games, or I will just emulate them in Quafios or BIOS. The GPU is to be modified to be compatible with NES Picture Processing Unit (PPU). This is feasible; I have already written a simulator for NES PPU. If we are going to support NES games, then it will take us extra work because NES sound system is greatly different from PS1.



NES simulator

Proposed Implementations:

- **Simulation:** I have already finished a simulator for MIPS-1 (but no pipeline, cache, etc...), which can be turned into a simulator for R3000A-based computer, then a simulator for Sony Playstation 1.
- **FPGA:** It is a good idea to implement the MIPS processor using FPGA. A Digilent Nexys II board with Spartan-3 500K-gate FPGA chip will mostly be used.
- **Micro-controllers** and **SRAM** for peripherals (display, sound, etc...).
- If we have time, I might dig into **VLSI** topic.

Proposed Plan:

1. Complete the simulator of R3000A chip (see above).
2. Run Quafios (or a minimal clone of Quafios) on the simulator.
3. Write VHDL code for MIPS processor (pipeline, cache, MMU, TLB, etc...), then integrate it with the already-made VGA-comptaible VHDL unit and PS/2 keyboard controller. Now we have a usable MIPS computer implemented on FPGA.
4. Work on Playstation compatibility (both simulation and hardware implementation):
 - The PS1-compatible GPU.
 - CD-ROM.
 - BIOS.
 - Game controllers (or just use keyboard).
 - SPU (sound processing unit).
5. Work on Nintendo Entertainment System (NES) compatibility:
 - 6502 microprocessor (or just emulation inside Quafios).
 - NES PPU (picture processing unit, won't be efficient if emulated inside Quafios).
 - Game controllers (or just use keyboard).
 - Cartridge interface (or just emulation inside Quafios).
 - NES sound system (won't be efficient if emulated inside Quafios).
6. Work on extras (depend on how much time we will have):
 - Ethernet interface in FPGA.
 - TCP/IP protocol stack.
 - SATA interface.
 - Bring sound to Quafios.
 - VLSI.

Objectives Behind This Work:

1. Apply the topics I have studied in my computer engineering curriculum at university (like computer architecture, organization, digital design, operating systems, systems programming, embedded systems, and microprocessors).
2. Learn new topics and technologies (Sony Playstation architecture, NES architecture, sound, TCP/IP implementation, etc...)
3. Have fun.