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CSC 137

Homework #5

Problem 1 Consider the sequential circuit in Figure 5.31 where the adder is CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flops register set-up time, clock-to-q, and clock-skew are each 0.1 ns, AND gate = 0.2 ns, and EXOR = 0.3 ns. Determine the upper bound for its clock frequency.

Longest Path Delay

$$= \Delta AND + \Delta EXOR + \Delta AND + \Delta T_{DFlip}$$

$$= 0.2ns + 0.3ns + 0.2ns + 0.3ns$$

$$= 1.0\,ns$$

Upper Bound Frequency

$$= \frac{1}{\text{Longest Path Delay}}$$

$$= \frac{1}{1.0\,ns}$$

$$= \boxed{1\ GHz}$$

Problem 3 Textbook problem 5.11 (FSD only)