[illegible]
CoE 13[illegible]

Homework #3

1.) Design a single cell - 1 bit Carry propagate (Ripple Carry Adder) full adder.

ⓐ Generate the truth table

	INPUTS			OUTPUTS	
	A_x	B_x	C_{IN}	S_x	C_{OUT}
r_0	0	0	0	0	0
r_1	0	0	1	1	0
r_2	0	1	0	1	0
r_3	0	1	1	0	1
r_4	1	0	0	1	0
r_5	1	0	1	0	1
r_6	1	1	0	0	1
r_7	1	1	1	1	1

ⓑ Using K-map, determine the logical expression for Carry out (C-out) and Sum (S)

$$S_x = \overline{A_x}\,\overline{B_x}\,C_{IN} + \overline{A_x}\,B_x\,\overline{C_{IN}} + A_x\,\overline{B_x}\,\overline{C_{IN}} + A_x\,B_x\,C_{IN}$$

$$\boxed{S_x = A_x \oplus B_x \oplus C_{IN}}$$

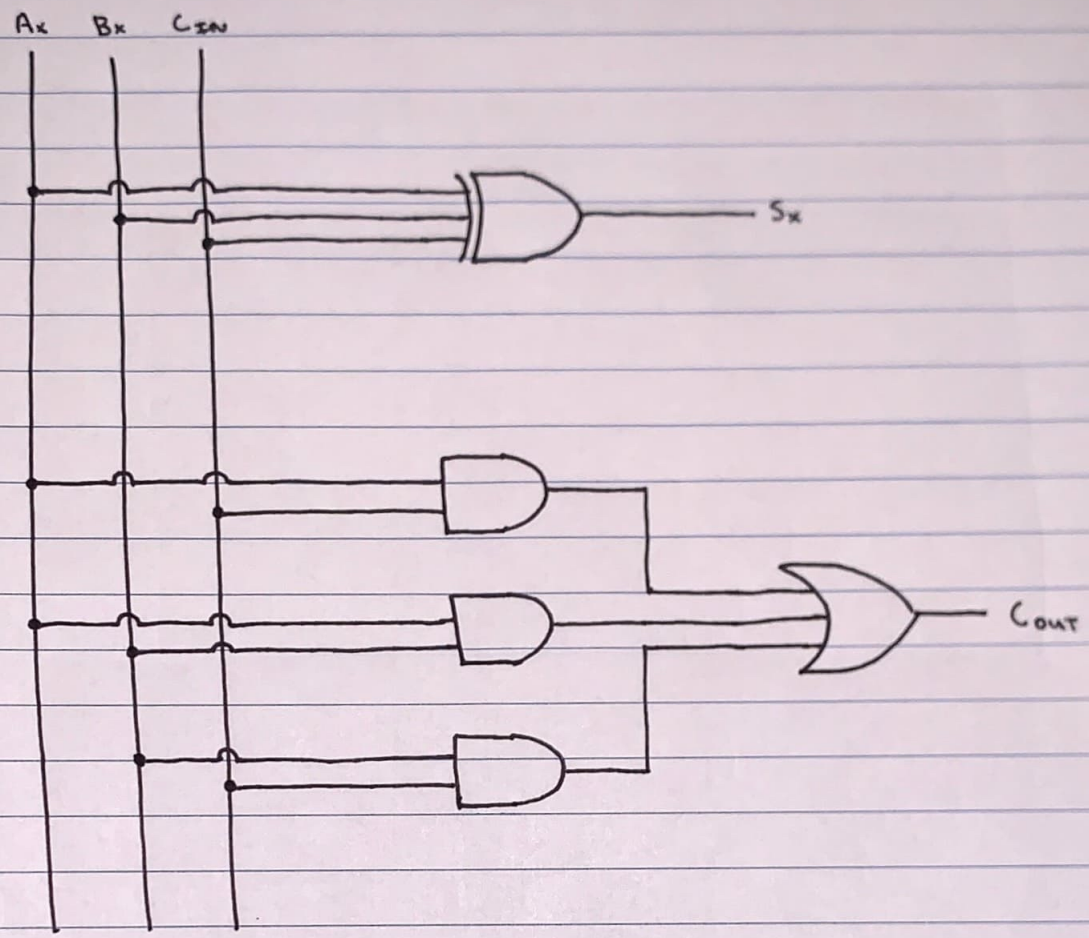
A_x \ $B_x C_{IN}$	00	01	11	10
0		1		1
1	1		1	

$$C_{OUT} = \overline{A_x}\,B_x\,C_{IN} + A_x\,\overline{B_x}\,C_{IN} + A_x\,B_x\,\overline{C_{IN}} + A_x\,B_x\,C_{IN}$$

$$\boxed{C_{OUT} = A_x C_{IN} + A_x B_x + B_x C_{IN}}$$

A_x \ $B_x C_{IN}$	00	01	11	10
0			1	
1		1	1	1

© Based on the logical expression, create the schematic diagram for full adder



2.) Design a 1 bit, 2 to 1 multiplexer (Mux). Outputs Y when S=0; X when S=1.

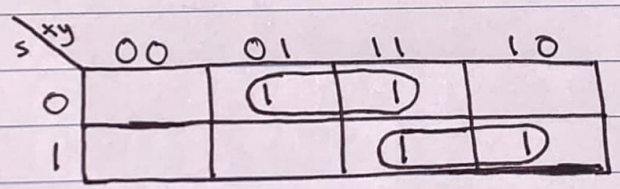
(a) Generate the truth table

Selector	Input		Output
S	X	Y	r
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(b) Using K-map, determine the logical expression for output

$$r = \bar{S}\bar{x}y + \bar{S}xy + Sx\bar{y} + Sxy$$

$$\boxed{r = \bar{S}y + Sx}$$



© Based on the logical expression, create the schematic diagram for Mux