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CSC 137

Homework 6

(6.1) Calculate the required maximum clock frequency for each of the following data paths:

(a) Single-cycle data path in Fig 6.2

[redacted] = Adder + Adder + Adder/Subtractor + T_{sr} + T_{ca} + T_{cs}

[redacted] = 0.8 ns + 0.8 ns + 1.1 ns + 0.05 ns + 0.05 ns + 0.05 ns

[redacted] = 2.85 ns

$$\text{Maximum Frequency} = \frac{1}{\text{Longest Path Delay}}$$

$$= \frac{1}{2.85\ ns} \cdot \frac{10^9\ ns}{Hz}$$

$$= 350,877,192.982\ Hz$$

$$= \boxed{350.88\ MHz}$$

(b) Multi-cycle data path in Fig 6.3

[redacted] = Mux 1 + adder/subtractor + Mux 2 + T_{sr} + T_{ca} + T_{cs}

= 0.6 ns + 1.1 ns + 0.3 ns + (0.05 ns x 3)

= 2.15 ns

$$\text{Maximum Frequency} = \frac{1}{2.15\ ns}$$

$$= \frac{1}{2.15\ ns} \cdot \frac{10^9\ ns}{Hz}$$

$$= 465,116,279.06977\ Hz$$

$$= \boxed{465.12\ MHz}$$

(c): Pipelined data path in Fig 6.4

= Adder/Subtractor + Register

= 1.1 ns + 0.15 ns

= 1.25 ns

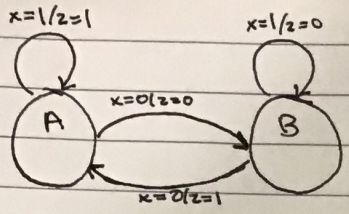
$$\text{Maximum Frequency} = \frac{1}{1.25\,ns} = \frac{1}{1.25\,ns} \cdot \frac{10^9\,ns}{Hz} = 800,000,000\ Hz = 800\ MHz$$

(6.2) Estimate the speedup between the following data paths when generating N = 1000 quantities $A_i + B_i + C_i \pm D_i$ for $i = 0, 1, 2, \ldots, 999$. Ignore the data reading and writing delays.

(a) Problem 6.1a vs. 6.1c

$$\text{Speedup} = \frac{N \cdot k}{k + (N-1)} = \frac{1000 \cdot 3}{3 + (1000-1)} = \frac{3000}{1002} = \boxed{2.994}$$

(5.1)



Number of Bits = $\log_2(2) = 1$

		q_0	x	d_0	z
0	A	0	0	1	0
1		0	1	0	1
2	B	1	0	0	1
3		1	1	1	0

$$d_0 = \overline{q_0}\,\overline{x} + q_0 x = q_0 \oplus x$$

$$z = \overline{q_0} x + q_0 \overline{x} = q_0 \oplus x$$