Homework #7

P1)	In orde	r to	minimize	the .	n officeurb	œ a	read	cycle,	the.	٥٤	can be	0.5584	rtea	at	any
			a maxim												

(A. True)

B. False

(P2) A memory write cycle is similar to a read cycle, except the data must be placed on the data bus at the same time that ce is asserted or within a maximum aday after we is asserted to minimize the time the data bus is used. Figure 7.17 illustrates an SRAM memory write cycles.

I: A memory cycle is initiated by which component in the computer motherboard?

- By the CPU (central Processing Unit)

II: A memory cycle, typically, how many CPU clock cycles to complete?

— It typically takes multiple CPU clock cycles to complete.

(7.10) (ansider a 32-bit data bus SDRAM. Given that the clock frequency of the bus is 200 MHz, what is the peak memory bandwith in megabyte per second (1985)?

(3.11) Consider a 64-bit data bus SDBAM. Given that the clock frequency of the bus is 200 MH2, what is the peak memory bandwith in megabyte per second (MBs)? 64 bits x 1 Byte = 8 Bytes PMB = 200,000,000 SEC × 8 Systes = 1,600,000,000 Bytes = 1,600 MBS (7.12) Consider a 32-bit data bus DDR SDRAM. Given that the clock frequency of the bus is 200 MHz, what is the peak memory bandwith in megabyte per second (MBs)? 32 bits x 1 Byte = 4 Bytes DOR SDRAM -> 4 Bytes x 2 = 8 Bytes PMB = 200,000,000 Sec × 8 Bytes a 1,600,000,000 Bytes 2 1,600 MBS