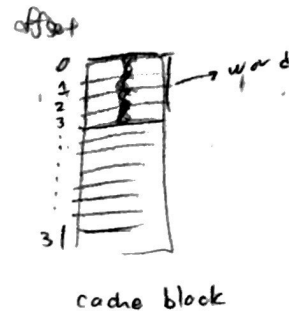


CS M151B HW7 Junhong Wang

5.3.1.

$$2^5 = 32$$



So cache block size is $\frac{32}{4} = 8$ [words]

5.3.2

5.3.4

Address

decimal	binary	replace?
0	0000 0000 0000 0000 0000 0000 0000 0000	N
4	0000 0000 0000 0000 0000 0000 0000 0100	N
16	0000 0000 0000 0000 0000 0000 0001 0000	N
132	0000 0000 0000 0000 0000 0000 1000 0100	N
232	0000 0000 0000 0000 0000 0000 1110 1000	N
160	0000 0000 0000 0000 0000 0000 1010 0000	N
1024	0000 0000 0000 0000 0000 0100 0000 0000	Y
30	0000 0000 0000 0000 0000 0000 0001 1110	Y
140	0000 0000 0000 0000 0000 0000 1000 1100	N
3100	0000 0000 0000 0000 0001 1000 0011 1100	Y
180	0000 0000 0000 0000 0000 0000 1011 0100	N
2180	0000 0000 0000 0000 0000 1000 1000 0100	Y

4 blocks are replaced

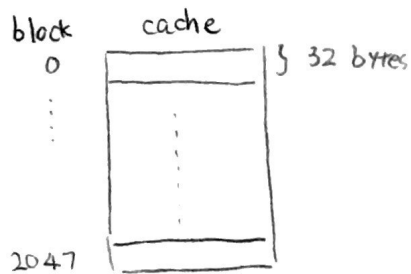
5.3.5.

Address		Hit or Miss
decimal	binary	
0	0000 0000 0000 0000 0000 0000 0000 0000	M
4	0000 0000 0000 0000 0000 0000 0000 0100	H
16	0000 0000 0000 0000 0000 0000 0001 0000	H
132	0000 0000 0000 0000 0000 0000 1000 0100	M
232	0000 0000 0000 0000 0000 0000 1110 1000	M
160	0000 0000 0000 0000 0000 0000 1010 0000	M
1024	0000 0000 0000 0000 0000 0100 0000 0000	M
30	0000 0000 0000 0000 0000 0000 0001 1110	M
140	0000 0000 0000 0000 0000 0000 1000 1100	H
3100	0000 0000 0000 0000 0001 1000 0011 1100	M
180	0000 0000 0000 0000 0000 0000 1011 0100	H
2180	0000 0000 0000 0000 0000 1000 1000 0100	M

$$(\text{hit ratio}) = \frac{4}{12} \times 100 = 33.3\%$$

5.5.1

$$64 \text{ KiB} = 64 \cdot 1024 \text{ bytes}$$



address	block	Hit
0	0	M
2	0	H
4	0	H
6	0	H
8	0	H
10	0	H
12	0	H
14	0	H
16	0	H
18	0	H
20	0	H
22	0	H
24	0	H
26	0	H
28	0	H
30	0	H
32	1	M
⋮	⋮	⋮

$$(\text{Miss Rate}) = \frac{1}{16} \times 100 = 6.25 \text{ (\%)}$$

Miss rate is independent of the size of the cache and the working set.

The misses this workload is experiencing are compulsory misses.

5.5.2

$$16 \text{ bytes} : \frac{1}{8} \cdot 100 = 12.5 [\%]$$

$$64 \text{ bytes} : \frac{1}{32} \cdot 100 = 3.125 [\%]$$

$$128 \text{ bytes} : \frac{1}{64} \cdot 100 = 1.5625 [\%]$$

This workload is exploiting spatial locality.

5.6.2

$$AMAT = (\text{Latency}) + (\text{Miss Rate}) \cdot (\text{Miss Penalty})$$

$$AMAT_{P1} = 0.66 + 0.08 \cdot 70$$

$$= 0.66 + 5.6$$

$$= 6.26 \text{ [ns]}$$

$$AMAT_{P2} = 0.90 + 0.06 \cdot 70$$

$$= 0.90 + 4.2$$

$$= 5.10 \text{ [ns]}$$

5.6.4

$$\begin{aligned} \text{AMAT}_{P_{\text{new}}} &= 0.66 + 0.08 (5.62 + 0.95 \cdot 70) \\ &= 0.66 + 0.08 (5.62 + 66.5) \\ &= 0.66 + 0.08 \cdot 72.12 \\ &= 0.66 + 5.7696 \\ &= 6.4296 \text{ [ns]} \end{aligned}$$

$\text{AMAT}_{P_1} < \text{AMAT}_{P_{\text{new}}}$, so AMAT is
worse with the L2 cache.

5. a

$$AMAT = \frac{(1 + 0.1(10 + 0.2 \cdot 80)) + 0.3(1 + 0.3(10 + 0.2 \cdot 80))}{1.3}$$

$$= \frac{(1 + 0.1 \cdot 26) + 0.3(1 + 0.3 \cdot 26)}{1.3}$$

$$= \frac{3.6 + 0.3 \cdot 8.8}{1.3}$$

$$= 4.8 \quad [\text{cycles}]$$

5.6

$$TCPI = BCPI + MCPI$$

$$BCPI = (\text{peak CPI}) + \sum (\text{hazard rate}) (\text{hazard cost})$$

$$= 1.0 + (\text{control hazard rate}) \cdot (\text{control hazard cost}) \\ + (\text{data hazard rate}) \cdot (\text{data hazard cost})$$

$$= 1.0 + (0.3 \cdot 0.5) \cdot 1 + (0.2 \cdot 0.6) \cdot 1$$

$$= 1.0 + 0.15 \cdot 1 + 0.12$$

$$= 1.0 + 0.15 + 0.12$$

$$= 1.27$$

$$MCPI = (I\#M) + (D\#M)$$

$$= 1 \cdot 0.1 (10 + 0.2 \cdot 80) + 0.2 \cdot 0.3 (10 + 0.2 \cdot 80)$$

$$= 0.1 \cdot 26 + 0.06 \cdot 26$$

$$= 0.16 \cdot 26$$

$$= 4.16$$

$$\therefore TCPI = 1.27 + 4.16 = 5.43$$

5.c

Let x be instruction cache miss rate

$$ET_{OLD} \geq ET_{NEW}$$

$$\Leftrightarrow IC_{OLD} \cdot TCPI_{OLD} \cdot CT_{OLD} \geq IC_{NEW} \cdot TCPI_{NEW} \cdot CT_{NEW}$$

$$\Leftrightarrow IC_{OLD} \cdot TCPI_{OLD} \geq IC_{NEW} \cdot TCPI_{NEW} \quad (\because CT_{NEW} = CT_{OLD} = \frac{1}{2 \cdot 10^9})$$

$$\begin{aligned} \Leftrightarrow & ((\text{Peak CPI})_{OLD} + (\text{control hazard rate})_{OLD} \cdot (\text{control hazard cost})_{OLD} \\ & + (\text{data hazard rate})_{OLD} \cdot (\text{data hazard cost})_{OLD} \\ & + (I\#M)_{OLD} + (D\#M)_{OLD}) \cdot IC_{OLD} \\ & \geq ((\text{Peak CPI})_{NEW} + (\text{control hazard rate})_{NEW} \cdot (\text{control hazard cost})_{NEW} \\ & + (\text{data hazard rate})_{NEW} \cdot (\text{data hazard cost})_{NEW} \\ & + (I\#M)_{NEW} + (D\#M)_{NEW}) \cdot IC_{NEW} \end{aligned}$$

$$\begin{aligned} \Leftrightarrow & (1.0 + (0.3 \cdot 0.5) \cdot 1 + (0.2 \cdot 0.6) \cdot 1 + 1 \cdot 0.1 (10 + 0.2 \cdot 80) + 0.2 \cdot 0.3 (10 + 0.2 \cdot 80)) \cdot IC_{OLD} \\ & \geq (1.0 + (\frac{2}{9} \cdot \frac{1}{4}) \cdot 1 + (\frac{2}{9} \cdot 0.6) \cdot 1 + 1 \cdot x (10 + 0.2 \cdot 80) + \frac{2}{9} \cdot 0.3 (10 + 0.2 \cdot 80)) \cdot IC_{NEW} \end{aligned}$$

$$\Leftrightarrow (0.15 + 0.12 + 0.1 \cdot 26 + 0.06 \cdot 26) \geq (\frac{1}{18} + \frac{2}{15} + x \cdot 26 + \frac{1}{15} \cdot 26) \cdot IC_{NEW}$$

$$\Leftrightarrow 4.43 \cdot IC_{OLD} \geq (\frac{1}{18} + \frac{2}{15} + \frac{26}{15} + 26x) \cdot IC_{NEW}$$

$$\Leftrightarrow 4.43 \cdot \frac{10}{9} \geq \frac{1}{18} + \frac{2}{15} + \frac{26}{15} + 26x$$

$$\Leftrightarrow 26x \leq 4.43 \cdot \frac{10}{9} - \frac{1}{18} - \frac{2}{15} - \frac{26}{15}$$

$$\Leftrightarrow x \leq \frac{1}{26} (4.43 \cdot \frac{10}{9} - \frac{1}{18} - \frac{2}{15} - \frac{26}{15})$$

$$= 0.11538 \dots$$

\therefore instruction miss rate must be $\leq 11.54\%$

100000 instructions
300000 branch instructions
50000 procedure calls
50000 return calls

Total # of instructions is 900000.

- branch instructions : 200000

- taken : 50000

- not taken : 150000

- load instructions : 200000