

CS M151B Practice Final

1. P: too many capacity misses in the data cache

S: increase data cache capacity

D: more latency for data cache access

P: too many control hazards

X: Branch Delay Slots Loop Unrolling With Compiler

X: There may not be enough instructions we can bring to the slots. Also, the compiler needs to know the architecture of the machine to determine how many slots to fill. Increase Code Size

P: dummy look ahead adder is too slow

S: carry select Adder / HCLA

D: consumes more space and power

P: larger immediate field in MIPS ISA

X: modify ISA and increase instruction size reduce register field

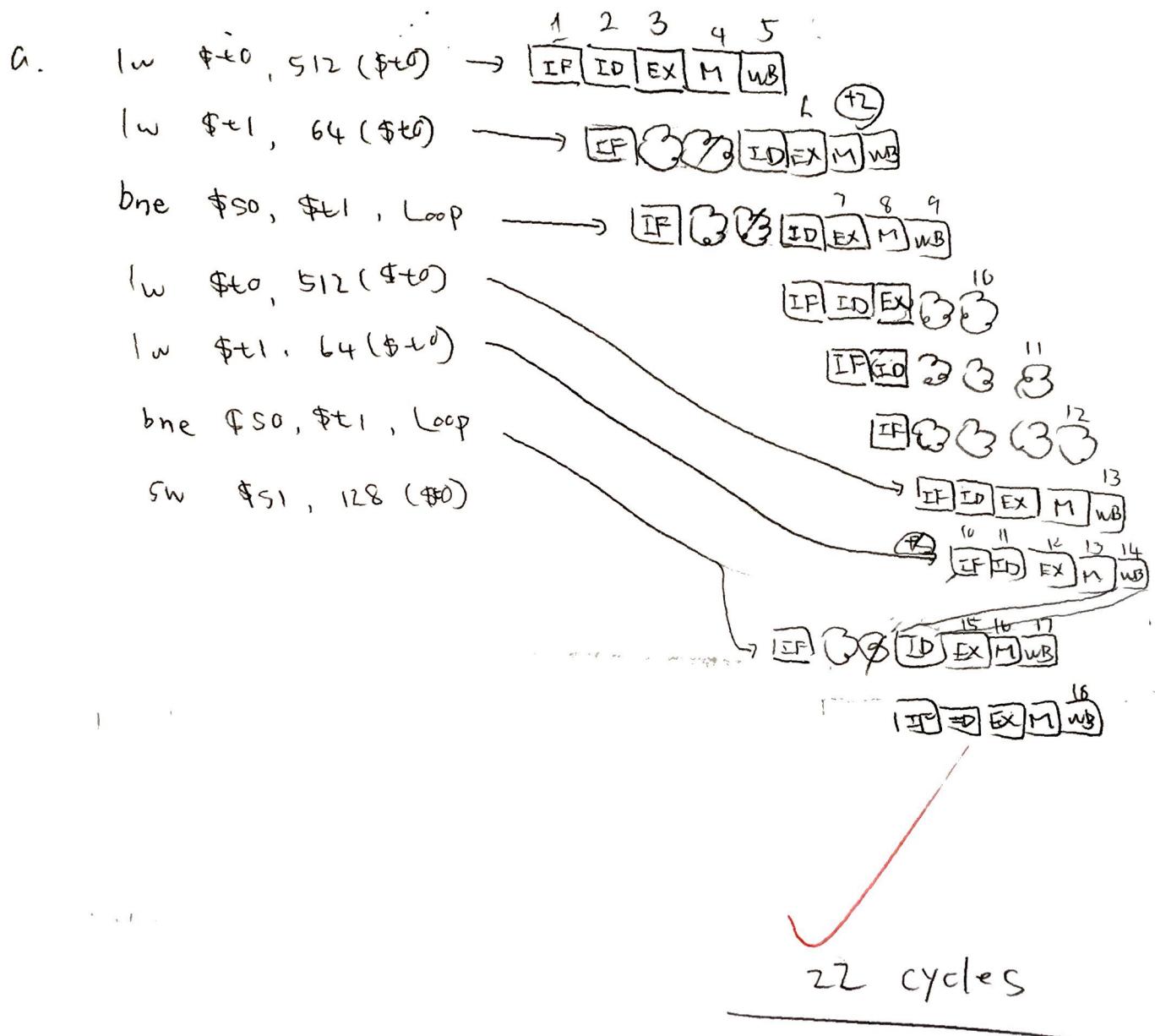
X: move bits to read per instruction. More register spilling

P: ET of CPU with single-cycle data path is too high

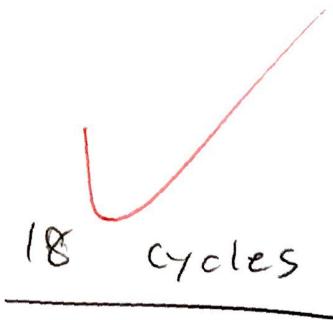
S: use pipelining

D: more hardware complexity

2.



b.



3.

1024 bytes

8

$$\frac{2^{10}}{2^6} = 2^4$$

64-byte blocks



$$2^6 = \frac{2 \cdot 2}{4} \cdot \frac{2 \cdot 2}{4} \cdot \frac{2}{4}$$

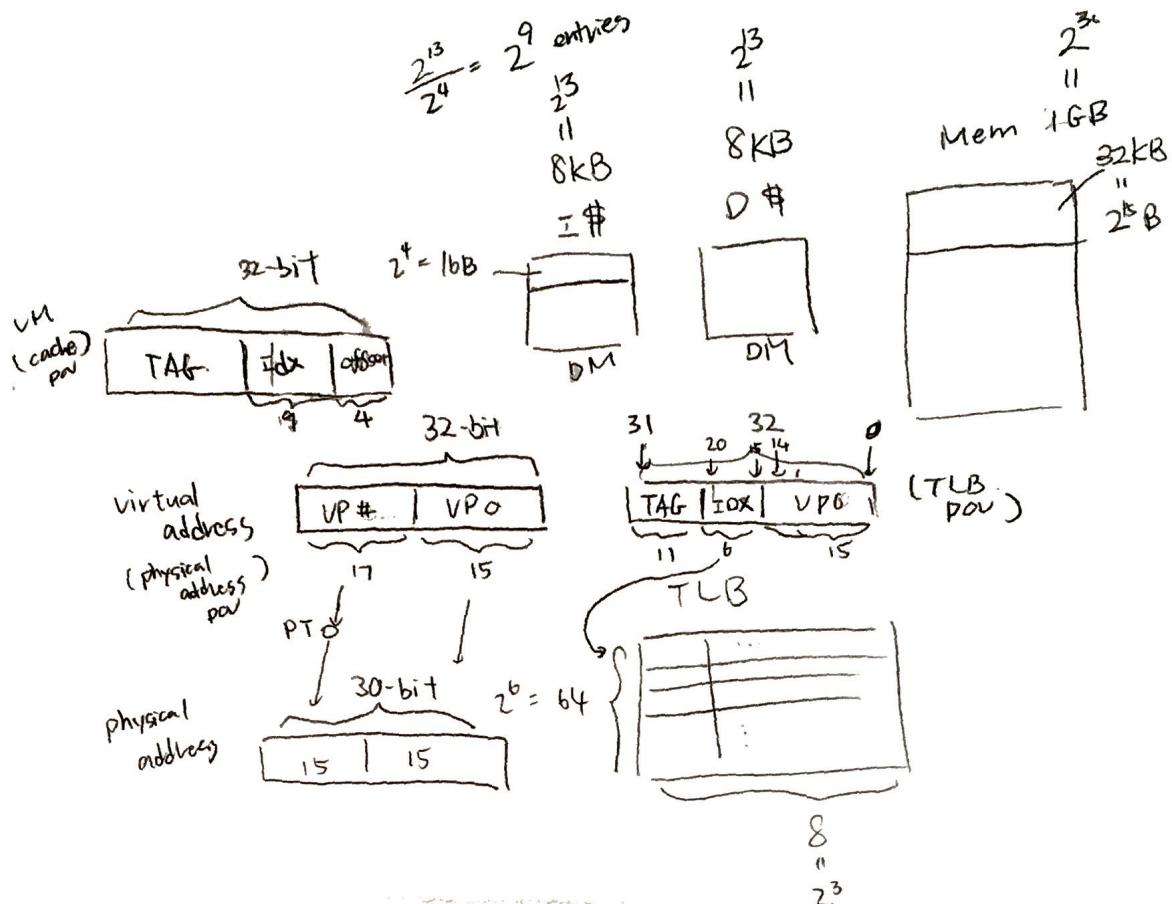
$$\frac{16}{4} \quad \frac{4}{4}$$

$$64$$

address	cache Hit or Miss	Miss Type
... 00110110.0000	M	compulsory
... 0001011100000	M	compulsory
... 0000011010000	M	compulsory
... 0011011100000	M	compulsory
... 0011011010000	H	
... 0001011100000	NM	conflict
... 0000011010000	H	
... 0011011100000	NM	conflict

5. HW

4

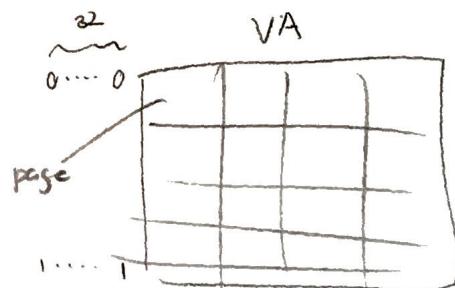


a. $\frac{2^{30}}{2^{15}} = \boxed{2^{15}}$ ✓

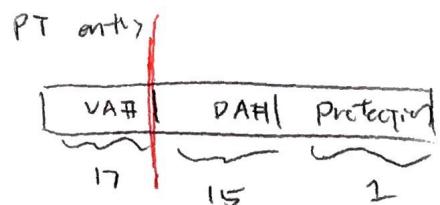
b. $\frac{2^n \cdot 33^2}{2^{15}} = \boxed{2^{14} \cdot 33 \text{ Bytes}}$

c. $\frac{2^6 \cdot 2^3}{2^{17}} = \boxed{\frac{1}{2^8}}$ ✓

d. $\boxed{\text{bits 15 to 20}}$ ✓



$\frac{2^{32}}{2^{15}} = 2^{17} \text{ pages}$



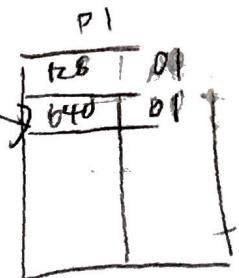
↳ 33-bit

2^{17} entries

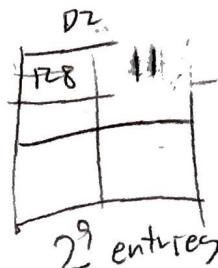
6.

Y/N

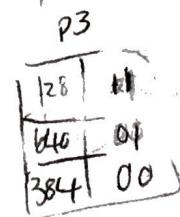
PC	Actual Direction	Correctly Predicted?	Note
128	T	✓ N (NT)	$128 \% 2^0 = 128$ $128 \% 768 = 128$
640	NT	✓ Y (NT)	$640 \% 2^0 = 640$ $640 \% 768 = 640$
1152	NT	✓ Y (NT)	$1152 \% 1024 = 128$ $1152 \% 768 = 384$
128	T	✓ N (NT)	128 128
640	T	✓ N (NT)	640 128
1152	NT	✓ Y (NT)	128 128
128	T	✓ Y (T)	128 128
640	NT	✓ Y (NT)	640 128
1152	NT	✓ Y (NT)	128 128
128	T	✓ N (NT)	128 128
640	T	✓ N (NT)	640 128
1152	NT	✓ Y (NT)	128 128



2^{10} entries
1024



11 entries



768 entries

768

7

7. a.

$$TCPPI = BCPI + MCPI$$

$$BCPI = (\text{peak CPI}) + \sum (\text{hazard rate})(\text{hazard cost})$$

$$= 1.0 + (\text{control hazard rate})(\text{control hazard cost}) \\ + (\text{data hazard rate})(\text{data hazard cost})$$

$$= 1.0 + (0.05 \cdot \frac{1}{3}) \cdot 2 + (0.25 \cdot 0.3) \cdot 1 \\ = 1 + 0.1 + 0.075 \\ = 1.175$$

$$MCPI = (\text{SW M}) + (\text{D M})$$

$$= 1 \cdot 0.1 (10 + 0.05 \cdot 100) + \frac{(0.1 + 0.25) \cdot 0.2 (10 + 0.05 \cdot 100)}{10}$$

$$= 0.1 (10 + 5) + \frac{0.35}{0.07} (10 + 5)$$

$$= \frac{1.5}{0.07} + \frac{0.75}{0.05}$$

$$= 0.9$$

$$2.55$$

$$TCPPI = \frac{1.175 + 2.55}{0.9} = 3.725$$

b. wrong

|w \$t1, O(\$t0)

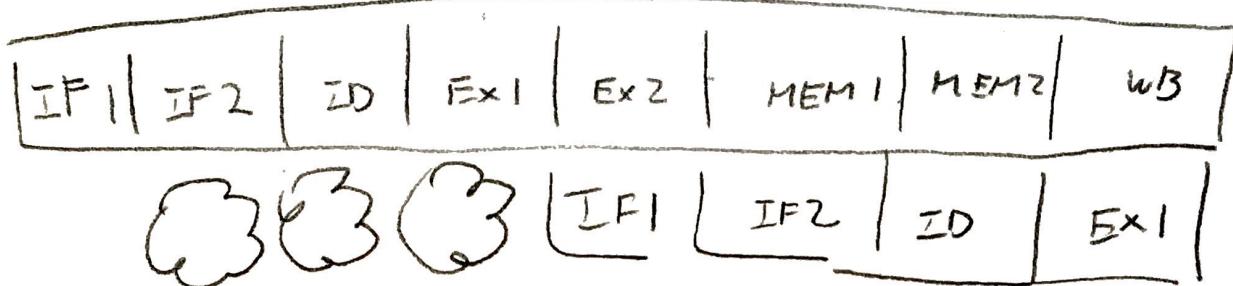
|w ~~\$t2~~, O(\$t1)

C

ΣF_D	F_M	w_B
ΣF	ΣD	ΣM

ΣR_D	ΣF_x	M	w_B
ΣD	ΣF_x	M	w_B

Right



% of loads	Cost (cycles)	Relative	IF
30%	3		
20%	2		
20%	1		
10%	0		
10%	0		
5%	0		
5%	0		

$$\begin{aligned}
 BCPI &= 1 + \left(\frac{0.9}{0.25} \cdot \frac{1}{8} \right) \cdot 4 + 0.25 \left(0.3 \cdot 3 + 0.2 \cdot 2 + 0.2 \cdot 1 \right) \\
 &= 1 + 0.2 + 0.25 \cdot \frac{15}{0.25} \\
 &= 1 + 0.2 + \frac{0.375}{0.0375} \\
 &= 1.2375
 \end{aligned}$$

$\frac{0.25}{0.125}$
 $\frac{125}{25}$
 0.0375

$$\begin{aligned}
 T_CPI &= 1.2375 + \frac{0.9}{2.1375} = 2.1375
 \end{aligned}$$

Need to double memory access time
 unit was cycles

$$ET = IC \cdot TCPD \cdot CT$$

$$= 1 \cdot 10^9 \cdot 2.1375 \cdot 100 \cdot 10^{-12}$$

$$= 2.1375 \cdot 100 \cdot 10^{-3}$$

$$= 0.21375 [s]$$