Gooch & Housego

# SPECIFICATIONS

Document

**Part Number: 97-04500-04 Revision A**

10/20/17

**MODEL NUMBER: R64093-127-10ADMDFS-A-F04**

Control

Firmware: **47-04000-04**

**A Digital Frequency Synthesizer in a OEM Module with analog and digital modulation input and having up to a 15 watt RF output.**

| PARAMETER | SPECIFICATION |
|---|---|
| Total Bandwidth: | 93-127 MHz |
| 20MHz Segment Bandwidth: | 93-113 MHz<br>100-120MHz<br>107-127 MHz |
| Clock Frequency: | 1000 MHz |
| Step Size: | ≤ 1 Hz with 30 Bits input |
| Frequency Settling Time: | 310 ns maximum |
| Nominal Power Out: | 10 Watts ± 10% over segment bandwidth |
| Maximum Power Out: | 15 Watts ±10% over segment bandwidth |
| Harmonic Distortion: 2nd:<br>3rd: | -15 dBc maximum<br>-15 dBc maximum |
| Analog Modulation: | 0 to +1 Volt Analog into 50 Ω, +1Volt = Full RF power output. |
| Digital Modulation: | TTL levels<br>TTL High = Full RF output power<br>TTL Low = Minimum RF output power<br>No Signal = Full RF output power (pulled high internally) |
| Rise and Fall Time: | 20 ns |
| Extinction Ratio:<br>Digital:<br>Analog: | <br>30 dB minimum<br>40 dB minimum |
| Reference Out: | A reference signal from the un-modulated output of the synthesizer. 0 dBm nominal |
| Applied Power: | +28 Volts DC @ 2 Amp maximum<br>+3.3 Volts DC @ 1 Amp maximum |
| Outline Drawing | 97-04500-04-15 |
| **MAXIMUM RATINGS**: | |
| Ambient Temperature: | $45^0$ C |
| RF Output: | No DC Feedback |
| **INPUT / OUTPUT CONNECTIONS:** | |
| "FREQUENCY SELECT" Control | TTL 30 bit binary word, Digital Modulation Input, Reset, and a Latch control input through the 37 pin D sub connector.<br>See page 2 for pinout. |
| +28V, +3.3V, and Gnd | Filtered Feedthrough |
| Mod In Analog | SMC Male |
| Reference Out | SMC Male |
| RF Output | SMA Female |

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"FREQUENCY SELECT" PIN OUT

37-PIN MALE D-SUB CONNECTOR

| PIN | | | PIN | |
|---|---|---|---|---|
| 1 | $FS_0$ | LSB | 20 | $FS_1$ |
| 2 | $FS_2$ | | 21 | $FS_3$ |
| 3 | $FS_4$ | | 22 | $FS_5$ |
| 4 | $FS_6$ | | 23 | $FS_7$ |
| 5 | $FS_8$ | | 24 | $FS_9$ |
| 6 | $FS_{10}$ | | 25 | $FS_{11}$ |
| 7 | $FS_{12}$ | | 26 | $FS_{13}$ |
| 8 | $FS_{14}$ | | 27 | $FS_{15}$ |
| 9 | $FS_{16}$ | | 28 | $FS_{17}$ |
| 10 | $FS_{18}$ | | 29 | $FS_{19}$ |
| 11 | $FS_{20}$ | | 30 | $FS_{21}$ |
| 12 | $FS_{22}$ | | 31 | $FS_{23}$ |
| 13 | $FS_{24}$ | | 32 | $FS_{25}$ |
| 14 | $FS_{26}$ | | 33 | $FS_{27}$ |
| 15 | $FS_{28}$ | | 34 | $FS_{29}$ MSB |
| 16 | Latch | | 35 | Digital Modulation Input (Active High) |
| 17 | Master Reset (Active High) | | 36 | Delta Frequency Latch |
| 18 | N/C | | 37 | N/C |
| 19 | Ground | | | |

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## CONTROL WORD CALCULATIONS

The output frequency and step size is a function of the clock rate and the FREQUENCY SELECT (FS) data. The output frequency can be calculated from the formula:

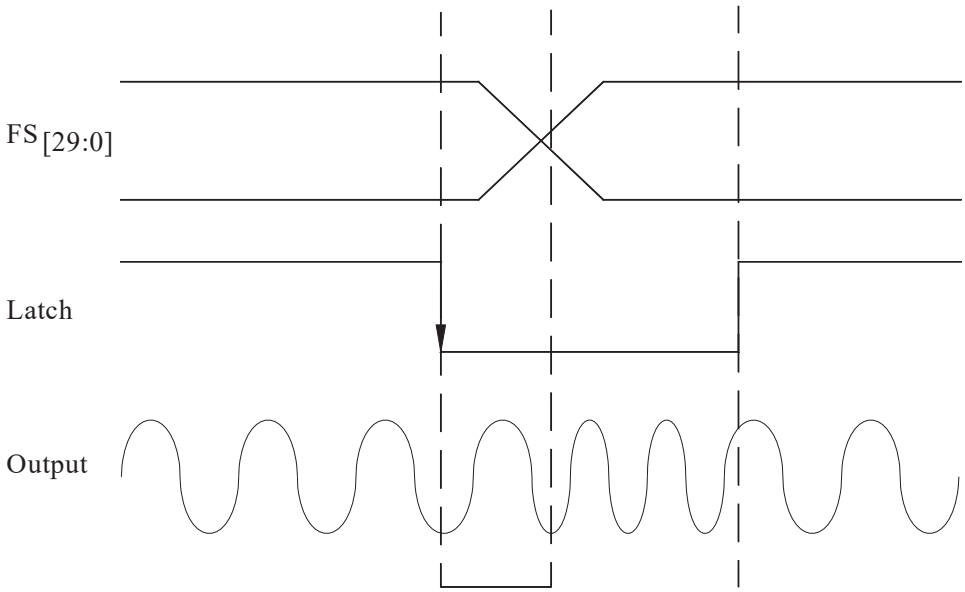
$$FS_{[29:0]} = \frac{F_{OUT}\,(2^{31})}{1000\,\text{MHz}}$$ Where Fout is output frequency in MHz

The LATCH function (pin 16) is a TTL compatible input which is used to load new frequency information into the driver. Frequency data is loaded into the driver when the signal on the LATCH pin goes from HIGH to LOW (falling edge).

The DELTA FREQUENCY LATCH function (pin 36) is a TTL compatible input which is used to load new data frequency information into the driver. For Delta frequency word, the same calculation is used as the output frequency with negative values being entered in twos compliment data is loaded on the falling edge.

Master RESET is a TTL active HIGH and resets the accumulator to zero, ie, no frequency output, when a TTL HIGH is applied to pin 17. This is pulled LOW via. a 1 KΩ resistor.

To generate a single frequency, apply the binary frequency word to the FS input,
A falling edge on the LATCH input will then load the data and change the frequency.




To generate a ferquency chirp, set the starting frequency as above and then apply the delta word to the FS input. A falling edge on DLATCH will then load the delta frequency word and initiate the chrip. The chirp will stop and output will return to to starting value or a rising edge.