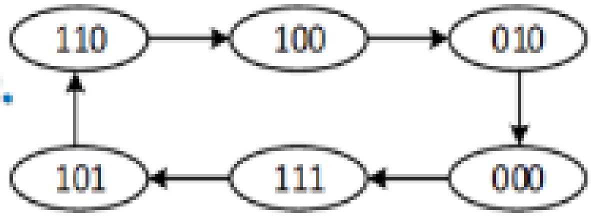
PROIECT

CIRCUITE INTEGRALE DIGITALE

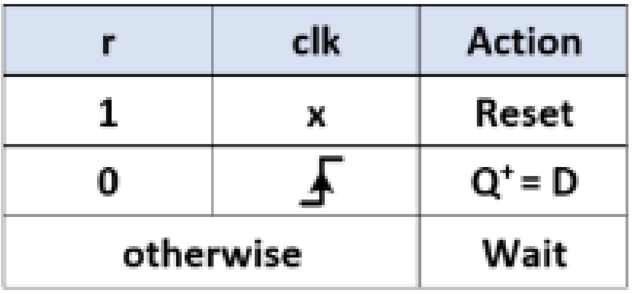
Automatul de tranzitie

19.



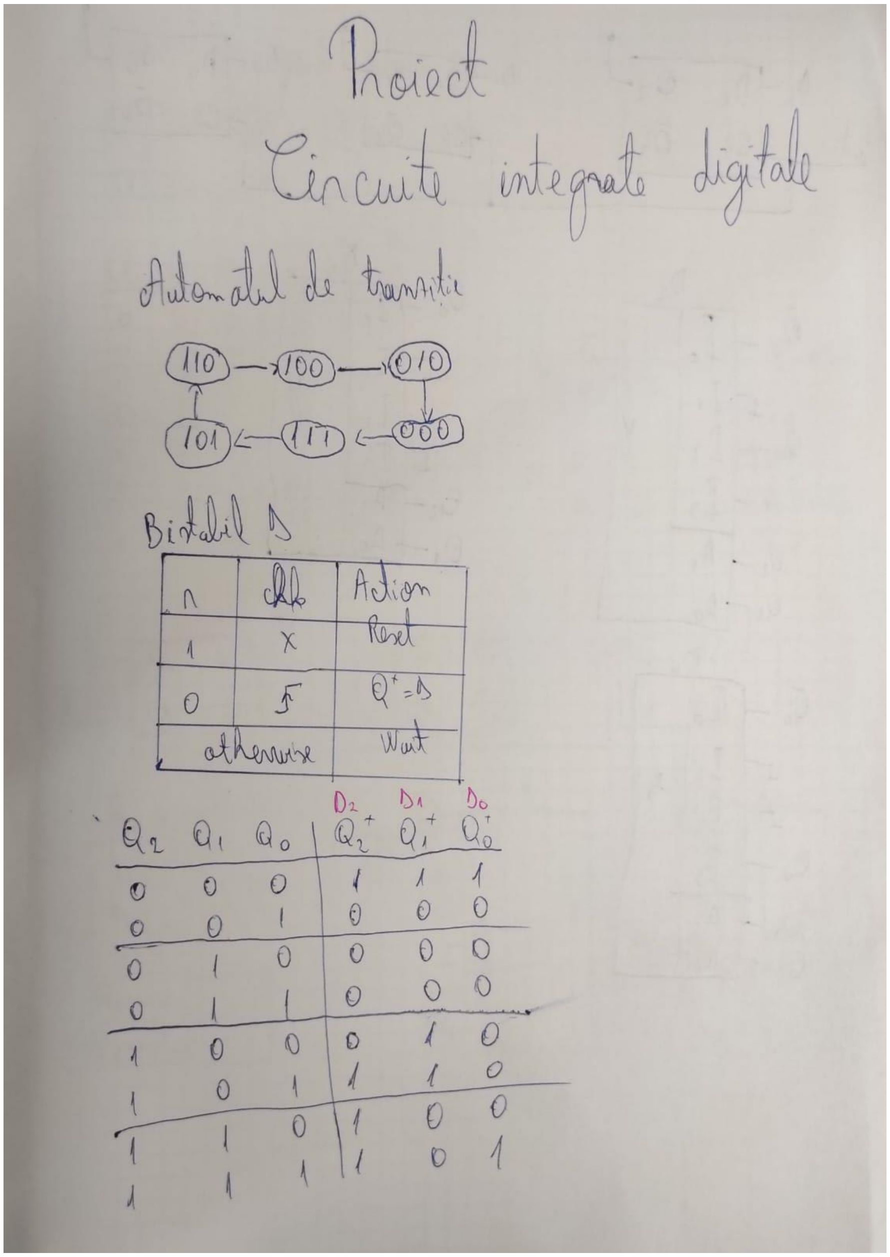
Bistabil D

A.



r	clk	Action
1	x	Reset
0	↑	$Q^+ = D$
otherwise		Wait

Rezolvarea proiectului pe hartie



Proiect

Circuite integrate digitale

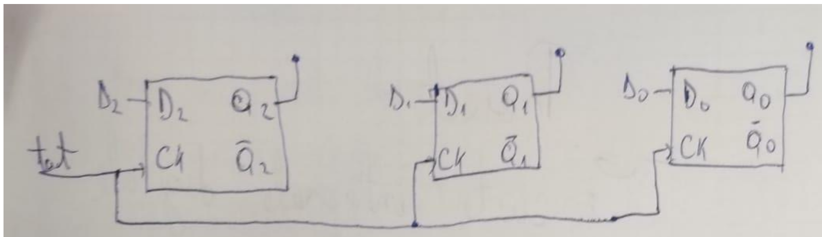
Automatul de tranzitie

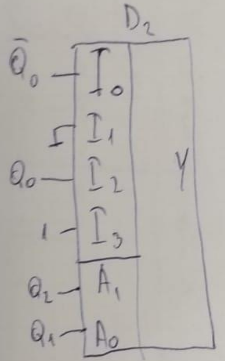
110
100
010
000
111
101

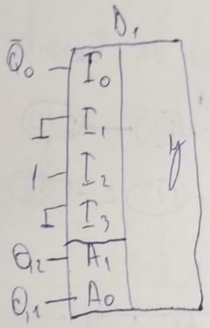
Bistabil D

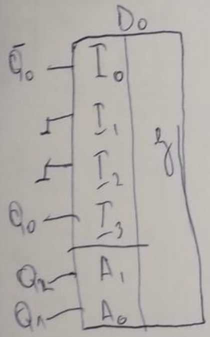
n	Clk	Action
1	X	Reset
0	↑	$Q^+ = D$
otherwise		Wait

			D_2	D_1	D_0
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1
1	1				

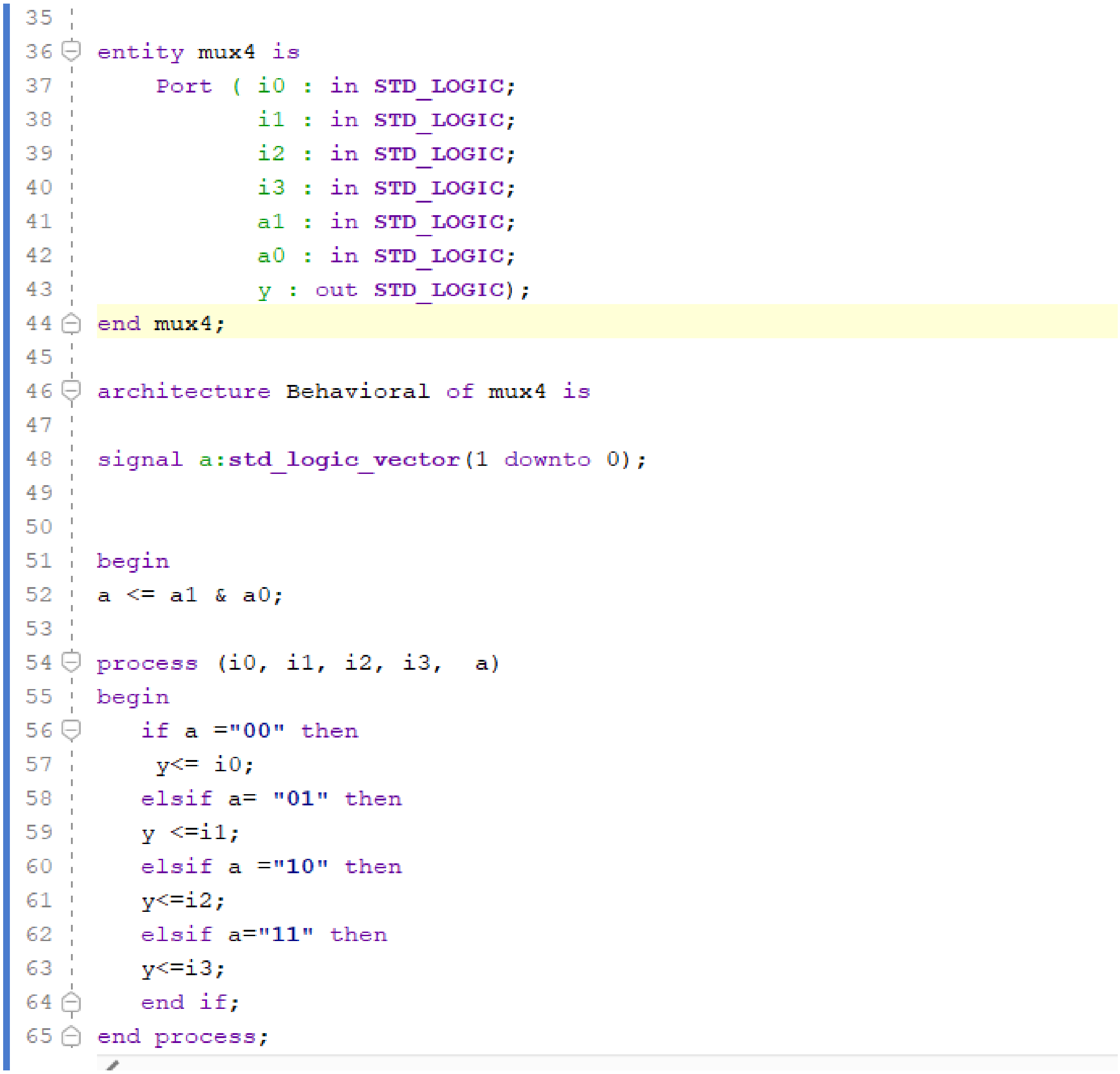

D2
D2
Q2
Ck
$\bar{Q}_2$
tact
D1
D1
Q1
Ck
$\bar{Q}_1$
D0
D0
Q0
CK
$\bar{Q}_0$


D2
$\bar{Q}_0$
I0
I1
Q0
I2
1
I3
Q2
A1
Q1
A0
Y


D1
$\bar{Q}_0$
I0
I1
1
I2
I3
Q2
A1
Q1
A0
y

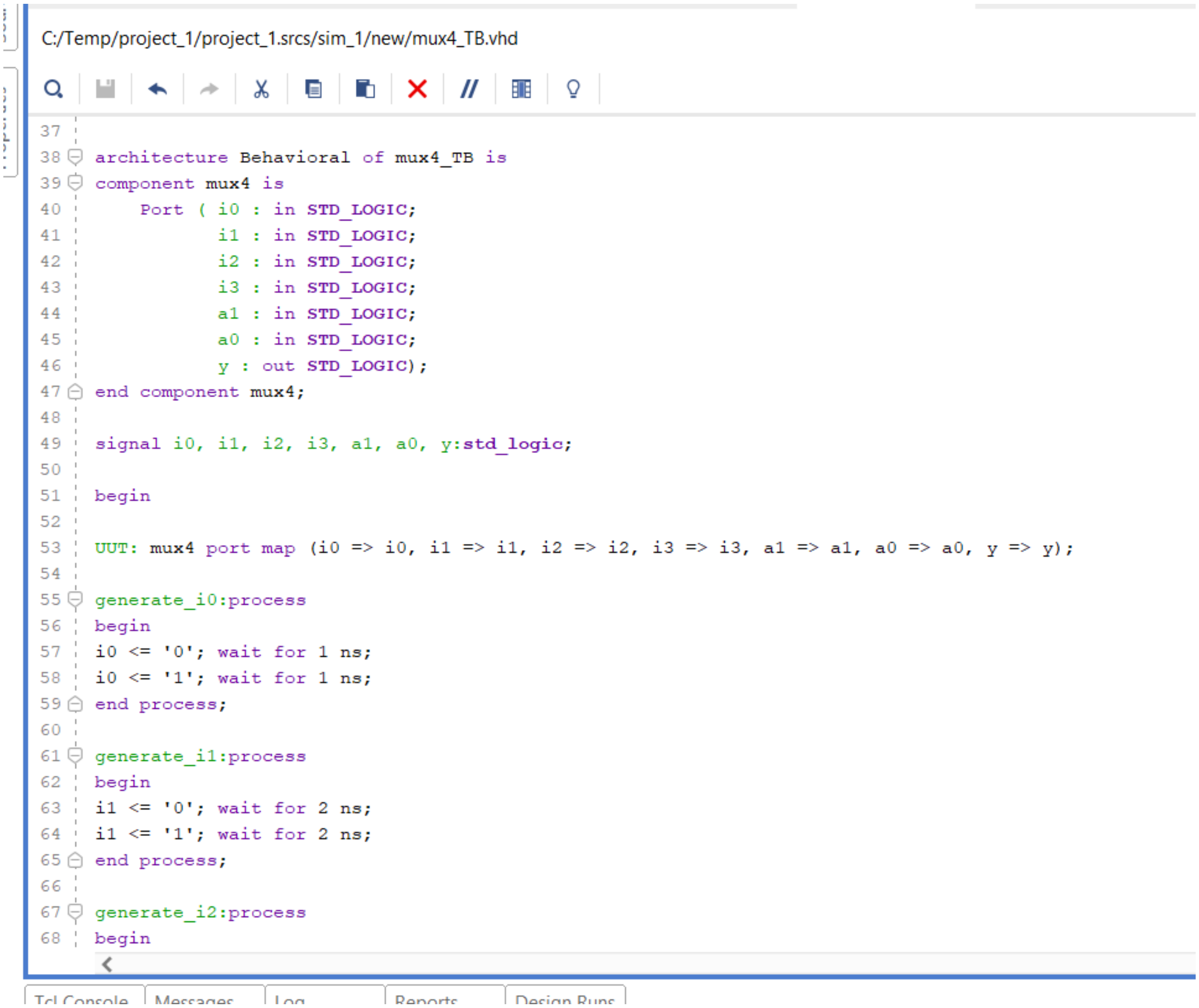

D0
$\bar{Q}_0$
I0
I1
I2
Q0
I3
Q2
A1
Q1
A0
y

Sursa de design pentru MUX4:1



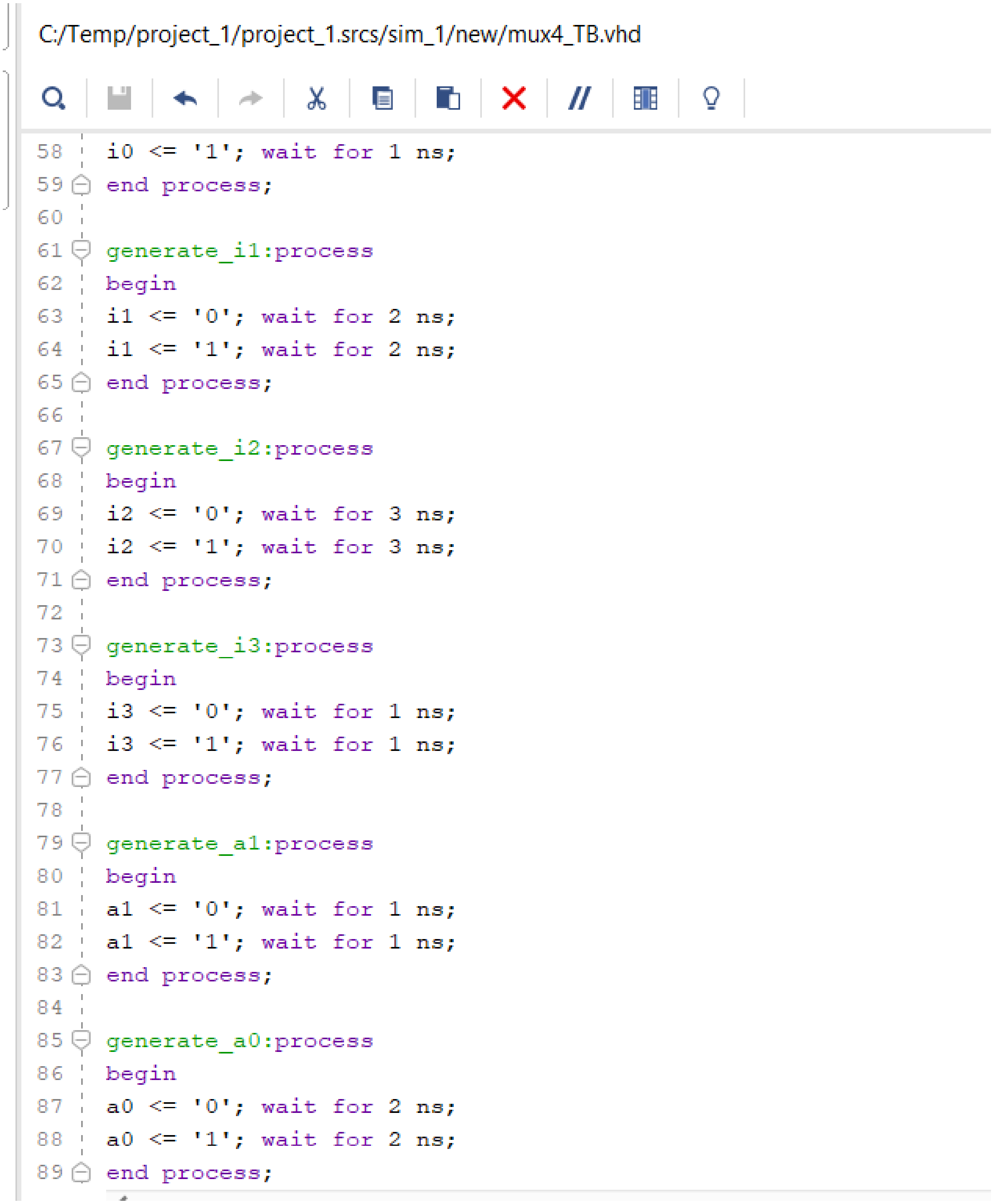
```

entity mux4 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           i2 : in STD_LOGIC;
           i3 : in STD_LOGIC;
           a1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end mux4;

architecture Behavioral of mux4 is

signal a:std_logic_vector(1 downto 0);


begin
a <= a1 & a0;

process (i0, i1, i2, i3,  a)
begin
   if a ="00" then
    y<= i0;
   elsif a= "01" then
   y <=i1;
   elsif a ="10" then
   y<=i2;
   elsif a="11" then
   y<=i3;
   end if;
end process;
```

Sursa de simulare MUX4:1



C:/Temp/project_1/project_1.srcs/sim_1/new/mux4_TB.vhd

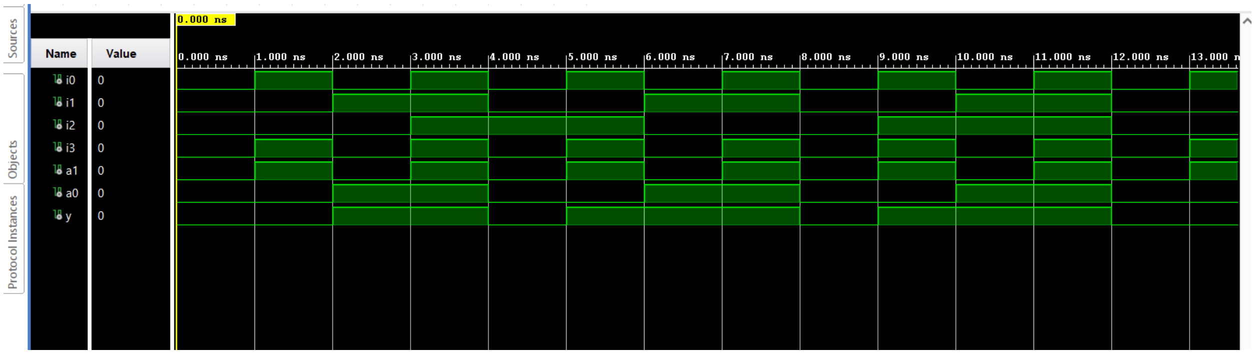
```vhdl

architecture Behavioral of mux4_TB is
component mux4 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           i2 : in STD_LOGIC;
           i3 : in STD_LOGIC;
           a1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux4;

signal i0, i1, i2, i3, a1, a0, y:std_logic;

begin

UUT: mux4 port map (i0 => i0, i1 => i1, i2 => i2, i3 => i3, a1 => a1, a0 => a0, y => y);

generate_i0:process
begin
i0 <= '0'; wait for 1 ns;
i0 <= '1'; wait for 1 ns;
end process;

generate_i1:process
begin
i1 <= '0'; wait for 2 ns;
i1 <= '1'; wait for 2 ns;
end process;

generate_i2:process
begin
```



C:/Temp/project_1/project_1.srcs/sim_1/new/mux4_TB.vhd

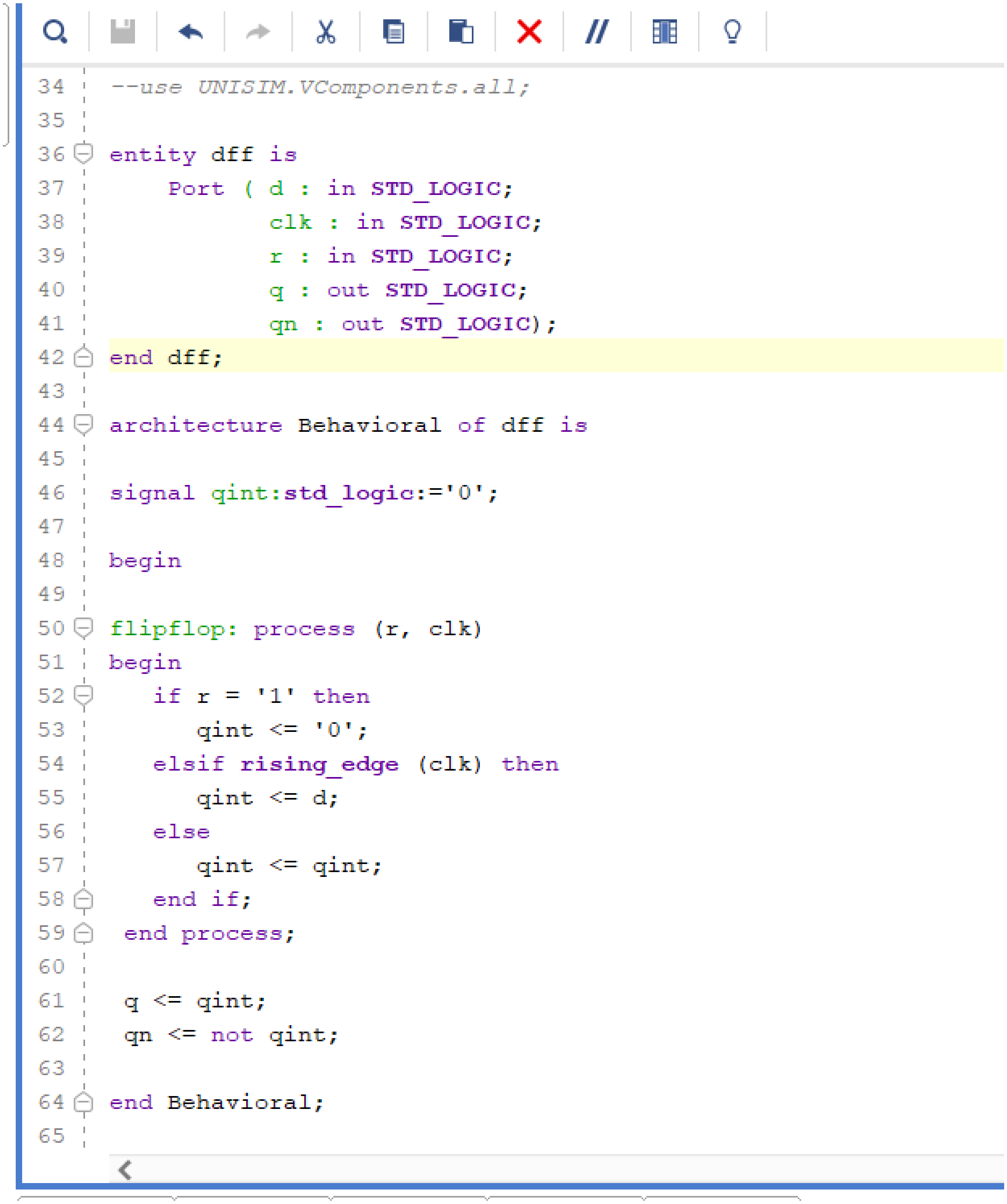
```vhdl
i0 <= '1'; wait for 1 ns;
end process;

generate_i1:process
begin
i1 <= '0'; wait for 2 ns;
i1 <= '1'; wait for 2 ns;
end process;

generate_i2:process
begin
i2 <= '0'; wait for 3 ns;
i2 <= '1'; wait for 3 ns;
end process;

generate_i3:process
begin
i3 <= '0'; wait for 1 ns;
i3 <= '1'; wait for 1 ns;
end process;

generate_a1:process
begin
a1 <= '0'; wait for 1 ns;
a1 <= '1'; wait for 1 ns;
end process;

generate_a0:process
begin
a0 <= '0'; wait for 2 ns;
a0 <= '1'; wait for 2 ns;
end process;
```

Simulare MUX4:1



Name	Value
i0	0
i1	0
i2	0
i3	0
a1	0
a0	0
y	0

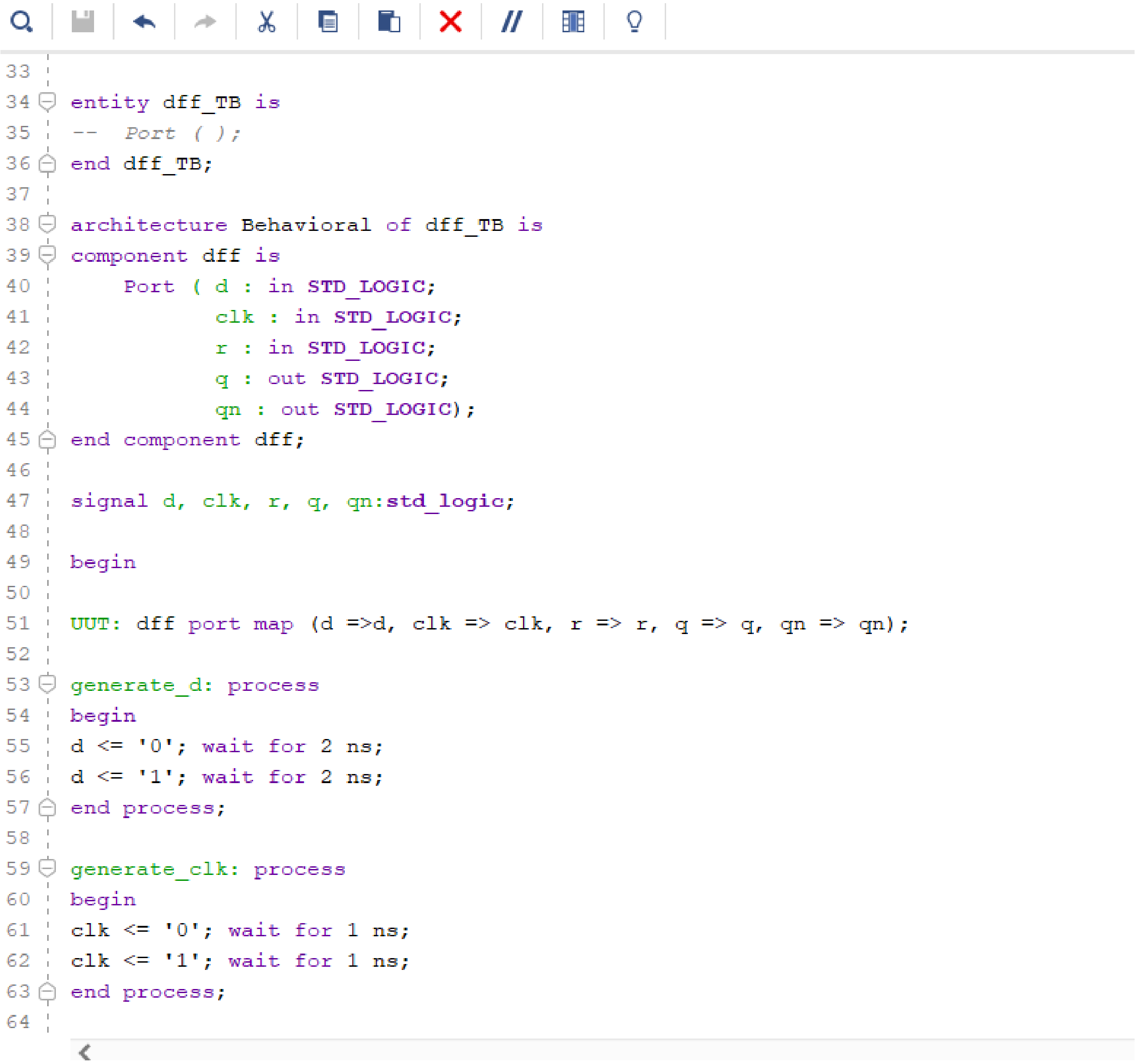
Sursa de design bistabil



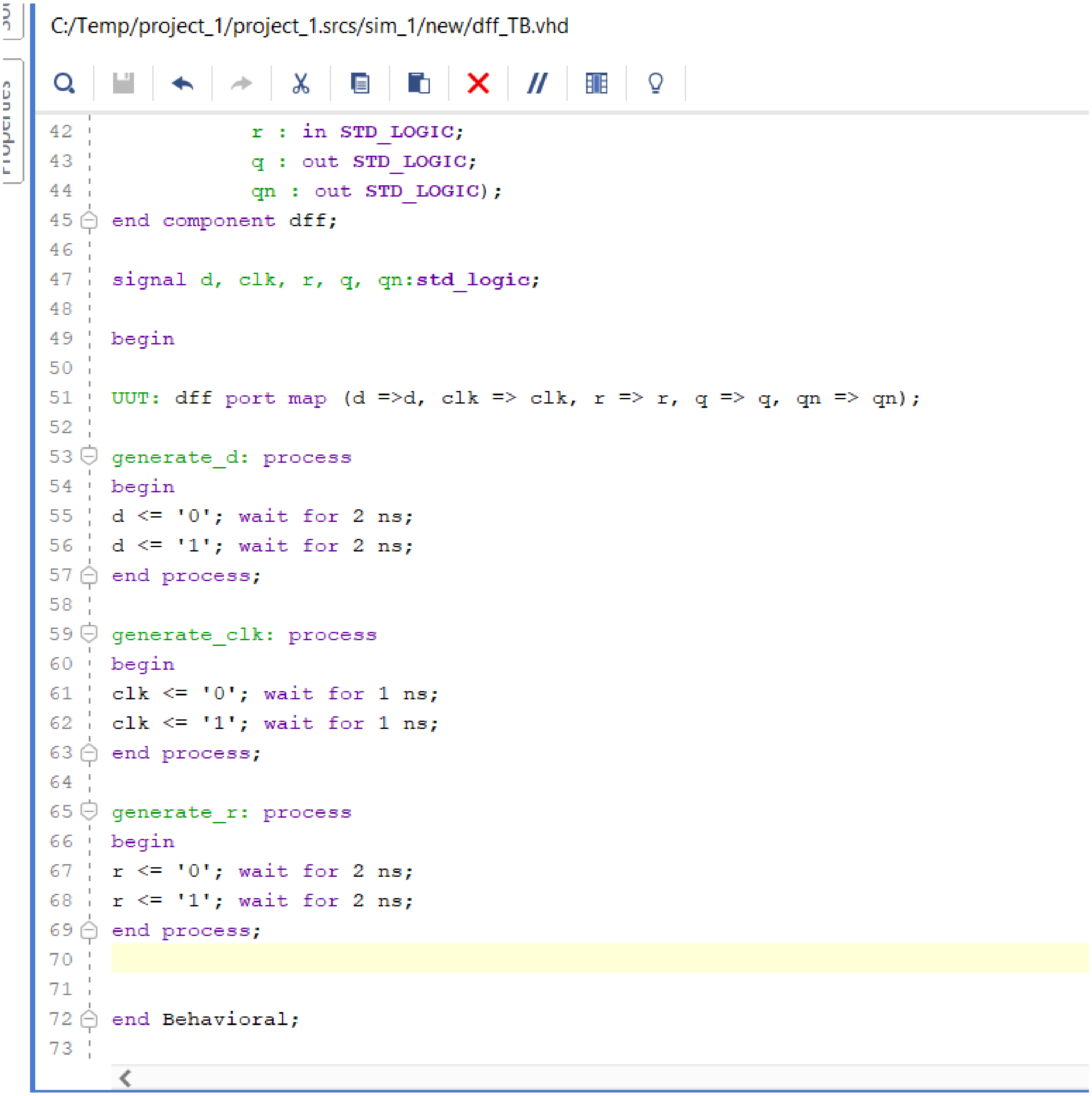
```vhdl
--use UNISIM.VComponents.all;

entity dff is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end dff;

architecture Behavioral of dff is

signal qint:std_logic:='0';

begin

flipflop: process (r, clk)
begin
   if r = '1' then
      qint <= '0';
   elsif rising_edge (clk) then
      qint <= d;
   else
      qint <= qint;
   end if;
 end process;

 q <= qint;
 qn <= not qint;

end Behavioral;
```

Sursa de simulare Bistabil

C:/Temp/project_1/project_1.srcs/sim_1/new/dff_TB.vhd



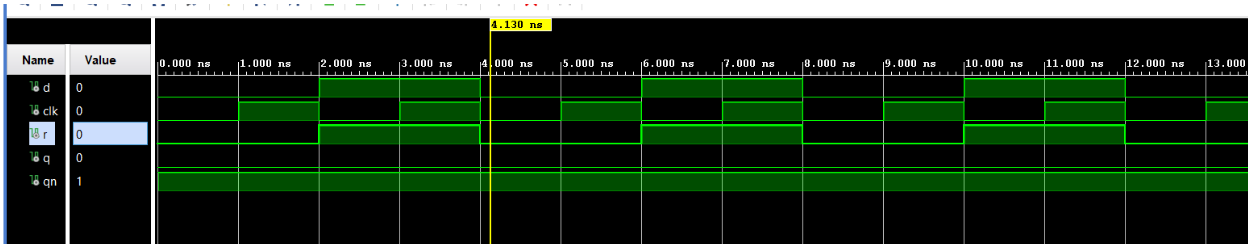
```
entity dff_TB is
--  Port ( );
end dff_TB;

architecture Behavioral of dff_TB is
component dff is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component dff;

signal d, clk, r, q, qn:std_logic;

begin

UUT: dff port map (d =>d, clk => clk, r => r, q => q, qn => qn);

generate_d: process
begin
d <= '0'; wait for 2 ns;
d <= '1'; wait for 2 ns;
end process;

generate_clk: process
begin
clk <= '0'; wait for 1 ns;
clk <= '1'; wait for 1 ns;
end process;

```



C:/Temp/project_1/project_1.srcs/sim_1/new/dff_TB.vhd

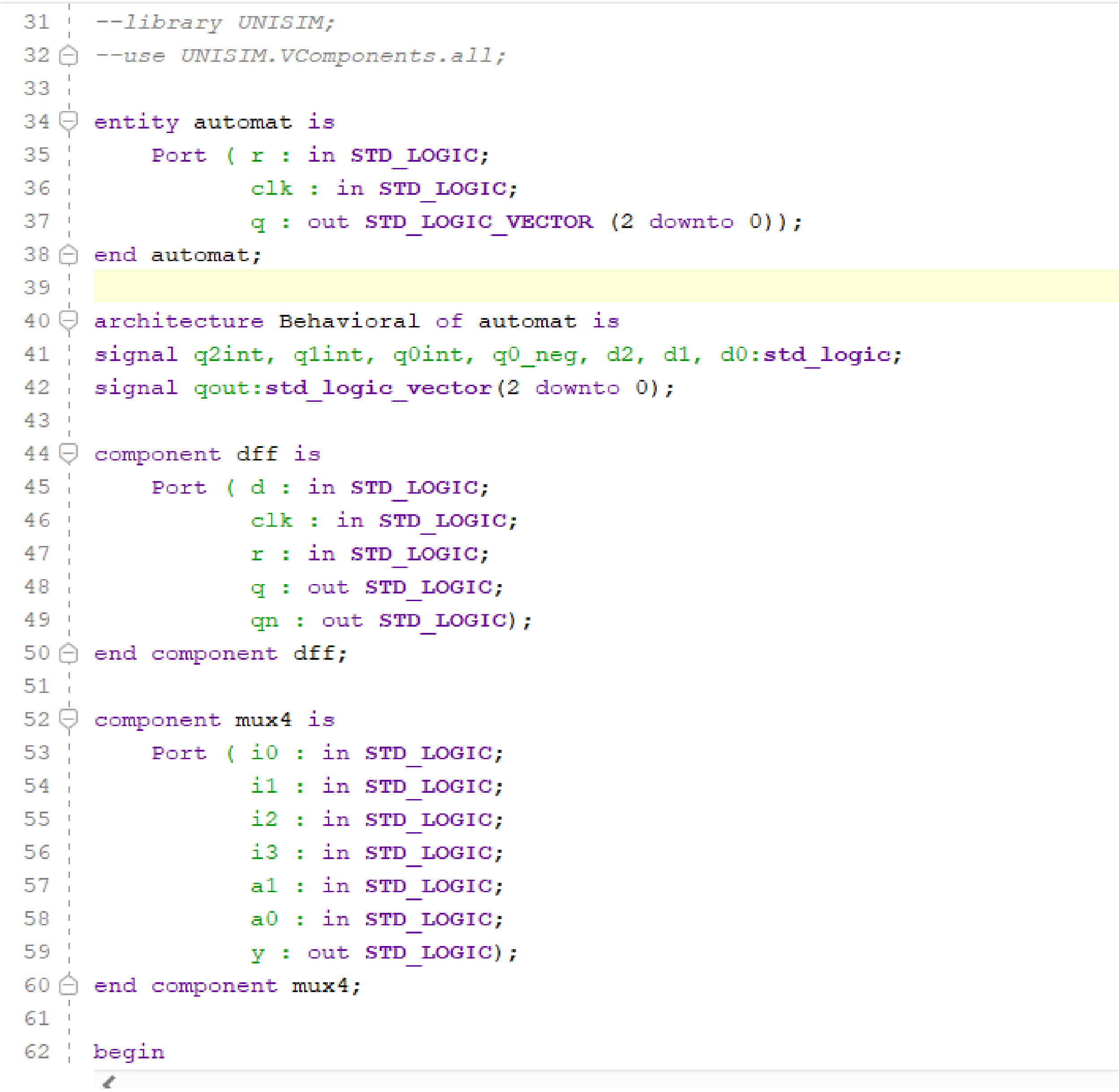
```vhdl
            r : in STD_LOGIC;
            q : out STD_LOGIC;
            qn : out STD_LOGIC);
end component dff;

signal d, clk, r, q, qn:std_logic;

begin

UUT: dff port map (d =>d, clk => clk, r => r, q => q, qn => qn);

generate_d: process
begin
d <= '0'; wait for 2 ns;
d <= '1'; wait for 2 ns;
end process;

generate_clk: process
begin
clk <= '0'; wait for 1 ns;
clk <= '1'; wait for 1 ns;
end process;

generate_r: process
begin
r <= '0'; wait for 2 ns;
r <= '1'; wait for 2 ns;
end process;


end Behavioral;
```

Simulare Bistabil

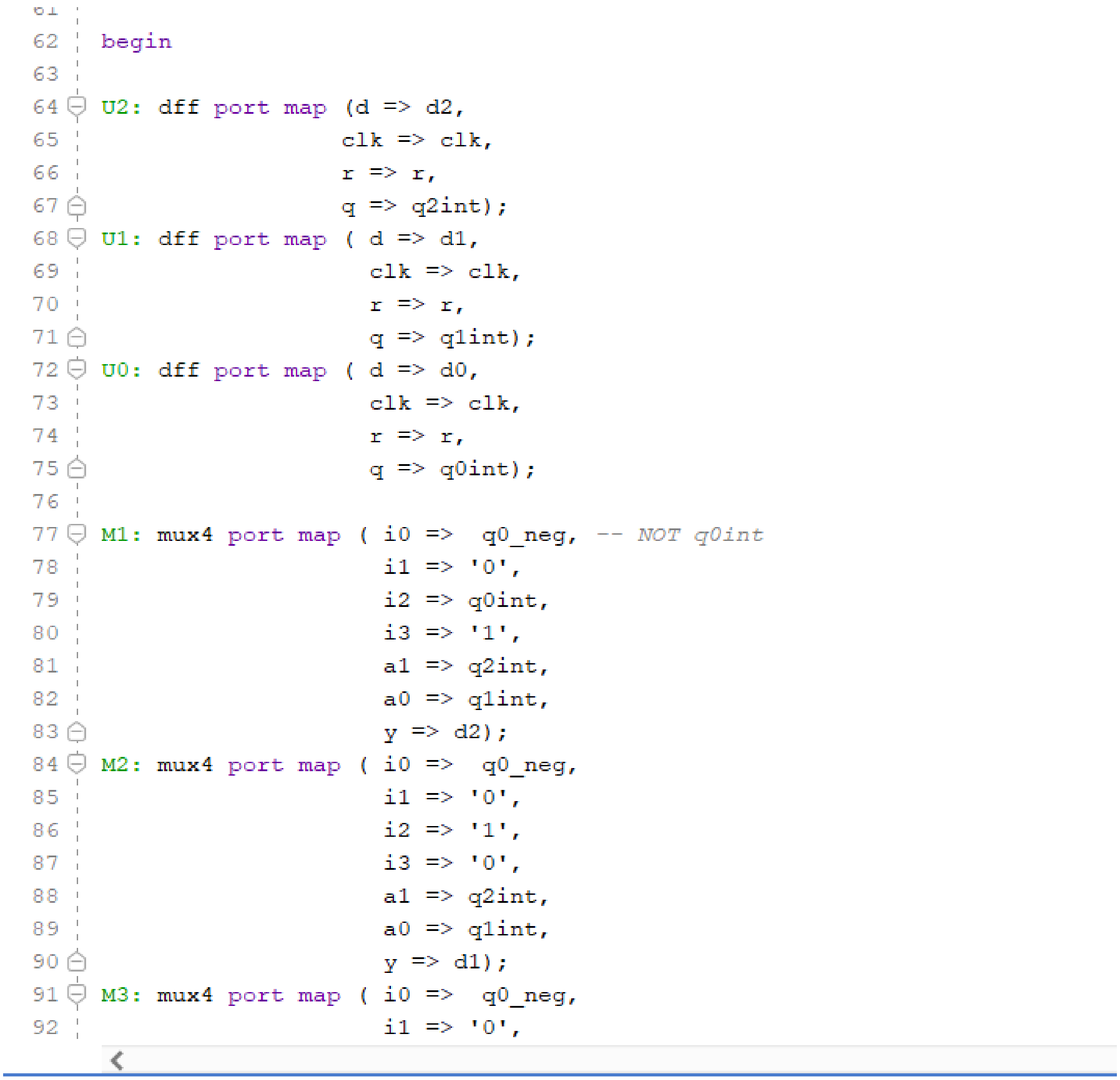


Name	Value
d	0
clk	0
r	0
q	0
qn	1

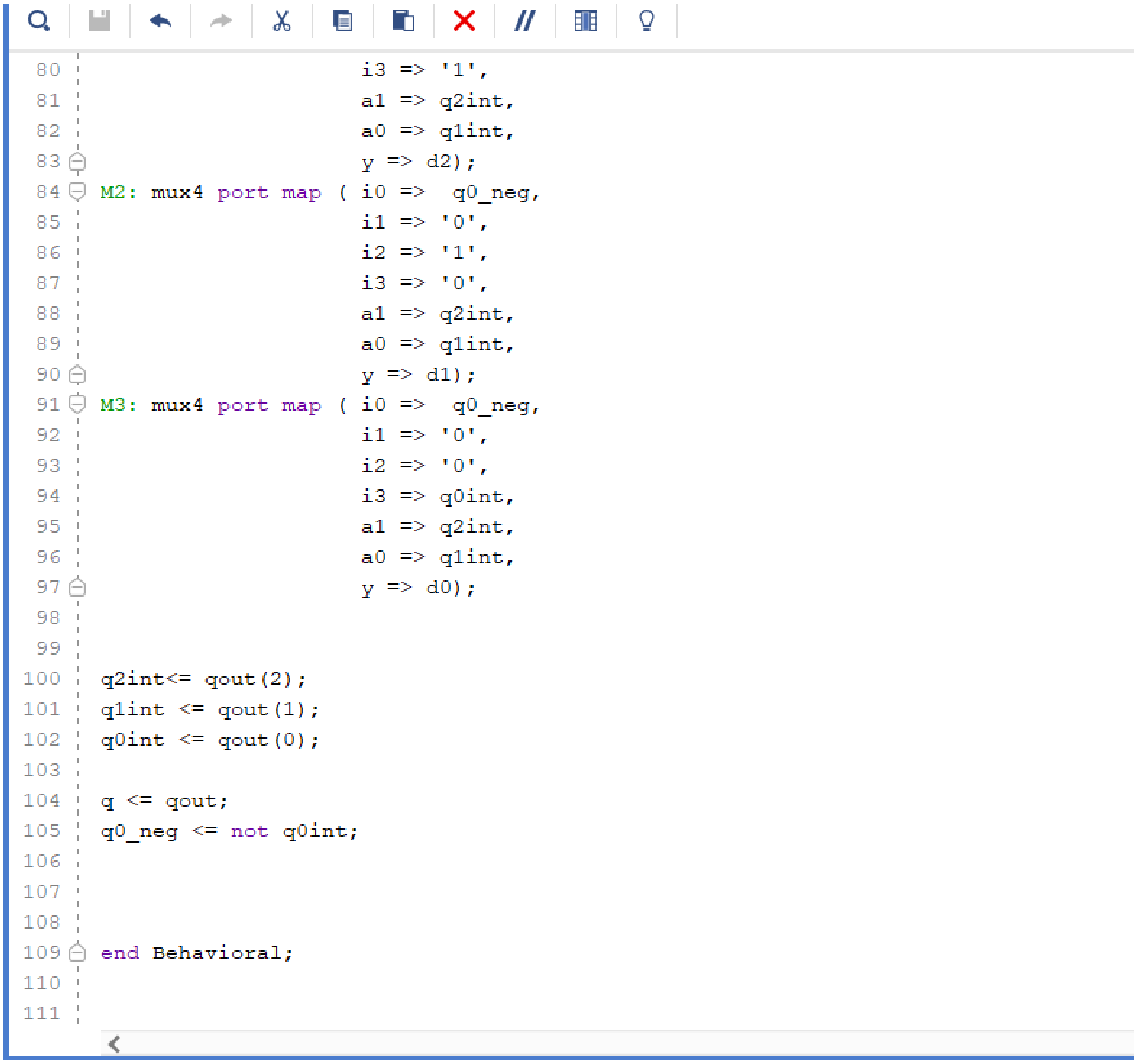
Sursa de design automat



```vhdl
--library UNISIM;
--use UNISIM.VComponents.all;

entity automat is
    Port ( r : in STD_LOGIC;
           clk : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (2 downto 0));
end automat;

architecture Behavioral of automat is
signal q2int, q1int, q0int, q0_neg, d2, d1, d0:std_logic;
signal qout:std_logic_vector(2 downto 0);

component dff is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component dff;

component mux4 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           i2 : in STD_LOGIC;
           i3 : in STD_LOGIC;
           a1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux4;

begin
```

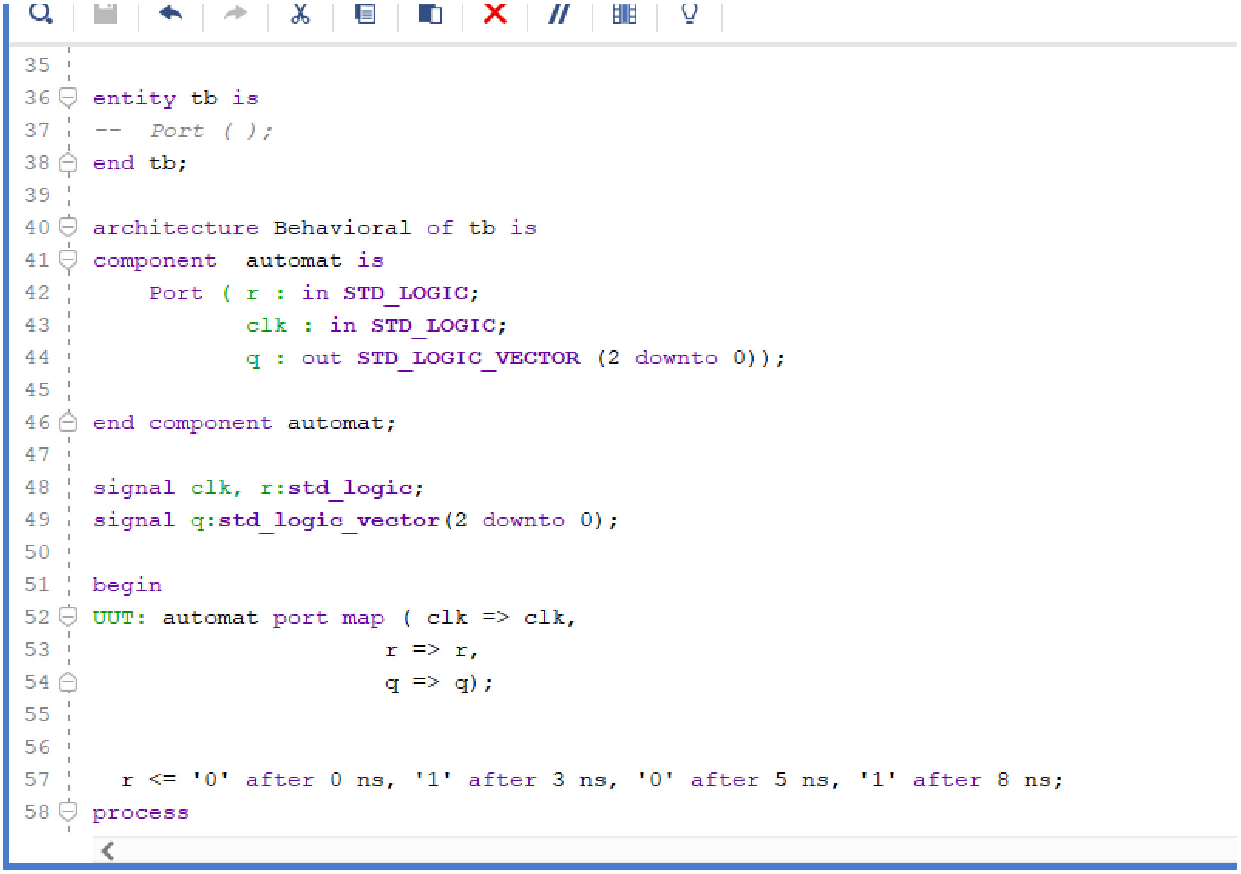


```
begin

U2: dff port map (d => d2,
                 clk => clk,
                 r => r,
                 q => q2int);
U1: dff port map ( d => d1,
                   clk => clk,
                   r => r,
                   q => q1int);
U0: dff port map ( d => d0,
                   clk => clk,
                   r => r,
                   q => q0int);

M1: mux4 port map ( i0 =>  q0_neg, -- NOT q0int
                    i1 => '0',
                    i2 => q0int,
                    i3 => '1',
                    a1 => q2int,
                    a0 => q1int,
                    y => d2);
M2: mux4 port map ( i0 =>  q0_neg,
                    i1 => '0',
                    i2 => '1',
                    i3 => '0',
                    a1 => q2int,
                    a0 => q1int,
                    y => d1);
M3: mux4 port map ( i0 =>  q0_neg,
                    i1 => '0',
```

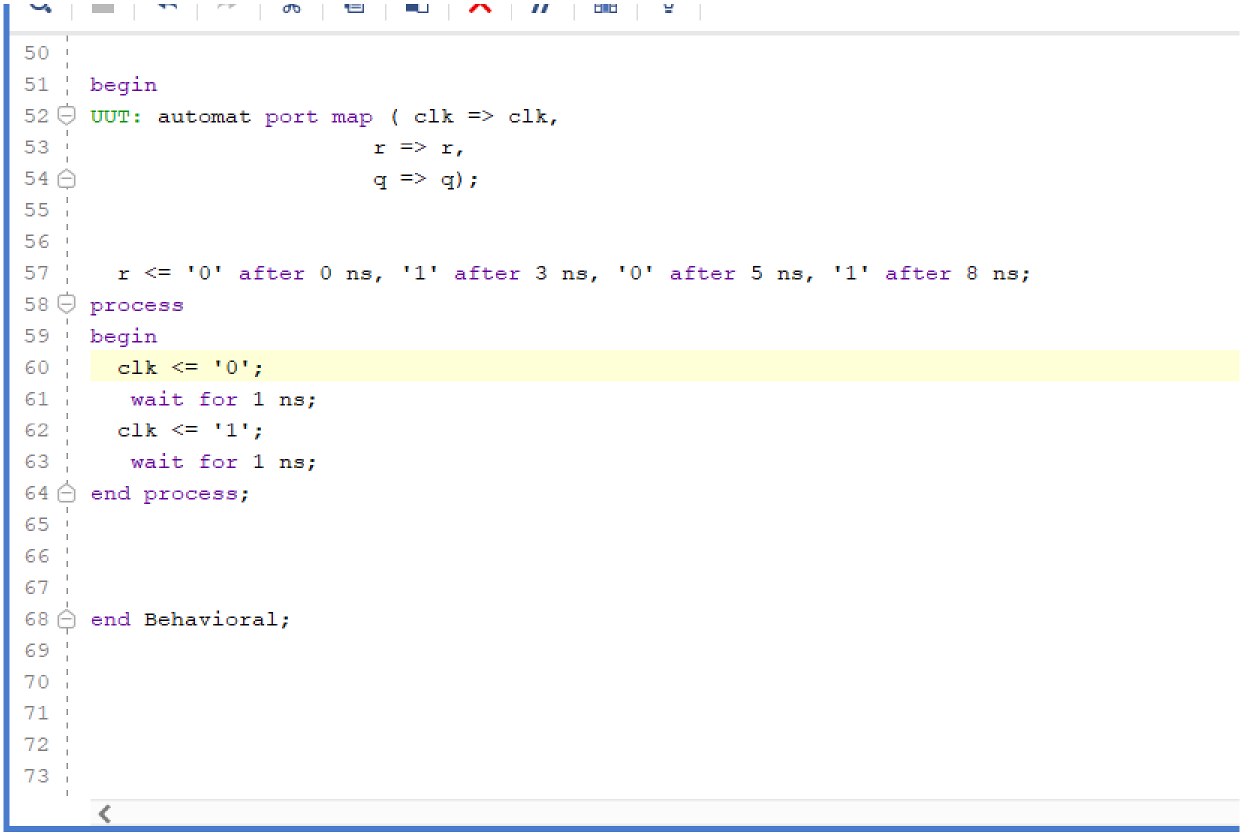


```
                    i3 => '1',
                    a1 => q2int,
                    a0 => q1int,
                    y => d2);
M2: mux4 port map ( i0 =>  q0_neg,
                    i1 => '0',
                    i2 => '1',
                    i3 => '0',
                    a1 => q2int,
                    a0 => q1int,
                    y => d1);
M3: mux4 port map ( i0 =>  q0_neg,
                    i1 => '0',
                    i2 => '0',
                    i3 => q0int,
                    a1 => q2int,
                    a0 => q1int,
                    y => d0);


q2int<= qout(2);
q1int <= qout(1);
q0int <= qout(0);

q <= qout;
q0_neg <= not q0int;



end Behavioral;
```

Sursa de simulare automat

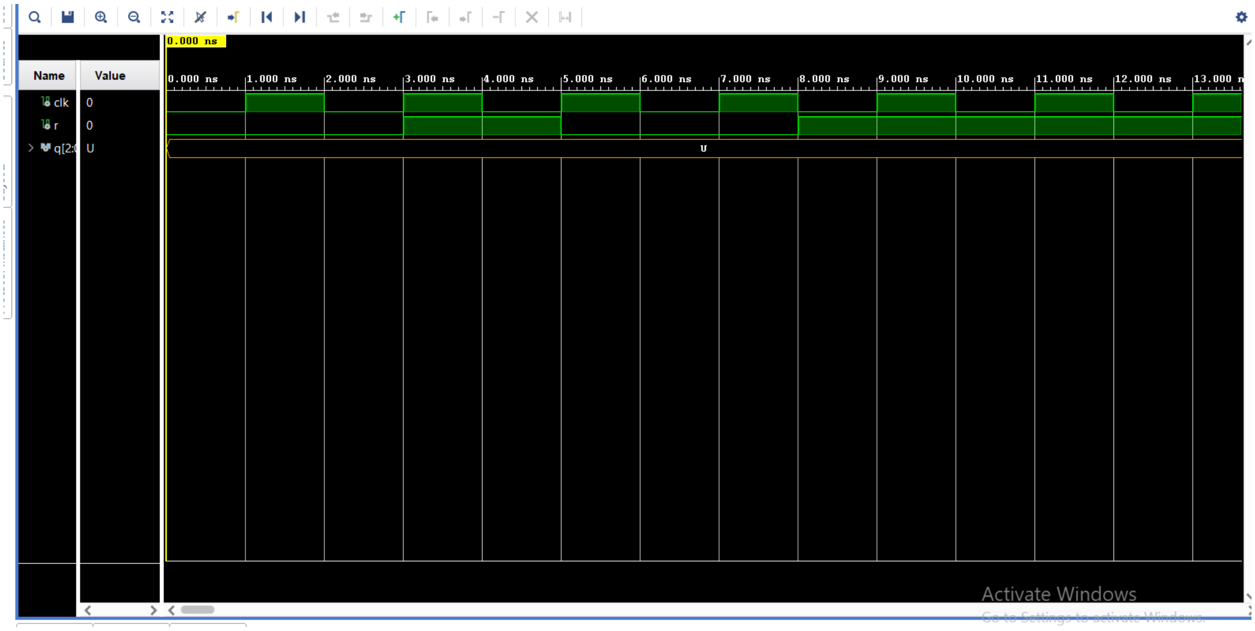


```
entity tb is
--  Port ( );
end tb;

architecture Behavioral of tb is
component  automat is
    Port ( r : in STD_LOGIC;
           clk : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (2 downto 0));

end component automat;

signal clk, r:std_logic;
signal q:std_logic_vector(2 downto 0);

begin
UUT: automat port map ( clk => clk,
                     r => r,
                     q => q);


  r <= '0' after 0 ns, '1' after 3 ns, '0' after 5 ns, '1' after 8 ns;
process
```



```
begin
UUT: automat port map ( clk => clk,
                     r => r,
                     q => q);


  r <= '0' after 0 ns, '1' after 3 ns, '0' after 5 ns, '1' after 8 ns;
process
begin
  clk <= '0';
   wait for 1 ns;
  clk <= '1';
   wait for 1 ns;
end process;



end Behavioral;
```

Simulare finala


0.000 ns
Name
Value
clk
0
r
0
q[2:0]
U
0.000 ns
1.000 ns
2.000 ns
3.000 ns
4.000 ns
5.000 ns
6.000 ns
7.000 ns
8.000 ns
9.000 ns
10.000 ns
11.000 ns
12.000 ns
13.000 ns
U
Activate Windows
Go to Settings to activate Windows.