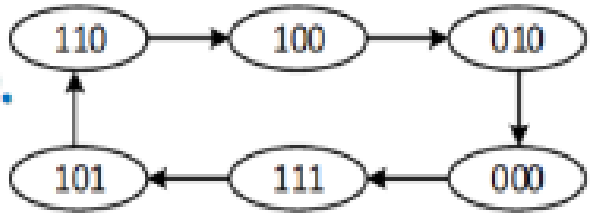
PROIECT

CIRCUITE INTEGRALE DIGITALE

Automatul de tranzitie

19.

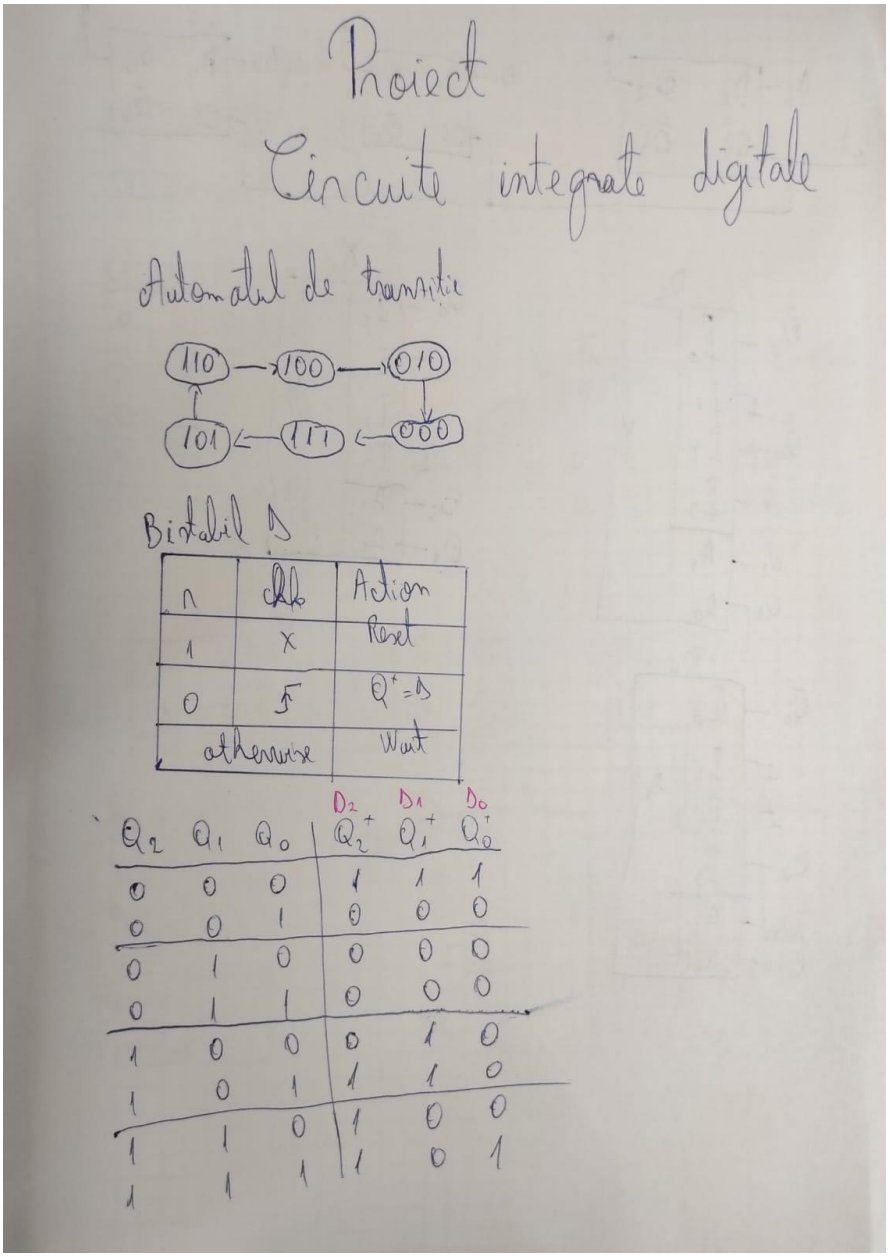


Bistabil D

A.

r	clk	Action
1	x	Reset
0	↑	$Q^+ = D$
otherwise		Wait

Rezolvarea proiectului pe hartie



Proiect

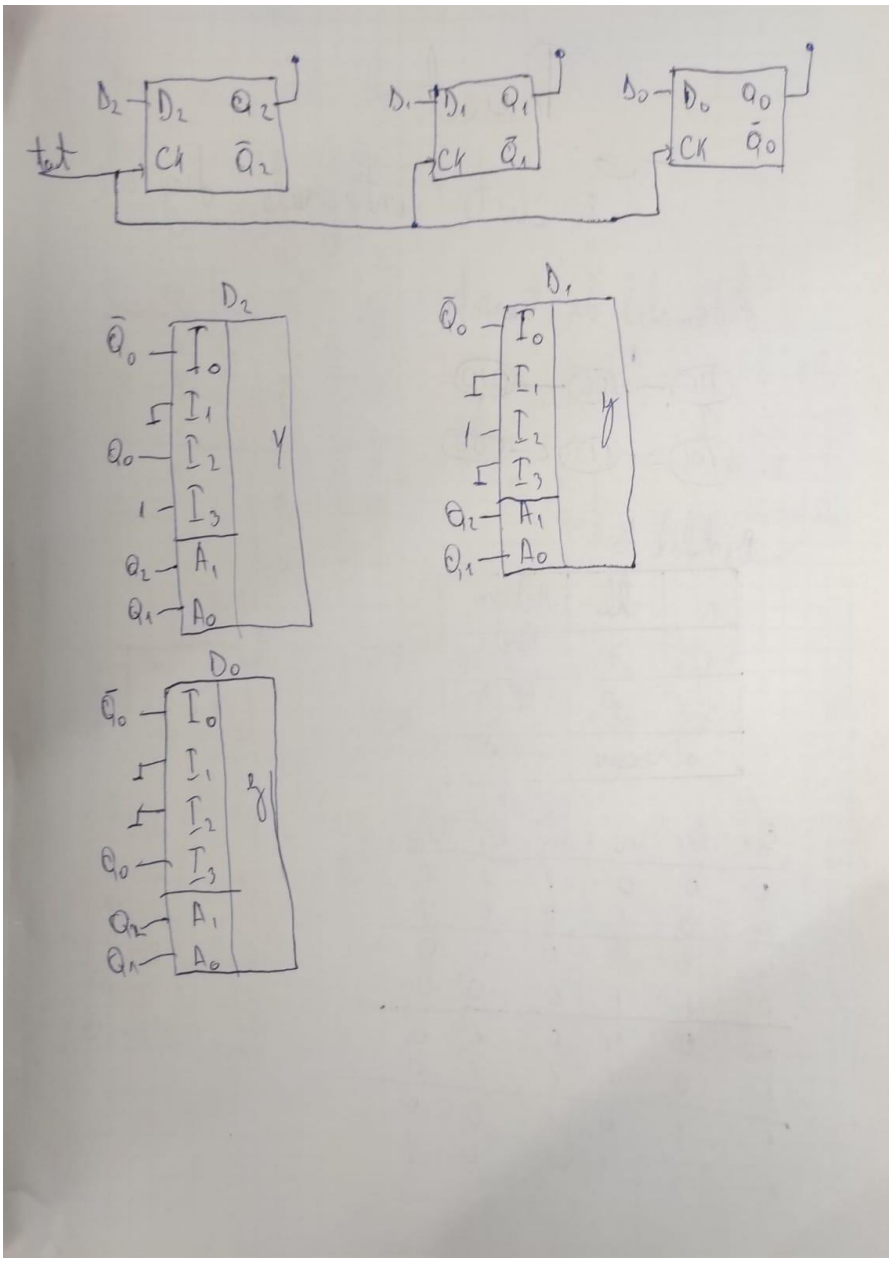
Circuite integrate digitale

Automatul de tranzitie

Bistabil D

R	clk	Action
1	X	Reset
0	↑	$Q^+ = D$
otherwise		Wait

Q_2	Q_1	Q_0	D_2 = Q_2^+	D_1 = Q_1^+	D_0 = Q_0^+
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1


D2
D2 Q2
CK Q̄2
D1
D1 Q1
CK Q̄1
D0
D0 Q0
CK Q̄0
D2
Q̄0
I0
I1
Q0
I2
1
I3
Y
Q2
A1
Q1
A0
D1
Q̄0
I0
I1
1
I2
I3
Y
Q2
A1
Q1
A0
D0
Q̄0
I0
I1
I2
Q0
I3
Y
Q2
A1
Q1
A0

Sursa de design pentru MUX4:1

```
35
36  entity mux4 is
37      Port ( i0 : in STD_LOGIC;
38             i1 : in STD_LOGIC;
39             i2 : in STD_LOGIC;
40             i3 : in STD_LOGIC;
41             a1 : in STD_LOGIC;
42             a0 : in STD_LOGIC;
43             y : out STD_LOGIC);
44  end mux4;
45
46  architecture Behavioral of mux4 is
47
48  signal a:std_logic_vector(1 downto 0);
49
50
51  begin
52  a <= a1 & a0;
53
54  process (i0, i1, i2, i3,  a)
55  begin
56     if a ="00" then
57      y<= i0;
58     elsif a= "01" then
59     y <=i1;
60     elsif a ="10" then
61     y<=i2;
62     elsif a="11" then
63     y<=i3;
64     end if;
65  end process;
```

Sursa de simulare MUX4:1

C:/Temp/project_1/project_1.srcs/sim_1/new/mux4_TB.vhd

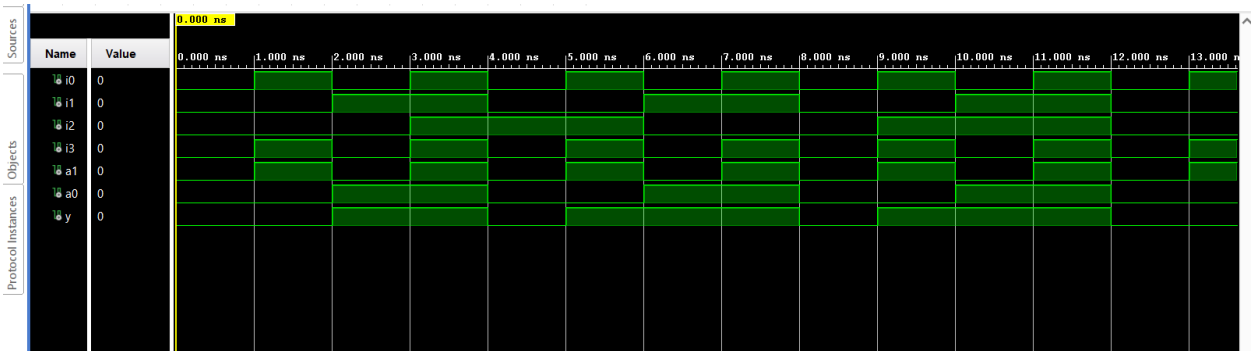
```
37
38  architecture Behavioral of mux4_TB is
39  component mux4 is
40      Port ( i0 : in STD_LOGIC;
41             i1 : in STD_LOGIC;
42             i2 : in STD_LOGIC;
43             i3 : in STD_LOGIC;
44             a1 : in STD_LOGIC;
45             a0 : in STD_LOGIC;
46             y : out STD_LOGIC);
47  end component mux4;
48
49  signal i0, i1, i2, i3, a1, a0, y:std_logic;
50
51  begin
52
53  UUT: mux4 port map (i0 => i0, i1 => i1, i2 => i2, i3 => i3, a1 => a1, a0 => a0, y => y);
54
55  generate_i0:process
56  begin
57  i0 <= '0'; wait for 1 ns;
58  i0 <= '1'; wait for 1 ns;
59  end process;
60
61  generate_i1:process
62  begin
63  i1 <= '0'; wait for 2 ns;
64  i1 <= '1'; wait for 2 ns;
65  end process;
66
67  generate_i2:process
68  begin
```

Tcl Console | Messages | Log | Reports | Design Runs

C:/Temp/project_1/project_1.srcs/sim_1/new/mux4_TB.vhd

```
58  i0 <= '1'; wait for 1 ns;
59  end process;
60
61  generate_i1:process
62  begin
63  i1 <= '0'; wait for 2 ns;
64  i1 <= '1'; wait for 2 ns;
65  end process;
66
67  generate_i2:process
68  begin
69  i2 <= '0'; wait for 3 ns;
70  i2 <= '1'; wait for 3 ns;
71  end process;
72
73  generate_i3:process
74  begin
75  i3 <= '0'; wait for 1 ns;
76  i3 <= '1'; wait for 1 ns;
77  end process;
78
79  generate_a1:process
80  begin
81  a1 <= '0'; wait for 1 ns;
82  a1 <= '1'; wait for 1 ns;
83  end process;
84
85  generate_a0:process
86  begin
87  a0 <= '0'; wait for 2 ns;
88  a0 <= '1'; wait for 2 ns;
89  end process;
```

Simulare MUX4:1



Sursa de design bistabil

```
34  --use UNISIM.VComponents.all;
35
36  entity dff is
37      Port ( d : in STD_LOGIC;
38             clk : in STD_LOGIC;
39             r : in STD_LOGIC;
40             q : out STD_LOGIC;
41             qn : out STD_LOGIC);
42  end dff;
43
44  architecture Behavioral of dff is
45
46  signal qint:std_logic:='0';
47
48  begin
49
50  flipflop: process (r, clk)
51  begin
52     if r = '1' then
53        qint <= '0';
54     elsif rising_edge (clk) then
55        qint <= d;
56     else
57        qint <= qint;
58     end if;
59   end process;
60
61   q <= qint;
62   qn <= not qint;
63
64  end Behavioral;
65
```

Sursa de simulare Bistabil

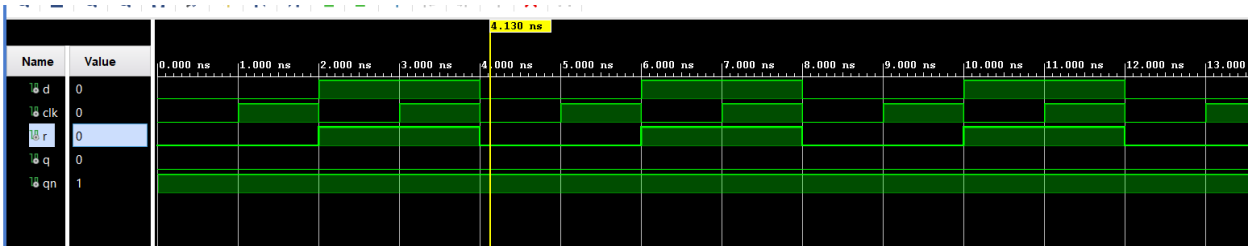
C:/Temp/project_1/project_1.srcs/sim_1/new/dff_TB.vhd

```
33
34  entity dff_TB is
35  --  Port ( );
36  end dff_TB;
37
38  architecture Behavioral of dff_TB is
39  component dff is
40      Port ( d : in STD_LOGIC;
41             clk : in STD_LOGIC;
42             r : in STD_LOGIC;
43             q : out STD_LOGIC;
44             qn : out STD_LOGIC);
45  end component dff;
46
47  signal d, clk, r, q, qn:std_logic;
48
49  begin
50
51  UUT: dff port map (d =>d, clk => clk, r => r, q => q, qn => qn);
52
53  generate_d: process
54  begin
55  d <= '0'; wait for 2 ns;
56  d <= '1'; wait for 2 ns;
57  end process;
58
59  generate_clk: process
60  begin
61  clk <= '0'; wait for 1 ns;
62  clk <= '1'; wait for 1 ns;
63  end process;
64
```

C:/Temp/project_1/project_1.srcs/sim_1/new/dff_TB.vhd

```
42              r : in STD_LOGIC;
43              q : out STD_LOGIC;
44              qn : out STD_LOGIC);
45  end component dff;
46
47  signal d, clk, r, q, qn:std_logic;
48
49  begin
50
51  UUT: dff port map (d =>d, clk => clk, r => r, q => q, qn => qn);
52
53  generate_d: process
54  begin
55  d <= '0'; wait for 2 ns;
56  d <= '1'; wait for 2 ns;
57  end process;
58
59  generate_clk: process
60  begin
61  clk <= '0'; wait for 1 ns;
62  clk <= '1'; wait for 1 ns;
63  end process;
64
65  generate_r: process
66  begin
67  r <= '0'; wait for 2 ns;
68  r <= '1'; wait for 2 ns;
69  end process;
70
71
72  end Behavioral;
73
```

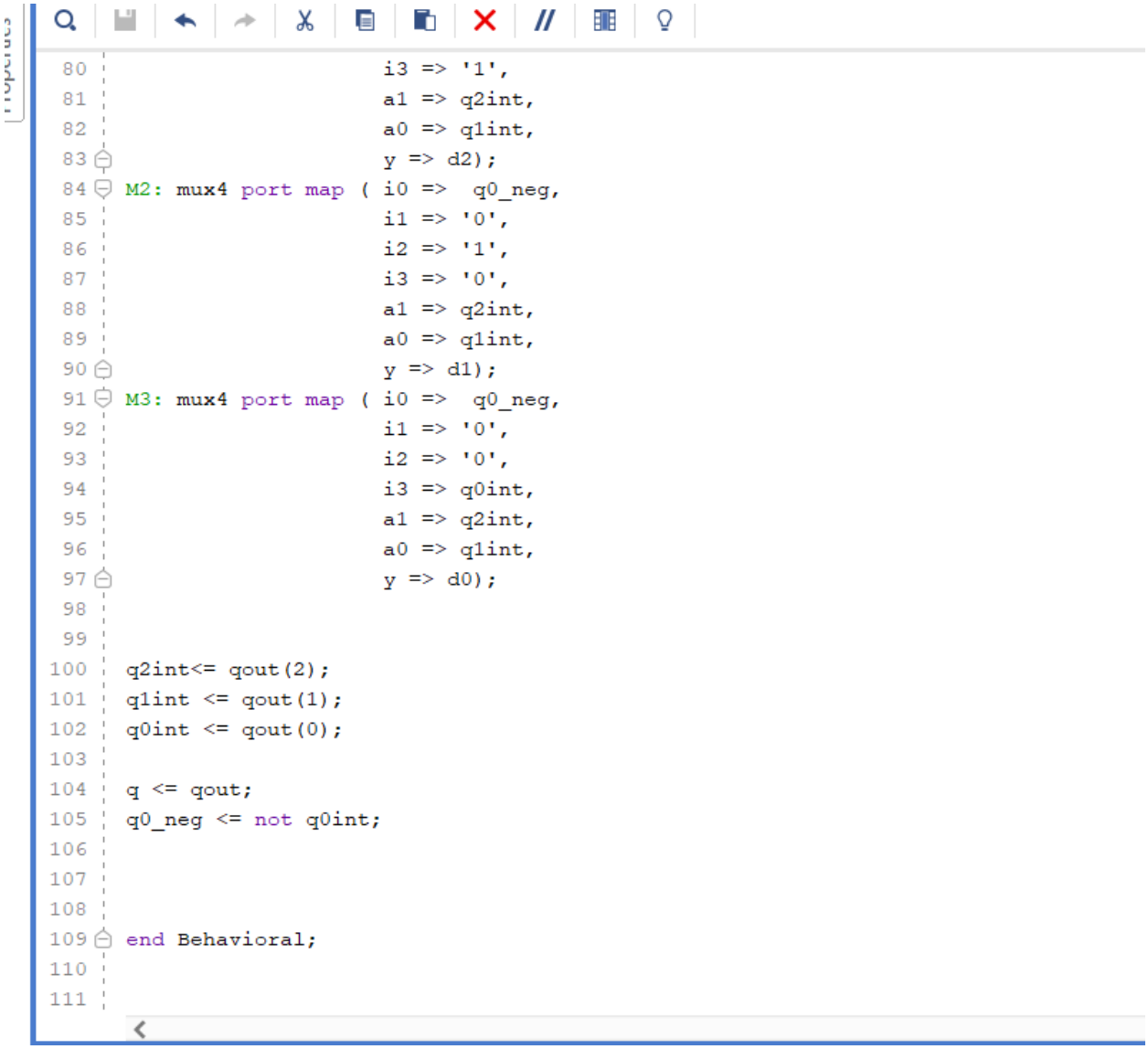
Simulare Bistabil



Sursa de design automat

```
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity automat is
35      Port ( r : in STD_LOGIC;
36             clk : in STD_LOGIC;
37             q : out STD_LOGIC_VECTOR (2 downto 0));
38  end automat;
39
40  architecture Behavioral of automat is
41  signal q2int, q1int, q0int, q0_neg, d2, d1, d0:std_logic;
42  signal qout:std_logic_vector(2 downto 0);
43
44  component dff is
45      Port ( d : in STD_LOGIC;
46             clk : in STD_LOGIC;
47             r : in STD_LOGIC;
48             q : out STD_LOGIC;
49             qn : out STD_LOGIC);
50  end component dff;
51
52  component mux4 is
53      Port ( i0 : in STD_LOGIC;
54             i1 : in STD_LOGIC;
55             i2 : in STD_LOGIC;
56             i3 : in STD_LOGIC;
57             a1 : in STD_LOGIC;
58             a0 : in STD_LOGIC;
59             y : out STD_LOGIC);
60  end component mux4;
61
62  begin
```

```
61
62  begin
63
64  U2: dff port map (d => d2,
65                    clk => clk,
66                    r => r,
67                    q => q2int);
68  U1: dff port map ( d => d1,
69                     clk => clk,
70                     r => r,
71                     q => q1int);
72  U0: dff port map ( d => d0,
73                     clk => clk,
74                     r => r,
75                     q => q0int);
76
77  M1: mux4 port map ( i0 =>  q0_neg, -- NOT q0int
78                      i1 => '0',
79                      i2 => q0int,
80                      i3 => '1',
81                      a1 => q2int,
82                      a0 => q1int,
83                      y => d2);
84  M2: mux4 port map ( i0 =>  q0_neg,
85                      i1 => '0',
86                      i2 => '1',
87                      i3 => '0',
88                      a1 => q2int,
89                      a0 => q1int,
90                      y => d1);
91  M3: mux4 port map ( i0 =>  q0_neg,
92                      i1 => '0',
```



```
                        i3 => '1',
                        a1 => q2int,
                        a0 => q1int,
                        y => d2);
M2: mux4 port map ( i0 =>  q0_neg,
                        i1 => '0',
                        i2 => '1',
                        i3 => '0',
                        a1 => q2int,
                        a0 => q1int,
                        y => d1);
M3: mux4 port map ( i0 =>  q0_neg,
                        i1 => '0',
                        i2 => '0',
                        i3 => q0int,
                        a1 => q2int,
                        a0 => q1int,
                        y => d0);


q2int<= qout(2);
q1int <= qout(1);
q0int <= qout(0);

q <= qout;
q0_neg <= not q0int;



end Behavioral;

```

Sursa de simulare automat

```
35
36  entity tb is
37  --  Port ( );
38  end tb;
39
40  architecture Behavioral of tb is
41  component  automat is
42      Port ( r : in STD_LOGIC;
43             clk : in STD_LOGIC;
44             q : out STD_LOGIC_VECTOR (2 downto 0));
45
46  end component automat;
47
48  signal clk, r:std_logic;
49  signal q:std_logic_vector(2 downto 0);
50
51  begin
52  UUT: automat port map ( clk => clk,
53                          r => r,
54                          q => q);
55
56
57    r <= '0' after 0 ns, '1' after 3 ns, '0' after 5 ns, '1' after 8 ns;
58  process
```

```
50
51  begin
52  UUT: automat port map ( clk => clk,
53                          r => r,
54                          q => q);
55
56
57    r <= '0' after 0 ns, '1' after 3 ns, '0' after 5 ns, '1' after 8 ns;
58  process
59  begin
60    clk <= '0';
61     wait for 1 ns;
62    clk <= '1';
63     wait for 1 ns;
64  end process;
65
66
67
68  end Behavioral;
69
70
71
72
73
```

Simulare finala