ECE 314
Cycle-accurate MIPS Simulator

Implementation Details
and
Requirements for Input/Output Files

Test input file format

```
.data
.text

main:
<code>
```

General format of the file. The **.data** section should remain unused

```
and $v0, $zero, $zero
and $v1, $zero, $zero
and $a0, $zero, $zero
and $a1, $zero, $zero
and $a2, $zero, $zero
<…>
```

Initialization section. All registers are initialized to zero except $gp and $sp (special registers with values that indicate a memory index)

Test input file format

```
ori $s0, $zero , 0x100
sw $s0, 0($gp)

ori $s0, $zero , 0x1
sw $s0, 4($gp)

ori $s0, $zero , 0x2
sw $s0, 8($gp)
<…>
```

Manually save values to memory starting from the address of $gp

```
next:
        lw $t0, 0($s0)
        sltu $t2, $s1, $t0
        bne $t2, $zero, less
        addi $s2, $s2, -1
        beq $s2, $zero, out
        addi $s0, $s0, 4
        j next
less:
        and $s1, $zero, $zero
        or $s1, $t0, $zero
        j next
out:
        sll $zero, $zero, 0
```

Code returning max in $s1.
The last line (sll $zero, $zero, 0) indicates the end of the sequence. It will always be there for consistency.

Output file format

- Three main sections:
  1. Name and ID
  2. Cycle per cycle architectural state, monitors, control signals and memory dump
  3. Final memory dump, architectural state and total execution cycles

- Section 1: Name and ID
  - Simple as that →

Name:
ID:

Output file format

- Section 2: Architectural state, control signals and memory dump

Cycle X:
Register File:

Reg1	Reg2	...	Reg31	Reg32

Monitors:

Mon1	Mon2	...	MonN-1	MonN

Memory State:

Add1	Add2	...	AddN-1	AddN

Cycle Y:
Regiser File:

Reg1	Reg2	...	Reg31	Reg32

Monitors:

Mon1	Mon2	...	MonN-1	MonN

Memory State:

Add1	Add2	...	AddN-1	AddN

Output file format

- Final State

Final State:
Register File:
Reg1 Reg2 ... Reg31 Reg32

Memory State:
Add1 Add2 ... AddN-1 AddN

Total Cycles:
Cycles

!!IMPORTANT!!
Never print the whole memory. Print only the addresses that changed over the course of your program

Output file Overview

Name: Student Name
ID: Student ID

Cycle X:
Register File:
Reg1 Reg2 ... Reg31 Reg32

Monitors:
Mon1 Mon2 ... MonN-1 MonN

Memory State:
Add1 Add2 ... AddN-1 AddN

Cycle Y:
Register File:
Reg1 Reg2 ... Reg31 Reg32

Monitors:
Mon1 Mon2 ... MonN-1 MonN

Memory State:
Add1 Add2 ... AddN-1 AddN

Final State:
Register File:
Reg1 Reg2 ... Reg31 Reg32

Memory State:
Add1 Add2 ... AddN-1 AddN

Total Cycles:
Cycles

!!IMPORTANT!!
All values in each line should be separated with a TAB, not a space or any other character!!