GOWIN
PROGRAMMING FOR THE FUTURE

# GW2A series of FPGA Products

# Data Sheet

**DS102-2.6.3E, 07/26/2023**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 06/03/2018 | 1.1E | Initial version published. |
| 09/12/2018 | 1.2E | ● MG196 and PG256S information added;<br>● The description of the Programable IO status for blank chips added;<br>● QN88 information added;<br>● GW2A-18 PLL list added. |
| 04/02/2019 | 1.3E | ● Recommended Operating Conditions updated;<br>● Changed Operating Temperature to Junction Temperature;<br>● The figure of part naming updated and automotive and fastest devices info. Added;<br>● The package of PG256C added. |
| 04/12/2019 | 1.4E | The package of EQ144 added. |
| 07/10/2019 | 1.5E | The GW2A-55 UG324 added. |
| 09/19/2019 | 1.6E | ● The GW2A-18 UG324 added;<br>● Power supply ramp rates updated. |
| 09/27/2019 | 1.7E | Junction temperature of Automotive operation updated. |
| 10/12/2019 | 1.8E | ● LQ144/EQ144 package size fixed;<br>● Part naming examples optimized. |
| 11/12/2019 | 1.9E | ● Number of Max. I/O updated;<br>● IODELAY description updated. |
| 12/13/2019 | 2.0E | ● The package of GW2A-55 UG324D added;<br>● The package of GW2A-18 PG256E added. |
| 03/09/2019 | 2.1E | GW2A-18C and GW2A-55C added. |
| 04/16/2020 | 2.1.1E | ● I/O Information of GW2A-55/ GW2A-55C UG324 updated;<br>● CFU view updated;<br>● One note for “I/O Operating Conditions Recommended” added. |
| 07/07/2020 | 2.1.2E | ● The recommended minimum value of VCCX revised.<br>● A note to “Package Mark Example” added. |
| 09/25/2020 | 2.2E | The GW2A-55 UG676 package info. Added. |
| 05/28/2021 | 2.2.1E | Parameters optimized. |
| 07/16/2021 | 2.3E | The UG484 and PG256CF packages of GW2A-18 added. |
| 12/27/2021 | 2.3.1E | ● The PG256SF package of GW2A-18 added.<br>● The UG324F package of GW2A-55 added.<br>● Further information about I/O logic added. |
| 02/17/2022 | 2.3.2E | Information on I/O standards optimized. |
| 05/25/2022 | 2.3.3E | ● Recommended I/O Operating Conditions updated.<br>● Power Supply Ramp Rates updated. |
| 09/05/2022 | 2.3.4E | ● The maximum value of the differential input threshold $V_{THD}$ updated.<br>● Note about DC current limit added.<br>● Table 4-3 Power Supply Ramp Rates updated.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated.<br>● Figure 3-1 Architecture Diagram updated. |
| 09/15/2022 | 2.4E | ● GW2A-55 UG484S package added.<br>● Table 4-5 POR Specifications updated. |
| 10/28/2022 | 2.5E | GW2A-18 PG484C package added. |
| 11/11/2022 | 2.5.1E | ● Section 3.4.4 Byte-enable removed.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. |
| 01/12/2023 | 2.5.2E | ● Table 4-1 Absolute Max. Ratings updated. |

| Date | Version | Description |
| --- | --- | --- |
| | | ● Table 2-3 Package Information, Max. User I/O, and LVDS Pairs updated.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. |
| 03/16/2023 | 2.6E | ● GW2A-18 LQ144 package removed.<br>● Informaion on Slew Rate removed.<br>● Table 4-3 Power Supply Ramp Rates updated.<br>● Note about the default state of GPIO modified. |
| 05/11/2023 | 2.6.1E | ● 3.4.2 Memory Configuration Mode updated.<br>● Table 4-17 External Switching Characteristics updated.<br>● Table 4-18 I/O Regiter Parameters Using Dedicated GCLK Input through GCLK Tree without PLL added. |
| 05/25/2023 | 2.6.2E | ● Table 4-13 CFU Block Internal Timing Parameters updated.<br>● Table 4-14 BSRAM Internal Timing Parameters updated.<br>● Table 4-15 DSP Internal Timing Parameters updated. |
| 07/26/2023 | 2.6.3E | ● Table 2-3 Package Information, Max. User I/O, and LVDS Pairs updated, correcting the maximum numbers of user IOs of the GW2A-55 device in UG324, UG324F, and UG324D packages.<br>● Figure 5-3 Package Mark Example updated.<br>● Note about the default state of GPIO optimized. |

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# 1 About This Guide

## 1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW2A series of the FPGA products, which helps you to understand the GW2A series of the FPGA products quickly and select and use devices appropriately.

## 1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG111, GW2A series FPGA Products Package and Pinout
- UG110, GW2A-18 Pinout
- UG113, GW2A-55 Pinout

## 1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

**Table 1-1 Abbreviations and Terminologies**

| Abbreviations and Terminology | Name |
|---|---|
| ALU | Arithmetic Logic Unit |
| BSRAM | Block Static Random Access Memory |
| CFU | Configurable Function Unit |
| CLS | Configurable Logic Section |
| CRU | Configurable Routing Unit |
| DCS | Dynamic Clock Selector |
| DP | True Dual Port 16K BSRAM |
| DQCE | Dynamic Quadrant Clock Enable |

| Abbreviations and Terminology | Name |
|---|---|
| DSP | Digital Signal Processing |
| EQ | ELQFP |
| FPGA | Field Programmable Gate Array |
| GPIO | Gowin Programable IO |
| IOB | Input/Output Block |
| LQ | LQFP |
| LUT4 | 4-input Look-up Table |
| LUT5 | 5-input Look-up Table |
| LUT6 | 6-input Look-up Table |
| LUT7 | 7-input Look-up Table |
| LUT8 | 8-input Look-up Table |
| PG | PBGA |
| PLL | Phase-locked Loop |
| REG | Register |
| SDP | Semi Dual Port 16K BSRAM |
| SP | Single Port 16K BSRAM |
| SSRAM | Shadow Static Random Access Memory |
| TDM | Time Division Multiplexing |
| UG | UBGA |

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

# 2 General Description

The GW2A series of FPGA products are the first generation products of the Arora family. They offer a range of comprehensive features and rich internal resources like high-performance DSP resources, a high-speed LVDS interface, and abundant BSRAM memory resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products suitable for high-speed, low-cost applications.

GOWINSEMI continually invests the development of next-generation FPGA hardware environment through the market-oriented independent research and developments that supports the GW2A series of FPGA products, which can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

## 2.1 Features

- Lower power consumption
  - 55nm SRAM technology
  - Core voltage: 1.0V
  - Clock dynamically turns on and off
- Multiple I/O standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, II, SSTL15; HSTL18 I, II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Output drive strength option
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
  - Hot socket
- High performance DSP
  - High performance digital signal processing ability
  - Supports 9 x 9,18 x 18,36 x 36 bits multiplier and 54 bits accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter

- Abundant slices
  - Four input LUT (LUT4)
  - Supports shift register and distributed register
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Configuration
  - JTAG configuration
  - Four GowinCONFIG configuration modes: SSPI, MSPI, CPU, SERIAL
  - Supports JTAG and SSPI programming SPI Flash directly and other modes programming SPI Flash via IP
  - Data stream file encryption and security bit settings

# 2.2 Product Resources

**Table 2-1 Product Resources**

| Device | GW2A-18 | GW2A-55 |
|---|---|---|
| LUT4 | 20,736 | 54,720 |
| Flip-Flop (FF) | 15,552 | 41,040 |
| Shadow SRAM SSRAM (bits) | 41,472 | 109,440 |
| Block SRAM BSRAM (bits) | 828K | 2,520K |
| BSRAM quantity BSRAM | 46 | 140 |
| 18 x 18 Multiplier | 48 | 40 |
| Maximum[1](PLLs) | 4 | 6 |
| Total number of I/O banks | 8 | 8 |
| Max. I/O | 384 | 608 |
| Core voltage | 1.0V | 1.0V |

**Note!**

[1] Different packages support different numbers of PLLs. Up to six PLLs can be supported.

**Table 2-2 GW2A-18 PLL List**

| Package | Device | PLL |
|---|---|---|
| EQ144 | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |
| MG196 | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |
| QN88 | GW2A-18 | PLLL1/ PLLR1 |
| PG256/ PG256S/ PG256C/ PG256CF/ | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |

| Package | Device | PLL |
|---|---|---|
| PG256E/ PG256SF | | |
| PG484/ PG484C | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |
| UG324 | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |
| UG484 | GW2A-18 | PLLL0/PLLL1/PLLR0/PLLR1 |

**Table 2-3 Package Information, Max. User I/O, and LVDS Pairs**

| Package | Pitch(mm) | Size(mm) | E-pad Size (mm) | GW2A-18 | GW2A-55 |
|---|---|---|---|---|---|
| QN88 | 0.4 | 10 x10 | 6.74 x 6.74 | 66（22） | - |
| EQ144 | 0.5 | 20 x 20 | 9.74 x 9.74 | 119（34） | - |
| MG196 | 0.5 | 8 x 8 | - | 114（39） | - |
| PG256 | 1.0 | 17 x 17 | - | 207（73） | - |
| PG256S | 1.0 | 17 x 17 | - | 192（72） | - |
| PG256SF | 1.0 | 17 x 17 | - | 192（71） | - |
| PG256C | 1.0 | 17 x 17 | - | 190（64） | - |
| PG256CF | 1.0 | 17 x 17 | - | 190（65） | - |
| PG256E | 1.0 | 17 x 17 | - | 162（29） | - |
| PG484 | 1.0 | 23 x 23 | - | 319（78） | 319（76） |
| PG484C | 1.0 | 23 x 23 | - | 355（89） | - |
| PG1156 | 1.0 | 35 x 35 | - | - | 607（97） |
| UG324 | 0.8 | 15 x 15 | - | 239（90） | 239（86） |
| UG324D | 0.8 | 15 x 15 | - | - | 239（71） |
| UG324F | 0.8 | 15 x 15 | - | - | 239（86） |
| UG484 | 0.8 | 15 x 15 | - | 379（94） | - |
| UG484S | 0.8 | 19 x 19 | - | - | 344（91） |
| UG676 | 0.8 | 21 x 21 | - | - | 525（97） |

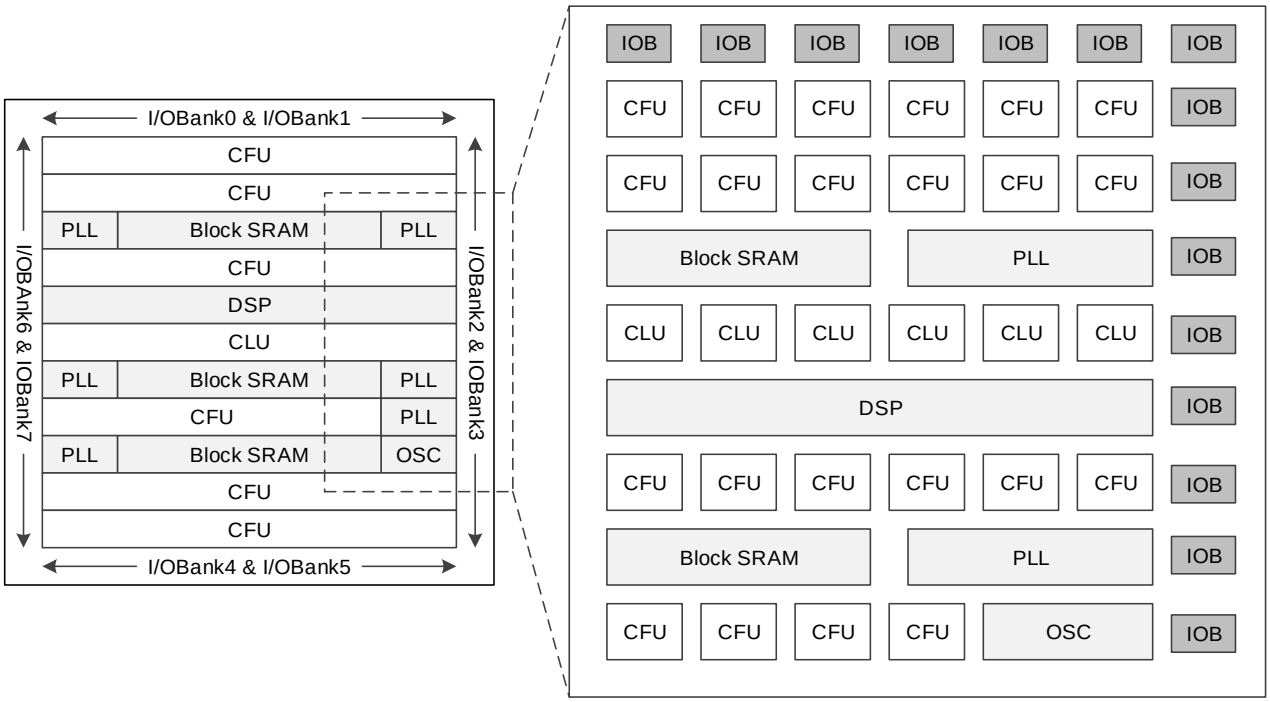
**Note!**

- The package types in this data sheet are written with abbreviations. See 5.1 Part Name for further information.
- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- The IO speed of JTAG pins multiplexing is less than 40 MHz.

# 3 Architecture

## 3.1 Architecture Overview

**Figure 3-1 Architecture Diagram**




See Figure 3-1 for an overview of the architecture of the GW2A series of FPGA products. Please refer to Table 2-1 for GW2A-18 and GW2A-55 devices internal resources. The core of device is an array of Configurable Logic Unit (CFU) surrounded by IO blocks. Besides, GW2A provides BSRAM, DSP, PLL, and on chip oscillator.

Configurable Function Unit (CFU) is the base cell for the array of GW2A series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see 3.2 Configurable Function Unit.

The I/O resources in the GW2A series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, which are divided into eight Banks, including Bank0 ~ Bank7. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see 3.3 IOB.

The BSRAM is embedded as a row in the GW2A series of FPGA products. In the FPGA array, each BSRAM occupies three columns of CFU. Each BSRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. For more detailed information, see 3.4 Block SRAM (BSRAM).

DSP is embedded in the GW2A series of FPGA products. DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. For more detailed information, see 3.5 DSP.

GW2A provides one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each GW2A series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching ±5%. For more detailed information, please refer to 3.6 Clock, 3.10 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW2A series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see 3.6 Clock, 3.7 Long Wire (LW), *and* 3.8 Global Set/Reset (GSR).

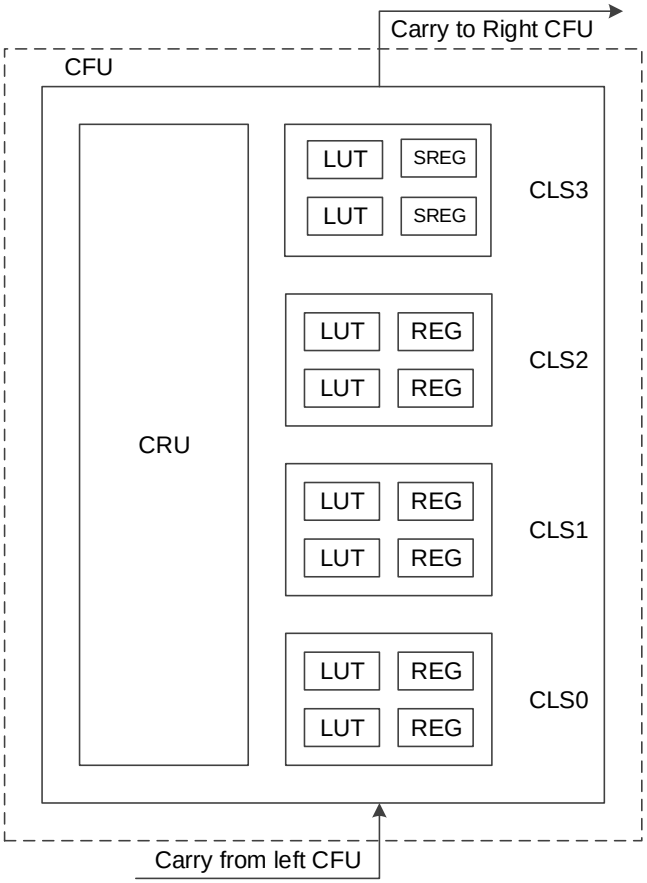
## 3.2 Configurable Function Unit

The configurable function unit and the configurable logic unit are two basic units for FPGA core of GOWINSEMI. As shown in Figure 3-2, each unit consists of four configurable logic sections and its configurable routing unit. Each of the three configurable logic sections contains two 4-input LUTs and two registers, and the other one only contians two 4-input LUTs.

Configurable logical sections in CLU cannot be configured as SRAM, but as basic logic, ALU, and ROM. The configurable logic sections in the CFU can be configured as basic logic, ALU, SRAM, and ROM depending on the applications. This section takes CFU as an example to introduce CFU and CLU.

For more information about CFU, please refer to *UG288, Gowin Configurable Function Unit (CFU) User Guide*.

**Figure 3-2 CFU Structure**



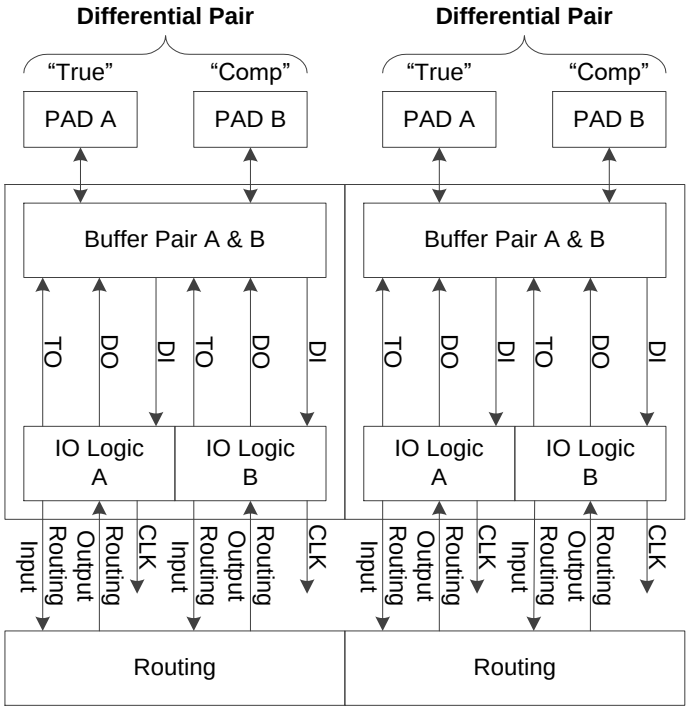

**Note!**

SREG needs special patch supporting. Please contact Gowin technical support or local O ffice for this patch.

# 3.3 IOB

The IOB in the GW2A series of FPGA products includes IO Buffer, IO Logic, and its Routing Unit. As shown below, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a Single-ended input/output.

**Figure 3-3 IOB Structure View**




IOB Features:

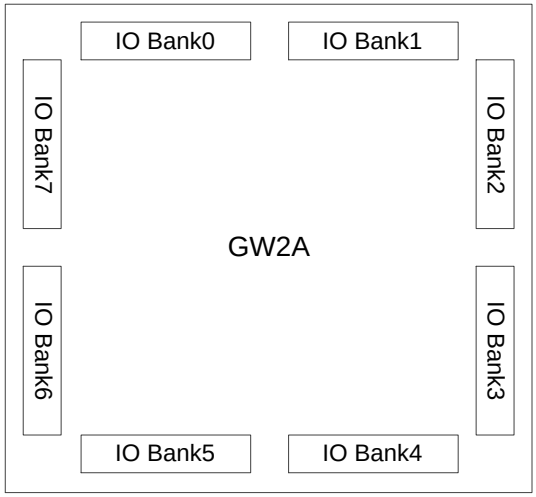
- $V_{CCIO}$ supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode

## 3.3.1 I/O Buffer

There are eight I/O Banks in the GW2A series of FPGA products, as shown in Figure 3-4. Each Bank has independent IO source $V_{CCIO}$. $V_{CCIO}$ can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. In order to support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as reference voltage. User can choose from internal reference voltage of the bank (0.5 x $V_{CCIO}$) or external reference voltage using any IO from the bank. $V_{CCX}$ is 2.7V and 3.3V.

Different banks in the GW2A Series of FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O and is supported in Bank 2/3/6/7. Differential resistor is set for LVDS input and is only supported in Bank 0/1. Please refer to *UG289, Gowin Programable IO User Guide* for more detailed information.

**Figure 3-4 GW2A I/O Bank Distribution**




**Note!**

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of CONFIG-related I/Os varies depending on the configuration mode.

For the $V_{CCIO}$ requirements of different I/O standards, see Table 3-1 and Table 3-2.

**Table 3-1 Output I/O Standards and Configuration Options**

| I/O output Type | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typ. Applicaiton |
|---|---|---|---|---|
| LVTTL33 | Single-ended | 3.3 | 4,8,12,16,24 | universal interface |
| LVCMOS33 | Single-ended | 3.3 | 4,8,12,16,24 | universal interface |
| LVCMOS25 | Single-ended | 2.5 | 4,8,12,16 | universal interface |
| LVCMOS18 | Single-ended | 1.8 | 4,8,12 | universal interface |
| LVCMOS15 | Single-ended | 1.5 | 4,8 | universal interface |
| LVCMOS12 | Single-ended | 1.2 | 4,8 | universal interface |
| SSTL25_I | Single-ended | 2.5 | 8 | memory interface |
| SSTL25_II | Single-ended | 2.5 | 8 | memory interface |
| SSTL33_I | Single-ended | 3.3 | 8 | memory interface |
| SSTL33_II | Single-ended | 3.3 | 8 | memory interface |
| SSTL18_I | Single-ended | 1.8 | 8 | memory interface |
| SSTL18_II | Single-ended | 1.8 | 8 | memory interface |
| SSTL15 | Single-ended | 1.5 | 8 | memory interface |
| HSTL18_I | Single-ended | 1.8 | 8 | memory interface |
| HSTL18_II | Single-ended | 1.8 | 8 | memory interface |
| HSTL15_I | Single-ended | 1.5 | 8 | memory interface |
| PCI33 | Single-ended | 3.3 | N/A | PC and embedded system |
| LVPECL33E | Differential | 3.3 | 16 | High-speed data transmission |

| I/O output Type | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typ. Applicaiton |
|---|---|---|---|---|
| MLVDS25E | Differential | 2.5 | 16 | LCD timing driver interface and column driver interface |
| BLVDS25E | Differential | 2.5 | 16 | Multi-point high-speed data transmission |
| RSDS25E | Differential | 2.5 | 8 | high-speed point-to-point data transmission |
| LVDS25E | Differential | 2.5 | 8 | high-speed point-to-point data transmission |
| LVDS25 | Differential (TLVDS) | 2.5/3.3 | 3.5/2.5/2/1.25 | high-speed point-to-point data transmission |
| RSDS | Differential (TLVDS) | 2.5/3.3 | 2 | high-speed point-to-point data transmission |
| MINILVDS | Differential (TLVDS) | 2.5/3.3 | 2 | LCD timing driver interface and column driver interface |
| PPLVDS | Differential (TLVDS) | 2.5/3.3 | 3.5 | LCD row/column driver |
| SSTL15D | Differential | 1.5 | 8 | memory interface |
| SSTL25D_I | Differential | 2.5 | 8 | memory interface |
| SSTL25D_II | Differential | 2.5 | 8 | memory interface |
| SSTL33D_I | Differential | 3.3 | 8 | memory interface |
| SSTL33D_II | Differential | 3.3 | 8 | memory interface |
| SSTL18D_I | Differential | 1.8 | 8 | memory interface |
| SSTL18D_II | Differential | 1.8 | 8 | memory interface |
| HSTL18D_I | Differential | 1.8 | 8 | memory interface |
| HSTL18D_II | Differential | 1.8 | 8 | memory interface |
| HSTL15D_I | Differential | 1.5 | 8 | memory interface |
| LVCMOS12D | Differential | 1.2 | 8/4 | universal interface |
| LVCMOS15D | Differential | 1.5 | 8/4 | universal interface |
| LVCMOS18D | Differential | 1.8 | 8/12/4 | universal interface |
| LVCMOS25D | Differential | 2.5 | 8/16/12/4 | universal interface |
| LVCMOS33D | Differential | 3.3 | 8/24/16/12/4 | universal interface |

**Table 3-2 Input I/O Standards and Configuration Options**

| I/O Input Type | Single-ended /Differential | Bank $V_{CCIO}$ (V) | Hysteresis | Need $V_{REF}$ |
|---|---|---|---|---|
| LVTTL33 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS33 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS25 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS18 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |

| I/O Input Type | Single-ended /Differential | Bank $V_{CCIO}$ (V) | Hysteresis | Need $V_{REF}$ |
|---|---|---|---|---|
| LVCMOS15 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS12 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| SSTL15 | Single-ended | 1.5/1.8/2.5/3.3 | No | Yes |
| SSTL25_I | Single-ended | 2.5/3.3 | No | Yes |
| SSTL25_II | Single-ended | 2.5/3.3 | No | Yes |
| SSTL33_I | Single-ended | 3.3 | No | Yes |
| SSTL33_II | Single-ended | 3.3 | No | Yes |
| SSTL18_I | Single-ended | 1.8/2.5/3.3 | No | Yes |
| SSTL18_II | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL18_I | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL18_II | Single-ended | 1.8/2.5/3.3 | No | Yes |
| HSTL15_I | Single-ended | 1.5/1.8/2.5/3.3 | No | Yes |
| PCI33 | Single-ended | 3.3 | Yes | No |
| LVCMOS33OD25 | Single-ended | 2.5 | No | No |
| LVCMOS33OD18 | Single-ended | 1.8 | No | No |
| LVCMOS33OD15 | Single-ended | 1.5 | No | No |
| LVCMOS25OD18 | Single-ended | 1.8 | No | No |
| LVCMOS25OD15 | Single-ended | 1.5 | No | No |
| LVCMOS18OD15 | Single-ended | 1.5 | No | No |
| LVCMOS15OD12 | Single-ended | 1.2 | No | No |
| LVCMOS25UD33 | Single-ended | 3.3 | No | No |
| LVCMOS18UD25 | Single-ended | 2.5 | No | No |
| LVCMOS18UD33 | Single-ended | 3.3 | No | No |
| LVCMOS15UD18 | Single-ended | 1.8 | No | No |
| LVCMOS15UD25 | Single-ended | 2.5 | No | No |
| LVCMOS15UD33 | Single-ended | 3.3 | No | No |
| LVCMOS12UD15 | Single-ended | 1.5 | No | No |
| LVCMOS12UD18 | Single-ended | 1.8 | No | No |
| LVCMOS12UD25 | Single-ended | 2.5 | No | No |
| LVCMOS12UD33 | Single-ended | 3.3 | No | No |
| LVDS25 | Differential | 2.5/3.3 | No | No |
| RSDS | Differential | 2.5/3.3 | No | No |
| MINILVDS | Differential | 2.5/3.3 | No | No |
| PPLVDS | Differential | 2.5/3.3 | No | No |
| LVDS25E | Differential | 2.5/3.3 | No | No |
| MLVDS25E | Differential | 2.5/3.3 | No | No |
| BLVDS25E | Differential | 2.5/3.3 | No | No |
| RSDS25E | Differential | 2.5/3.3 | No | No |
| LVPECL33E | Differential | 3.3 | No | No |

| I/O Input Type | Single-ended /Differential | Bank $V_{CCIO}$ (V) | Hysteresis | Need $V_{REF}$ |
|---|---|---|---|---|
| SSTL15D | Differential | 1.5/1.8/2.5/3.3 | No | No |
| SSTL25D_I | Differential | 2.5/3.3 | No | No |
| SSTL25D_II | Differential | 2.5/3.3 | No | No |
| SSTL33D_I | Differential | 3.3 | No | No |
| SSTL33D_II | Differential | 3.3 | No | No |
| SSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| SSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| HSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| HSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| HSTL15D_I | Differential | 1.5/1.8/2.5/3.3 | No | No |

## 3.3.2 I/O Logic

Figure 3-5 shows the I/O logic output of the GW2A series of FPGA products.

**Figure 3-5 I/O Logic Output**

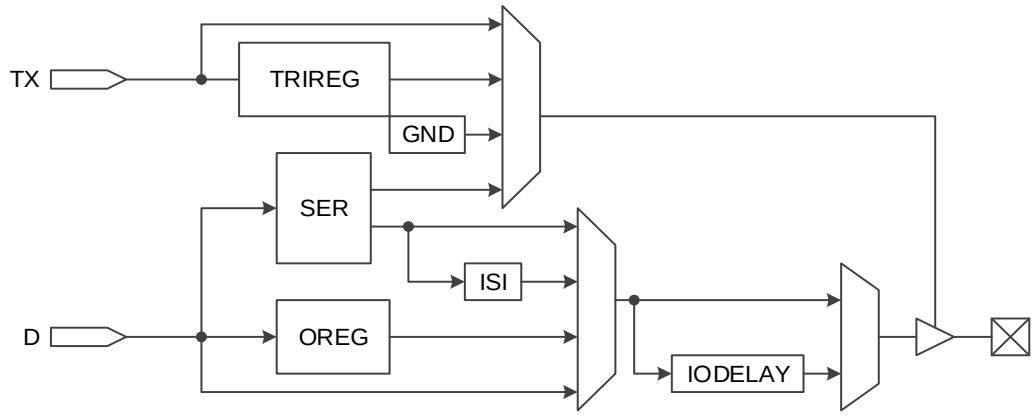



Figure 3-6 shows the I/O logic input of the GW2A series of FPGA products.

**Figure 3-6 I/O Logic Input**

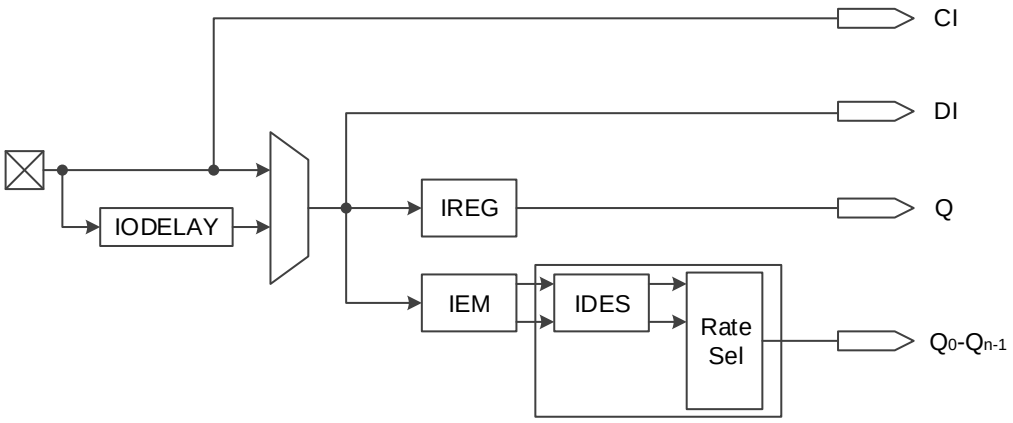


**Table 3-1 Port Descsription**

| Ports | I/O | Description |
|---|---|---|
| CI[1] | Input | GCLK input signal.<br>For the number of GCLK input signals, please refer to *UG110, GW2A-18 Pinout* and *UG113, GW2A-55 Pinout*. |
| DI | Input | IO port low-speed input signal, entering into Fabric directly. |
| Q | Output | IREG output signal in SDR module. |
| $Q_0$-$Q_{n-1}$ | Output | IDES output signal in DDR module. |

**Note!**

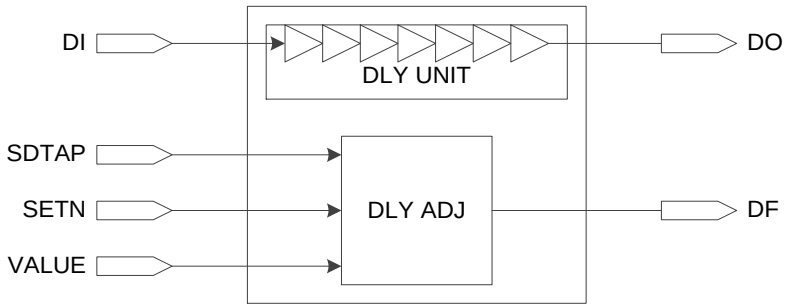
When CI is used as GCLK input, DI, Q, and $Q_0$-$Q_{n-1}$ cannot be used as I/O input and output.

A description of the I/O logic modules of the GW2A series of FPGA products is presented below.

## IODELAY

See Figure 3-7 for an overview of the IODELAY. Each I/O of the GW2A series of FPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 18ps.

**Figure 3-7 IODELAY**



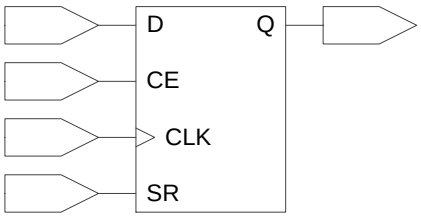

The delay cell can be controlled in two ways:

- Static control.
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time.

## I/O Register

See Figure 3-8 for the I/O register in the GW2A series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and a tristate Register (TRIREG).

**Figure 3-8 Register Structure in I/O Logic**



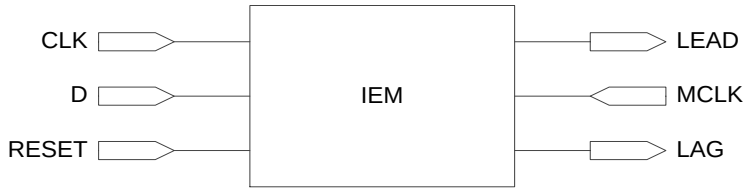

**Note!**

- CE can be either active low (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

### IEM

IEM is for sampling clock edge and is used in the generic DDR mode, as shown in Figure 3-9.

**Figure 3-9 IEM Structure**




### De-serializer DES and Clock Domain Transfer

The GW2A series of FPGA products provides a simple serializer SER for each output I/O to support advanced I/O protocols. The Clock domain transfer module of the input clock in DES provides the ability to safely switch the external sampling clock to the internal continuous running clock. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. The function is applied to the interface of DDR memory.
- For the DDR3 memory interface standard, align the data after DQS read-leveling.
- In regular DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module also needs to be used.

Each DQS provides WADDR and RADDR signals to the same group in the clock domain transfer module.

### Serializer SER

The GW2A series of FPGA products provides a simple serializer (SER) for each output I/O to support advanced I/O protocols.

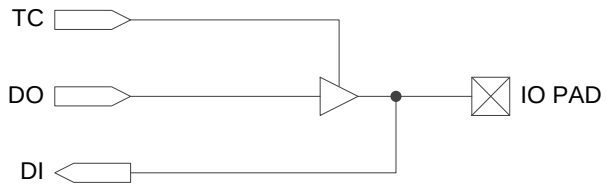
## 3.3.3 I/O Logic Modes

The I/O Logic in the GW2A series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

### Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-10, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

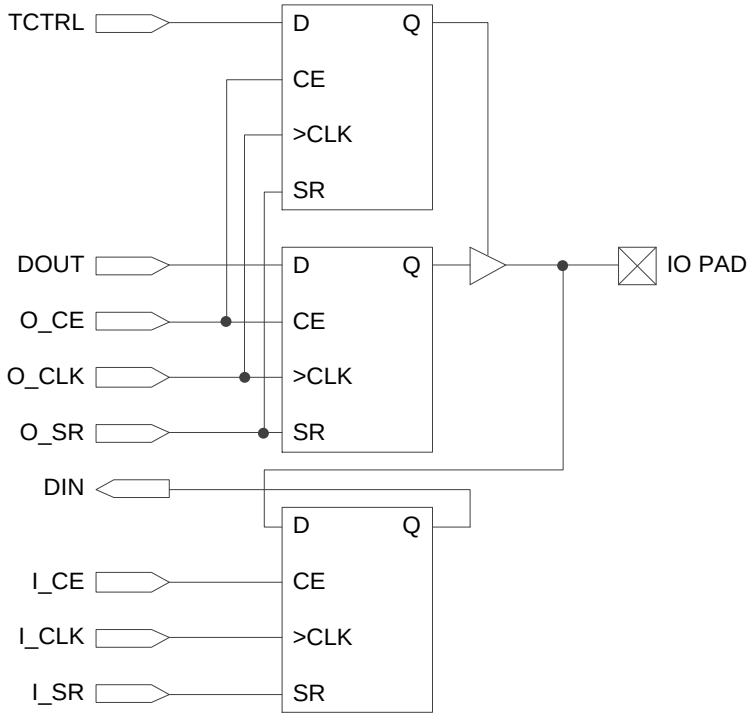
**Figure 3-10 I/O Logic in Basic Mode**




### SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-11. This can effectively improve IO timing.

**Figure 3-11 I/O Logic in SDR Mode**




**Note!**

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

### Generic DDR Mode

Higher speed I/O protocols can be supported in generic DDR mode.

Figure 3-12 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

**Figure 3-12 I/O Logic in DDR Input Mode**

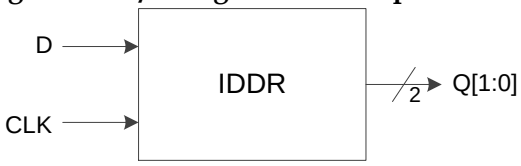
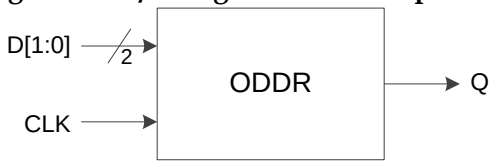



Figure 3-13 shows the generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

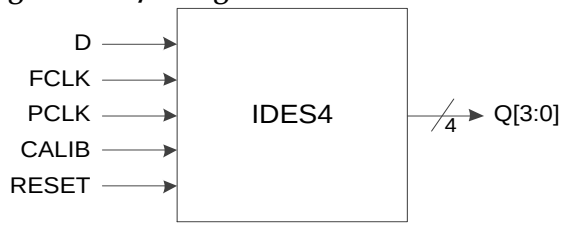
**Figure 3-13 I/O Logic in DDR Output Mode**




### IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

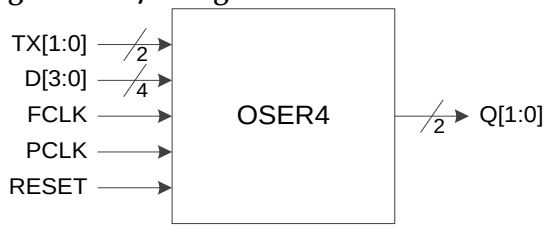
**Figure 3-14 I/O Logic in IDES4 Mode**




### OSER4 Mode

In OSER4 mode, the speed ratio of PAD to FPGA internal logic is 4:1.

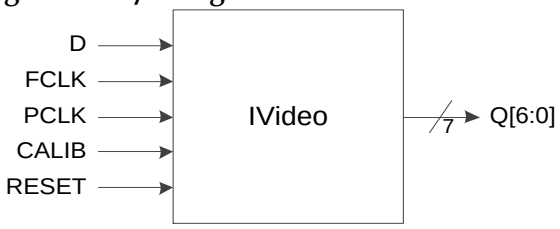
**Figure 3-15 I/O Logic in OSER4 Mode**



### IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

**Figure 3-16 I/O Logic in IVideo Mode**



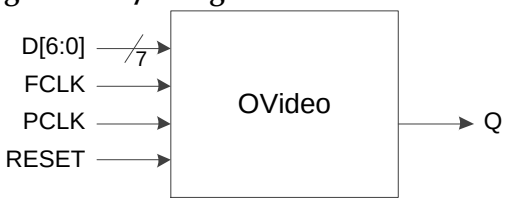

**Note!**

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

### OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

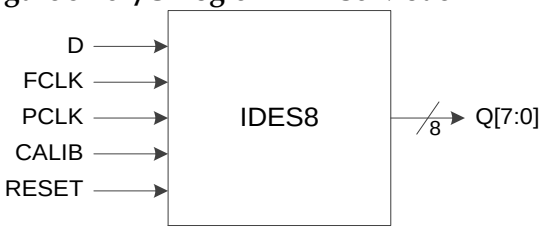
**Figure 3-17 I/O Logic in OVideo Mode**




### IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

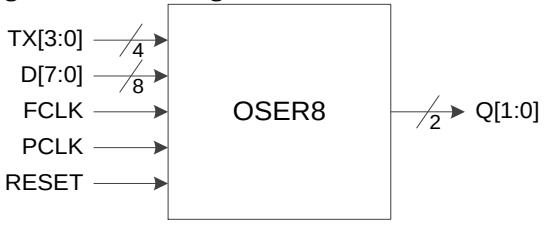
**Figure 3-18 I/O Logic in IDES8 Mode**




### OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

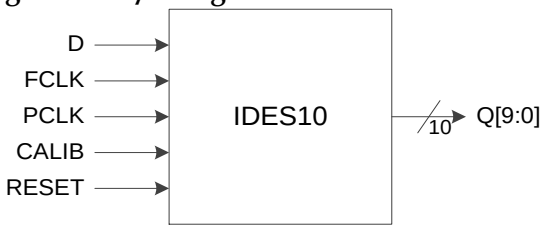
**Figure 3-19 I/O Logic in OSER8 Mode**



### IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

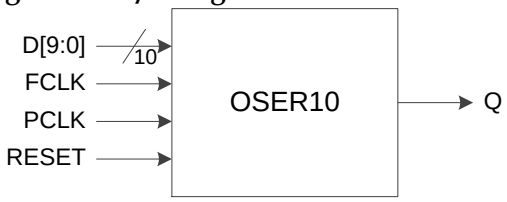
**Figure 3-20 I/O Logic in IDES10 Mode**




### OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

**Figure 3-21 I/O Logic in OSER10 Mode**



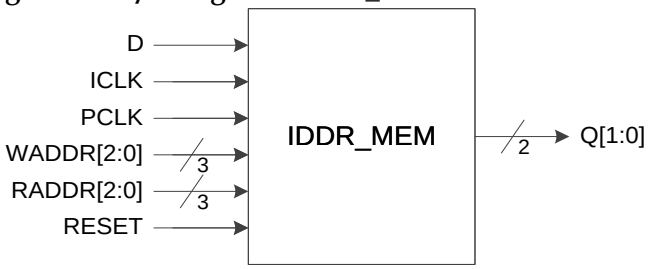

The GW2A series of FPGA products support IO interface mode with memory, support double/four/eight speed rate input and output, including IDDR_MEM, IDES4_MEM, IDES8_MEM, ODDR_MEM, OSER4_MEM, and OSER8_MEM modes.

IDDR_MEM/IDES4_MEM/IDES8_MEM needs to be used with DQS. ICLK connects output signal DQSR90 of DQS and sends data to IO interfaces aCCIOrding to ICLK clock edge. WADDR [2: 0] connects output signal WPOINT of DQS; RADDR [2: 0] connects output signal RPOINT of DQS.

ODDR_MEM/OSER4_MEM/OSER8_MEM needs to be used with DQS. TCLK connects output signal DQSW0 or DQSW270 of DQS, and outputs data from IO interfaces aCCIOrding to TCLK clock edge.

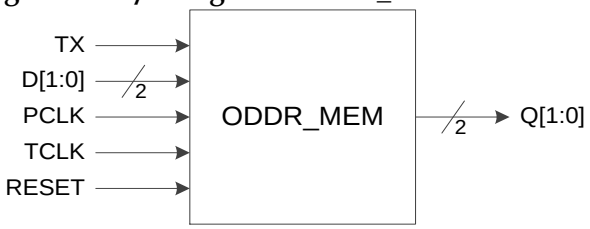
### IDDR_MEM Mode

**Figure 3-22 I/O Logic in IDDR_MEM Mode**



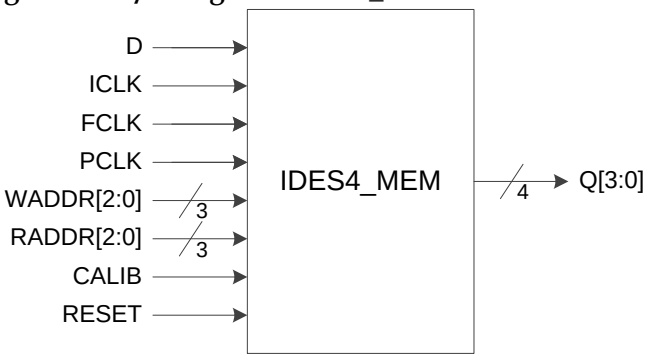
## ODDR_MEM Mode

**Figure 3-23 I/O Logic in ODDR_MEM Mode**



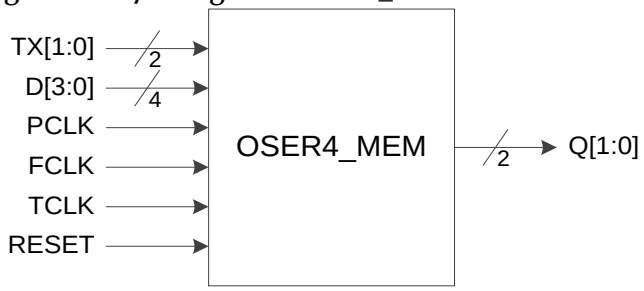

## IDES4_MEM Mode

**Figure 3-24 I/O Logic in IDES4_MEM Mode**



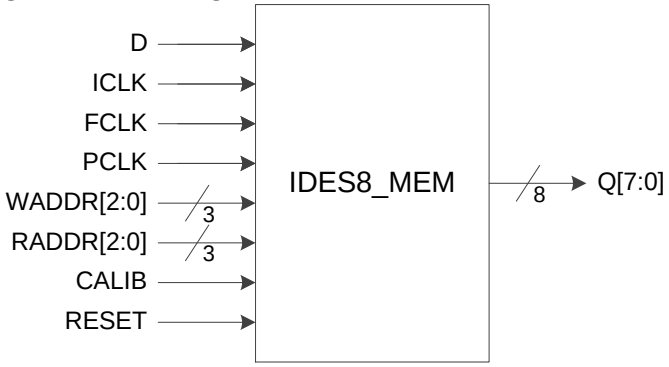

## OSER4_MEM Mode

**Figure 3-25 I/O Logic in OSER4_MEM Mode**



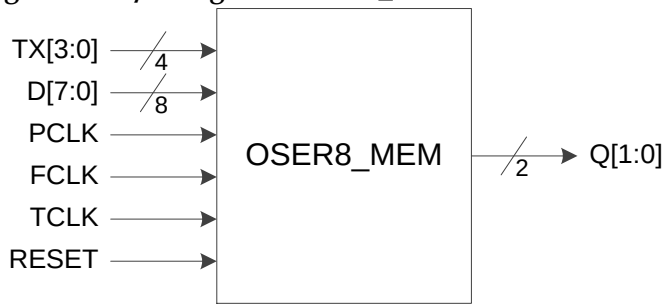

## IDES8_MEM Mode

**Figure 3-26 I/O Logic in IDES8_MEM Mode**



**OSER8_MEM Mode**

**Figure 3-27 I/O Logic in OSER8_MEM Mode**




# 3.4 Block SRAM (BSRAM)

## 3.4.1 Introduction

The GW2A series of FPGA products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from SSRAM (Shadow SRAM). Each BSRAM occupies three columns of CFU in the FPGA array. Each BSRAM has 18,432 bits (18Kbits). There are five operation modes: single port, dual port, semi-dual port, ROM, and FIFO. The signals and functional descriptions of BSRAM are listed in the following table.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features include the following:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 380 MHz at max (typical, Read-before-write is 230MHz)
- Single port
- Dual port
- Semi-dual port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Normal read and write mode
- Read-before-write mode
- Write-through mode

## 3.4.2 Memory Configuration Mode

The BSRAM mode in the GW2A series of FPGA products supports different data bus widths. See Table 3-3.

**Table 3-3 Memory Size Configuration**

| Single Port Mode | Dual Port Mode | Semi-Dual Port Mode | Read Only |
|---|---|---|---|
| 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 |

| Single Port Mode | Dual Port Mode | Semi-Dual Port Mode | Read Only |
|---|---|---|---|
| 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 |
| 4K x 4 | 4K x 4 | 4K x 4 | 4K x 4 |
| 2K x 8 | 2K x 8 | 2K x 8 | 2K x 8 |
| 1K x 16 | 1K x 16 | 1K x 16 | 1K x 16 |
| 512 x 32 | - | 512 x 32 | 512 x 32 |
| 2K x 9 | 2K x 9 | 2K x 9 | 2K x 9 |
| 1K x 18 | 1K x 18 | 1K x 18 | 1K x 18 |
| 512 x 36 | - | 512 x 36 | 512 x 36 |

### Single Port Mode

The single port mode can support 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In the single port mode, BSRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of BSRAM. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to *SUG283, Gowin Primitives User Guide* > 3 Memory.

### Dual Port Mode

The dual port mode can support 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Dual Port BSRAM.

For further information about Dual Port Block Memory ports and the related description, please refer to *SUG283, Gowin Primitives User Guide* > 3 Memory.

### Semi-Dual Port Mode

The semi-dual port mode can support 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Semi-Dual

Port BSRAM.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to *SUG283, Gowin Primitives User Guide* > 3 Memory.

**Read Only**

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to *SUG283, Gowin Primitives User Guide* > 3 Memory.

## 3.4.3 Mixed Data Bus Width Configuration

The BSRAM in the GW2A series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-4 and Table 3-5 below.

**Table 3-4 Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 2K x 9 | 1K x 18 |
| 16K x 1 | * | * | * | * | * | | |
| 8K x 2 | * | * | * | * | * | | |
| 4K x 4 | * | * | * | * | * | | |
| 2K x 8 | * | * | * | * | * | | |
| 1K x 16 | * | * | * | * | * | | |
| 2K x 9 | | | | | | * | * |
| 1K x 18 | | | | | | * | * |

**Note!**

"*"denotes the modes supported.

**Table 3-5 Semi Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512x32 | 2K x 9 | 1K x 18 | 512x36 |
| 16K x 1 | * | * | * | * | * | * | | | |
| 8K x 2 | * | * | * | * | * | * | | | |
| 4K x 4 | * | * | * | * | * | * | | | |
| 2K x 8 | * | * | * | * | * | * | | | |
| 1K x 16 | * | * | * | * | * | * | | | |
| 512x32 | * | * | * | * | * | * | | | |
| 2K x 9 | | | | | | | * | * | * |

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512x32 | 2K x 9 | 1K x 18 | 512x36 |
| 1K x 18 | | | | | | | * | * | * |

**Note!**

”*”denotes the modes supported.

## 3.4.4 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

## 3.4.5 Synchronous Operation

- All the input registers of BSRAM support synchronous write.
- The output register can be used as a pipeline register to improve design performance.
- The output registers are bypass-able.

## 3.4.6 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

## 3.4.7 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

### Read Mode

Read data from the BSRAM via output registers or without using the registers.

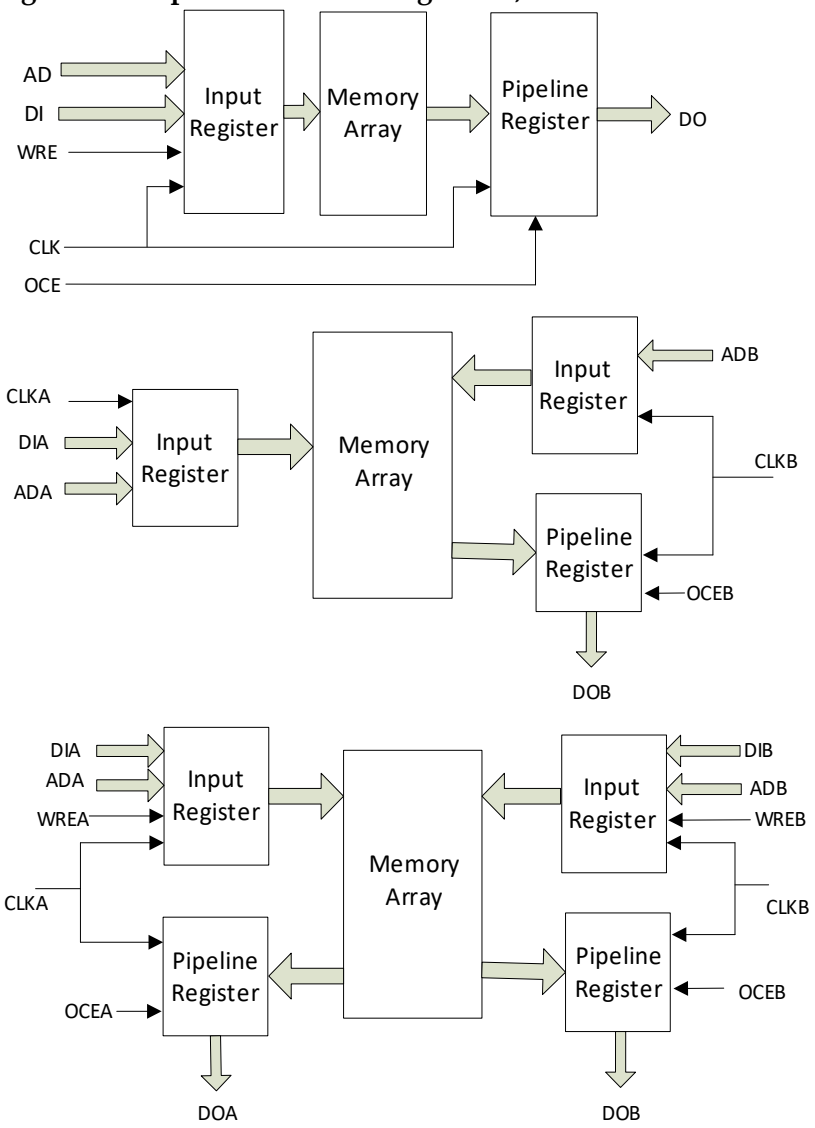
### Pipeline Mode

While writing in the BSRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

### Bypass Mode

The output register is not used. The data is kept in the output of the memory array.

**Figure 3-28 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port**




## Write Mode

#### NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

#### WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

#### READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory aCCIOrding to the address. The original data in this address will appear at the output of this port.

## 3.4.8 Clock Operations

Table 3-6 lists the clock operations in different BSRAM modes:

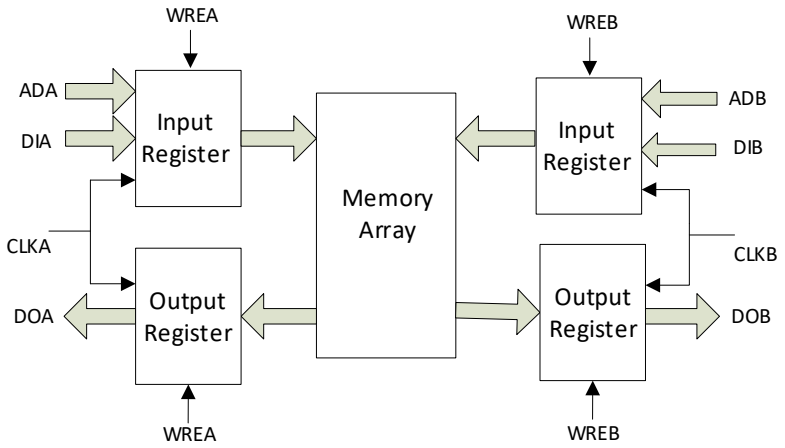
**Table 3-6 Clock Operations in Different BSRAM Modes**

| Clock Operations | Dual Port Mode | Semi-Dual Port Mode | Single Port Mode |
|---|---|---|---|
| Independent Clock Mode | Yes | No | No |
| Read/Write Clock Mode | Yes | Yes | No |
| Single Port Clock Mode | No | No | Yes |

### Independent Clock Mode

Figure 3-29 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

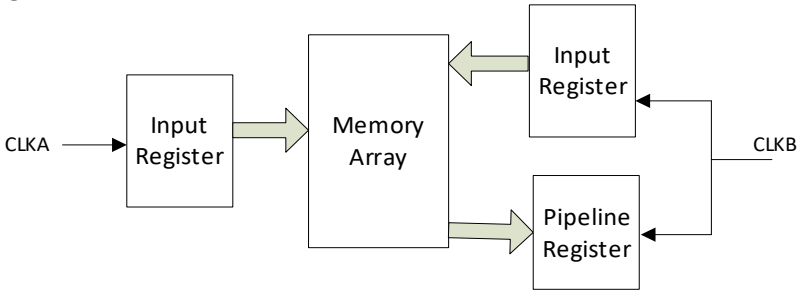
**Figure 3-29 Independent Clock Mode**




### Read/Write Clock Operation

Figure 3-30 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

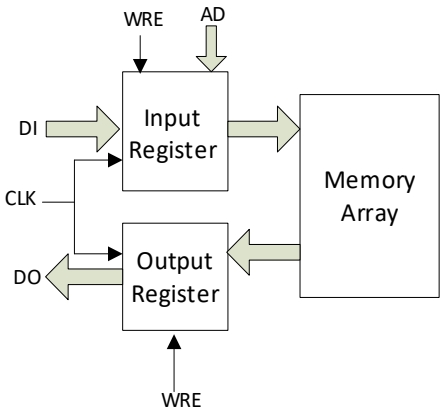
**Figure 3-30 Read/Write Clock Mode**



### Single Port Clock Mode

Figure 3-31 shows the clock operation in single port mode.

**Figure 3-31 Single Port Clock Mode**




# 3.5 DSP

## 3.5.1 Introduction

The GW2A series of FPGA products have abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

### Macro

DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one 3 input ALU.

Figure 3-32 shows the structure of one Macro:

**Figure 3-32 DSP Macro**

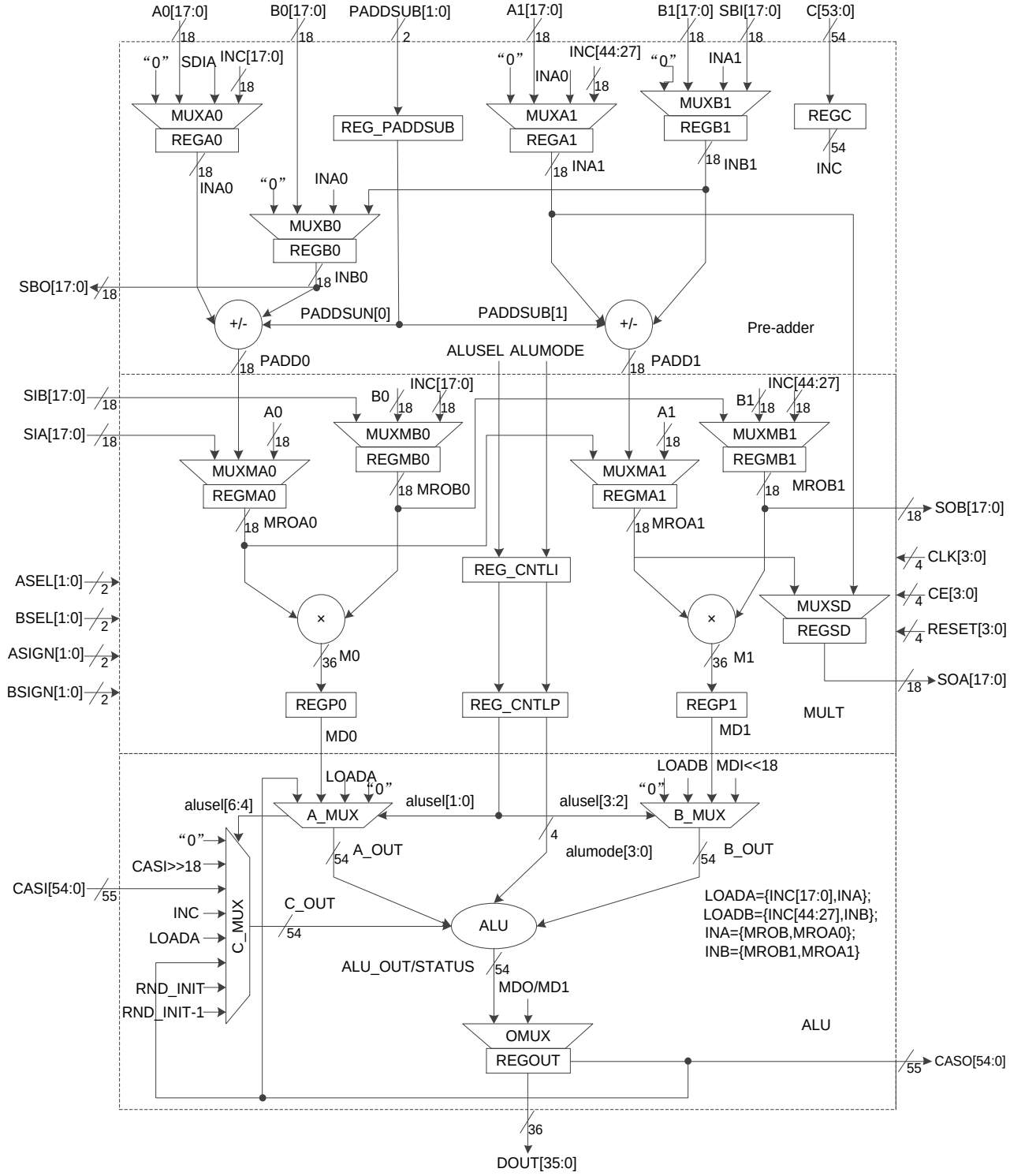



Table 3-7 shows DSP ports description.

Table 3-8 shows internal registers.

**Table 3-7 DSP Ports Description**

| Port Name | I/O | Description |
|---|---|---|
| A0[17:0] | I | 18-bit data input A0 |
| B0[17:0] | I | 18-bit data input B0 |
| A1[17:0] | I | 18-bit data input A1 |
| B1[17:0] | I | 18-bit data input B1 |

| Port Name | I/O | Description |
|---|---|---|
| C[53:0] | I | 54-bit data input C |
| SIA[17:0] | I | Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle. |
| SIB[17:0] | I | Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle. |
| SBI[17:0] | I | Pre- adder logic shift input, backward direction. |
| CASI[54:0] | I | ALU input from previous DSP block, used for cascade connection. |
| PADDSI0[1:0] | I | Source select for Multiplier or pre-adder input A |
| BSEL[1:0] | I | Source select for Multiplier input B |
| ASIGN[1:0] | I | Sign bit for input A |
| BSIGN[1:0] | I | Sign bit for input B |
| PADDSUB[1:0] | I | Operation control signals of pre-adder, used for pre-adder logic add/subtract selection |
| CLK[3:0] | I | Clock input |
| CE[3:0] | I | Clock Enable |
| RESET[3:0] | I | Reset input, synchronous or asynchronous |
| SOA[17:0] | O | Shift data output A |
| SOB[17:0] | O | Shift data output B |
| SBO[17:0] | O | Pre- adder logic shift output, backward direction. |
| DOUT[35:0] | O | DSP output data |
| CASO[54:0] | O | ALU output to next DSP block for cascade connection, the highest bit is sign-extended. |

**Table 3-8 Internal Registers Description**

| Register | Description and Associated Attributes |
|---|---|
| A0 register | Registers for A0 input |
| A1 register | Registers for A1 input |
| B0 register | Registers for B0 input |
| B1 register | Registers for B1 input |
| C register | C register |
| P1_A0 register | Registers for A0 input of left multiplier |
| P1_A1 register | Registers for A1 input of right multiplier |
| P1_B0 register | Registers for B0 input of left multiplier |
| P1_B1 register | Registers for B1 input of right multiplier |
| P2_0 register | Registers for pipeline of left multiplier |
| P2_1 register | Registers for pipeline of right multiplier |
| OUT register | Registers for DOUT output |
| OPMODE register | Registers for operation mode control |
| SOA register | Registers for shift output at port SOA |

### PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs.,

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.
  Each input end supports pipeline mode and bypass mode.
  GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

**MULT**

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Pipeline Mode and Bypass Mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two adjacent DSP macros can form a 36 x 36 multiplier.

**ALU**

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The registered and bypass mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

## 3.5.2 DSP Operations

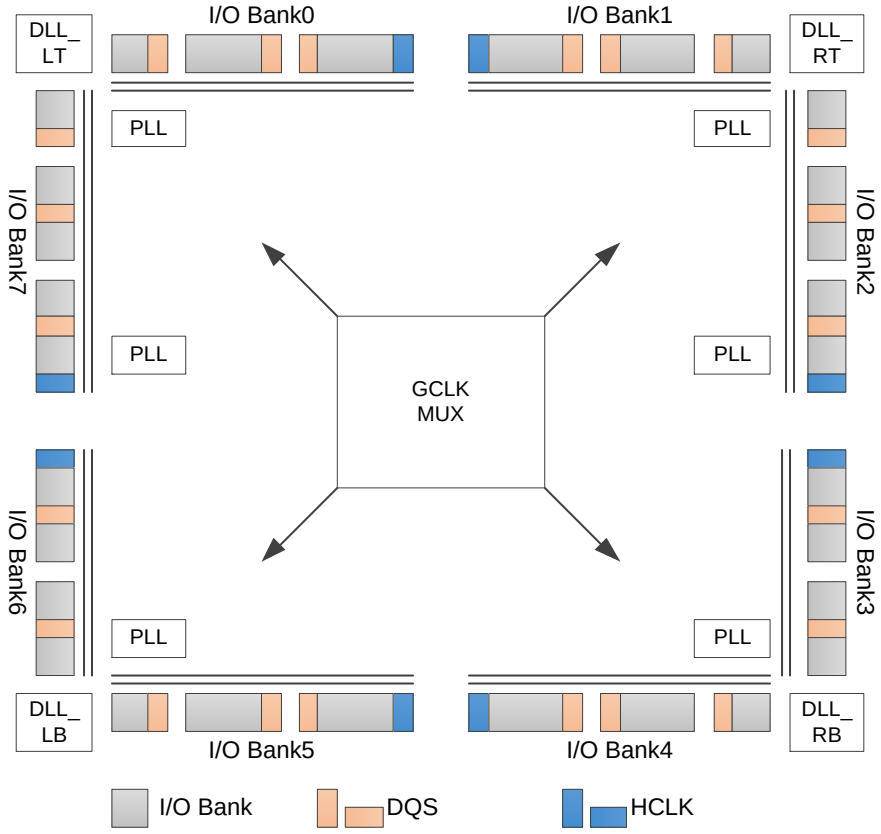
Based on ALUSEL [6:0] and ALUMODE [3:0], DSP can be configured as different operation modes: Operation Mode:

- Multiplier
- Accumulator
- MULTADDALU

# 3.6 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2A series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW2A series of FPGA products provide PLL, high speed clock HCLK, DDR memory interface, DQS, etc.

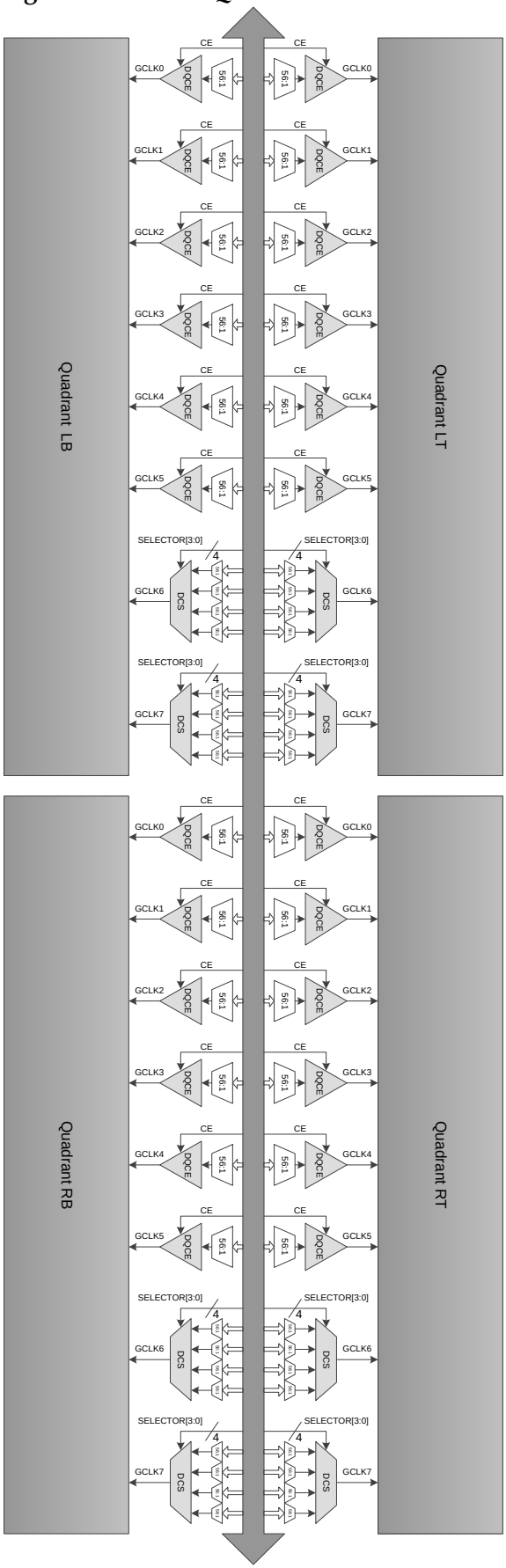
**Figure 3-33 GW2A Clock Resources**




## 3.6.1 Global Clock

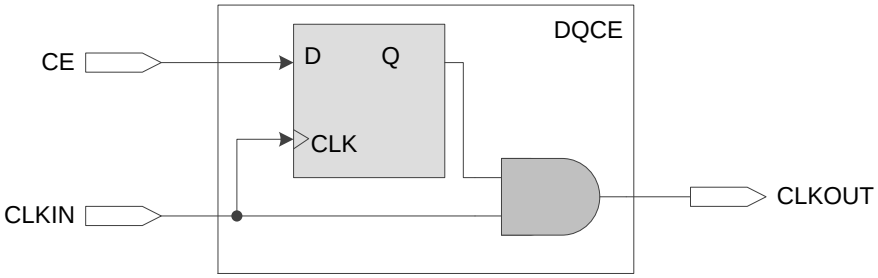
GCLK is distributed in the GW2A devices as four quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

**Figure 3-34 GCLK Quadrant Distribution**



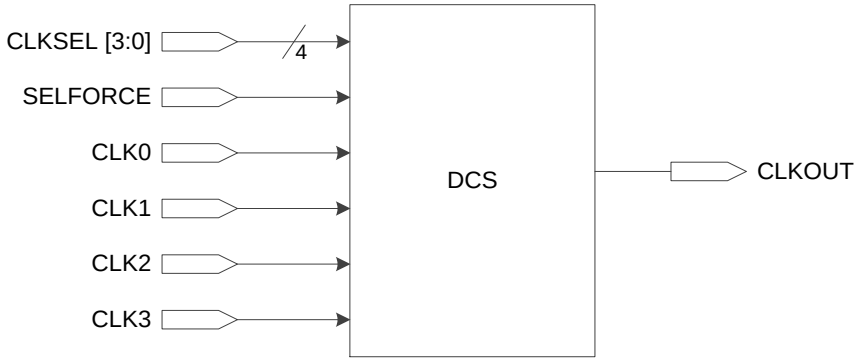
GCLK0~GCLK5 can be turned on or off by Dynamic Quadrant Clock Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

**Figure 3-35 DQCE Concept**




GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-36. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

**Figure 3-36 DCS Concept**

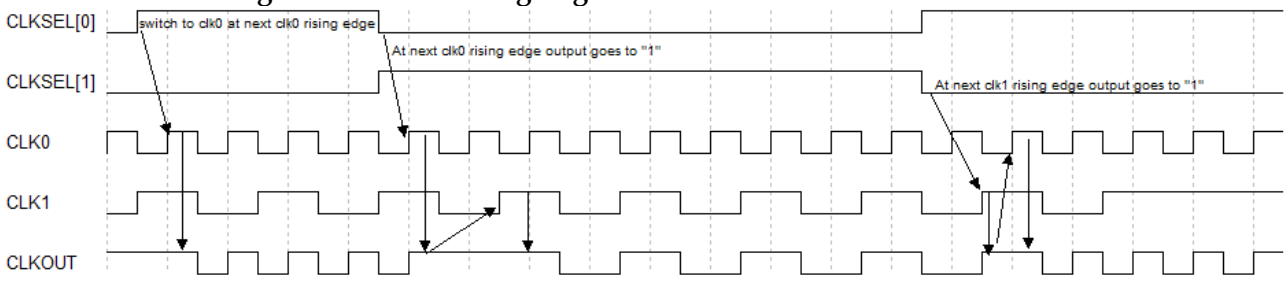



DCS can be configured in the following modes:

- DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-37.

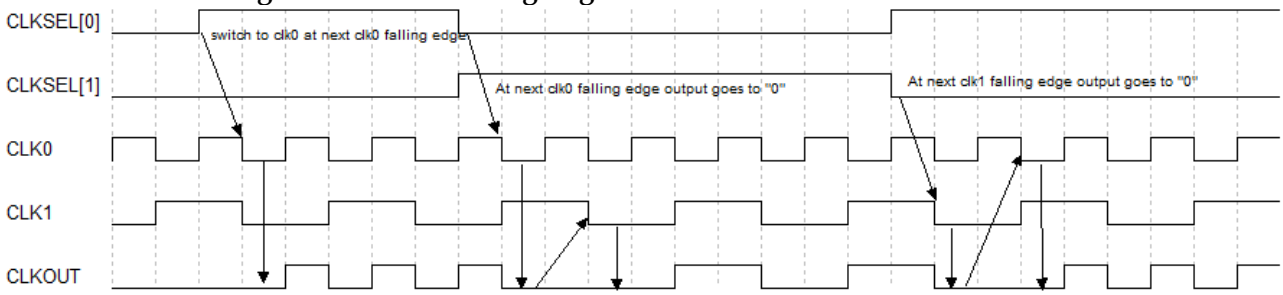
**Figure 3-37 DCS Rising Edge**




- DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-38.

**Figure 3-38 DCS Falling Edge**




- Clock Buffer Mode

In this mode, DCS acts as a clock buffer.

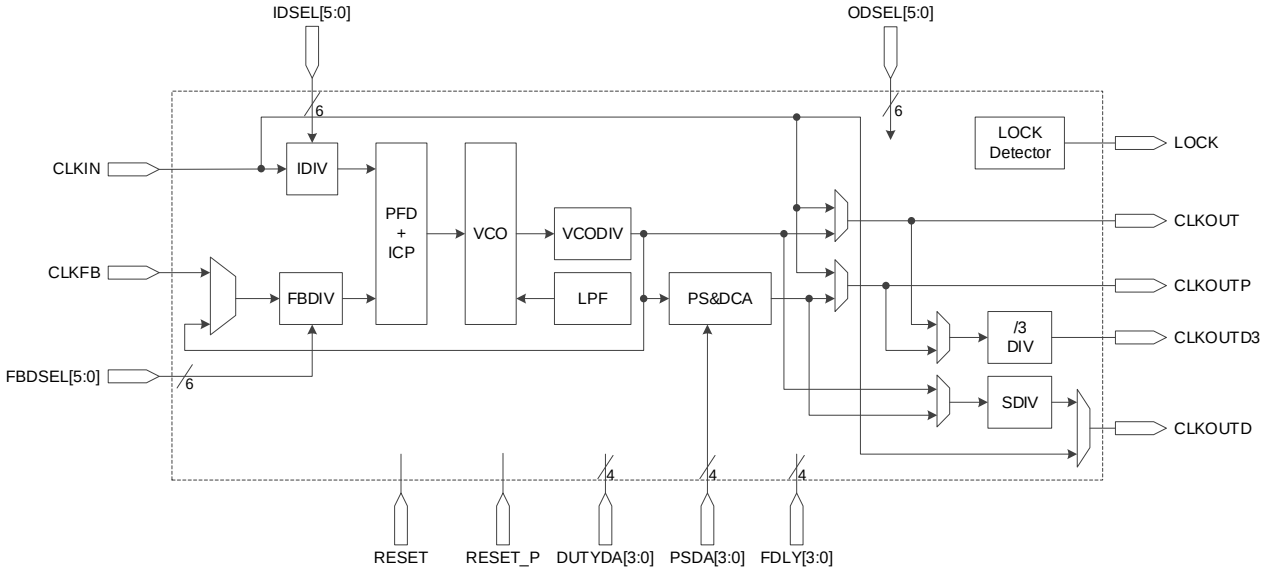
## 3.6.2 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks in the GW2A series of FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-39 for the PLL structure.

**Figure 3-39 PLL Structure**




See Table 3-9 for a definition of the PLL ports.

**Table 3-9 PLL Ports Definition**

| Port Name | Signal | Description |
|---|---|---|
| CLKIN [5:0] | I | Reference clock input |
| CLKFB | I | Feedback clock input |
| RESET | I | PLL reset |
| RESET_P | I | PLL Power Down |
| INSEL[2:0] | I | Dynamic clock control selector: 0~5 |

| Port Name | Signal | Description |
|---|---|---|
| IDSEL [5:0] | I | Dynamic IDIV control: 1~64 |
| FBDSEL [5:0] | I | Dynamic FBDIV control:1~64 |
| PSDA [3:0] | I | Dynamic phase control (rising edge effective) |
| DUTYDA [3:0] | I | Dynamic duty cycle control (falling edge effective) |
| FDLY[3:0] | I | CLKOUTP dynamic delay control |
| CLKOUT | O | Clock output with no phase and duty cycle adjustment |
| CLKOUTP | O | Clock output with phase and duty cycle adjustment |
| CLKOUTD | O | Clock divider from CLKOUT and CLKOUTP (controlled by SDIV) |
| CLKOUTD3 | O | clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3) |
| LOCK | O | PLL lock status: 1 locked, 0 unlocked |

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For further PLL features, please refer to 4.4.7 PLL Switching Characteristic.

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

- $f_{CLKOUT} = (f_{CLKIN} * FBDIV)/IDIV$
- $f_{VCO} = f_{CLKOUT} * ODIV$
- $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
- $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FBDIV$

**Note!**

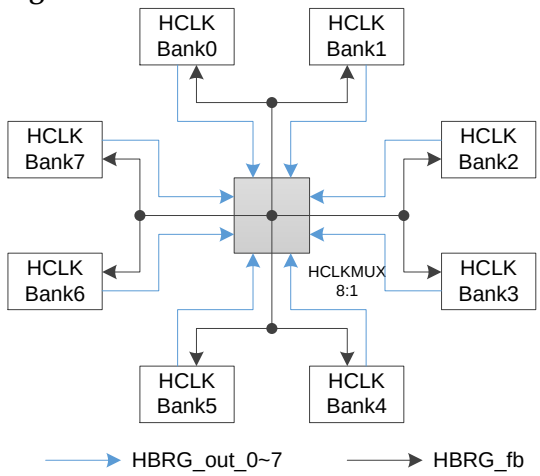
- $f_{CLKIN}$: The frequency of the input clock CLKIN
- $f_{CLKOUT}$: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- $f_{PFD}$: PFD Phase Comparison Frequency, and the minimum value of $f_{PFD}$ should be no less than $3\mathrm{MHz}$

Adjust IDIV, FBDIV, ODIV, and SDIV to achieve the required clock frequency.

### 3.6.3 HCLK

HCLK is the high-speed clock in the GW2A series FPGA products, which can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-40.

**Figure 3-40 GW2A HCLK Distribution**




As shown in Figure 3-40, there is an 8: 1 HCLKMUX module in the middle of the high-speed clock HCLK. HCLKMUX can send HCLK clock signal from any Bank to any other bank, which makes the use of HCLK more flexible.

HCLK can provide user with the function modules as follows:

- DHCEN: Dynamic high-speed clock enable module, functions similar to DQCE. Dynamically turn on / off high-speed clock signal.
- CLKDIV/ CLKDIV2: high-speed clock divider module, each bank has a CLKDIV. Generates a clock divided by the input clock phase, which is used in the IO logic mode.
- DCS: Dynamic High Speed Clock Selector.
- DLLDLY: The dynamic delay adjustment module, the clock signal for the dedicated clock pin input.

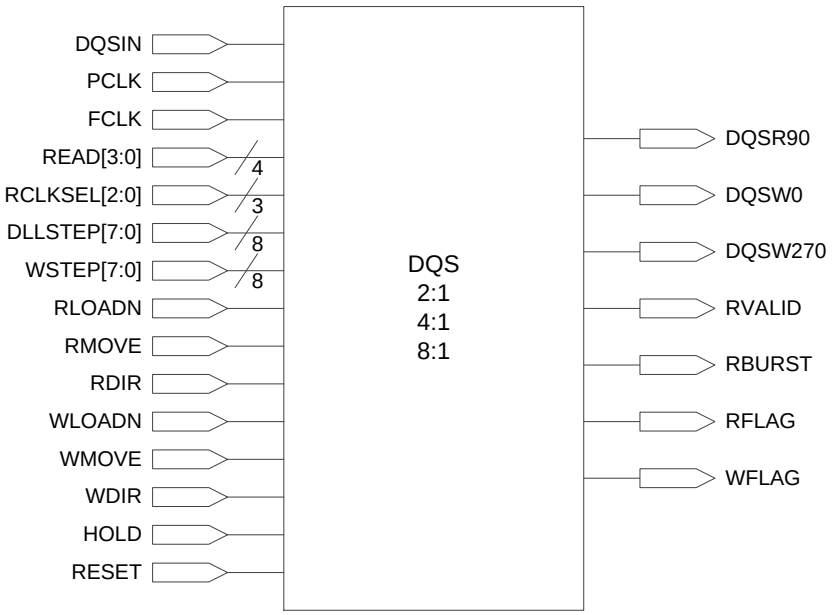
### 3.6.4 DDR Memory Interface Clock Management DQS

The DQS module of the GW2A series of FPGA products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module has three operating modes to meet the needs of different I/O interfaces, as shown in Figure 3-41.

**Figure 3-41 DQS**




**CDRCLKGEN**

CDRCLKGEN is used to support high-speed asynchronous input interfaces, such as SGMII. Each location has only one DQS and CDRCLKGEN.

**CDRCLKDIV**

The function of the clock divider module is similar to that of HCLKDIV.

# 3.7 Long Wire (LW)

As a supplement to the CRU, the GW2A series of FPGA products provide another routing resource - Long Wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

# 3.8 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW2A series of FPGA products. There is a direct connection to core logic. It can be used as asynchronous/synchronous set/reset. The registers in CFUs and I/Os can be individually configured to use GSR.

# 3.9 Programming Configuration

The GW2A series of FPGA products support SRAM. Each time the device is powered on, it needs to download the bit stream file to configure. Users can select to keep backup data in external Flash chip aCCIOrding to requirements. After power-up, the GW2A devices read configuration data

from external Flash into the SRAM.

Besides JTAG, the GW2A series of FPGA products also support GOWINSEMI's own configuration mode: GowinCONFIG (SSPI, MSPI, SERIAL, and CPU). For more detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide*.

# 3.10 On Chip Oscillator

There is an internal oscillator in each of the GW2A series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-10 for the output frequency. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formal is employed to get the output clock frequency:

$f_{out}$=250 MHz/Param

**Note!**

"Param" is the configuration parameter with a range of 2~128. It supports even number only.

**Table 3-10 Oscillator Output Frequency Options**

| Mode | Frequency | Mode | Frequency | Mode | Frequency |
|---|---|---|---|---|---|
| 0 | 2.5MHz[1] | 8 | 7.8MHz | 16 | 15.6MHz |
| 1 | 5.4MHz | 9 | 8.3MHz | 17 | 17.9MHz |
| 2 | 5.7MHz | 10 | 8.9MHz | 18 | 21MHz |
| 3 | 6.0MHz | 11 | 9.6MHz | 19 | 25MHz |
| 4 | 6.3MHz | 12 | 10.4MHz | 20 | 31.3MHz |
| 5 | 6.6MHz | 13 | 11.4MHz | 21 | 41.7MHz |
| 6 | 6.9MHz | 14 | 12.5MHz | 22 | 62.5MHz |
| 7 | 7.4MHz | 15 | 13.9MHz | 23 | 125MHz[2] |

**Note!**

- [1] Default Frequency is 2.5 MHz.
- [2] 125 MHz is not suitable for MSPI.

# 4 AC/DC Characteristic

**Note!**

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

## 4.1 Operating Conditions

### 4.1.1 Absolute Max. Ratings

**Table 4-1 Absolute Max. Ratings**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | Core voltage | -0.5V | 1.1V |
| $V_{CCPLL}$ | PLL Power | -0.5V | 1.1V |
| $V_{CCIO}$ | I/O Bank Power | -0.5V | 3.75V |
| $V_{CCX}$ | Auxiliary voltage | -0.5V | 3.75V |
| - | I/O Voltage Applied[1] | -0.5V | 3.75V |
| Storage Temperature | Storage Temperature | -65℃ | +150℃ |
| Junction Temperature (Industrial) | Junction Temperature | -40℃ | +125℃ |

**Note!**

[1] Overshoot and undershoot of –2 V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20 ns.

## 4.1.2 Recommended Operating Conditions

**Table 4-2 Recommended Operating Conditions**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | Core voltage. | 0.95V | 1.05V |
| $V_{CCPLLLx}$ | Left PLL power supply | 0.95V | 1.05V |
| $V_{CCPLLRx}$ | Right PLL power supply | 0.95V | 1.05V |
| $V_{CCIO}$ | I/O Bank Power | 1.14V | 3.6V |
| $V_{CCX}$ | Auxiliary voltage | 2.7V | 3.6V |
| $T_{JCOM}$ | Junction temperature of commercial operation | 0 ℃ | +85 ℃ |
| $T_{JIND}$ | Junction temperature of Industrial operation | -40 ℃ | +100 ℃ |

**Note!**

For the detailed recommended operating conditions for different packages, please refer to *UG110, GW2A-18 Pinout* and *UG113, GW2A-55 Pinout.*

## 4.1.3 Power Supply Ramp Rates

**Table 4-3 Power Supply Ramp Rates**

| Name | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| Vcc Ramp | Power supply ramp rates for Vcc | 0.1mV/μs | - | 10mV/μs |
| $V_{CCIO}$/Vccx Ramp | Power supply ramp rates for $V_{CCIO}$ and $V_{CCX}$ | 0.01mV/μs | - | 100mV/μs |

**Note!**

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

## 4.1.4 Hot Socket Specifications

**Table 4-4 Hot Socket Specifications**

| Name | Description | Condition | I/O | Max. |
|---|---|---|---|---|
| $I_{HS}$ | Input leakage current (Input or I/O leakage current) | $V_{IN}$=$V_{IL}$ (MAX) | I/O | 150uA |
| $I_{HS}$ | Input leakage current (Input or I/O leakage current) | $V_{IN}$=$V_{IL}$ (MAX) | TDI,TDO TMS,TCK | 120uA |

## 4.1.5 POR Specifications

**Table 4-5 POR Specifications**

| Name | Description | Device | Name | Value |
|---|---|---|---|---|
| $V_{POR\_UP}$ | Power on reset ramp up trip point | GW2A-18 | $V_{CC}$ | 0.8V |
| | | | $V_{CCX}$ | 2.45V |
| | | | $V_{CCIO}$ | 0.9V |
| | | GW2A-55 | $V_{CC}$ | 0.8V |
| | | | $V_{CCX}$ | 2.45V |

| Name | Description | Device | Name | Value |
|---|---|---|---|---|
| | | | $V_{CCIO}$ | 0.9V |
| $V_{POR\_DOWN}$ | Power on reset ramp down trip point | GW2A-18 | $V_{CC}$ | 0.7V |
| | | | $V_{CCX}$ | 2.2V |
| | | | $V_{CCIO}$ | 0.6V |
| | | GW2A-55 | $V_{CC}$ | 0.7V |
| | | | $V_{CCX}$ | 2.2V |
| | | | $V_{CCIO}$ | 0.65V |

# 4.2 ESD

**Table 4-6 GW2A ESD – HBM**

| Device | GW2A-18 | GW2A-55 |
|---|---|---|
| QN88 | HBM>1,000V | - |
| EQ144 | HBM>1,000V | - |
| MG196 | HBM>1,000V | - |
| PG256 | HBM>1,000V | - |
| PG256S | HBM>1,000V | - |
| PG256SF | HBM>1,000V | - |
| PG256C | HBM>1,000V | - |
| PG256CF | HBM>1,000V | - |
| PG256E | HBM>1,000V | - |
| PG484 | HBM>1,000V | HBM>1,000V |
| PG484C | HBM>1,000V | - |
| PG1156 | - | HBM>1,000V |
| UG324 | HBM>1,000V | HBM>1,000V |
| UG324D | - | HBM>1,000V |
| UG324F | - | HBM>1,000V |
| UG484 | HBM>1,000V | - |
| UG484S | - | HBM>1,000V |
| UG676 | - | HBM>1,000V |

**Table 4-7 GW2A ESD – CDM**

| Device | GW2A-18 | GW2A-55 |
|---|---|---|
| QN88 | CDM>500V | - |
| EQ144 | CDM>500V | - |
| MG196 | CDM>500V | - |
| PG256 | CDM>500V | - |
| PG256S | CDM>500V | - |
| PG256SF | CDM>500V | - |

| Device | GW2A-18 | GW2A-55 |
|---|---|---|
| PG256C | CDM>500V | - |
| PG256CF | CDM>500V | - |
| PG256E | CDM>500V | - |
| PG484 | CDM>500V | CDM>500V |
| PG484C | CDM>500V | - |
| PG1156 | - | CDM>500V |
| UG324 | CDM>500V | CDM>500V |
| UG324D | - | CDM>500V |
| UG324F | - | CDM>500V |
| UG484 | CDM>500V | - |
| UG484S | - | CDM>500V |
| UG676 | - | CDM>500V |

# 4.3 DC Electrical Characteristics

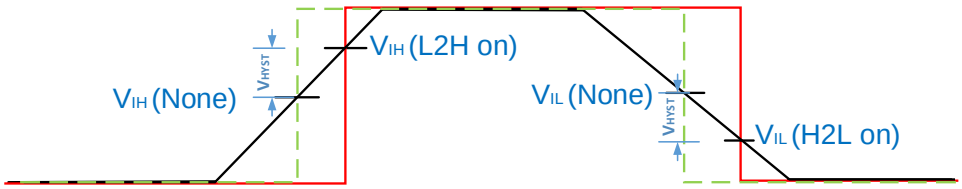
## 4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

**Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions**

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $I_{IL}$,$I_{IH}$ | Input or I/O leakage | $V_{CCIO}<V_{IN}<V_{IH}$(MAX) | - | - | 210μA |
| | | $0V<V_{IN}<V_{CCIO}$ | - | - | 10μA |
| $I_{PU}$ | I/O Active Pull-up Current | $0<V_{IN}<0.7V_{CCIO}$ | -30μA | - | -150μA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$(MAX)$<V_{IN}<V_{CCIO}$ | 30μA | - | 150μA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN}=V_{IL}$(MAX) | 30μA | - | - |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN}=0.7V_{CCIO}$ | -30μA | - | - |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0\leq V_{IN}\leq V_{CCIO}$ | - | - | 150μA |
| $I_{BHHO}$ | BusHoldHigh Overdrive Current | $0\leq V_{IN}\leq V_{CCIO}$ | - | - | -150μA |
| $V_{BHT}$ | Bus hold trip points | - | $V_{IL}$(MAX) | - | $V_{IH}$(MIN) |
| C1 | I/O Capacitance | - | - | 5pF | 8pF |
| $V_{HYST}$ | Hysteresis for | $V_{CCIO}$=3.3V, Hysteresis=L2H[1],[2] | - | 240mV | - |

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| | Schmitt Trigger inputs | $V_{CCIO}$=2.5V, Hysteresis=L2H | - | 140mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis=L2H | - | 65mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis=L2H | - | 30mV | - |
| | | $V_{CCIO}$=3.3V, Hysteresis=H2L[1],[2] | - | 200mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis=H2L | - | 130mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis=H2L | - | 60mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis=H2L | - | 40mV | - |
| | | $V_{CCIO}$=3.3V,Hysteresis=HIGH[1],[2] | - | 440mV | - |
| | | $V_{CCIO}$=2.5V,Hysteresis= HIGH | - | 270mV | - |
| | | $V_{CCIO}$=1.8V,Hysteresis= HIGH | - | 125mV | - |
| | | $V_{CCIO}$=1.5V,Hysteresis= HIGH | - | 70mV | - |

**Note!**

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising $V_{IH}$ by $V_{HYST}$; enabling the H2L (high to low) option means lowering $V_{IL}$ by $V_{HYST}$; enabling the HIGH option means enabling both L2H and H2L options, i.e. $V_{HYST}$(HIGH) = $V_{HYST}$(L2H) + $V_{HYST}$(L2H). The diagram is shown below.
- 


## 4.3.2 Static Supply Current

**Table 4-9 Static Supply Current**

| Name | Description | Device | Typ. |
|---|---|---|---|
| $I_{CC}$[1] | Core Current | GW2A-55[2] | 150mA |
| | | GW2A-18 | 70mA |
| $I_{CCX}$[2] | $V_{CCX}$ current | GW2A-55 | 35mA |
| | | GW2A-18 | 15mA |
| $I_{CCIO}$ | I/O Bank current ($V_{CCIO}$=3.3V) | GW2A-55 | <2mA |
| | | GW2A-18 | <2mA |

**Note!**

- [1] Tested with $V_{CC}$ =1V, room temperature, speed grade -8.
- [2] Tested with $V_{CCX}$=3.3V.

## 4.3.3 I/O Operating Conditions Recommended

**Table 4-10 I/O Operating Conditions Recommended**

| Name | Output $V_{CCIO}$ (V) | | | Input $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVTTL33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVCMOS33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | - | - | - |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | - | - | - |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | - | - | - |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | - | - | - |
| SSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| SSTL18_I | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL25_II | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL33_I | 3.135 | 3.3 | 3.6 | 1.3 | 1.5 | 1.7 |
| SSTL33_II | 3.135 | 3.3 | 3.6 | 1.3 | 1.5 | 1.7 |
| HSTL18_I | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL18_II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| PCI33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVPECL33E | 3.135 | 3.3 | 3.6 | - | - | - |
| MLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| BLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| RSDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| LVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL15D | 1.425 | 1.5 | 1.575 | - | - | - |
| SSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL25D_I | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL25D_II | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL33D_I | 3.135 | 3.3 | 3.6 | - | - | - |
| SSTL33D_II | 3.135 | 3.3 | 3.6 | - | - | - |
| HSTL15D | 1.425 | 1.575 | 1.89 | - | - | - |
| HSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| HSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |

**Note!**

It is recommended to set the $V_{CCIO}$ of the Bank using True LVDS to 2.5V.

## 4.3.4 IOB Single - Ended DC Electrical Characteristic

**Table 4-11 IOB Single - Ended DC Electrical Characteristic**

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| LVCMOS33 LVTTL33 | -0.3V | 0.8V | 2.0V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | | | 24 | -24 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS25 | -0.3V | 0.7V | 1.7V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS18 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS15 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS12 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 2 | -2 |
| | | | | | | | 4 | -4 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| PCI33 | -0.3V | 0.3 x $V_{CCIO}$ | 0.5 x $V_{CCIO}$ | 3.6V | 0.1 x $V_{CCIO}$ | 0.9 x $V_{CCIO}$ | 1.5 | -0.5 |
| SSTL33_I | -0.3V | $V_{REF}$-0.2V | $V_{REF}$+0.2V | 3.6V | 0.7 | $V_{CCIO}$-1.1V | 8 | -8 |
| SSTL25_I | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | 0.54V | $V_{CCIO}$-0.62 V | 8 | -8 |
| SSTL25_II | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | NA | NA | NA | NA |
| SSTL18_II | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125 V | 3.6V | NA | NA | NA | NA |
| SSTL18_I | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125 V | 3.6V | 0.40V | $V_{CCIO}$-0.40 V | 8 | -8 |
| SSTL15 | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40 V | 8 | -8 |
| HSTL18_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40 V | 8 | -8 |
| HSTL18_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | NA | NA | NA | NA |
| HSTL15_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40 V | 8 | -8 |

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| HSTL15_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | NA | NA | NA | NA |

**Note!**

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

## 4.3.5 IOB Differential Electrical Characteristics

**Table 4-12 IOB Differential Electrical Characteristics**

LVDS

| Name | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{INA}$,$V_{INB}$ | Input Voltage | - | 0 | - | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage | - | 0.05 | - | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Minimum Input Swing | ±100 | - | ±600 | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | - | - | ±10 | µA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100Ω | - | - | 1.6 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100Ω | 0.9 | - | - | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$=100Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Between High and Low | - | - | - | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$=100Ω | 1.125 | 1.2 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between High and Low | - | - | - | 50 | mV |
| $I_S$ | Short-circuit current | $V_{OD}$ = 0V, output short-circuit | - | - | 15 | mA |

# 4.4 Switching Characteristics

## 4.4.1 CFU Switching Characteristics

**Table 4-13 CFU Block Internal Timing Parameters**

| Device | Name | Description | C9/I8 | | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| GW2A-18 | $t_{LUT4\_CFU}$ | LUT4 delay | 0.27 | 0.40 | 0.31 | 0.46 | 0.39 | 0.58 | ns |
| | $t_{SR\_CFU}$ | Set/Reset to Register output | 0.95 | 0.99 | 1.10 | 1.15 | 1.37 | 1.44 | ns |
| | $t_{CO\_CFU}$ | Clock to Register output | 0.17 | 0.20 | 0.20 | 0.23 | 0.25 | 0.29 | ns |
| GW2A-55 | $t_{LUT4\_CFU}$ | LUT4 delay | 0.27 | 0.40 | 0.31 | 0.46 | 0.39 | 0.58 | ns |
| | $t_{SR\_CFU}$ | Set/Reset to Register output | 0.95 | 0.99 | 1.10 | 1.15 | 1.37 | 1.44 | ns |
| | $t_{CO\_CFU}$ | Clock to Register output | 0.17 | 0.20 | 0.20 | 0.23 | 0.25 | 0.29 | ns |

## 4.4.2 BSRAM Internal Timing Parameters

**Table 4-14 BSRAM Internal Timing Parameters**

| Device | Name | Description | C9/I8 | | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| GW2A-18 | $t_{COAD\_BSRAM}$ | Clock to output from read address/data | 1.95 | 1.95 | 2.26 | 2.26 | 2.83 | 2.83 | ns |
| | $t_{COOR\_BSRAM}$ | Clock to output from output register | 0.26 | 0.26 | 0.31 | 0.31 | 0.38 | 0.38 | ns |
| GW2A-55 | $t_{COAD\_BSRAM}$ | Clock to output from read address/data | 1.95 | 1.95 | 2.26 | 2.26 | 2.83 | 2.83 | ns |
| | $t_{COOR\_BSRAM}$ | Clock to output from output register | 0.26 | 0.26 | 0.31 | 0.31 | 0.38 | 0.38 | ns |

## 4.4.3 DSP Internal Timing Parameters

**Table 4-15 DSP Internal Timing Parameters**

| Device | Name | Description | C9/I8 | | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| GW2A-18 | $t_{COIR\_DSP}$ | Clock to output from input register | 0.20 | 0.22 | 0.24 | 0.25 | 0.30 | 0.32 | ns |
| | $t_{COPR\_DSP}$ | Clock to output from pipeline register | 0.06 | 0.07 | 0.07 | 0.08 | 0.09 | 0.10 | ns |
| | $t_{COOR\_DSP}$ | Clock to output from output register | 0.03 | 0.04 | 0.04 | 0.04 | 0.05 | 0.05 | ns |
| GW2A-55 | $t_{COIR\_DSP}$ | Clock to output from input register | 0.20 | 0.22 | 0.24 | 0.25 | 0.30 | 0.32 | ns |
| | $t_{COPR\_DSP}$ | Clock to output from pipeline register | 0.06 | 0.07 | 0.07 | 0.08 | 0.09 | 0.10 | ns |
| | $t_{COOR\_DSP}$ | Clock to output from output register | 0.03 | 0.04 | 0.04 | 0.04 | 0.05 | 0.05 | ns |

## 4.4.4 Gearbox Switching Characteristics

**Table 4-16 Gearbox Internal Timing Parameters**

TBD

## 4.4.5 Clock and I/O Switching Characteristics

**Table 4-17 External Switching Characteristics**

| Device | Name | Description | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| GW2A-18 | Pin-LUT-Pin Delay[1] | Pin(IOxA) to Pin(IOxB) delay | - | 3.83 | - | 4.59 | ns |
| | $T_{HCLKdly}$ | HCLK tree delay | - | 0.82 | - | 0.98 | ns |

| Device | Name | Description | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| | $T_{GCLKdly}$ | GCLK tree delay | - | 1.77 | - | 2.12 | ns |
| GW2A-55 | Pin-LUT-Pin Delay[1] | Pin(IOxA) to Pin(IOxB) delay | - | 3.83 | - | 4.59 | ns |
| | $T_{HCLKdly}$ | HCLK tree delay | - | 1.32 | - | 1.48 | ns |
| | $T_{GCLKdly}$ | GCLK tree delay | - | 2.27 | - | 2.62 | ns |

**Note!**

[1] Tested with $V_{CCIO}$=3.3V, $V_{CCX}$ = 3.3V, LVCMOS33, 8mA, 15pF load.

**Table 4-18 I/O Regiter Parameters Using Dedicated GCLK Input through GCLK Tree without PLL**

| Device | Name | Description | C8/I7 | | C7/I6 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| GW2A-18 | $T_{SU}$ | clock to data setup( using GPIO input register) | -1.5 | - | -1.6 | - | ns |
| | $T_H$ | clock to data hold( using GPIO input register) | 2.5 | - | 2.9 | - | ns |
| | $T_{SU\_DEL}$ | clock to data setup( using GPIO input register, with IODELAY enabled and Tap = 0) | -1.1 | - | -1.2 | - | ns |
| | $T_{H\_DEL}$ | clock to data hold( using GPIO input register, with IODELAY enabled and Tap = 0) | 2.1 | - | 2.5 | - | ns |
| GW2A-55 | $T_{SU}$ | clock to data setup( using GPIO input register) | -1 | - | -1.1 | - | ns |
| | $T_H$ | clock to data hold( using GPIO input register) | 2 | - | 2.4 | - | ns |
| | $T_{SU\_DEL}$ | clock to data setup( using GPIO input register, with IODELAY enabled and Tap = 0) | -0.6 | - | -0.7 | - | ns |
| | $T_{H\_DEL}$ | clock to data hold( using GPIO input register,with IODELAY enabled and Tap = 0) | 1.6 | - | 2 | - | ns |

**Note!**

The values in this table are based on LVCMOS33, 8mA, 15pF load.

### 4.4.6 On chip Oscillator Output Frequency

**Table 4-19 On chip Oscillator Output Frequency**

| Name | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency(0 to+ 85℃) | 106.25MHz | 125MHz | 143.75MHz |
| | Output Frequency (-40 to +100℃) | 100MHz | 125MHz | 150MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43% | 50% | 57% |
| $t_{OPJIT}$ | Output Clock Period Jitter | 0.01UIPP | 0.012UIPP | 0.02UIPP |

### 4.4.7 PLL Switching Characteristic

**Table 4-20 PLL Switching Characteristic**

| Device | Speed Grade | Name | Min. | Max. |
|---|---|---|---|---|
| GW2A-18 | -9/-8/-7 | CLKIN | 3MHz | 500MHz |
| | | PFD | 3MHz | 500MHz |
| | | VCO | 500MHz | 1250MHz |
| | | CLKOUT | 3.90625MHz | 625MHz |
| | -6 | CLKIN | 3MHz | 400MHz |
| | | PFD | 3MHz | 400MHz |
| | | VCO | 400MHz | 1000MHz |
| | | CLKOUT | 3.125MHz | 500MHz |
| GW2A-55 | -9/-8/-7 | CLKIN | 3MHz | 500MHz |
| | | PFD | 3MHz | 500MHz |
| | | VCO | 500MHz | 1250MHz |
| | | CLKOUT | 3.90625MHz | 625MHz |
| | -6 | CLKIN | 3MHz | 400MHz |
| | | PFD | 3MHz | 400MHz |
| | | VCO | 400MHz | 1000MHz |
| | | CLKOUT | 3.125MHz | 500MHz |

## 4.5 Configuration Interface Timing Specification

The GW2A series of FPGA products GowinCONFIG support the following configuration modes: MSPI, SSPI, CPU, and SERIAL. For detailed information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

# 5 Ordering Information

## 5.1 Part Name

**Figure 5-1 Part Naming Example– ES**

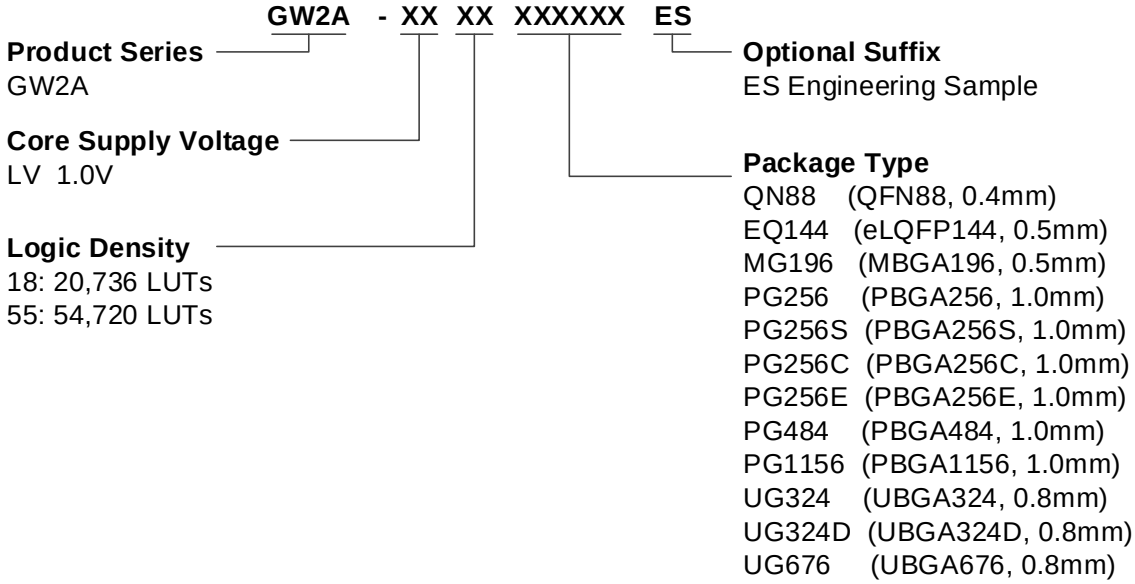
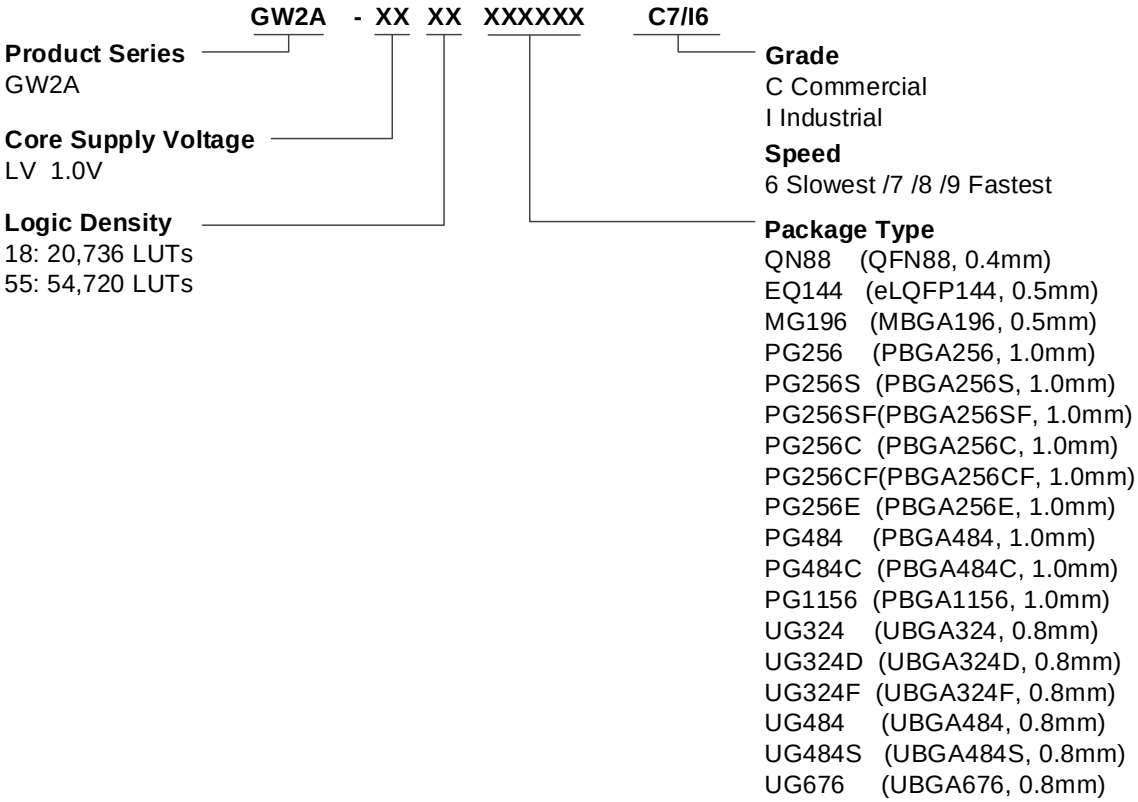


**Figure 5-2 Part Naming Example– Production**



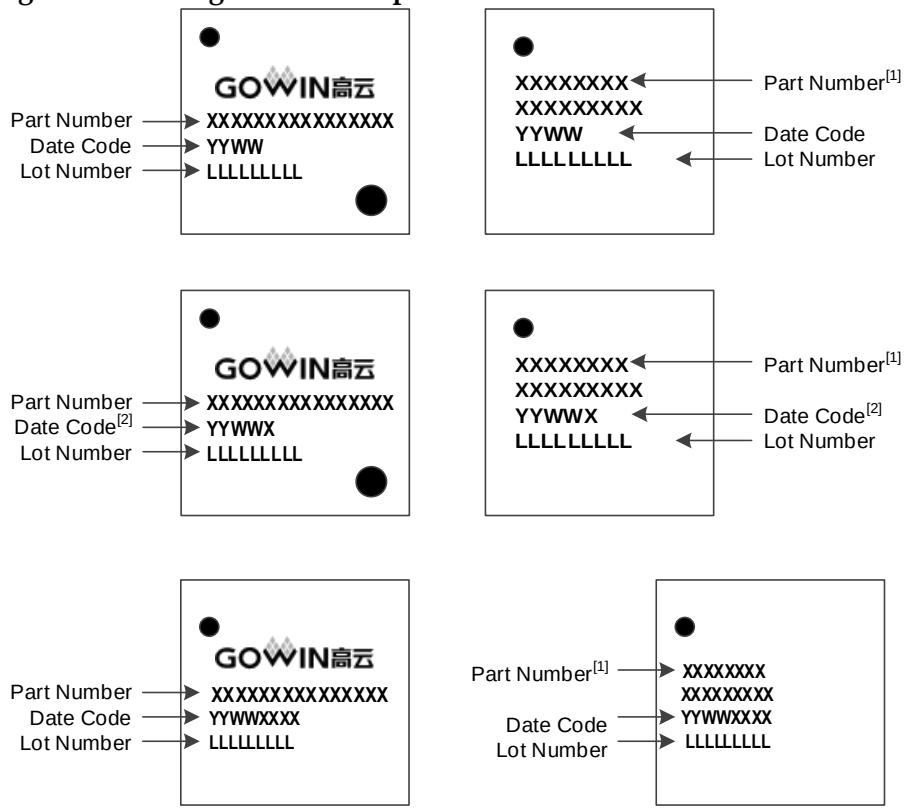

**Note!**

- For further information of Package type and pin number, please refer to 2.2 Product Resources.
- The LittleBee® family devices and Arora family devices of the same speed grade may have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one same device. GOWIN devices are screened using industrial standards, so one device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets the speed grade 7 in commercial grade applications, its speed grade is 6 in industrial grade applications.

# 5.2 Package Mark Example

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

**Figure 5-3 Package Mark Example**




**Note!**

- [1] The first two lines in the right figure(s) above are both the “Part Number”.
- [2] The Date Code followed by an “X” is for X version devices.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