

Quartus® Prime Pro Edition User Guide

Getting Started

Updated for Quartus® Prime Design Suite: **24.1**

This document is part of a collection - [Quartus® Prime Pro Edition User Guides - Combined PDF link](#)

Answers to Top FAQs:

- Q What do I need for FPGA design?**
A [FPGA Basic Design Prerequisites](#) on page 10
- Q What do I need to download to use Quartus?**
A [Intel FPGA Design Software for Download](#) on page 5
- Q Which Quartus version should I use?**
A [Quartus Design Suite Overview](#) on page 5
- Q How do I setup a project?**
A [Select a Starting Point for Your Project](#) on page 22
- Q Do you have an example design to start with?**
A [Start a Project from a Design Example](#) on page 24
- Q Does Quartus work with my other tools?**
A [Integrate Other EDA Tools](#) on page 99
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- Q How do I migrate an old project?**
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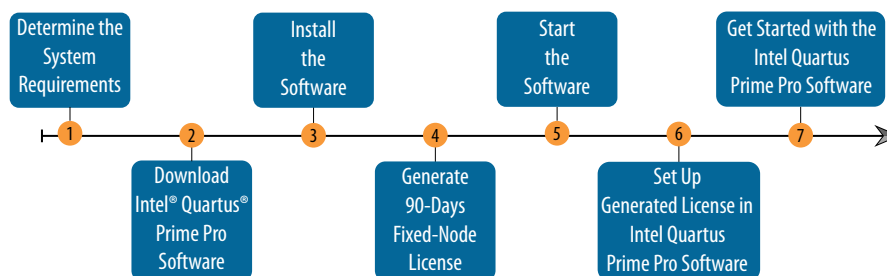
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1. Introduction to Quartus® Prime Pro Edition

This user guide describes basic concepts, files, and design flow of the Quartus® Prime Pro Edition software, including initial design planning considerations, selecting a starting point to set up your Quartus Prime Pro Edition project and managing those projects and working with intellectual property (IP).

The Quartus Prime design suite is a comprehensive development platform to design with Intel FPGAs⁽¹⁾, from design entry and synthesis to optimization, verification, simulation, and binary generation. The Quartus Prime software supports fast design processing, straightforward device programming, and integration with other industry-standard EDA tools. The user interface makes it easy for you to focus on your design—not on the design tool. The modular compiler streamlines the FPGA development process and ensures the highest performance for the least effort.


Quartus Prime Pro Edition Software Quick Start Steps



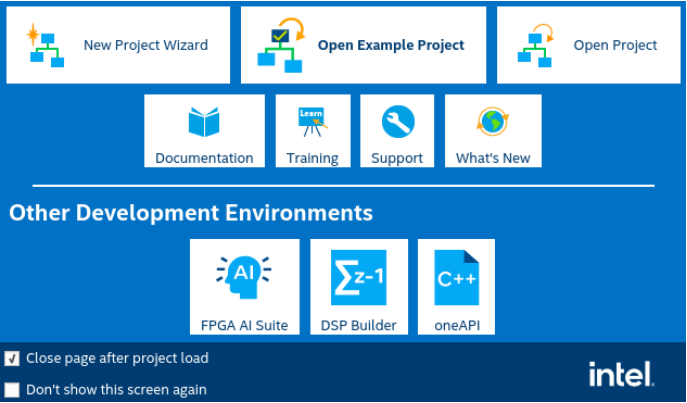
⁽¹⁾ A field-programmable gate array (FPGA) is a specialized integrated circuit that you can customize and reconfigure multiple times. To learn about and select a target Intel FPGA device family, refer to <https://www.intel.com/content/www/us/en/products/details/fpga.html>.

Use the following links to get started with the Quartus Prime Pro Edition software:

Table 1. Quartus Prime Pro Edition Software Quick Start Steps

Step		Useful Links
Determine the System Requirements	Verify hardware and software requirements and review Quartus Prime Pro Edition software release notes.	<ul style="list-style-type: none"> • Reviewing the Quartus Prime Installer Software Release Notes • Determining Hardware Requirements • Determining Software Requirements
Download the software	Download the latest Quartus Prime Pro Edition software.	<ul style="list-style-type: none"> • Quartus Prime Design Software Download Page • FPGA Software Download Center • Downloading Software Using the Quartus Prime Installer or Quartus Prime Installer (GUI mode) • Downloading Software Packages Manually
Install the software	Install the latest Quartus Prime Pro Edition software.	<ul style="list-style-type: none"> • Quartus Prime Installer (GUI mode) or Installing Intel® FPGA Software Through Quartus Prime Installer • Installing the Intel FPGA Software Manually • Setting Quartus Prime Environment Variables
Generate 90-days Fixed-node License	Generate 90- days free license in Intel FPGA Self-Service Licensing Center (SSLC).	<ul style="list-style-type: none"> • Intel FPGA Self-Service Licensing Center • Intel FPGA SSLC No-cost/Evaluation License Setup • Setting up Intel FPGA SSLC No-cost/Evaluation License
Start the software	<p>On Windows: Use one of the following options:</p> <ul style="list-style-type: none"> • On the desktop, double-click the Intel FPGA software icon.  <ul style="list-style-type: none"> • Click Start > All Programs > Intel FPGA <Version> Pro Edition > Quartus (Quartus Prime Pro <Version>) • At the command prompt, type: <code><installation-directory>\bin64\quartus</code> <p>On Linux:</p> <ul style="list-style-type: none"> • At the command prompt, type: <code><installation-directory>/quartus/bin/quartus</code> 	Starting the Quartus Prime Software
Set up the generated license in the Quartus Prime Pro Edition software	In the Quartus Prime Pro Edition software, click Tools > License Setup , browse and select the license file, and click OK .	<ul style="list-style-type: none"> • Intel FPGA Self-Service Licensing Center (SSLC) • Setting up Intel FPGA SSLC No-cost/Evaluation License • Summary of Intel FPGA Software Licenses Required • Licensing Intel FPGA Software Walkthrough


continued...

Step	Useful Links	
Quartus Prime Software Home Page	<p>Main page of the Quartus Prime software.</p> 	
Plan FPGA Design for RTL Flow	Planning for RTL flow is an essential step for advanced FPGA design. Determining your design priorities early on helps you to choose the best device, tools, features, and methodologies for your design.	Plan FPGA Design for RTL Flow
Create your FPGA project	The Quartus Prime software makes it easy for you to quickly setup a new FPGA design project.	Creating a New FPGA Design Project on page 22

Quartus Prime Software Editions

The Quartus Prime Software is available in three editions based on your design requirements:

Table 2. Quartus Prime Software Editions

	Pro Edition	Standard Edition	Lite Edition
	<p>Optimized to support the advanced features in Intel FPGAs and SoCs with the following device families:</p> <ul style="list-style-type: none"> Agilex™ 5 Agilex 7 Stratix® 10 Arria® 10 Cyclone® 10 GX 	<p>Includes extensive support for earlier device families in addition to the following device families:</p> <ul style="list-style-type: none"> Cyclone 10 LP MAX® 10 	<p>An ideal entry point to Intel's high-volume device families and is available as a free download with no license file required.</p>

Supported Features

The following is the Quartus Prime feature support matrix:

Figure 2. Quartus Prime Feature Support Matrix

Software Features	Intel Quartus® Prime Pro Edition	Intel Quartus® Prime Standard Edition
Intel Agilex® 5 Device Support	✓	
Intel Agilex® 7 Device Support	✓	
Intel Stratix® 10 Device Support	✓	
New Hybrid Placer & Global Router	✓	✓
New Timing Analyzer	✓	✓
New Physical Synthesis	✓	✓
Platform Designer (formerly Qsys)	✓	✓
Partial Reconfiguration	✓	
Block-Based (Hierarchical) Design Flows	✓	
Interface Planner (formerly BluePrint)	✓	
Incremental Fitter Optimization	✓	

The following features are only available in the Quartus Prime Pro Edition software:

Table 3. Supported Features of the Quartus Prime Pro Edition Software

Feature	Description
Hyper-Aware Design Flow	Use Hyper-Retiming to reach the highest performance in Agilex 5, Agilex 7, and Stratix 10 devices.
Advanced synthesis	Integrates new, stricter language parser supporting all major IEEE RTL languages, with enhanced algorithms, and parallel synthesis capabilities, and support for SystemVerilog 2009.
Hierarchical project structure	Preserves individual post-synthesis, post-placement, and post-place and route results for design instances. Optimizes without impacting other partition placement or routing.
Incremental Fitter Optimizations	Run and optimize Fitter stages incrementally. Each Fitter stage generates detailed reports.
Faster, more accurate I/O placement	Plan interface I/O in Interface Planner.
Platform Designer (Pro)	Builds on the system design and custom IP integration capabilities of Platform Designer (Standard). Platform Designer (Pro) introduces hierarchical isolation between system interconnect and IP components.
Block-Based Design Flows	Preserve and reuse design blocks at various stages of compilation.

Quartus Prime Pro Edition software does not support the following Quartus Prime Standard Edition features:

- I/O Timing Analysis
- NativeLink third party tool integration (other third-party tool integration available)
- Video and Image Processing Suite IP Cores
- Talkback features
- Various register merging and duplication settings
- Saving a node-level netlist as .vqm or RTL to schematic conversion

Supported Intel FPGA Developmental Tools

The Quartus Prime software suite supports the following Intel FPGA development tools:

Table 4. Intel FPGA Developmental Tools Supported by the Quartus Prime Software Suite

Tools	Description
Questa*-Intel FPGA Edition	Simulates FPGA designs using Intel-specific simulation libraries. It includes all features of Siemens EDA Questa* Core, including behavioral simulation, HDL test benches, and Tcl scripting.
Intel Advanced Link Analyzer	Analyzes jitter/noise and evaluates high-speed serial link performance. It is an ideal predesign tool supporting Intel FPGA IBIS-AMI standards and enhanced models to help you understand how Intel FPGA solutions can fit your system requirements.
Intel SoC FPGA Embedded Development Suite	A comprehensive tool suite for embedded software development on Intel SoC FPGAs.
Ashling* RiscFree* IDE for Intel FPGAs	Integrated development environment for creating embedded applications on the RISC-V-based Nios® V soft processors and the Arm*-based hard processor system.
Intel HLS Compiler	A high-level synthesis (HLS) tool that accepts untimed C++ code as an input and generates production-quality register transfer level (RTL) code optimized for Intel FPGAs. This tool accelerates verification time over RTL by raising the abstraction level for FPGA hardware design. Models developed in C++ have typically verified orders of magnitude faster than RTL.
DSP Builder for Intel FPGAs	Supports a model-based design flow from algorithms to hardware in a common environment.
Intel oneAPI Base Toolkit	Enables you to target FPGAs for heterogeneous acceleration and simulate entire system flows by abstracting some parts of the hardware.
Intel Simics® simulator for Intel FPGAs	A full-system simulator that supports defining, developing, and deploying virtual platforms.
FPGA AI Suite	Provides several components to help in enabling Artificial Intelligence (AI) and creating optimized Intel FPGA AI platforms efficiently.
Intel FPGA Power and Thermal Calculator	Estimates your design's power consumption and provides thermal design parameters for Intel FPGA devices, such as Agilex 5, Agilex 7, and Stratix 10.

1.1. Before You Begin

Before you get started with setting up your Quartus Prime Pro Edition project, review the following topics:

1.1.1. Prerequisite Knowledge and Training

Using the Quartus Prime software to create a basic FPGA design requires the following basic knowledge. There are several training modules available if you need help.

Prerequisite Knowledge

- Basic knowledge of digital logic design.
- Basic knowledge of how to describe a hardware design using VHDL, Verilog HDL, SystemVerilog, or EDA schematic tools.

Note: You can accelerate design creation and success by starting your design project from a pre-verified design example that targets an Intel FPGA development board, as [Creating a New Project from a Design Example](#) on page 24 describes.

Prerequisite Training

If you are new to FPGA or the Quartus Prime software, you can review the following training modules:

- [Read Me First!](#)
- [How to Begin a Simple FPGA Design](#)
- [University Self-Guided Lab: Become an FPGA Designer in 4 Hours](#)
- [Beginner Workshop for Intel FPGAs](#)
- [University Self-Guided Lab: Introduction to FPGAs and the Quartus Prime Software](#)
- [Basics of Programmable Logic: History of Digital Logic Design](#)
- [Basics of Programmable Logic: FPGA Architecture](#)
- [The Quartus Prime Software: Foundation \(Pro Edition\) \(Online Training\)](#)
- [Instructor-Led Training: Using Quartus Prime Software](#)
- [Using the Quartus Prime Standard Edition Software: An Introduction](#)
- [Verilog HDL Basics](#)
- [Verilog HDL Advanced](#)
- [VHDL Basics](#)
- [SystemVerilog with the Quartus Prime Software](#)
- [Introduction to Tcl Scripting](#)

Related Information

- [Intel FPGA Software Installation and Licensing](#)
- [FPGAs for Dummies eBook](#)

1.1.2. Navigate Content Through Tasks

Use the following navigation diagram to navigate this guide through user-tasks:

Table 6. Navigate Content Through Tasks

			
Plan FPGA Design for RTL Flow or Work With Intel FPGA IP Cores	Create a New Project or Migrate Your Existing Project to Quartus Prime Pro Edition Software	Manage Your Quartus Prime Pro Edition Projects	Review Next Steps

1.1.3. Acronyms

This document uses the following acronyms throughout:

Acronym	Meaning
ALR	Additional Logic Resources
DSE	Design Space Explorer
DSP	Digital Signal Processing
EDA	Electronic Design Automation
EDS	Embedded Design Suite
EPE	Early Power Estimator
FIFO	First In, First Out
FPGA	Field Programmable Gate Arrays
GUI	Graphical User Interface
HDL	Hardware Description Language
HTML	HyperText Markup Language
HPS	Hard Processor System
IEEE	Institute of Electrical and Electronics Engineers
IP	Intellectual Property
JTAG	Joint Test Action Group
LAB	Logic Array Block
LAI	Logic Analyzer Interface
MTBF	Mean Time Between Failures
PCB	Printed Circuit Board
PLD	Programmable Logic Devices
PLLs	Phase-Locked Loops
PTC	Power and Thermal Calculator
PVT	Process, Voltage, and Temperature
QSF	Quartus Settings File
continued...	

Acronym	Meaning
RAM	Random-Access Memory
RTL	Register-Transfer Level or Register-Transfer Logic
SDC	Synopsys* Design Constraints
Tcl	Tool Command Language
UART	Universal Asynchronous Receiver-Transmitter
VCS	Verilog Compiler and Simulator
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VPN	Virtual Private Network
VREF	Voltage Reference

2. Planning FPGA Design for RTL Flow

Navigating Content Through Tasks

Use the following navigation diagram to navigate this guide through user-tasks:



Planning for RTL flow is an essential step for advanced FPGA design. This chapter provides some useful tips and programming methods to consider in your planning process to help you detect and solve potential problems early in the design cycle. Determining your design priorities early on helps you to choose the best device, tools, features, and methodologies for your design.

Review the following topics to help you get started with the planning process:

2.1. Design Planning

Design planning is an essential step in advanced FPGA design. System architects must consider the target device characteristics in order to plan for interface I/O, integration of IP, on-chip debugging tools, and use of other EDA tools. Designers must consider device power consumption and programming methods when planning the layout. You can solve potential problems early in the design cycle by following the design planning considerations in this chapter.

By default, the Quartus Prime software optimizes designs for the best overall results. However, you can adjust settings to better optimize one aspect of your design, such as performance, routability, area, or power utilization. Consider your own design priorities and trade-offs when reviewing the techniques in this chapter. For example, certain device features, density, and performance requirements can increase system cost. Signal integrity and board issues can impact I/O pin locations. Power, timing performance, and area utilization all affect one another. Compilation time is affected when optimizing these priorities.

Determining your design priorities early on helps you to choose the best device, tools, features, and methodologies for your design.

Table 7. Checklist for Design Planning

Item	Considerations	Links
Create a design specification and test plan	<ul style="list-style-type: none"> • Create detailed design specifications that define the system. • Specify the I/O interfaces for the FPGA. • Identify the different clock domains. • Include a block diagram of basic design functions. • Create a test plan for verification and ease of manufacture. • Consider a common design directory structure or source control system to make design integration easy. • Consider whether you want to standardize on an interface protocol for each design block. 	
Planning for Target Device or Board	<ul style="list-style-type: none"> • Refer to the Product Selector tool to compare the specifications and features of Intel FPGA devices and development kits. • Refer to the device family documentation for detailed device characteristics. View a summary of each device's resources by selecting a device in the Device dialog box (Assignments > Device). • Consider whether the device family meets your design requirements for high-speed transceivers, global or regional clock networks, and the number of phase-locked loops (PLLs). • Consider the density requirements of your design. <ul style="list-style-type: none"> — Devices with more logic resources and higher I/O counts can implement larger and more complex designs, but at a higher cost. — Smaller devices use lower static power. — Select a device larger than what your design requires if you may want to add more logic later in the design cycle, or to reserve logic and memory for on-chip debugging. • Consider requirements for types of dedicated logic blocks, such as memory blocks of different sizes, or digital signal processing (DSP) blocks to implement certain arithmetic functions. • Alternatively, create a system that targets a specific development board to accelerate the process of appropriately configuring, connecting, and validating IP for the target board. 	<ul style="list-style-type: none"> • Product Selector Guide Tool • Using the Board-Aware Flow
Planning for Device Migration	<ul style="list-style-type: none"> • Determine whether you want to migrate your design to another device density to allow flexibility when your design nears completion. • Target a small (less expensive) device and move to a larger device if necessary to meet your design requirements. • Develop a prototype of your design in a larger device to reduce optimization time and achieve timing closure more quickly, and then migrate to a smaller device after prototyping. <p><i>Note:</i> Selecting a migration device impacts pin placement because some pins may serve different functions in different device densities or package sizes.</p>	
Planning for Intellectual Property (IP) Cores	<p>Plan which I/O interfaces or blocks in the system you want to implement using IP cores.</p> <p>Integrate functions into your design using Intel FPGA IP cores, many of which are available for production use in the Quartus Prime software without additional license.</p>	<ul style="list-style-type: none"> • Working With Intel FPGA IP Cores on page 50 • Intel FPGA IP Portfolio Web Page
continued...		

Item	Considerations	Links
	For IP cores that require additional licenses for production, use the Intel FPGA IP Evaluation Mode, which allows you to program the FPGA to verify the IP in the hardware before you purchase the IP license.	
Planning for Standard Interfaces	<ul style="list-style-type: none"> Use standard interfaces in system design to ensure compatibility between design blocks from different design teams or vendors. Use the Quartus Prime Interface Planner to accurately plan constraints for design implementation, prototype interface implementations, and rapidly define a legal device floorplan. Use the Quartus PrimePlatform Designer system integration tool to use standard interfaces and speed-up system-level integration. 	Quartus Prime Pro Edition User Guide: Platform Designer
Planning for Device Power Consumption	<p>Estimating power consumption early in the design cycle allows you to plan power budgets and avoid unexpected results when designing the PCB.</p> <ul style="list-style-type: none"> Use the Early Power Estimator (EPE) spreadsheet for older devices, such as the Arria 10 and Cyclone 10 families or to estimate power consumption before compiling or creating any source code. Use the Quartus Prime Power Analyzer to ensure that your design satisfies thermal and power supply requirements. Use the Intel FPGA Power and Thermal Calculator (PTC) to estimate power utilization for your design for Stratix 10, Agilex 7, and Agilex 5 device families. PTC does not support older devices. 	<ul style="list-style-type: none"> Quartus Prime Pro Edition User Guide: Power Analysis and Optimization Intel FPGA Power and Thermal Calculator User Guide
Planning for I/O Interfaces	<ul style="list-style-type: none"> Create a preliminary pin-out for an Intel FPGA with the Quartus Prime Pin Planner before you develop the source code, based on standard I/O interfaces (such as memory and bus interfaces) and any other I/O requirements for your system. Configure how to connect the functions and cores to each other by specifying matching node names for selected ports. Create other I/O-related assignments for these interfaces or other design I/O pins in the Pin Planner. Compile your design to automatically run I/O Assignment Analysis in Fitter to validate I/O-related assignments that you created or modified throughout the design process. 	<ul style="list-style-type: none"> Quartus Prime Pro Edition User Guide: Design Optimization I/O Planning Overview
Planning for Other EDA Tools	<ul style="list-style-type: none"> Use supported standard third-party EDA synthesis tools to synthesize your Verilog HDL or VHDL design, and compile the resulting output netlist file in the Quartus Prime software. Use the simulator version that your Quartus Prime software version supports for best results. You must also use the model libraries provided with your Quartus Prime software version. Libraries can change between versions, which might cause a mismatch with your simulation netlist. 	<ul style="list-style-type: none"> Quartus Prime Pro Edition User Guide: Third-party Synthesis Quartus Prime Pro Edition User Guide: Third-party Synthesis
continued...		

Item	Considerations	Links
Planning for On-Chip Debugging Tools	<ul style="list-style-type: none"> Consider whether to include on-chip debugging tools early in the design process. Adding the debugging tools late in the design process can be more time-consuming and error-prone. Consider the following debugging requirements when planning your design to support debugging tools: <ul style="list-style-type: none"> JTAG connections—required to perform in-system debugging with JTAG tools. Plan your system and board with JTAG ports that are available for debugging. Additional logic resources (ALR)—required to implement JTAG hub logic. If you set up the appropriate tool early in your design cycle, you can include these device resources in your early resource estimations to ensure that you do not overload the device with logic. Reserve device memory—required if your tool uses device memory to capture data during system operation. To ensure that you have enough memory resources to take advantage of this debugging technique, consider reserving device memory to use during debugging. Reserve I/O pins—required if you use the Logic Analyzer Interface (LAI), which requires I/O pins for debugging. If you reserve I/O pins for debugging, you do not have to later change your design or board. The LAI can multiplex signals with design I/O pins if required. Ensure that your board supports a debugging mode, in which debugging signals do not affect system operation. Instantiate an IP core in your HDL code—required if your debugging tool uses an Intel FPGA IP core. Instantiate the Signal Tap Logic Analyzer IP core—required if you want to manually connect the Signal Tap Logic Analyzer to nodes in your design and ensure that the tapped node names do not change during synthesis. 	<ul style="list-style-type: none"> Factors to Consider When Using Debugging Tools During Design Planning Stages Quartus Prime Pro Edition User Guide: Debug Tools
Planning HDL Coding Styles	<ul style="list-style-type: none"> Use synchronous design practices to consistently meet your design goals. In a synchronous design, a clock signal triggers all events. When you meet all register timing requirements, a synchronous design behaves in a predictable and reliable manner for all process, voltage, and temperature (PVT) conditions. You can easily target synchronous designs to different device families or speed grades. <i>Note:</i> Problems with asynchronous design techniques include reliance on propagation delays in a device, incomplete timing analysis, and possible glitches. Use dedicated clock pins and clock routing for best results, and if you have PLLs in your target device, use the PLLs for clock inversion, multiplication, and division. For clock multiplexing and gating, use the dedicated clock control block or PLL clock switchover feature instead of combinational logic, if these features are available in your device. If you must use internally generated clock signals, register the output of any combinational logic used as a clock signal to reduce glitches. 	<ul style="list-style-type: none"> Quartus Prime Pro Edition User Guide: Design Recommendations Quartus Prime Pro Edition User Guide: Timing Analyzer

continued...

Item	Considerations	Links
	<ul style="list-style-type: none"> Consider the architecture of the device you choose so that you can use specific features in your design. For example, the control signals should use the dedicated control signals in the device architecture. Sometimes, you might need to limit the number of different control signals used in your design to achieve the best results. HDL coding styles can have a significant effect on the quality of results for programmable logic designs. Follow the coding guidelines for inferring Intel FPGA IP and targeting dedicated device hardware, such as memory and DSP blocks. Ensure that your design accounts for synchronization between any asynchronous clock domains. Consider using a synchronizer chain of more than two registers for high-frequency clocks and frequently-toggling data signals to reduce the chance of a metastability failure. Use the Quartus Prime software to analyze the average mean time between failures (MTBF) due to metastability when a design synchronizes asynchronous signals, and optimize your design to improve the metastability MTBF. 	
Planning your Project Path Length	<p>Design files with lengthy file paths might cause an internal error in the Windows* version of the Quartus Prime Pro Edition software. Windows has a 260-character maximum path length limitation on the combined length of a file name and its file path.</p> <p>To reduce the length of a file path to a design file, Intel strongly recommends creating, storing, or moving your Quartus Prime project to a shorter path. For example:</p> <pre>C:\quartus_pro\<version>\project</pre> <p><i>Tip:</i> There are several third-party software freely available to help you fix the long path issue for Windows.</p>	Maximum Path Length Limitation

Table 8. Factors to Consider When Using Debugging Tools During Design Planning Stages

Design Planning Factor	Signal Tap Logic Analyzer	System Console	In-System Memory Content Editor	Logic Analyzer Interface (LAI)	Signal Probe	In-System Sources and Probes	Virtual JTAG IP Core
JTAG connections	Yes	Yes	Yes	Yes	—	Yes	Yes
Additional logic resources	—	Yes	—	—	—	—	Yes
Reserve device memory	Yes	Yes	—	—	—	—	—
Reserve I/O pins	—	—	—	Yes	Yes	—	—
Instantiate IP core in your HDL code	—	—	—	—	—	Yes	Yes

2.2. Selecting the Design Methodology

When creating an FPGA design, you must consider various design methodologies the Quartus Prime software offers, such as the incremental block-based design, flat design, and partial reconfiguration design. You can use these design flows with or without EDA design entry and synthesis tools. Refer to the following topics for more information about each of these methodologies.

2.2.1. Flat Design Vs. Incremental Block-based Design

With the Quartus Prime Pro Edition software, you can either develop a flat design or a block-based design:

- **Flat Designs:** In a flat compilation flow, the design hierarchy is flattened without design partitions and the Quartus Prime software compiles the entire design in a “flat” netlist. Although the source code may be hierarchical, the compiler flattens and synthesizes all the design logic. Whenever you recompile the project, the compiler re-performs all available logic and placement optimizations on the entire design.

The flat compilation flow does not require any planning for design partitions. However, because the Quartus Prime software recompiles the entire design whenever you change your design, flat design practices may require more overall compilation time for large designs. Additionally, you may find that the results for one part of the design change when you change a different part of your design.

If you plan to develop a small design with no plans to reuse or preserve blocks, use a flat design. However, flat designs are generally more difficult to optimize and debug because you cannot always isolate the timing issue.

- **Block-based designs:** In block-based (hierarchical) flows, you can divide your design by creating design partitions. Block-based design flow is also known as modular or hierarchical design flow. You can designate a design block as a design partition to preserve or reuse the block. A design partition is a logical, named, hierarchical boundary assignment that you can apply to a design instance. Hierarchical flows allow you to isolate, optimize, and preserve compilation results for specific design blocks but require more design planning to ensure effective results.

Using a hierarchical design methodology offers several advantages, such as:

- Reuse design blocks with the same periphery configuration, share a synthesized design block with another designer, or replicate placed and routed IP in another project.
- Design, implement, and verify core or periphery blocks once, and then reuse those blocks multiple times across different projects that use the same device.
- Perform easier debugging and optimization of individual design blocks.
- Assign the design hierarchy elements into logical partitions that are functionally independent.
- Perform stand-alone block verification.
- Use design blocks for reuse and preserve synthesis and timing results for blocks that are fully coded and meeting timing.
- Preserve earlier results for a block you do not want to change when you change RTL code or compiler settings for another block in the design. The compiler produces different compilation results compared to previous settings and can cause timing violations in blocks that do not reflect the same corresponding code or setting changes. Block-based incremental compilation flow allows for preserving the block.
- Partition a design, compile the design partitions separately, and reuse the results for unchanged partitions. You can preserve the performance of unchanged blocks and reduce the number of design iterations. The performance preservation of incremental block-based compilation allows you to focus timing closure on unpreserved partitions or on blocks that have difficulty meeting timing requirements

For more information about the block-based designing, refer to the *Quartus Prime Pro Edition User Guide: Block-Based Design*.

Related Information

[Quartus Prime Pro Edition: Block-Based Design](#)

2.2.2. Partial Reconfiguration Design

Partial reconfiguration (PR) allows you to reconfigure a portion of the FPGA dynamically while the remaining FPGA design continues to function. You can define multiple personas for a particular region in your design without impacting operation in areas outside this region. This methodology is effective in systems with various functions that time-share the same FPGA device resources. PR enables the implementation of more complex FPGA systems.

The Quartus Prime Pro Edition software supports the PR feature for the Agilex 5, Agilex 7, Stratix 10, Arria 10, and Cyclone 10 GX device families.

PR provides the following advantages over a flat design:

- Allows run-time design reconfiguration.
- Increases scalability of the design through time-multiplexing.
- Lowers cost and power consumption through efficient use of board space.
- Supports dynamic time-multiplexing functions in the design.
- Improves initial programming time through smaller bitstreams.
- Reduces system downtime through line upgrades.
- Enables easy system updates by allowing remote hardware change.
- Supports a simplified compilation flow for partial reconfiguration.

For more information about the PR design, refer to the *Quartus Prime Pro Edition User Guide: Partial Reconfiguration*.

Related Information

[Quartus Prime Pro Edition: Partial Reconfiguration](#)

2.3. Related Trainings

You can take up the following training to help you when planning FPGA design for RTL flow:

- [Creating Reusable Design Blocks: Introduction to IP Reuse with the Quartus Prime Software](#)
- [Design Block Reuse in the Quartus Prime Pro Edition Software](#)
- [Incremental Block-Based Compilation in the Quartus Prime Pro Edition Software: Introduction](#)
- [Incremental Block-Based Compilation in the Quartus Prime Pro Edition Software: Design Partitioning](#)
- [Incremental Block-Based Compilation in the Quartus Prime Pro Edition Software: Timing Closure & Tips](#)
- [Partial Reconfiguration in Quartus Prime](#)
- [Partial Reconfiguration for Intel FPGA Devices: Introduction & Project Assignments](#)

- [Partial Reconfiguration for Intel FPGA Devices: Design Guidelines & Host Requirements](#)
- [Partial Reconfiguration for Intel FPGA Devices: PR Host IP & Implementations](#)
- [Partial Reconfiguration for Intel FPGA Devices: Output Files & Demonstration](#)

3. Selecting a Starting Point for Your Quartus Prime Pro Edition Project

Navigating Content Through Tasks

Use the following navigation diagram to navigate this guide through user-tasks:



There are multiple ways you can set up your project depending on your design needs. Either you can create a new project with project files and libraries or with a design example, or you can import an existing project into the Quartus Prime Pro Edition software.

Select one of the following methods to set up your Quartus Prime Pro Edition project:

[Creating a New FPGA Design Project](#) on page 22

[Migrating Projects from Other Quartus Prime Editions to Quartus Prime Pro Edition](#) on page 33

[Migrating Your AMD* Vivado* Project to Quartus Prime Pro Edition](#) on page 45

[Migrating Projects Across Operating Systems](#) on page 45

[Migrating Project From One Device to Another](#) on page 47

[Related Trainings](#) on page 49

3.1. Creating a New FPGA Design Project

The Quartus Prime software makes it easy for you to quickly setup a new FPGA design project.

Use the quick access icons on the home page to set up your FPGA design project:

- **New Project Wizard:** Use this option to create a project either by specifying project files, libraries, target device family, and EDA tool settings, or using an existing design example.
- **Open Example Project:** Use this option if you want to base your current project on a pre-installed and verified design example.
- **Open Project:** Use this option to browse and open your existing projects.

The wizard guides you through specifying various options for new project setup and includes access to helpful project templates and design examples that allow you to preconfigure project settings for specific applications, FPGA devices, and target boards.

3.1.1. Using the Board-Aware Flow

The Quartus Prime Pro Edition software allows you to create a system that targets a specific development board, rather than only targeting a specific FPGA device. When you target a specific development board, the Quartus Prime software is *aware* of the target board (board-aware) which accelerates the process of appropriately configuring, connecting, and validating IP for the target board.

What is the Quartus Prime Software Board-Aware Flow?

In the board-aware flow, you can optionally start your project from a pre-verified design example (rather than an empty project) and target a specific Intel FPGA development board. You can also create appropriate IP presets to target the specific board. The Quartus Prime Platform Designer system integration tool is also board-aware, allowing you to automatically set pin assignments and export appropriate system interfaces for the target board.

The board-aware flow simplifies the application of appropriate parameters and pin assignments for the instantiated IP in your project, thereby reducing the chance of configuration errors. You can also save and reuse your preferred and verified board and IP configurations for use in other projects that target the same IP or board.

The board-aware flow helps to ensure the proper hand-off, consistency, and reuse of configuration options across multiple projects, developers, and boards.

Note:

To define new boards and IP preset files in Platform Designer, refer to *Intel Quartus Prime Pro Edition User Guide: Platform Designer* and *AN 988: Using the Board-Aware Flow in the Intel Quartus Prime Pro Edition Software*.

Related Information

- [Creating a New Project from a Design Example](#) on page 24
- [Specifying a Target Board for the Project](#) on page 32
- [Applying Preset Parameters for Specific Applications](#) on page 61
- [Intel Quartus Prime Pro Edition User Guide: Platform Designer](#)
- [AN 988: Using the Board-Aware Flow in the Intel Quartus Prime Pro Edition Software](#)

3.1.1.1. Creating a New Project from a Design Example

The Quartus Prime software provides access to installed and online platform- and board-specific design examples that you can use as a starting point for your own design. You can accelerate your design progress by starting from a pre-validated design example that installs with the Quartus Prime software or is available online.

This technique can be especially helpful if you are new to FPGA design or EDA design tools. The design example can help you to quickly analyze a validated design on a board and appropriately configure it in various ways to match your users' needs. Alternatively, you can start with an **Empty Project** for which you specify all settings and design files.

- **Pre-installed design examples**—you can immediately access the design examples that install along with the Quartus Prime software installation at: `<quartus>\acds\quartus\common\board_designs`.
- **Online design examples**—you can access design examples hosted online, which includes designs from the [Intel FPGA Design Store](#) or directly from Quartus Prime software by clicking **Open Example Project** from the home page. For more information, refer to [Design Example Discovery](#).
- **Downloaded design examples**—you can access your previously downloaded design examples, or any design example that you store in a local drive, under downloaded reference designs.

To create a new Quartus Prime project that is based on a design example, follow these steps:

1. the Quartus Prime software, click **File > New Project Wizard**. Click **Next** to view the **Family, Device & Board Settings** wizard page.
2. Under the **Select the type of project to create**, select **Design Example** and click **Next**. The **Family, Device & Board Settings** page appears, allowing you to find and select the design example from which to base your project.

Figure 4. Family, Device & Board Settings Page of New Project Wizard

3. Under **What is the working directory for this project?**, specify the directory to store your project files and click **Next**.

- Under **Find Options**, select the **Family**, **Development Kit**, and **Vendor** design example you want to use. Refer to [Family, Device & Board Settings](#) on page 25.

Figure 5. Board Tab in New Project Wizard

Device Board

Select the board/development kit you want to target for compilation.

Find Options

Family: Agilex 7

Development Kit: Any

Vendor: Any

☐ Show only boards/development kits with design examples

Filter: Device

	Development Kit
✓	Intel Agilex 7 F-Series FPGA Development Kit DK-DEV-AGF014EA
✓	Intel Agilex 7 F-Series Transceiver-SoC Development Kit DK-SI-AGF014EA
✓	Intel Agilex 7 I-Series FPGA Development Kit DK-DEV-AGI027RES
✓	Intel Agilex 7 2_F-Tile FPGA F-Series Development Kit

The search results display the design examples that meet your search criteria.

- Select the design example that you want in the search results and click **Next**. If the design example is licensed by Intel FPGA, a **Software License Agreement** page appears that prompts you to accept the license agreement before you can proceed.
- Click **Next** to proceed to the **Summary** page.
- Click **Finish** to deploy the selected design example in the Quartus Prime software. When a design example downloads, the design's .par downloads to the download path that you define in **More Settings**, but the design itself extracts to the project working directory that you specify.

Also refer to [Accessing Online Design Examples](#) on page 27 and [Accessing Downloaded Design Examples](#) on page 31.

Related Information

[Intel FPGA Design Examples](#)

3.1.1.1.1. Family, Device & Board Settings

The following options are available in the **Family, Device & Board Settings** page of the **New Project Wizard**. Specify these options to locate and deploy a validated design example targeting a specific board as a starting point for your FPGA design project. Some options are only available from **File > Open Example Project**

Table 9. Family, Device & Board Settings Page Options

Option	Description
Select the type of project to create	<ul style="list-style-type: none"> • Empty—create a new empty FPGA design project to which you add all design files, settings, and constraints. • Design example—create a new project from an existing design example. You can access installed or online available design examples.
What is the working directory for this project?	Specifies the directory where you want to extract and deploy the design example.
Find Options	<p>Allows you to filter design example search results by one of the following facets:</p> <ul style="list-style-type: none"> • Load from > Pre-installed design examples—specifies that search includes examples installed with the Quartus Prime software. • Load from > User downloaded design examples—search includes design examples that you download or your own design examples that you store in a local repository. • Load from > Online design examples—search includes design examples hosted online, including examples from the Intel FPGA Design Store. • Family—search only includes design examples for the device families that you specify. You can specify multiple values. • Quartus Prime version—search only includes design examples that support the Quartus Prime software version that you specify. You can specify multiple pipe separated values. • Development kit—search only includes design examples that support the Intel FPGA development kit that you specify. You can specify multiple pipe separated values.
More settings button	Opens the Options panel that allows you to configure the Internet Connectivity and Design Examples connection and download settings, as Design Examples Options on page 30 describes.
Reset button	Resets the Find Options to default settings.
Legend panel	Displays the meaning of design example status icons in the search results. Design example status is validated (checkmark icon), unvalidated (question mark icon), or unsupported for the current Intel Quartus Prime software version (x icon).
Filter text box	Specifies a text string to further filter design example search results according to any text string you specify.
Search results list	Displays the design examples, status, and location that match your search filters.
Details panel	Displays a detailed description and diagram of the selected design example.
Design Store button	Opens the Design Store website in your default web browser from which you can download available Intel FPGA validated design examples.

3.1.1.1.2. Accessing Pre-Installed Design Examples

The Quartus Prime software installation includes design examples for your immediate use.

You can access the pre-installed design examples while using the Quartus Prime software using the following methods:

- Click **File > New Project Wizard > Family, Device & Board Settings** page.
- Click **Open Example Project** on the **Home** tab (**Help > Home**).
- Click **File > Open Example Project**.

To create a new project based on pre-installed design examples, follow these steps Quartus Prime Pro Edition software:

1. Click **File > Open Example Project**. The **Design Example** page of the **New Project Wizard** opens.
2. For **What is the working directory for this project?**, specify the directory location to store your project files.

Figure 6. Find Options Locate Pre-Installed Design Example

Load From	Design Name
Pre-installed	Agilex 7 - Nios® V/m PIO LED Toggle Design
Pre-installed	Agilex 7 - Nios® V/m EMIF Data Mover Design
Pre-installed	Agilex 7 - Nios® II-EMIF-PIO Design

3. Under **Find Options**, specify the following settings to filter the list of design examples for the target device and board. Also refer to [Family, Device & Board Settings](#) on page 25.
 - a. In **Load from**, select the **Pre-Installed design examples**, repository.
 - b. In **Family**, select your target FPGA device family.
 - c. In **Intel Quartus Prime version**, select the software version.
 - d. In **Development kit**, select the target kit or board.
4. Under **Design name**, select the design example to base your project on.
5. Click **Next**, and then click **Finish**. The design extracts to the working directory and opens in the Quartus Prime software.

Related Information

[Design Example Discovery](#)

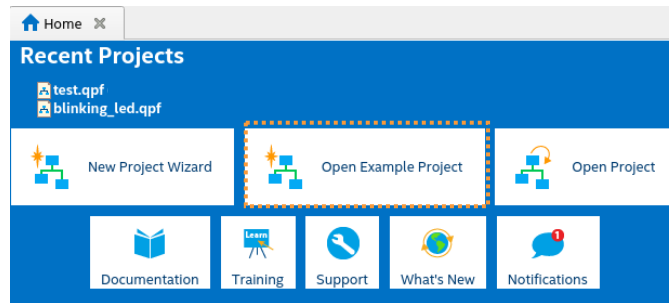
3.1.1.1.3. Accessing Online Design Examples

You can create a new project based on a design example that you access from an online repository. To use this method, you may need to specify a proxy server for access and the download path.

To create a new project in the Intel Quartus Prime software based on online design examples, follow these steps:

1. Click **File > Open Example Project**. The **Design Example** page of the **New Project Wizard** opens.

Figure 7. Open Example Project Icon on Home Page



2. For **What is the working directory for this project?**, specify the directory location to store your project files.
3. Click the **More Settings** button. The **Options** dialog box opens with the **Internet Connectivity** tab open by default.

Figure 8. Intel Quartus Prime Software Internet Connectivity Settings

4. If your internet connection requires a proxy server (using VPN), turn on the **Access online design examples using a proxy server** option, and then specify your proxy **Address**, **Port**, **User name**, and **Password**. If your internet connection does not require a proxy server, skip this step.
5. On the **Design Example Search Locations** tab, specify the **Download path** for download of the design example .par file.
6. Click **OK**.
7. Under **Find Options**, specify the following settings. Also refer to [Family, Device & Board Settings](#) on page 25.
 - a. In **Load from**, select **Downloaded design examples**.
 - b. In **Family**, **Intel Quartus Prime version**, and **Development kit** fields select the values to match your target design and board.
8. In the design example list, select the design that you want to deploy.

Figure 9. Online Agilex 7 - I/O PLL Reconfiguration Design

Find Options

Load from: Online design examples

Family: Agilex 7

Intel Quartus Prime version: 22.4

Development kit: Intel® Agilex™ F-Series Transceiver-SoC Development Kits

More settings... Reset

Legend

Q <<Filter>>

	Load From	Design Name
?	Online	Agilex 7 - Agilex - I/O PLL Reconfiguration

- Click **Next**, and then click **Finish**. The design extracts to the working directory and opens in the Quartus Prime software.

Internet Connectivity Options

You can specify the following internet connectivity options that determine how the Quartus Prime software connects to the internet for various functions, such as accessing Help and design examples, with either of the following:

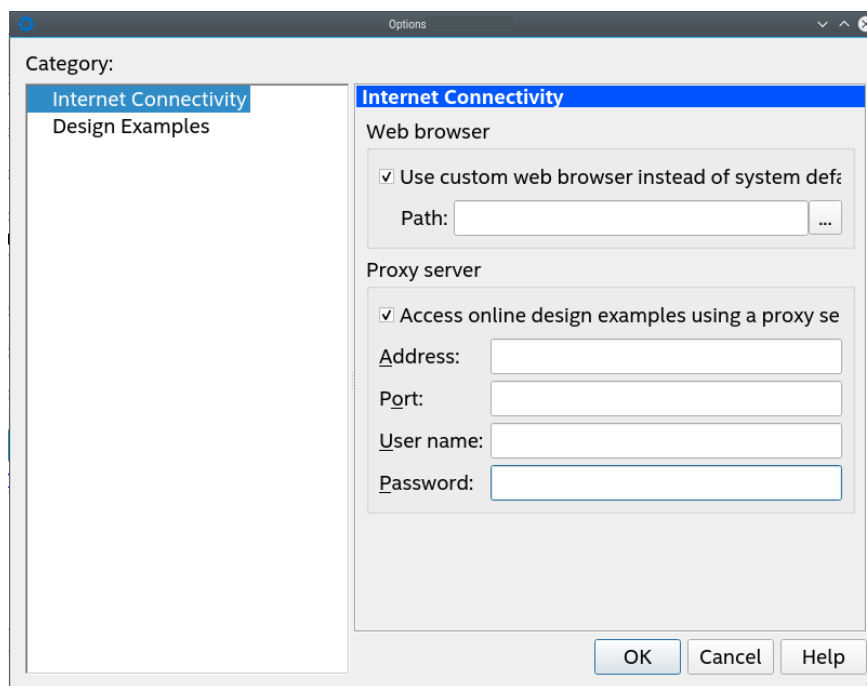
- Click **Tools > Options > Internet Connectivity**
Or
- Click **More Settings** on the **Design Example** page of the **New Project Wizard** (**File > New Project Wizard**).

The following options are available on the **Internet Connectivity** options page.

Table 10. Internet Connectivity Options

Option	Description
Web browser	Specifies the web browser that deploys when the Quartus Prime software accesses the internet, including the Intel FPGA Design Store web page. Enable Use custom web browser to specify the path to your preferred supported web browser.
Proxy server	Specify options if connecting to the internet through a proxy server. To access online design examples specify the appropriate option: <ul style="list-style-type: none"> Access online design examples using a proxy server—turn on this option if you are connected to the internet through a VPN. Turn off this option if you are not connected to the internet through a VPN (such as connection through a private network).

Figure 10. Internet Connectivity Page



Related Information

[Design Example Options Page](#) on page 30

Design Examples Options

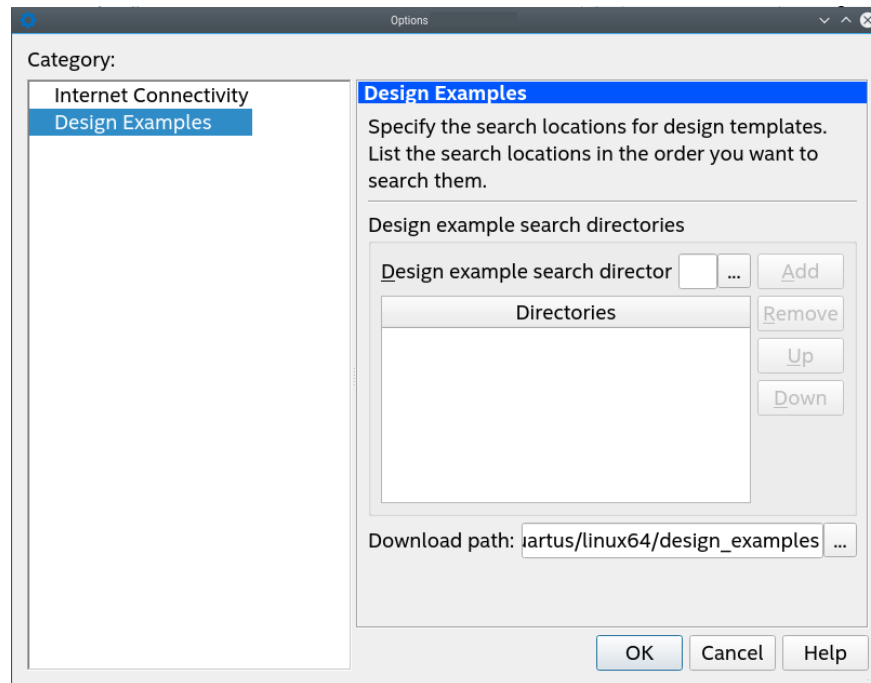
You can click the following to specify options that determine how the Quartus Prime software accesses available design examples.

- Click **File > New Project Wizard** and then click the **More Settings** button on the **Design Example** page of the **New Project Wizard**.

Table 11. Design Examples Options

Option	Description
Design Example search directory	Specifies the local directories that the Quartus Prime software searches for design examples. This setting determines which directories you include in search when using the New Project Wizard to start a project from an existing design example. Click Add , Remove , Up , or Down to change the search order and contents in the Directories list.
Directories	Lists the various directories that you include in the design example search path for the New Project Wizard .
Download path	Specifies the path for download of online design examples.

Figure 11. Design Examples Page



3.1.1.1.4. Accessing Downloaded Design Examples

You can create a new project from a design example that you have previously downloaded. Download a design example .par file from an online repository (such as the Intel FPGA Design Store) into your working directory. Designs that you create yourself and store in a local drive also appear as downloaded examples.

To create a new project based on downloaded design examples, follow these steps:

1. Download a design example, as [Accessing Online Design Examples](#) on page 27 describes.
2. Click the **Open Example Project** icon on the Quartus Prime Pro Edition **Home** page. The **Design Example** page of the **New Project Wizard** opens.
3. For **What is the working directory for this project?**, specify the directory location to store your project files.
4. Under **Find Options**, specify the following settings. Refer to [Family, Device & Board Settings](#) on page 25.
 - a. In **Load from**, select **Downloaded design examples**.
 - b. In **Family**, **Intel Quartus Prime version**, and **Development kit** fields select the values to match your target design and board.
5. In the design example list, select the design that you want to deploy.

Figure 12. Downloaded Agilex 7 I/O PLL Reconfiguration Design

Find Options

Load from: User downloaded design examples

Family: Agilex 7

Intel Quartus Prime version: 19.4.0

Development kit: Agilex F-Series Transceiver-SoC Development Kit

More settings... Reset

Legend

Q <<Filter>>

Load From	Design Name
Downloaded	I/O PLL Reconfiguration

- Click **Next**, and then click **Finish**. The design extracts to the working directory and opens in the Quartus Prime software.

3.1.1.2. Specifying a Target Board for the Project

You can specify the target for a new project in the New Project Wizard, or you can specify a target board for an existing project by clicking **Assignments** ► **Device**. To specify a target board for an existing project, follow these steps:

- Click **Assignments** ► **Device**. The **Device** dialog box appears.
- Click the **Board** tab. The **Board** tab allows you to target a specific FPGA device board, rather than just a specific FPGA device.

Figure 13. Board Tab Settings

Device Board

Select the board/development kit you want to target for compilation.

Find Options

Family: Agilex 7

Development Kit: Intel Agilex 7 F-Series FPGA Development Kit DK-DEV-A

Vendor: Intel

☐ Show only boards/development kits with design examples

Filter: Device

Development Kit	Family
Intel Agilex 7 F-Series FPGA Development Kit DK-DEV-AGF014EA	Agilex 7

- In the **Family**, **Intel Quartus Prime version**, and **Development kit** fields, select the values to match your target design and board.
- Click the desired board in the list. The board details appear in the right pane.
- Click **OK**. Your project now targets the specified board and device.

3.2. Migrating Projects from Other Quartus Prime Editions to Quartus Prime Pro Edition

The Quartus Prime Pro Edition software supports migration of Quartus Prime Standard Edition, Quartus Prime Lite Edition, and Quartus II software projects.

Note: The migration steps for Quartus Prime Lite Edition, Quartus Prime Standard Edition, and the Quartus II software are identical. For brevity, this section refers to these design tools collectively as "other Quartus software products."

Migrating to Quartus Prime Pro Edition requires the following changes to other Quartus software product projects:

1. Upgrade project assignments and constraints with equivalent Quartus Prime Pro Edition assignments.
2. Upgrade all Intel FPGA IP core variations and Platform Designer systems in your project.
3. Upgrade design RTL to standards-compliant VHDL, Verilog HDL, or SystemVerilog.

This document describes each migration step in detail.

Related Information

[Migrating to the Quartus Prime Pro Edition Software](#)

3.2.1. Keeping Pro Edition Project Files Separate

The Quartus Prime Pro Edition software does not support project or constraint files from other Quartus software products. Do not place project files from other Quartus software products in the same directory as Quartus Prime Pro Edition project files. In general, use Quartus Prime Pro Edition project files and directories only for Quartus Prime Pro Edition projects, and use other Quartus software product files only with those software tools.

Quartus Prime Pro Edition projects do not support compilation in other Quartus software products, and vice versa. The Quartus Prime Pro Edition software generates an error if the Compiler detects other Quartus software product's features in project files.

Before migrating other Quartus software product projects, click **Project ► Archive Project** to save a copy of your original project before making modifications for migration.

3.2.2. Upgrading Project Assignments and Constraints

Quartus Prime Pro Edition software introduces changes to handling of project assignments and constraints that the Quartus Settings File (.qsf) stores. Upgrade other Quartus software product project assignments and constraints for migration to the Quartus Prime Pro Edition software. Upgrade other Quartus software product assignments with **Assignments ► Assignment Editor**, by editing the .qsf file directly, or by using a Tcl script.

Note: If you open a Quartus Prime Standard Edition software project in the Quartus Prime Pro Edition software, and that project contains unsupported junction temperature setting values, you can modify these settings by clicking **Assignments > Settings > Operating Settings and Conditions > Temperature**. Click **OK**, and then click **Yes** when prompted to update the values.

The following sections detail the various types of project assignment upgrade that migration requires.

Related Information

- [Modifying Entity Name Assignments](#) on page 34
- [Resolving Timing Constraint Entity Names](#) on page 34
- [Verifying Generated Node Name Assignments](#) on page 35
- [Replace Logic Lock \(Standard\) Regions](#) on page 35
- [Modifying Signal Tap Logic Analyzer Files](#) on page 37
- [Removing Unsupported Feature Assignments](#) on page 38

3.2.2.1. Modifying Entity Name Assignments

Quartus Prime Pro Edition software supports assignments that include instance names *without* a corresponding entity name.

- "a_entity:a|b_entity:b|c_entity:c" (includes deprecated entity names)
- "a|b|c" (omits deprecated entity names)

While the current version of the Quartus Prime Pro Edition software still *accepts* entity names in the .qsf, the Compiler *ignores* the entity name. The Compiler generates a warning message upon detection of an entity names in the .qsf. Whenever possible, you should remove entity names from assignments, and discontinue reliance on entity-based assignments. Future versions of the Quartus Prime Pro Edition software may eliminate all support for entity-based assignments.

3.2.2.2. Resolving Timing Constraint Entity Names

The Quartus Prime Pro Edition Timing Analyzer honors entity names in Synopsys Design Constraints (.sdc) files.

Use .sdc files from other Quartus software products without modification. However, any scripts that include custom processing of names that the .sdc command returns, such as `get_registers` may require modification. Your scripts must reflect that returned strings do not include entity names.

The .sdc commands respect wildcard patterns containing entity names. Review the Timing Analyzer reports to verify application of all constraints. The following example illustrates differences between functioning and non-functioning .sdc scripts:

```
# Apply a constraint to all registers named "acc" in the entity "counter".
# This constraint functions in both SE and PE, because the SDC
# command always understands wildcard patterns with entity names in them
set_false_path -to [get_registers "counter:*|*acc"]

# This does the same thing, but first it converts all register names to
# strings, which includes entity names by default in the SE
# but excludes them by default in the PE. The regexp will therefore
# fail in PE by default.
```

```
#
# This script would also fail in the SE, and earlier
# versions of Quartus II, if entity name display had been disabled
# in the QSF.
set_all_reg_strs [query_collection -list -all [get_registers *]]
foreach keeper $all_reg_strs {
  if {[regexp {counter:*|:*acc} $keeper]} {
    set_false_path -to $keeper
  }
}
```

Removal of the entity name processing from .sdc files may not be possible due to complex processing involving node names. Use standard .sdc whenever possible to replace such processing. Alternatively, add the following code to the top and bottom of your script to temporarily re-enable entity name display in the .sdc file:

```
# This script requires that entity names be included
# due to custom name processing
set_old_mode [set_project_mode -get_mode_value always_show_entity_name]
set_project_mode -always_show_entity_name on

<... the rest of your script goes here ...>

# Restore the project mode
set_project_mode -always_show_entity_name $old_mode
```

3.2.2.3. Verifying Generated Node Name Assignments

Quartus Prime synthesis generates and automatically names internal design nodes during processing. The Quartus Prime Pro Edition uses different conventions than other Quartus software products to generate node names during synthesis. When you synthesize your other Quartus software product project in Quartus Prime Pro Edition, the synthesis-generated node names may change. If any scripts or constraints depend on the synthesis-generated node names, update the scripts or constraints to match the Quartus Prime Pro Edition synthesis node names.

Avoid dependence on synthesis-generated names due to frequent changes in name generation. In addition, verify the names of duplicated registers and PLL clock outputs to ensure compatibility with any script or constraint.

3.2.2.4. Replace Logic Lock (Standard) Regions

Quartus Prime Pro Edition software introduces more simplified and flexible Logic Lock constraints, compared with previous Logic Lock regions. You must replace all Logic Lock (Standard) assignments with compatible Logic Lock assignments for migration.

To convert Logic Lock (Standard) regions to Logic Lock regions:

1. Edit the .qsf to delete or comment out all of the following Logic Lock assignments:

```
set_global_assignment -name LL_ENABLED*
set_global_assignment -name LL_AUTO_SIZE*
set_global_assignment -name LL_STATE FLOATING*
set_global_assignment -name LL_RESERVED*
set_global_assignment -name LL_CORE_ONLY*
set_global_assignment -name LL_SECURITY_ROUTING_INTERFACE*
set_global_assignment -name LL_IGNORE_IO_BANK_SECURITY_CONSTRAINT*
set_global_assignment -name LL_PR_REGION*
set_global_assignment -name LL_ROUTING_REGION_EXPANSION_SIZE*
set_global_assignment -name LL_WIDTH*
```

```
set_global_assignment -name LL_HEIGHT
set_global_assignment -name LL_ORIGIN
set_instance_assignment -name LL_MEMBER_OF
```

2. Edit the .qsf or click **Tools ► Chip Planner** to define new Logic Lock regions. Logic Lock constraint syntax is simplified, for example:

```
set_instance_assignment -name PLACE_REGION "1 1 20 20" -to fifo1
set_instance_assignment -name RESERVE_PLACE_REGION OFF -to fifo1
set_instance_assignment -name CORE_ONLY_PLACE_REGION OFF -to fifo1
```

Compilation fails if synthesis finds other Quartus software product's Logic Lock assignments in an Quartus Prime Pro Edition project. The following table compares other Quartus software product region constraint support with the Quartus Prime Pro Edition software.

Table 12. Region Constraints Per Edition

Constraint Type	Logic Lock (Standard) Region Support Other Quartus Software Products	Logic Lock Region Support Quartus Prime Pro Edition
Fixed rectangular, nonrectangular or non-contiguous regions	Full support.	Full support.
Chip Planner entry	Full support.	Full support.
Periphery element assignments	Supported in some instances.	Full support. Use "core-only" regions to exclude the periphery.
Nested ("hierarchical") regions	Supported but separate hierarchy from the user instance tree.	Supported in same hierarchy as user instance tree.
Reserved regions	Limited support for nested or nonrectangular reserved regions. Reserved regions typically cannot cross I/O columns; use non-contiguous regions instead.	Full support for nested and nonrectangular regions. Reserved regions can cross I/O columns without affecting periphery logic if the regions are "core-only".
Routing regions	Limited support via "routing expansion." No support with hierarchical regions.	Full support (including future support for hierarchical regions).
Floating or autosized regions	Full support.	No support.
Region names	Regions have names.	Regions are identified by the instance name of the constrained logic.
Multiple instances in the same region	Full support.	Support for non-reserved regions. Create one region per instance, and then specify the same definition for multiple instances to assign to the same area. Not supported for reserved regions.
Member exclusion	Full support.	No support for arbitrary logic. Use a core-only region to exclude periphery elements. Use non-rectangular regions to include more RAM or DSP columns as needed.

3.2.2.4.1. Logic Lock Region Assignment Examples

The following examples show the syntax of Logic Lock region assignments in the .qsf file. Optionally, you can enter these assignments in the Assignment Editor, the Logic Lock Regions Window, or the Chip Planner.

Example 1. Assign Rectangular Logic Lock Region

Assigns a rectangular Logic Lock region to a lower left corner location of (10,10), and an upper right corner of (20,20) inclusive.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"
```

Example 2. Assign Non-Rectangular Logic Lock Region

Assigns instance with full hierarchical path "x|y|z" to non-rectangular L-shaped Logic Lock region. The software treats each set of four numbers as a new box.

```
set_instance_assignment -name PLACE_REGION -to x|y|z "X10 Y10 X20 Y50; X20 Y10 X50 Y20"
```

Example 3. Assign Subordinate Logic Lock Instances

By default, the Quartus Prime software constrains every child instance to the Logic Lock region of its parent. Any constraint to a child instance intersects with the constraint of its ancestors. For example, in the following example, all logic beneath "a|b|c|d" constrains to box (10,10), (15,15), and not (0,0), (15,15). This result occurs because the child constraint intersects with the parent constraint.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"  
set_instance_assignment -name PLACE_REGION -to a|b|c|d "X0 Y0 X15 Y15"
```

Example 4. Assign Multiple Logic Lock Instances

By default, a Logic Lock region constraint allows logic from other instances to share the same region. These assignments place instance c and instance g in the same location. This strategy is useful if instance c and instance g are heavily interacting.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"  
set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X20 Y20"
```

Example 5. Assigned Reserved Logic Lock Regions

Optionally reserve an entire Logic Lock region for one instance and any of its subordinate instances.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"  
set_instance_assignment -name RESERVE_PLACE_REGION -to a|b|c ON  
  
# The following assignment causes an error. The logic in e|f|g is not  
# legally placeable anywhere:  
# set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X20 Y20"  
  
# The following assignment does *not* cause an error, but is effectively  
# constrained to the box (20,10), (30,20), since the (10,10),(20,20) box is  
# reserved  
# for a|b|c  
set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X30 Y20"
```

3.2.2.5. Modifying Signal Tap Logic Analyzer Files

Quartus Prime Pro Edition introduces new methodology for entity names, settings, and assignments. These changes impact the processing of Signal Tap Logic Analyzer Files (.stp).

If you migrate a project that includes .stp files generated by other Quartus software products, you must make the following changes to migrate to the Quartus Prime Pro Edition:

1. Remove entity names from .stp files. The Signal Tap Logic Analyzer allows without error, but ignores, entity names in .stp files. Remove entity names from .stp files for migration to Quartus Prime Pro Edition:
 - a. Click **View > Node Finder** to locate and remove appropriate nodes. Use Node Finder options to filter on nodes.
 - b. Click **Processing > Start > Start Analysis & Elaboration** to repopulate the database and add valid node names.
2. Remove post-fit nodes. Quartus Prime Pro Edition uses a different post-fit node naming scheme than other Quartus software products.
 - a. Remove post-fit tap node names originating from other Quartus software products.
 - b. Click **View > Node Finder** to locate and remove post-fit nodes. Use Node Finder options to filter on nodes.
 - c. Click **Processing > Start Compilation** to repopulate the database and add valid post-fit nodes.
3. Run an initial compilation in Quartus Prime Pro Edition from the GUI. The Compiler automatically removes Signal Tap assignments originating other Quartus software products. Alternatively, from the command-line, run `quartus_stp` once on the project to remove outmoded assignments.

Note: `quartus_stp` introduces no migration impact in the Quartus Prime Pro Edition. Your scripts require no changes to `quartus_stp` for migration.
4. Modify .sdc constraints for JTAG. Quartus Prime Pro Edition does not support embedded .sdc constraints for JTAG signals. Modify the timing template to suit the design's JTAG driver and board.

3.2.2.6. Removing References to .qip Files

In Quartus Prime Standard Edition projects, Platform Designer (Standard) generates .qip files. These files describe the parameterized IP cores to the Compiler, and appear as assignments in the project's .qsf file. However, in Quartus Prime Pro Edition projects, the parameterized IP core description occurs in .ip files. Moreover, references to .qip files in a project's .qsf file cause synthesis errors during compilation.

- When migrating a project to Quartus Prime Pro Edition, remove all references to .qip files from the .qsf file.

3.2.2.7. Removing Unsupported Feature Assignments

The Quartus Prime Pro Edition software does not support some feature assignments that other Quartus software products support. Remove the following unsupported feature assignments from other Quartus software product .qsf files for migration to the Quartus Prime Pro Edition software.

- Incremental Compilation (partitions)—The current version of the Quartus Prime Pro Edition software does not support Quartus Prime Standard Edition incremental compilation. Remove all incremental compilation feature assignments from other Quartus software product .qsf files before migration.
- Quartus Prime Standard Edition Physical synthesis assignments. Quartus Prime Pro Edition software does not support Quartus Prime Standard Edition Physical synthesis assignments. Remove any of the following assignments from the .qsf file or design RTL (instance assignments) before migration.

```

PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA
PHYSICAL_SYNTHESIS_COMBO_LOGIC
PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION
PHYSICAL_SYNTHESIS_REGISTER_RETIMING
PHYSICAL_SYNTHESIS_ASYNCHRONOUS_SIGNAL_PIPELINING
PHYSICAL_SYNTHESIS_MAP_LOGIC_TO_MEMORY_FOR_AREA
  
```

Note: If you open a Quartus Prime Standard Edition software project in the Quartus Prime Pro Edition software, and that project contains unsupported junction temperature setting values, you can modify these settings by clicking **Assignments > Settings > Operating Settings and Conditions > Temperature**. Click **OK**, and then click **Yes** when prompted to update the values.

3.2.3. Upgrading IP Cores and Platform Designer Systems

Upgrade all IP cores and Platform Designer systems in your project for migration to the Quartus Prime Pro Edition software. The Quartus Prime Pro Edition software uses standards-compliant methodology for instantiation and generation of IP cores and Platform Designer systems. Most Intel FPGA IP cores and Platform Designer systems upgrade automatically in the **Upgrade IP Components** dialog box.

Other Quartus software products use a proprietary Verilog configuration scheme within the top level of IP cores and Platform Designer systems for synthesis files. The Quartus Prime Pro Edition does not support this scheme. To upgrade all IP cores and Platform Designer systems in your project, click **Project > Upgrade IP Components**.⁽²⁾

Table 13. IP Core and Platform Designer System Differences

Other Quartus Software Products	Quartus Prime Pro Edition
IP and Platform Designer system generation use a proprietary Verilog HDL configuration scheme within the top level of IP cores and Platform Designer systems for synthesis files. This proprietary Verilog HDL configuration scheme prevents RTL entities from ambiguous instantiation errors during synthesis. However, these errors may manifest in simulation. Resolving this issue requires writing a Verilog HDL configuration to disambiguate the instantiation, delete the duplicate entity from the project, or rename one of the conflicting entities. Quartus Prime Pro Edition IP strategy resolves these issues.	<p>IP and Platform Designer system generation does not use proprietary Verilog HDL configurations. The compilation library scheme changes in the following ways:</p> <ul style="list-style-type: none"> • Compiles all variants of an IP core into the same compilation library across the entire project. Quartus Prime Pro Edition identically names IP cores with identical functionality and parameterization to avoid ambiguous entity instantiation errors. For example, the files for every Arria 10 PCI Express* IP core variant compile into the <code>altera_pcie_a10_hip_151</code> compilation library. • Simulation and synthesis file sets for IP cores and systems instantiate entities in the same manner. • The generated RTL directory structure now matches the compilation library structure.

⁽²⁾ For brevity, this section refers to Quartus Prime Standard Edition, Intel Quartus Prime Lite Edition, and the Quartus II software collectively as "other Quartus software products."

Note: For complete information on upgrading IP cores, refer to *Managing Quartus Prime Projects*.

Related Information

- [Working With Intel FPGA IP Cores](#) on page 50
- [Managing Quartus Prime Projects](#) on page 85

3.2.4. Upgrading Non-Compliant Design RTL

The Quartus Prime Pro Edition software introduces a new synthesis engine (`quartus_syn` executable).

The `quartus_syn` synthesis enforces stricter industry-standard HDL structures and supports the following enhancements in this release:

- Support for modules with SystemVerilog Interfaces
- Improved support for VHDL2008
- New RAM inference engine infers RAMs from GENERATE statements or array of integers
- Stricter syntax/semantics check for improved compatibility with other EDA tools

Account for these synthesis differences in existing RTL code by ensuring that your design uses standards-compliant VHDL, Verilog HDL, or SystemVerilog. The Compiler generates errors when processing non-compliant RTL. Use the guidelines in this section to modify existing RTL for compatibility with the Quartus Prime Pro Edition synthesis.

Related Information

- [Verifying Verilog Compilation Unit](#) on page 40
- [Updating Entity Auto-Discovery](#) on page 41
- [Ensuring Distinct VHDL Namespace for Each Library](#) on page 42
- [Removing Unsupported Parameter Passing](#) on page 42
- [Removing Unsized Constant from WYSIWYG Instantiation](#) on page 42
- [Removing Non-Standard Pragmas](#) on page 43
- [Declaring Objects Before Initial Values](#) on page 43
- [Confining SystemVerilog Features to SystemVerilog Files](#) on page 43
- [Avoiding Assignment Mixing in Always Blocks](#) on page 44
- [Avoiding Unconnected, Non-Existent Ports](#) on page 44
- [Avoiding Invalid Parameter Ranges](#) on page 44
- [Updating Verilog HDL and VHDL Type Mapping](#) on page 45

3.2.4.1. Verifying Verilog Compilation Unit

Quartus Prime Pro Edition synthesis uses a different method to define the compilation unit. The Verilog LRM defines the concept of compilation unit as “a collection of one or more Verilog source files compiled together” forming the compilation-unit scope. Items visible only in the compilation-unit scope include macros, global declarations,

and default net types. The contents of included files become part of the compilation unit of the parent file. Modules, primitives, programs, interfaces, and packages are visible in all compilation units. Ensure that your RTL accommodates these changes.

Table 14. Verilog Compilation Unit Differences

Other Quartus Software Products	Quartus Prime Pro Edition
Synthesis in other Quartus software products follows the Multi-file compilation unit (MFCU) method to select compilation unit files. In MFCU, all files compile in the same compilation unit. Global definitions and directives are visible in all files. However, the default net type is reset at the start of each file.	Quartus Prime Pro Edition synthesis follows the Single-file compilation unit (SFCU) method to select compilation unit files. In SFCU, each file is a compilation unit, file order is irrelevant, and the macro is only defined until the end of the file.

Note: You can optionally change the MFCU mode using the following assignment:
`set_global_assignment -name VERILOG_CU_MODE MFCU`

3.2.4.1.1. Verilog HDL Configuration Instantiation

Quartus Prime Pro Edition synthesis requires instantiation of the Verilog HDL configuration, and not the module. In other Quartus software products, synthesis automatically finds any Verilog HDL configuration relating to a module that you instantiate. The Verilog HDL configuration then instantiates the design.

If your top-level entity is a Verilog HDL configuration, set the Verilog HDL configuration, rather than the module, as the top-level entity.

Table 15. Verilog HDL Configuration Instantiation

Other Quartus Software Products	Quartus Prime Pro Edition
From the Example RTL, synthesis automatically finds the <code>mid_config</code> Verilog HDL configuration relating to the instantiated module.	From the Example RTL, synthesis does not find the <code>mid_config</code> Verilog HDL configuration. You must instantiate the Verilog HDL configuration directly.
Example RTL: <pre> config mid_config; design good_lib.mid; instance mid.sub_inst use good_lib.sub; endconfig module test (input a1, output b); mid_config mid_inst (.a1(a1), .b(b)); // in other Quartus products preceding line would have been: //mid mid_inst (.a1(a1), .b(b)); endmodule module mid (input a1, output b); sub sub_inst (.a1(a1), .b(b)); endmodule </pre>	

3.2.4.2. Updating Entity Auto-Discovery

All editions of the Quartus Prime and Quartus II software search your project directory for undefined entities. For example, if you instantiate entity "sub" in your design without specifying "sub" as a design file in the Quartus Settings File (`.qsf`), synthesis searches for `sub.v`, `sub.vhd`, and so on. However, Quartus Prime Pro Edition performs auto-discovery at a different stage in the flow. Ensure that your RTL code accommodates these auto-discovery changes.

Table 16. Entity Auto-Discovery Differences

Other Quartus Software Products	Quartus Prime Pro Edition
Always automatically searches your project directory and search path for undefined entities.	Always automatically searches your project directory and search path for undefined entities. Quartus Prime Pro Edition synthesis performs auto-discovery earlier in the flow than other Quartus software products. This results in discovery of more syntax errors. Optionally disable auto-discovery with the following .qsf assignment: <code>set_global_assignment -name AUTO_DISCOVER_AND_SORT OFF</code>

3.2.4.3. Ensuring Distinct VHDL Namespace for Each Library

Quartus Prime Pro Edition synthesis requires that VHDL namespaces are distinct for each library. The stricter library binding requirement complies with VHDL language specifications and results in deterministic behavior. This benefits team-based projects by avoiding unintentional name collisions. Confirm that your RTL respects this change.

Table 17. VHDL Namespace Differences

Other Quartus Software Products	Quartus Prime Pro Edition
For the Example RTL, the analyzer searches all libraries in an unspecified order until the analyzer finds package <code>utilities_pack</code> and uses items from that package. If another library, for example <code>projectLib</code> also contains <code>utilities_pack</code> , the analyzer may use this library instead of <code>myLib.utilities_pack</code> if found before the analyzer searches <code>myLib</code> .	For the Example RTL, the analyzer uses the specific <code>utilities_pack</code> in <code>myLib</code> . If <code>utilities_pack</code> does not exist in library <code>myLib</code> , the analyzer generates an error.
Example RTL: <pre>library myLib; use myLib.utilities_pack.all;</pre>	

3.2.4.4. Removing Unsupported Parameter Passing

Quartus Prime Pro Edition synthesis does not support parameter passing using `set_parameter` in the .qsf. Synthesis in other Quartus software products supports passing parameters with this method. Except for the top-level of the design where permitted, ensure that your RTL does not depend on this type of parameter passing.

Table 18. SystemVerilog Feature Differences

Other Quartus Software Products	Quartus Prime Pro Edition
From the Example RTL, synthesis overwrites the value of parameter <code>SIZE</code> in the instance of <code>my_ram</code> instantiated from entity <code>mid_level</code> .	From the Example RTL, synthesis generates a syntax error for detection of parameter passing assignments in the .qsf. Specify parameters in the RTL. The following example shows the supported top-level parameter passing format. This example applies only to the top-level and sets a value of 4 to parameter <code>N</code> : <code>set_parameter -name N 4</code>
Example RTL: <pre>set_parameter -entity mid_level -to my_ram -name SIZE 16</pre>	

3.2.4.5. Removing Unsized Constant from WYSIWYG Instantiation

Quartus Prime Pro Edition synthesis does not allow use of an unsized constant for WYSIWYG instantiation. Synthesis in other Quartus software products allows use of SystemVerilog (.sv) unsized constants when instantiating a WYSIWYG in a .v file.

Quartus Prime Pro Edition synthesis allows use of unsized constants in .sv files for uses other than WYSIWYG instantiation. Ensure that your RTL code does not use unsized constants for WYSIWYG instantiation. For example, specify a sized literal, such as 2'b11, rather than '1.

3.2.4.6. Removing Non-Standard Pragmas

Quartus Prime Pro Edition synthesis does not support the `vhdl(verilog)_input_version` pragma or the `library` pragma. Synthesis in other Quartus software products supports these pragmas. Remove any use of the pragmas from RTL for Quartus Prime Pro Edition migration. Use the following guidelines to implement the pragma functionality in Quartus Prime Pro Edition:

- `vhdl(verilog)_input_version` Pragma—allows change to the input version in the middle of an input file. For example, to change VHDL 1993 to VHDL 2008. For Quartus Prime Pro Edition migration, specify the input version for each file in the .qsf.
- `library` Pragma—allows changes to the VHDL library into which files compile. For Quartus Prime Pro Edition migration, specify the compilation library in the .qsf.

3.2.4.7. Declaring Objects Before Initial Values

Quartus Prime Pro Edition synthesis requires declaration of objects before initial value. Ensure that your RTL declares objects before initial value. Other Quartus software products allow declaration of initial value prior to declaration of the object.

Table 19. Object Declaration Differences

Other Quartus Software Products	Quartus Prime Pro Edition
From the Example RTL, synthesis initializes the output <code>p_prog_iol</code> with the value of <code>p_prog_iol_reg</code> , even though the register declaration occurs in Line 2.	From the Example RTL, synthesis generates a syntax error when you specify initial values before declaring the register.
Example RTL: <pre>1 output p_prog_iol = p_prog_iol_reg; 2 reg p_prog_iol_reg;</pre>	

3.2.4.8. Confining SystemVerilog Features to SystemVerilog Files

Quartus Prime Pro Edition synthesis does not allow SystemVerilog features in Verilog HDL files. Other Quartus software products allow use of a subset of SystemVerilog (.sv) features in Verilog HDL (.v) design files. To avoid syntax errors in Quartus Prime Pro Edition, allow only SystemVerilog features in Verilog HDL files.

To use SystemVerilog features in your existing Verilog HDL files, rename your Verilog HDL (.v) files as SystemVerilog (.sv) files. Alternatively, you can set the file type in the .qsf, as shown in the following example:

```
set_global_assignment -name SYSTEMVERILOG_FILE <file>.v
```

Table 20. SystemVerilog Feature Differences

Other Quartus Software Products	Quartus Prime Pro Edition
From the Example RTL, synthesis interprets <code>\$clog2</code> in a <code>.v</code> file, even though the Verilog LRM does not define the <code>\$clog2</code> feature. Other Quartus software products allow other SystemVerilog features in <code>.v</code> files.	From the Example RTL, synthesis generates a syntax error for detection of any non-Verilog HDL construct in <code>.v</code> files. Quartus Prime Pro Edition synthesis honors SystemVerilog features only in <code>.sv</code> files.
<p>Example RTL:</p> <pre>localparam num_mem_locations = 1050; wire mem_addr [\$clog2(num_mem_locations)-1 : 0];</pre>	

3.2.4.9. Avoiding Assignment Mixing in Always Blocks

Quartus Prime Pro Edition synthesis does not allow mixed use of blocking and non-blocking assignments within `ALWAYS` blocks. Other Quartus software products allow mixed use of blocking and non-blocking assignments within `ALWAYS` blocks. To avoid syntax errors, ensure that `ALWAYS` block assignments are of the same type for Quartus Prime Pro Edition migration.

Table 21. ALWAYS Block Assignment Differences

Other Quartus Software Products	Quartus Prime Pro Edition
Synthesis honors the mixed blocking and non-blocking assignments, although the Verilog Language Specification no longer supports this construct.	Synthesis generates a syntax error for detection of mixed blocking and non-blocking assignments within an <code>ALWAYS</code> block.

3.2.4.10. Avoiding Unconnected, Non-Existent Ports

Quartus Prime Pro Edition synthesis requires that a port exists in the module prior to instantiation and naming. Other Quartus software products allow you to instantiate and name an unconnected port that does not exist in the module. Modify your RTL to match this requirement.

To avoid syntax errors, remove all unconnected and non-existent ports for Quartus Prime Pro Edition migration.

Table 22. Unconnected, Non-Existent Port Differences

Other Quartus Software Products	Quartus Prime Pro Edition
Synthesis allows you to instantiate and name unconnected or non-existent ports that do not exist on the module.	Synthesis generates a syntax error for detection of mixed blocking and non-blocking assignments within an <code>ALWAYS</code> block.

3.2.4.11. Avoiding Invalid Parameter Ranges

Quartus Prime Pro Edition synthesis generates an error for detection of constant numeric (integer or floating point) parameter values that exceed the language specification. Other Quartus software products allow constant numeric (integer or floating point) values for parameters that exceed the language specifications. To avoid syntax errors, ensure that constant numeric (integer or floating point) values for parameters conform to the language specifications.

3.2.4.12. Updating Verilog HDL and VHDL Type Mapping

Quartus Prime Pro Edition synthesis requires that you use 0 for "false" and 1 for "true" in Verilog HDL files (.v). Other Quartus software products map "true" and "false" strings in Verilog HDL to TRUE and FALSE Boolean values in VHDL. Quartus Prime Pro Edition synthesis generates an error for detection of non-Verilog HDL constructs in .v files. To avoid syntax errors, ensure that your RTL accommodates these standards.

3.2.4.13. Converting Symbolic BDF Files to Acceptable File Formats

Starting from the Quartus Prime Pro Edition software version 23.3, the compiler cannot synthesize schematic Block Design File (.bdf). You must convert it to an acceptable format, such as Verilog HDL or VHDL using the Intel Quartus Prime Standard Edition command `quartus_map` as shown in the following:

- To convert your .bdf file to Verilog Design File (.v):

```
quartus_map <project_name> --convert_bdf_to_verilog=<bdf_file_name>
```

- To convert your .bdf file to VHDL Design File (.vhd):

```
quartus_map <project_name> --convert_bdf_to_vhdl=<bdf_file_name>
```

3.3. Migrating Your AMD* Vivado* Project to Quartus Prime Pro Edition

Designing for Intel FPGA devices is similar in concept and practice to designing for AMD* Xilinx* FPGA devices. In most cases, you can import your RTL into the Quartus Prime Pro Edition software and compile your design to the target device.

Refer to the [AN 307: Intel FPGA Design Flow for AMD* Xilinx* Users](#), which covers the following information:

- A comparison of the current AMD* Xilinx* and Intel FPGA technologies, features, and devices available for different process technologies.
- A comparison between the design flows in the AMD* Vivado* software and Quartus Prime Pro Edition software.
- Guidelines to convert AMD* Vivado* designs to the Quartus Prime Pro Edition software, including AMD* Xilinx* IP catalog modules and instantiated primitives.
- Guidelines to translate device and design constraints.

3.4. Migrating Projects Across Operating Systems

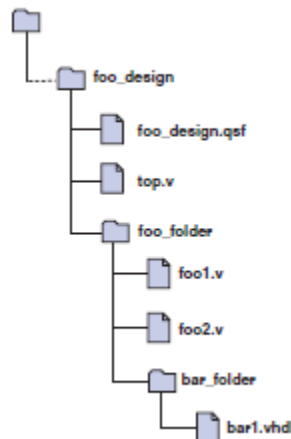
Consider the following cross-platform issues when moving your project from one operating system to another (for example, from Windows* to Linux*).

3.4.1. Migrating Design Files and Libraries

Consider file naming differences when migrating projects across operating systems.

- Use appropriate case for your platform in file path references.
- Use a character set common to both platforms.
- Do not change the forward-slash (/) and back-slash (\) path separators in the .qsf. The Quartus Prime software automatically changes all back-slash (\) path separators to forward-slashes (/) in the .qsf.
- Observe the target platform's file name length limit.
- Use underscore instead of spaces in file and directory names.
- Change library absolute path references to relative paths in the .qsf.
- Ensure that any external project library exists in the new platform's file system.
- Specify file and directory paths as relative to the project directory. For example, for a project titled `foo_design`, specify the source files as: `top.v`, `foo_folder /foo1.v`, `foo_folder /foo2.v`, and `foo_folder /bar_folder/bar1.vhdl`.
- Ensure that all the subdirectories are in the same hierarchical structure and relative path as in the original platform.

Figure 14. All Inclusive Project Directory Structure

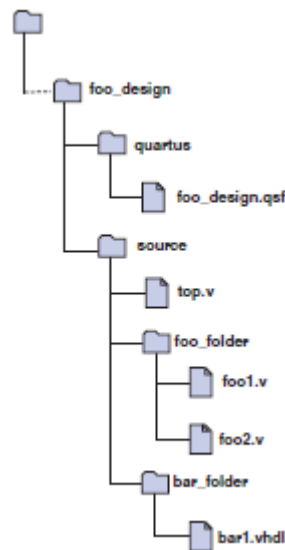


3.4.1.1. Use Relative Paths

Express file paths using relative path notation (`./`).

For example, in the directory structure shown you can specify `top.v` as `../source/top.v` and `foo1.v` as `../source/foo_folder/foo1.v`.

Figure 15. Quartus Prime Project Directory Separate from Design Files



3.4.2. Design Library Migration Guidelines

The following guidelines apply to library migration across computing platforms:

1. The project directory takes precedence over the project libraries.
2. For Linux, the Quartus Prime software creates the file in the `altera.quartus` directory under the `<home>` directory.
3. All library files are relative to the libraries. For example, if you specify the `user_lib1` directory as a project library and you want to add the `/user_lib1/foo1.v` file to the library, you can specify the `foo1.v` file in the `.qsf` as `foo1.v`. The Quartus Prime software includes files in specified libraries.
4. If the directory is outside of the project directory, an absolute path is created by default. Change the absolute path to a relative path before migration.
5. When copying projects that include libraries, you must either copy your project library files along with the project directory or ensure that your project library files exist in the target platform.
 - On Windows*, the Quartus Prime software searches for the `quartus2.ini` file in the following directories and order:
 - `USERPROFILE`, for example, `C:\Documents and Settings\<user name>`
 - Directory specified by the `TMP` environmental variable
 - Directory specified by the `TEMP` environmental variable
 - Root directory, for example, `C:\`

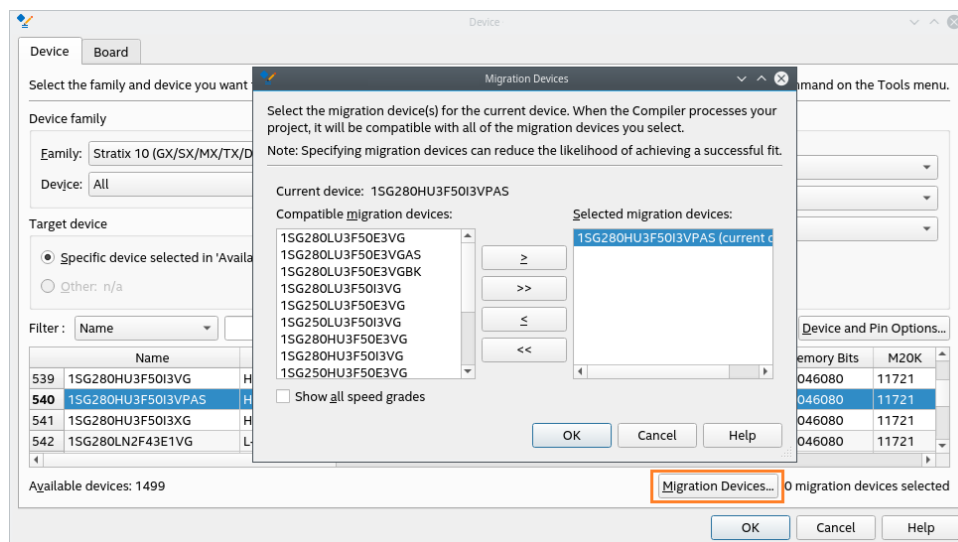
3.5. Migrating Project From One Device to Another

The Quartus Prime Pro Edition software supports migrating project from one device to another by providing a list of compatible migration devices available for the device your design targets.

To migrate your device, launch **Migration Devices** using one of the following options in the Quartus Prime Pro Edition software GUI:

- Right-click on your device in the **Project Navigator** and select **Device ► Migration Devices**.
- **Assignments ► Device ► Migration Devices**

Figure 16. Device Migration



In the **Migration Devices** dialog box, click **>**, **>>**, **<**, and **<<** to move migration devices between the **Compatible migration devices** list and the **Selected migration devices** list.

A device name in the **Selected migration devices** list with the text (current device) indicates that the device is currently specified in the **Available devices** list in the **Device** dialog box.

A device name in the **Compatible migration devices** list with the text (not installed) indicates that the device is supported in the Quartus Prime Pro Edition software, but support for the device is not installed in your copy of the software. To move this device to the **Selected migration devices** list, you must first install support for the device by running a custom installation procedure of the Quartus Prime software. For more information, refer to the [Downloading Device Support](#) in the *Intel FPGA Software Installation and Licensing* or contact [Intel Support](#).

If you want the Quartus Prime software to display all compatible migration devices in the **Compatible migration devices** list regardless of a migration device's speed grade, turn on the **Show All Speed Grades** checkbox. If you want the Quartus Prime software to display in the **Compatible migration devices** list only the compatible migration devices that have the same speed grade as the target device, turn off **Show all speed grades**.

Related Information

- [Migrating to the Quartus Prime Pro Edition Software](#)
- [AN 822: Intel FPGA Configuration Device Migration Guideline](#)

3.6. Related Trainings

You can take up the following training to help you select your starting point for your project:

- [Getting Started with the Quartus Prime New Project Wizard](#)
- [Creating a New Project with Quartus Prime Pro Edition Software](#)
- [Migrating to the Quartus Prime Pro Edition Software](#)
- [Migrating an Quartus Prime Project to a Different Intel FPGA Device](#)
- [Quartus Prime Software Pin Migration](#)
- [Preserve Compilation Results for migration to newer Quartus Prime Software releases](#)

4. Working With Intel FPGA IP Cores

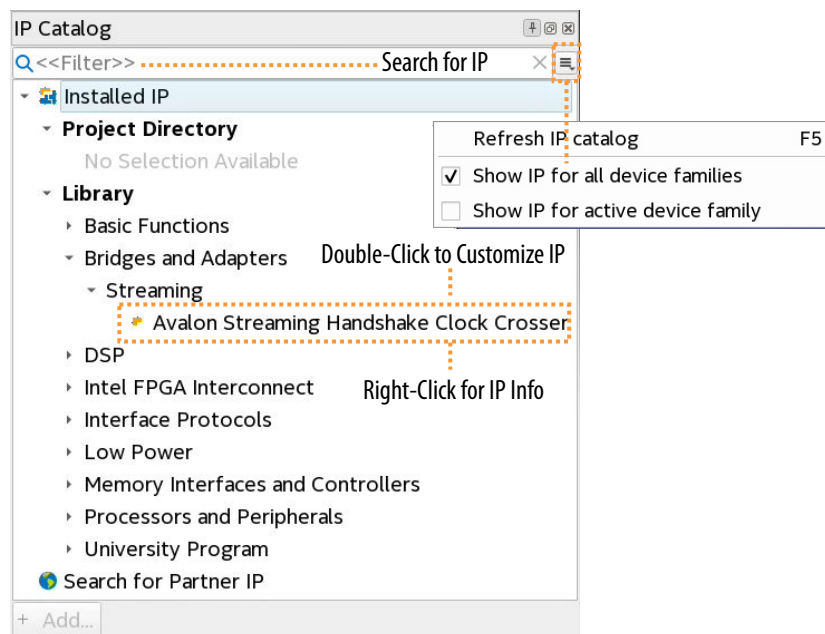
Intel and strategic IP partners offer a broad portfolio of configurable IP cores optimized for Intel FPGA devices.

The Quartus Prime software installation includes the Intel FPGA IP library. Integrate optimized and verified Intel FPGA IP cores into your design to shorten design cycles and maximize performance. The Quartus Prime software also supports integration of IP cores from other sources. Use the IP Catalog (**Tools > IP Catalog**) to efficiently parameterize and generate synthesis and simulation files for your custom IP variation. The Intel FPGA IP library includes the following types of IP cores:

Basic functions	Interface protocols
Bridges and adapters	Low power functions
DSP functions	Memory interfaces and controllers
Intel FPGA interconnect	Processors and peripherals

This document provides basic information about parameterizing, generating, upgrading, and simulating stand-alone IP cores in the Quartus Prime software.

Figure 17. Intel FPGA IP Catalog



Navigating Content Through Tasks

Use the following navigation diagram to navigate this guide through user-tasks:



4.1. IP Catalog and Parameter Editor

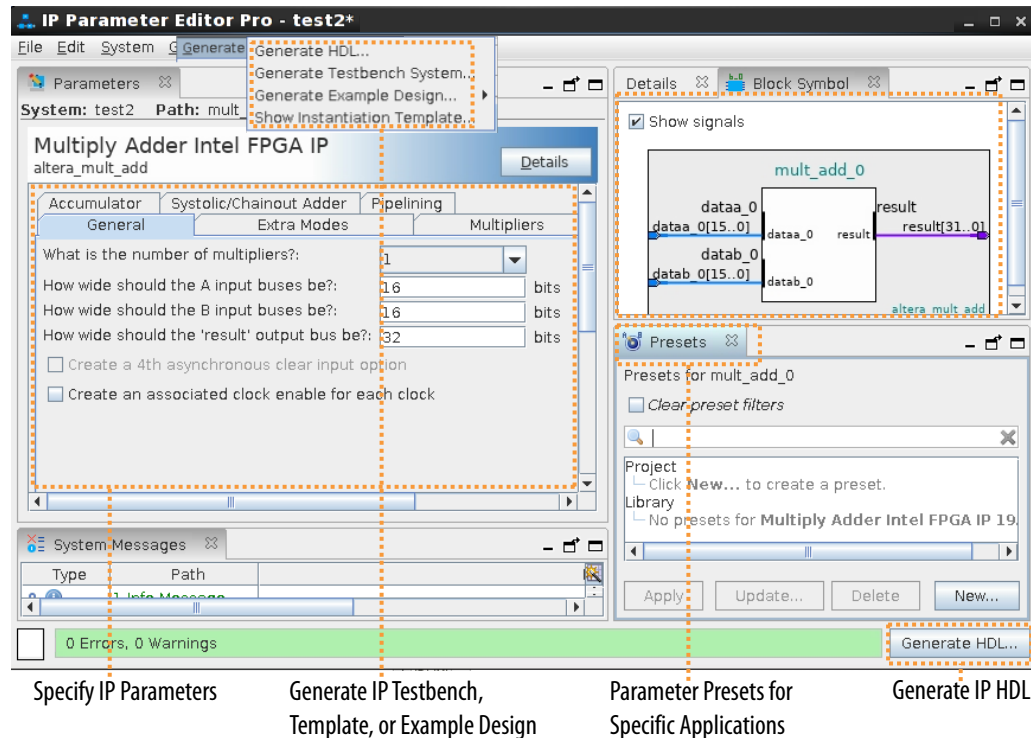
The IP Catalog displays the IP cores available for your project, including Intel FPGA IP and other IP that you add to the IP Catalog search path. Use the following features of the IP Catalog to locate and customize an IP core:

- Filter IP Catalog to **Show IP for active device family** or **Show IP for all device families**. If you have no project open, select the **Device Family** in IP Catalog.
- Type in the Search field to locate any full or partial IP core name in IP Catalog.
- Right-click an IP core name in IP Catalog to display details about supported devices, to open the IP core's installation folder, and for links to IP documentation.
- Click **Search for Partner IP** to access partner IP information on the web.

The parameter editor prompts you to specify an IP variation name, optional ports, and output file generation options. The parameter editor generates a top-level Quartus Prime IP file (.qip) for an IP variation in Quartus Prime Pro Edition projects. This file represents the IP variation in the project, and stores parameterization information.⁽³⁾

⁽³⁾ The parameter editor generates a top-level Quartus IP file (.qip) for an IP variation in Quartus Prime Standard Edition projects.

Figure 18. Example IP Parameter Editor



4.1.1. The Parameter Editor

The parameter editor helps you to configure IP core ports, parameters, and output file generation options. The basic parameter editor controls include the following:

- Use the **Presets** window to apply preset parameter values for specific applications (for select cores).
- Use the **Details** window to view port and parameter descriptions, and click links to documentation.
- Click **Generate** ► **Generate Testbench System** to generate a testbench system (for select cores).
- Click **Generate** ► **Generate Example Design** to generate an example design (for select cores).
- Click **Validate System Integrity** to validate a system's generic components against companion files. (Platform Designer systems only)
- Click **Sync All System Info** to validate a system's generic components against companion files. (Platform Designer systems only)

The IP Catalog is also available in Platform Designer (**View** ► **IP Catalog**). The Platform Designer IP Catalog includes exclusive system interconnect, video and image processing, and other system-level IP that are not available in the Quartus Prime IP Catalog. Refer to *Creating a System with Platform Designer* or *Creating a System with Platform Designer* for information on use of IP in Platform Designer and Platform Designer, respectively.

Related Information

Creating a System with Platform Designer

4.2. Installing and Licensing Intel FPGA IP Cores

The Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Quartus Prime software installs IP cores in the following locations by default:

Figure 19. IP Core Installation Path

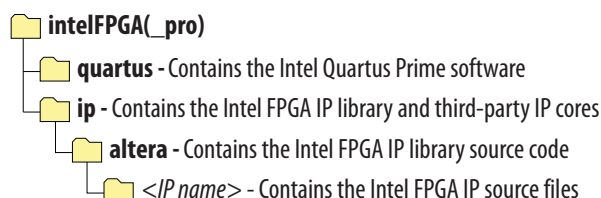


Table 23. IP Core Installation Locations

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\altera	Quartus Prime Pro Edition	Windows
<drive>:\intelFPGA\quartus\ip\altera	Quartus Prime Standard Edition	Windows
<home directory>:/intelFPGA_pro/quartus/ip/altera	Quartus Prime Pro Edition	Linux*
<home directory>:/intelFPGA/quartus/ip/altera	Quartus Prime Standard Edition	Linux

Note: The Quartus Prime software does not support spaces in the installation path.

4.2.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

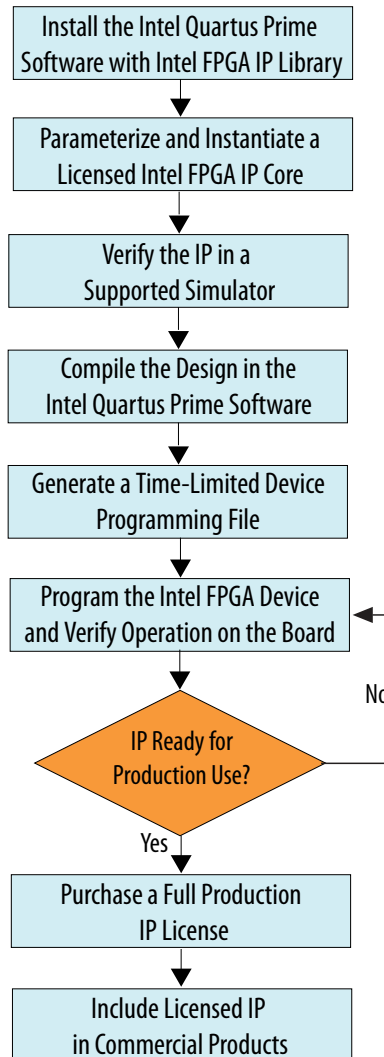
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Quartus Prime software, and requires no Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit.

Figure 20. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the [Intel FPGA Self-Service Licensing Center](#).

The [Intel FPGA Software License Agreements](#) govern the installation and use of licensed IP cores, the Quartus Prime design software, and all unlicensed IP cores.

Related Information

- [Intel FPGA Licensing Support Center](#)
- [Introduction to Intel FPGA Software Installation and Licensing](#)

4.2.1.1. Intel FPGA IP Versioning

Intel FPGA IP versions match the Quartus Prime Design Suite software versions until v19.1. Starting in Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

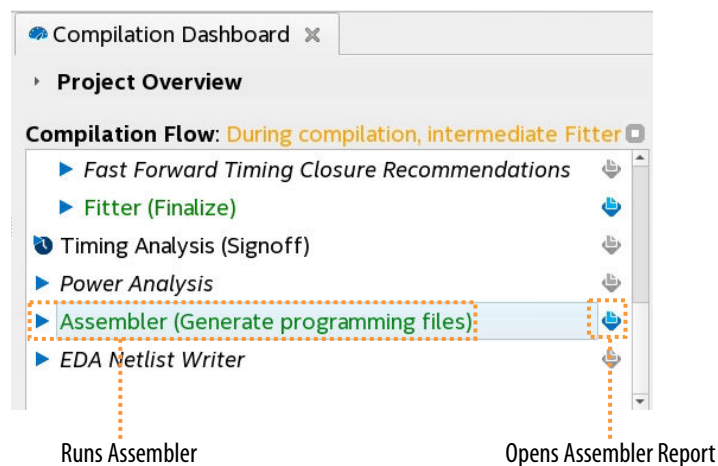
4.2.1.2. Checking the IP License Status

You can check the license status of all IP in an Quartus Prime project by viewing the Assembler report.

To generate and view the Assembler report in the GUI:

1. Click **Assembler** on the Compilation Dashboard.
2. When the Assembler (and any prerequisite stages of compilation) complete, click the **Report** icon for the Assembler in the Compilation Dashboard.

Figure 21. Assembler Report Icon in Compilation Dashboard



3. Click the **Encrypted IP Cores Summary** report.

Figure 22. Encrypted IP Cores Summary Report

Assembler Encrypted IP Cores Summary			
Show:	Visible ▾	Hide	Q <<Filter>>
	Vendor	IP Core Name	License Type
1	Intel FPGA	Signal Tap (6AF7 BCE1)	Licensed
2	Intel FPGA	Signal Tap (6AF7 BCEC)	Licensed

To generate and view the Assembler report at the command line:

1. Type the following command:

```
quartus_asm <project name> -c <project revision>
```

2. View the output report in /output_files/<project_name>.asm.rpt.

```
+-----+-----+-----+
; Assembler Encrypted IP Cores Summary
+-----+-----+-----+
; Vendor ; IP Core Name ; License Type ;
+-----+-----+-----+
; Intel ; PCIe SRIOV with 4-PFs and 2K-VFs (6AF7 00FB) ; Unlicensed ;
; Intel ; Signal Tap (6AF7 BCE1) ; Licensed ;
; Intel ; Signal Tap (6AF7 BCEC) ; Licensed ;
+-----+-----+-----+
```

4.3. IP General Settings

The following settings control how the Quartus Prime software manages IP cores in a project:

Table 24. Location of IP Core General Settings in the Quartus Prime Software

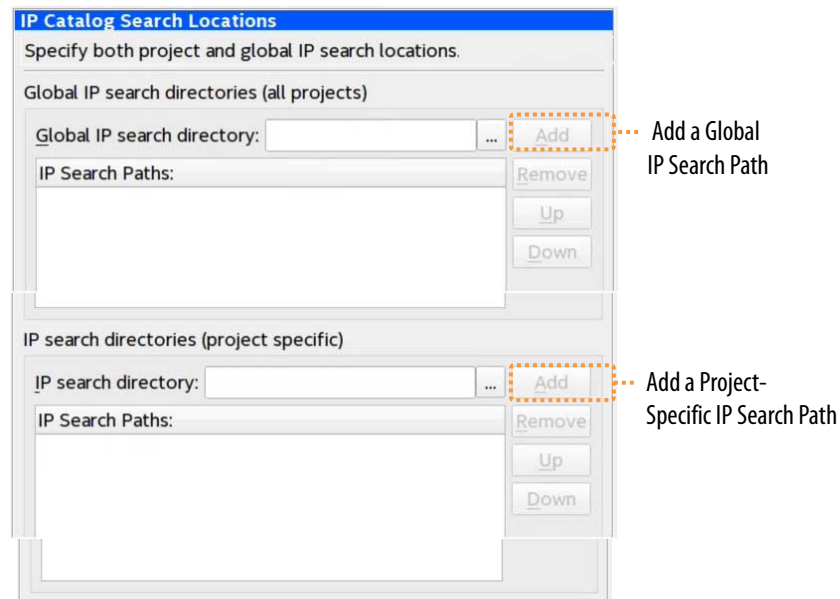
Setting	Description	Location
Maximum Platform Designer memory usage size	Increase if you experience slow processing for large systems, or for out of memory errors.	Tools > Options > IP Settings Or Tasks pane > Settings > IP Settings
IP generation HDL preference	The parameter editor generates the HDL you specify for IP variations.	
IP Regeneration Policy	Controls when synthesis files regenerate for each IP variation. Typically, you Always regenerate synthesis files for IP cores after making changes to an IP variation.	
Generate IP simulation model when generating IP	Enables automatic generation of simulation models every time you generate the IP.	
Use available processors for parallel generation of Quartus project IPs	Directs Platform Designer to generate IPs in parallel, using the number of processors that you specify in the Compilation Process Settings pane of the Quartus Prime project settings.	
Additional project and global IP search locations.	The Quartus Prime software searches for IP cores in the project directory, in the Quartus Prime installation directory, and in the IP search path.	Tools > Options > IP Catalog Search Locations Or Tasks pane > Settings > IP Catalog Search Locations

4.4. Adding IP to IP Catalog

The IP Catalog automatically displays Intel FPGA IP and other IP components that have a corresponding `_hw.tcl` or `.ipx` file located in the project directory, in the default Quartus Prime installation directory, or in the IP search path. You can optionally add your own custom or third-party IP component to IP Catalog by adding the component's `_hw.tcl` or `.ipx` file to the IP search path.

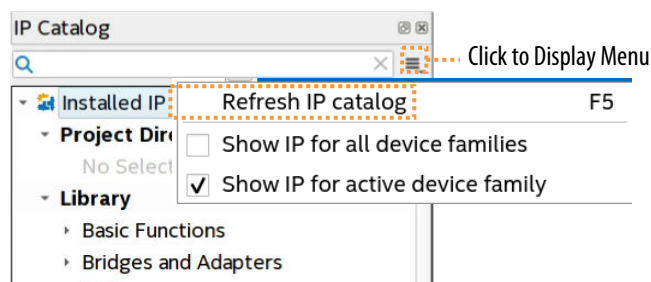
Follow these steps to add custom or third-party IP to the IP Catalog:

Figure 23. Specifying IP Search Locations



1. In the Quartus Prime software, click **Tools > Options > IP Search Path** to open the **IP Search Path Options** dialog box.
2. Click **Add** or **Remove** to add/remove a location that contains IP.
3. To refresh the IP Catalog, click **Refresh IP Catalog** in the Quartus Prime Platform Designer, or click **File > Refresh System** in Platform Designer.

Figure 24. Refreshing IP Catalog



4.5. Best Practices for Intel FPGA IP

Use the following best practices when working with Intel FPGA IP:

- Do not manually edit or write your own `.qsys`, `.ip`, or `.qip` file. Use the Quartus Prime software tools to create and edit these files.

Note: When generating IP cores, do not generate files into a directory that has a space in the directory name or path. Spaces are not legal characters for IP core paths or names.

- When you generate an IP core using the IP Catalog, the Quartus Prime software generates a `.qsys` (for Platform Designer-generated IP cores) or a `.ip` file (for Quartus Prime Pro Edition) or a `.qip` file. The Quartus Prime Pro Edition software automatically adds the generated `.ip` to your project. In the Quartus Prime Standard Edition software, add the `.qip` to your project. Do not add the parameter editor generated file (`.v` or `.vhd`) to your design without the `.qsys` or `.qip` file. Otherwise, you cannot use the IP upgrade or IP parameter editor feature.
- Plan your directory structure ahead of time. Do not change the relative path between a `.qsys` file and its generation output directory. If you must move the `.qsys` file, ensure that the generation output directory remains with the `.qsys` file.
- Do not add IP core files directly from the `/quartus/libraries/megafunctions` directory in your project. Otherwise, you must update the files for each subsequent software release. Instead, use the IP Catalog and then add the `.qip` to your project.
- Do not use IP files that the Quartus Prime software generates for RAM or FIFO blocks targeting older device families (even though the Quartus Prime software does not issue an error). The RAM blocks that Quartus Prime generates for older device families are not optimized for the latest device families.
- When generating a ROM function, save the resulting `.mif` or `.hex` file in the same folder as the corresponding IP core's `.qsys` or `.qip` file. For example, moving all of your project's `.mif` or `.hex` files to the same directory causes relative path problems after archiving the design.
- Always use the Quartus Prime `ip-setup-simulation` and `ip-make-simscript` utilities to generate simulation scripts for each IP core or Platform Designer system in your design. These utilities produce a single simulation script that does not require manual update for upgrades to Quartus Prime software or IP versions, as [Simulating Intel FPGA IP Cores](#) on page 75 describes.

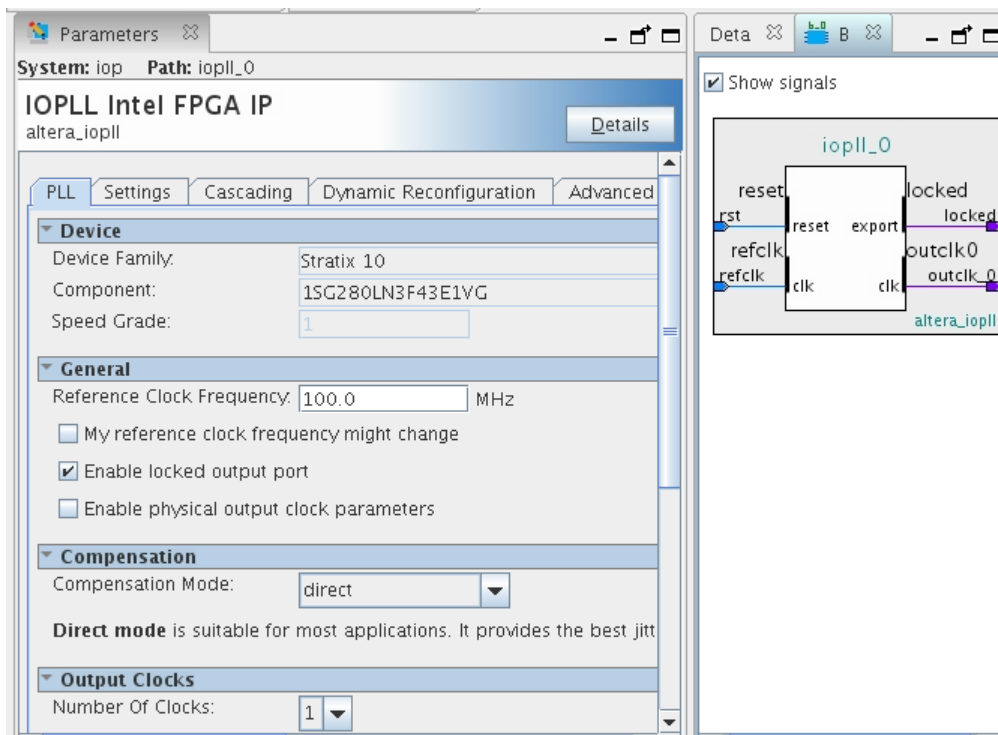
4.6. Specifying the IP Core Parameters and Options (Quartus Prime Pro Edition)

Quickly configure Intel FPGA IP cores in the Quartus Prime parameter editor. Double-click any component in the IP Catalog to launch the parameter editor. The parameter editor allows you to define a custom variation of the IP core. The parameter editor generates the IP variation synthesis and optional simulation files, and adds the `.ip` file representing the variation to your project automatically.

Follow these steps to locate, instantiate, and customize an IP core in the parameter editor:

1. Create or open an Quartus Prime project (.qpf) to contain the instantiated IP variation.
2. In the IP Catalog (**Tools > IP Catalog**), locate and double-click the name of the IP core to customize. To locate a specific component, type some or all of the component's name in the IP Catalog search box. The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. Do not include spaces in IP variation names or paths. The parameter editor saves the IP variation settings in a file named `<your_ip>.ip`. Click **OK**. The parameter editor appears.

Figure 25. IP Parameter Editor (Quartus Prime Pro Edition)



4. Set the parameter values in the parameter editor and view the block diagram for the component. The **Parameterization Messages** tab at the bottom displays any errors in IP parameters:
 - Optionally, select preset parameter values if provided for your IP core. Presets specify initial parameter values for specific applications.
 - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
 - Specify options for processing the IP core files in other EDA tools.

Note: Refer to your IP core user guide for information about specific IP core parameters.

5. Click **Generate HDL**. The **Generation** dialog box appears.

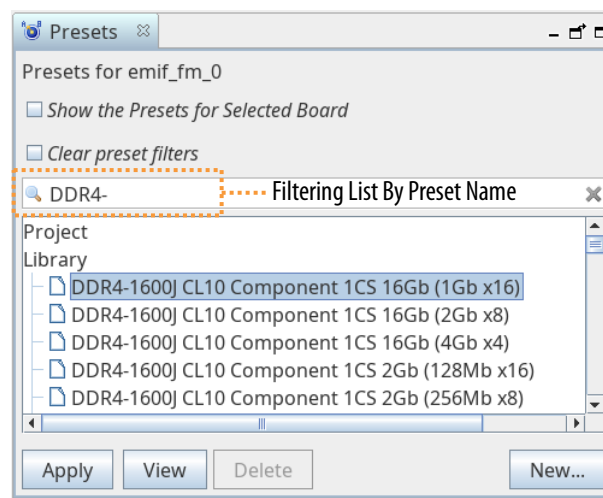
6. Specify output file generation options, and then click **Generate**. The synthesis and simulation files generate according to your specifications.
7. To generate a simulation testbench, click **Generate > Generate Testbench System**. Specify testbench generation options, and then click **Generate**.
8. To generate an HDL instantiation template that you can copy and paste into your text editor, click **Generate > Show Instantiation Template**.
9. Click **Finish**. Click **Yes** if prompted to add files representing the IP variation to your project.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Note: Some IP cores generate different HDL implementations according to the IP core parameters. The underlying RTL of these IP cores contains a unique hash code that prevents module name collisions between different variations of the IP core. This unique code remains consistent, given the same IP settings and software version during IP generation. This unique code can change if you edit the IP core's parameters or upgrade the IP core version. To avoid dependency on these unique codes in your simulation environment, refer to *Generating a Combined Simulator Setup Script*.

4.6.1. Applying Preset Parameters for Specific Applications

The **Preset** tab displays the names of available preset settings for an IP component. A preset is a specific collection of parameter settings that are appropriate for a specific protocol, application, or board. Double-click the preset name (or click **Apply**) to instantly apply the parameter values defined in the preset to the current IP instance.

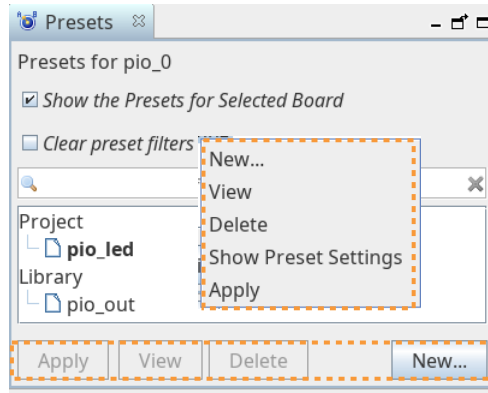
Figure 26. Selecting Preset Parameters



4.6.1.1. Viewing, Applying, and Deleting IP Presets

You can view the properties of a preset, apply a preset, or delete any existing preset in the **Presets** tab.

Figure 27. View, Apply, and Delete Presets in Presets Tab

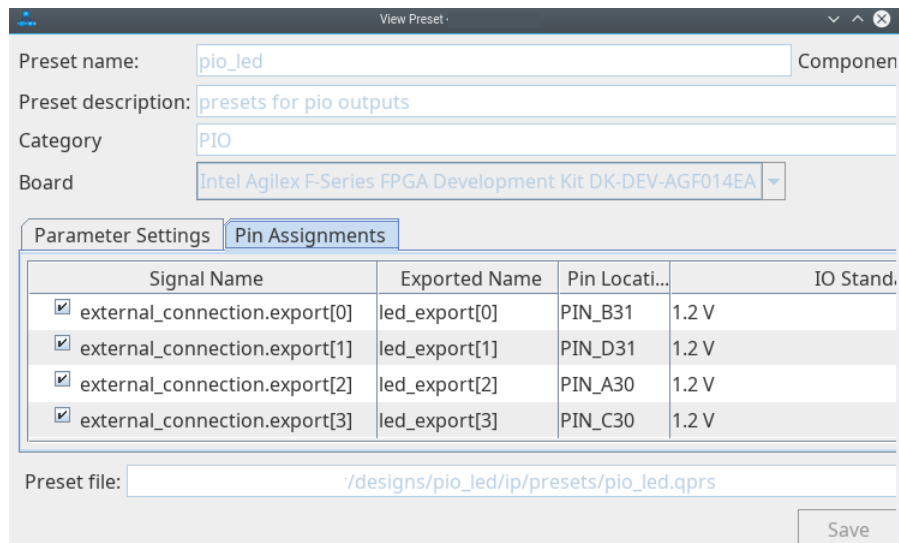


Note: Right-click a preset to access the same **View**, **Apply**, and **Delete** preset functions in the context menu.

Viewing Presets

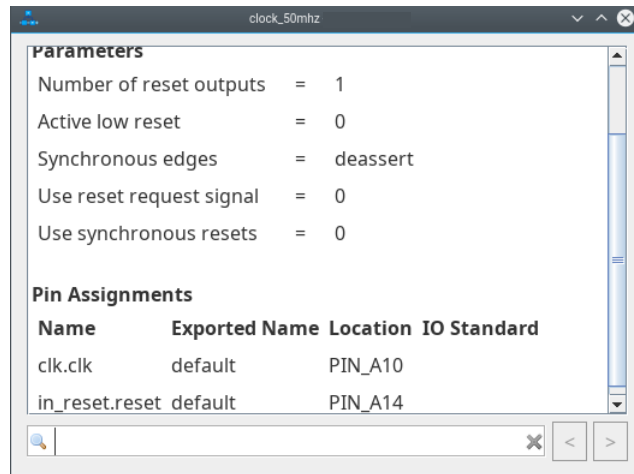
Click the **View** button to show the preset properties in the read-only **Update Preset** dialog box.

Figure 28. View Button Opens View Preset Dialog Box



Right-click a preset and click **Show Preset Settings** to view a searchable report of the preset settings.

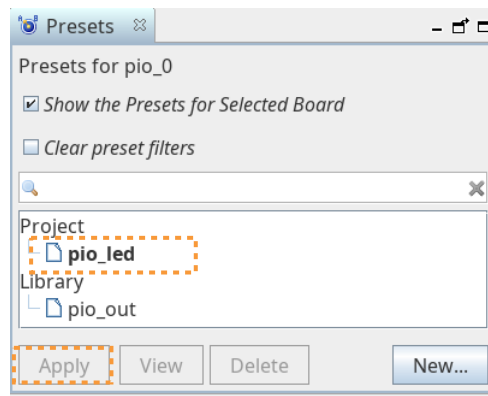
Figure 29. Show Preset Settings Searchable Report



Applying Presets to IP Instances

Click the **Apply** button (or double-click) to apply the IP preset to the currently selected IP. Applied presets appear in bold text.

Figure 30. Applied Presets Appear in Bold Text



Deleting Presets from the System

Click the **Delete** button to delete the current preset from the Platform Designer system.

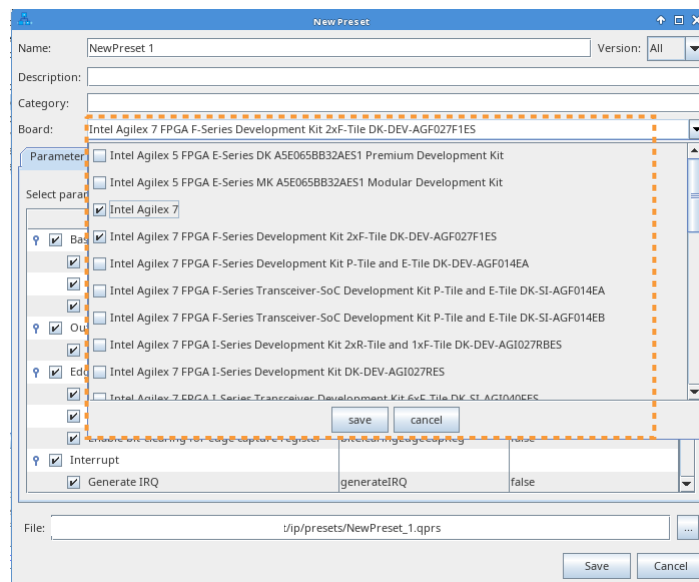
4.6.2. Customizing IP Presets

You can optionally define and save a custom set of parameter settings as an IP preset, and then apply the preset whenever you add an instance of the IP component to any system.

Follow these steps to save a custom IP preset:

1. In IP Catalog, double-click any component to launch the parameter editor.
2. To search for a specific preset to base initial settings, type a partial preset name in the search box.
3. In the **Presets** tab, click **New** to specify the **Preset name** and **Preset description**.
4. In the **Board** dropdown, specify the target board. The **Default** setting specifies the current board as the target board for this preset.
Note: You can specify multiple boards for a preset, provided that the preset parameters and assignments are applicable to all boards in the preset.
5. Under **Select parameters to include in the preset**, enable or disable the parameters you want to include in the preset.
6. Specify the path for the **Preset file** that preserves the collection of parameter settings. The location of the new .qprs preset file is added to the IP search path automatically.

Figure 31. Create New Preset



7. Click **Save**.
8. To apply the preset to an IP component, click **Apply**. Preset parameter values that match the current parameter settings appear in bold.

4.6.2.1. Defining Preset Pin Assignments

You can define pin assignments that are included as part of an IP preset. When you apply the IP preset to an IP instance, the pin assignments export during the IP or system's HDL generation.

You define preset pin assignments in the **Pin Assignments** tab of the **New Preset** dialog box, or in a Pin Assignments File (.tcl) that you create.

4.6.2.1.1. Defining Preset Pin Assignments in Pin Assignments Tab

The **Pin Assignments** tab allows you to specify the **Exported Name** of the signals, to select the appropriate **Pin Location**, and to select the appropriate **IO Standard** for the target board.

By default, the **Exported Name** name takes the form of:

```
module_name + interface_name + pin_role
```

For example:

```
pio0_external_connection_export[0]
```

You can change the **Exported Name** by double-clicking on the **Exported Name** for the interface and typing a new name. All of the signals of the interface then update automatically to reflect the name you specify.

Figure 32. Pin Assignments Tab

Signal Name	Exported Name	Pin Location	IO Standard
<input type="checkbox"/> clk			
<input type="checkbox"/> reset			
<input type="checkbox"/> s1			
<input checked="" type="checkbox"/> external_connection	led		
<input checked="" type="checkbox"/> export[4]			
<input checked="" type="checkbox"/> external_connection.export[0]	led_export[0]	PIN_B31	1.2 V
<input checked="" type="checkbox"/> external_connection.export[1]	led_export[1]	PIN_D31	1.2 V
<input checked="" type="checkbox"/> external_connection.export[2]	led_export[2]	PIN_A30	1.2 V
<input checked="" type="checkbox"/> external_connection.export[3]	led_export[3]	PIN_C30	1.2 V

Preset file: /designs/pio_led/ip/presets/pio_led.qprs

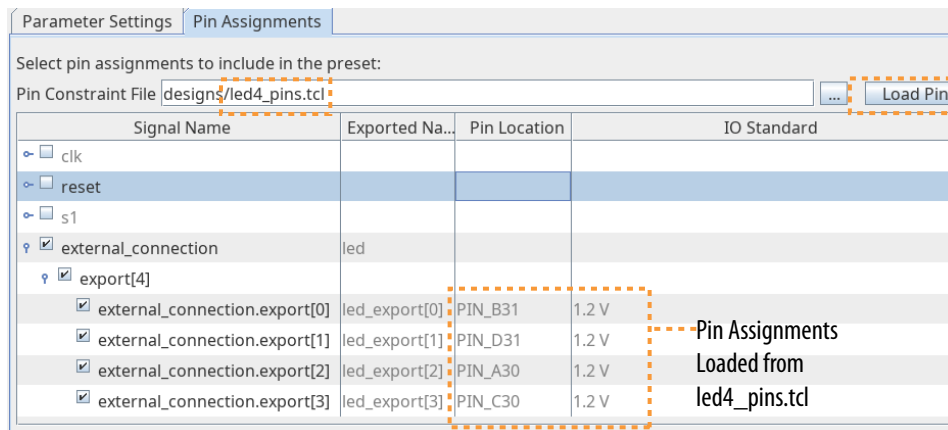
Save

For example, typing **led** for the **external_connection** interface updates the signals of the interface to **led_export[n]**. The **external_connection** is the interface name, and **external_connection_export(0)** is the signal name.

4.6.2.1.2. Defining Preset Pin Assignments in a Pin File

Alternatively, you can specify the pin assignments in a Pin Constraints File (.tcl), which can be more efficient for projects with many ports. You specify this .tcl file as the **Pin Constraint File** on the **Pin Assignments** tab, and then click **Load Pin**. The **Pin Location** and **IO Standard** update per the loaded pin assignments.

Figure 33. Loading Pin Assignments from Tcl File



The following shows the contents of an example Pin Constraints File (.tcl):

```
set_instance_assignment -to "led_export[0]" -name IO_STANDARD "1.2 V"
set_location_assignment -to "led_export[0]" "PIN_B31"
set_instance_assignment -to "led_export[1]" -name IO_STANDARD "1.2 V"
set_location_assignment -to "led_export[1]" "PIN_D31"
set_instance_assignment -to "led_export[2]" -name IO_STANDARD "1.2 V"
set_location_assignment -to "led_export[2]" "PIN_A30"
set_instance_assignment -to "led_export[3]" -name IO_STANDARD "1.2 V"
set_location_assignment -to "led_export[3]" "PIN_C30"
```

4.7. IP Core Generation Output (Quartus Prime Pro Edition)

The Quartus Prime software generates the following output file structure for individual IP cores that are not part of a Platform Designer system.

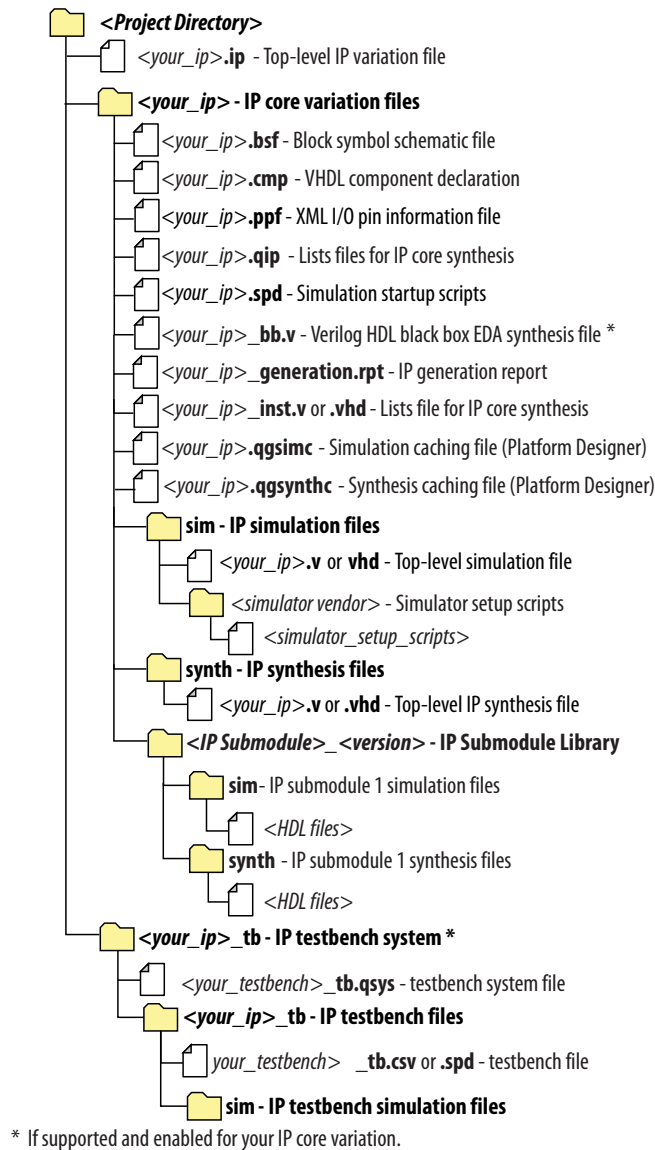
Table 25. Output Files of Intel FPGA IP Generation

File Name	Description
<your_ip>.ip	Top-level IP variation file that contains the parameterization of an IP core in your project. If the IP variation is part of a Platform Designer system, the parameter editor also generates a .qsys file.
<your_ip>.cmp	The VHDL Component Declaration (.cmp) file is a text file that contains local generic and port definitions that you use in VHDL design files.
<your_ip>_generation.rpt	IP or Platform Designer generation log file. Displays a summary of the messages during IP generation.
<your_ip>.qgsimc (Platform Designer systems only)	Simulation caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<your_ip>.qgsynth (Platform Designer systems only)	Synthesis caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<your_ip>.csv	Contains information about the upgrade status of the IP component.
<your_ip>.bsf	A symbol representation of the IP variation for use in Block Diagram Files (.bdf).

continued...

File Name	Description
<your_ip>.spd	Input file that ip-make-simscript requires to generate simulation scripts. The .spd file contains a list of files you generate for simulation, along with information about memories that you initialize.
<your_ip>.ppf	The Pin Planner File (.ppf) stores the port and node assignments for IP components you create for use with the Pin Planner.
<your_ip>_bb.v	Use the Verilog blackbox (_bb.v) file as an empty module declaration for use as a blackbox.
<your_ip>_inst.v or _inst.vhd	HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.
<your_ip>.regmap	If the IP contains register information, the Quartus Prime software generates the .regmap file. The .regmap file describes the register map information of host and agent interfaces. This file complements the .sopcinfo file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.
<your_ip>.svd	Allows HPS System Debug tools to view the register maps of peripherals that connect to HPS within a Platform Designer system. During synthesis, the Quartus Prime software stores the .svd files for agent interface visible to the System Console hosts in the .sof file in the debug session. System Console reads this section, which Platform Designer queries for register map information. For system agents, Platform Designer accesses the registers by name.
<your_ip>.v <your_ip>.vhd	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a msim_setup.tcl script to set up and run a simulation with a supported Siemens EDA simulator, such as the QuestaSim simulator.
aldec/	Contains a Riviera-PRO* script rivierapro_setup.tcl to setup and run a simulation.
/synopsys/vcs /synopsys/vcsmx	Contains a shell script vcs_setup.sh to set up and run a VCS* simulation. Contains a shell script vcsmx_setup.sh and synopsys_sim.setup file to set up and run a VCS MX simulation.
/xcelium	Contains an Xcelium* Parallel simulator shell script xcelium_setup.sh and other setup files to set up and run a simulation.
/submodules	Contains HDL files for the IP core submodule.
<IP submodule>/	Platform Designer generates /synth and /sim sub-directories for each IP submodule directory that Platform Designer generates.

Figure 34. Individual IP Core Generation Output (Quartus Prime Pro Edition)



4.8. Scripting IP Core Generation

Use the `qsys-script` and `qsys-generate` utilities to define and generate an IP core variation outside of the Quartus Prime GUI.

To parameterize and generate an IP core at command-line, follow these steps:

1. Run `qsys-script` to start a Tcl script that instantiates the IP and sets parameters:

```
qsys-script --script=<script_file>.tcl
```

2. Run `qsys-generate` to generate the IP core variation:

```
qsys-generate <IP variation file>.qsys
```

4.9. Modifying an IP Variation

After generating an IP core variation, use any of the following methods to modify the IP variation in the parameter editor.

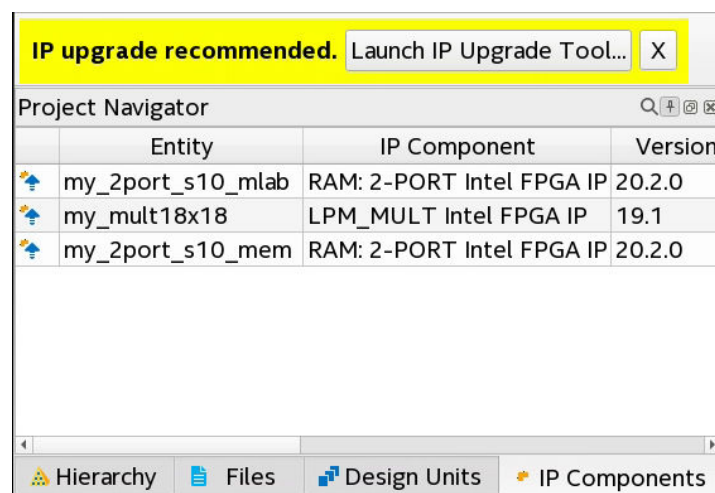
Table 26. Modifying an IP Variation

Menu Command	Action
File > Open	Select the top-level HDL (.v, or .vhd) IP variation file to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.
View > Project Navigator > IP Components	Double-click the IP variation to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.
Project > Upgrade IP Components	Select the IP variation and click Upgrade in Editor to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.

4.10. Upgrading IP Cores

Any Intel FPGA IP variations that you generate from a previous version or different edition of the Quartus Prime software, may require upgrade before compilation in the current software edition or version. The Project Navigator displays a banner indicating the IP upgrade status. Click **Launch IP Upgrade Tool** or **Project > Upgrade IP Components** to upgrade outdated IP cores.







Figure 35. IP Upgrade Alert in Project Navigator



Icons in the **Upgrade IP Components** dialog box indicate when IP upgrade is required, optional, or unsupported for an IP variation in the project. Upgrade IP variations that require upgrade before compilation in the current version of the Quartus Prime software.

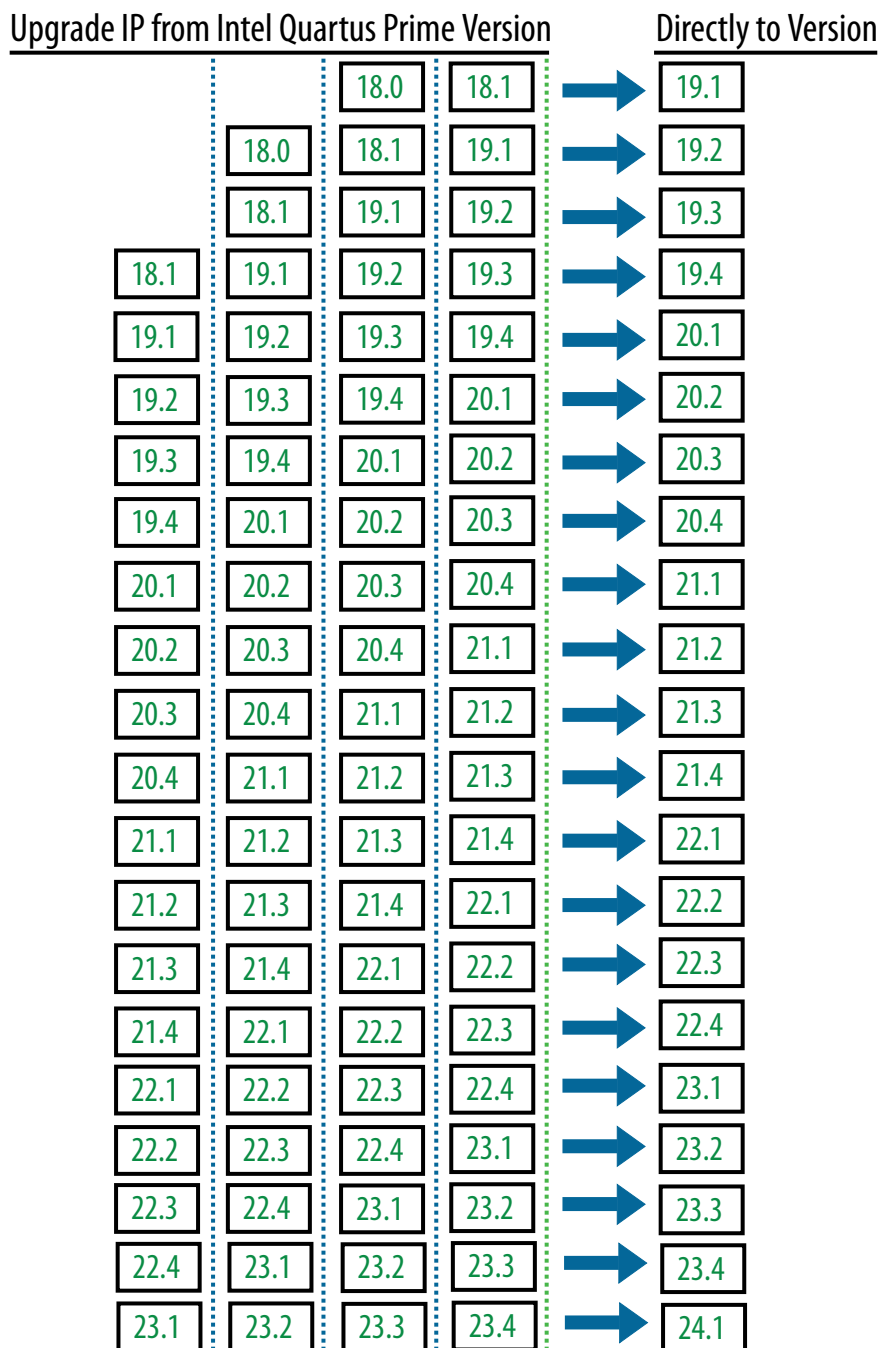
Note: Upgrading IP cores may append a unique identifier to the original IP core entity names, without similarly modifying the IP instance name. There is no requirement to update these entity references in any supporting Quartus Prime file, such as the Quartus Prime Settings File (.qsf), Synopsys* Design Constraints File (.sdc), or Signal Tap File (.stp), if these files contain instance names. The Quartus Prime software reads only the instance name and ignores the entity name in paths that specify both names. Use only instance names in assignments.

Table 27. IP Core Upgrade Status

IP Core Status	Description
IP Upgraded 	Indicates that your IP variation uses the latest version of the Intel FPGA IP core.
IP Component Outdated 	Indicates that your IP variation uses an outdated version of the IP core.
IP End of Life 	Indicates that Intel designates the IP core as end-of-life status. You may or may not be able to edit the IP core in the parameter editor. Support for this IP core discontinues in future releases of the Quartus Prime software.
IP Upgrade Mismatch Warning 	Provides warning of non-critical IP core differences in migrating IP to another device family.
IP has incompatible subcores 	Indicates that the current version of the Quartus Prime software does not support compilation of your IP variation, because the IP has incompatible subcores.
Compilation of IP Not Supported 	Indicates that the current version of the Quartus Prime software does not support compilation of your IP variation. This can occur if another edition of the Quartus Prime software, such as the Quartus Prime Standard Edition, generated this IP. Replace this IP component with a compatible component in the current edition.

Note: Beginning with the Quartus Prime Pro Edition software version 19.1, IP upgrade supports migration of IP released within one year of the Quartus Prime Pro Edition software version, as the following chart defines:

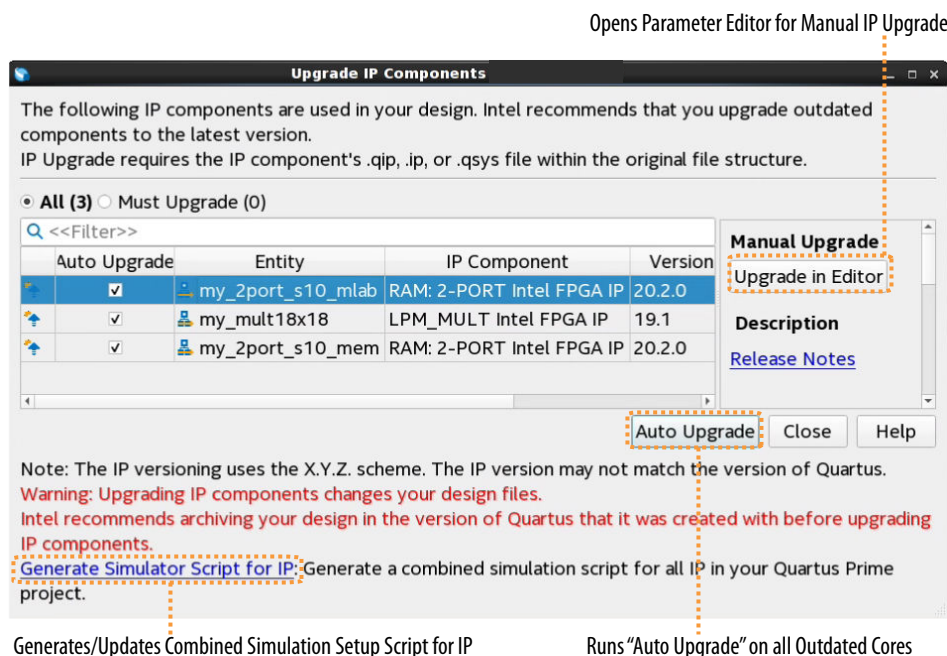
Figure 36. Quartus Prime Pro Edition IP Version Upgrade Paths



Follow these steps to upgrade IP cores:

1. In the latest version of the Quartus Prime software, open the Quartus Prime project containing an outdated IP core variation. The **Upgrade IP Components** dialog box automatically displays the status of IP cores in your project, along with instructions for upgrading each core. To access this dialog box manually, click **Project > Upgrade IP Components**.
2. To upgrade one or more IP cores that support automatic upgrade, ensure that you turn on the **Auto Upgrade** option for the IP cores, and click **Auto Upgrade**. The **Status** and **Version** columns update when upgrade is complete. Example designs that any Intel FPGA IP core provides regenerate automatically whenever you upgrade an IP core.
3. To manually upgrade an individual IP core, select the IP core and click **Upgrade in Editor** (or simply double-click the IP core name). The parameter editor opens, allowing you to adjust parameters and regenerate the latest version of the IP core.

Figure 37. Upgrading IP Cores (Quartus Prime Pro Edition Example)



Note: Intel FPGA IP cores older than Quartus Prime software version 12.0 do not support upgrade. Intel verifies that the current version of the Quartus Prime software compiles the previous two versions of each IP core. The *Intel FPGA IP Core Release Notes* reports any verification exceptions for Intel FPGA IP cores. Intel does not verify compilation for IP cores older than the previous two releases.

Related Information

[Intel FPGA IP Release Notes](#)

4.10.1. Upgrading IP Cores at Command-Line

Optionally, upgrade an Intel FPGA IP core at the command-line, rather than using the GUI. IP cores that do not support automatic upgrade do not support command-line upgrade.

- To upgrade a single IP core at the command-line, type the following command:

```
quartus_sh -ip_upgrade -variation_files <my_ip>.<qsys,.v, .vhd> \
    <quartus_project>
```

Example:

```
quartus_sh -ip_upgrade -variation_files mega/pll25.qsys hps_testx
```

- To simultaneously upgrade multiple IP cores at the command-line, type the following command:

```
quartus_sh -ip_upgrade -variation_files "<my_ip1>.<qsys,.v, .vhd>> \
    ; <my_ip_filepath/my_ip2>.<hdl>" <quartus_project>
```

Example:

```
quartus_sh -ip_upgrade -variation_files "mega/pll_tx2.qsys;mega/
pll13.qsys" hps_testx
```

4.10.2. Migrating IP Cores to a Different Device

Migrate an Intel FPGA IP variation when you want to target a different (often newer) device. Most Intel FPGA IP cores support automatic migration. Some IP cores require manual IP regeneration for migration. A few IP cores do not support device migration, requiring you to replace them in the project. The **Upgrade IP Components** dialog box identifies the migration support level for each IP core in the design.

- To display the IP cores that require migration, click **Project > Upgrade IP Components**. The **Description** field provides migration instructions and version differences.
- To migrate one or more IP cores that support automatic upgrade, ensure that the **Auto Upgrade** option is turned on for the IP cores, and click **Perform Automatic Upgrade**. The **Status** and **Version** columns update when upgrade is complete.
- To migrate an IP core that does not support automatic upgrade, double-click the IP core name, and click **OK**. The parameter editor appears. If the parameter editor specifies a **Currently selected device family**, turn off **Match project/default**, and then select the new target device family.
- Click **Generate HDL**, and confirm the **Synthesis** and **Simulation** file options. Verilog HDL is the default output file format. If you specify VHDL as the output format, select **VHDL** to retain the original output format.
- Click **Finish** to complete migration of the IP core. Click **OK** if the software prompts you to overwrite IP core files. The **Device Family** column displays the new target device name when migration is complete.
- To ensure correctness, review the latest parameters in the parameter editor or generated HDL.

Note: IP migration may change ports, parameters, or functionality of the IP variation. These changes may require you to modify your design or to re-parameterize your IP variant. During migration, the IP variation's HDL generates into a library that is different from the original output location of the IP core. Update any assignments that reference outdated locations. If a symbol in a supporting Block Design File schematic represents your upgraded IP core, replace the symbol with the newly generated `<my_ip>.bsf`. Migration of some IP cores requires installed support for the original and migration device families.

Related Information

[Intel FPGA IP Release Notes](#)

4.10.3. Troubleshooting IP or Platform Designer System Upgrade

The **Upgrade IP Components** dialog box reports the version and status of each Intel FPGA IP core and Platform Designer system following upgrade or migration.

If any upgrade or migration fails, the **Upgrade IP Components** dialog box provides information to help you resolve any errors.

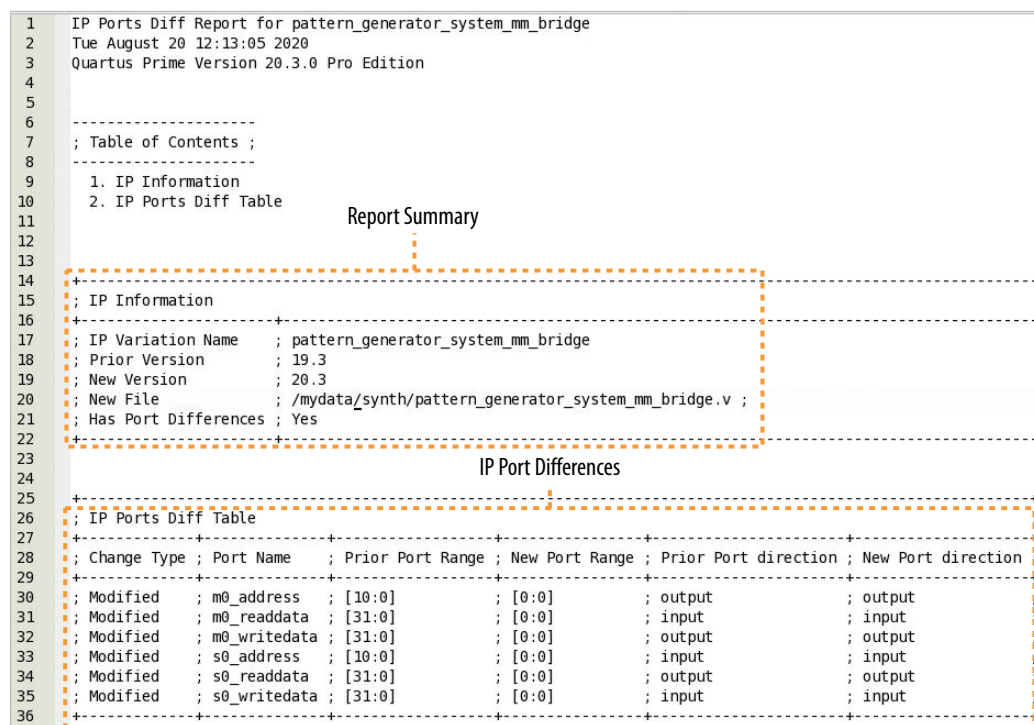
Note: Do not use spaces in IP variation names or paths.

During automatic or manual upgrade, the Messages window dynamically displays upgrade information for each IP core or Platform Designer system. Use the following information to resolve upgrade errors:

Table 28. IP Upgrade Error Information

Upgrade IP Components Field	Description
Status	Displays the "Success" or "Failed" status of each upgrade or migration. Click the status of any upgrade that fails to open the IP Upgrade Report .
Version	Dynamically updates the version number when upgrade is successful. The text is red when the IP requires upgrade.
Device Family	Dynamically updates to the new device family when migration is successful. The text is red when the IP core requires upgrade.
Auto Upgrade	Runs automatic upgrade on all IP cores that support auto upgrade. Also, automatically generates a <code><Project Directory>/ip_upgrade_port_diff_reports</code> report for IP cores or Platform Designer systems that fail upgrade. Review these reports to determine any port differences between the current and previous IP core version.

Use the following techniques to resolve errors if your IP core or Platform Designer system "Failed" to upgrade versions or migrate to another device. Review and implement the instructions in the **Description** field, including one or more of the following:



The Quartus Prime software supports IP core RTL simulation in specific EDA simulators. IP generation optionally creates simulation files, including the functional simulation model, any testbench (or example design), and vendor-specific simulator

setup scripts for each IP core. You can use the functional simulation model and any testbench or example design for simulation. IP generation output may also include scripts to compile and run any testbench. The scripts list all models or libraries you require to simulate your IP core.

The Quartus Prime software provides integration with many simulators and supports multiple simulation flows, including your own scripted and custom simulation flows. Whichever flow you choose, IP core simulation involves the following steps:

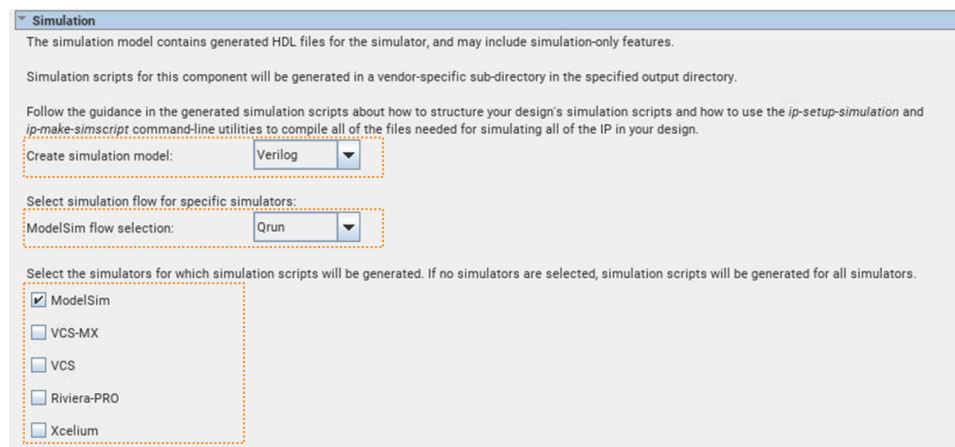
1. Generate IP HDL, testbench (or example design), and simulator setup script files.
2. Set up your simulator environment and any simulation scripts.
3. Compile simulation model libraries.
4. Run your simulator.

4.11.1. Generating IP Simulation Files

The Quartus Prime software optionally generates the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts when you generate an IP core. To specify options for the generation of IP simulation files, follow these steps:

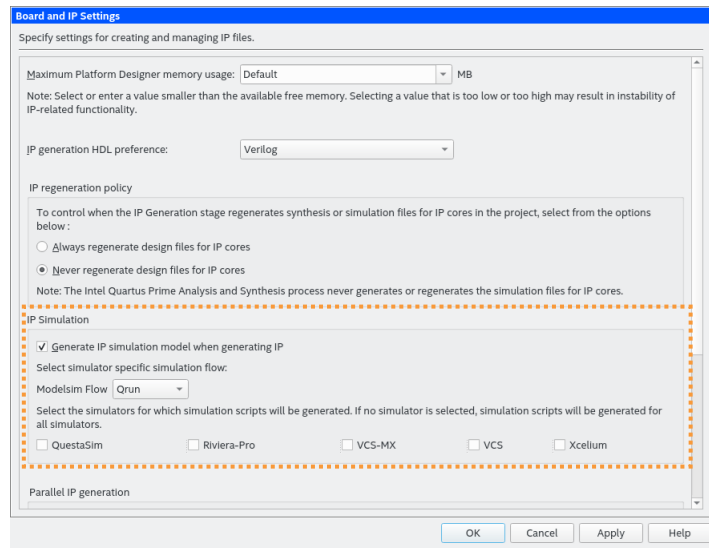
- To specify your supported simulator and options for design simulation file generation, click **Assignment > Settings > EDA Tool Settings > Simulation**.

Figure 39. Simulation Options in Generation Dialog Box



- To specify your supported simulator and options for IP simulation file generation, click **Assignments > Settings > Board and IP Settings > IP Simulation** and specify the following:
 - To enable automatic generation of simulation models for all IP in the project when you generate IP during compilation, turn on the **Generate IP simulation model when generating IP** option.
 - To specify one or more supported simulators for which to generate setup scripts, turn on one or more simulator option, or disable all simulator options to generate scripts for all simulators automatically.

Figure 40. Project-Wide IP Generation Settings



- To generate the simulation files, click **Processing ► Start Compilation** to compile the design. The simulation models and setup scripts for the Intel FPGA IP generate in the `<your_project>/<ip_name>/sim/<vendor>` directory.

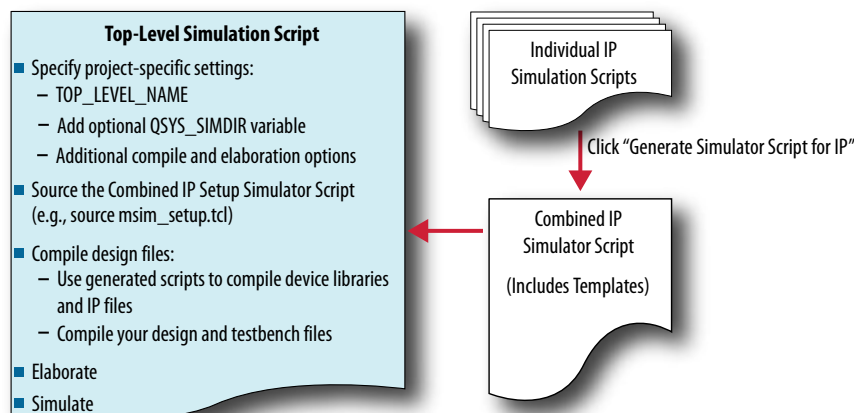
You can optionally override these project-level **IP Settings** when you generate HDL for individual IP cores with the IP Parameter Editor. Prior to generation, you can specify a supported simulator, or specify no simulator to generate the setup scripts for all simulators in the parameter editor.

4.11.2. Scripting IP Simulation

The Quartus Prime software supports the use of scripts to automate simulation processing in your preferred simulation environment. Use the scripting methodology that you prefer to control simulation.

Use a version-independent, top-level simulation script to control design, testbench, and IP core simulation. Because Quartus Prime-generated simulation file names may change after IP upgrade or regeneration, your top-level simulation script must "source" the generated setup scripts, rather than using the generated setup scripts directly. Follow these steps to generate or regenerate combined simulator setup scripts:

Figure 41. Incorporating Generated Simulator Setup Scripts into a Top-Level Simulation Script



1. Click **Tools > Generate Simulator Script for IP** (or run the `ip-setup-simulation` utility) to generate or regenerate a combined simulator setup script for all IP for each simulator.
2. Use the templates in the generated script to source the combined script in your top-level simulation script. Each simulator's combined script file contains a rudimentary template that you adapt for integration of the setup script into a top-level simulation script.

This technique eliminates manual update of simulation scripts if you modify or upgrade the IP variation.

4.11.2.1. Generating a Combined Simulator Setup Script

You can run the **Generate Simulator Setup Script for IP** command to generate a combined simulator setup script.

You can then source this combined script from a top-level simulation script. Click **Tools > Generate Simulator Setup Script for IP** (or use of the `ip-setup-simulation` utility at the command-line) to generate or update the combined scripts, after any of the following occur:

- IP core initial generation or regeneration with new parameters
- Quartus Prime software version upgrade
- IP core version upgrade

Table 29. ip-setup-simulation Utility

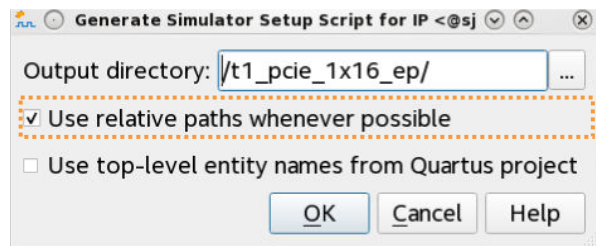
Utility	Syntax
ip-setup-simulation generates a combined, version-independent simulation script for all Intel FPGA IP cores in your project. The command also automates regeneration of the script after upgrading software or IP versions. Use the <code>compile-to-work</code> option to compile all simulation files into a single work library if your simulation environment requires. Use the <code>--use-relative-paths</code> option to use relative paths whenever possible.	<pre>ip-setup-simulation --quartus-project=<my_proj> --output-directory=<my_dir> --use-relative-paths --compile-to-work</pre> <p><code>--use-relative-paths</code> and <code>--compile-to-work</code> are optional. For command-line help listing all options for these executables, type: <code><utility name> --help</code>.</p>

To generate a combined simulator setup script for all project IP cores for each simulator:⁽⁴⁾

1. Click **Tools > Generate Simulator Setup Script for IP** (or run the `ip-setup-simulation` utility). Specify the **Output Directory** and library compilation options. Click **OK** to generate the file. By default, the files generate into the `/<project directory>/<simulator>/` directory using relative paths.

Note: For designs with F-tile IP, do not turn on the **Use top-level entity names from Quartus project** option.

Figure 42. Generate Simulator Setup Script for IP Dialog Box



2. To incorporate the generated simulator setup script into your top-level simulation script, refer to the template section in the generated simulator setup script as a guide to creating a top-level script:
 - a. Copy the specified template sections from the simulator-specific generated scripts and paste them into a new top-level file.
 - b. Remove the comments at the beginning of each line from the copied template sections.
 - c. Specify the customizations you require to match your design simulation requirements, for example:
 - Specify the `TOP_LEVEL_NAME` variable to the design's simulation top-level file. The top-level entity of your simulation is often a testbench that instantiates your design. Then, your design instantiates IP cores or Platform Designer systems. Set the value of `TOP_LEVEL_NAME` to the top-level entity.
 - If necessary, set the `QSYS_SIMDIR` variable to point to the location of the generated IP simulation files.
 - Specify any other changes, such as using the `grep` command-line utility to search a transcript file for error signatures, or e-mail a report.
3. Re-run **Tools > Generate Simulator Setup Script for IP** (or `ip-setup-simulation`) after regeneration of an IP variation.

Related Information

[Quartus Prime Pro Edition User Guide: Third-party Simulation](#)

⁽⁴⁾ If your design contains one or more F-tile IPs, you must first perform **Start Analysis & Elaboration** and then **Support-Logic Generation** before performing these steps.

4.12. Generating Simulation Files for Platform Designer Systems and IP Variants

If your design contains Intel FPGA IP or a Platform Designer system, you must first generate files for RTL simulation of the IP or system with the Quartus Prime Platform Designer before running simulation.

When you generate the system (or IP variant), Platform Designer optionally creates simulation files, including the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts for each IP core.

You can use the functional simulation model and any testbench or example design for simulation of the IP or system. The IP generation output may also include scripts to compile and run any testbench. The scripts list all models or libraries you require to simulate your IP core.

To generate the simulation model and simulator setup scripts for your Platform Designer system or component, follow these steps:

1. Click **Tools > Platform Designer**. Platform Designer and open or create a Platform Designer system or IP variant.
2. In Platform Designer, after specifying parameters, click **Generate > Generate HDL**. The **Generation** dialog box appears.
3. Under **Simulation**, specify **Verilog** or **VHDL** for the **Create simulation model** option.

Figure 43. Simulation Options in Generation Dialog Box

Simulation

The simulation model contains generated HDL files for the simulator, and may include simulation-only features.

Simulation scripts for this component will be generated in a vendor-specific sub-directory in the specified output directory.

Follow the guidance in the generated simulation scripts about how to structure your design's simulation scripts and how to use the *ip-setup-simulation* and *ip-make-simscript* command-line utilities to compile all of the files needed for simulating all of the IP in your design.

Create simulation model: Verilog

Select simulation flow for specific simulators:

ModelSim flow selection: Qrun

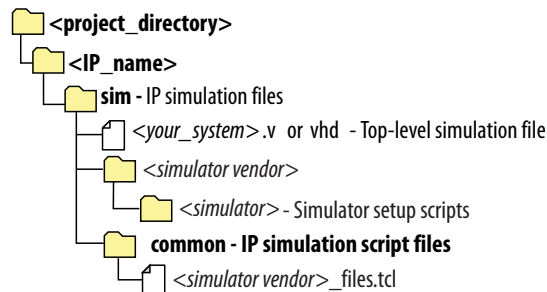
Select the simulators for which simulation scripts will be generated. If no simulators are selected, simulation scripts will be generated for all simulators.

- ☒ ModelSim
- ☐ VCS-MX
- ☐ VCS
- ☐ Riviera-PRO
- ☐ Xcelium

4. If you want to specifically use ModelSim*, specify **Traditional** or **Qrun** for the ModelSim flow option. Otherwise, **Qrun** flow is the default selection.
5. Turn on or off the **ModelSim**, **VCS-MX**, **VCS**, **Riviera-Pro**, or **Xcelium** option to generate simulator setup scripts for the simulation tool. If you turn on no simulator options, the scripts generate for all simulators.
6. Click the **Generate** button. Platform Designer generates the simulation models and setup scripts for your system or IP component in the following directory:

```
<top-level system name>/<system name>/<sim>/<simulator>
```


Figure 44. Generated Simulation Files Location



By default, Platform Designer generates the simulation scripts for the currently loaded system and all subsystems. Alternatively, you can open a subsystem to generate a simulation script only for that subsystem.

You can use scripts to compile the required device libraries and system design files in the correct order and elaborate or load the top-level system for simulation.

Table 30. Simulation Script Variables

The simulation scripts provide variables that allow flexibility in your simulation environment.

Variable	Description
TOP_LEVEL_NAME	If the testbench Platform Designer system is not the top-level instance in your simulation environment because you instantiate the Platform Designer testbench within your own top-level simulation file, set the TOP_LEVEL_NAME variable to the top-level hierarchy name.
QSYS_SIMDIR	If the simulation files generated by Platform Designer are not in the simulation working directory, use the QSYS_SIMDIR variable to specify the directory location of the Platform Designer simulation files.
QUARTUS_INSTALL_DIR	Points to the Quartus installation directory that contains the device family library.

Example 6. Top-Level Simulation HDL File for a Testbench System

The example below shows the `pattern_generator_tb` generated for a Platform Designer system called `pattern_generator`. The `top.sv` file defines the top-level module that instantiates the `pattern_generator_tb` simulation model, as well as a custom SystemVerilog test program with BFM transactions, called `test_program`.

```

module top();
  pattern_generator_tb tb();
  test_program pgm();
endmodule

```

4.13. Synthesizing IP Cores in Other EDA Tools

Optionally, use another supported EDA tool to synthesize a design that includes Intel FPGA IP cores. When you generate the IP core synthesis files for use with third-party EDA synthesis tools, you can create an area and timing estimation netlist. To enable generation, turn on **Create timing and resource estimates for third-party EDA synthesis tools** when customizing your IP variation.

The area and timing estimation netlist describes the IP core connectivity and architecture, but does not include details about the true functionality. This information enables certain third-party synthesis tools to better report area and timing estimates. In addition, synthesis tools can use the timing information to achieve timing-driven optimizations and improve the quality of results.

The Quartus Prime software generates the `<variant name>_syn.v` netlist file in Verilog HDL format, regardless of the output file format you specify. If you use this netlist for synthesis, you must include the IP core wrapper file `<variant name>.v` or `<variant name>.vhd` in your Quartus Prime project.

4.14. Instantiating IP Cores in HDL

Instantiate an IP core directly in your HDL code by calling the IP core name and declaring the IP core's parameters. This approach is similar to instantiating any other module, component, or subdesign. When instantiating an IP core in VHDL, you must include the associated libraries.

4.14.1. Example Top-Level Verilog HDL Module

Verilog HDL ALTFP_MULT in Top-Level Module with One Input Connected to Multiplexer.

```
module MF_top (a, b, sel, datab, clock, result);
    input [31:0] a, b, datab;
    input clock, sel;
    output [31:0] result;
    wire [31:0] wire_dataaa;

    assign wire_dataaa = (sel)? a : b;
    altfp_mult inst1
    (.dataaa(wire_dataaa), .datab(datab), .clock(clock), .result(result));

    defparam
        inst1.pipeline = 11,
        inst1.width_exp = 8,
        inst1.width_man = 23,
        inst1.exception_handling = "no";
endmodule
```

4.14.2. Example Top-Level VHDL Module

VHDL ALTFP_MULT in Top-Level Module with One Input Connected to Multiplexer.

```
library ieee;
use ieee.std_logic_1164.all;
library altera_mf;
use altera_mf.altera_mf_components.all;

entity MF_top is
    port (clock, sel : in std_logic;
          a, b, datab : in std_logic_vector(31 downto 0);
          result : out std_logic_vector(31 downto 0));
end entity;

architecture arch_MF_top of MF_top is
    signal wire_dataaa : std_logic_vector(31 downto 0);
begin

    wire_dataaa <= a when (sel = '1') else b;

    inst1 : altfp_mult
```

```

generic map (
    pipeline => 11,
    width_exp => 8,
    width_man => 23,
    exception_handling => "no")
port map (
    dataaa => wire_dataaa,
    datab => datab,
    clock => clock,
    result => result);
end arch_MF_top;

```

4.15. Support for the IEEE 1735 Encryption Standard

The Quartus Prime Pro Edition software supports the IEEE 1735 v1 encryption standard for IP core file decryption. You can encrypt the Verilog HDL or VHDL IP files with the `encrypt_1735` utility, or with a third-party encryption tool that supports the IEEE 1735 standard. You can then use the encrypted files in the Quartus Prime Pro Edition software and simulation tools that support the IEEE 1735 encryption standard.

The encryption key is the same for Verilog HDL and VHDL. You can pass parameters to the instantiation of an encrypted module using the same method as a non-encrypted module.

Type `encrypt_1735 --help` at the Quartus Prime command line to view syntax and all supported options for the `encrypt_1735` utility.

```

encrypt_1735 [-h | --help[=<option|topic>] | -v]
encrypt_1735 <other options>

Options:
-----
-?
-f <argument file>
-h
--256_bit[=<value>]
--help[=<option|topic>]
--language=<verilog | systemverilog | vhdl>
--lower_priority
--of=<some_file>
--quartus
--simulation[=<aldec | cadence | mentor | synopsys (comma delimited)>]
--tcl_jou_file=<[tcl_jou_filename=]on|off>
--tcl_log_file=<[tcl_log_filename=]on|off>

```

Adding the following Verilog or VHDL pragma to your RTL, along with the public key, enables the Quartus Prime software to use the key to decrypt IP core files.

Verilog/SystemVerilog Encryption Pragma (Third-Party Tools):

```

`pragma protect key_keyowner="Intel Corporation"
`pragma protect data_method="aes128-cbc"
`pragma protect key_method="rsa"
`pragma protect key_keyname="Intel-FPGA-Quartus-RSA-1"
`pragma protect key_public_key
<encrypted session key>

`pragma protect begin
`pragma protect end

```

VHDL Encryption Pragma (Third-Party Tools):

```
\protect key_keyowner = "Intel Corporation"
\protect data_method="aes128-cbc"
\protect key_method = "rsa"
\protect key_keyname = "Intel-FPGA-Quartus-RSA-1"
\protect key_block
<Encrypted session key>
```

Only file encryption with a third-party tool requires the public encryption key. File encryption with the Quartus Prime Pro Edition software does not require the public encryption key.

Use one of the following methods to obtain the public encryption key:

- If you are using the Quartus Prime Pro Edition software version 19.3 or later, the public encryption key is in `<install_directory>\quartus\common\misc\public_key`.
- If you are using a version of the Quartus Prime Pro Edition software earlier than version 19.3, to obtain the encryption key, login or register for a My-Intel account, and then submit an Intel Premier Support case requesting the encryption key.
- If you are ineligible for Intel Premier Support, you can submit a question regarding the "IEEE 1735 Encryption Public Key" to the Intel Community Forum for assistance.

Note: The Quartus Prime Standard Edition software does not support IEEE 1735 encryption.

Related Information

- [My-Intel.com](https://www.intel.com/my-intel)
- [Intel Community Forum](https://www.intel.com/community)

4.16. Related Trainings and Resources

You can take up the following training to help you understand how you can work with Intel FPGA IP cores:

- [Creating Reusable Design Blocks: Introduction to IP Reuse with the Quartus Prime Software](#)
- [Creating Reusable Design Blocks: IP Integration with the Quartus Prime Software](#)
- [Creating Reusable Design Blocks: IP Design & Implementation with the Quartus Prime Software](#)

For other IP-related trainings, review the [Intel FPGA Training Catalog](#) and [YouTube*'s Intel FPGA channel](#).

Also, refer to the [Embedded Peripherals IP User Guide](#) for detailed description of the IP cores that the Quartus Prime design software provides.

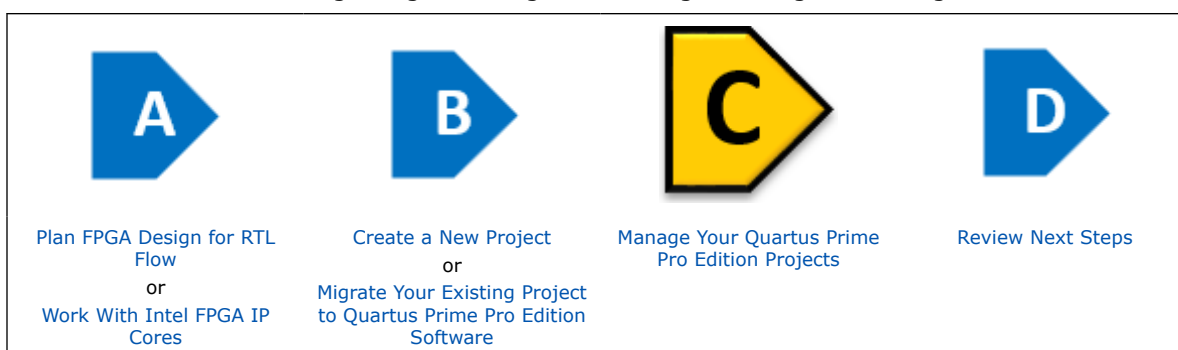
5. Managing Quartus Prime Projects

The Quartus Prime software organizes and manages the elements of your design within a *project*. The project encapsulates information about your design files, hierarchy, libraries, constraints, and project settings. This chapter describes the basics of working with Quartus Prime software projects, including viewing project information, adding design files and constraints, and viewing and exporting the design compilation results.

After you create or open a project, the GUI displays integrated information and controls for the open project.

Navigating Content Through Tasks

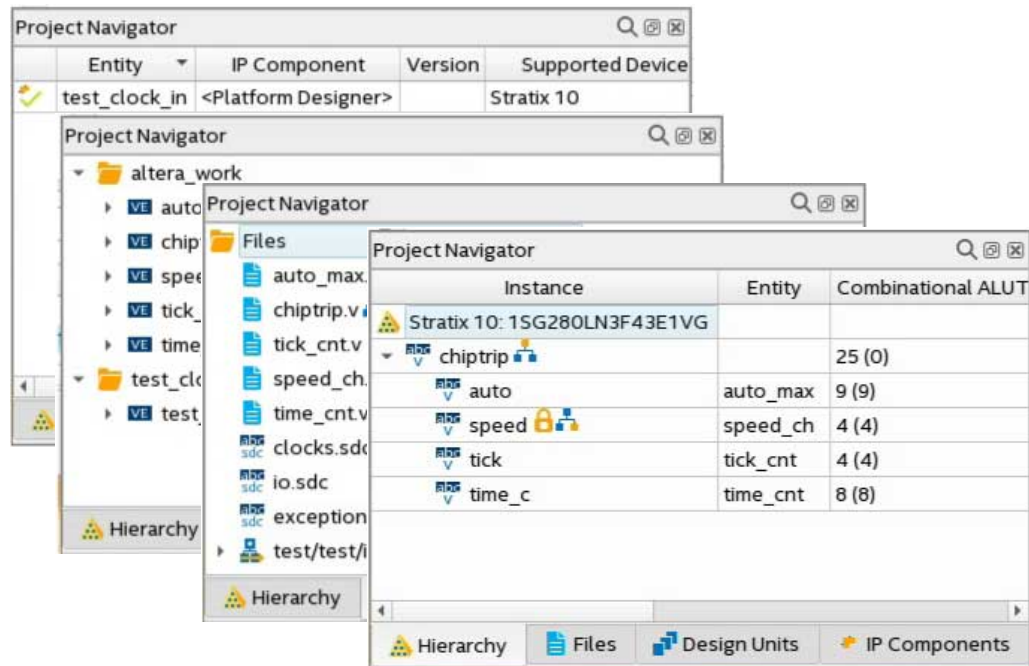
Use the following navigation diagram to navigate this guide through user-tasks:



5.1. Viewing Basic Project Information

View basic information about your project in the Project Navigator, the **Tasks** pane, Compilation Dashboard, Report panel, and **Messages** window.

Figure 45. Project Navigator Hierarchy, Files, Design Units, and IP Components Tabs



The Project Navigator

The **Project Navigator** (**View > Project Navigator**) displays the elements of your project, such as the design files, IP components, and your project hierarchy (after elaboration). Right-click in the **Project Navigator** to locate the elements of your project. Project information appears on the **Files**, **Hierarchy**, **Design Units**, and **IP Components** tabs.

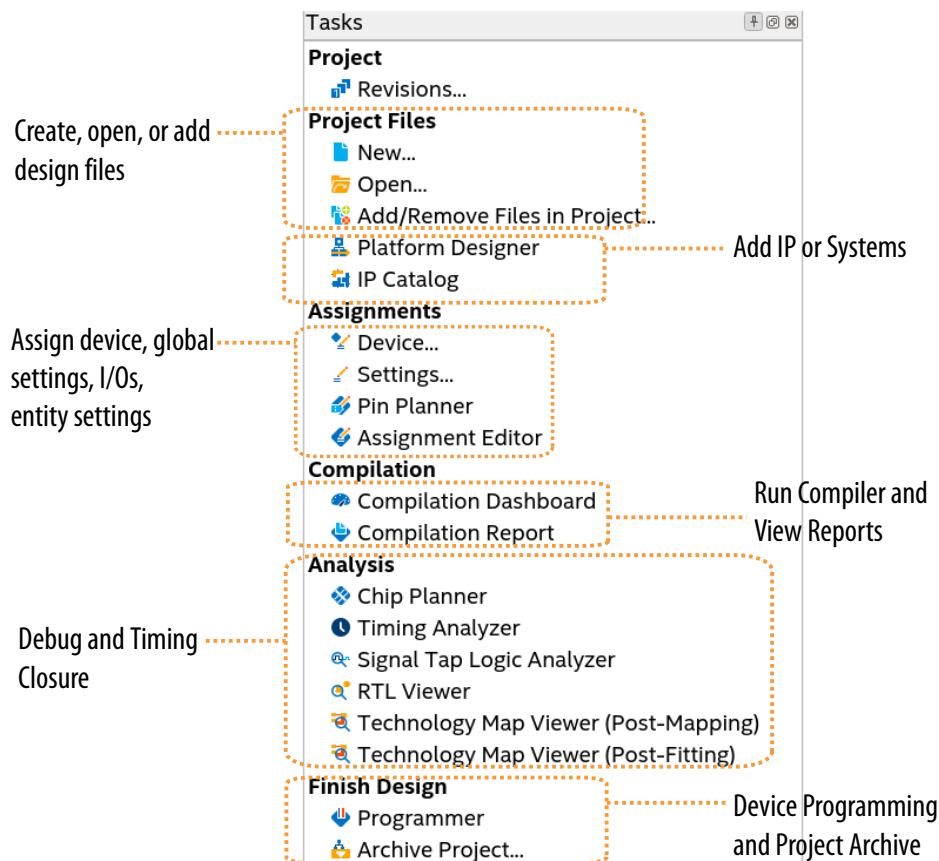
Table 31. Project Navigator Tabs

Project Navigator Tab	Description
Files	Lists all design files in the current project. Right-click design files in this tab to run these commands: <ul style="list-style-type: none"> • Open the file • Remove the file from project • View file Properties
Hierarchy	Provides a visual representation of the project hierarchy, specific resource usage information, and device and device family information. Right-click items in the hierarchy to Locate , Set as Top-Level Entity , or define Logic Lock regions or design partitions.
Design Units	Displays the design units in the project. Right-click a design unit to Locate in Design File .
IP Components	Displays the design files that make up the IP instantiated in the project, including Intel FPGA IP, Platform Designer components, and third-party IP. Click Launch IP Upgrade Tool from this tab to upgrade outdated IP components.

Project Tasks Pane

The **Tasks** pane (**View > Tasks**) launches common project tasks, such as creating design files, adding IP, running compilation, and device programming.

Figure 46. Tasks Pane

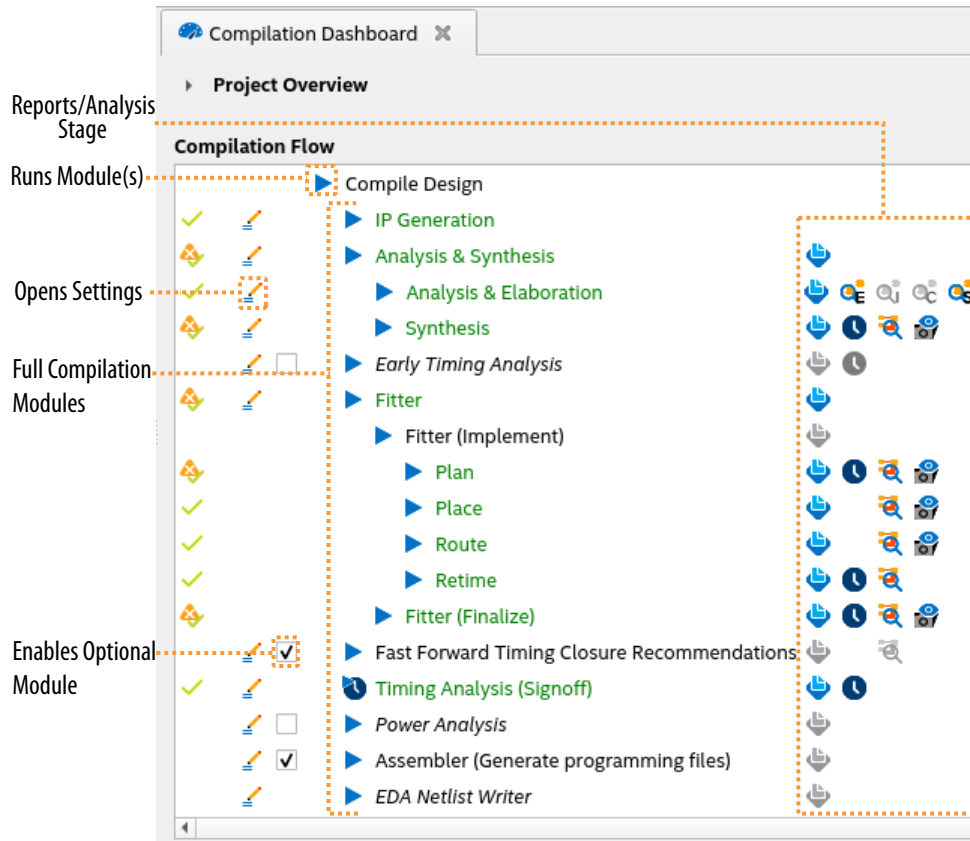


5.1.1. Using the Compilation Dashboard

The Compilation Dashboard provides immediate access to settings, controls, and reporting for each stage of the compilation flow.

The Compilation Dashboard appears by default when you open a project, or you can click **Compilation Dashboard** in the Tasks window to re-open it.

Figure 47. Compilation Dashboard



- Click the **Pencil** icon to edit settings for that stage of the compilation flow.
- Click any Compiler stage to run one or more Compiler stage.
You can click a Compiler stage to resume an interrupted compilation flow provided no compilation settings have changed from the initial start of the compilation flow.
- Click the **Report**, **RTL Viewer**, **Technology Map Viewer**, **Timing Analyzer**, or **Snapshot Viewer** icons for analysis of stage results.

As the Compiler progresses through the flow, the dashboard updates the status of each module, and enables icons that you can click for reports and analysis. The dashboard is also updated if you run your compilation flow from a command line with the `quartus_sh --flow` command.

5.1.2. Exploring Quartus Prime Project Contents

The Quartus Prime software organizes your design work within a project. You can create and compare multiple revisions of your project, to experiment with settings that achieve your design goals. When you create a new project in the GUI, the Quartus Prime software automatically creates an Quartus Prime Project File (`.qpf`) for that project. The `.qpf` references the Quartus Prime Settings File (`.qsf`). The `.qsf` lists the project's design, constraint, and IP files, and stores project-wide and entity-

specific settings that you specify in the GUI. You do not need to edit the text-based `.qpf` or `.qsf` files directly. The Quartus Prime software creates and updates these files automatically as you make changes in the GUI.

Table 32. Quartus Prime Project Files

File Type	Contains	To Edit	Format
Project file	Project and revision name	File > New Project Wizard	Quartus Prime Project File (<code>.qpf</code>)
Settings file	Lists design files, entity settings, target device, synthesis directives, placement constraints	Assignments > Settings	Quartus Prime Settings File (<code>.qsf</code>)
Quartus database	Project compilation results	Project > Export Design	Quartus Database File (<code>.qdb</code>)
Partition database	Partition compilation results	Project > Export Design Partition	Partition Database File (<code>.qdb</code>)
Timing constraints	Clock properties, exceptions, setup/hold	Tools > Timing Analyzer	Synopsys Design Constraints File (<code>.sdc</code>)
Logic design files	RTL and other design source files	File > New	All supported HDL files
Programming files	Device programming image and information	Tools > Programmer	SRAM Object File (<code>.sof</code>) Programmer Object File (<code>.pof</code>)
IP core files	IP core variation parameterization	Tools > IP Catalog	Quartus Prime IP File (<code>.ip</code>)
Platform Designer system files	System definition	Tools > Platform Designer	Platform Designer System File (<code>.qsys</code>)
EDA tool files	Scripts for third-party EDA tools	Assignments > Settings > EDA Tool Settings	Verilog Output File (<code>.vo</code>) VHDL Output File (<code>.vho</code>) Verilog Quartus Mapping File (<code>.vqm</code>)
Archive files	Complete project as single compressed file	Project > Archive Project	Quartus Prime Archive File (<code>.qar</code>)

5.1.2.1. Project File Best Practices

The Quartus Prime software provides various options for specifying project settings and constraints. The following best practices help ensure automated management and portability of your project files.

- Avoid manually editing Quartus Prime data files, such as the Quartus Prime Project File (`.qpf`), Quartus Prime Settings File (`.qsf`), Quartus IP File (`.ip`), or Platform Designer System File (`.qsys`). Syntax errors in these files cause errors during compilation. For example, the software may ignore improperly formatted settings and assignments.
- Do not compile multiple projects into the same directory. Instead, use a separate directory for each project.
- By default, the Quartus Prime software saves all project output files, such as Text-Format Report Files (`.rpt`), in the project directory. If you want to change the location of output files, instead of manually moving project output files, click **Assignments > Settings > Compilation Process Settings**, and specify the **Save project output files in specified directory** option.

5.1.3. Viewing Design Hierarchy and Adding Missing Source Files

With the introduction of the fast hierarchy display feature, you can now view the design hierarchy quickly and add the missing source files without having to wait until the completion of the Analysis & Elaboration compilation process.

Perform these steps to view the design hierarchy and add the missing source files:

Prerequisite: After launching the Quartus Prime Pro Edition software GUI and creating your project, ensure you have added all RTL source files to the project and top-level entity name of the design, without which, you cannot proceed with Analysis & Elaboration.

1. Run either **Analysis & Synthesis** or **Analysis & Elaboration** on the compilation dashboard.
2. Navigate to the left-hand **Project Navigator** > **Hierarchy** tab.

The **Hierarchy** viewer allows you to quickly view your design hierarchy, and any errors or warnings before the design is fully elaborated. You can also cross-probe between the source files and information, warnings or error messages. All entities with missing source files are highlighted enabling you to make quick design fixes.

Figure 48. Fast Display of Design Hierarchy

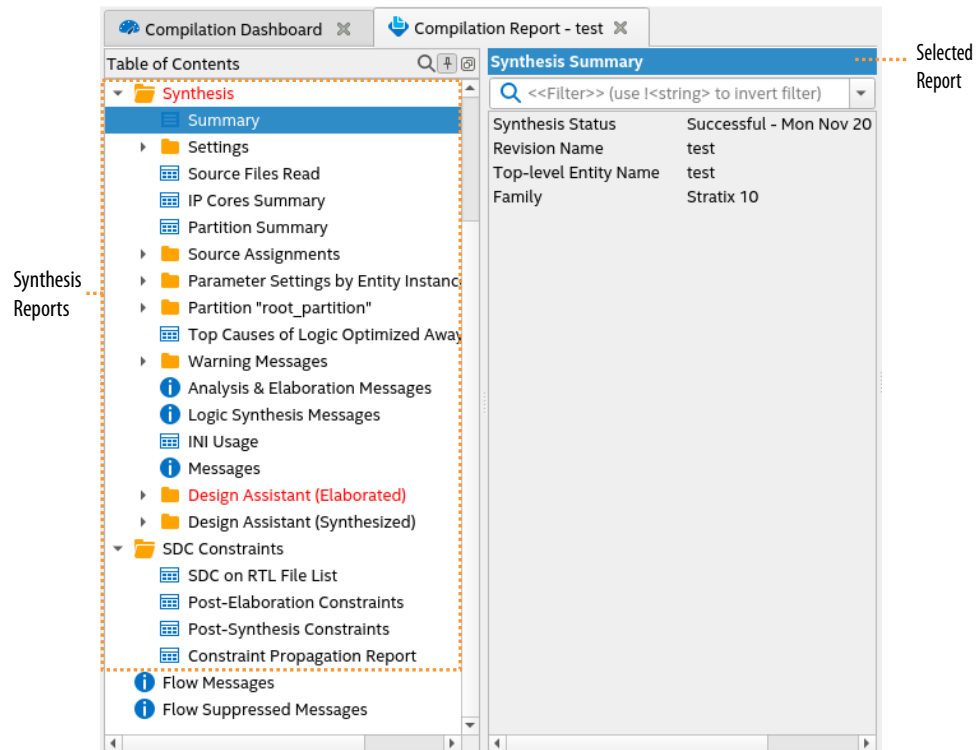
Instance	Entity	mbinational ALU	cated Logic Regi	lock Memory Bit	DSP Blocks	Pins	Max Depth	ull Hierarchy Nam
Agilex 5: ASECO65BB32AE55		3935 (1)	3146 (0)	515072 (0)	0 (0)	77 (0)	11.3 (3)	
alt_sld_fab_0	alt_sld_fab_0	125 (0)	88 (0)	0	0	67	3.0 (2.0)	auto_fab_0
pd_top_clk	pd_top_clk		pd_top_clk	ip/pd_top/pd...				
clk	clk		pd_top_clk	ip/pd_top/pd...				
irq_mapper	pd_top_altera...	irq_mapper	altera_irq_ma...	pd_top.qsys				
jtag	pd_top_jtag	121 (0)	113 (0)	1024	0	0	5.0 (0.0)	jtag
led	pd_top_led	2 (0)	4 (0)	0	0	0	4.0 (0.0)	led
mm_interconnect_0	pd_top_altera...	653 (0)	535 (0)	0	0	0	8.0 (0.0)	mm_interconne...
new_ocm	new_ocm	72 (0)	3 (0)	512000	0	0	8.0 (0.0)	new_ocm
new_pll	new_pll	0 (0)	0 (0)	0	0	0	0.0 (0.0)	new_pll
niosv	niosv	2953 (0)	2378 (0)	2048	0	0	8.3 (0.0)	niosv
reset	pd_top_reset	reset	pd_top_reset	ip/pd_top/pd...				
resetrelease	resetrelease	resetrelease	resetrelease	ip/pd_top/res...				
rst_controller	altera_reset_c...	6 (5)	16 (10)	0	0	0	1.0 (1.0)	rst_controller

5.1.4. Viewing Project Reports

The Compilation Report panel updates dynamically to display detailed reports during project processing. To access Compilation Reports, click (**Processing** > **Compilation Report**).

Review the detailed information in these the compilation reports to determine correct implementation. Right-click report data to locate and edit the source in project files.

Figure 49. Compilation Report

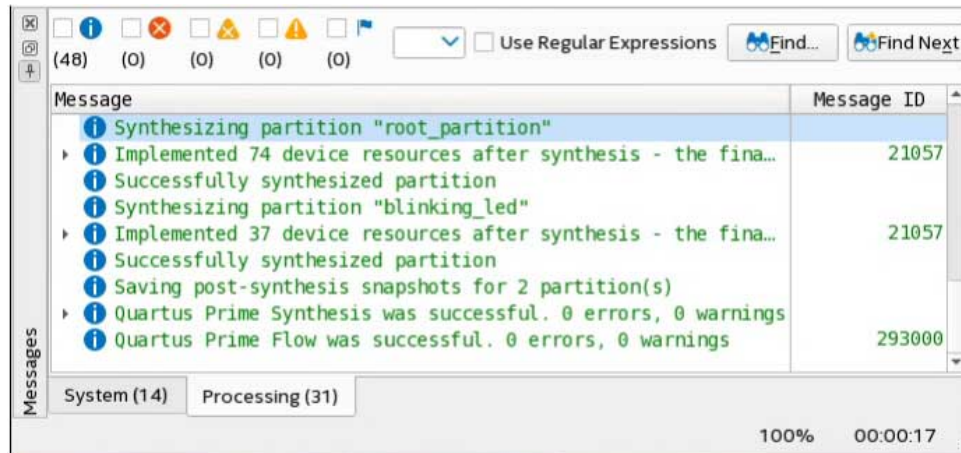


5.1.5. Viewing Project Messages

The Messages window (**View ► Messages**) displays information, warning, and error messages about Quartus Prime processes. Right-click messages to locate the source or get message help.

- **Processing** tab—displays messages from the most recent process
- **System** tab—displays messages unrelated to design processing
- **Find**—locates specific messages

Figure 50. Messages Window



5.1.5.1. Viewing Synthesis Warning Messages

Warning messages may contain hierarchies. In **Compilation Report > Synthesis > Messages** window, you can view hierarchical warning messages up to any level including the parent and child messages. For each message, you can view its source, file location, line number, and message ID by selecting appropriate column under **Message Column** (right-click on a message in the **Message** panel as shown in the following image and click **Message Column**).

Figure 51. Synthesis Warning Messages (Two levels)

Message	Source	File	Line	Message ID
ⓘ Synthesizing partition "root_partition"	Synthesis			
ⓘ Timing-Driven Synthesis is running on partition "root_partition"	Synthesis			286031
➤ ⓘ Implemented 48 device resources after synthesis - the final report	Synthesis			21057
ⓘ Successfully synthesized partition	Synthesis			
ⓘ Synthesizing partition "blinking_led_top"	Synthesis			
⚠ Output pins are stuck at VCC or GND	Synthesis			13024
⚠ Pin "u_blinking_led_top value_top[0]" is stuck at VCC	Design Software	/nfs/site/...	33	13410
⚠ Pin "u_blinking_led_top value_top[1]" is stuck at VCC	Design Software	/nfs/site/...	33	13410
⚠ Pin "u_blinking_led_top value_top[2]" is stuck at VCC	Design Software	/nfs/site/...	33	13410
⚠ Pin "u_blinking_led_top value_top[3]" is stuck at VCC	Design Software	/nfs/site/...	33	13410
➤ ⓘ Implemented 6 device resources after synthesis - the final report	Synthesis			21057
ⓘ Successfully synthesized partition	Synthesis			
ⓘ Saving post-synthesis snapshots for 2 partition(s)	Synthesis			
➤ ⓘ Quartus Prime Synthesis was successful. 0 errors, 6 warnings	Synthesis			

Figure 52. Example of Synthesis Warning Messages With Three Levels

⚠ Synthesized away the following node(s):
➤ ⚠ Synthesized away the following node(s) of type LCELL buffer:
⚠ Synthesized away node "ab"
⚠ Synthesized away node "abd"

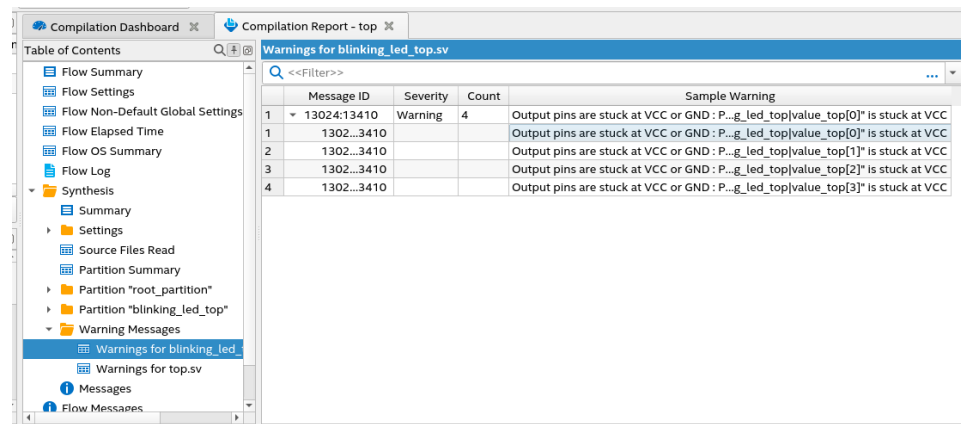
In **Compilation Report > Synthesis > Warning Messages**, you can view a comprehensive list of synthesis warning messages for each source file included in your design. You can view all child warning messages hidden within a parent warning message by expanding the collapsible rows. To view the location of each warning, perform these steps:

1. Right-click on the message.
2. Select the **Locate Node** option.
3. Select the desired tool to view the node.

Note: In the source file-specific warning messages window, messages are hierarchical in nature and display up to three levels. If the warning messages go deeper than three levels, use the **Message (View > Messages)** window to view them.

In the source file-specific warning messages window, hierarchical messages are displayed with message IDs and sample warning messages that are a combination of the parent and child messages.

Figure 53. Synthesis Warning Messages for Each Source File



5.1.5.2. Suppressing Message Display

You can suppress display of unimportant messages from the Messages window, so that you can focus on the messages that are important to you. To suppress one or more messages from displaying in the Messages window, right-click the message, and then click any of the following commands:

- **Suppress Message**—suppresses all messages that match the exact text you specify.
- **Suppress Messages with Matching ID**—suppresses all messages that match the message ID number you specify, ignoring variables.
- **Suppress Messages with Matching Keyword**—suppresses all messages that match the keyword or hierarchy you specify.
- **Message Suppression Manager**—allows you to create and edit message suppression rules. You can define message suppression rules by message text, message ID number, or keyword.

Note:

- You cannot suppress error or Intel legal agreement messages.
- Suppressing a message also suppresses any submessages.
- A root message does not display if you suppress all of the root message's submessages.
- Message suppression is project revision-specific. Derivative project revisions inherit any suppression.
- You cannot edit messages or suppression rules during compilation.
- Messages are written to `stdout` when you use command-line executables.

Figure 54. Message Suppression Manager



Suppressing Messages by Design Entity

You can optionally suppress messages by design entity without modifying HDL. Entity-based message suppression can be helpful to eliminate insignificant warnings for specific IP components or design entities that may be obscuring other more important warnings.

To suppress messages by design entity, add the following line to the project `.qsf`, or to the `.qip` file for stand-alone IP components:

```
set_global_assignment -name MESSAGE_DISABLE -entity <name>
```

5.1.5.3. Promoting Critical Warnings to Errors

You can promote critical warnings to errors so that the compilation flow halts on receiving the critical warnings as it does with an errors. All critical warnings are supported.

You can only promote the message IDs on open projects.

1. In the **Message** dialog box, right-click on the critical warning you want to promote to an error.
2. Click **Message Promotion** ► **Promote Critical Message ID to Error**
The software now treats the critical warning as an error.
3. To clear all promotions, click **Message Promotion** ► **Clear All Message Promotions**
4. Alternatively, manually promote or demote a critical warning in the .qsf. For example:

```
set_global_assignment -name PROMOTE_WARNING_TO_ERROR 12677
```

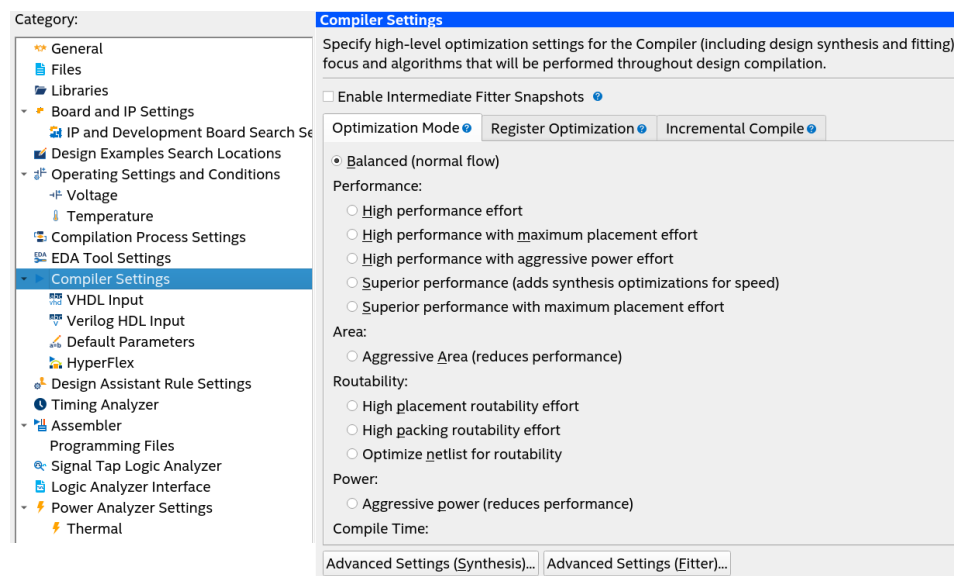
5.2. Managing Project Settings

The New Project Wizard guides you to make initial project settings when you setup a new project. You can modify these and other global project settings in the **Settings** and **Device** dialog boxes, respectively. The .qsf stores the settings for each project revision. The optimization of these project settings helps the Compiler to generate programming files that meet or exceed your specifications.

Global Project Settings

To access global project settings, click **Assignments** ► **Settings**, or click **Settings** on the **Tasks** pane.

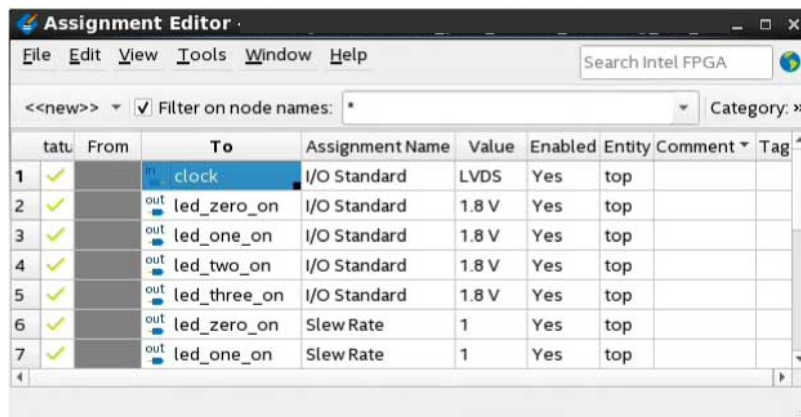
Figure 55. Settings Dialog Box for Global Project Settings



The **Settings** dialog box provides access to settings that control project design files, synthesis, Fitter, and timing constraints, operating conditions, EDA tool file generation, programming file generation, and other project-level settings.

Additionally, the Assignment Editor (**Assignments** ► **Assignment Editor**) provides a spreadsheet-like interface for specifying instance-specific settings and constraints.

Figure 56. Assignment Editor

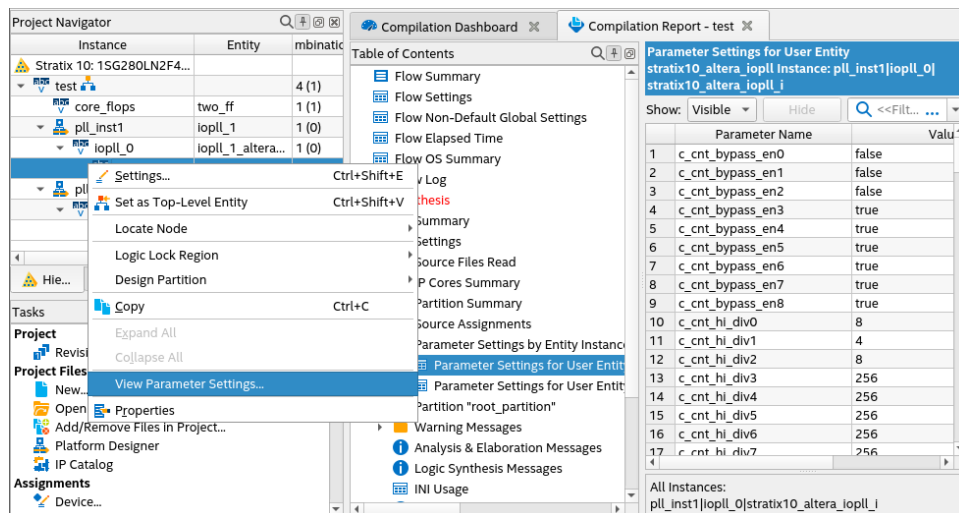


5.3. Viewing Parameter Settings From the Project Navigator

Starting from the Quartus Prime Pro Edition software version 23.3, you can view the parameter settings for a module directly from the **Project Navigator**.

To access the settings, locate the module, right-click and select **View Parameter Settings** in the context-sensitive menu. Compilation Report appears displaying the parameter settings for the entity, as shown in the following image:

Figure 57. Viewing Parameter Settings



5.4. Managing Logic Design Files

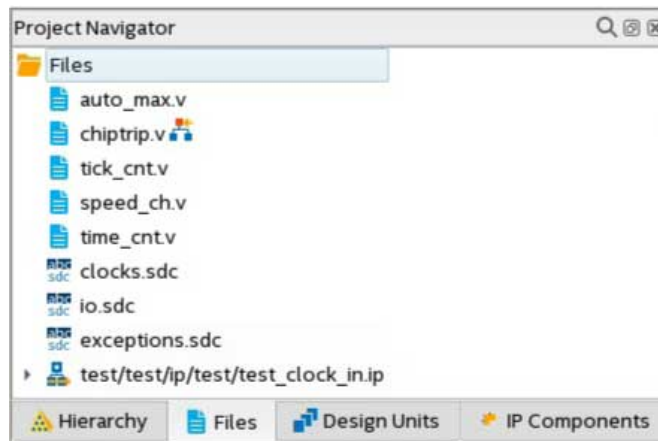
The Quartus Prime software helps you create and manage the logic design files in your project. Logic design files contain the logic that implements your design. When you add a logic design file to the project, the Compiler automatically includes that file in the next compilation. The Compiler synthesizes your logic design files to generate programming files for your target device.

The Quartus Prime software includes full-featured schematic and text editors, as well as HDL templates to accelerate your design work. The Quartus Prime software supports VHDL Design Files (.vhd), Verilog HDL Design Files (.v), and SystemVerilog (.sv). In addition, you can combine your logic design files with Intel and third-party IP core design files, including combining components into a Platform Designer system (.qsys).

Caution: Starting from the Quartus Prime Pro Edition software version 23.3, the compiler cannot synthesize schematic Block Design File (.bdf). For more information, refer to [Converting Symbolic BDF Files to Acceptable File Formats](#) on page 45.

The New Project Wizard prompts you to identify logic design files. Add or remove project files by clicking **Project > Add/Remove Files in Project**. View the project's logic design files in the Project Navigator.

Figure 58. Design and IP Files in Project Navigator



Right-click files in the Project Navigator to to:

- **Open** and edit the file
- **Remove File from Project**
- **Set as Top-Level Entity** for the project revision
- **Create a Symbol File for Current File** for display in schematic editors
- Edit file **Properties**

5.4.1. Including Design Libraries

Include design files libraries in your project. Specify libraries for a single project, or for all Quartus Prime projects. The .qsf stores project library information.

The quartus2.ini file stores global library information.

1. Click **Assignment > Settings**.
2. Click **Libraries** and specify the **Project Library name** or **Global Library name**. Alternatively, you can specify project libraries with SEARCH_PATH in the .qsf, and global libraries in the quartus2.ini file.

Related Information

[Design Library Migration Guidelines](#) on page 47

5.4.2. Creating a Project Copy

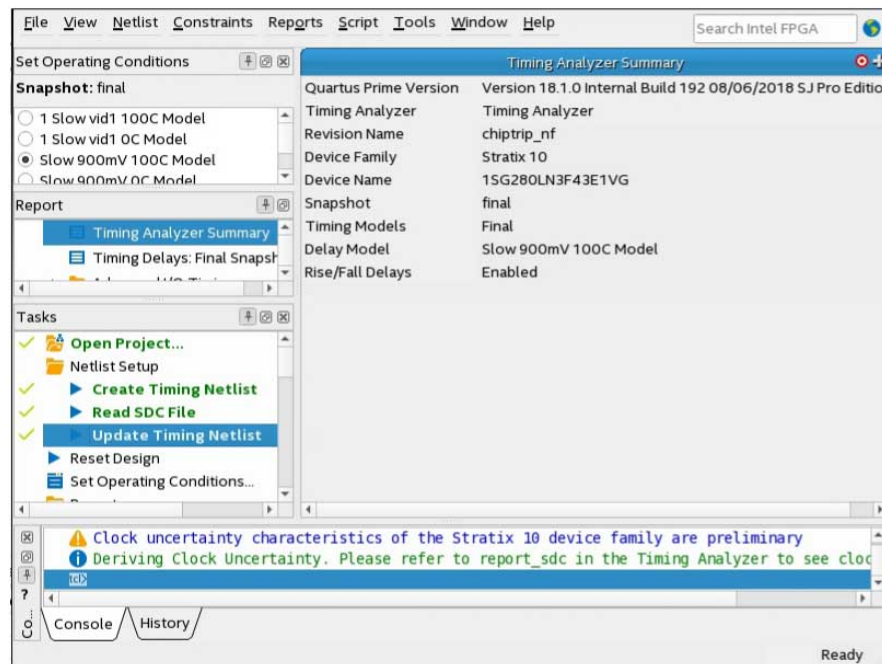
Click **Project > Copy Project** to create a separate copy of your project, rather than just a revision within the same project.

The project copy includes separate copies of all design files, any .qsf files, and project revisions. You can use this technique to optimize project copies for different applications that require design file differences. For example, you can optimize one project to interface with a 32-bit data bus, and optimize a project copy to interface with a 64-bit data bus.

5.5. Managing Timing Constraints

Apply appropriate timing constraints to correctly optimize fitting and analyze timing for your design. The Fitter optimizes the placement of logic in the device to meet your specified timing and routing constraints.

Figure 59. Timing Analyzer



Specify timing constraints in the Timing Analyzer (**Tools > Timing Analyzer**), or in an .sdc file. Specify constraints for clock characteristics, timing exceptions, and external signal setup and hold times before running analysis. The Timing Analyzer reports detailed information about the performance of your design compared with constraints in the Compilation Report panel.

Save the constraints you specify in the GUI in an industry-standard Synopsys Design Constraints File (.sdc). You can subsequently edit the text-based .sdc file directly. If you refer to multiple .sdc files in a parent .sdc file, the Timing Analyzer reads the .sdc files in the order you list.

5.6. Integrating Other EDA Tools

You can optionally integrate supported EDA synthesis, netlist partitioning, simulation, and signal integrity verification tools into the Quartus Prime design flow.

The Quartus Prime software supports input netlist files from supported EDA synthesis tools. The Compiler's EDA Netlist Writer module (quartus_eda) can automatically generate output files for processing in other EDA tools. The EDA Netlist Writer runs optionally as part of a full compilation, or you can run EDA Netlist Writer separately from the GUI or at the command line. The following functions are available to simplify EDA tool integration:

Table 33. EDA Tool Integration Functions

EDA Integration Task	EDA Integration Function
Specify settings for generation of output files for processing in other EDA tools.	Click Assignments > Settings > EDA Tool Settings to specify options for supported tools.
Generate output files for processing in other EDA tools.	Click Processing > Start > Start EDA Netlist Writer (or run quartus_eda) to generate files.
Compile RTL and gate-level simulation model libraries for your device, supported EDA simulators, and design language.	Click Tools > Launch Simulation Library Compiler to compile simulation libraries easily.
Generate EDA tool-specific setup scripts to compile, elaborate, and simulate Intel FPGA IP models and simulation model library files.	Specify options for Simulation file output when generating Intel FPGA IP with IP parameter editor.
Generate files that allow supported EDA tools to perform netlist modifications, such as adding new modules, partitioning the netlist, and changing module connectivity.	Use the quartus_eda -resynthesis command to generate a Verilog Quartus Mapping File (.vqm) that contains a node-level (or atom) representation of the netlist in standard structural Verilog RTL.
Include files generated by other EDA design entry or synthesis tools in your project as synthesized design files.	Click Project > Add/Remove Files In Project to add supported Design File files from other EDA tools.

5.7. Exporting Compilation Results

The Quartus Prime Compiler writes the results to a set of database files. You can run a command to export the compilation results database as a single Quartus Database File (.qdb).

After running design compilation, the exported .qdb file contains the data to reproduce similar compilation results in another project, or in a later software version. You can export your project's compilation results database for import to another project or migration to a later Quartus Prime software version.

You can export the .qdb for your entire project or for a design partition that you define in your project. When migrating the database for an entire project, you can export the compilation database in a *version-compatible* format to ensure

compatibility for import to a later software version. Although you cannot directly read the contents of the .qdb file after export, you can view attributes of the database file in the Quartus Database File Viewer.

Table 34. Exporting Compilation Results

To Export Compilation Results For	Method	Description
Complete Design	Click Project > Export Design	Saves compilation results for the current project revision in a version-compatible Quartus database file (.qdb) that you can import to another project or migrate to a later version of the Quartus Prime software. You can export the results for the synthesized or final compilation snapshot. <i>Note:</i> Not supported for Agilex 7 devices.
Design Partition	Click Project > Export Design Partition	Saves compilation results for a design partition as a Partition Database File (.qdb) that you can import to another project using the same version of the Quartus Prime software. You can export the results for the synthesized or final compilation snapshot.

Related Information

[Creating Database-Only Archives](#) on page 112

5.7.1. Exporting a Version-Compatible Compilation Database

You can export a project compilation database to a format that ensures version-compatibility with a later version of the Quartus Prime software. The Quartus Prime Pro Edition software version supports export of version-compatible databases for the following software versions and devices:

Table 35. Version-Compatible Compilation Database Support

The first table column indicates the first version to support version-compatible compilation database export for the specified devices.

- Note:*
- Database import supports two major versions back. For example, a database that you export from version 19.3, you can then import using version 19.3, 20.1, and 20.3. However, you cannot import version 19.3 to 21.1.
 - You can export from any version that follows a supported version, if the version still supports the devices.

First Version with 'Export Design' Support	Stratix 10 and Devices	Arria 10 and Cyclone 10 GX Devices
18.0	No Support.	Supports all devices.
18.1	<ul style="list-style-type: none"> 1SG250L 1SG280H_S2 1SG280L 1SG280L_S3 1SX250L 1SX280L 1SX280L_S3 	Supports all devices.
19.1	<ul style="list-style-type: none"> 1SM16BH 1SM21BH 1SM16CH 	Supports all devices.
<i>continued...</i>		

First Version with 'Export Design' Support	Stratix 10 and Devices	Arria 10 and Cyclone 10 GX Devices
	<ul style="list-style-type: none"> 1SM21CH 1SM21KH 1SM16KH 1SM21LH 1SM16LH 	
19.3	<ul style="list-style-type: none"> 1SG10MH_U1 1SG10MH_U2 1ST250E 1ST280E 1SM16E 1SM21E 1ST165E 1ST210E 1SG166H 1SG211H 	Supports all devices.
20.1	<ul style="list-style-type: none"> 1SD280P 1ST040E 1ST085E 1ST110E 	Supports all devices.
20.3	<ul style="list-style-type: none"> 1SD21BP 1SG040H 1SX040H 	Supports all devices.
20.4	<ul style="list-style-type: none"> 1SN21BH 1SN21CE 	Supports all devices.

1. In the Quartus Prime software, open the project that you want to export.
2. Generate synthesis or final compilation results by running one of the following commands:
 - Click **Processing > Start > Start Analysis & Synthesis** to generate synthesized compilation results.
 - Click **Processing > Start Compilation** to generate final compilation results.
3. Click **Project > Export Design**. Select the **synthesized** or **final Snapshot**.

Figure 60. Export Design Dialog Box



4. Specify a name for the **Quartus Database File** to contain the exported results, and click **OK**.
5. To include the exported design's settings and constraint files, copy the `.qsf` and `.sdc` files to the import project directory.

5.7.2. Importing a Version-Compatible Compilation Database

Follow these steps to import a project compilation database into a newer version of the Quartus Prime software:

Note: Designs exported from the Quartus Prime Pro Edition software versions 23.2 or earlier cannot be imported into version 23.3 due to the new DNI database.

1. Export a version-compatible compilation database for a complete design, as [Exporting a Version-Compatible Compilation Database](#) on page 100 describes.
2. In a newer version of the Quartus Prime software, open the original project. Click **Yes** if prompted to open a project created with a different software version.
3. Click **Project > Import Design** and specify the **Quartus Database File**. To remove previous results, turn on **Overwrite existing project's databases**

Figure 61. Import Design Dialog Box

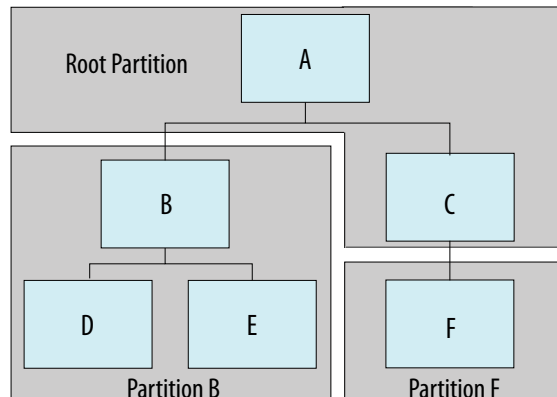


4. Click **OK**. When you compile the imported design, run only Compiler stages that occur after the stage the .qdb preserves, rather than running a full compilation. For example, if you import a version-compatible database that contains the synthesized snapshot, start compilation with the Fitter (**Processing > Start > Start Fitter**). If you import a version-compatible database that contains the final snapshot, start compilation with Timing Analysis (Signoff) (**Processing > Start > Start Timing Analysis (Signoff)**).

5.7.3. Creating a Design Partition

A design partition is a logical, named, hierarchical boundary that you can assign to an instance in your design. Defining a design partition allows you to optimize and lock down the compilation results for individual blocks. You can then optionally export the compilation results of a design partition for reuse in another context, such as reuse in another project.

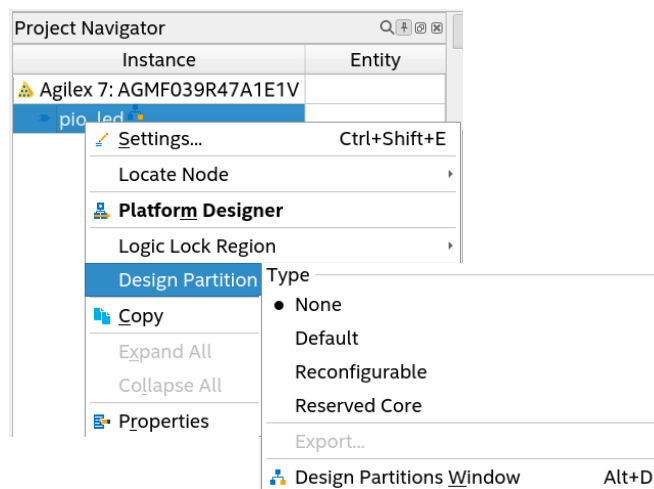
Figure 62. Design Partitions in Design Hierarchy



Follow these steps to create and modify design partitions:

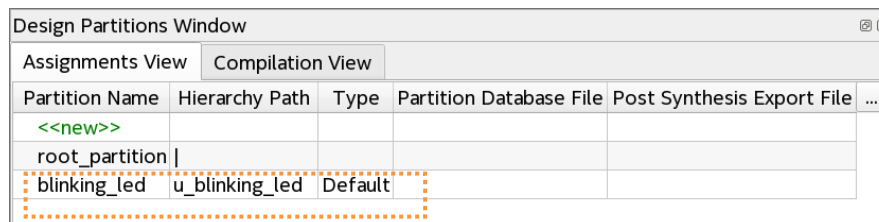
1. In the Quartus Prime software, open the project that you want to partition.
2. Generate synthesis or final compilation results by running one of the following commands:
 - Click **Processing** > **Start** > **Start Analysis & Synthesis** to generate synthesized compilation results.
 - Click **Processing** > **Start Compilation** to generate final compilation results.
3. In the Project Navigator, right-click an instance in the **Hierarchy** tab, click **Design Partition** > **Set as Design Partition**.

Figure 63. Creating a Design Partition from the Project Hierarchy



4. To view and edit all design partitions in the project, click **Assignments** > **Design Partitions Window**.

Figure 64. Design Partitions Window



- Specify the properties of the design partition in the Design Partitions Window. The following settings are available:

Table 36. Design Partition Settings

Option	Description
Partition Name	Specifies the partition name. Each partition name must be unique and consist of only alphanumeric characters. The Quartus Prime software automatically creates a top-level () "root_partition" for each project revision.
Hierarchy Path	Specifies the hierarchy path of the entity instance that you assign to the partition. You specify this value in the Create New Partition dialog box. The root partition hierarchy path is .
Type	Double-click to specify one of the following partition types that control how the Compiler processes and implements the partition: <ul style="list-style-type: none"> Default—Identifies a standard partition. The Compiler processes the partition using the associated design source files. Reconfigurable—Identifies a reconfigurable partition in a partial reconfiguration flow. Specify the Reconfigurable type to preserve synthesis results, while allowing refit of the partition in the PR flow. Reserved Core—Identifies a partition in a block-based design flow that is reserved for core development by a Consumer reusing the device periphery.
Empty	Specifies an empty partition that the Compiler skips. This setting is incompatible with the Reserved Core and Partition Database File settings for the same partition.
Partition Database File	Specifies a Partition Database File (.qdb) that the Compiler uses during compilation of the partition. You export the .qdb for the stage of compilation that you want to reuse (synthesized or final). Assign the .qdb to a partition to reuse those results in another context.
Entity Re-binding	<ul style="list-style-type: none"> PR Flow—specifies the entity that replaces the default persona in each implementation revision. Root Partition Reuse Flow —specifies the entity that replaces the reserved core logic in the consumer project.
Color	Specifies the color-coding of the partition in the Chip Planner and Design Partition Planner displays.
Post Synthesis Export File	Automatically exports post-synthesis compilation results for the partition to the specified .qdb file each time Analysis & Synthesis runs. You can automatically export any design partition that does not have a preserved parent partition, including the root_partition.
Post Final Export File	Automatically exports post-final compilation results for the partition to the specified .qdb file each time the final stage of the Fitter runs. You can automatically export any design partition that does not have a preserved parent partition, including the root_partition.

5.7.4. Exporting a Design Partition

The following steps describe export of design partitions that you create in your project.

Note: Design partitions exported from the Quartus Prime Pro Edition software versions 23.2 or earlier cannot be imported into version 23.3 or later due to the new DNI database.

When you compile a design containing design partitions, the Compiler can preserve a synthesis or final snapshot of results for each partition. You can export the synthesized or final compilation results for individual design partitions with the **Export Design Partition** dialog box.

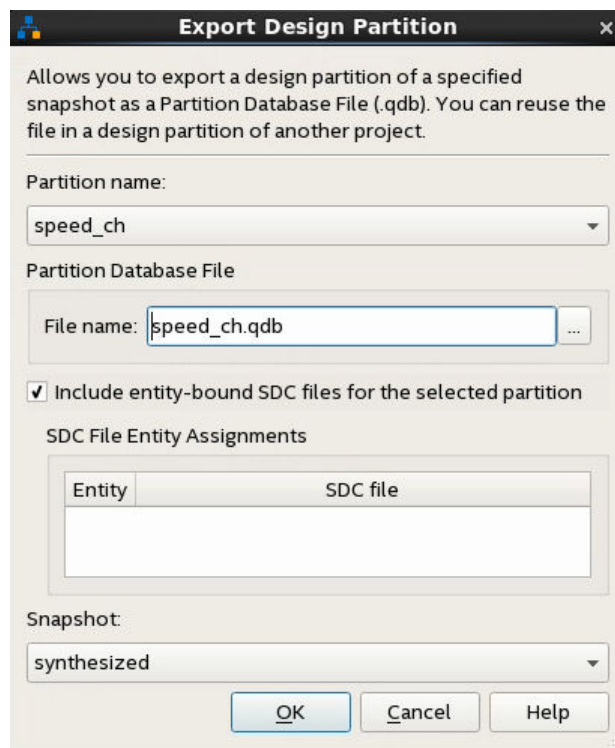
If the partition includes any entity-bound .sdc files, you can include those constraints in the .qdb. In addition, you can automate export of one or more partitions in the Design Partitions Window.

Manual Design Partition Export

Follow these steps to manually export a design partition with the **Export Design Partition** dialog box:

1. Open a project and create one or more design partitions. [Creating a Design Partition](#) on page 102 describes this process.
2. Run synthesis (**Processing > Start > Start Analysis & Synthesis**) or full compilation (**Processing > Start Compilation**), depending on which compilation results that you want to export.
3. Click **Project > Export Design Partition**, and specify one or more options in the **Export Design Partition** dialog box:

Figure 65. Export Design Partition Dialog Box



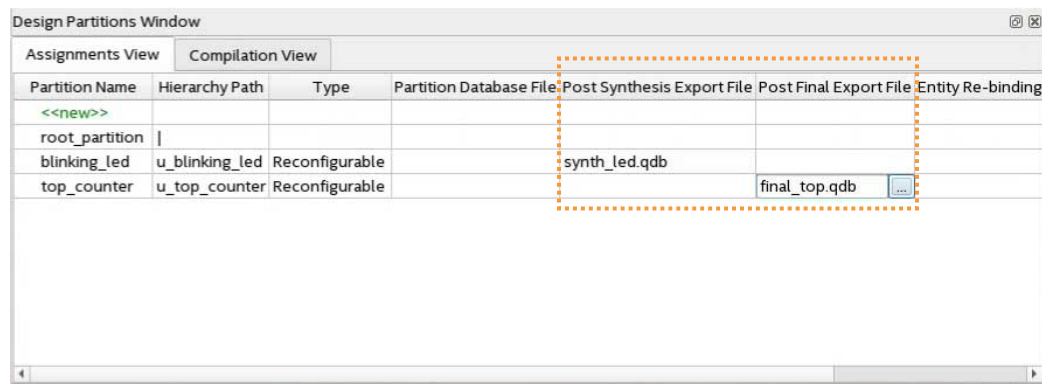
- Select the **Partition name** and the compilation **Snapshot** for export.
 - To include any entity-bound .sdc files in the exported .qdb, turn on **Include entity-bound SDC files for the selected partition**.
4. Click **OK**. The compilation results for the design partition exports to the file that you specify.

Automated Design Partition Export

Follow these steps to automatically export one or more design partitions following each compilation:

1. Open a project containing one or more design partitions. [Creating a Design Partition](#) on page 102 describes this process.
2. To open the Design Partitions Window, click **Assignments > Design Partitions Window**.
3. To automatically export a partition with synthesis results after each time you run synthesis, specify the a .qdb export path and file name for the **Post Synthesis Export File** option for that partition. If you specify only a file name without a path, the file exports to the output_files directory after compilation.
4. To automatically export a partition with final snapshot results each time you run the Fitter, specify a .qdb file name for the **Post Final Export File** option for that partition. If you specify only a file name without a path, the file exports to the output_files directory after compilation.

Figure 66. Specifying Export File in Design Partitions Window



.qsf Equivalent Assignment:

```
set_instance_assignment -name EXPORT_PARTITION_SNAPSHOT_<FINAL|SYNTHESIZED> \
    <hpath> -to <file_name>.qdb
```

Related Information

- [Intel Quartus Prime Pro Edition User Guide: Block Based Design](#)
- [Intel Quartus Prime Pro Edition User Guide: Partial Reconfiguration](#)

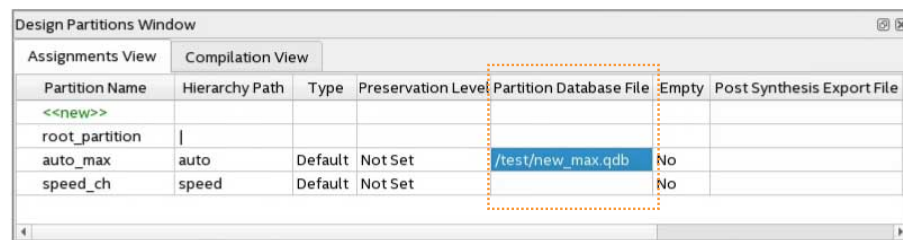
5.7.5. Reusing a Design Partition

You can reuse the compilation results of a design partition exported from another Quartus Prime project. Reuse of a design partition allows you to share a synthesized or final design block with another designer. Refer to *Intel Quartus Prime Pro Edition User Guide: Block-Based Design* for more information about reuse of design partitions.

To reuse an exported design partition in another project, you assign the exported partition .qdb to an appropriately configured design partition in the target project via the Design Partition Window:

1. Export a design partition with the appropriate snapshot, as [Exporting a Design Partition](#) on page 104 describes.
2. Open the target Quartus Prime project that you want to reuse the exported partition.
3. Click **Processing > Start > Start Analysis & Elaboration**.
4. Click **Assignments > Design Partitions Window**, and then create a design partition to contain the logic and compilation results of the exported .qdb.
5. Click the **Partition Database File** option for the new partition and select the exported .qdb file.

Figure 67. Partition Database File Setting in Design Partitions Window



6. Specify any other properties of the design partition in the Design Partitions Window. The Compiler uses the partition's assigned .qdb as the source.

5.7.6. Viewing Quartus Database File Information

Although you cannot directly read a .qdb file, you can view helpful attributes about the file to quickly identify its contents and suitability for use.

The Quartus Prime software automatically stores metadata about the project of origin when you export a Quartus Database File (.qdb). You can then use the Quartus Database File Viewer to display the attributes of any of these .qdb files.

Follow these steps to view the attributes of a .qdb file:

1. In the Quartus Prime software, click **File > Open**, select **Design Files** for **Files of Type**, and select a .qdb file.
2. Click **Open**. The Quartus Database File Viewer displays project and resource utilization attributes of the .qdb.

Alternatively, run the following command-line equivalent:

```
quartus_cdb --extract_metadata --file <archive_name.qdb> \
--type quartus --dir <extraction_directory> \
[--overwrite]
```

Figure 68. Quartus Database File Viewer

The screenshot shows the 'Project Summary' window for 'blinking_led.qdb'. It contains two main sections: 'Project Information' and 'Resource Utilization'.

Attribute	Value
Project Information	
Contents	Partition
Date	Thu Aug 16 10:37:40 2018
Device	1SG280HN1F43E2VGS1
Entity	blinking_led
Family	Stratix 10
Partition Name	blinking_led
Revision Name	blinking_led
Revision Type	Unspecified
Snapshot	synthesized
Version	18.1.0
Version-Compatible	No
Resource Utilization	
Average fan-out	0.16
Combinational ALUT usage for logic	0
Dedicated logic registers	2
Estimate of Logic utilization (ALMs needed)	1
I/O pins	35
Maximum fan-out	2
Maximum fan-out node	u_blinking_led[counter[23]]
Total DSP Blocks	0
Total fan-out	6

5.7.6.1. QDB File Attribute Types

The Quartus Database Viewer can display the following attributes of a .qdb file:

Table 37. QDB File Attributes

QDB Attribute Types	Attribute	Example
Project Information	Contents	Partition
	Date	Thu Jan 23 10:56:23 2018
	Device	10AX016C3U19E2LG
	Entity (if Partition)	Counter
	Family	Arria 10
	Partition Name	root_partition
	Revision Name	Top
	Revision Type	PR_BASE
	Snapshot	synthesized
	Version	18.1.0 Pro Edition
	Version-Compatible	Yes
Resource Utilization (exported for partition QDB only)	For synthesized snapshot partition lists data from the Synthesis Resource Usage Summary report.	Average fan-out:16 Dedicated logic registers:14 Estimate of Logic utilization:1

continued...

		I/O pins:35 Maximum fan-out:2 Maximum fan-out node:counter[23] Total DSP Blocks:0 Total fan-out:6 ...
	For the final snapshot partition, lists data from the Fitter Partition Statistics report.	Average fan-out:.16 Combinational ALUTs: 16 I/O Registers M20Ks ...

5.7.7. Clearing Compilation Results

You can clean the project database if you want to remove prior compilation results for all project revisions or for specific revisions. For example, you must clear previous compilation results before importing a version-compatible database to an existing project.

1. Click **Project > Clean Project**.
2. Select **All revisions** to clear the databases for all revisions of the current project, or specify a **Revision name** to clear only the revision's database you specify.
3. Click **OK**. A message indicates when the database is clean.

Figure 69. Clean Project Dialog Box Cleans the Project Database



5.8. Archiving Projects

You can optionally save the elements of a project in a single, compressed Quartus Prime Archive File (.qar) by clicking **Project > Archive Project**. The .qar preserves RTL design, project, and settings files required to restore the project.

Use this technique to share projects between designers, or to transfer your project to a new version of the Quartus Prime software, or to Intel support. Optionally add compilation results, Platform Designer system files, and third-party EDA tool files to the archive.

Related Information

[Project Archive Commands](#) on page 114

5.8.1. Manually Adding Files To Archives

Follow these steps to add files to a project archive manually:

Note: If preserving a custom component as part of an Quartus Prime Archive (.qar), you must first explicitly add the component _hw.tcl file to the project to ensure that the .qar includes the component. Click **Project > Add/Remove Files in Project** to add files to your project.

1. Click **Project > Archive Project** and specify the archive file name.
2. Click **Advanced**.
3. Select the **File set** for archive or select **Custom**. Turn on **File subsets** for the archive.
4. Click **Add** and select Platform Designer system or EDA tool files. Click **OK**.
5. Click **Archive**.

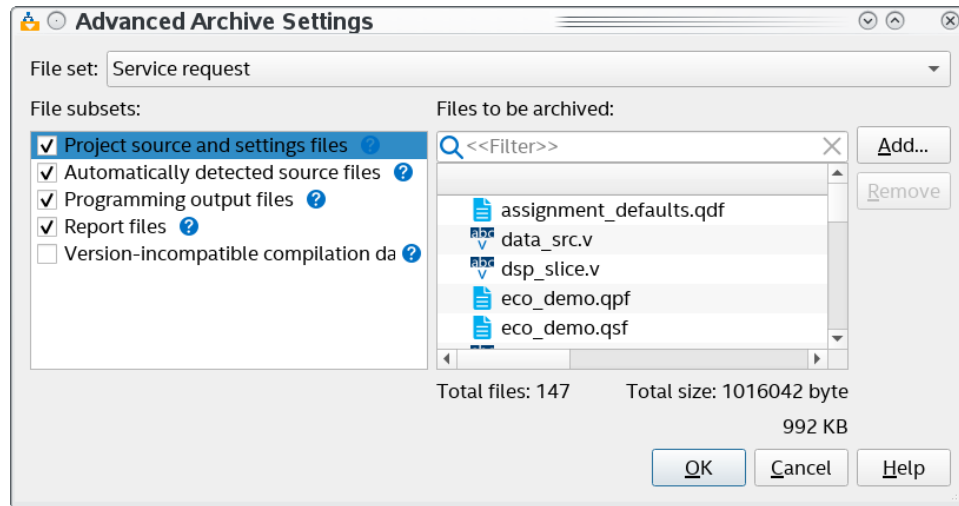
5.8.2. Archiving Projects for Service Requests

When archiving projects for a service request, include all needed file types for proper debugging by customer support.

To identify and include appropriate archive files for an Intel service request:

1. Click **Project > Archive Project** and specify the archive file name.
2. Click **Advanced**.
3. In **File set**, select **Service request** to include files for Intel Support.
 - Project source and setting files
(.v, .vhd, .vqm, .qsf, .sdc, .qip, .qpf, .cmp)
 - Automatically detected source files (various)
 - Programming output files (.jdi, .sof, .pof)
 - Report files (.rpt, .pin, .summary, .msg)
4. Click **OK**, and then click **Archive**.

Figure 70. Archiving Project for Service Request



5.8.3. Archiving Projects for External Revision Control

Your project may involve different team members with distributed responsibilities, such as sub-module design, device and system integration, simulation, and timing closure. In such cases, it may be useful to track and protect file revisions in an external revision control system.

While Quartus Prime project revisions preserve various project setting and constraint combinations, external revision control systems can also track and merge RTL source code, simulation testbenches, and build scripts. External revision control supports design file version experimentation through branching and merging different versions of source code from multiple designers. Refer to your external revision control documentation for setup information.

5.8.3.1. Project Files to Include In External Revision Control

When archiving Quartus Prime projects for external source control, The **Source control** setting in **Advanced Archive Settings** dialog box is preset to include all appropriate file types for source control automatically.

Figure 71. Advanced Archive Settings Dialog Box

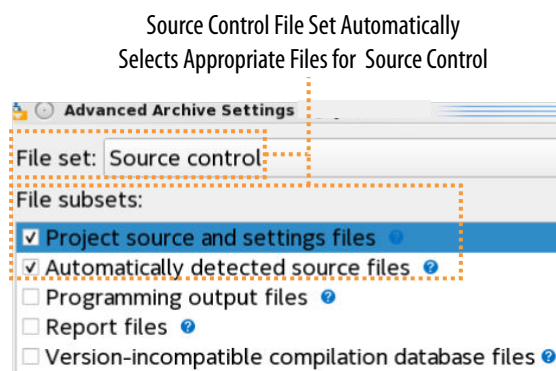


Table 38. Project Files to Include In External Revision Control

File Type	Description
Quartus Prime project setting and assignment files	<ul style="list-style-type: none"> Quartus Prime Project Files (.qpf) Quartus Prime Settings Files (.qsf) Quartus Prime Pin Planner File (.ppf)
Timing constraint files	Synopsys Design Constraint Files (.sdc)
Design files	<ul style="list-style-type: none"> Verilog HDL Design Files (.v) SystemVerilog Design Files (.sv) VHDL Design Files (.vhd) Block Symbol Files (.bsf) Verilog Quartus Mapping Files (.vqm) Platform Designer System Files (.qsys) State Machine Editor Files (.smf) Tcl Script Design Files (.tcl)
System and IP files	<ul style="list-style-type: none"> IP variation file (.ip) Verilog IP design files (.v) SystemVerilog IP design files (.sv) VHDL IP design files (.sv) VHDL Component Declaration Files (.cmp) Quartus Prime IP file (.qip) Quartus Prime Simulation IP File (.sip) Platform Designer System Files (.qsys) Platform Designer connection and parameterization files (.sopcinfo) IP upgrade status files (.csv) IP synthesis parameters files (.qgsynthc) IP simulation parameters files (.qgsimc) Platform Designer system exported as (.tcl).
EDA tool integration files	<ul style="list-style-type: none"> Verilog HDL Output Files (.vo) VHDL Output Files (.vho) VHDL simulation model files (.vhd) Verilog HDL simulation model files (.v) Simulation library files (cds.lib, hdl.var) Simulation setup scripts (_setup.sh, .tcl, .spd, .txt)

5.8.4. Creating Database-Only Archives

If your project contains sensitive RTL that you do not want to share with Intel support, you can create a *database-only* archive. A database-only archive contains only the minimum files required to run timing analysis, fitter, assembler, and GUI design-inspection tools like Chip Planner.

A database-only archive includes only the project Quartus databases and any additional files required for compilation. It does not include RTL files.

You can review the complete list of files included in the archive in a report generated when you create a database-only archive.

**Security
Note:**

A database-only archive does not guarantee protection for sharing your design without sharing your RTL. The RTL Netlist Viewer, Technology Map Viewer, and other views, along with the EDA Netlist Writer, are still available for projects exported using this feature.

With some effort, the original content can be reverse engineered.

To disable these features, encrypt your design. For details, see [Support for the IEEE 1735 Encryption Standard](#) on page 83.

Before creating a database-only archive, your project must have completed one of the following compilation stages:

- **Synthesis**
Archives that are created after running Synthesis can be used to run the fitter and then complete timing analysis, run the assembler, and use GUI-based design-inspection tools.
- **Finalized**
Archives that are created after completing a full compilation flow for your project can be used to complete timing analysis, run the assembler, and use GUI design-inspection tools.

To create a database-only archive, run the following command:

```
quartus_sh --archive_database -project <project_file> [-use_final_db]
```

Specify the `-use_final_db` option to create a database-only archive based on the finalized snapshot of your project. Otherwise, a database-only archive based on the synthesized snapshot is created.

The command generates two files: a `.qar` file that contains the database-only archive, and a `.contents.txt` file that lists files that are included in the `.qar` file.

You can get command syntax details by running the following command:

```
quartus_sh --help=archive_database
```

Related Information

[Support for the IEEE 1735 Encryption Standard](#) on page 83

5.9. Command-Line Interface

You can optionally use command-line executables or scripts to run project commands, rather than using the GUI. This technique can be helpful if you have many settings and wish to track them in a single file or spreadsheet for iterative comparison. The `.qsf` supports only a limited subset of Tcl commands. Therefore, pass settings and constraints using a Tcl script:

1. Create a text file with the extension `.tcl` that contains your assignments in Tcl format.
2. Source the Tcl script file by adding the following line to the `.qsf`:

```
set_global_assignment -name SOURCE_TCL_SCR IPT_FILE <file name>.
```

5.9.1. Project Revision Commands

create_revision Command

create_revision defines the properties of a new project revision.

```
create_revision <name> -based_on <revision_name> -set_current -new_rev_type \
    <rev_type> -root_partition_qdb_file <root qdb>
```

Table 39. create_revision Command Options

Option	Description
based_on (optional)	Specifies the revision name on which the new revision bases its settings.
set_current (optional)	Sets the new revision as the current revision.
-new_rev_type	Specifies a base or impl (implementation) type for a new revision.
root_partition_qdb_file	Specifies the name of a static region .qdb if already known when creating a revision.

get_project_revisions Command

get_project_revisions returns a list of all revisions in the project.

```
get_project_revisions <project_name>
```

delete_revision Command

delete_revision deletes the revision you specify from your project.

```
delete_revision <revision name>
```

set_current_revision Command

set_current_revision sets the revision you specify as the current revision.

```
set_current_revision -force <revision name>
```

Related Information

- [Optimizing Settings with Project Revisions](#) on page 121
- [Optimize Settings with Design Space Explorer II](#)
- [Design Space Explorer II Tool](#)
- [Using Design Space Explorer II \(DSE II\) Video](#)

5.9.2. Project Archive Commands

project_archive Command

project_archive archives your project into a single, compressed .qar file.

```
project_archive <name>.qar
```

Table 40. project_archive Command Options

Options	Description
-all_revisions	Includes all revisions of the current project in the archive.
-common_directory /<name>	Preserves original project directory structure in specified subdirectory.
-include_libraries	Includes libraries in archive.
-include_outputs	Includes output files in archive.
-use_file_set <file_set>	Includes specified fileset in archive.
-version_compatible_database	Includes version-compatible database files in archive.

restore_archive Command

Restores an archived project to a destination directory with optional overwriting of current contents.

```
project_restore <name>.qar -destination <directory name> -overwrite
```

Related Information

[Archiving Projects](#) on page 109

5.9.3. Project Database Commands

export_database Command

export_design exports the specified project database to the .qdb file you specify.

These commands require the quartus_cdb executable.

```
quartus_cdb <revision name> --export_design --file <file name>.qdb \
--snapshot <synthesized/final>
```

import_database Command

import_design imports the specified project database to the .qdb file you specify.

```
quartus_cdb <revision name> --import_design --file <file name>.qdb
```

export_block Command

export_block exports the specified partition database to the .qdb file you specify.

```
quartus_cdb -r <project name> -c <revision name> --export_block \
<partition name> --snapshot <name> --file <file name>.qdb
```

5.9.3.1. quartus_cdb Executables to Manage Version-Compatible Databases

The command-line arguments to the quartus_cdb executable in the Quartus Prime Pro software are export_design and import_design. The exported version-compatible design files are archived in a file (with a .qdb extension). This differs from the Quartus Prime Standard Edition software, which writes all files to a directory.

In the Quartus Prime Standard Edition software, the flow exports both post-map and post-fit databases. In the Quartus Prime Pro Edition software, the export command requires the `snapshot` argument to indicate the target snapshot to export. If the specified snapshot has not been compiled, the flow exits with an error. In ACDS 16.0, export is limited to “synthesized” and “final” snapshots.

```
quartus_cdb <project_name> [-c <revision_name>] --export_design  
--snapshot <snapshot_name> --file <filename>.qdb
```

The import command takes the exported *.qdb file and the project to which you want to import the design.

```
quartus_cdb <project_name> [-c <revision_name>] --import_design  
--file <archive>.qdb [--overwrite] [--timing_analysis_mode]
```

The `--timing_analysis_mode` option is only available for Arria 10 designs. The option disables legality checks for certain configuration rules that may have changed from prior versions of the Quartus Prime software. Use this option only if you cannot successfully import your design without it. After you have imported a design in timing analysis mode, you cannot use it to generate programming files.

5.10. Related Trainings

You can take up the following training to help you understand how to manage your project:

- [Instructor-Led Training: Using Quartus Prime Software](#)

A. Next Steps After Getting Started

Navigating Content Through Tasks

Use the following table to navigate this guide through user-tasks:

			
Plan FPGA Design for RTL Flow or Work With Intel FPGA IP Cores	Create a New Project or Migrate Your Existing Project to Quartus Prime Pro Edition Software	Manage Your Quartus Prime Pro Edition Projects	Review Next Steps

Once you complete installing and licensing the required Intel FPGA development software and setting up your Quartus Prime Pro Edition project, refer to the following topics for additional resources and training to aid your design journey:

A.1. Additional Resources

Resource	Description
Intel Community for FPGA Intellectual Property	Allows you to post queries and get responses to Intel FPGA IP-related issues.
Intel Community for Quartus Prime Software	Allows you to post queries and get responses to Quartus Prime software-related issues.
Intel Community for Intel FPGA Software Installation and Licensing	Allows you to post queries and get responses to Intel FPGA software installation and licensing issues.
Intel FPGA Knowledge Base	Provides links to applicable articles that span a variety of Quartus Prime software-related issues.
Intel FPGA Self-Service Licensing Center	Provides support for licensing Intel FPGA software.
Quartus Prime Pro Edition User Guide: Design Recommendations	Describes best practices for designing FPGAs with the Quartus Prime Pro Edition software.
Quartus Prime Pro Edition User Guide: Design Compilation	Describes how to set up, run, and optimize for all stages of the Quartus Prime Pro Edition software compiler. The compiler synthesizes, places, and routes your design before generating a device programming file.
Quartus Prime Pro Edition User Guide: Scripting	Describes use of Tcl and command line scripts to control the Quartus Prime Pro Edition software and to perform a wide range of functions, such as managing projects, specifying constraints, running compilation or timing analysis, or generating reports.
continued...	

Resource	Description
Scripting with Quartus Prime Software	Demonstrates how to use the command-line executables for the Quartus Prime design flow.
Quartus Prime Pro Edition User Guide: Third-party Simulation	Describes RTL- and gate-level design simulation support for third-party simulation tools by Aldec*, Cadence*, Mentor Graphics*, and Synopsys* that allow you to verify design behavior before device programming. Includes simulator support, simulation flows, and simulating Intel FPGA IP.
Questa*-Intel FPGA Edition Quick-Start: Quartus Prime Pro Edition User Guide	Demonstrates how to simulate a Quartus Prime Pro Edition design in the Questa*-Intel FPGA Edition simulator.
How to Setup RTL Simulations in Quartus Prime, Platform Designer, and Third-Party Simulators	Describes how to setup an RTL-based simulation using the IP setup simulation utility.
Quartus Prime Pro Edition Software User Guides Collection	Each user guide in the collection covers a specific topic and is designed to help you easily and efficiently find the information you need to see your design through to completion.

A.2. Training

You can take up the following training to aid your FPGA design journey:

- [University Self-Guided Lab: Become an FPGA Designer in 4 Hours](#)
- [Introduction to Tcl](#)
- [Quartus Prime Software Tcl Scripting](#)
- [Command Line Scripting Capabilities in the Quartus Prime Pro Edition Software](#)
- [Quartus Prime Software Tcl Scripting](#)
- [Intel FPGA Power and Thermal Calculator for Intel FPGA Devices](#)
- [DSP Builder Advanced Blockset: Getting Started](#)
- [Using FPGAs with the Intel oneAPI Toolkits](#)
- [Instructor-Led Training: Intel SoC FPGA Basics](#)
- [University Self-Guided Lab: Introduction to Simulation and Debug of FPGAs](#)

For more Intel FPGA trainings, refer to the [Intel FPGA Technical Training Catalog](#) and [Intel FPGA channel on YouTube*](#).



B. Using the Design Space Explorer II

The Design Space Explorer II tool (**Tools ► Launch Design Space Explorer II**) allows you to find optimal project settings for resource, performance, or power optimization goals.

Refer to the following links for information on how to use the tool and what each option means in the GUI:

- [Design Space Explorer II Tool](#)
 - [Setup Page](#)
 - [Project Page](#)
 - [Exploration Page](#)
 - [Status Page](#)
 - [Report Page](#)
- [Using Design Space Explorer](#)

B.1. Optimizing Project Settings

Optimize project settings to meet your design goals.

The Quartus Prime Design Space Explorer II iteratively compiles your project with various setting combinations to find the optimal settings for your goals. Alternatively, you can create a project revision or project copy to manually compare various project settings and design combinations.

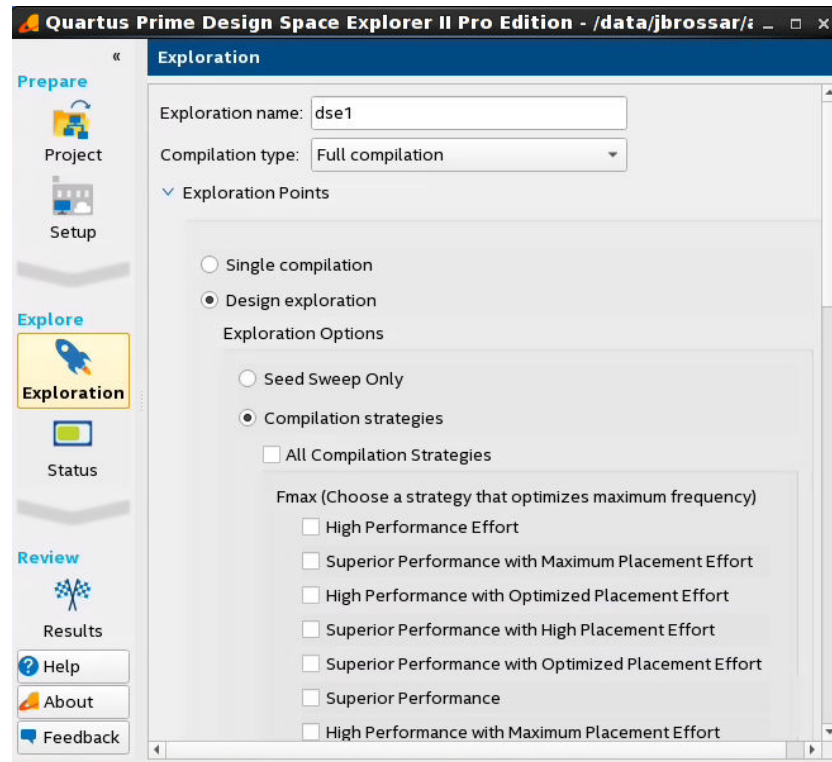
B.1.1. Optimizing Settings with Design Space Explorer II

Design Space Explorer II (DSE II) processes a design using combinations of settings and constraints, and reports the best combination of settings and constraints for the design. You can also take advantage of the DSE II parallelization abilities to compile on multiple computers.

In DSE II, an *exploration point* is a collection of Analysis & Synthesis, Fitter, and placement settings, and a group of exploration points is a *design exploration*. A design exploration can also include different fitter seeds.

DSE II compiles the design using the settings corresponding to each exploration point. When the compilation finishes, DSE II evaluates the performance data against an optimization goal that you specify. You can direct the DSE II to optimize for timing, area, or power. DSE II attempts multiple seeds to identify one meeting your requirements. DSE II can run different compilations on multiple computers in parallel to streamline timing closure.

Figure 72. Design Space Explorer II



You can run DSE II at any step in the design process. However, because large changes in a design can neutralize gains achieved from optimizing settings, Intel recommends that you run DSE II late in the design cycle.

Note: When comparing the results of different seed sweeps with DSE II, changing any of the following variables can cause differences in the compilation results between seed sweeps, resulting in a somewhat different fit in each case:

- The number or type of CPUs that DSE II uses to perform the seed sweeps
- Any change to the operating system
- Any change to source file content or location
- Any change to the Compiler settings or Timing Analyzer settings

For more information, refer to [Fitter Seed](#).

B.1.1.1. DSE II Computing Resources

You can configure DSE II to take advantage of your computing resources to run the design explorations. In the DSE II GUI, the **Setup** page contains the job launch options, and the **Status** page allows you to monitor and control jobs.

DSE II supports running compilations on your local computer or a remote host through LSF, SSH or Torque. For SSH, you can also define a comma-separated list of remote hosts.

If you have a laptop or standard computer, you can use the single compilation feature to compile your design on a workstation with higher computing performance and memory capacity.

When running on a compute farm, you can direct the DSE II to safely exit after submitting all the jobs while the compilations continue to run until completion. Optionally, you can receive an e-mail when the compilations are complete.

If you launch jobs using SSH, the remote host must enable public and private key authentication. For private keys encrypted with a pass phrase, the remote host must run the ssh key agent to decrypt the private key, so the `quartus_dse` executable can access the key.

Note: Windows remote hosts require Cygwin's sshd server and PuTTY.

B.1.1.2. DSE II Optimization Parameters

DSE II provides a collection of predefined exploration spaces that focus on what you want to optimize. Additionally, you can define a set of compilation seeds. The number of explorations points is the number of seeds multiplied by the number of exploration modes.

Note: The availability of predefined spaces depends on the device family that the design targets.

In the DSE GUI, you specify these settings in the **Exploration** page.

B.1.1.3. DSE II Result Management

DSE II compares the compilation results to determine the best Quartus Prime software settings for the design. The **Report** page displays a summary of results.

In an exploration, DSE II selects the best worst-case slack value from among all timing corners across all exploration points. If you want to optimize for worst-case setup slack or hold slack, specify timing constraints in the Quartus Prime software.

Disk Space

By default, DSE II saves all the compilation data. You can save disk space by limiting the type of files that you want to save after a compilation finishes. These settings are in the **Exploration** page, **Results** section.

Reports

DSE II has reporting tools that help you quickly determine important design metrics, such as worse-case slack, across all exploration points.

DSE II provides a performance data report for all points it explores and saves the information in a `project-name.dse.rpt` file in the project directory. DSE II archives the settings of the exploration points in Quartus Prime Archive Files (`.qar`).

B.1.2. Optimizing Settings with Project Revisions

You can save multiple, named project revisions within your Quartus Prime project (**Project > Revisions**). Each project revision captures a unique set of project settings and constraints, while using the same set of logic design files.

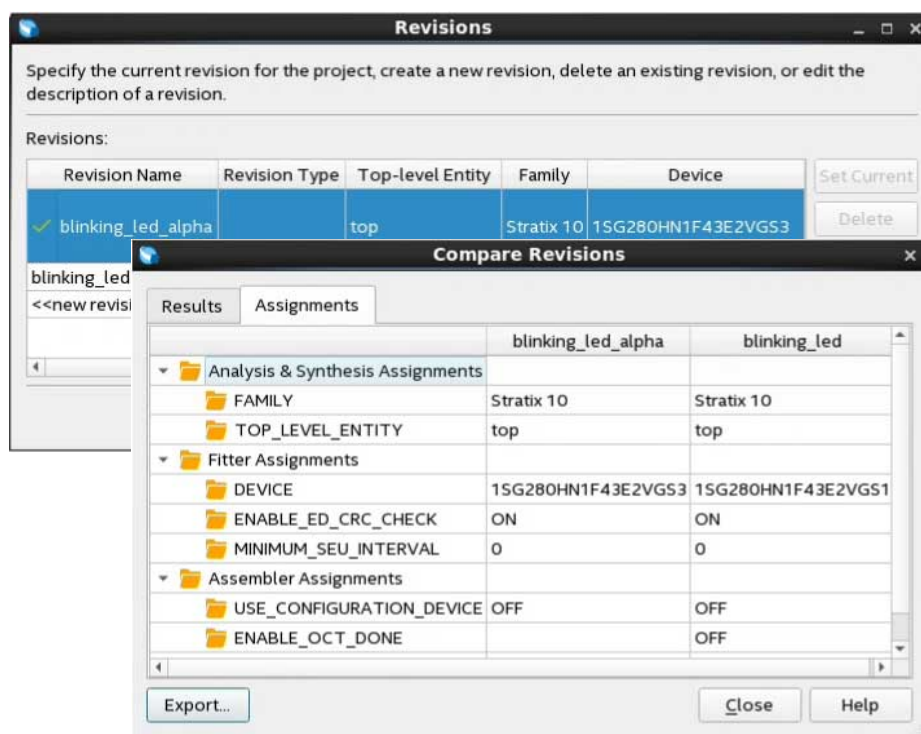
Use revisions to experiment with different settings while preserving the original. Optimize different revisions for separate applications:

- Create a unique revision to optimize a design for different criteria, such as by area in one revision and by f_{MAX} in another revision.
- When you create a new revision the default Quartus Prime settings initially apply.
- Create a revision of a revision to experiment with settings and constraints. The child revision includes all the assignments and settings of the parent revision.

You create, delete, and edit revisions in the **Revisions** dialog box. Each time you create a new project revision, the Quartus Prime software creates a new .qsf using the revision name.

To compare each revision's synthesis, fitting, and timing analysis results side-by-side, click **Project > Revisions** and then click **Compare**. In addition to viewing the compilation **Results** of each revision, you can also compare the **Assignments** for each revision. This comparison reveals how different optimization options affect your design.

Figure 73. Comparing Project Revisions



Related Information

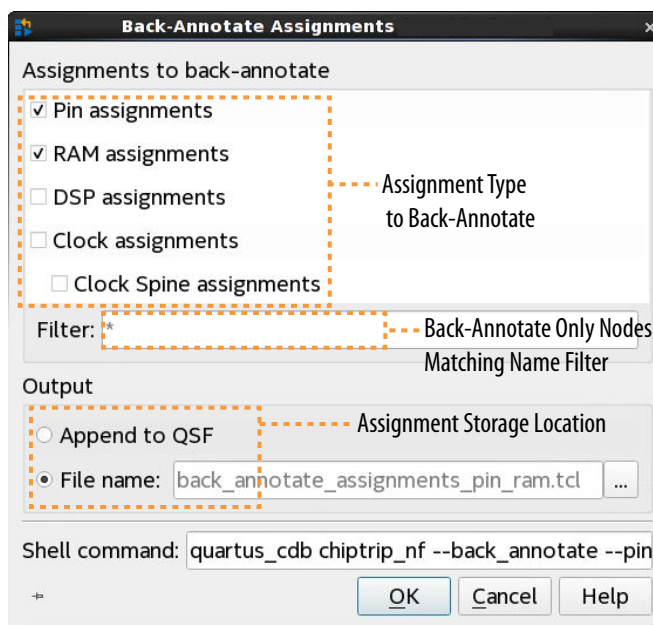
- [Project Revision Commands](#) on page 114
- [Optimize Settings with Design Space Explorer II](#)
- [Design Space Explorer II Tool](#)
- [Using Design Space Explorer II \(DSE II\) Video](#)

B.1.3. Back-Annotating Optimized Assignments

The Compiler maps the elements of your design to specific device resources during fitting. After compilation, you can back-annotate (copy) the Compiler's resource assignments to preserve that same implementation in subsequent compilations. Back-annotation can simplify timing closure by allowing you to lock down placement of your optimized results.

Locking down placement of large blocks related to Clocks, RAMs, and DSPs can produce higher f_{MAX} with less noise. Large blocks like RAMs and DSPs have heavier connectivity than regular LABs, complicating movement during placement. When a seed produces good results from suitable RAM and DSP placement, you can capture that placement with back-annotation. Subsequent compiles can then benefit from the high quality RAM and DSP placement from the good seed.

Figure 74. Back-Annotate Assignments Dialog Box



To back-annotate (copy) the device resource assignments from the last compilation to the project .qsf (or to a Tcl file) for use in the next compilation:

1. Run a full compilation, or run the Fitter through at least the **Place** stage.
2. Click **Assignments** ► **Back-Annotate Assignments**.
3. Under **Assignments to back-annotate**, specify whether you want to preserve **Pin assignments**, **RAM assignments**, **DSP assignments**, **Clock assignments**, and **Clock Spine assignments** in the back-annotation.
4. In **Filter**, specify a text string (including wildcards) if you want to filter back-annotated assignments by entity name.
5. Under **Output**, specify whether to save the back-annotated assignments to the .qsf or to a Tcl file. A default Tcl file name displays.

Alternatively, you can run back-annotation with the following `quartus_cdb` executable. The **Shell command** field displays the shell command constructed by the options that you specify in the GUI.

```
quartus_cdb chiptrip_nf --back_annotate --pin --ram --dsp --clocks \
--spines --file "<file>.tcl"
```

Note: Check available arguments by running `quartus_cdb <project> --back_annotate --help`.

Related Information

[Back Annotation in Quartus Prime Software](#)

B.2. Running DSE II

Note: Before running DSE II, specify the timing constraints for the design.

This description covers the type of settings that you need to define when you want to run a design exploration. For details about all the options available in the GUI, refer to the Quartus Prime Help.

To perform a design exploration with the DSE II tool:

1. Start the DSE II tool.
If you have an open project in the Quartus Prime software and launch DSE II, a dialog box appears asking if you want to close the Quartus Prime software. Click **Yes**.
2. In the **Project** page, specify the project and revision that you want to explore.
3. In the **Setup** page, specify whether you want to perform a local or a remote exploration, and set up the job launch.
4. In the **Exploration** page, specify optimization settings and goals.
5. When the configuration is complete, click **Start**.

B.3. Setting Up Remote Farm Using Design Space Explorer II

To launch Design Space Explorer II, in the Quartus Prime Pro Edition GUI, click **Tools** ► **Launch Design Space Explorer II**. Click **Yes** to the message that appears. This closes the Quartus Prime software and launches the Design Space Explorer II.

Under the **Project** tab, click **Open Project** to add your project to the Design Space Explorer II. Refer to [Project Page \(Design Space Explorer II\)](#) for information about all options on this tab.

Use one of the following methods to set up your remote farm:

LSF Remote Farm

Follow these steps to set up your remote machine using the Design Space Explorer II and LSF remote compilation type:

1. Ensure you have set up your LSF environment. If not, request your IT administrator to set up the LSF environment.
2. Once the LSF environment is ready, launch the command line interface and execute the `bsub sleep 60` command.
3. Under the **Setup** tab, select **Remote** compilation type and choose the LSF option from the drop-down list. Populate all mandatory settings under **Specify custom settings for LSF** with the LSF environment-specific information.

Refer to [Setup Page \(Design Space Explorer II\)](#) for information about all options on this tab.

4. Customize the settings as necessary.
5. Under the **Exploration** tab, expand the **Exploration Points** section.
6. Select **Design exploration**.
7. Under **Exploration Options**, select **Seed Sweep Only**.
8. Under **Seeds**, select **Create**. By default, it must be set to 2 seeds.
9. Click **Start**. Wait until the design exploration is complete.
10. Click the **Results** tab to review the status of the design exploration.

SSH Remote Farm

Follow these steps to set up your remote machine using the Design Space Explorer II and SSH remote compilation type:

1. Install the open-source PuTTY Key Generator tool and launch it.
2. Click **Generate** to generate the public/private key pair.
3. Enter the key passphrase.
4. Click **Save private key** to save the private key with a `.ppk` extension.
5. Click **Save public key** to save the public key as `putty_gen_public_key.pub`.
6. On your machine, change to the SSH directory and copy the contents of the `putty_gen_public_key.pub` file.
7. In the Design Space, under the **Setup** tab, select **SSH** compilation type and specify the following:
 - For **Hostname**, enter the server name.
 - For **private_key**, enter the path to your private key (`.ppk` file).
 - For **SSH Client**, enter the path to the `plink.exe` file. You can find this in the same directory where you installed the PuTTY tool.
 - For **Farm Operating System**, enter your system type (`linux` or `windows`).

The remaining settings are similar to LSF settings. Refer to [Setup Page \(Design Space Explorer II\)](#) for information about all options on this tab.

8. Under the **Exploration** tab, expand the **Exploration Points** section.
9. Select **Design exploration**.

10. Under **Exploration Options**, select **Seed Sweep Only**.
11. Under **Seeds**, select **Create**. By default, it must be set to 2 seeds.
12. Click **Start**. Wait until the design exploration is complete.
13. Click the **Results** tab to review the status of the design exploration.

C. Document Revision History for Quartus Prime Pro Edition User Guide Getting Started

Document Version	Quartus Prime Version	Changes
2024.04.01	24.1	<ul style="list-style-type: none"> Made the following updates in <i>Introduction to Quartus Prime Pro Edition</i>: <ul style="list-style-type: none"> Included additional steps to the quick start table. Updated the Quartus Prime software main page image in the table. Updated the support matrix image to include Agilex 5 device support. Updated supported features table to include Agilex 5 device support for hyper-aware design flow. Updated the Intel FPGA developmental tools table to include Agilex 5 device support for PTC. Revised prerequisite training list in <i>Prerequisite Knowledge and Training</i>. Consolidated the information of design planning into a table in <i>Planning FPGA Design for RTL Flow</i>. Added <i>Viewing Design Hierarchy and Adding Missing Source Files</i>. Removed the Quartus Prime software main page image in <i>Creating a New FPGA Design Project</i>. Revised the IP version upgrade path image in <i>Upgrading IP Cores</i>. Revised <i>Generating IP Simulation Files</i> topic entirely. Revised the note about .bdf files in <i>Managing Logic Design Files</i>.
2023.12.04	23.4	<ul style="list-style-type: none"> Made major reorganization of chapters and topics. Added additional information to <i>Introduction to Quartus Prime Pro Edition</i>. Renamed <i>FPGA Basic Design Prerequisites</i> as <i>Prerequisite Knowledge and Training</i> and included a list of trainings. Revised the information for accessing online design examples in <i>Creating a New Project from a Design Example</i>. Renamed the chapter title "Design Planning" to "Planning FPGA Design for RTL Flow." Renamed the topic "Plan for Hierarchical and Team-Based Designs" to "Selecting the Design Methodology."

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Document Version	Quartus Prime Version	Changes
		<ul style="list-style-type: none"> Added the following: <ul style="list-style-type: none"> Before You Begin Acronyms Navigate Content Through Tasks Selecting the Design Methodology Flat Design Vs. Incremental Block-based Design Partial Reconfiguration Design Related Trainings Migrating Your AMD* Vivado* Project to Quartus Prime Pro Edition Migrating Project From One Device to Another Converting Symbolic BDF Files to Acceptable File Formats Project Path Length Considerations Renamed the chapter name from <i>Migrating to Quartus Prime Pro Edition</i> to <i>Selecting a Starting Point for Your Quartus Prime Pro Edition Project</i>. Moved <i>Creating a New FPGA Design Project, Migrating Projects Across Operating Systems</i> and their subtopics from <i>Managing Quartus Prime Projects</i> chapter to this chapter. Chapter renamed as "Working With Intel FPGA IP Cores." Removed the following topics and added a reference to <i>Quartus Prime Pro Edition User Guide: Third-party Simulation</i> where these topics are explained in detail. <ul style="list-style-type: none"> Sourcing Aldec ActiveHDL* or Riviera Pro* Simulator Setup Scripts Sourcing Cadence Incisive* Simulator Setup Scripts Sourcing Cadence Xcelium Simulator Setup Scripts Sourcing QuestaSim* Simulator Setup Scripts Sourcing Synopsys VCS Simulator Setup Scripts Sourcing Synopsys VCS MX Simulator Setup Scripts Moved <i>Creating a New FPGA Design Project, Migrating Projects Across Operating Systems</i> and their subtopics to <i>Selecting a Starting Point for Your Quartus Prime Pro Edition Project</i> chapter. In <i>Managing Logic Design Files</i>, added information about converting .bdf to .v or .vhdl file. Removed "Block Diagram/Schematic Design Files (.bdf)" in <i>Project Files to Include In External Revision Control</i>. Added <i>Viewing Parameter Settings From the Project Navigator</i>. Added an appendix about <i>Using Design Space Explorer II</i> and included related topics. Revised the Power and Thermal Calculator (PTC) image in <i>Planning for Device Power Consumption</i>.
2023.10.02	23.3	<ul style="list-style-type: none"> Updated the compilation dashboard image in <i>Introduction to Quartus Prime Pro Edition</i> and <i>Using the Compilation Dashboard</i>. Removed OpenCL support from the "Intel Quartus Prime Feature Support Matrix" image in <i>Selecting an Quartus Prime Software Edition</i>. Made a minor correction in <i>Logic Lock Region Assignment Examples</i>. Revised the "Quartus Prime Pro Edition IP Version Upgrade Paths" image in <i>Upgrading IP Cores</i>. Updated the dashboard image in <i>Using the Compilation Dashboard</i>.
2023.06.26	23.2	<ul style="list-style-type: none"> Updated <i>Power Analyzer Settings</i> screenshot for new settings name.
continued...		

Document Version	Quartus Prime Version	Changes
2023.04.03	23.1	<ul style="list-style-type: none"> Updated product family name to "Intel Agilex 7." Added note to <i>Upgrade Project Assignments and Constraints</i> about new prompt to update operating temperatures in a migrated project. Updated <i>Support for the IEEE 1735 Encryption Standard</i> topic for new installed location of public encryption key. Updated <i>Intel Quartus Prime Pro Edition IP Version Upgrade Paths</i> support chart.
2022.12.12	22.4	<ul style="list-style-type: none"> Updated <i>Plan for the Target Device or Board</i> topic for board-aware features. Revised <i>Applying Preset Parameters for Specific Applications</i> topic for board-aware features. Added new <i>Viewing, Applying, and Deleting IP Presets</i> topic. Added new <i>Example IP Preset File (.qprs)</i> topic. Revised <i>Customizing IP Presets</i> topic for board-aware features. Added new <i>Defining Preset Pin Assignments</i> section. Revised <i>Creating a New FPGA Design Project</i> for board-aware features. Added <i>Using the Board-Aware Flow</i> topic. Added <i>Creating a New Project from a Design Example</i> topic. Added <i>Family, Device & Board Settings</i> topic. Added <i>Accessing Pre-Installed Design Examples</i> topic. Added <i>Accessing Online Design Examples</i> topic. Added <i>Accessing Downloaded Design Examples</i> topic. Added <i>Internet Connectivity Options</i> topic. Added <i>Design Examples Options</i> topic. Added <i>Specifying a Target Board for the Project</i> topic.
2022.06.20	22.2	<ul style="list-style-type: none"> Added new <i>Top FAQs</i> navigation to document cover. Revised <i>Introduction</i> to add FPGA definition and device selection footnote. Added new <i>FPGA Basic Design Prerequisites</i> topic. Added new <i>Experiment with a Design Example</i> topic. Removed obsolete <i>Simultaneous Switching Noise Analysis</i> topic from this basic discussion.
2022.03.28	22.1	<ul style="list-style-type: none"> Added information about Power and Thermal Calculator in <i>Plan for Device Power Consumption</i>. Removed references to obsolete Advisors from <i>Optimizing Project Settings</i> topic. Added <i>Viewing Synthesis Warning Messages</i> topic. Removed the topic <i>Automated Problem Reports</i>.
2021.10.04	21.3	<ul style="list-style-type: none"> Added support for Questa*-Intel FPGA Edition simulator. Removed support for ModelSim - Intel FPGA Edition simulator. Updated <i>Quartus Prime Pro Edition IP Version Upgrade Paths</i> figure for latest versions.
2021.06.21	21.2	<ul style="list-style-type: none"> Added <i>Version-Compatible Compilation Database Support</i> table. Added "Promoting Critical Warnings to Errors" topic.
2021.03.29	21.1	<ul style="list-style-type: none"> Enhanced <i>Simulating Intel FPGA Designs</i> topic with screenshot, links, and additional contextual details. Updated supported simulator versions and removed support for Cadence Incisive Enterprise* in <i>Simulator Support</i> topic. Revised <i>Generating IP Simulation Files</i> topic for new simulation file output options.
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Document Version	Quartus Prime Version	Changes
		<ul style="list-style-type: none"> Revised <i>Using the EDA Netlist Writer</i> wording for clarity. Added "Creating Database-Only Archives" topic. Added "Promoting Critical Warnings to Errors" topic
2020.11.09	20.3	<ul style="list-style-type: none"> Revised "Introduction to Intel FPGA IP Cores" topic to include Bridges and Adapters and Intel FPGA Interconnect categories in IP Catalog. Updated IP Catalog image. Revised wording of "Intel FPGA IP Versioning" topic for clarity. Added screenshot to "Checking the IP License Status" topic. Added "IP Version Upgrade Paths" diagram to "Upgrading IP Cores" topic. Updated IP Port Differences Report image in "Troubleshooting IP or System Upgrade" topic.
2020.09.28	20.3	<ul style="list-style-type: none"> Updated GUI screenshot in Introduction. Updated "Back-Annotate Optimized Assignments" for support of pins, clocks, RAMs, and DSPs.
2020.05.01	20.1	<ul style="list-style-type: none"> Added note about .qar file requirements to "Design Guidelines for Component Instances" topic.
2019.09.30	19.3	<ul style="list-style-type: none"> Added compilation support for Agilex 7 devices. Added "Checking the IP License Status" topic. Added details to "Support for the IEEE 1735 Encryption Standard." Added Intel FPGA IP Versioning" topic. Added "Disabling Automated Problem Reports" topic. Added "Suppressing Messages" topic.
2019.05.13	18.1	<ul style="list-style-type: none"> Added archives topic. Updated the keyname and added --help information to "Support for the IEEE 1735 Encryption Standard."
2018.10.24	18.1	<ul style="list-style-type: none"> Updated information about obtaining IEEE 1735 Encryption key.
2018.09.24	18.1	<ul style="list-style-type: none"> Added screenshot of Quartus Prime Pro Edition GUI. Moved information about specifying the target board to "Specifying the Target Device or Board" in <i>Managing Projects</i> chapter. Retitled "Creating Design Specifications" to "Create a Design Specification and Test Plan." Retitled "Selecting Intellectual Property Cores" to "Plan for Intellectual Property Cores." Retitled "Using Standard Interfaces" to "Plan for Standard Interfaces." Corrected references to Platform Designer. Retitled "Device Selection" to "Plan for the Target Device." Updated this content to correct Platform Designer names. Moved "Setting Pin Assignments" to <i>Managing Projects</i> chapter as "Generating Pin Assignments for a Target Board." Retitled "Estimating Power" to "Plan for Device Power Consumption." Reorganized this topic into sections for EPE and Power Analyzer. Added link to "Simulator Support, <i>Third-Party Simulation User Guide</i> Retitled "Planning for Device Programming or Configuration" to "Plan for Device Programming" Retitled "Selecting Third-Party EDA Tools" to "Plan for other EDA Tools." Retitled "Planning for On-Chip Debugging Tools" to "Plan for On-Chip Debugging Tools."
continued...		

Document Version	Quartus Prime Version	Changes
		<ul style="list-style-type: none"> Retitled <i>Design Planning with the Intel Quartus Prime Software</i> to <i>Design Planning</i>. Added information about removing assignments from the qsf file that point to legacy output files. Added statement that the Quartus Prime software installer does not support spaces in the installation path. Added "Intel FPGA IP Best Practices" topic. Divided "Introduction to Intel FPGA IP Cores" into separate chapter of <i>Getting Started User Guide</i>. Subdivided "Exporting, Archiving, and Migrating Projects" into separate sections. Described migration of full chip database in "Exporting a Version-Compatible Compilation Database" topic. Described automated .qdb partition export in "Exporting a Design Partition" topic. Added "Viewing Quartus Database File Information" topic. Added "Specifying the Target Device or Board" topic. Divided "Introduction to Intel FPGA IP Cores" into separate chapter. Moved "IP Core Best Practices" topic to <i>Introduction to Intel FPGA IP Cores</i> chapter. Moved "Factors Affecting Compilation Results" topic to <i>Design Compilation: Intel Quartus Prime Pro Edition User Guide</i>.
2018.05.07	18.0	<ul style="list-style-type: none"> Initial release as separate chapter of <i>Getting Started User Guide</i>. Separated <i>Migrating to Quartus Prime Pro Edition</i> as independent chapter in user guide. Initial release as separate chapter of <i>Getting Started User Guide</i>. Separated <i>Design Planning</i> as independent chapter in user guide. Initial release as separate chapter of <i>Getting Started User Guide</i>. Separated <i>Introduction to Intel FPGA IP Cores</i> as independent chapter in user guide. Updated screenshots of IP Catalog and Parameter Editor for latest IP names. Added note about Generate Combined Simulator Setup Scripts command limitations. Added information about generation of simulation files for Xcelium*. Initial release as chapter of <i>Getting Started User Guide</i>. Revised "Exporting a Design Partition" topic to add Include entity-bound SDC files for the selected partition option, to add prerequisite steps, and to remove import step covered in separate topic. Changed title of "Managing Team-Based Designs" to "Exporting, Archiving, and Migrating Projects" and updated content. Changed title of "Migrating Compilation Results Across Software Versions" to "Exporting the Compilation Database" and updated content. Changed title of "Exporting the Results Database" to "Exporting a Version-Compatible Design Compilation Database" and updated content. Changed title of "Importing the Results Database" to "Importing a Version-Compatible Design Compilation Database" and updated content. Changed title of "Cleaning the Project Database" to "Cleaning the Project Compilation Database." Updated screenshots of IP Catalog and Parameter Editor for latest IP names.
continued...		

Document Version	Quartus Prime Version	Changes
2017.11.06	17.1	<ul style="list-style-type: none"> Described Quartus Prime tool name updates for Platform Designer (Qsys), Interface Planner (Blueprint), Timing Analyzer (TimeQuest), Eye Viewer (EyeQ), and Intel Advanced Link Analyzer (Advanced Link Analyzer). Added Verilog HDL Macro example. Updated for latest Intel branding conventions. Added Verilog HDL Macro example. Updated for latest Intel branding conventions. Revised product branding for Intel standards. Revised topics on Intel FPGA IP Evaluation Mode (formerly OpenCore).
2017.05.08	17.0	<ul style="list-style-type: none"> Removed statement about limitations for safe state machines. The Compiler supports safe state machines. State machine inference is enabled by default. Added reference to Block-Based Design Flows. Removed procedure on manual dynamic synthesis report generation. The Compiler automatically generates dynamic synthesis reports when enabled. Removed statement about limitations for safe state machines. The Compiler supports safe state machines. State machine inference is enabled by default. Added note that IP core encryption is supported only in Quartus Prime Pro Edition. Revised product branding for Intel standards.
2016.10.31	16.1	<ul style="list-style-type: none"> Implemented Intel rebranding. Added reference to Partial Reconfiguration support. Added to list of Quartus Prime Standard Edition features unsupported by Quartus Prime Pro Edition. Added topic on Safe State Machine encoding. Described unsupported Quartus Prime Standard Edition physical synthesis options. Removed deprecated Per-Stage Compilation (Beta) Compilation Flow. Changed title from "Remove Filling Vectors" to "Remove Unsized Constant". Implemented Intel rebranding. Described unsupported Quartus Prime Standard Edition physical synthesis options. Changed title from "Remove Filling Vectors" to "Remove Unsized Constant". Removed references to .qsys file creation during Quartus Prime Pro Edition stand-alone IP generation. Added references to .ip file creation during Quartus Prime Pro Edition stand-alone IP generation. Updated IP Core Generation Output files list and diagram. Indicated distinctions between Quartus Prime Pro Edition and Quartus Prime Standard Edition features. Added Support for IP Core Encryption topic.
2016.05.03	16.0	<ul style="list-style-type: none"> Removed software beta status and revised feature set. Added topic on Safe State Machine encoding. Added Generating Dynamic Synthesis Reports. Corrected statement about Verilog Compilation Unit. Corrected typo in Modify Entity Name Assignments. Added description of Fitter Plan, Place and Route stages, reporting, and optimization. Added Per-Stage Compilation (Beta) Compilation Flow.
continued...		

Document Version	Quartus Prime Version	Changes
		<ul style="list-style-type: none">Added Platform Designer information.Added OpenCL and Signal Tap with routing preservation as unique Pro Edition features.Clarified limitations for multiple Logic Lock instances in the same region.Added topic on Safe State Machine encoding.Corrected statement about Verilog Compilation Unit.Corrected typo in Modify Entity Name Assignments.Clarified limitations for multiple Logic Lock instances in the same region.
2015.11.02	15.1	<ul style="list-style-type: none">First version of document.



D. Quartus Prime Pro Edition User Guides

Refer to the following user guides for comprehensive information on all phases of the Quartus Prime Pro Edition FPGA design flow.

Related Information

- [Quartus Prime Pro Edition User Guide: Getting Started](#)
Introduces the basic features, files, and design flow of the Quartus Prime Pro Edition software, including managing Quartus Prime Pro Edition projects and IP, initial design planning considerations, and project migration from previous software versions.
- [Quartus Prime Pro Edition User Guide: Platform Designer](#)
Describes creating and optimizing systems using Platform Designer, a system integration tool that simplifies integrating customized IP cores in your project. Platform Designer automatically generates interconnect logic to connect intellectual property (IP) functions and subsystems.
- [Quartus Prime Pro Edition User Guide: Design Recommendations](#)
Describes best design practices for designing FPGAs with the Quartus Prime Pro Edition software. HDL coding styles and synchronous design practices can significantly impact design performance. Following recommended HDL coding styles ensures that Quartus Prime Pro Edition synthesis optimally implements your design in hardware.
- [Quartus Prime Pro Edition User Guide: Design Compilation](#)
Describes set up, running, and optimization for all stages of the Quartus Prime Pro Edition Compiler. The Compiler synthesizes, places, and routes your design before generating a device programming file.
- [Quartus Prime Pro Edition User Guide: Design Optimization](#)
Describes Quartus Prime Pro Edition settings, tools, and techniques that you can use to achieve the highest design performance in Intel FPGAs. Techniques include optimizing the design netlist, addressing critical chains that limit retiming and timing closure, optimizing device resource usage, device floorplanning, and implementing engineering change orders (ECOs).
- [Quartus Prime Pro Edition User Guide: Programmer](#)
Describes operation of the Quartus Prime Pro Edition Programmer, which allows you to configure Intel FPGA devices, and program CPLD and configuration devices, via connection with an Intel FPGA download cable.
- [Quartus Prime Pro Edition User Guide: Block-Based Design](#)
Describes block-based design flows, also known as modular or hierarchical design flows. These advanced flows enable preservation of design blocks (or logic that comprises a hierarchical design instance) within a project, and reuse of design blocks in other projects.

- [Quartus Prime Pro Edition User Guide: Partial Reconfiguration](#)
Describes Partial Reconfiguration, an advanced design flow that allows you to reconfigure a portion of the FPGA dynamically, while the remaining FPGA design continues to function. Define multiple personas for a particular design region, without impacting operation in other areas.
- [Quartus Prime Pro Edition User Guide: Third-party Simulation](#)
Describes RTL- and gate-level design simulation support for third-party simulation tools by Aldec*, Cadence*, Siemens EDA, and Synopsys that allow you to verify design behavior before device programming. Includes simulator support, simulation flows, and simulating Intel FPGA IP.
- [Quartus Prime Pro Edition User Guide: Third-party Synthesis](#)
Describes support for optional synthesis of your design in third-party synthesis tools by Siemens EDA, and Synopsys. Includes design flow steps, generated file descriptions, and synthesis guidelines.
- [Quartus Prime Pro Edition User Guide: Third-party Logic Equivalence Checking Tools](#)
Describes support for optional logic equivalence checking (LEC) of your design in third-party LEC tools by OneSpin*.
- [Quartus Prime Pro Edition User Guide: Debug Tools](#)
Describes a portfolio of Quartus Prime Pro Edition in-system design debugging tools for real-time verification of your design. These tools provide visibility by routing (or “tapping”) signals in your design to debugging logic. These tools include System Console, Signal Tap logic analyzer, system debugging toolkits, In-System Memory Content Editor, and In-System Sources and Probes Editor.
- [Quartus Prime Pro Edition User Guide: Timing Analyzer](#)
Explains basic static timing analysis principals and use of the Quartus Prime Pro Edition Timing Analyzer, a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design using an industry-standard constraint, analysis, and reporting methodology.
- [Quartus Prime Pro Edition User Guide: Power Analysis and Optimization](#)
Describes the Quartus Prime Pro Edition Power Analysis tools that allow accurate estimation of device power consumption. Estimate the power consumption of a device to develop power budgets and design power supplies, voltage regulators, heat sink, and cooling systems.
- [Quartus Prime Pro Edition User Guide: Design Constraints](#)
Describes timing and logic constraints that influence how the Compiler implements your design, such as pin assignments, device options, logic options, and timing constraints. Use the Interface Planner to prototype interface implementations, plan clocks, and quickly define a legal device floorplan. Use the Pin Planner to visualize, modify, and validate all I/O assignments in a graphical representation of the target device.
- [Quartus Prime Pro Edition User Guide: PCB Design Tools](#)
Describes support for optional third-party PCB design tools by Siemens EDA and Cadence*. Also includes information about signal integrity analysis and simulations with HSPICE and IBIS Models.
- [Quartus Prime Pro Edition User Guide: Scripting](#)
Describes use of Tcl and command line scripts to control the Quartus Prime Pro Edition software and to perform a wide range of functions, such as managing projects, specifying constraints, running compilation or timing analysis, or generating reports.