
# GW1NZ series of FPGA Products

# **Datasheet**

**DS841-2.1E, 07/20/2023**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 01/23/2019 | 1.0E | Initial version published. |
| 02/12/2019 | 1.1E | Figures of part naming updated. |
| 04/03/2019 | 1.2E | ● I/O BANK view updated;<br>● The description of I3C bus and SPMI added; the precision of the on chip OSC added;<br>● Changed “Operating Temperature” to “Junction Temperature”. |
| 09/25/2019 | 1.3E | ● The note of “GW1NZ-1 I/Os support differential output, rather than differential input” added;<br>● Power supply ramp rate modified. |
| 11/06/2019 | 1.4E | Number of Max. I/O updated. |
| 01/06/2020 | 1.5E | ● The static current of ZV devices added;<br>● Low power description of user flash added. |
| 06/30/2020 | 1.6E | GW1NZ-1 FN32F added. |
| 12/12/2020 | 1.7E | The new device of GW1NZ-2 added. |
| 01/19/2021 | 1.7.1E | I/O Input/Output type updated. |
| 01/27/2021 | 1.7.2E | GW1NZ-2 QN48/QN48M added. |
| 02/26/2021 | 1.8E | GW1NZ-2 removed. |
| 11/26/2021 | 1.81E | I/O logic info., etc., optimized. |
| 11/18/2022 | 1.9E | ● Note about DC current limit added.<br>● Figure 3-1 GW1NZ-1 Architecture Overview updated.<br>● Table 3-1 Output I/O Types and Configuration Options of GW1NZ-1 updated.<br>● Table 4-3 Power Supply Ramp Rates updated.<br>● Table 4-5 POR Specification updated.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated.<br>● Table 4-12 I/O Operating Conditions Recommended updated.<br>● Section 3.6.4 Byte-enable removed.<br>● Description of configuration Flash added. |
| 02/27/2023 | 2.0E | ● Table 4-1 Absolute Max. Ratings updated.<br>● Table 4-22 User Flash Timing Parameters updated.<br>● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated.<br>● Information on Slew Rate removed.<br>● Description added to 3.7 User Flash (GW1NZ-1). |
| 07/20/2023 | 2.1E | ● Note about the default state of GPIO modified.<br>● The I/O logic output diagram and the I/O logic input diagram combined into Figure 3-8 I/O Logic Input and Output.<br>● 3.6.2 Memory Configuration Mode updated.<br>● Description of Flash resources updated.<br>● Table 4-9 Static Supply Current (LV Device) updated.<br>● Table 4-3 Power Supply Ramp Rates updated.<br>● Figure 5-3 Package Mark updated.<br>● Information on GW1NZ-2 added. |

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# 1 About This Guide

## 1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NZ series of FPGA products. It is designed to help you understand the GW1NZ series of FPGA products quickly and select and use devices appropriately.

## 1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG843, GW1NZ series of FPGA Products Package and Pinout
- UG842, GW1NZ-1 Pinout
- UG847, GW1NZ-2 Pinout

# 1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are shown in Table 1-1 below.

**Table 1-1 Abbreviations and Terminologies**

| Abbreviations and Terminology | Full Name |
|---|---|
| ALU | Arithmetic Logic Unit |
| BSRAM | Block Static Random Access Memory |
| CFU | Configurable Functional Unit |
| CLS | Configurable Logic Section |
| CRU | Configurable Routing Unit |
| CS16 | WLCSP16 |
| DCS | Dynamic Clock Selector |
| DP | True Dual Port 16K BSRAM |
| DQCE | Dynamic Quadrant Clock Enable |
| FN32 | QFN32 |
| FN32F | QFN32F |
| FPGA | Field Programmable Gate Array |
| GPIO | Gowin Programmable IO |
| IOB | Input/output Bank |
| LUT4 | Four-input Look-up Table |
| LUT5 | Five-input Look-up Table |
| LUT6 | Six-input Look-up Table |
| LUT7 | Seven-input Look-up Table |
| LUT8 | Eight-input Look-up Table |
| PLL | Phase Locked Loop |
| QN48 | QFN48 |
| REG | Register |
| SDP | Semi Dual Port 16K BSRAM |
| SP | Single Port 16K BSRAM |
| SPMI | System Power Management Interface |

# 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

# 2 General Description

The GW1NZ series of FPGA products are the first generation products in the LittleBee® family. They offer ultra-low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage. They can be widely used in communication, industry control, consumer, video control, etc.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NZ series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

## 2.1 Features

- Zero power consumption
  - 55nm embedded flash technology
  - LV: Supports 1.2V core voltage
  - ZV: Supports 0.9V core voltage. Please refer to Table 4-10 Static Supply Current (GW1NZ-1, ZV Version) for the lowest power consumption.
  - Supports dynamically turning on/off the clock.
  - User Flash dynamically turns on and off
- Power Management Module (GW1NZ-1)
  - SPMI: System power management interface
  - VCC and VCCM are independent in the device
- User Flash (GW1NZ-1)
  - NOR Flash
  - Can be turned on and off Dynamically
  - Capacity:64Kbits
  - Data Width: 32
  - 10,000 write cycles
  - Greater than ten years' data retention at +85 ℃
  - Supports page erasure: 2048 bytes per page
  - Duration: Max. 25ns
  - Electric current
    a). Read Operation: 2.19 mA/25 ns ($V_{CC}$) & 0.5 mA/25 ns ($V_{CCX}$) (MAX);

b). Write operation/erase operation: 12/12 mA (MAX)
- Quick page erasure/Write operation
- Clock frequency: 40MHz
- Write operation time: ≤16μs
- Page erasure time: ≤120 ms

- User Flash (GW1NZ-2)
  - 10,000 write cycles
  - Greater than 10 years' Data Retention at +85 ℃
  - Data Width: 32
  - Capacity: 96Kbits
  - Page Erase Capability: 2,048 bytes per page
  - Word Programming Time:⩽16 μs
  - Page Erasure Time:⩽120 ms
- Configuration Flash (GW1NZ-1)
  - NOR Flash
  - 10,000 write cycles
  - Greater than ten years' data retention at +85 ℃
- Configuration Flash (GW1NZ-2)
  - NOR Flash
  - 10,000 write cycles
  - Greater than ten years' data retention at +85 ℃
- Hard Core - MIPI D-PHY RX (GW1NZ-2)
  - Interfaces to MIPI CSI2 and DSI, RX devices
  - IO Bank6 supports MIPI D-PHY RX
  - MIPI transmission rate up to 2Gbps per lane
  - Supports up to 4 data lanes and one clock lane
- GPIOs support MIPI D-PHY RX/TX using MIPI IO mode（GW1NZ-2）
  - Interfaces to MIPI CSI2 and DSI, RX and TX devices
  - IO Bank0, IO Bank3, IO Bank4, and IO Bank5 support MIPI D-PHY TX, and the transmission rate can be up to 1.2 Gbps per lane
  - IO Bank2 supports MIPI D-PHY RX, and the transmission rate can be up to 1.2Gbps per lane
- Multiple I/O Standards
  - GW1NZ-1: LVCMOS33/25/18/15/12; LVTTL33; PCI; LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - GW1NZ-2：LVCMOS33/25/18/15/12；LVTTL33，SSTL33/25/18 I， SSTL33/25/18 II，SSTL15；HSTL18 I，HSTL18 II，HSTL15 I；PCI，LVDS25，RSDS，LVDS25E，BLVDSE，MLVDSE，LVPECLE，RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA, etc. drive options
  - Output drive strength option
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket
  - Hard I3C core supporting SDR mode
  - Support differential output, rather than differential input
- Abundant Slices
  - Four input LUT (LUT4)

  - Supports shifter register
  - Supports shadow SRAM
- Block SRAM with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clock
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, and DUAL BOOT

# 2.2 Product Resources

**Table 2-1 Product Resources**

| Device | GW1NZ-1 | GW1NZ-2 |
|---|---|---|
| LUT4 | 1,152 | 2304 |
| Register | 864 | 2016 |
| Shadow SRAM (bits) | 4K | 18432 |
| Block SRAM (bits) | 72K | 72K |
| PLLs | 1 | 1 |
| User Flash (bits) | 64K | 96K |
| Max. I/O | 48 | 125 |
| Core Voltage (LV) | 1.2V | - |
| Core Voltage (ZV) | 0.9V | 0.9V |

# 2.3 Package Information

**Table 2-2 Package Information and Max. User I/O**

| Package | Pitch (mm) | Size (mm) | GW1NZ-1 | GW1NZ-2 |
|---|---|---|---|---|
| FN32 | 0.4 | 4 x 4 | 25 | - |
| FN32F | 0.4 | 4 x 4 | 25 | - |
| CS16 | 0.4 | 1.8 x 1.8 | 11 | - |
| QN48 | 0.4 | 6 x 6 | 40 | TBD |
| CS100H | 0.4 | 4 x 4 | - | TBD |

**Note!**

- In this manual, abbreviations are employed to refer to the package types. See 5.1 Part Name.
- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. User I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one.

# 3 Architecture

## 3.1 Architecture Overview

**Figure 3-1 GW1NZ-1 Architecture Overview**

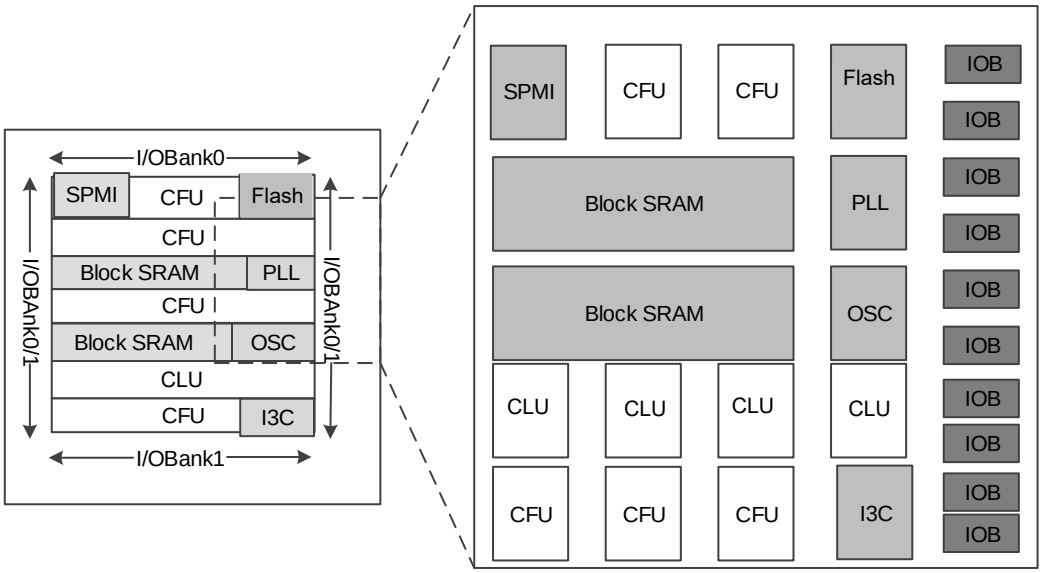


**Figure 3-2 GW1NZ-2 Architecture Overview**

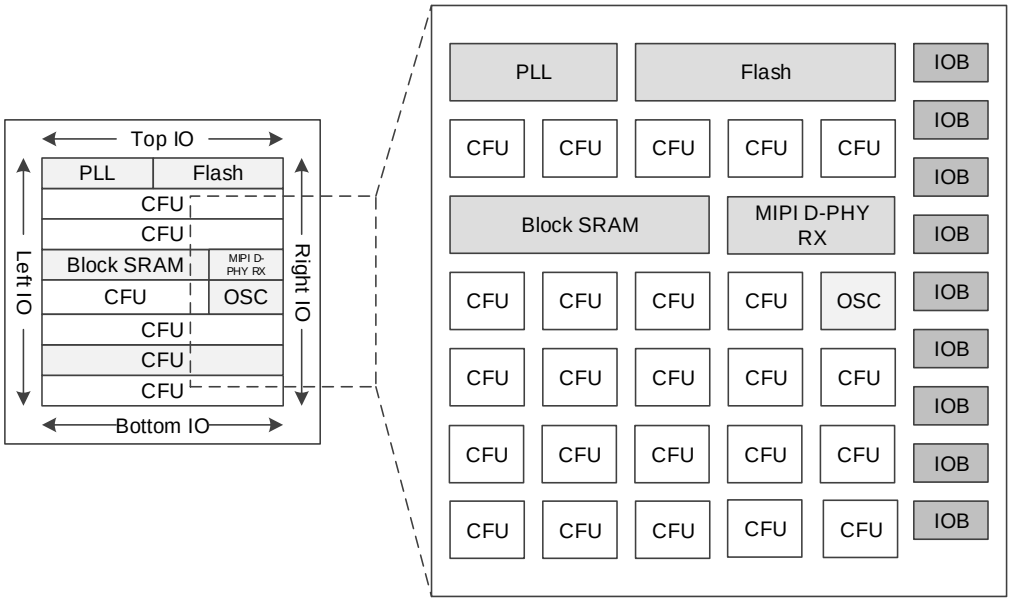



Figure 3-1 shows the GW1NZ devices architecture view. The core of the GW1NZ devices is the array of logic units surrounded by IO blocks. GW1NZ also provides BSRAM, PLL, on-chip oscillator, and Flash that supports Instant-on. SPMI and I3C are also embedded in the GW1NZ devices. See Table 2-1 for more detailed information on internal resources.

Configurable Function Unit (CFU) is the base cell for the array of the GW1NZ series of FPGA Products. These CFUs arrange in rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. See 3.2 Configurable Function Unit for further detailed information.

The I/O resources in the GW1NZ series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0 and Bank1. The I/O resources support multiple level standards and support basic mode, SDR mode, and generic DDR mode. See 3.3 IOB for further detailed information.

The BSRAM is embedded as a row in the GW1NZ series of FPGA products. In the FPGA array, each BSRAM occupies three columns of CFU. Each BSRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. See 3.6 Block SRAM (BSRAM) for further detailed information.

The GW1NZ series of FPGA products are embedded with Flash resources, including configuration Flash resources and user Flash resources. Configuration Flash resources are used for internal Flash programming, please refer to 3.13 Programming Configuration for detailed information. User Flash resources are used for user storage, See 3.7 User Flash (GW1NZ-1) and 3.8 User Flash (GW1NZ-2).

The GW1NZ-2 FPGA provides the hard MIPI D-PHY RX IP core, and its GPIOs support the soft MIPI D-PHY RX TX IP core. For further details, please refer to 3.9 MIPI D-PHY(GW1NZ-2).

GW1NZ provides one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. See 3.10 Clock for further detailed information.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NZ series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), programming options, etc. See 3.11 Long Wire (LW), 3.12 Global Set/Reset (GSR), and 3.13 Programming Configuration for further detailed information.

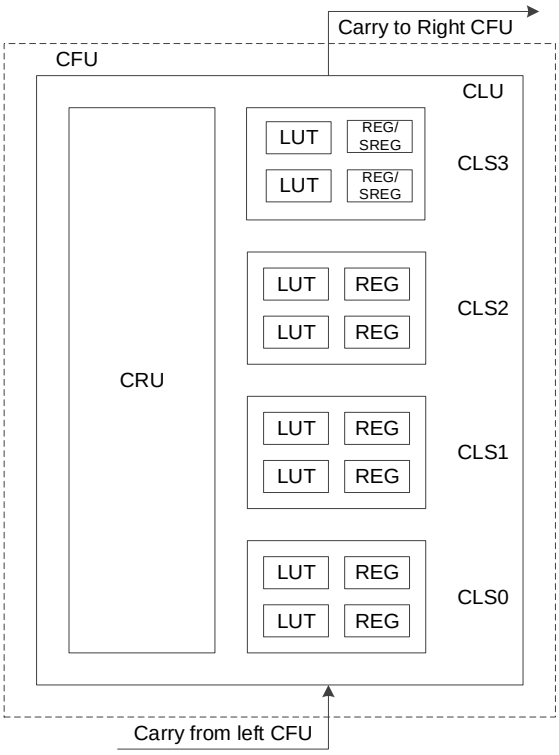
## 3.2 Configurable Function Unit

The configurable function unit and the configurable logic unit are the two basic units for the FPGA core of GOWINSEMI. As shown in Figure 3-3, each unit consists of four configurable logic sections and its configurable routing unit. Each of the three configurable logic sections contains two 4-input LUTs and two registers, and the other one only contains two 4-input LUTs.

Configurable logical sections in CLUs cannot be configured as SRAMs, but can be configured as basic logic, ALUs, and ROMs. The configurable logic sections in the CFU can be configured as basic logic, ALU, SRAM, and ROM depending on the applications. This section takes the CFU as an example to introduce the CFU and the CLU.

For more information about the CFU, please refer to *UG288, Gowin Configurable Function Unit (CFU) User Guide*.

**Figure 3-3 CFU View**




**Note!**

- SREGs require special patch support. Please contact Gowin's technical support or the local Office for this patch.
- Only the GW1N-2 device supports REGs in the CLS3 currently, and the CLK, CE, and SR of the CLS3 and the CLS2 are driven by the same source.

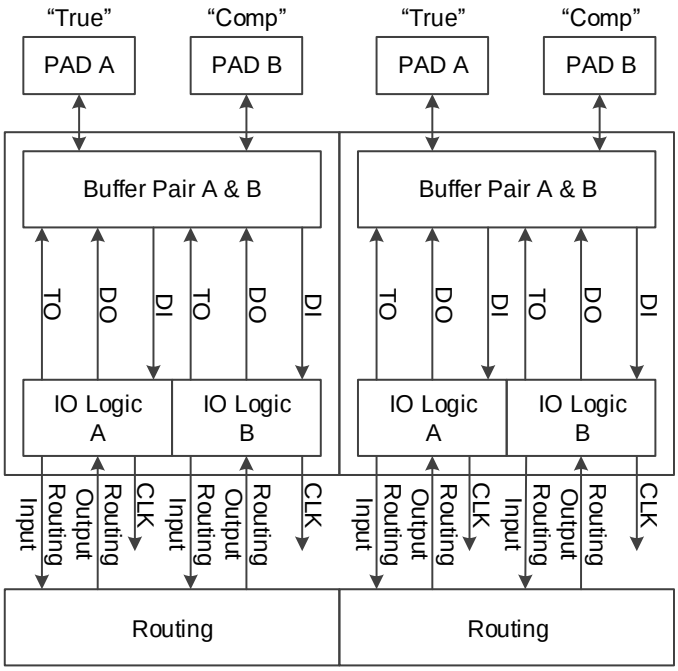
# 3.3 IOB

The IOB in the GW1NZ series of FPGA products includes an IO buffer pair, IO logic, and its routing resources. As shown in Figure 3-4, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as two single-ended signals[1].

**Note!**

The IOs of the GW1NZ-1 device do not support differential inputs.

**Figure 3-4 IOB Structure View**




IOB Features:

- $V_{CCIO}$ supplied with each bank
- Supports multiple levels: LVCMOS, PCI, LVTTL, etc.
- Input hysteresis option
- Output drive strength option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Hot Socket
- IO Logic supports basic mode, SRD mode, and generic DDR mode
- Hard I3C core supporting SDR mode(GW1NZ-1)

## 3.3.1 I/O Buffer

The GW1NZ-1 device includes Bank0 and Bank1, as shown in Figure 3-5. The GW1NZ-2 device includes six I/O Banks, as shown in Figure 3-6. Each Bank has its own $V_{CCIO}$. It can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V.

**Figure 3-5 I/O Bank Distribution of GW1NZ-1**

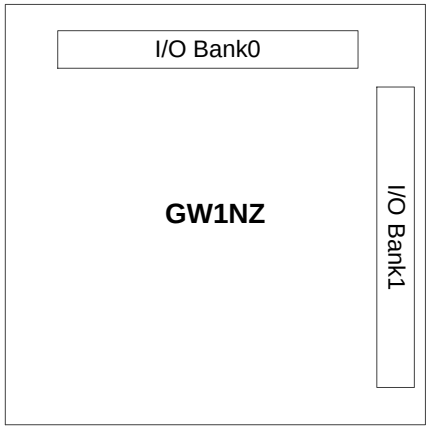
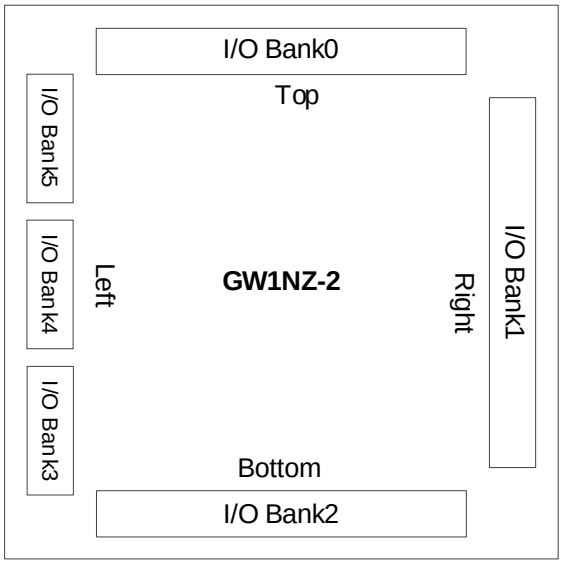


**Figure 3-6 I/O Bank Distribution of GW1NZ-2**




GW1NZ series FPGA products contain both LV and UV. LV devices support 1.2V core voltage to meet users' low power needs. ZV devices support 0.9V core voltage. Zero-power consumption can be available for ZV devices. $V_{CCIO}$ supplied with I/O Bank can be set as 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V according to requirements. $V_{CCX}$ supports 1.8V, 2.5V, and 3.3V power supplies.

**Note!**

During configuration, all GPIOs of the device have internally weak pull-ups. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of CONFIG-related I/Os varies depending on the configuration mode.

For the $V_{CCIO}$ requirements of different I/O standards, see Table 3-1 and Table 3-2.

**Table 3-1 Output I/O Types and Configuration Options of GW1NZ-1**

| I/O Type (Output) | Single-ended/Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Application |
|---|---|---|---|---|
| LVCMOS33/LVTTL33 | Single-ended | 3.3 | 8/24/16/12/4 | universal interface |
| LVCMOS25 | Single-ended | 2.5 | 8/16/12/4 | universal interface |
| LVCMOS18 | Single-ended | 1.8 | 8/12/4 | universal interface |
| LVCMOS15 | Single-ended | 1.5 | 8/4 | universal interface |
| LVCMOS12 | Single-ended | 1.2 | 8/4 | universal interface |
| PCI33 | Single-ended | 3.3 | 8/4 | PC and embedded system |
| LVCMOS33D | Differential | 3.3 | 8/24/16/12/4 | universal interface |
| LVCMOS25D | Differential | 2.5 | 8/16/12/4 | universal interface |
| LVCMOS18D | Differential | 1.8 | 8/12/4 | universal interface |
| LVCMOS15D | Differential | 1.5 | 8/4 | universal interface |
| LVCMOS12D | Differential | 1.2 | 8/4 | universal interface |

**Table 3-2 Input I/O Types and Configuration Options of GW1NZ-1**

| I/O Type (Input) | Single-ended/Differential | Bank $V_{CCIO}$(V) | HYSTERESIS | Need $V_{REF}$ |
|---|---|---|---|---|
| LVCMOS33/LVTTL33 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS25 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS18 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS15 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS12 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| PCI33 | Single-ended | 3.3 | Yes | No |
| LVCMOS33OD25 | Single-ended | 2.5 | Yes | No |
| LVCMOS33OD18 | Single-ended | 1.8 | Yes | No |
| LVCMOS33OD15 | Single-ended | 1.5 | Yes | No |
| LVCMOS25OD18 | Single-ended | 1.8 | Yes | No |
| LVCMOS25OD15 | Single-ended | 1.5 | Yes | No |
| LVCMOS18OD15 | Single-ended | 1.5 | Yes | No |
| LVCMOS15OD12 | Single-ended | 1.2 | Yes | No |
| LVCMOS25UD33 | Single-ended | 3.3 | Yes | No |
| LVCMOS18UD25 | Single-ended | 2.5 | Yes | No |
| LVCMOS18UD33 | Single-ended | 3.3 | Yes | No |
| LVCMOS15UD18 | Single-ended | 1.8 | Yes | No |
| LVCMOS15UD25 | Single-ended | 2.5 | Yes | No |
| LVCMOS15UD33 | Single-ended | 3.3 | Yes | No |
| LVCMOS12UD15 | Single-ended | 1.5 | Yes | No |
| LVCMOS12UD18 | Single-ended | 1.8 | Yes | No |
| LVCMOS12UD25 | Single-ended | 2.5 | Yes | No |
| LVCMOS12UD33 | Single-ended | 3.3 | Yes | No |

**Table 3-3 Output I/O Types and Configuration Options of GW1NZ-2**

| I/O Type (Output) | Single-ended/ Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| MIPI[1] | Differential (TLVDS) | 1.2 | 3.5 | Mobile industry processor interface |
| LVDS25 | Differential (TLVDS) | 2.5/3.3 | 3.5/2.5/2/1.25 | High-speed point-to-point data transmission |
| RSDS | Differential (TLVDS) | 2.5/3.3 | 2 | High-speed point-to-point data transmission |
| MINILVDS | Differential (TLVDS) | 2.5/3.3 | 2 | LCD timing driver interface and column driver interface |
| PPLVDS | Differential (TLVDS) | 2.5/3.3 | 1.25/2.0/2.5/3.5 | LCD row/column driver |

| I/O Type (Output) | Single-ended/ Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| LVDS25E | Differential | 2.5 | 8 | High-speed point-to-point data transmission |
| BLVDS25E | Differential | 2.5 | 16 | Multi-point high-speed data transmission |
| MLVDS25E | Differential | 2.5 | 16 | LCD timing driver interface and column driver interface |
| RSDS25E | Differential | 2.5 | 8 | High-speed point-to-point data transmission |
| LVPECL33E | Differential | 3.3 | 16 | High-speed data transmission |
| HSTL18D_I | Differential | 1.8 | 8 | memory interface |
| HSTL18D_II | Differential | 1.8 | 8 | memory interface |
| HSTL15D_I | Differential | 1.5 | 8 | memory interface |
| SSTL15D | Differential | 1.5 | 8 | memory interface |
| SSTL18D_I | Differential | 1.8 | 8 | memory interface |
| SSTL18D_II | Differential | 1.8 | 8 | memory interface |
| SSTL25D_I | Differential | 2.5 | 8 | memory interface |
| SSTL25D_II | Differential | 2.5 | 8 | memory interface |
| SSTL33D_I | Differential | 3.3 | 8 | memory interface |
| SSTL33D_II | Differential | 3.3 | 8 | memory interface |
| LVCMOS12D | Differential | 1.2 | 4/8 | universal interface |
| LVCMOS15D | Differential | 1.5 | 4/8 | universal interface |
| LVCMOS18D | Differential | 1.8 | 4/8/12 | universal interface |
| LVCMOS25D | Differential | 2.5 | 4/8/12/16 | universal interface |
| LVCMOS33D | Differential | 3.3 | 4/8/12/16/24 | universal interface |
| HSTL15_I | Single-ended | 1.5 | 8 | memory interface |
| HSTL18_I | Single-ended | 1.8 | 8 | memory interface |
| HSTL18_II | Single-ended | 1.8 | 8 | memory interface |
| SSTL15 | Single-ended | 1.5 | 8 | memory interface |
| SSTL18_I | Single-ended | 1.8 | 8 | memory interface |
| SSTL18_II | Single-ended | 1.8 | 8 | memory interface |
| SSTL25_I | Single-ended | 2.5 | 8 | memory interface |
| SSTL25_II | Single-ended | 2.5 | 8 | memory interface |
| SSTL33_I | Single-ended | 3.3 | 8 | memory interface |
| SSTL33_II | Single-ended | 3.3 | 8 | memory interface |
| LVCMOS12 | Single-ended | 1.2 | 4/8 | universal interface |
| LVCMOS15 | Single-ended | 1.5 | 4/8 | universal interface |
| LVCMOS18 | Single-ended | 1.8 | 4/8/12 | universal interface |

| I/O Type (Output) | Single-ended/ Differential | Bank $V_{CCIO}$ (V) | Drive Strength (mA) | Typical Application |
|---|---|---|---|---|
| LVCMOS25 | Single-ended | 2.5 | 4/8/12/16 | universal interface |
| LVCMOS33/ LVTTL33 | Single-ended | 3.3 | 4/8/12/16/24 | universal interface |
| PCI33 | Single-ended | 3.3 | 4/8 | PC and embedded system |

**Note!**

[1] Bank0/Bank3/Bank4/Bank5 of the GW1NZ-2 device support MIPI output by using MIPI IO mode.

**Table 3-4 Input I/O Types and Configuration Options of GW1NZ-2**

| I/O Type (Input) | Single-ended/ Differential | Bank $V_{CCIO}$ (V) | HYSTERESIS | Need $V_{REF}$ |
|---|---|---|---|---|
| MIPI[1] | Differential (TLVDS) | 1.2 | No | No |
| LVDS25 | Differential (TLVDS) | 2.5/3.3 | No | No |
| RSDS | Differential (TLVDS) | 2.5/3.3 | No | No |
| MINILVDS | Differential (TLVDS) | 2.5/3.3 | No | No |
| PPLVDS | Differential (TLVDS) | 2.5/3.3 | No | No |
| LVDS25E | Differential | 2.5/3.3 | No | No |
| BLVDS25E | Differential | 2.5/3.3 | No | No |
| MLVDS25E | Differential | 2.5/3.3 | No | No |
| RSDS25E | Differential | 2.5/3.3 | No | No |
| LVPECL33E | Differential | 3.3 | No | No |
| HSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| HSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| HSTL15D_I | Differential | 1.5/1.8/2.5/3.3 | No | No |
| SSTL15D | Differential | 1.5/1.8/2.5/3.3 | No | No |
| SSTL18D_I | Differential | 1.8/2.5/3.3 | No | No |
| SSTL18D_II | Differential | 1.8/2.5/3.3 | No | No |
| SSTL25D_I | Differential | 2.5/3.3 | No | No |
| SSTL25D_II | Differential | 2.5/3.3 | No | No |
| SSTL33D_I | Differential | 3.3 | No | No |
| SSTL33D_II | Differential | 3.3 | No | No |
| LVCMOS12D | Differential | 1.2/1.5/1.8/2.5/3.3 | No | No |
| LVCMOS15D | Differential | 1.5/1.8/2.5/3.3 | No | No |
| LVCMOS18D | Differential | 1.8/2.5/3.3 | No | No |
| LVCMOS25D | Differential | 2.5/3.3 | No | No |
| LVCMOS33D | Differential | 3.3 | No | No |
| HSTL15_I | Single-ended | 1.5 or 1.5/1.8/2.5/3.3[2] | No | Yes |
| HSTL18_I | Single-ended | 1.8 or 1.8/2.5/3.3[3] | No | Yes |
| HSTL18_II | Single-ended | 1.8 or 1.8/2.5/3.3[3] | No | Yes |
| SSTL15 | Single-ended | 1.5 or 1.5/1.8/2.5/3.3[2] | No | Yes |

| I/O Type (Input) | Single-ended/ Differential | Bank $V_{CCIO}$ (V) | HYSTERESIS | Need $V_{REF}$ |
|---|---|---|---|---|
| SSTL18_I | Single-ended | 1.8 or 1.8/2.5/3.3[3] | No | Yes |
| SSTL18_II | Single-ended | 1.8 or 1.8/2.5/3.3[3] | No | Yes |
| SSTL25_I | Single-ended | 2.5 or 2.5/3.3[4] | No | Yes |
| SSTL25_II | Single-ended | 2.5 or 2.5/3.3[4] | No | Yes |
| SSTL33_I | Single-ended | 3.3 | No | Yes |
| SSTL33_II | Single-ended | 3.3 | No | Yes |
| LVCMOS12 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS15 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS18 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS25 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| LVCMOS33/ LVTTL33 | Single-ended | 1.2/1.5/1.8/2.5/3.3 | Yes | No |
| PCI33 | Single-ended | 3.3 | Yes | No |
| LVCMOS33OD25 | Single-ended | 2.5 | No | No |
| LVCMOS33OD18 | Single-ended | 1.8 | No | No |
| LVCMOS33OD15 | Single-ended | 1.5 | No | No |
| LVCMOS25OD18 | Single-ended | 1.8 | No | No |
| LVCMOS25OD15 | Single-ended | 1.5 | No | No |
| LVCMOS18OD15 | Single-ended | 1.5 | No | No |
| LVCMOS15OD12 | Single-ended | 1.2 | No | No |
| LVCMOS25UD33 | Single-ended | 3.3 | No | No |
| LVCMOS18UD25 | Single-ended | 2.5 | No | No |
| LVCMOS18UD33 | Single-ended | 3.3 | No | No |
| LVCMOS15UD18 | Single-ended | 1.8 | No | No |
| LVCMOS15UD25 | Single-ended | 2.5 | No | No |
| LVCMOS15UD33 | Single-ended | 3.3 | No | No |
| LVCMOS12UD15 | Single-ended | 1.5 | No | No |
| LVCMOS12UD18 | Single-ended | 1.8 | No | No |
| LVCMOS12UD25 | Single-ended | 2.5 | No | No |
| LVCMOS12UD33 | Single-ended | 3.3 | No | No |

**Note!**

- [1] GW1NZ-2 Bank6 (Hard core) and GW1NZ-2 support MIPI I/O input.
- [2] When $V_{REF}$ is INTERNAL, the $V_{CCIO}$ of this I/O type is 1.5V; when $V_{REF}$ is VREF1_LOAD, the $V_{CCIO}$ of this I/O type is 1.5 V/1.8 V/2.5 V/3.3 V.
- [3] When $V_{REF}$ is INTERNAL, the $V_{CCIO}$ of this I/O type is 1.8 V; when $V_{REF}$ is VREF1_LOAD, the $V_{CCIO}$ of this I/O type is 1.8 V /2.5 V /3.3 V.
- [4] When $V_{REF}$ is INTERNAL, the $V_{CCIO}$ of this I/O type is 2.5 V; when $V_{REF}$ is VREF1_LOAD, the $V_{CCIO}$ of this I/O type is 2.5 V /3.3 V.

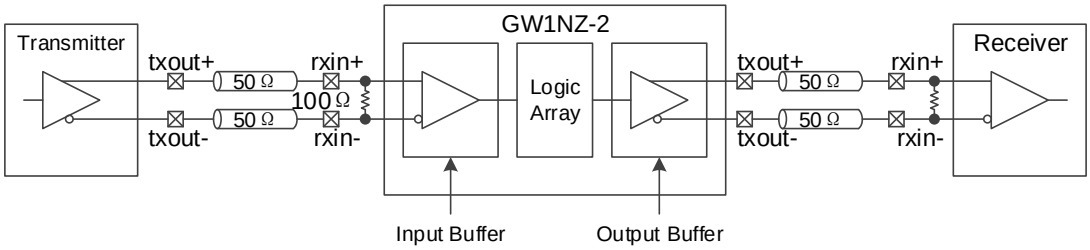
### 3.3.2 True LVDS Design

The GW1NZ-2 device supports true LVDS output as well as LVDS25E, MLVDS25E, BLVDS25E, etc.

For more detailed information about true LVDS, please refer to *UG844, GW1NZ-2 Pinout*, *UG847, GW1NZ-2 Pinout.*

True LVDS input I/O needs a 100Ω termination resistor. See Figure 3-7 for the true LVDS design. Bank2 of the GW1NZ-2 device supports a programmable on-chip 100 ohm input differential termination resistor, see *UG289, Gowin Programable IO User Guide*.

**Figure 3-7 True LVDS Design**




For more information about termination for LVDS25E, MLVDS25E, and BLVDS25E, please refer to *UG289, Gowin Programable IO User Guide*.

## 3.3.3 I/O Logic

Figure 3-8 shows the I/O logic input and output of the GW1NZ series

of FPGA products.

**Figure 3-8 I/O Logic Input and Output**

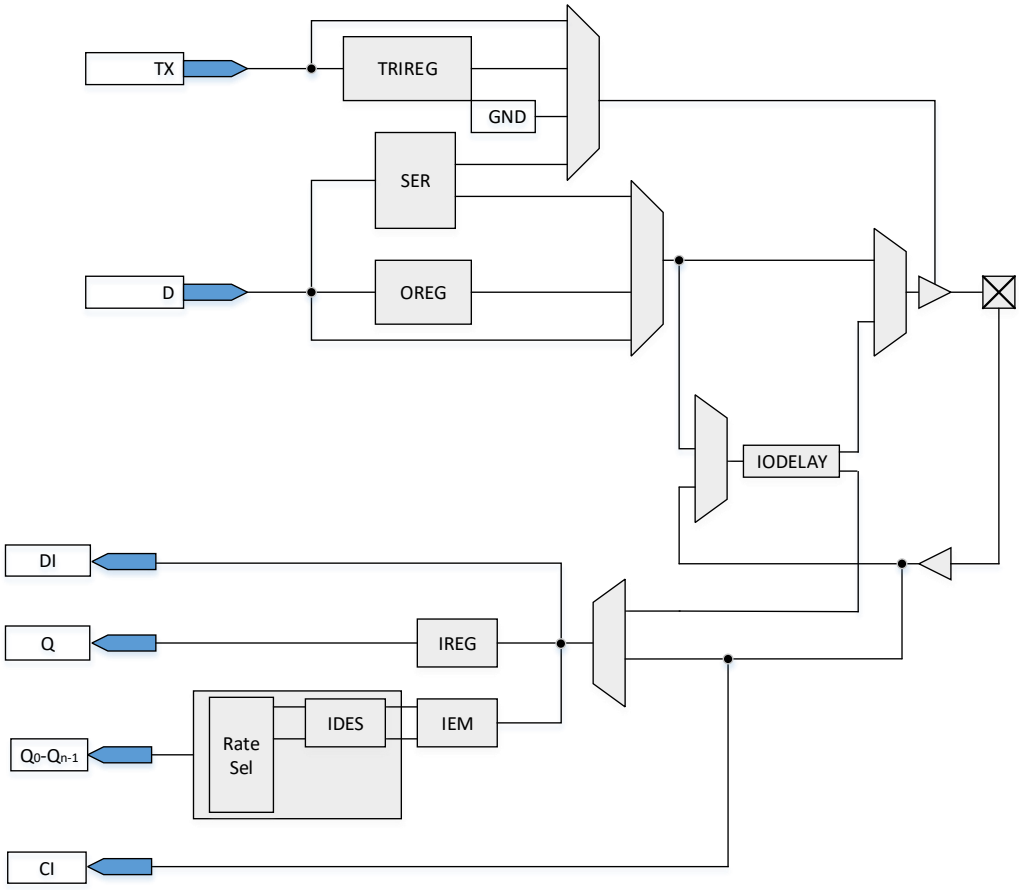



**Table 3-5 Port Description**

| Ports | I/O | Description |
|---|---|---|
| CI[1] | Input | GCLK input signal.<br>For the number of GCLK input signals, please refer to *UG842, GW1NZ-1 Pinout, UG847, GW1NZ-2 Pinout* . |
| DI | Input | IO port low-speed input signal, entering into Fabric directly. |
| Q | Output | IREG output signal in SDR module. |
| $Q_0$-$Q_{n-1}$ | Output | IDES output signal in DDR module. |

**Note!**

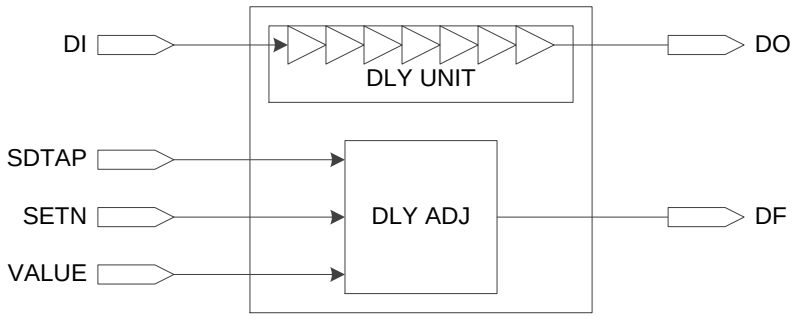
When CI is used as GCLK input, DI, Q, and $Q_0$-$Q_{n-1}$ cannot be used as I/O input and output.

A description of the I/O logic modules of the GW1NZ series of FPGA products is presented below:

## IODELAY

See Figure 3-9 for an overview of the IODELAY. Each I/O of the GW1NZ series of FPGA products has an IODELAY cell. A total of 128(0~127) steps of delay are provided, with one step of delay time being about 30 ps.

**Figure 3-9 IODELAY**



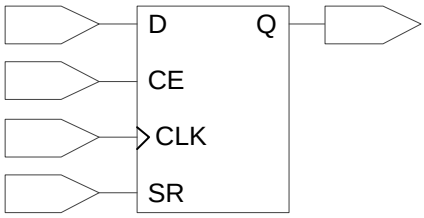

There are two ways to control the delay cell:

- Static control
- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

## I/O Register

See Figure Figure 3-10 for the I/O register in the GW1NZ series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

**Figure 3-10 Register Structure in I/O Logic**



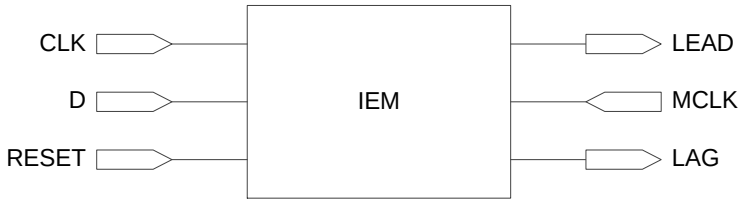

**Note!**

- CE can be programmed as either active low (0: enable)or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET or RESET or disabled.
- The register can be programmed as a register or latch.

## IEM

IEM is for sampling clock edge and is used in the generic DDR mode, as shown in Figure 3-11.

**Figure 3-11 IEM Structure**



#### De-serializer DES and Clock Domain Transfer

The GW1NZ series of FPGA products provide a simple DES for each input I/O to support advanced I/O protocols.

#### Serializer SER

The GW1NZ series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

### 3.3.4 I/O Logic Modes

The I/O Logic in the GW1NZ series of FPGA products supports several modes. In each operation, the I/O can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

The GW1NZ-1 pins IOR6 (A, B, C….J) do not support IO logic.

For further information about I/O logic modes, please refer to *UG289, Gowin Programmable IO (GPIO) User Guide*.

## 3.4 I3C Bus (GW1NZ-1)

### 3.4.1 Overview

The GW1NZ series of FPGA products include a hard I3C bus controller IP core that supports SDR mode. The I3C controller is backwards compatible with I2C features low power, and is high speed and extensible. The I3C bus is compliant with MIPI I3C protocol, adopts register interfaces, and supports operation modes of I3C SDR Master and I3C SDR Slave.

#### I3C SDR Master

- Compliance with MIPI I3C protocol;
- Supports I3C address arbitration detection;
- Supports Single Data Rate (SDR) mode;
- The data rate can be up to 12.5Mbps;
- Start / Stop / Repeated Start / Acknowledge generation;
- Start / Stop / Repeated Start detection;
- Support dynamically allocating addresses via SETDASA or ENTDAA;
- Supports Receive/Send data;
- Supports In-band Interrupts;
- Supports Hot-Join;
- Supports dynamically allocating address when hot-join;
- Supports CCC's command;
- Supports dynamic adjusting SCL frequency;
- Compatible with I2C Slave;
- Adopts register interfaces.

#### I3C SDR Slave

- Compliance with MIPI I3C protocol;
- Start / Acknowledge generation;
- Start / Stop / Repeated Start detection;
- Support dynamically allocating addresses via SETDASA or ENTDAA;
- Receive/Send data;

- Send an IBI or hot-join request. If more than one slaves send the IBI or hot-join requests, the min. address obtains the arbitration;
- Static address of Slave configuration;
- Adopts register interfaces.

### 3.4.2 Port Signal

For more information about I3C port signals, working principle, timing, and examples, please refer to *IPUG508-1.2_Gowin I3C SDR IP User Guide*.

**Table 3-6 I3C Port Signals**

| Port Name | I/O | Description |
|---|---|---|
| AAC | Input | The setting to clear ACK response, single pulse signal |
| AAO | output | Output ACK signal |
| AAS | Input | Set ACK response, single pulse signal |
| ACC | Input | The setting to clear continuous operation mode, single pulse signal |
| ACKHS | Input | Set ACK high-level time |
| ACKLS | Input | Set ACK low-level time |
| ACO | output | Continuous operation mode output |
| ACS | Input | Set continuous operation mode, single pulse signal |
| ADDRS | Input | Set slave address |
| CE | Input | Clock enable signal |
| CLK | Input | Clock input |
| CMC | Input | Clear the current master role, single pulse signal |
| CMO | output | Output the flag of the current master role |
| CMS | Input | Set the current Master role, single pulse signal |
| DI[7:0] | Input | Data input |
| DO[7:0] | output | Data output |
| DOBUF[7:0] | output | Buffer data output |
| LGYC | Input | Clear the setting of I2C as the current communication object, single pulse signal |
| LGYO | output | The output of I2C as the current communication object |
| LGYS | Input | Set I2C as the current communication object, single pulse signal |
| PARITYERROR | output | Parity error signal |
| RECVDHS | Input | Set high-level time of receiving data |
| RECVDLS | Input | Set low-level time of receiving data |
| RESET | Input | Asynchronous reset, active high |
| SCLI | Input | I3C serial clock input |
| SCLO | output | I3C serial clock line |
| SCLOEN | output | I3C serial clock output enable |
| SCLPULLO | output | I3C serial clock pull-up output |

| Port Name | I/O | Description |
|---|---|---|
| SCLPULLOEN | output | I3C serial clock pull-up output enable |
| SDAI | Input | I3C serial data input |
| SDAO | output | I3C serial data output |
| SDAOEN | output | I3C serial data output enable |
| SDAPULLO | output | I3C serial data pull-up output |
| SDAPULLOEN | output | I3C serial data pull-up output enable |
| SENDAHS | Input | Set high-level time of sending address |
| SENDALS | Input | Set low-level time of sending address |
| SENDDHS | Input | Set high-level time of sending data |
| SENDDLS | Input | Set low-level time of sending data |
| SIC | Input | Signal of clearing interrupt flag |
| SIO | output | Signal of output signal interrupt |
| STRTC | Input | Setting of clearing the START command, single pulse signal |
| STRTO | output | Output START command |
| STRTS | Input | Set START command, single pulse signal |
| STATE | output | Output internal state |
| STRTHDS | Input | Set the holding time of the START command |
| STOPC | Input | Clear the STOP command setting, single pulse signal |
| STOPO | output | Output the STOP command |
| STOPS | Input | Set the STOP command, single pulse signal |
| STOPSUS | Input | Set the setting time of the STOP command |
| STOPHDS | Input | Set the holding time of the STOP command |

# 3.5 SPMI (GW1NZ-1)

## 3.5.1 Overview

The GW1NZ-1 product provides an SPMI module as well as an SPMI controller IP. As a Master, it supports controlling external Slave devices through the SPMI interface for power management. As a Slave, it supports FPGA power management.

The GW1NZ-1 device supports controlling the main power supply in the following way:

- You can turn off the main power supply by sending the shutdown command from the Master. And the main power supply of the FPGA can be restored by sending the reset/sleep/wakeup command from the Master, or by a low pulse of the SPMI_EN signal.

**Note!**

For more information on operation modes, communication modes, commands, timing, etc, please refer to *IPUG529, Gowin SPMI User Guide*.

### 3.5.2 Port Signal

**Table 3-7 SPMI Port Signal**

| Name | I/O | Description |
|---|---|---|
| SPMI_EN | input | SPMI enable signal |
| SPMI_CLK | input | System clock signal |
| SPMI_SCLK | inout | SPMI serial clock signal |
| SPMI_SDATA | inout | SPMI serial data signal |

## 3.6 Block SRAM (BSRAM)

### 3.6.1 Introduction

GW1NZ series FPGA products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each BSRAM occupies three columns of CFU in the FPGA array. Each BSRAM has 18,432 bits (18Kbits). There are five operation modes: Single Port, Dual Port, Semi-dual Port, ROM, and FIFO.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 170MHz at max (typical, Read-before-write is 100MHz)
- Single Port
- Dual Port
- Semi-dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Byte Enable operation for double-byte and above data
- Normal read and write mode
- Read-before-write mode
- Write-through Mode

### 3.6.2 Memory Configuration Mode

The BSRAM mode in the GW1NZ series of FPGA products supports different data bus widths. See Table 3-8.

**Table 3-8 Memory Size Configuration**

| Single Port Mode | Dual Port Mode[1] | Semi-Dual Port Mode |
|---|---|---|
| 16K x 1 | 16K x 1 | 16K x 1 |
| 8K x 2 | 8K x 2 | 8K x 2 |
| 4K x 4 | 4K x 4 | 4K x 4 |
| 2K x 8 | 2K x 8 | 2K x 8 |

| | | |
|---|---|---|
| 1K x 16 | 1K x 16 | 1K x 16 |
| 512 x 32 | - | 512 x 32 |
| 2K x 9 | 2K x 9 | 2K x 9 |
| 1K x 18 | 1K x 18 | 1K x 18 |
| 512 x 36 | - | 512 x 36 |

**Note!**

[1] The GW1NZ-1 device does not support Dual Port Mode.

### Single Port Mode

The single port mode can support 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In the single port mode, BSRAM can write to or read from one port at one clock edge. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Dual Port Mode

The dual port mode can support 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode). The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Dual Port BSRAM.

For further information about Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Semi-Dual Port Mode

The semi-dual port mode can support 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). The semi-dual port mode supports reading and writing at the same time on different ports, but it is not possible to write and read to the same port at the same time. It only supports writing on Port A and reading on Port B.

**Note!**

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address for all modes of the Dual Port BSRAM.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

### Read Only

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

## 3.6.3 Mixed Data Bus Width Configuration

BSRAM in the GW1NZ series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the available configuration options, please see Table 3-9 and Table 3-10 below.

**Table 3-9 Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 2K x 9 | 1K x 18 |
| 16K x 1 | * | * | * | * | * | | |
| 8K x 2 | * | * | * | * | * | | |
| 4K x 4 | * | * | * | * | * | | |
| 2K x 8 | * | * | * | * | * | | |
| 1K x 16 | * | * | * | * | * | | |
| 2K x 9 | | | | | | * | * |
| 1K x 18 | | | | | | * | * |

**Note!**

"*" denotes the modes supported.

**Table 3-10 Semi Dual Port Mixed Read/Write Data Width Configuration**

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512 x 32 | 2K x 9 | 1K x 18 | 512 x 36 |
| 16K x 1 | * | * | * | * | * | * | | | |
| 8K x 2 | * | * | * | * | * | * | | | |
| 4K x 4 | * | * | * | * | * | * | | | |
| 2K x 8 | * | * | * | * | * | * | | | |
| 1K x 16 | * | * | * | * | * | * | | | |
| 512 x 32 | * | * | * | * | * | * | | | |
| 2K x 9 | | | | | | | * | * | * |
| 1K x 18 | | | | | | | * | * | * |

**Note!**

"*" denotes the modes supported.

## 3.6.4 Byte-enable

The BSRAM in the GW1NZ series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the BSRAM write operation.

**Note!**

For the GW1NZ series, only the GW1NZ-2 device supports the byte-enable function.

## 3.6.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

## 3.6.6 Synchronous Operation

- All the input registers of the BSRAM support synchronous writes.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypassable.

## 3.6.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

## 3.6.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

### Read Mode

Read data from the BSRAM via output registers or without using the registers.

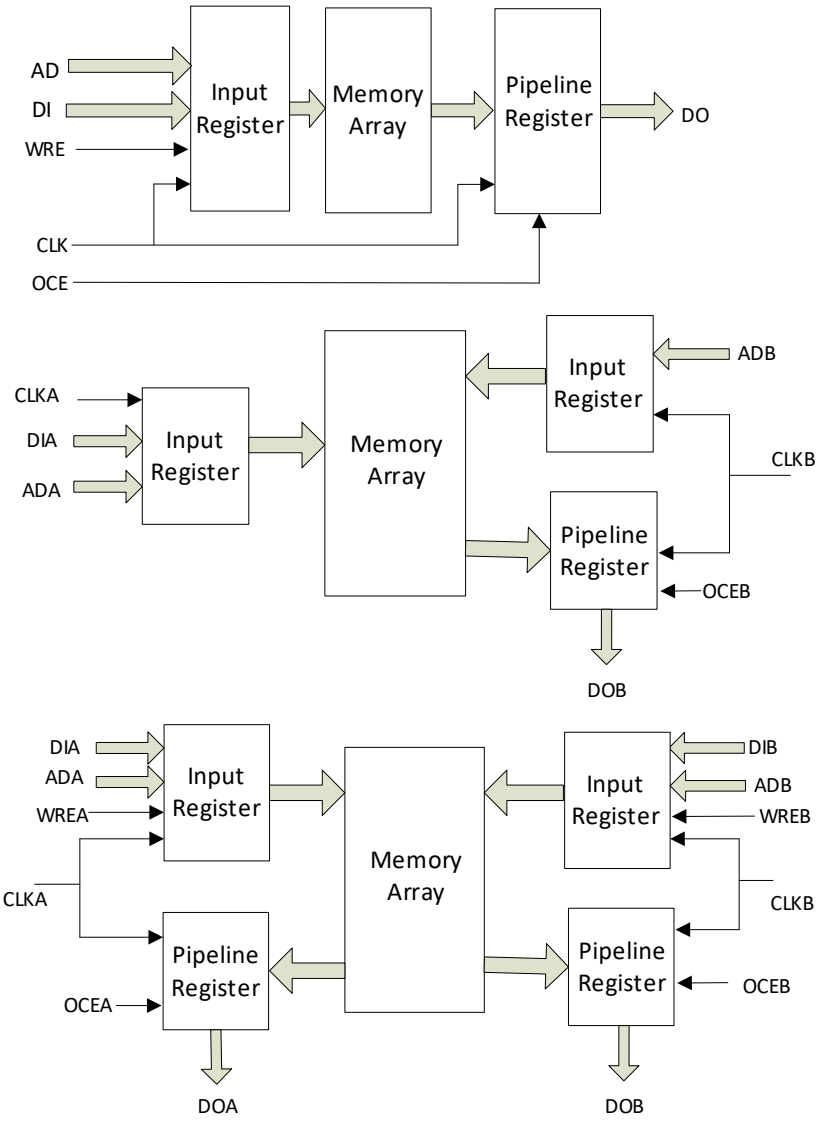
#### PIPELINE MODE

While writing in the BSRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

#### BYPASS MODE

The output register is not used. The data is kept in the output of the memory array.

**Figure 3-12 Pipeline Mode in Single Port, Dual Port, and Semi Dual Port**




## Write Mode

#### NORMAL WRITE MODE

In this mode, when the user writes data to one port, the output data of this port does not change. The data written in will not appear at the read port.

#### WRITE-THROUGH MODE

In this mode, when the user writes data to one port, the data written in will also appear at the output of this port.

#### READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

## 3.6.9 Clock Operations

Table 3-11 lists the clock operations in different BSRAM modes:

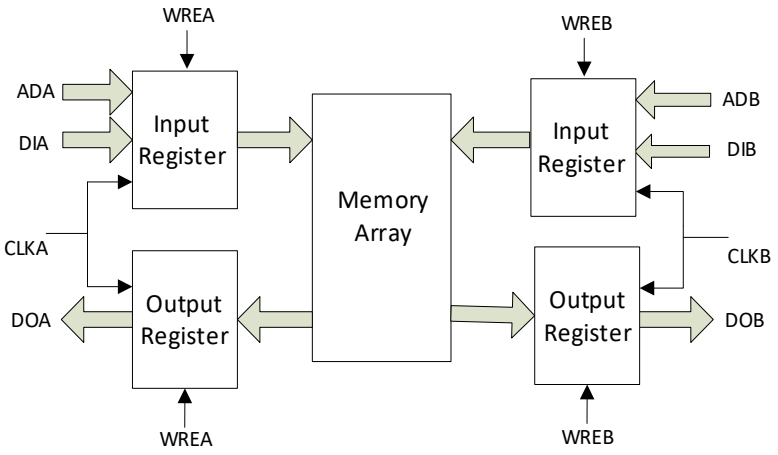
**Table 3-11 Clock Operations in Different BSRAM Modes**

| Clock Operations | Dual Port Mode | Semi-Dual Port Mode | Single Port Mode |
|---|---|---|---|
| Independent Clock Mode | Yes | No | No |
| Read/Write Clock Mode | Yes | Yes | No |
| Single Port Clock Mode | No | No | Yes |

### Independent Clock Mode

Figure 3-13 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

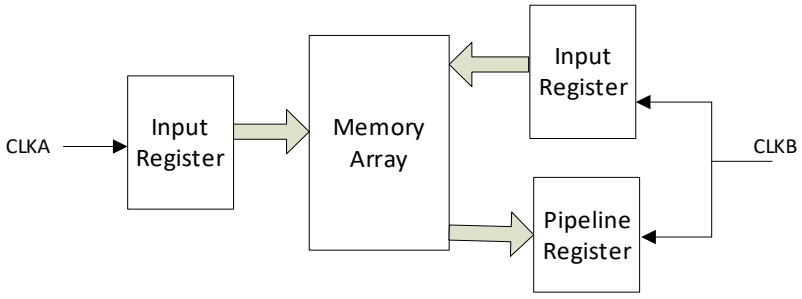
**Figure 3-13 Independent Clock Mode**




### Read/Write Clock Operation

Figure 3-14 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

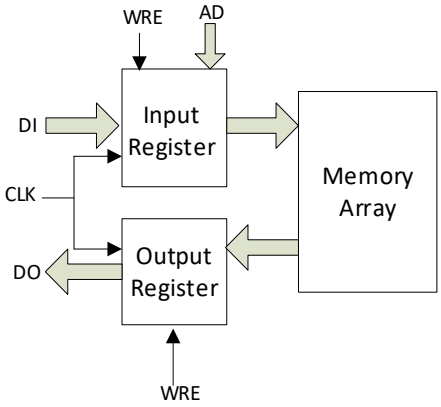
**Figure 3-14 Read/Write Clock Mode**



**Single Port Clock Mode**

Figure 3-15 shows the clock operation in single port mode.

**Figure 3-15 Single Port Clock Mode**




# 3.7 User Flash (GW1NZ-1)

## 3.7.1 Introduction

GW1NZ-1 offers User Flash, the features are shown below:

- NOR Flash
- 10,000 write cycles
- Capacity: 64K bits
- Greater than ten years' data retention at +85 ℃
- Supports page erasure: 2,048 bytes per page
- Quick page erasure/Write operation
- Clock frequency: 40MHz
- Write operation time: ≤16μs
- Page erasure time: ≤120 ms
- Electric current
  - Read Operation: 2.19 mA/25 ns ($V_{CC}$) & 0.5 mA/25 ns ($V_{CCX}$) (MAX).
  - Write operation/erase operation: 12/12 mA(MAX)

## 3.7.2 Mode

The User Flash in the GW1NZ series of FPGA products contains two modes: Normal mode and sleep mode.

- Normal mode: User flash is turned on by default. Users can perform erase/write/read operations after the device is powered on. It cannot be turned off.
- Sleep mode: User flash is turned off by default to save power. Users can turn on/turn off the user flash mode using the “Sleep” port. When the user flash is turned on, it’s the same as the normal mode user flash, and users can perform erase/write/read operations.

The GW1NZ LV/ZV devices with different speeds offer different user flash modes. For further detailed information, please refer to Table 3-12.

**Table 3-12 User Flash Modes**

| Mode | Default Status | Turn on/Turn off | Device Version | Speed Grade |
|---|---|---|---|---|
| Normal mode | On | No | LV | C6/I5 |
| | | | | C5/I4 |
| | | | ZV | C5/I4 |
| Sleep mode | Off | Yes | ZV | I2 |
| | | | | I3 |

For further information about the user Flash in GW1NZ-1, please refer to UG295, Gowin User Flash User Guide. For the correspondence between user Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

# 3.8 User Flash (GW1NZ-2)

## 3.8.1 Introduction

The GW1NZ-2 device offers User Flash. The capacity of the User Flash in the GW1NZ-2 device is 96Kbits. The user Flash memory is composed of row memory units and column memory units. One row memory unit is composed of 64 column memory units. The capacity of one column memory unit is 32 bits, and the capacity of one row memory unit is 64*32=2048 bits. Page erase is supported, and the capacity of one page is 2048 bytes, i.e., one page includes 8 rows. The key features are shown below:

- NOR Flash
- 10,000 write cycles
- Greater than 10 years of data retention at +85 ℃
- Data Width: 32
- Capacity: 48 rows x 64 columns x 32 = 96Kbits
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Clock frequency: 40 MHz
- Word Programming Time:≤16 μs
- Page Erasure Time:≤120 ms
- Electric current
  - Read current/duration:2.19 mA/25 ns ($V_{CC}$) & 0.5 mA/25 ns ($V_{CCX}$) (MAX)
  - Program/Erase operation: 12/12 mA(MAX)

For more information about the user Flash in the GW1NZ-2 device, please refer to *UG295, Gowin User Flash User Guide*. For the correspondence between user Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295.

# 3.9 MIPI D-PHY(GW1NZ-2)

## 3.9.1 Hard Core - MIPI D-PHY RX(GW1NZ-2)

The GW1NZ-2 device provides the hard MIPI D-PHY RX IP core. This

IP applies to the display serial interface (DSI) and the camera serial interface (CSI), which are designed to receive and send image data or video data. MIPI D-PHY provides a physical layer definition.

The key features are as follows:

- High-Speed RX at up to 8 Gbps per quad
- Supports up to 4 data lanes and one clock lane per PHY
- Bidirectional Low-power (LP) mode at up to 10mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers
- Available on Bank6

For further detailed information, please refer to *IPUG778, Gowin GW1N-2 Hardened MIPI D-PHY RX User Guide*.

### 3.9.2 GPIOs Support MIPI D-PHY RX/TX by Using MIPI IO mode(GW1NZ-2)

The GPIOs of the GW1NZ-2 device also support MIPI D-PHY RX/TX by using MIPI IO mode. This applies to the display serial interface (DSI) and the camera serial interface (CSI), which are designed to receive and send image data or video data. MIPI D-PHY provides a physical layer definition.

The key features are as follows:

- Compliant to MIPI Alliance Standard for D-PHY Specification, version 1.2;
- Interfaces to MIPI CSI2 and DSI, RX and TX devices;
- Supports unidirectional High-speed (HS) mode;
- Supports bidirectional Low-power operation mode;
- Deserializes serial high-speed data into byte data packets;
- Supports MIPI D-PHY RX 1:8 mode and 1:16 mode;
- Supports IO Types of ELVDS, TLVDS, and MIPI IO;
- IO Bank0, IO Bank3, IO Bank4, and IO Bank5 support MIPI D-PHY TX, and the transmission rate can be up to 1.2 Gbps;
- IO Bank2 supports MIPI D-PHY RX, and the transmission rate can be up to 1.2Gbps;
- Supports up to 4 data lanes and one clock lane.

For further detailed information, please refer to *IPUG112, Gowin MIPI D-PHY RX TX user guide*.

## 3.10 Clock

For further detailed information, please refer to UG286, Gowin Clock User Guide.

### 3.10.1 Global Clock

The GCLK resources are distributed in the device as quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources

to achieve better timing.

### 3.10.2 PLL

PLL (Phase-locked Loop) is one kind of feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

### 3.10.3 HCLK

HCLK is the high-speed clock in the GW1NZ series of FPGA products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure Figure 3-16. HCLK can be used for the whole I/O Bank.

**Figure 3-16 GW1NZ-1 HCLK Distribution**

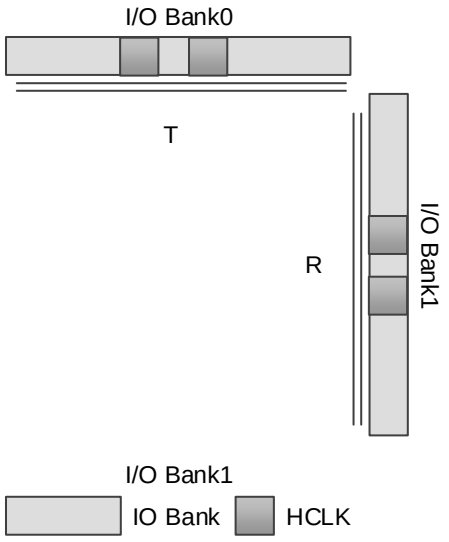



**Figure 3-17 GW1NZ-2 HCLK Distribution**

TBD

## 3.11 Long Wire (LW)

As a supplement to the CRU, the GW1NZ series of FPGA products provide another routing resource, Long Wire, which can be used as clock, clock enable, set/reset, or other high fan-out signals.

## 3.12 Global Set/Reset (GSR)

A global set/reset (GSR) network is built in the GW1NZ series of FPGA products. There is a direct connection to the core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset. The registers in CFU and I/O can be individually configured to use GSR.

# 3.13 Programming Configuration

The GW1NZ series of FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. The GW1NZ series of FPGA products support DUAL BOOT, providing a selection for users to back up data to off-chip Flash according to requirements.

Besides JTAG, the GW1NZ series of FPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, CPU, and $I^2C$ Slave). All the devices support JTAG and AUTO BOOT. For more information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

## 3.13.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the device.

## 3.13.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”. The GW1NZ series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

# 3.14 On-Chip Oscillator

There is an on-chip oscillator in each of the GW1NZ series of FPGA products. The on-chip oscillator provides a programmable user clock with precision of ±5%. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-13 for the output frequency.

**Table 3-13 Oscillator Output Frequency Options**

| Mode | Frequency | Mode | Frequency | Mode | Frequency |
|---|---|---|---|---|---|
| 0 | 2.5MHz[1] | 8 | 7.8MHz | 16 | 15.6MHz |
| 1 | 5.4MHz | 9 | 8.3MHz | 17 | 17.9MHz |
| 2 | 5.7MHz | 10 | 8.9MHz | 18 | 21MHz |
| 3 | 6.0MHz | 11 | 9.6MHz | 19 | 25MHz |
| 4 | 6.3MHz | 12 | 10.4MHz | 20 | 31.3MHz |
| 5 | 6.6MHz | 13 | 11.4MHz | 21 | 41.7MHz |
| 6 | 6.9MHz | 14 | 12.5MHz | 22 | 62.5MHz |
| 7 | 7.4MHz | 15 | 13.9MHz | 23 | 125MHz[2] |

**Note!**

- [1] The default frequency is 2.5MHz.
- [2] 125 MHz is not suitable for MSPI.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

$f_{out}$=250MHz/Param.

“Param” is the configuration parameter with a range of 2~128. It supports even numbers only.

# 4 AC/DC Characteristic

## 4.1 Operating Conditions

### 4.1.1 Absolute Max. Ratings

**Table 4-1 Absolute Max. Ratings**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | Core voltage | -0.5V | 1.32V |
| $V_{CCIO}$ | I/O Bank Power | -0.5V | 3.75V |
| $V_{CCX}$ | Auxiliary Power | -0.5V | 3.75V |
| - | I/O Voltage Applied[1] | -0.5V | 3.75V |
| Storage Temperature | Storage Temperature | -65℃ | +150℃ |
| Junction Temperature | Junction Temperature | -40℃ | +125℃ |

**Note!**

[1] Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2)V are allowed for a duration of <20 ns.

### 4.1.2 Recommended Operating Conditions

**Table 4-2 Recommended Operating Conditions**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | LV: Core Power | 1.14V | 1.26V |
| | ZV: Core Power | 0.88V | 1.2V |
| $V_{CCIO}$ | I/O Bank Power | 1.14V | 3.6V |
| $V_{CCX}$ | Auxiliary voltage | 1.71V | 3.6V[2] |
| $T_{JCOM}$ | Junction temperature Commercial operation | 0℃ | +85℃ |
| $T_{JIND}$ | Junction temperature Industrial operation | -40℃ | +100℃ |

**Note!**

- For the detailed recommended operating conditions for different packages, please refer to *UG842, GW1NZ-1 Pinout*, *UG847, GW1NZ-2 Pinout*.
- The low power mode of GW1NZ-2 requires $V_{CCX} \leqslant 2.5V$.

### 4.1.3 Power Supply Ramp Rates

**Table 4-3 Power Supply Ramp Rates**

| Name | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| $V_{CC}$ Ramp | Power supply ramp rates for $V_{CC}$ | 1.2mV/μs | - | 40mV/μs |
| $V_{CCX}$ Ramp | Power supply ramp rates for $V_{CCX}$ | 0.6mV/μs | - | 10mV/us |
| $V_{CCIO}$ Ramp | Power supply ramp rates for $V_{CCIO}$ | 0.1mV/μs | - | 10mV/us |

**Note!**

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

### 4.1.4 Hot Socket Specifications

**Table 4-4 Hot Socket Specifications**

| Name | Description | Condition | I/O Type | Max. |
|---|---|---|---|---|
| $I_{HS}$ | Input or I/O leakage current | $0<V_{IN}<V_{IH}$(MAX) | I/O | 150uA |
| $I_{HS}$ | Input or I/O leakage current | $0<V_{IN}<V_{IH}$(MAX) | TDI, TDO, TMS, TCK | 120uA |

### 4.1.5 POR Specification

**Table 4-5 POR Specification**

| Name | Description | Device | Name | Value |
|---|---|---|---|---|
| $V_{POR\_UP}$ | Power on reset ramp up trip point | GW1NZ-1 | $V_{CC}$ | 0.8V |
| | | | $V_{CCX}$ | 1.5V |
| | | | $V_{CCIO}$ | 0.9V |
| $V_{POR\_DOWN}$ | Power on reset ramp down trip point | | $V_{CC}$ | 0.65V |
| | | | $V_{CCX}$ | 1.4V |
| | | | $V_{CCIO}$ | 0.7V |
| $V_{POR\_UP}$ | Power on reset ramp up trip point | GW1NZ-2 | $V_{CC}$ | 0.8V |
| | | | $V_{CCX}$ | 1.5V |
| | | | $V_{CCIO}$ | 0.95V |
| $V_{POR\_DOWN}$ | Power on reset ramp down trip point | | $V_{CC}$ | 0.65V |
| | | | $V_{CCX}$ | 1.3V |
| | | | $V_{CCIO}$ | 0.75V |

## 4.2 ESD

**Table 4-6 GW1NZ ESD - HBM**

| Device | GW1NZ-1 | GW1NZ-2 |
|---|---|---|
| CS16 | HBM>1,000V | - |

| Device | GW1NZ-1 | GW1NZ-2 |
|---|---|---|
| FN32 | HBM>1,000V | - |
| FN32F | HBM>1,000V | - |
| QN48 | HBM>1,000V | HBM>1,000V |
| CS100H | - | HBM>1,000V |

**Table 4-7 GW1NZ ESD – CDM**

| Device | GW1NZ-1 | GW1NZ-2 |
|---|---|---|
| CS16 | CDM>500V | - |
| FN32 | CDM>500V | - |
| FN32F | CDM>500V | - |
| QN48 | CDM>500V | CDM>500V |
| CS100H | - | CDM>500V |

# 4.3 DC Characteristic

## 4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

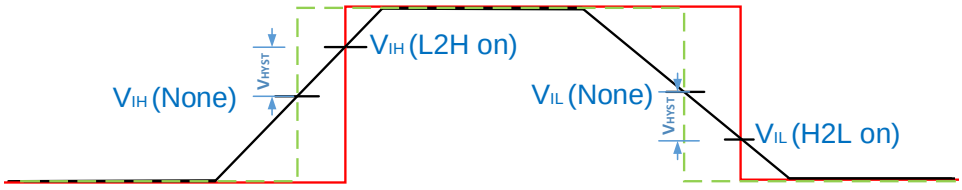
**Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions**

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$ | Input or I/O leakage | $V_{CCIO}<V_{IN}<V_{IH}$ (MAX) | - | - | 210 μA |
| | | $0V<V_{IN}<V_{CCIO}$ | - | - | 10μA |
| $I_{PU}$ | I/O Active Pull-up Current | $0<V_{IN}<0.7V_{CCIO}$ | -30 μA | - | -150 μA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX)$<V_{IN}<V_{CCIO}$ | 30 μA | - | 150 μA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN}=V_{IL}$ (MAX) | 30 μA | - | - |
| $I_{BHHO}$ | Bus Hold High Sustaining Current | $V_{IN}=0.7V_{CCIO}$ | -30 μA | - | - |
| $I_{BHLO}$ | Bus HoldLow Overdrive Current | $0\leq V_{IN}\leq V_{CCIO}$ | - | - | 150 μA |
| $I_{BHHO}$ | Bus HoldHigh Overdrive Current | $0\leq V_{IN}\leq V_{CCIO}$ | - | - | -150 μA |
| $V_{BHT}$ | Bus hold trigger points | | $V_{IL}$ (MAX) | - | $V_{IH}$ (MIN) |
| C1 | I/O Capacitance | | | 5 pF | 8 pF |
| $V_{HYST}$ | Hysteresis for Schmitt Trigger inputs | $V_{CCIO}$=3.3V, Hysteresis=L2H[1],[2] | - | 200mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= L2H | - | 125mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis= L2H | - | 60mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis= L2H | - | 40mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= L2H | - | 20mV | - |
| | | $V_{CCIO}$=3.3V, Hysteresis= H2L[1],[2] | - | 200mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= H2L | - | 125mV | - |

| Name | Description | Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| | | $V_{CCIO}$=1.8V, Hysteresis= H2L | - | 60mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis= H2L | - | 40mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= H2L | - | 20mV | - |
| | | $V_{CCIO}$=3.3V, Hysteresis= HIGH[1],[2] | - | 400mV | - |
| | | $V_{CCIO}$=2.5V, Hysteresis= HIGH | - | 250mV | - |
| | | $V_{CCIO}$=1.8V, Hysteresis= HIGH | - | 120mV | - |
| | | $V_{CCIO}$=1.5V, Hysteresis= HIGH | - | 80mV | - |
| | | $V_{CCIO}$=1.2V, Hysteresis= HIGH | - | 40mV | - |

**Note!**

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising $V_{IH}$ by $V_{HYST}$; enabling the H2L (high to low) option means lowering $V_{IL}$ by $V_{HYST}$; enabling the HIGH option means enabling both L2H and H2L options, i.e. $V_{HYST}$(HIGH) = $V_{HYST}$(L2H) + $V_{HYST}$(L2H). The diagram is shown below.




## 4.3.2 Static Current

**Table 4-9 Static Supply Current (LV Device)**

| Name | Description | Device | Typ. |
|---|---|---|---|
| $I_{CC}$ | Core current (Vcc=1.2V) | GW1NZ-1 | 3mA |
| $I_{CCX}$ | $V_{CCX}$ current ($V_{CCX}$=3.3V) | GW1NZ-1 | 0.5mA |
| | $V_{CCX}$ current ($V_{CCX}$=2.5V) | GW1NZ-1 | 0.5mA |
| $I_{CCIO}$ | I/O Bank current ($V_{CCIO}$=2.5V) | GW1NZ-1 | 0.5mA |

**Table 4-10 Static Supply Current (GW1NZ-1, ZV Version)**

| Name | Description | Device | Typ. |
|---|---|---|---|
| $I_{CC}$ | Core current (Vcc=0.9V) | GW1NZ-ZV1FN32C5/I4<br>GW1NZ-ZV1CS16C5/I4 | 50uA |
| | | GW1NZ-ZV1FN32I3<br>GW1NZ-ZV1CS16I3 | 40uA |
| | | GW1NZ-ZV1FN32I2<br>GW1NZ-ZV1CS16I2 | 30uA |
| $I_{CCX}$ | $V_{CCX}$ current ($V_{CCX}$ floating) | GW1NZ-ZV1FN32C5/I4<br>GW1NZ-ZV1CS16C5/I4 | 0uA |
| | | GW1NZ-ZV1FN32I3<br>GW1NZ-ZV1CS16I3 | 0uA |
| | | GW1NZ-ZV1FN32I2<br>GW1NZ-ZV1CS16I2 | 0uA |
| | $V_{CCX}$ current ($V_{CCX}$=1.8V~3.3V) | GW1NZ-ZV1FN32C5/I4<br>GW1NZ-ZV1CS16C5/I4 | 1uA |

| Name | Description | Device | Typ. |
|---|---|---|---|
| | | GW1NZ-ZV1FN32I3<br>GW1NZ-ZV1CS16I3 | 1uA |
| | | GW1NZ-ZV1FN32I2<br>GW1NZ-ZV1CS16I2 | 1uA |
| $I_{CCIO}$ | I/O Bank current ($V_{CCIO}$=3.3V) | GW1NZ-ZV1FN32C5/I4<br>GW1NZ-ZV1CS16C5/I4 | 0uA |
| | | GW1NZ-ZV1FN32I3<br>GW1NZ-ZV1CS16I3 | 0uA |
| | | GW1NZ-ZV1FN32I2<br>GW1NZ-ZV1CS16I2 | 0uA |

**Note!**

- After the device wakes up, you can turn off the external Vccx without affecting the normal operation of the device when you are not using the user flash.
- The typical values in the table above are tested at room temperature.
- In zero power circumstances, if you use the MODE pin, the PULL_MODE of this pin must be configured as KEEPER.

**Table 4-11 Static Supply Current (GW1NZ-2, ZV Version)[1],[3],[4]**

| Name | Description | Typ. |
|---|---|---|
| $I_{CC}$ | Core current（$V_{CC}$=1.1V） | 600uA |
| | Core current（$V_{CC}$=1.0V） | 240uA |
| | Core current（$V_{CC}$=0.9V） | 120uA |
| $I_{CCX}$ | $V_{CCX}$ current（$V_{CCX}$=1.8V） | 150uA |
| $I_{CCIO}$ | I/O Bank current ($V_{CCIO}$=1.8V) | 0uA[2] |

**Note!**

- [1] Test condition: 25℃, BGEN(bandgap enable)=0.
- [2] $I_{CCIO}$ is determined by your external IO circuit and pull-up/down state, and theoretically zero power consumption can be achieved.
- [3] Low power mode requires $V_{CCX}$≤2.5V.
- [4] You can also choose to turn off $V_{CCX}$/$V_{CCIO}$ when entering ultra-low power mode, and the data in the device's SRAM will be retained.

## 4.3.3 I/O Operating Conditions Recommended

**Table 4-12 I/O Operating Conditions Recommended**

| Name | Output $V_{CCIO}$ (V) | | | Input $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVTTL33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVCMOS33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | - | - | - |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | - | - | - |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | - | - | - |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | - | - | - |
| SSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| SSTL18_I | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |

| Name | Output $V_{CCIO}$ (V) | | | Input $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| SSTL18_II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL25_II | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL33_I | 3.135 | 3.3 | 3.6 | 1.3 | 1.5 | 1.7 |
| SSTL33_II | 3.135 | 3.3 | 3.6 | 1.3 | 1.5 | 1 |
| HSTL18_I | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL18_II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| PCI33 | 3.135 | 3.3 | 3.6 | - | - | - |
| LVPECL33E | 3.135 | 3.3 | 3.6 | - | - | - |
| MLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| BLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| RSDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| LVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL15D | 1.425 | 1.5 | 1.575 | - | - | - |
| SSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL25D_I | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL25D_II | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL33D_I | 3.135 | 3.3 | 3.6 | - | - | - |
| SSTL33D_II | 3.135 | 3.3 | 3.6 | - | - | - |
| HSTL15D | 1.425 | 1.575 | 1.89 | - | - | - |
| HSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| HSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |

## 4.3.4 Single - Ended IO DC Electrical Characteristic

**Table 4-13 Single - Ended IO DC Electrical Characteristic**

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| LVCMOS33 LVTTL33 | -0.3V | 0.8V | 2.0V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | | | 24 | -24 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS25 | -0.3V | 0.7V | 1.7V | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |

| Name | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ (Max) | $V_{OH}$ (Min) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS18 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS15 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| LVCMOS12 | -0.3V | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 3.6V | 0.4V | $V_{CCIO}$-0.4V | 2 | -2 |
| | | | | | | | 6 | -6 |
| | | | | | 0.2V | $V_{CCIO}$-0.2V | 0.1 | -0.1 |
| PCI33 | -0.3V | 0.3 x $V_{CCIO}$ | 0.5 x $V_{CCIO}$ | 3.6V | 0.1 x $V_{CCIO}$ | 0.9 x $V_{CCIO}$ | 1.5 | -0.5 |
| SSTL33_I | -0.3V | $V_{REF}$-0.2V | $V_{REF}$+0.2V | 3.6V | 0.7 | $V_{CCIO}$-1.1V | 8 | -8 |
| SSTL25_I | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | 0.54V | $V_{CCIO}$-0.62V | 8 | -8 |
| SSTL25_II | -0.3V | $V_{REF}$-0.18V | $V_{REF}$+0.18V | 3.6V | N/A | N/A | N/A | N/A |
| SSTL18_II | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125V | 3.6V | N/A | N/A | N/A | N/A |
| SSTL18_I | -0.3V | $V_{REF}$-0.125V | $V_{REF}$+0.125V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| SSTL15 | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL18_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL18_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | N/A | N/A | N/A | N/A |
| HSTL15_I | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | 0.40V | $V_{CCIO}$-0.40V | 8 | -8 |
| HSTL15_II | -0.3V | $V_{REF}$-0.1V | $V_{REF}$+ 0.1V | 3.6V | N/A | N/A | N/A | N/A |

**Note!**

[1 ]The total DC current limit(sourced and sunk) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

# 4.4 Switching Characteristic

## 4.4.1 CFU Block Internal Timing Parameters

**Table 4-14 CFU Block Internal Timing Parameters**

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{LUT4\_CFU}$ | LUT4 delay | - | 0.674 | ns |
| $t_{LUT5\_CFU}$ | LUT5 delay | - | 1.388 | ns |
| $t_{LUT6\_CFU}$ | LUT6 delay | - | 2.01 | ns |

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{LUT7\_CFU}$ | LUT7 delay | - | 2.632 | ns |
| $t_{LUT8\_CFU}$ | LUT8 delay | - | 3.254 | ns |
| $t_{SR\_CFU}$ | Set/Reset to Register output | - | 1.86 | ns |
| $t_{CO\_CFU}$ | Clock to Register output | - | 0.76 | ns |

## 4.4.2 Gearbox Switching Characteristics

**Table 4-15 Gearbox Switching Characteristics**

TBD

## 4.4.3 Clock and I/O Switching Characteristics

**Table 4-16 Clock and I/O Switching Characteristics**

| Name | Description | Device | -5 | | -6 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Clocks | TBD | TBD | TBD | TBD | TBD | TBD | |
| Pin-LUT-Pin Delay | TBD | TBD | TBD | TBD | TBD | TBD | |
| General I/O Pin Parameters | TBD | TBD | TBD | TBD | TBD | TBD | |

## 4.4.4 BSRAM Switching Characteristics

**Table 4-17 BSRAM Internal Timing Parameters**

| Name | Description | Speed Grade | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{COAD\_BSRAM}$ | Clock to output from read address/data | - | 5.10 | ns |
| $t_{COOR\_BSRAM}$ | Clock to output from output register | - | 0.56 | ns |

## 4.4.5 On-chip Oscillator Output Frequency

**Table 4-18 O-chip Oscillator Output Frequency**

| Name | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency (0 to 85℃) | 106.25MHz | 125MHz | 143.75MHz |
| | Output Frequency (-40 to +100℃) | 100MHz | 125MHz | 150MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43% | 50% | 57% |
| $t_{OPJIT}$ | Output Clock Period Jitter | 0.01UIPP | 0.012UIPP | 0.02UIPP |

## 4.4.6 PLL Switching Characteristics

**Table 4-19 PLL Switching Characteristics**

| Device | LV/ZV | Speed Grade | Name | Min. | Max. |
|---|---|---|---|---|---|
| GW1NZ-1 | LV | C6/I5 | CLKIN | 3MHZ | 400MHZ |
| | | | PFD | 3MHZ | 400MHZ |
| | | | VCO | 400MHZ | 800MHZ |
| | | | CLKOUT | 3.125MHZ | 400MHZ |

| Device | LV/ZV | Speed Grade | Name | Min. | Max. |
|---|---|---|---|---|---|
| | | C5/I4 | CLKIN | 3MHZ | 320MHZ |
| | | | PFD | 3MHZ | 320MHZ |
| | | | VCO | 320MHZ | 640MHZ |
| | | | CLKOUT | 2.5MHZ | 360MHZ |
| | ZV | C5/I4 | CLKIN | 3MHZ | 200MHZ |
| | | | PFD | 3MHZ | 200MHZ |
| | | | VCO | 200MHZ | 400MHZ |
| | | | CLKOUT | 1.5625MHZ | 200MHZ |
| | | I3 | CLKIN | 3MHZ | 150MHZ |
| | | | PFD | 3MHZ | 150MHZ |
| | | | VCO | 150MHZ | 300MHZ |
| | | | CLKOUT | 1.171875MHZ | 150MHZ |
| | | I2 | CLKIN | 3MHZ | 100MHZ |
| | | | PFD | 3MHZ | 100MHZ |
| | | | VCO | 100MHZ | 200MHZ |
| | | | CLKOUT | 0.78125MHZ | 100MHZ |
| GW1NZ-2 | ZV | I3 | CLKIN | TBD | TBD |
| | | | PFD | TBD | TBD |
| | | | VCO | TBD | TBD |
| | | | CLKOUT | TBD | TBD |
| | | I2 | CLKIN | TBD | TBD |
| | | | PFD | TBD | TBD |
| | | | VCO | TBD | TBD |
| | | | CLKOUT | TBD | TBD |

# 4.5 User Flash Characteristic

## 4.5.1 DC Characteristic

**Table 4-20 GW1NZ-1 User Flash DC Characteristics**

| Name | Parameter | Max. | | Unit | Wake-up Time | Condition |
|---|---|---|---|---|---|---|
| | | $V_{CC}$[3] | $V_{CCX}$ | | | |
| Read mode (w/l 25ns)[1] | $I_{CC1}$[2] | 2.19 | 0.5 | mA | N/A | Min. Clcok period, duty cycle 100%, VIN = “1/0” |
| Write mode | | 0.1 | 12 | mA | N/A | |
| Erase mode | | 0.1 | 12 | mA | N/A | |
| Page Erasure Mode | | 0.1 | 12 | mA | N/A | |
| Read mode static current (25-50ns) | $I_{CC2}$ | 980 | 25 | μA | N/A | XE=YE=SE=“1”, between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode. |

| Name | Parameter | Max. | | Unit | Wake-up Time | Condition |
|---|---|---|---|---|---|---|
| | | $V_{CC}$[3] | $V_{CCX}$ | | | |
| Standby mode | $I_{SB}$ | 5.2 | 20 | μA | 0 | $V_{SS}$, $V_{CCX}$, and $V_{CC}$ |
| Floating mode[3] | $I_{PD}$ | 0 | 0 | μA | 7us | $V_{CCX}$=0 |
| Typical Value (Room temperature: 25℃) | | | | | | |
| Standby mode | $I_{SB}$ | 0.4 | 7.5 | μA | 0 | $V_{SS}$, $V_{CCX}$, and $V_{CC}$ |
| Floating mode[3] | $I_{PD}$ | 0 | 0 | μA | 3.5us | $V_{CCX}$=0 |

**Note!**

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different $T_{new}$ clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + $I_{CC2}$
  - $T_{new}$>50ns: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + 50ns x $I_{CC2}/T_{new}$ + $I_{SB}$
  - t > 50ns, $I_{CC2}$ = $I_{SB}$
- [3] Only supported in user flash in sleep mode.

**Table 4-21 GW1NZ-2 User Flash DC Characteristic[4]**

| Name | Param-eter | Max. | | Unit | Wake-up Time | Condition |
|---|---|---|---|---|---|---|
| | | $V_{CC}$[3] | $V_{CCX}$ | | | |
| Read mode (w/l 25ns)[1] | $I_{CC1}$[2] | 2.19 | 0.5 | mA | NA | Min. Clock period, duty cycle 100%, VIN = “1/0” |
| Write mode | | 0.1 | 12 | mA | NA | |
| Erase mode | | 0.1 | 12 | mA | NA | |
| Page Erasure Mode | | 0.1 | 12 | mA | NA | |
| Read mode static current (25-50ns) | $I_{CC2}$ | 980 | 25 | μA | NA | XE=YE=SE=“1”, between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode. |
| Standby mode | $I_{SB}$ | 5.2 | 20 | μA | 0 | $V_{SS}$, $V_{CCX}$, and $V_{CC}$ |

**Note!**

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different $T_{new}$ clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + $I_{CC2}$
  - $T_{new}$>50ns: $I_{CC1}$ (new) = ($I_{CC1}$ - $I_{CC2}$)($T_{acc}/T_{new}$) + 50ns x $I_{CC2}/T_{new}$ + $I_{SB}$
  - t > 50ns, $I_{CC2}$ = $I_{SB}$
- [3] $V_{CC}$ must be greater than 1.08V from the zero wake-up time.
- [4] The leakage current of Flash is included in the leakage current of the device, see Table 4-4.

## 4.5.2 Timing Parameters[1],[5],[6]

**Table 4-22 User Flash Timing Parameters**

| User Modes | Parameter | Name | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Access time[2] | WC1 | $T_{acc}$[3] | - | 25 | ns |
| | TC | | - | 22 | ns |
| | BC | | - | 21 | ns |
| | LT | | - | 21 | ns |
| | WC | | - | 25 | ns |
| Program/Erase to data storage | | $T_{nvs}$ | 5 | - | μs |
| Data storage hold time | | $T_{nvh}$ | 5 | - | μs |
| Data storage hold time (Overall erase) | | $T_{nvh1}$ | 100 | - | μs |
| Time from data storage to program setup | | $T_{pgs}$ | 10 | - | μs |
| Program hold time | | $T_{pgh}$ | 20 | - | ns |
| Program time | | $T_{prog}$ | 8 | 16 | μs |
| Write prepare time | | $T_{wpr}$ | >0 | - | ns |
| Erase hold time | | $T_{whd}$ | >0 | - | ns |
| Time from control signal to write/Erase setup | | $T_{cps}$ | -10 | - | ns |
| Time from SE to read setup | | $T_{as}$ | 0.1 | - | ns |
| E pulse high level time | | $T_{pws}$ | 5 | - | ns |
| Address/data setup time | | $T_{ads}$ | 20 | - | ns |
| Address/data hold time | | $T_{adh}$ | 20 | - | ns |
| Data hold-up time | | $T_{dh}$ | 0.5 | - | ns |
| Read mode address hold time[3] | WC1 | $T_{ah}$ | 25 | - | ns |
| | TC | | 22 | - | ns |
| | BC | | 21 | - | ns |
| | LT | | 21 | - | ns |
| | WC | | 25 | - | ns |
| SE pulse low level time | | $T_{nws}$ | 2 | - | ns |
| Recovery time | | $T_{rcv}$ | 10 | - | μs |
| Data storage time | | $T_{hv}$[4] | - | 6 | ms |
| Erasure time | | $T_{erase}$ | 100 | 120 | ms |
| Overall erase time | | $T_{me}$ | 100 | 120 | ms |
| Wake-up time from power down to standby mode | | $T_{wk\_pd}$ | 7 | - | μs |
| Standby hold time | | $T_{sbh}$ | 100 | - | ns |
| $V_{CC}$ setup time | | $T_{ps}$ | 0 | - | ns |
| $V_{CCX}$ hold time | | $T_{ph}$ | 0 | - | ns |

**Note!**

- [1] The parameter values may change;
- [2] The values are simulation data only.

- [3]After XADR, YADR, XE, and YE are valid, $T_{acc}$ starts from the rising edge of the SE signal. DOUT is kept until the next valid read operation;
- [4]$T_{hv}$ is the time between write and the next erasure. The same address can not be written twice before the next erase, nor does the same register. This limitation is for safety;
- [5] All waveforms have a 1ns rising edge time and a 1ns falling edge time;
- [6] TX, YADR, XE, and YE hold time need to be $T_{acc}$ at least, and $T_{acc}$ starts from the rising edge of the SE signal.

## 4.5.3 Operation Timing Diagrams

**Figure 4-1 Read Mode**

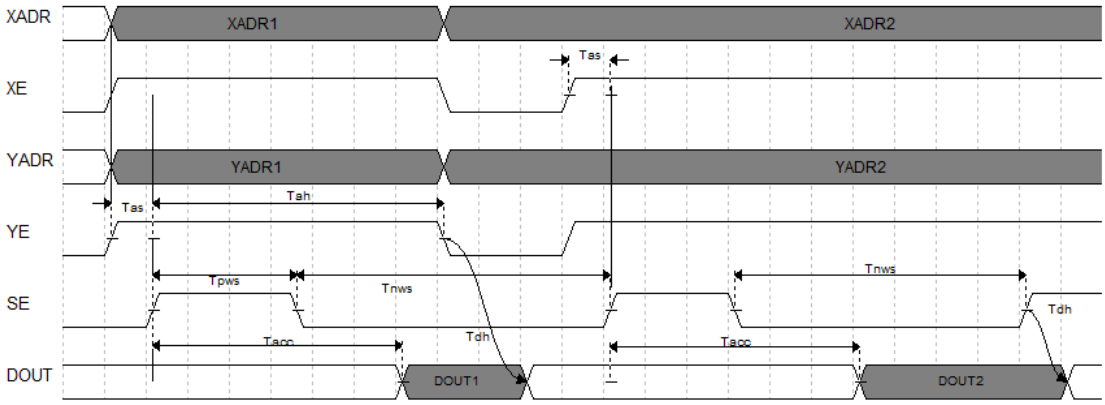


**Figure 4-2 Write Mode**

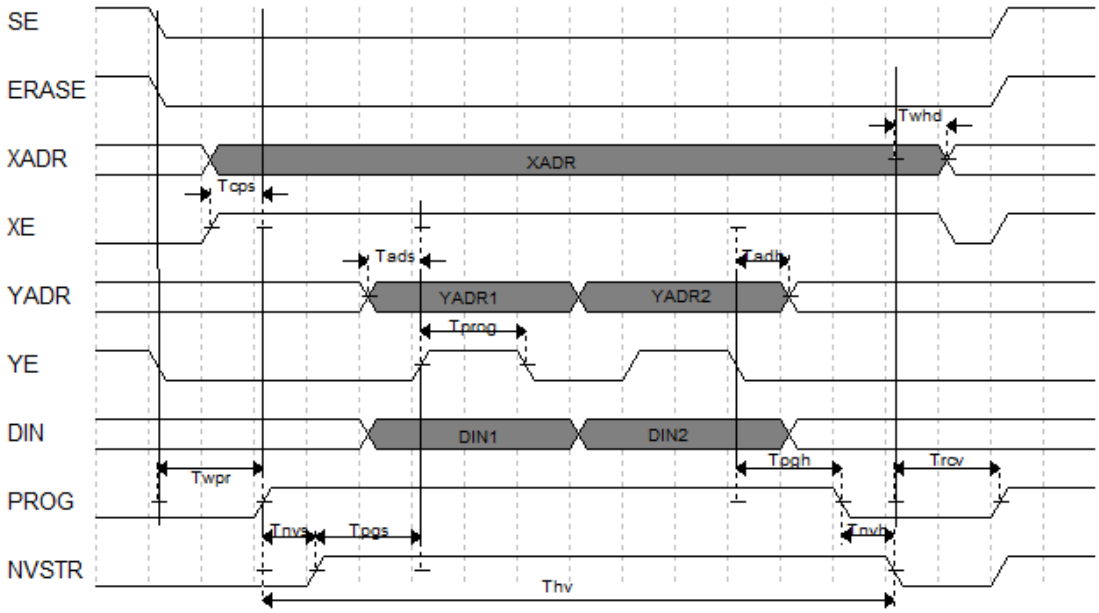
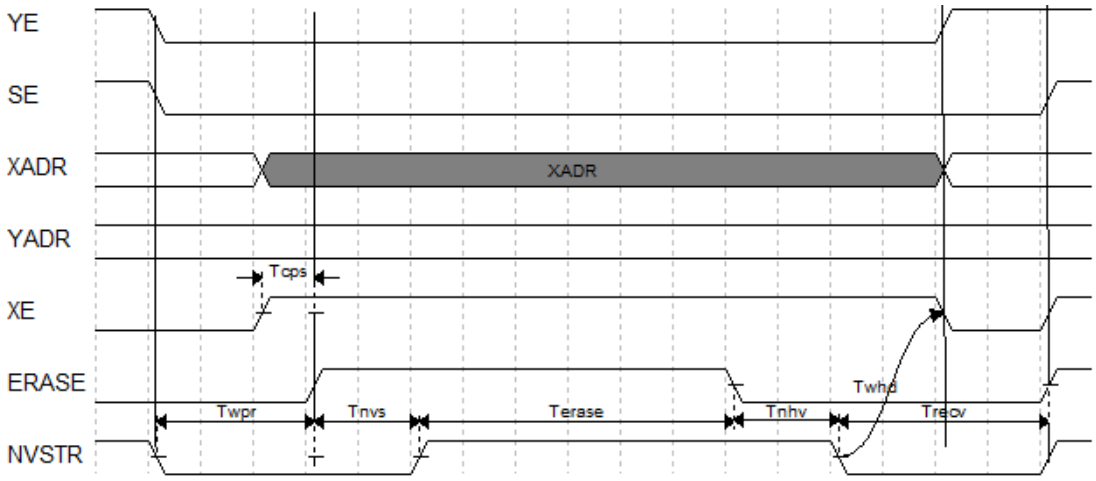



**Figure 4-3 Erasure Mode**




# 4.6 Configuration Interface Timing Specification

The GW1NZ series of FPGA products support six GowinCONFIG configuration modes: AUTO BOOT, DUAL BOOT, MSPI, SSPI, SERIAL, and CPU. For more detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration* User Guide.

# 5 Ordering Information

## 5.1 Part Name

**Figure 5-1 Part Naming Example–ES**

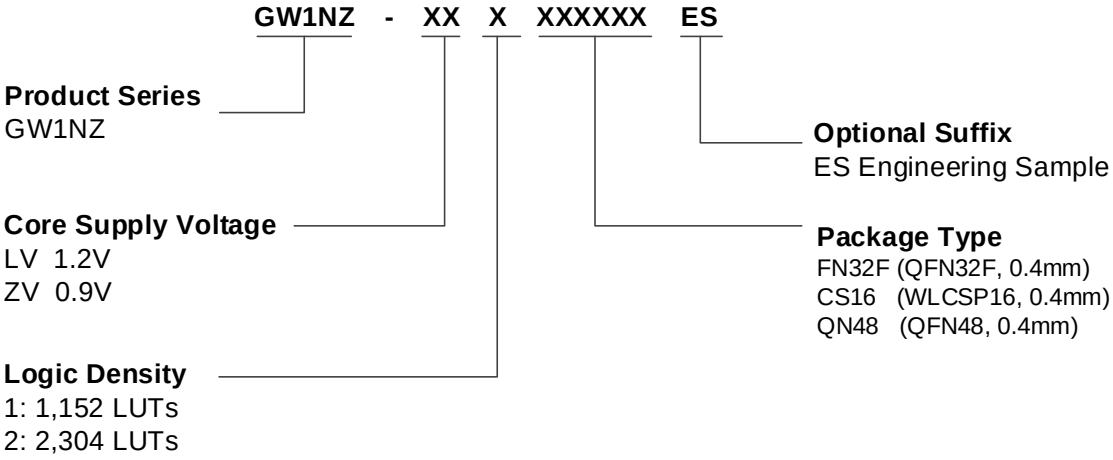
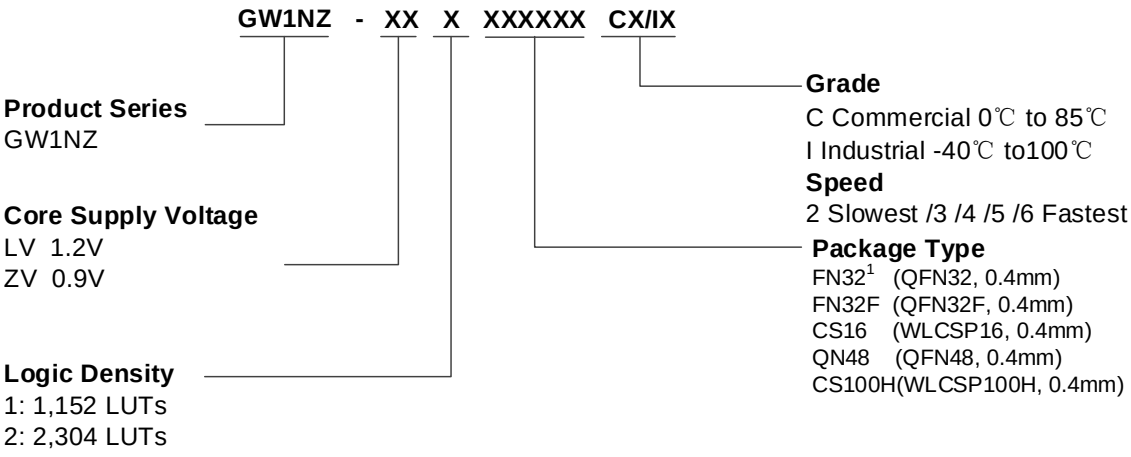



**Figure 5-2 Part Naming Example–Production**




**Note!**

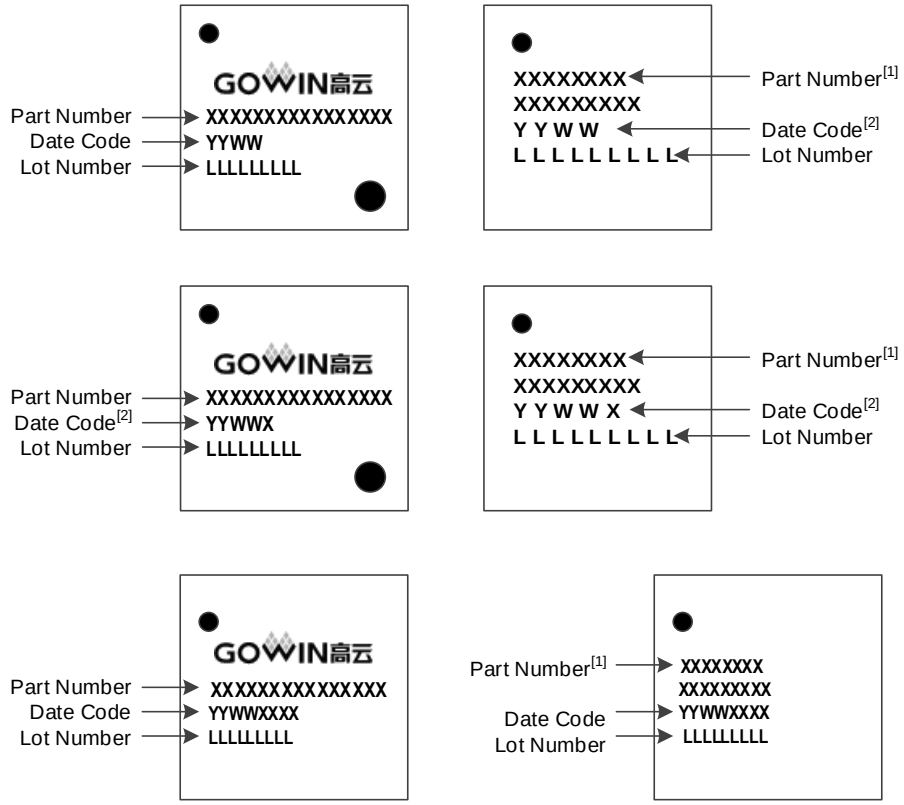
- [1] FN32 is the legacy version.
- For more package information and resource information, please refer to 2.2 Product Resources and 2.3 Package Information.

- Both “C” and “I” are used for some of the GW1NZ series of FPGA products. These devices are screened using industrial standards, so they can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets the speed grade 5 in the commercial grade application, the speed grade is 4 in the industrial grade application.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.

# 5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

**Figure 5-3 Package Mark**




**Note!**

- [1] The first two lines in the right figure above are the “Part Number”.
- [2] The Date Code followed by an “X” is for X version devices.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