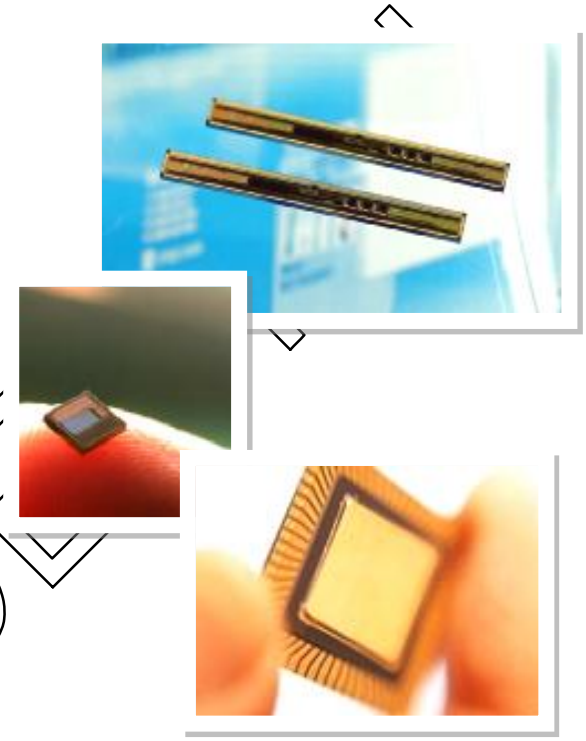
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM68140 Data Sheet

262,144-color, 320 RGB x 480 dots graphics liquid crystal controller driver for Amorphous-Silicon TFT Panel

Revision：0.3
Date：Jun 05, 2012

Revision History

Version No.	Date	Page	Description
0.0	2011/09/05		Initial
0.1	2011/12/1	Page.85	Modify DDVDH to VPG.
		Page.12	Modify from (DDVDH + 0.3) to (DDVDH - 0.3)
		Page.37	Modify from D[21:0] to D[17:0]
0.2	2011/12/29	Page.12 & 17	Add VREF description
		Page.219	Update BT[2:0] table
		Page.252	Update external component table
0.3	2012/06/05	P.104	Remove dummy read parameter

Table of Contents

1. General Description

The RM68140 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising 345,600 bytes RAM for a maximum 320RGB x 480 dots graphics display, source driver, gate driver and power supply circuit.

The RM68140 supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-/16-bit RGB interface, MDDI interface and MIPI interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

Also, the RM68140 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages. The RM68140's power management functions such as 8-color display and power operation mode such as deep standby mode and sleep mode make this LSI a perfect driver for the medium or small sized portable products with color display systems such as digital cellular phones or hand-held devices with outstanding battery consistency.

2. Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 320 RGB x 480 dots graphics display on amorphous TFT panel in 262k colors
- 345,600-byte internal RAM
- System interface
  - (1). Parallel 8080-series MCU Interface (8-, 9-. 16-, 18-bit)
  - (2). Serial Peripheral Interface
- 16, 18-bit RGB Interface
- High speed interface
  - (1). Mobile Display Digital Interface (MDDI V1.2, 1 clock and 1 data lane pairs)
  - (2). MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 data lane pairs)
- High-speed RAM write function
- Window address function to specify a rectangular area writing data in the internal RAM
- Abundant color display and drawing functions
  - (1). Programmable γ-correction function for 262k-color display
  - (2). Partial display function
- Display color mode
  - (1). Full color mode: 262k colors
  - (2). Reduce color mode:
    1. 65k colors
    2. 8 colors (Idle mode)
- Low power consumption architecture
  - (1). Deep standby mode
  - (2). Sleep mode
  - (3). 8-color display function
- Support dot, column and zigzag inversion
- Separate RGB gamma correction
- Content Adaptive Brightness Control (CABC)

- Input power supply voltages:

  (1). IOVCC = 1.65V~3.6V (interface I/O power supply)

  (2). VCI = 2.5V~3.6V (liquid crystal analog circuit power supply)

- Incorporates a liquid crystal drive power supply circuit

  (1). Source driver liquid crystal drive/VCOM power supply:

  1. DDVDH-GND = 4.5V ~ 6.0V
  2. DDVDL-GND = -4.5V ~ -5.0V
  3. VCL-GND ≦ -VCI1 (-2.0V ~ -3.0V)

  (2). Gate drive power supply:

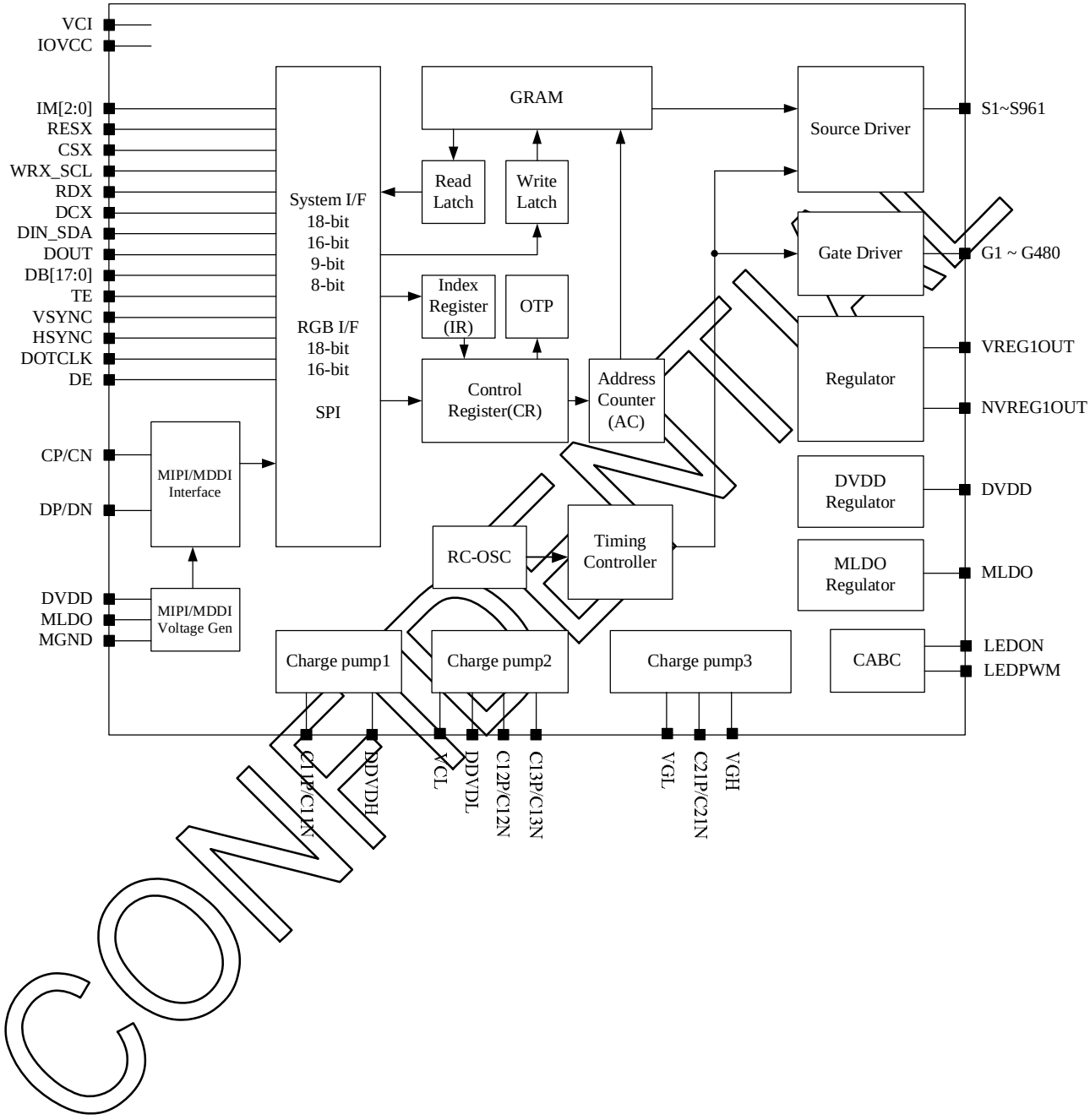
  1. VGH-GND = 10.0V ~ 17V
  2. VGL-GND = -7.5V ~ -15V
  3. VGH-VGL ≦ 32V

  (3). VCOM drive (VCOM power supply):

  1. VCOM = 0V ~ -2.0V

- Internal NVM: VCOM level adjustment, ID
- Operating temperature range: -40℃ ~ 85℃

3. Block Diagram



4. Pin Description

<table>
<tr><th colspan="3">Interface Logic Pins</th></tr>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Select MPU interface mode.
<table>
<tr><th>IM[2]</th><th>IM[1]</th><th>IM[0]</th><th>Interface Mode</th><th>DB Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI 9-bit interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI 16-bit interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI 8-bit interface</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MDDI</td><td>DATA_P/
DATA_N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI Type C 9-bit</td><td>DIN,DOUT</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI</td><td>DATA_P/
DATA_N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI Type C 8-bit</td><td>DIN,DOUT</td></tr>
</table></td></tr>
<tr><td>CSX</td><td>I</td><td>Chip select signal. Amplitude: IOVCC-DGND
Low: the chip is selected and accessible
High: the chip is not selected and not accessible.
Fix to IOVCC level when not in use.</td></tr>
<tr><td>DCX</td><td>I</td><td>Register select signal. Amplitude: IOVCC-DGND
Low: command data
High: parameter or display data
Fix to DGND when not in use.</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>Write strobe signal in DBI interface operation and enables write operation when WRX is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVCC-DGND
Fix to IOVCC level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>Read strobe signal in DBI interface operation and enables read operation when RDX is low. Amplitude: IOVCC-DGND.
Fix to IOVCC level when not in use.</td></tr>
<tr><td>DIN_SDA</td><td>I/O</td><td>Serial data pin in serial interface operation. Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
<tr><td>DOUT</td><td>O</td><td>Serial data output pin in serial interface operation. Amplitude: IOVCC-DGND
Leave the pin to open when not in use.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>18-bit parallel bi-directional data bus for DBI interface operation. Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable signal for DPI interface. Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Frame synchronous signal for DPI interface..
Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Line synchronous signal for DPI interface.
Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>Dot clock signal for DBI interface. Amplitude: IOVCC-DGND.
Fix to DGND when not in use.</td></tr>
</table>

TE	O	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. (Amplitude: IOVCC-DGND). *Leave the pin to open when not in use.*
RESX	I	Reset signal. Initializes the chip when it is low. Make sure to execute a power-on reset when turning on power supply. Amplitude: IOVCC-DGND.
STB_CLKP STB_CLKN	I	These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. These pins are MDDI_STB_P/N differential strobe signals if MDDI interface is used. STB_CLKP/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
DATA_P DATA_N	I/O	These pins are DSI-D0+/- differential data signals if MIPI interface is used. These pins are MDDI_DATA0_P/N differential strobe signals if MDDI interface is used. DATA_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
CABC_ON	O	This pin is connected to the external LED driver. It is a LED driver control signal which is used for turning ON/OFF the LED backlight. *Leave the pin to open when not in use.*
CABC_PWM	O	This pin is connected to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of CABC_PWM signal is set from 256 values between 0% (Low) and 100% (High). *Leave the pin to open when not in use.*

Power Supply		
Signal	I/O	Function
DGND AGND MGND	P	Power ground pin: GND = 0V.
IOVCC	P	Power supply to the interface pins: RESX, CSX, WRX, RDX, DCX, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.6V. VCC ≥ IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.
DVDD	O	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
VPG	P	Power supply pin for the NV memory programming. During OTP program mode, VPG=6V. Otherwise, please let VPG pin floating (or connected to VCI).
MLDO	O	Regulator output for internal MIPI/MDDI analog system Connect a capacitor for stabilization.

Step-up Circuit		
Signal	I/O	Function
VCI	P	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.
DDVDH	O	Power supply for the positive source driver. Connect to a stabilizing capacitor between DDVDH and GND. DDVDH = 4.5V ~ 6.0V

DDVDL	O	Power supply for the negative source driver. Connect to a stabilizing capacitor between DDVDL and GND. DDVDL = -4.5V ~ -5.0V
VGH	O	Power supply for the gate driver. Connect to a stabilizing capacitor between VGH and GND.
VGL	O	Power supply for the gate driver. Connect to a stabilizing capacitor between VGL and GND.
VCL	O	Charge pump output (-1 x VCI). Connect to a stabilizing capacitor between VCL and GND.
C11A, C11B C12A, C12B C13A, C13B	O	Capacitor connection pins for the step-up circuit 1.
C21A, C21B C22A, C22B	O	Capacitor connection pins for the step-up circuit 2. (C22A, C22B are not used)
VREG1OUT	O	Output voltage generated from the internal regulator. The voltage level is set with the VRH1 bits. VREG1OUT is positive source driver grayscale reference voltage, VREG1OUT = 3.5 ~ (DDVDH - 0.3)V
NVREG1OUT	O	Output voltage generated from the internal regulator. The voltage level is set with the VRH2 bits. NVREG1OUT is negative source driver grayscale reference voltage. NVREG1OUT = -3.5 ~ (DDVDL + 0.3)V
VREF	O	Output voltage generated from the internal reference voltage. (1.875V)

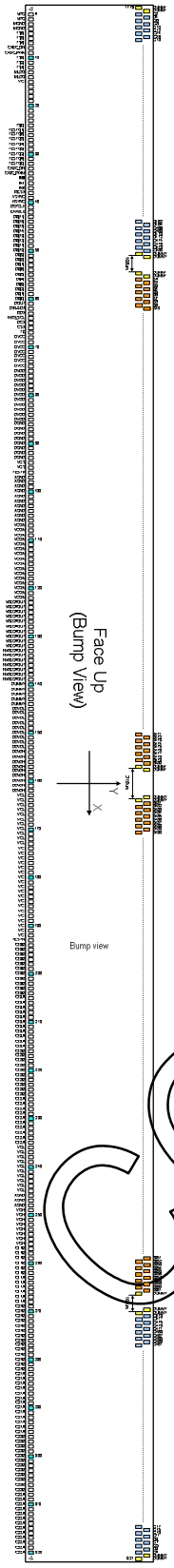
LCD Driver		
Signal	I/O	Function
VCOM	O	Power supply to TFT panel's common electrode, 0V ~ -2.0V.
VGS	I	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
S1~S961	O	Source driver output signals. Leave the pin to open when not in use.
G1~G480	O	Gate line output signals. VGH: gate line select level VGL: gate line non-select level *Leave the pin to open when not in use.*

Others		
Signal	I/O	Function
DUMMY	-	Dummy pads. *Leave the pin to open when not in use.*
TESTO[7:0]	O	Test pins. *Leave the pin to open.*
TESTP, TESTN	I	Test pins. *Leave these pins to open.*
TS[6:0]	I	Test pins. *Leave these pins to open.*

A- Si TFT LCD Drive Power Supply Specifications Table

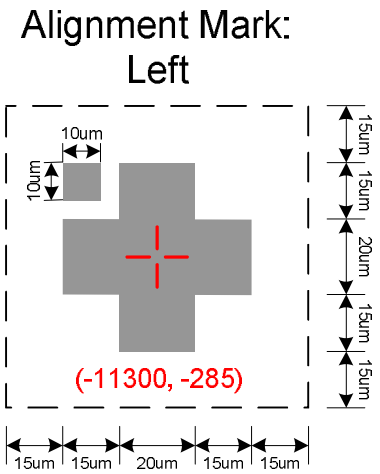
No.	Item		Description
1	TFT source driver		961 pins
2	TFT gate driver		480 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S961	V0 ~ V63 grayscales
		G1 ~ G480	VGH - VGL
		VCOM	DC VCOM
5	Input Voltage	IOVCC	1.65 ~ 3.6V
		VCI	2.50 ~ 3.6V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6V
		DDVDL	-4.5V ~ -5.0V
		VGH	10V ~ 17V
		VGL	-7.5V ~ -15V
		VCL	-2.0V ~ -3.0V
		VGH-VGL	Max. 32V
7	Internal Step-up Circuits	DDVDH	VCI x2
		DDVDL	VCI x-2
		VGH	VCI x4, x5, x6
		VGL	VCI x-3, x-4, x-5
		VCL	VCI x-1

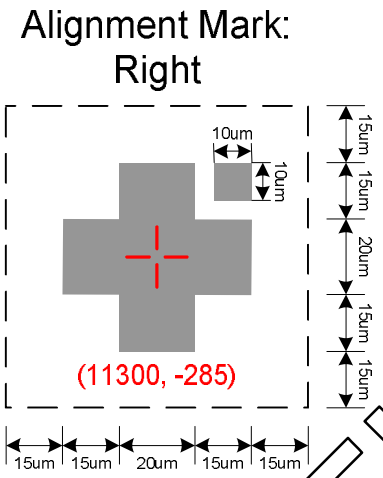
5. Pad Diagram and Coordination



	X (um)	Y (um)
Chip Size	22770	880
R-ALMARK	11300	-285
L-ALMARK	-11300	-285
Input Side-Bump	50	80
Output Side-Bump	15	100

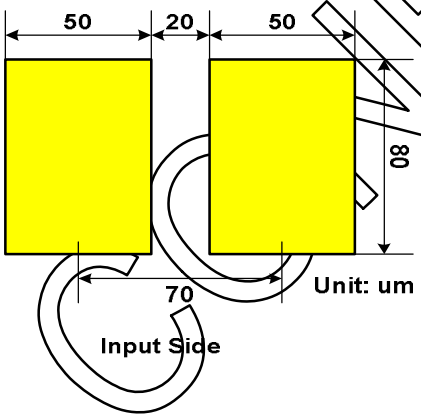
Alignment Mark:



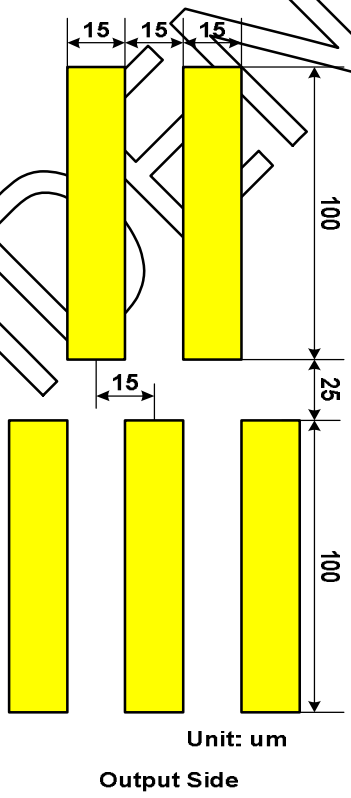


Bump Arrangment:

Input:



Output:



Coordinate:

Pad No.	Name	X-axis	Y-axis
1	VPG	-11165	-294
2	VPG	-11095	-294
3	MGND	-11025	-294
4	MGND	-10955	-294
5	TS[6]	-10885	-294
6	TS[5]	-10815	-294
7	TS[4]	-10745	-294
8	CABC_ON	-10675	-294
9	CABC_PWM	-10605	-294
10	TS[3]	-10535	-294
11	TS[2]	-10465	-294
12	TS[1]	-10395	-294
13	MLDO	-10325	-294
14	MLDO	-10255	-294
15	VCI	-10185	-294
16	DATA_N	-10115	-294
17	DATA_N	-10045	-294
18	DATA_P	-9975	-294
19	DATA_P	-9905	-294
20	STB_CLKN	-9835	-294
21	STB_CLKN	-9765	-294
22	STB_CLKP	-9695	-294
23	STB_CLKP	-9625	-294
24	TS[0]	-9555	-294
25	TESTO[7]	-9485	-294
26	TESTO[6]	-9415	-294
27	TESTO[5]	-9345	-294
28	TESTO[4]	-9275	-294
29	TESTO[3]	-9205	-294
30	TESTO[2]	-9135	-294
31	TESTO[1]	-9065	-294
32	TESTO[0]	-8995	-294
33	CABC_ON	-8925	-294
34	CABC_PWM	-8855	-294
35	IM[0]	-8785	-294
36	IM[1]	-8715	-294
37	IM[2]	-8645	-294
38	RESX	-8575	-294
39	VSYNC	-8505	-294
40	HSYNC	-8435	-294
41	DOTCLK	-8365	-294
42	ENABLE	-8295	-294
43	DB[17]	-8225	-294
44	DB[16]	-8155	-294
45	DB[15]	-8085	-294
46	DB[14]	-8015	-294
47	DB[13]	-7945	-294
48	DB[12]	-7875	-294
49	DB[11]	-7805	-294
50	DB[10]	-7735	-294
51	DB[9]	-7665	-294
52	DB[8]	-7595	-294
53	DB[7]	-7525	-294
54	DB[6]	-7455	-294
55	DB[5]	-7385	-294
56	DB[4]	-7315	-294
57	DB[3]	-7245	-294
58	DB[2]	-7175	-294
59	DB[1]	-7105	-294
60	DB[0]	-7035	-294
61	DOUT	-6965	-294
62	DIN_SDA	-6895	-294
63	RDX	-6825	-294
64	WRX_SCL	-6755	-294
65	DCX	-6685	-294
66	CSX	-6615	-294
67	TE	-6545	-294
68	IOVCC	-6475	-294
69	IOVCC	-6405	-294
70	IOVCC	-6335	-294
71	IOVCC	-6265	-294
72	IOVCC	-6195	-294
73	IOVCC	-6125	-294
74	IOVCC	-6055	-294
75	DVDD	-5985	-294
76	DVDD	-5915	-294
77	DVDD	-5845	-294
78	DVDD	-5775	-294
79	DVDD	-5705	-294
80	DVDD	-5635	-294
81	DVDD	-5565	-294
82	DVDD	-5495	-294
83	DVDD	-5425	-294
84	DVDD	-5355	-294
85	DVDD	-5285	-294
86	DGND	-5215	-294
87	DGND	-5145	-294
88	DGND	-5075	-294
89	DGND	-5005	-294
90	DGND	-4935	-294
91	DGND	-4865	-294
92	DGND	-4795	-294
93	DGND	-4725	-294
94	VGS	-4655	-294
95	VGS	-4585	-294
96	TESTP	-4515	-294
97	AGND	-4445	-294
98	AGND	-4375	-294
99	AGND	-4305	-294
100	AGND	-4235	-294
101	AGND	-4165	-294
102	AGND	-4095	-294
103	AGND	-4025	-294
104	AGND	-3955	-294
105	AGND	-3885	-294
106	AGND	-3815	-294
107	VCOM	-3745	-294
108	VCOM	-3675	-294
109	VCOM	-3605	-294
110	VCOM	-3535	-294
111	VCOM	-3465	-294
112	VCOM	-3395	-294

113	VCOM	-3325	-294
114	VCOM	-3255	-294
115	VCOM	-3185	-294
116	VCOM	-3115	-294
117	VCOM	-3045	-294
118	VCOM	-2975	-294
119	VCOM	-2905	-294
120	VCOM	-2835	-294
121	VCOM	-2765	-294
122	VCOM	-2695	-294
123	VREG1OUT	-2625	-294
124	VREG1OUT	-2555	-294
125	VREG1OUT	-2485	-294
126	VREG1OUT	-2415	-294
127	VREG1OUT	-2345	-294
128	VREG1OUT	-2275	-294
129	VREG1OUT	-2205	-294
130	VREG1OUT	-2135	-294
131	VREG1OUT	-2065	-294
132	VREG1OUT	-1995	-294
133	NVREG1OUT	-1925	-294
134	NVREG1OUT	-1855	-294
135	NVREG1OUT	-1785	-294
136	NVREG1OUT	-1715	-294
137	NVREG1OUT	-1645	-294
138	NVREG1OUT	-1575	-294
139	NVREG1OUT	-1505	-294
140	VREF	-1435	-294
141	VREF	-1365	-294
142	VREF	-1295	-294
143	VREF	-1225	-294
144	VREF	-1155	-294
145	DDVDL	-1085	-294
146	DDVDL	-1015	-294
147	DDVDL	-945	-294
148	DDVDL	-875	-294
149	DDVDL	-805	-294
150	DDVDL	-735	-294
151	DDVDL	-665	-294
152	DDVDL	-595	-294
153	DDVDL	-525	-294
154	DDVDH	-455	-294
155	DDVDH	-385	-294
156	DDVDH	-315	-294
157	DDVDH	-245	-294
158	DDVDH	-175	-294
159	DDVDH	-105	-294
160	DDVDH	-35	-294
161	DDVDH	35	-294
162	DDVDH	105	-294
163	VCL	175	-294
164	VCL	245	-294
165	VCL	315	-294
166	VCL	385	-294
167	VCL	455	-294
168	VCL	525	-294
169	VCL	595	-294
170	VCL	665	-294
171	VCL	735	-294
172	VCL	805	-294
173	VCL	875	-294
174	VCI	945	-294
175	VCI	1015	-294
176	VCI	1085	-294
177	VCI	1155	-294
178	VCI	1225	-294
179	VCI	1295	-294
180	VCI	1365	-294
181	VCI	1435	-294
182	VCI	1505	-294
183	VCI	1575	-294
184	VCI	1645	-294
185	VCI	1715	-294
186	VCI	1785	-294
187	VCI	1855	-294
188	VCI	1925	-294
189	VCI	1995	-294
190	VCI	2065	-294
191	VCI	2135	-294
192	VCI	2205	-294
193	TESTN	2275	-294
194	C13B	2345	-294
195	C13B	2415	-294
196	C13B	2485	-294
197	C13B	2555	-294
198	C13B	2625	-294
199	C13B	2695	-294
200	C13B	2765	-294
201	C13B	2835	-294
202	C13B	2905	-294
203	C13B	2975	-294
204	C13B	3045	-294
205	C13A	3115	-294
206	C13A	3185	-294
207	C13A	3255	-294
208	C13A	3325	-294
209	C13A	3395	-294
210	C13A	3465	-294
211	C13A	3535	-294
212	C13A	3605	-294
213	C13A	3675	-294
214	C13A	3745	-294
215	C13A	3815	-294
216	C12B	3885	-294
217	C12B	3955	-294
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219	C12B	4095	-294
220	C12B	4165	-294
221	C12B	4235	-294
222	C12B	4305	-294
223	C12B	4375	-294
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1582	G386	-8295	149
1583	G384	-8310	274
1584	G382	-8325	149
1585	G380	-8340	274
1586	G378	-8355	149
1587	G376	-8370	274
1588	G374	-8385	149
1589	G372	-8400	274
1590	G370	-8415	149
1591	G368	-8430	274
1592	G366	-8445	149
1593	G364	-8460	274
1594	G362	-8475	149

1595	G360	-8490	274
1596	G358	-8505	149
1597	G356	-8520	274
1598	G354	-8535	149
1599	G352	-8550	274
1600	G350	-8565	149
1601	G348	-8580	274
1602	G346	-8595	149
1603	G344	-8610	274
1604	G342	-8625	149
1605	G340	-8640	274
1606	G338	-8655	149
1607	G336	-8670	274
1608	G334	-8685	149
1609	G332	-8700	274
1610	G330	-8715	149
1611	G328	-8730	274
1612	G326	-8745	149
1613	G324	-8760	274
1614	G322	-8775	149
1615	G320	-8790	274
1616	G318	-8805	149
1617	G316	-8820	274
1618	G314	-8835	149
1619	G312	-8850	274
1620	G310	-8865	149
1621	G308	-8880	274
1622	G306	-8895	149
1623	G304	-8910	274
1624	G302	-8925	149
1625	G300	-8940	274
1626	G298	-8955	149
1627	G296	-8970	274
1628	G294	-8985	149
1629	G292	-9000	274
1630	G290	-9015	149
1631	G288	-9030	274
1632	G286	-9045	149
1633	G284	-9060	274
1634	G282	-9075	149
1635	G280	-9090	274
1636	G278	-9105	149
1637	G276	-9120	274
1638	G274	-9135	149
1639	G272	-9150	274
1640	G270	-9165	149
1641	G268	-9180	274
1642	G266	-9195	149
1643	G264	-9210	274
1644	G262	-9225	149
1645	G260	-9240	274
1646	G258	-9255	149
1647	G256	-9270	274
1648	G254	-9285	149
1649	G252	-9300	274
1650	G250	-9315	149
1651	G248	-9330	274
1652	G246	-9345	149
1653	G244	-9360	274
1654	G242	-9375	149
1655	G240	-9390	274
1656	G238	-9405	149
1657	G236	-9420	274
1658	G234	-9435	149
1659	G232	-9450	274
1660	G230	-9465	149
1661	G228	-9480	274
1662	G226	-9495	149
1663	G224	-9510	274
1664	G222	-9525	149
1665	G220	-9540	274
1666	G218	-9555	149
1667	G216	-9570	274
1668	G214	-9585	149
1669	G212	-9600	274
1670	G210	-9615	149
1671	G208	-9630	274
1672	G206	-9645	149
1673	G204	-9660	274
1674	G202	-9675	149
1675	G200	-9690	274
1676	G198	-9705	149
1677	G196	-9720	274
1678	G194	-9735	149
1679	G192	-9750	274
1680	G190	-9765	149
1681	G188	-9780	274
1682	G186	-9795	149
1683	G184	-9810	274
1684	G182	-9825	149
1685	G180	-9840	274
1686	G178	-9855	149
1687	G176	-9870	274
1688	G174	-9885	149
1689	G172	-9900	274
1690	G170	-9915	149
1691	G168	-9930	274
1692	G166	-9945	149
1693	G164	-9960	274
1694	G162	-9975	149
1695	G160	-9990	274
1696	G158	-10005	149
1697	G156	-10020	274
1698	G154	-10035	149
1699	G152	-10050	274
1700	G150	-10065	149
1701	G148	-10080	274
1702	G146	-10095	149
1703	G144	-10110	274
1704	G142	-10125	149
1705	G140	-10140	274
1706	G138	-10155	149
1707	G136	-10170	274
1708	G134	-10185	149

1709	G132	-10200	274
1710	G130	-10215	149
1711	G128	-10230	274
1712	G126	-10245	149
1713	G124	-10260	274
1714	G122	-10275	149
1715	G120	-10290	274
1716	G118	-10305	149
1717	G116	-10320	274
1718	G114	-10335	149
1719	G112	-10350	274
1720	G110	-10365	149
1721	G108	-10380	274
1722	G106	-10395	149
1723	G104	-10410	274
1724	G102	-10425	149
1725	G100	-10440	274
1726	G98	-10455	149
1727	G96	-10470	274
1728	G94	-10485	149
1729	G92	-10500	274
1730	G90	-10515	149
1731	G88	-10530	274
1732	G86	-10545	149
1733	G84	-10560	274
1734	G82	-10575	149
1735	G80	-10590	274
1736	G78	-10605	149
1737	G76	-10620	274
1738	G74	-10635	149
1739	G72	-10650	274
1740	G70	-10665	149
1741	G68	-10680	274
1742	G66	-10695	149
1743	G64	-10710	274
1744	G62	-10725	149
1745	G60	-10740	274
1746	G58	-10755	149
1747	G56	-10770	274
1748	G54	-10785	149
1749	G52	-10800	274
1750	G50	-10815	149
1751	G48	-10830	274
1752	G46	-10845	149
1753	G44	-10860	274
1754	G42	-10875	149
1755	G40	-10890	274
1756	G38	-10905	149
1757	G36	-10920	274
1758	G34	-10935	149
1759	G32	-10950	274
1760	G30	-10965	149
1761	G28	-10980	274
1762	G26	-10995	149
1763	G24	-11010	274
1764	G22	-11025	149
1765	G20	-11040	274
1766	G18	-11055	149
1767	G16	-11070	274
1768	G14	-11085	149
1769	G12	-11100	274
1770	G10	-11115	149
1771	G8	-11130	274
1772	G6	-11145	149
1773	G4	-11160	274
1774	G2	-11175	149
1775	DUMMY19	-11190	274
1776	DUMMY20	-11205	149

	X-axis (um)	Y-axis (um)
Chip Size	22770	880
R-ALMARK	11300	-285
L-ALMARK	-11300	-285
Input Side-Bump	50	80
Output Side-Bump	15	100

6. Block Function Description

Interface

The RM68140 supplies four kinds of MCU system interface with 8080-series parallel interface, 3-/4-line serial interface, MIPI DSI interface and MDDI interface.

The RM68140 has index register (IR) to store index information from control registers and the internal GRAM. The write data register (WDR) used to temporarily store data to be written to control registers and the internal GRAM. The read data register (RDR) used to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the RM68140 read the first data from the internal GRAM. Valid data are read out after the RM68140 performs the second read operation.

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CR, the data is transferred from CR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or –1 automatically. AC after data is read out increments by +1 or –1 likewise. The RM68140 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 345,600 bytes pattern data using 18 bits for one pixel, enabling maximum 320RGB x 480 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a TFT-LCD drive voltage, which corresponds to grayscale level set in the γ correction register. The RM68140 displays 262k colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to TFT-LCD panel, VREG1OUT, VGH, VGL and VCOM.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The

timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The RM68140 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The TFT-LCD display driver circuit consists of 960 source drivers (S1~S960). Display pattern data is latched when 960 data is input. This latched data controls source drivers and outputs drive waveform. The shift direction of 960-dot output from the source driver can be changed by setting commands. The gate signal consists from G1 to G480.

7. Function Description

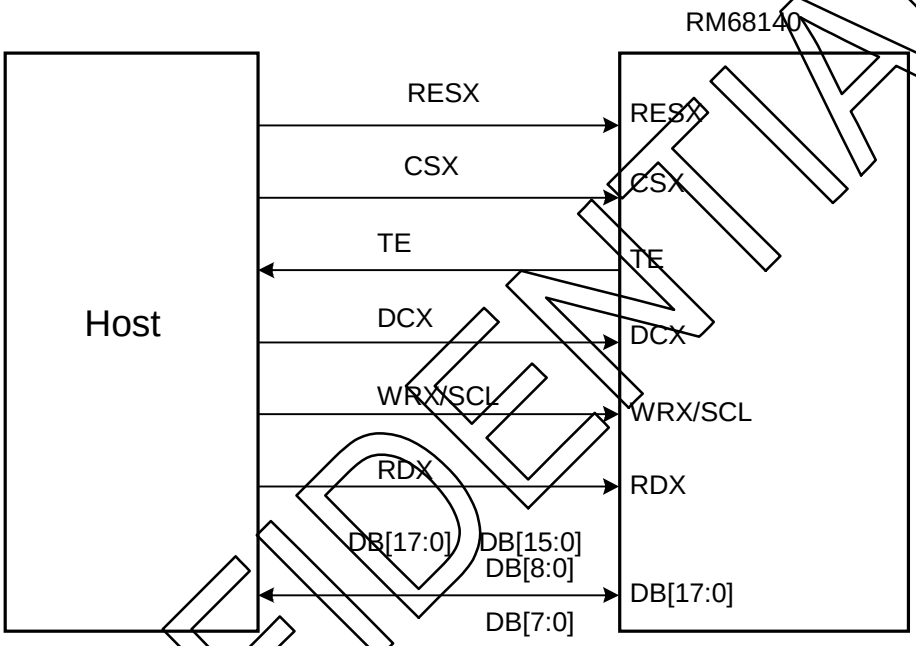
7.1 Interface Type Selection

The selection of a given interfaces are done by setting IM2, IM1 and IM0 pins as show below.

IM[2:0]	Display Data	Command
000	80-series 18-bit MPU I/F, D[17:0]	80-series 18-bit MPU I/F, D[17:0]
001	80-series 9-bit MPU I/F, D[8:0]	80-series 9-bit MPU I/F, D[8:0]
010	80-series 16-bit MPU I/F, D[15:0]	80-series 16-bit MPU I/F, D[15:0]
011	80-series 8-bit MPU I/F, D[7:0]	80-series 8-bit MPU I/F, D[7:0]
100	MDDI	MDDI, HSSI_D0_P/N, HSSI_D1_P/N ,3-wire SPI SDI/SDO
101	3 wire SPI	3 wire SPI SDI/SDO
110	MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI,HSSI_D0_P/N,HSSI_D1_P/N (Video Mode)
111	4 wire SPI	4 wire SPI SDI/SDO

7.2 Display Bus Interface (DBI)

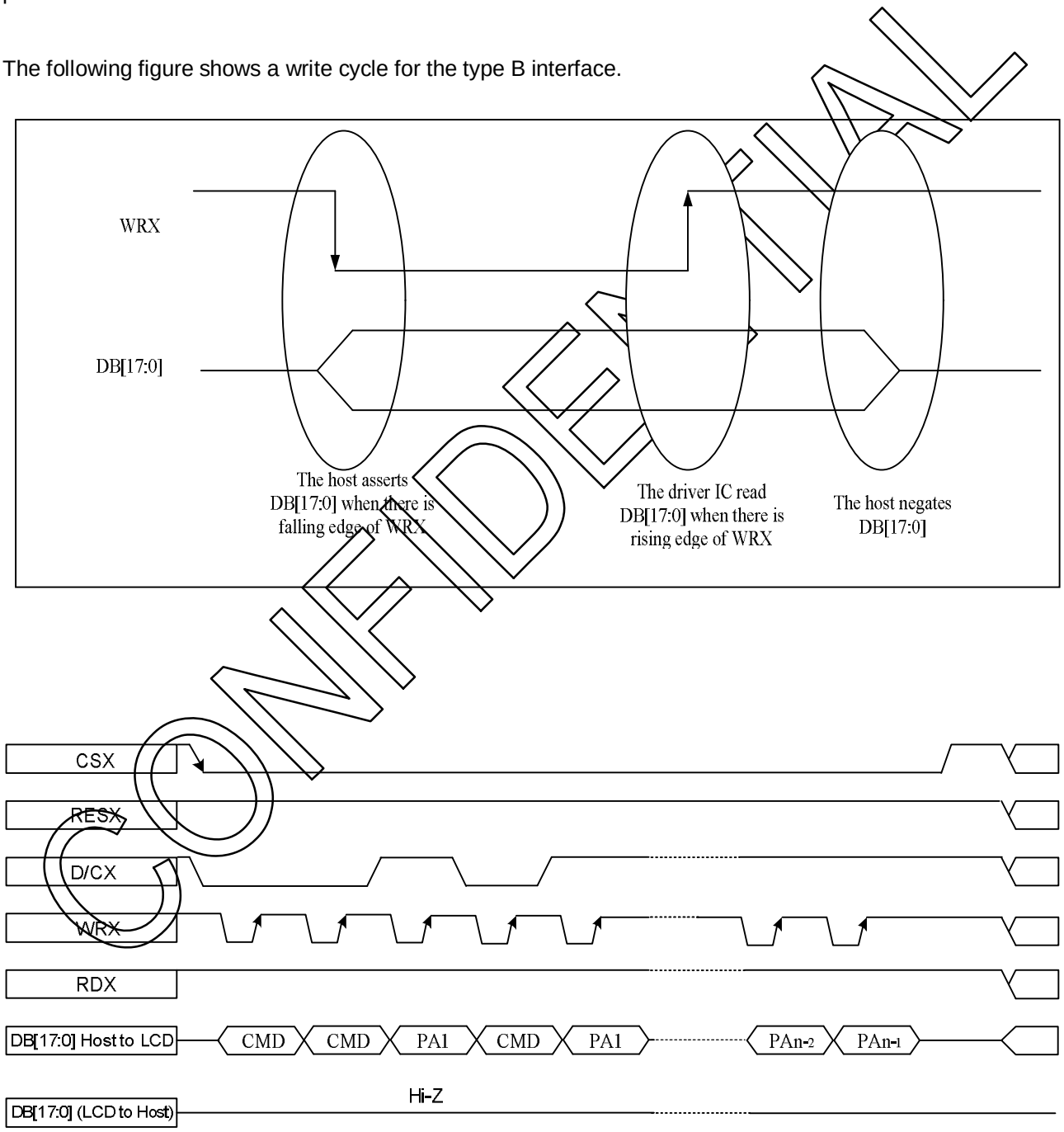
The RM68140 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and DB[17:0] is parallel DBI data. There are four 18/16/9/8-bit types interface supported for the display data transfer. The graphics controller chip reads the data at the rising edge of RDX signal. The DCX is data/command flag. When DCX = "1", D17 to D0 bits are display RAM data or command parameters. When DCX = "0", D7 to D0 bits are commands.



7.2.1 Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (DB[17:0]). WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. DCX is driven low while command information is on the interface and is pulled high when data is present.

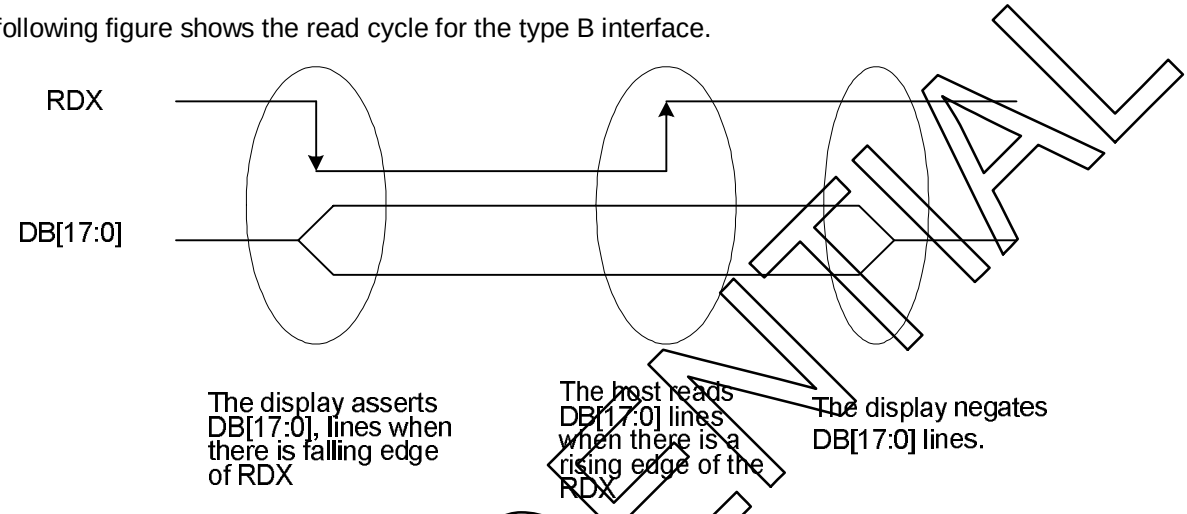
The following figure shows a write cycle for the type B interface.



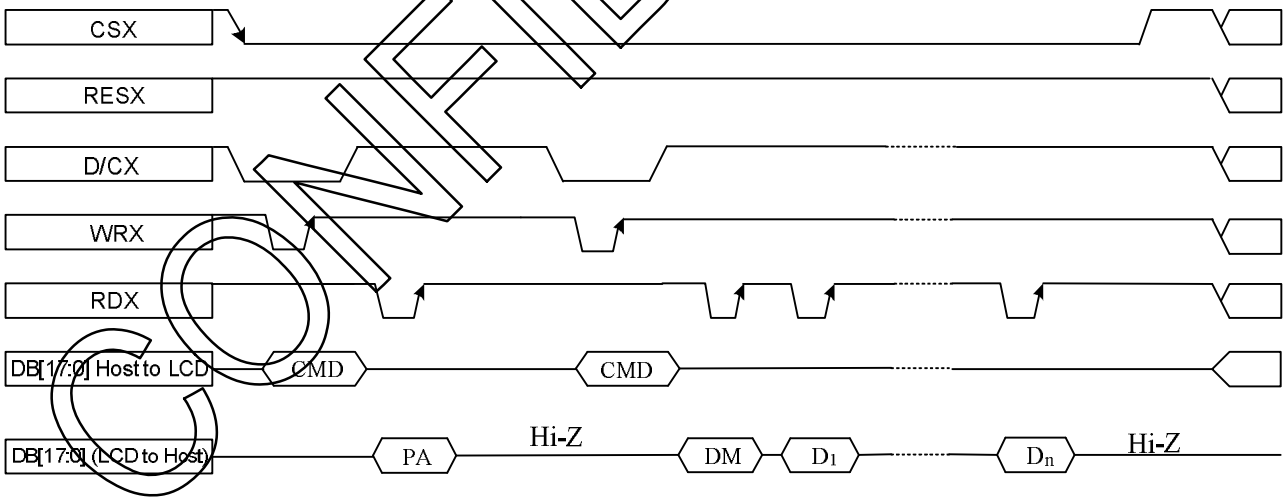
7.2.2 Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (D[17:0]). RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. DCX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the DCX input is pulled high. If DCX is driven low during read then the display information outputs will be High-Z.

DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000,

	IFPF	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Read	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	262k

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	IFPF	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Write	5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	65K
	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			262K
		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			
		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	IFPF	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Write	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	262 K
		G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

8-bit data bus DB[7:0] interface, IM[2:0] = 011

	IFPF	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Write	5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	65K
		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	
	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	X	X	262K
		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	X	X	
		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	X	X	

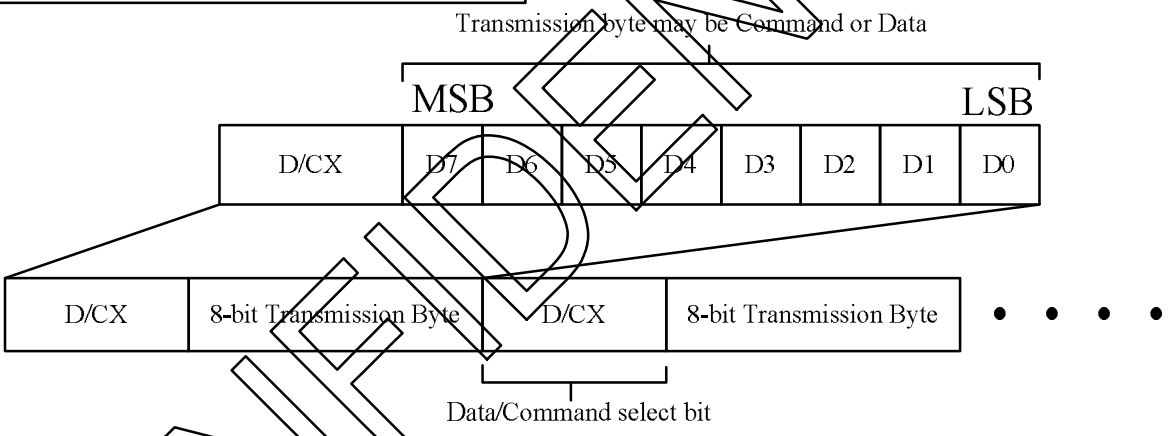
7.3 Serial Interface

7.3.1 Write Cycle and Sequence

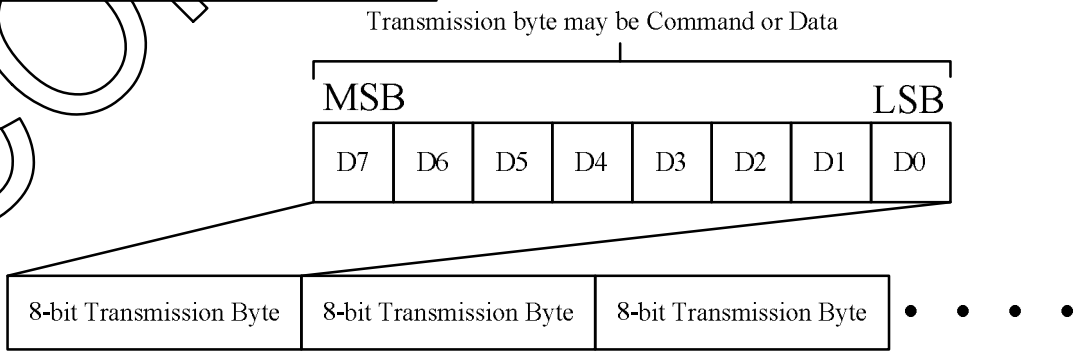
The write mode of the interface means the host writes commands and data to RM68140. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the RM68140 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-/4-line serial interface.

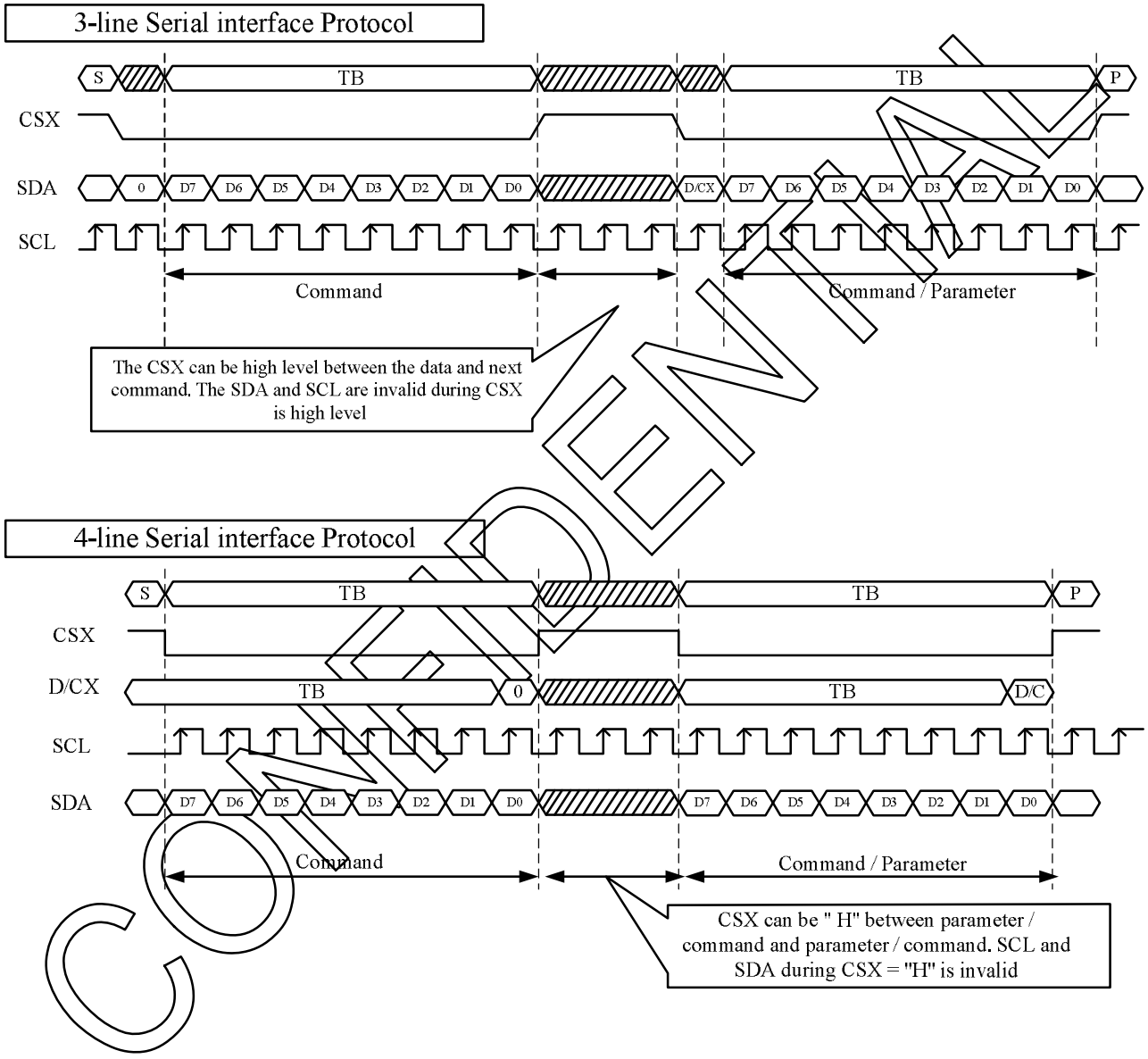
Data Format for 3-line Serial interface



Data Format for 4-line Serial interface



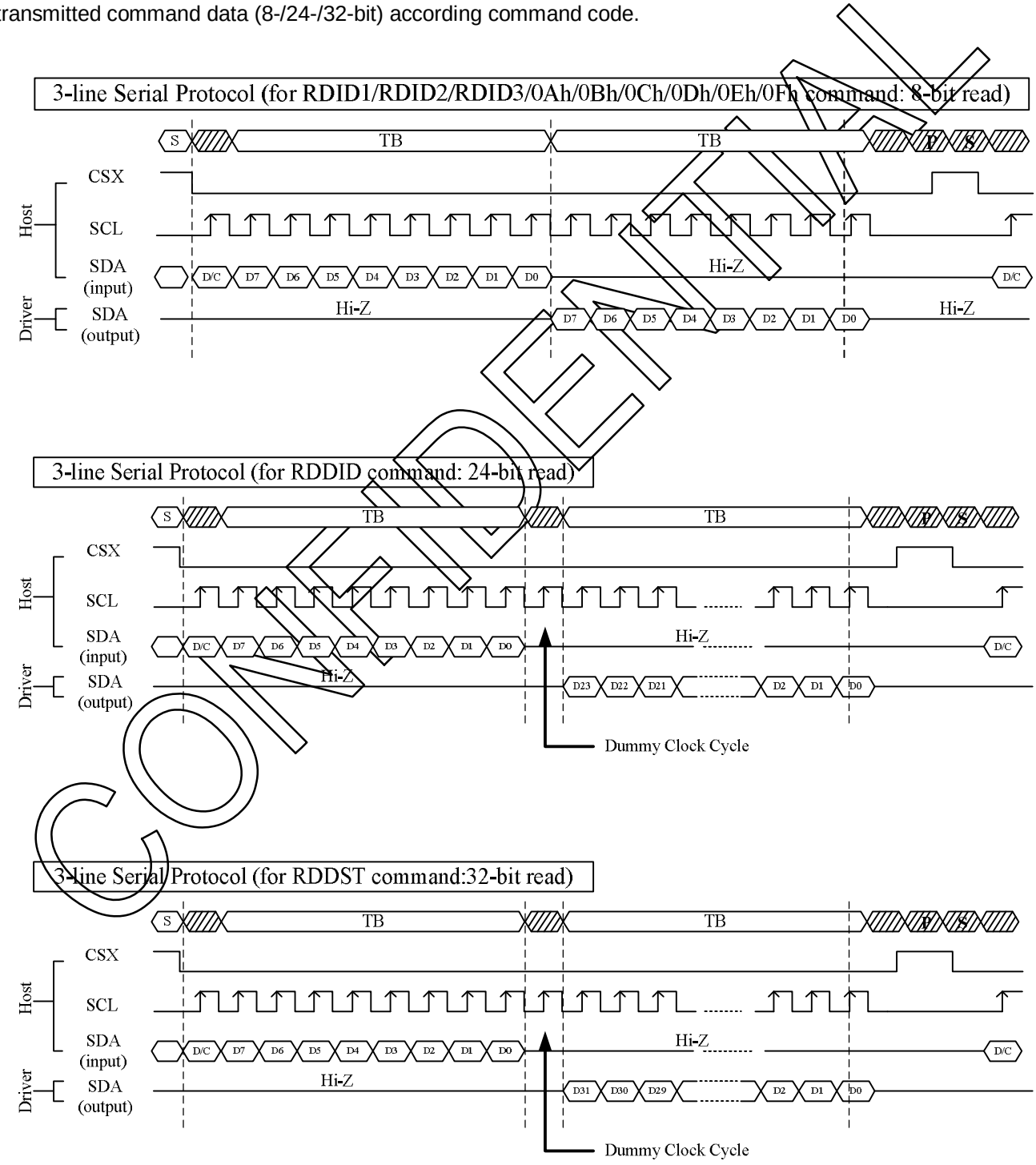
The host drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by RM68140 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host.On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eightread cycle long. The 3/4-line serial interface writes sequence described in the Figure as below.



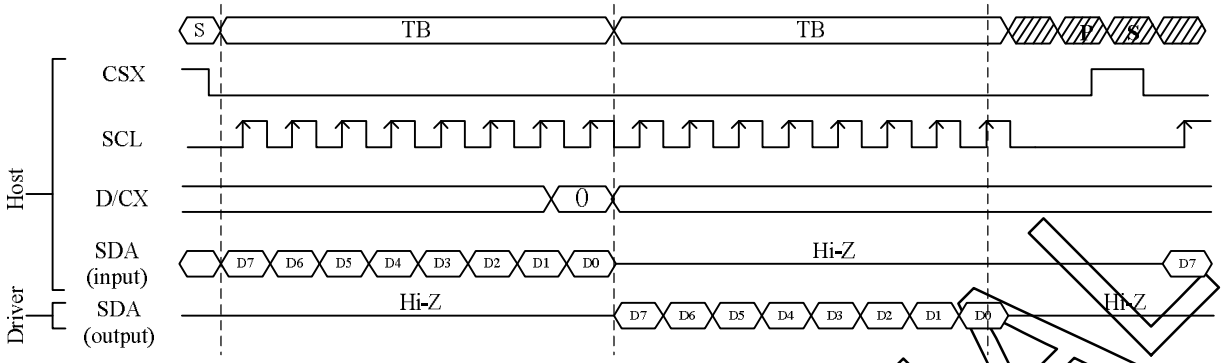
7.3.2 Read Cycle and Sequence

The read mode of the interface means that the host reads register value from RM68140. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction.

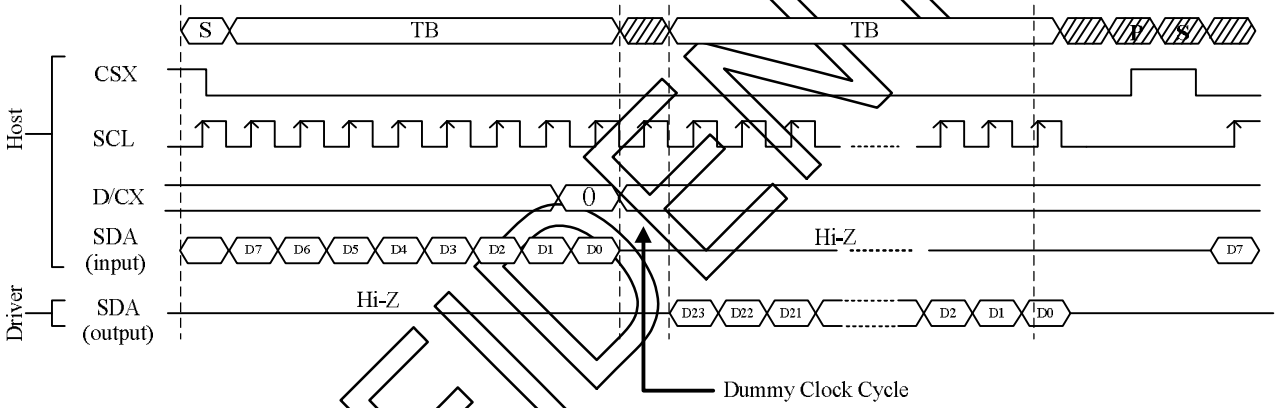
The RM68140 samples the SDA (input data) at the rising edges of SCL (serial clock), but shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.



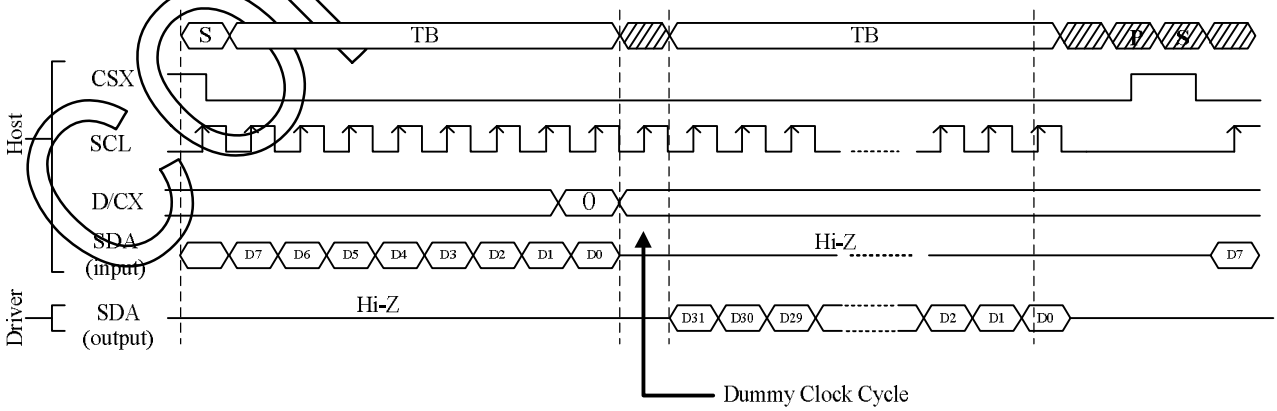
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command:24-bit read)



4-line Serial Protocol (for RDDST command:32-bit read)

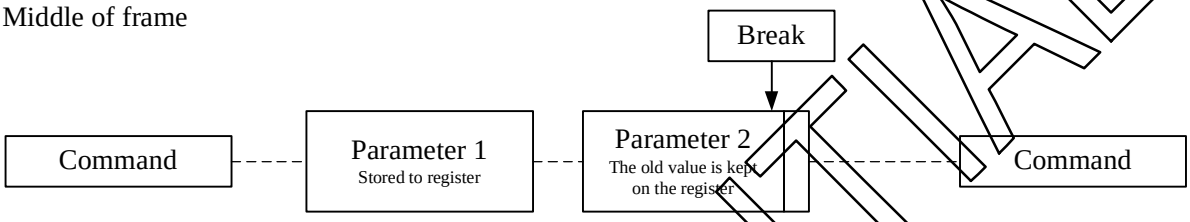


7.3.3 Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

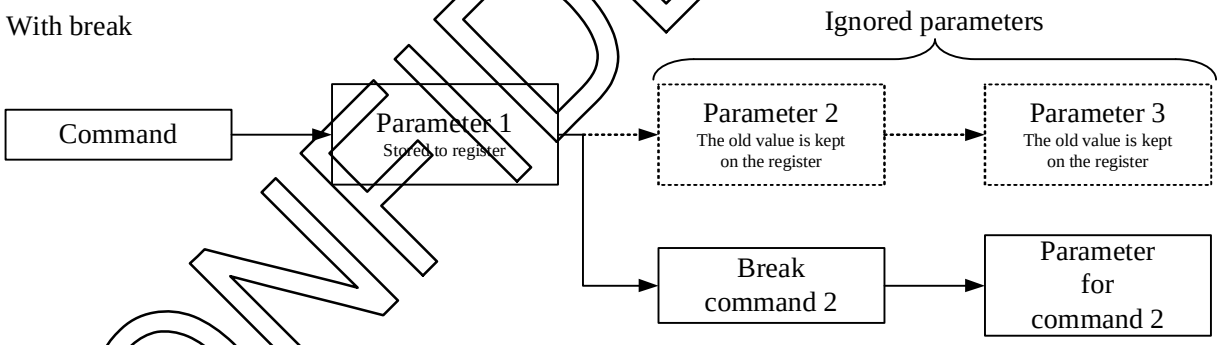
1. Middle of frame



1. Between frames

Without break

With break



Break can be e.g. another command or noise pulse.

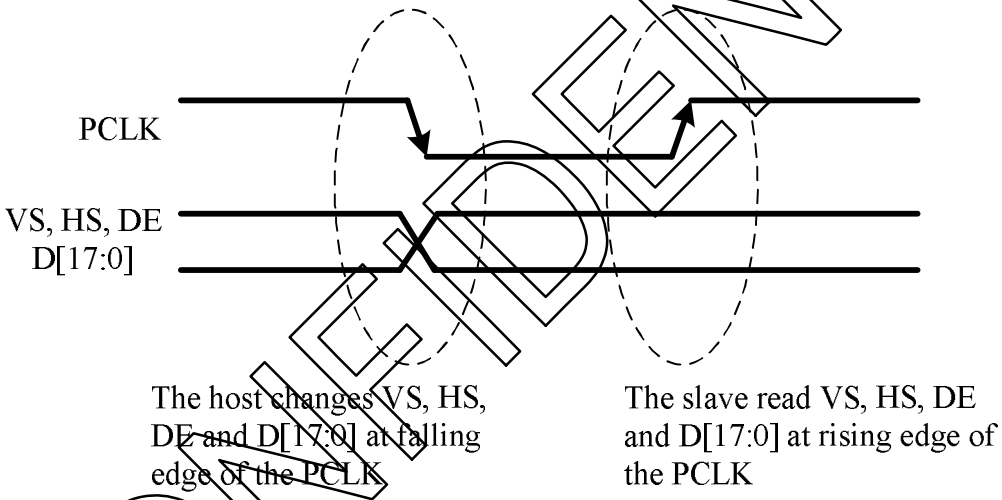
7.4 Display Pixel Interface (DPI)

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image. Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16, 18 bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

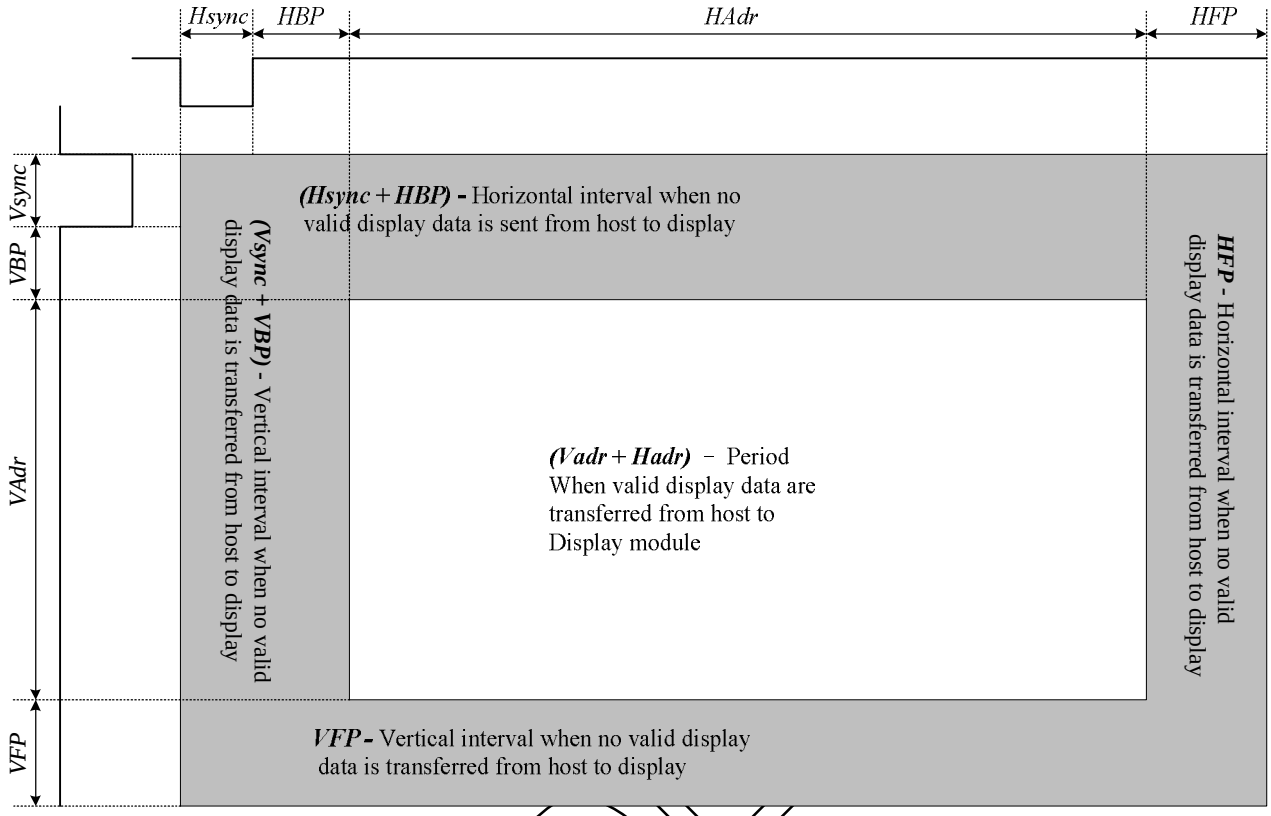
DPI signals are described in the follow figure.

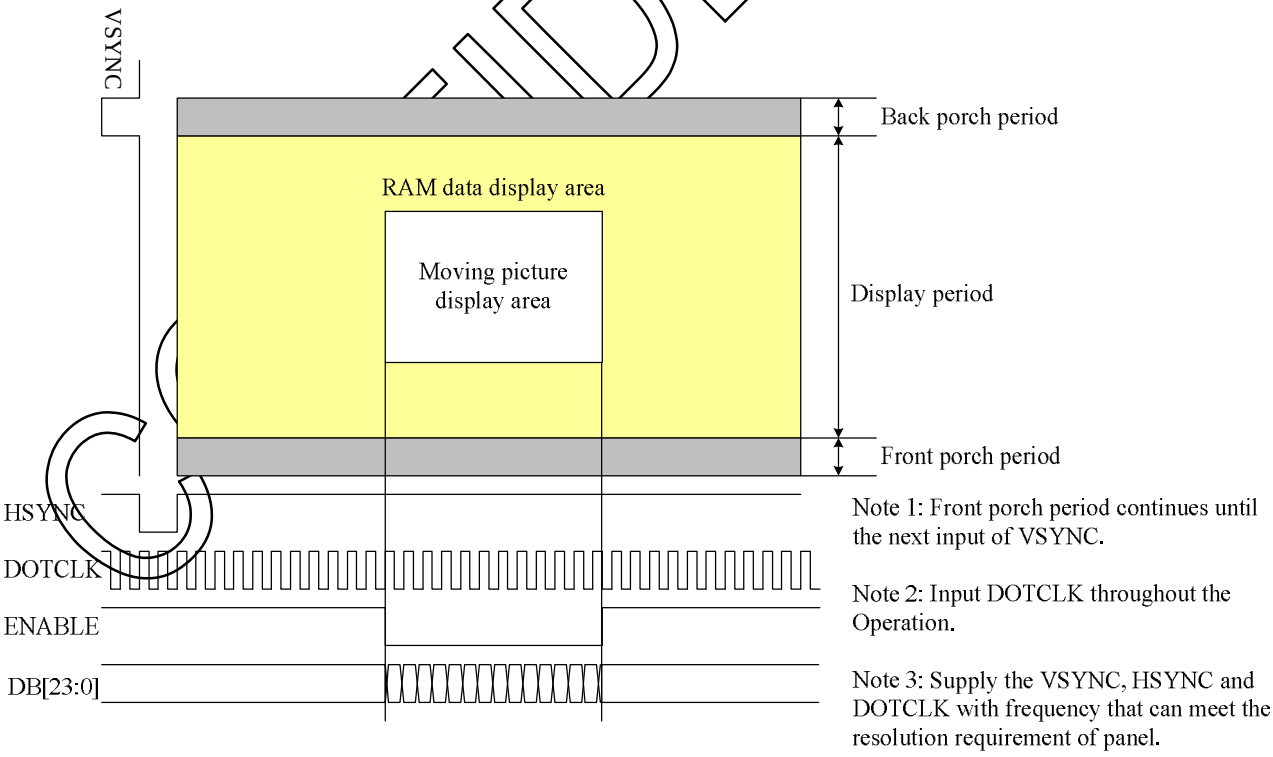


DPI Interface data bus format: (Selected by VIPF[2:0])

	VIPF	DFM	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory write	5	0			R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	65K
	6	0	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	262K

DPI Interface Timing Chart.





Note 1: Front porch period continues until the next input of VSYNC.

Note 2: Input DOTCLK throughout the Operation.

Note 3: Supply the VSYNC, HSYNC and DOTCLK with frequency that can meet the resolution requirement of panel.

7.5 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

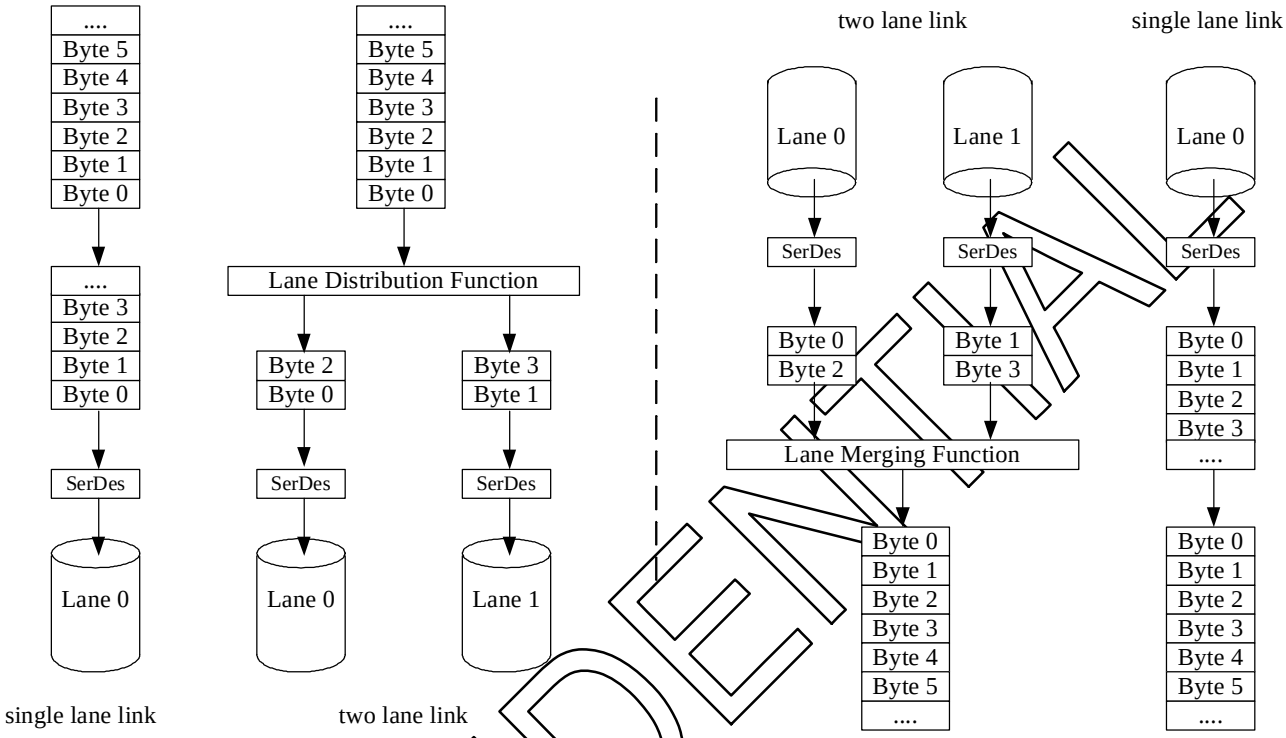
RM68140 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. RM68140 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM68140 Configuration:

Lane Pair	MCU(Master)　RM68140(Slave)
Clock Lane	Unidirectional Lane Clock only
Data Lane 0	Bi-directional Lane Ø Forward High-speed Ø Bi-directional Escape Mode Ø Bi-directional LPDT

7.5.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.



There are two kinds of packets, **short packet and long packet**.

Ø Short packet structure:

LP-11: low power mode

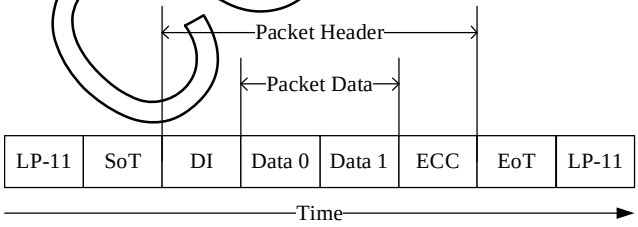
SoT: start of transmission

DI: data identification

Data 0, Data1: packet data

ECC: error correction code

EoT: End of Transmission



DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Ø Long packet structure:

LP-11: low power mode

SoT: start of transmission

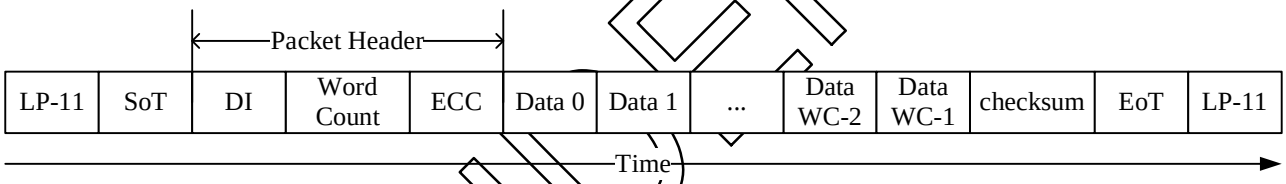
DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission



7.5.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Ø Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

Ø EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall system reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM68140 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Ø Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Ø Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

Ø DCS commands

- **n** DCS short write command

  DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

- **n** DCS read commands

  The commands are used to request data from s display module.

- **n** DCS Long Write / write_LUT command

  The commands are used to send larger blocks of data to a display module.

- **n** Maximum return packet size

  This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

n Null Packet

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

n Blanking Packet

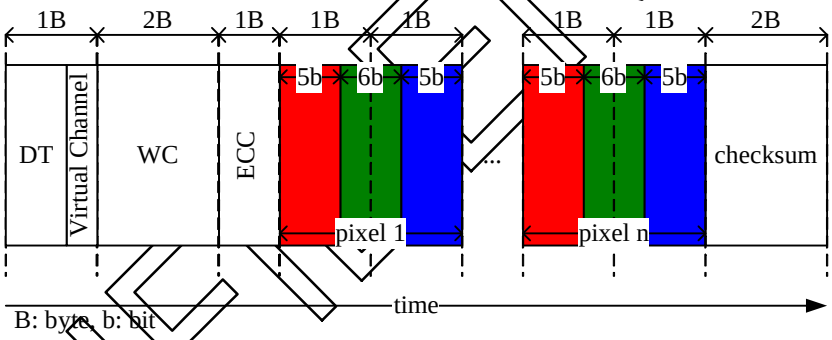
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

n Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

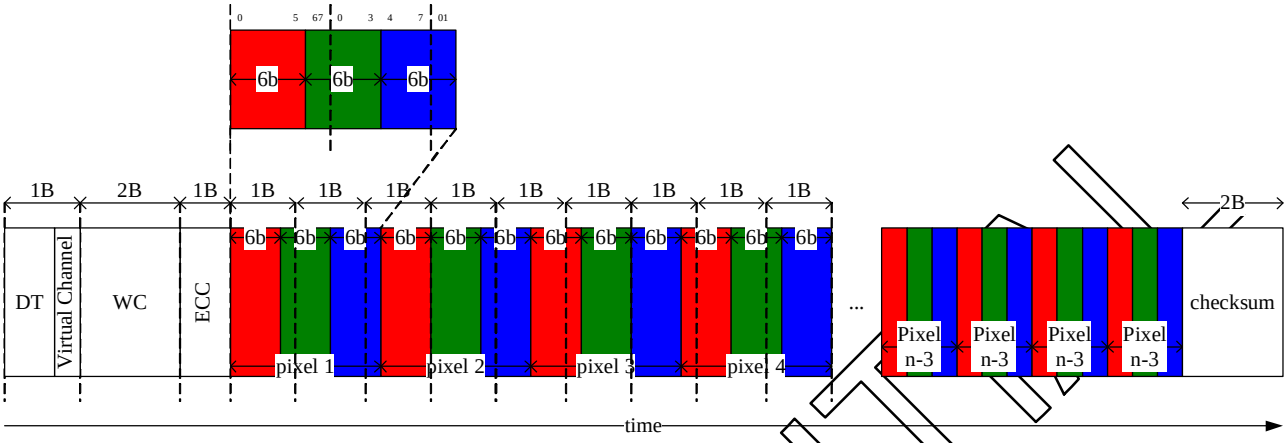
n Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



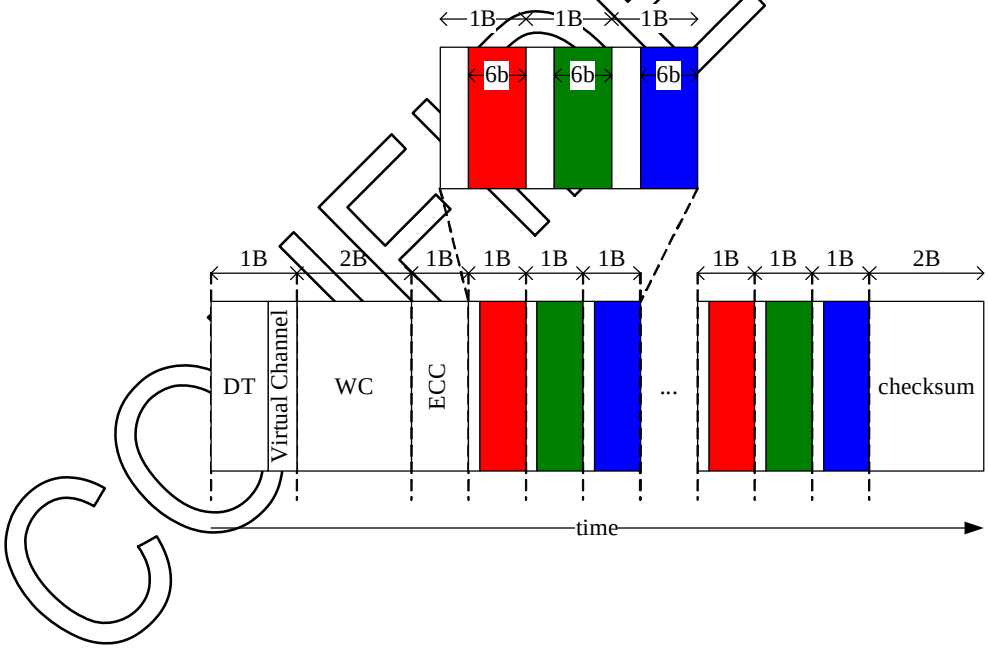
n Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



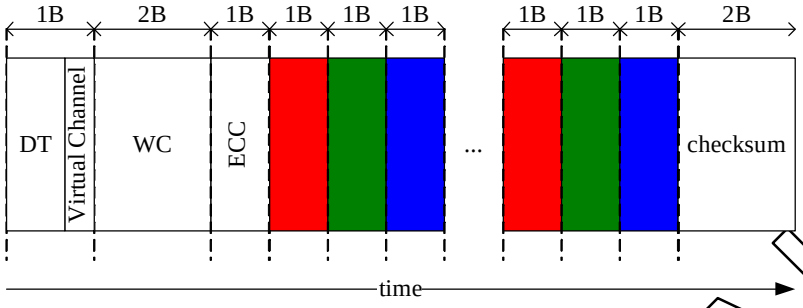
n Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.



n Packet pixel stream, 24-bit format, Data Type: 11 1110

The pixel format is eight bits red, eight bits green and eight bits blue.



7.5.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission. Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

- Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.
- Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.
- Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.
- Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.
- Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.
- Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.
- Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.
- Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.
- Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.
- Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error

is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

- Ø Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.
- Ø Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- Ø Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- Ø DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- Ø DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

7.6 MDDI Interface

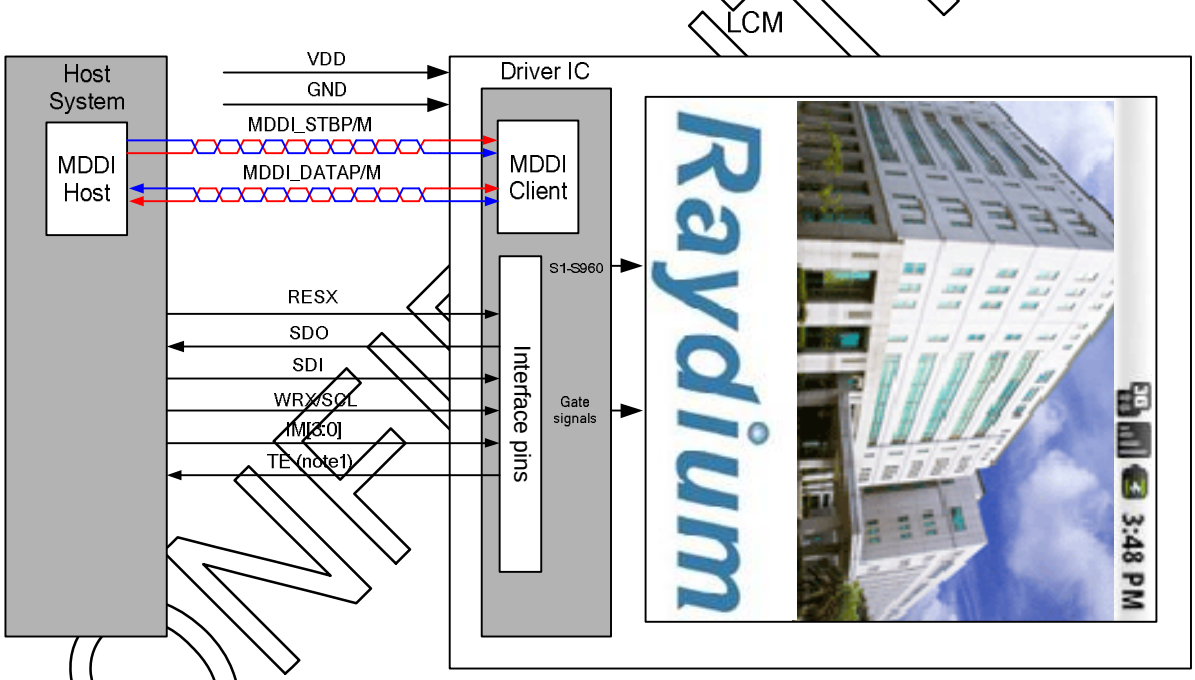
The RM68140 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following lines: DATA0_P/M and STB_P/M.

The specifications of MDDI supported by the RM68140 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA).

The RM68140 offers the bi-direction link to use for the register and display data read / write.

For power saving, the RM68140 offers both hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption.

The RM68140 supports the MDDI Type-I of the MDDI specifications Version 1.2 and the application diagram is illustrated as follow.



Notes:

1. Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effect.
2. When enter to the MDDI interface from other interface, the Host needs to wait 100ms and can start to send any packet. For example wake up packet.
3. After shutting down the MDDI interface the Host needs to wait 500ns and can start to send wake up packet to wake up the MDDI link.
4. The terminal resistors are embedded between MDDI_DATA0_P/M and MDDI_STB_P/M.

7.6.1 MDDI Link Protocol

The RM68140's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol.

DO NOT send any packets that are not supported by the RM68140 into a system containing the RM68140.

Supported MDDI packets are as follows:

RM68140 MDDI packets	Packet Name	Packet Type	Direction	Supported Type
Link Control Packet	Sub-frame header packet	15359 (0x3BFF)	Forward	Type I
	Filler packet	0	Forward/Reverse	Type I
	Link Shutdown packet	69 (0x45)	Forward	Type I
	Reverse link encapsulation packet	65 (0x41)	Forward	Type I
	Round-trip delay measurement packet	82 (0x52)	Forward	Type I
Client Status and Control Packet	Client capability packet	66 (0x42)	Reverse	Type I
	Client request and status packet	70 (0x46)	Reverse	Type I
	Register access packet	146 (0x92)	Forward/Reverse	Type I
Basic Media Stream Packet	Video stream packet	16 (0x10)	Forward	Type I
	Flexible video stream packet	20 (0x14)	Forward	Type I
	Windowless video stream packet	22 (0x16)	Forward	Type I

7.6.2 MDDI Link Packet Descriptions

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub-frame Header Packet

Packet Length	Packet Type =0x3bff	Unique word =0x005a	Reversed 1	Sub-frame Length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0x3bff

Unique Word: unique word is 0x005a

Reserved 1: not used (set to zero)

Sub-frame Length: specify the number of bytes per sub-frame

Protocol version: set to zero

- Bit [15:2] – Reserved for future expansion. These should be set to all zero.
- Bits[1:0] – Sub-frame operational mode

"00" – Sub-frame lengths strictly followed.

"01" – Sub-frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame length has been transmitted.

"10" – Sub-frame lengths are unlimited. No more sub-frame packets are required tobe transmitted after the first sub-Frame packet at startup.

Sub-frame Count: specify the number of sub-frame header packet

Media-frame Count: specify the number of media-frames

CRC: error check

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

Filler Packet

Packet Length	Packet Type=0	Filler Bytes (all zero recommended)	CRC
2 bytes	2 bytes	(Packet Length – 4) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0

Filler Bytes: set to zero

CRC: error check

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.

Link Shutdown Packet

Packet Length	Packet Type=69	CRC	All Zero
2 bytes	2 bytes	2 bytes	(Packet Length – 4) bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 69

CRC: error check

All Zero: set to zero (Type I: size is 16 bytes)

Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.

Reverse Link Encapsulation Packet

Packet Length	Packet Type=65	hClient ID	Reversed Link Flags	Reverse Rate Divisor	Turn-Around 1 Length	Turn-Around 2 Length
2 bytes	2 bytes	2 bytes	1 byte	1 byte	1 byte	1 byte

Parameter CRC	All Zero 1	Turn-Around 1	Reversed Data Packets	Turn-Around 2	All Zero 2
2 bytes	8 bytes	x bytes	(Packet Length –x –y -26) bytes	y bytes	8 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 65

hClient ID: set to zero

Reverse Link Flags:

- Bit 0 – 0: No packet request
  1: Host needs the Client Capability Packet
- Bit 1 – 0: No packet request
  1: Host needs the Client Request and Status Packet
- Bit [7:2] – set to zero

Reverse Rate Divisor: reverse data rate = reverse link data clock

Turn-Around 1 Length: the length of Turn-Around 1 is the forward link data rate

Turn-Around 2 Length: the length of Turn-Around 2 is determined by Round-trip delay of the link

Parameter CRC: error check

All zero: set to zero

Turn-Around 1: First turn-around period

Reverse Data Packets: A series of data packets transferred from the client to host

Turn-Around 2: The second turn-around period

Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

Round Trip Measurement Packet

Packet Length	Packet Type=82	hClient ID	Parameter CRC
2 bytes	2 bytes	2 bytes	2 byte

Guard Time 1	Measurement Period	All Zero	Guard Time 2
64 bytes	64 bytes	2 bytes	64 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 82

hCilent ID: set to zero

Parameter CRC: error check

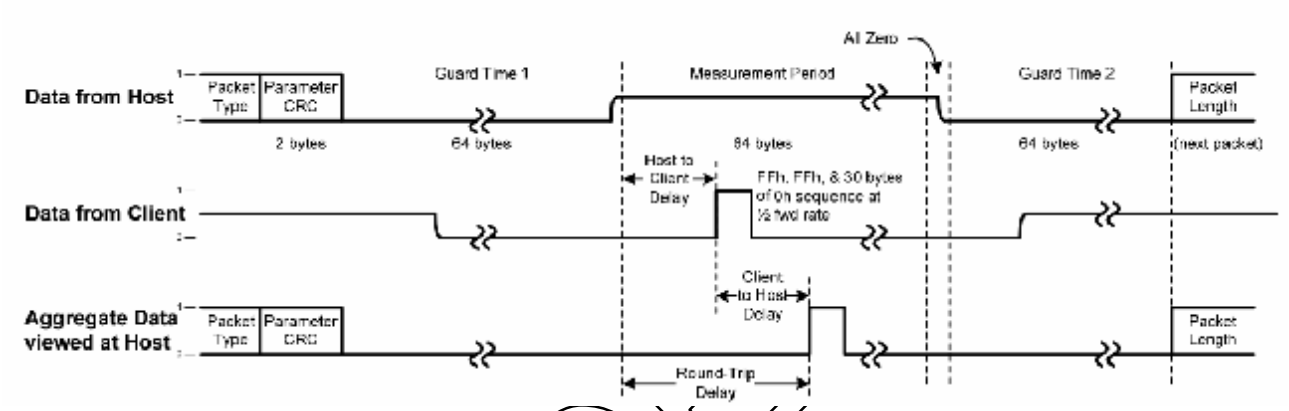
Guard Time 1: allow overlap of the host and client

Measurement Period: a 64 bytes window to allow the client to respond

All Zero: set to zero

Guard Time 2: allow overlap of the measurement period by the client

The timing of events during the Round-Trip Delay Measurement Packet illustrates as follow.



Client Capability Packet

It is recommended that the client send a Client Capability Packet to the host after forward link synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

Client Capability Packet

Packet Length	Packet Type=66	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	1 byte

Number of Alt Display	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size
1 byte	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	4 bytes

Color Map RGB Width	RGB Capability	Monochrome Capability	Reversed 1	Y Cb Cr Capability	Bayer Capability	Revered 2
2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes

Client Feature	Max Video	Min Video	Min Sub-frame Rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample

Capability	Frame Rate	Frame Rate				Rate Capability
4 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes	2 bytes

Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name
1 byte	1 byte	2 bytes	1 byte	1byte	2 bytes	2 bytes

Product Code	Reversed 3	Serial Number	Week of Mfr	Year of Mfr	CRC
2 bytes	2 bytes	4 bytes	1 byte	1 byte	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 66

cClient ID: set to zero

Protocol Version: set to 0002h

Min Protocol Version: specify the minimum protocol version (0001h)

Pre-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

Interface Type Capability: Client can function in Type I mode on the forward and reverse link (00h)

Number of Alt Displays: set to zero

Post-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

Bitmap Width: specify the width of the bitmap (140h)

Bitmap Height: specify the height of the bitmap (1E0h)

Display Window Width: specify the width of the display window (140h)

Display Window Height: specify the height of the display window (1E0h)

Color Map Size: set to zero

Color Map RGB Width: set to zero

RGB Capability: specify the resolution of RGB format (0666h)

Monochrome Capability: set to zero

Reserved 1: set to zero

Y Cb Cr Capability: set to zero

Bayer Capability: set to zero

Reserved 2: set to zero

Client Feature Capability Indicators: 00CC8000h

Maximum Video Frame Rate Capability: specify the maximum video frame (3Ch)

Minimum Video Frame Rate Capability: specify the minimum video frame (3Ch)

Minimum Sub-frame Rate: specify the minimum sub-frame rate (00h)

Audio Buffer Depth: set to zero

Audio Channel Capability: set to zero

Audio Sample Rate Capability: Set to zero

Audio Sample Resolution: set to zero

Mic Audio Sample Resolution: set to zero

Mic Sample Rate Capability: set to zero

Keyboard Data Format: set to zero

Pointing Device Data Format: set to zero

Content Protection Type: set to zero

Mfr Name: set to 0000h

Product Code: set to 6814h

Reserved 3: set to zero

Serial Number: set to zero

Week of Manufacture: set to zero

Year of Manufacture: 00h

CRC: error check

Client Request and Status Packet

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Client Request and Status Packet

Packet Length	Packet Type=70	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 bytes	2 bytes	2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 70

cClient ID: set to zero

Reverse Link Request: specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.

CRC Error Count: count the number of CRC errors occurred

Client Status:

- Bit 0 – 1: capability has changed
  0: capability has not changed
- Bit 1 – indicates the client has detected an error
- Bit [7:2] – set to zero

Client Busy Flags:

- Bit 0 – bitmap block transfer function is busy
- Bit 1 – bitmap area fill function is busy
- Bit 2 – bitmap pattern fill function is busy
- Bit 3 – the graphics subsystem is busy
- Bit [15:4] – set to zero

CRC: error check

Register Access Packet

Register Access Packet is utilized when setting instruction to the RM68140. This packet cannot be used for RAM access.

Register Access Packet

Packet Length	Packet Type=146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	(Packet Length -14) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 146

bClient ID: set to zero

Read/Write Info:

Bits[15:14]	Read/Write Flags
00	Write
01	Reserved
10	Read

11	Response to read

Bit [13:0] – specifies the number of 32-bit register data list items to be transferred in the Register Data List Filed.

Register Address: upper bits shall set to zero

Parameter CRC: error check from packet length to the register address

Register Data List: written (or read) registers to (from) client

Register Data CRC: error check of the register data list

Video Stream Packet

The RM68140 supports the Video Stream Packet to transfer display data including RGB data to RAM.

Video Stream Packet

Packet Length	Packet Type=16	bClient ID	Video Data Format Desriptor	Pixel Data Attributes	X Left Edge	Y Top Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	(Packet Length -26) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 16

bClient ID: set to zero

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68140 (00C3h)

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Pixel Data Format

MDDI data byte		D7	D6	D5	D4	D3	D2	D1	D0	Color
RGB 5:6:5	Byte n	G2	G1	G0	B4	B3	B2	B1	B0	65-Color (1 pixel/ 16 bits RGB format)
	Byte n+1	R4	R3	R2	R1	R0	G5	G4	G3	
RGB 6:6:6	Byte n	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1 pixel/ 18 bits RGB format)
	Byte n+1	R3	R2	R1	R0	G5	G4	G3	G2	
	Byte n+2	B5	B4	B3	B2	B1	B0	R5	R4	

Flexible Video Stream Packet

The RM68140 supports the Flexible Video Stream Packet to transfer display data including RGB data to RAM. This allows for a reduction in the number of fields sent in an environment where one or more fields are not changing values.

Flexible Video Stream Packet

Packet Length	Packet Type=20	bClient ID	Field Present Flags	Video Data Format Description	Pixel Data Attributes	X Left Edge	Y Top Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	Packet Length – present header bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 20

bClient ID: set to zero

Field Present Flags: indicates the field in the packet is present (value “1”) or not present (value “0”).

- Bit 0: indicates the presence of the Video Data Format Description Field.
- Bit 1: indicates the presence of the Pixel Data Attributes Field.
- Bit 2: indicates the presence of the X Left Edge Field.

- Bit 3: indicates the presence of the Y Top Edge Field.
- Bit 4: indicates the presence of the X Right Edge Field.
- Bit 5: indicates the presence of the Y Bottom Edge Field.
- Bit 6: indicates the presence of the X Start Field.
- Bit 7: indicates the presence of the Y Start Field.
- Bit 8: indicates the presence of the Pixel Count Field.
- Bits [15:9] are all “0”.

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68140 (00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Windowless Video Stream Packet

The RM68140 supports the Windowless Video Stream Packet to transfer display data including RGB data to RAM. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information.

Windowless Video Stream Packet

Packet Length	Packet Type=22	bClient ID	Video Data Format	Pixel Data	Pixel Count	Parameter CRC

			Description	Attributes		
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

Pixel Data	Pixel Data CRC
Packet Length – 14 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 22

bClient ID: set to zero

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68140 (00C3h)

Pixel Count: specify the number of pixels

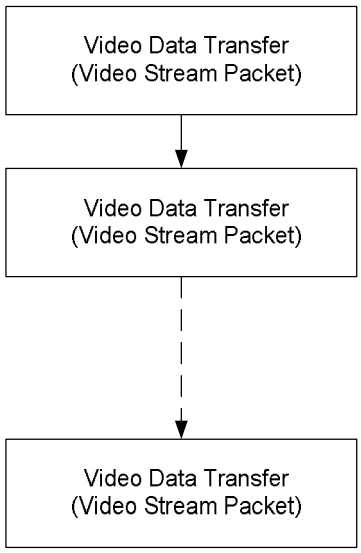
Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

7.6.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.

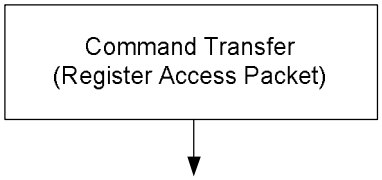


Writing Video Data to Memory Sequence

7.6.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.

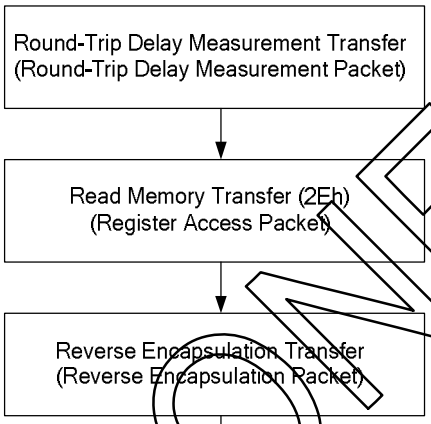
Writing Register Sequence:



7.6.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2Eh) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Video Data from Memory Sequence:



Notes:

1. X addresses for memory data read is set by 2Ah (XS[15:0]).

The parameters of 2Ah are stored on relative registers while command 2Ah is executed completely. See also section “6.1 User Command Set” and Note 2.

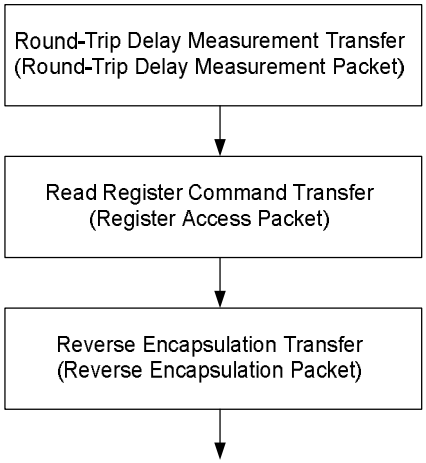
2. Y addresses for memory data read is set by 2Bh (YS[15:0]).

The parameters of 2Bh are stored on relative registers while command 2Bh is executed completely. See also section “6.1 User Command Set” and Note 2.

7.6.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Register Sequence:



7.6.7 Hibernation Setting

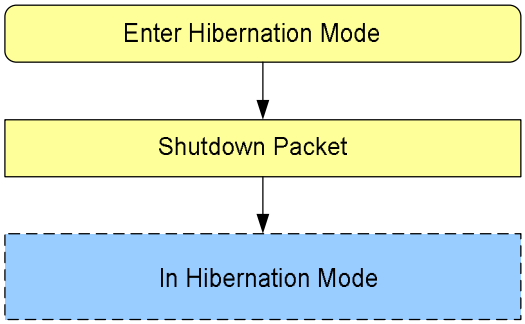
The Client MDDI of the RM68140 provides a hibernation setting. The methods for waking up the hibernation mode can be determined based on actual usage.

Wake-up	Condition
Host-Initiated Wake-up	Wake up the MDDI link by MDDI Host

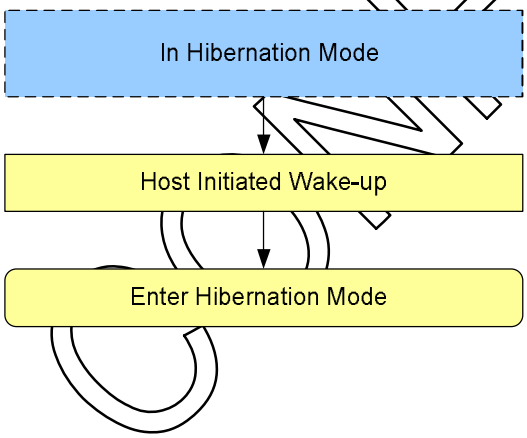
Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained.

Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

Hibernation setting sequence



Hibernation Wake-up sequence



7.6.8 MDDI Deep Standby Mode Setting

The Client MDDI of the RM68140 includes a MDDI deep standby mode setting so it can enter a off state and reduce power consumption during Hibernation mode.

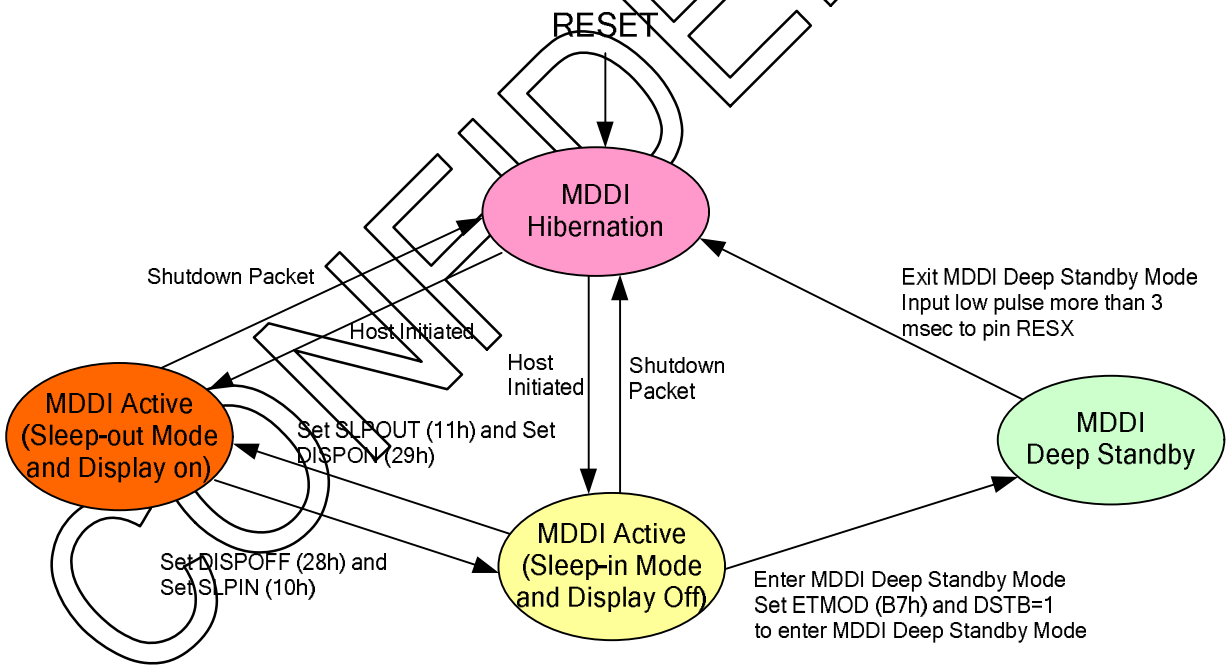
The MDDI enters Hibernation mode when a Shutdown Packet is sent. The standby power needs of the Client MDDI can be reduced, even while the MDDI Link is maintained in Hibernation mode.

When entering MDDI deep standby mode, the RM68140 stops operation rather than maintaining Hibernation mode. Input low pulse 3 msec from RESX pin to cancel deep standby mode, after which a Host-Initiated Wake-up should cancel the Hibernation mode.

When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

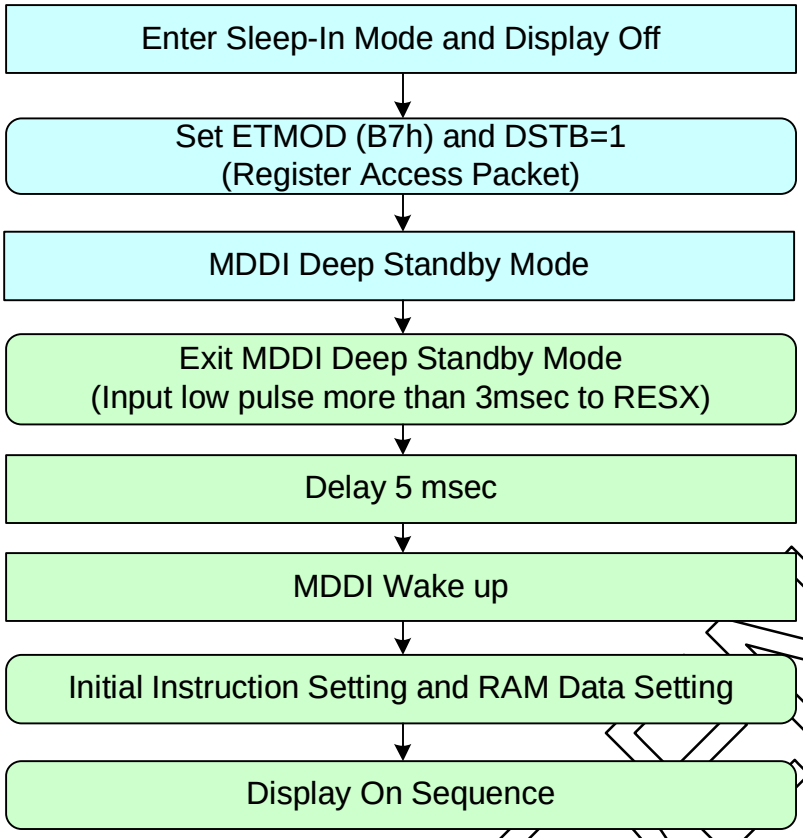
Follow the sequence indicated in the VESA MDDI specifications when initiating or canceling the Hibernation mode.

State Transitions in MDDI Deep Standby Mode:



Note: When the RM68140 is in the MDDI Hibernation mode or MDDI deep standby mode, both links are in the link hibernation states.

MDDI Deep Standby Mode Sequence

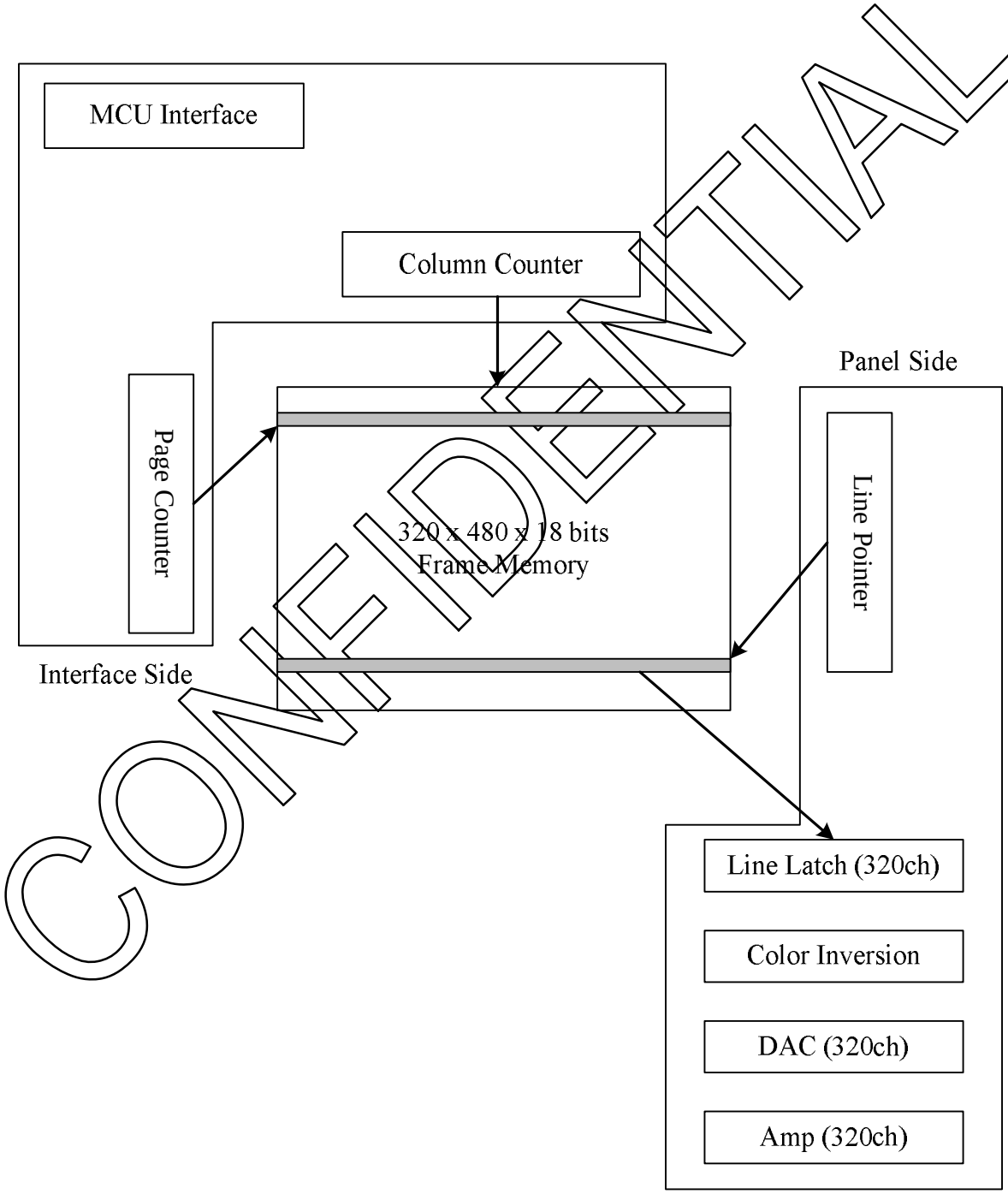


Note: When in MDDI Deep Standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

7.7 Display Data RAM

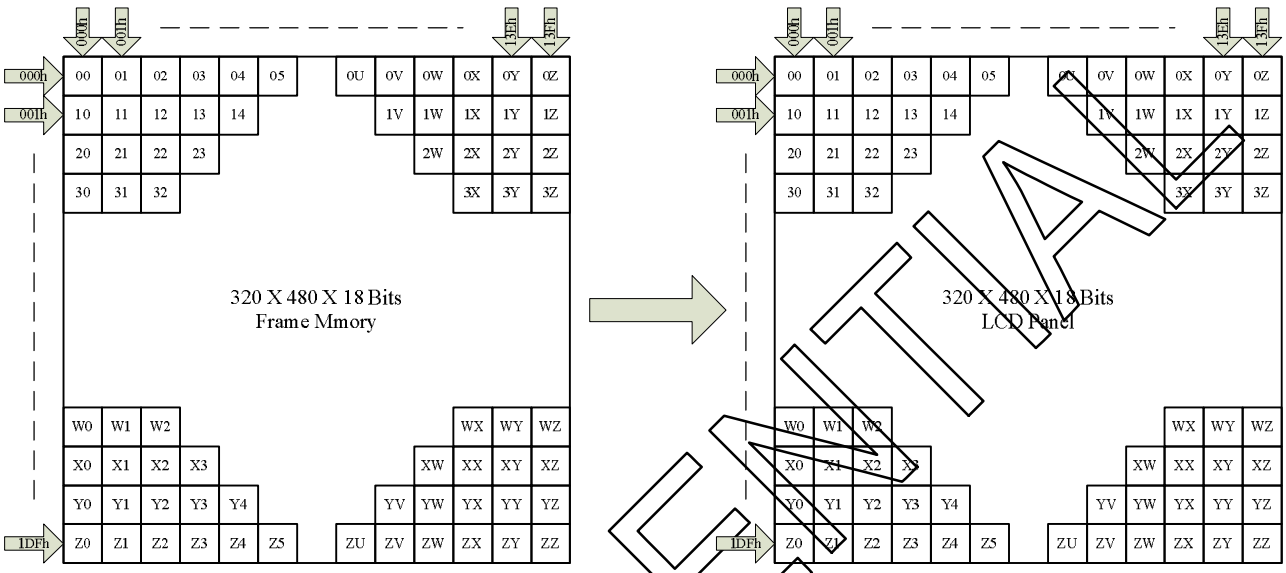
7.7.1 Configuration

The display data RAM stores display dots and consists of 2,764,800bits (320 x 18 x 480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



7.7.2 Memory to Display Address Mapping

In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

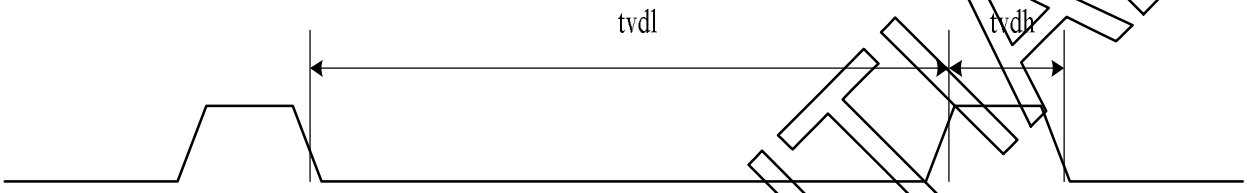


7.8 Tearing Effect Output

The tearing effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

7.8.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:

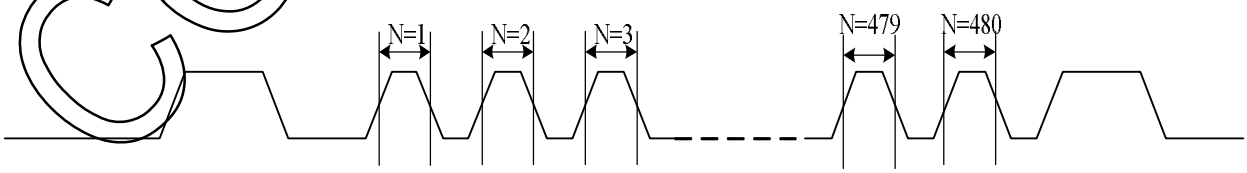


tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

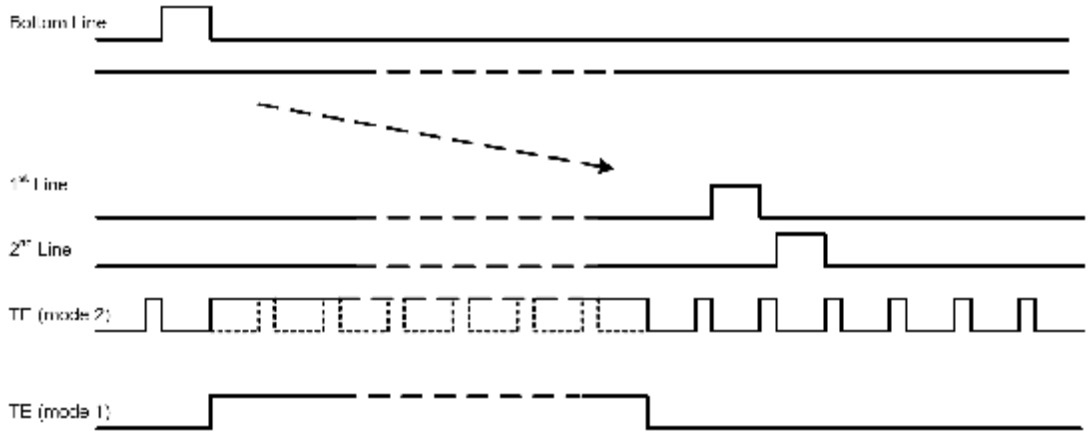
Mode 2, the tearing effect output signal consist of V-sync and H-sync information:

thdh = The LCD display is not updated from the frame memory.
thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



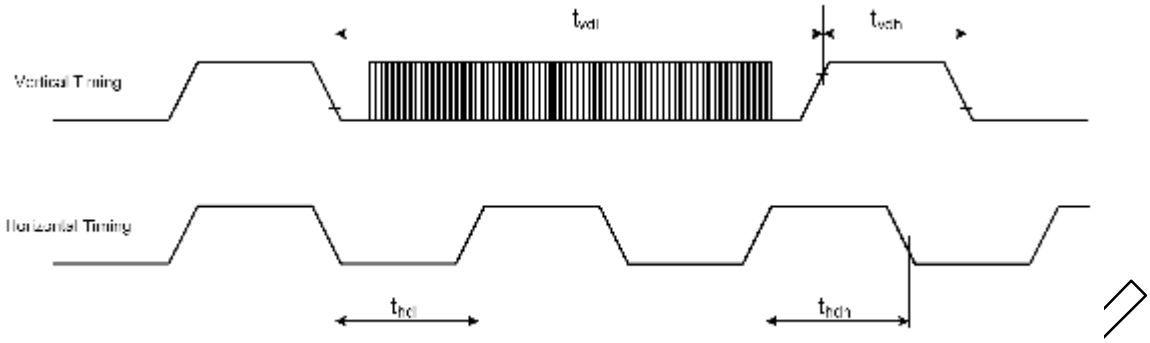
N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



Note. During Sleep In mode, the tearing effect output signal is active low.

7.8.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

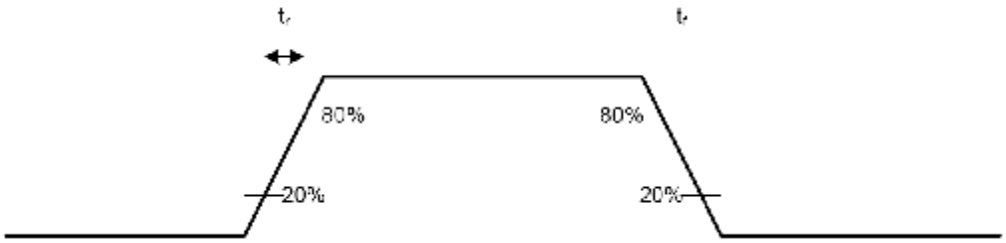


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical timing low duration	TBD		ms	
tvdh	Vertical timing high duration	TBD		us	
thdl	Horizontal timing low duration	TBD		us	
thdh	Horizontal timing high duration	TBD		us	

Notes:

1. The timings apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid tearing effect:

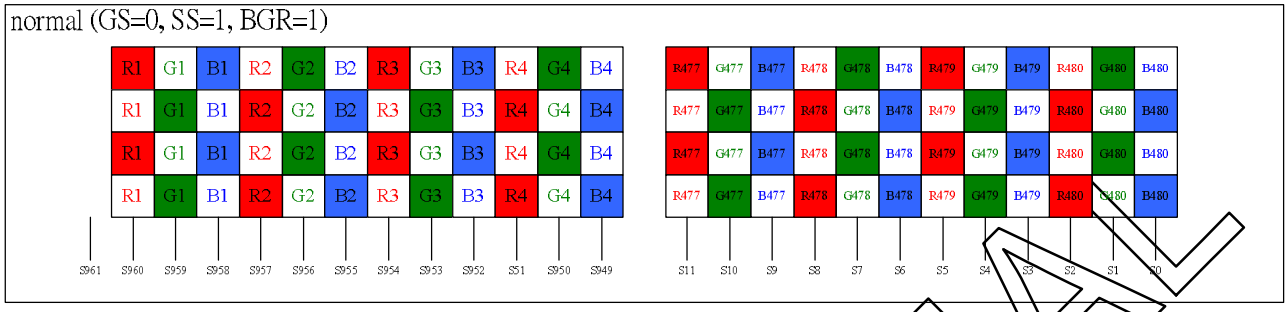
The Tearing Effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TELOM (35h, 1st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

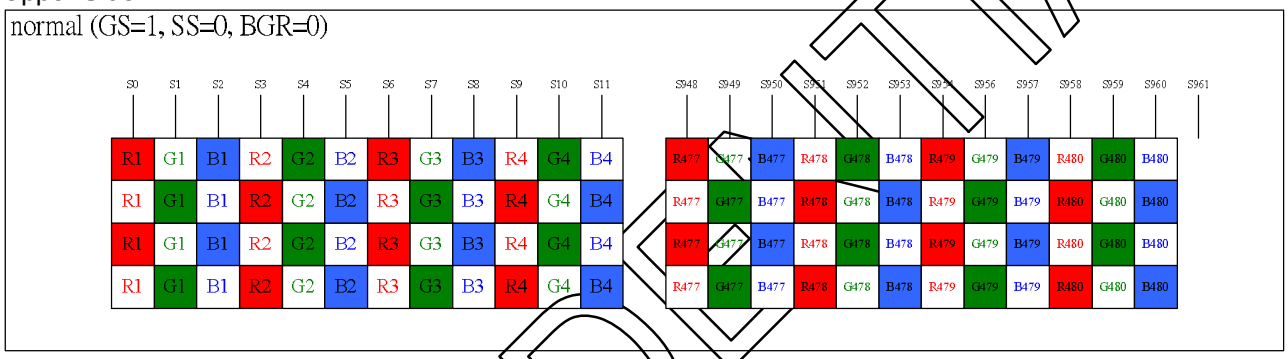
7.9 Panel Type

7.9.1 Normal Type

Bottom Side

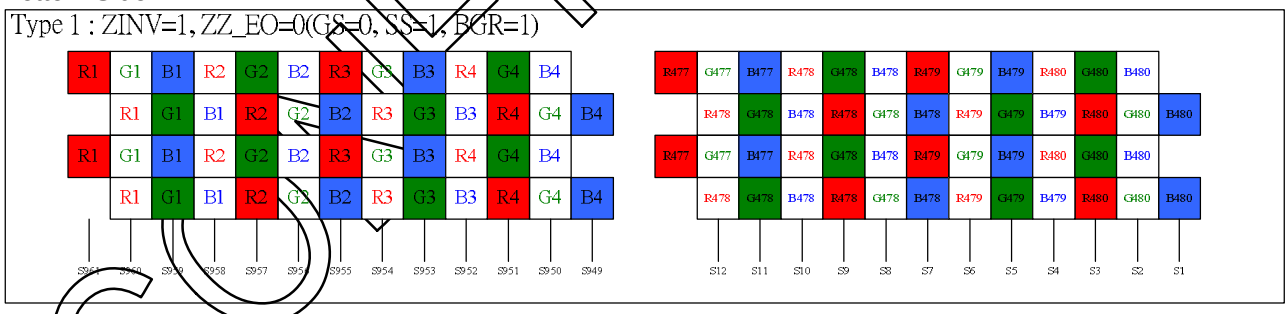


Upper Side

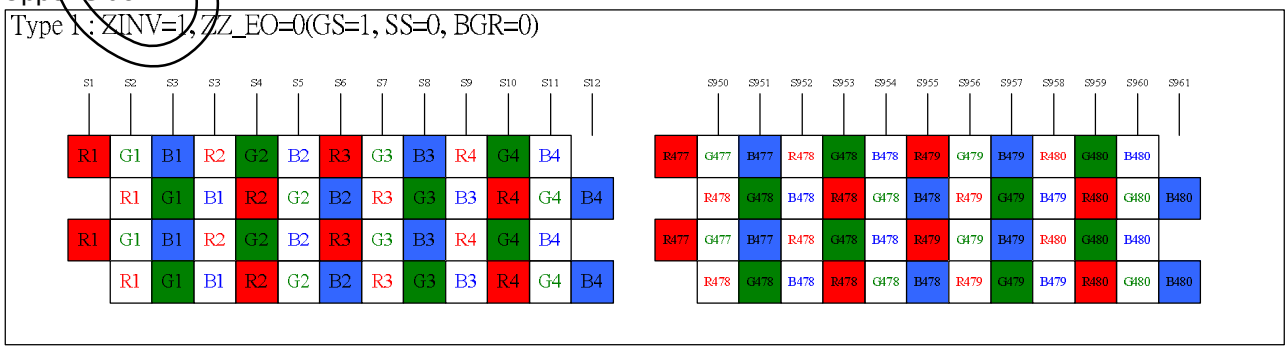


7.9.2 Zigzag Type 1

Bottom Side

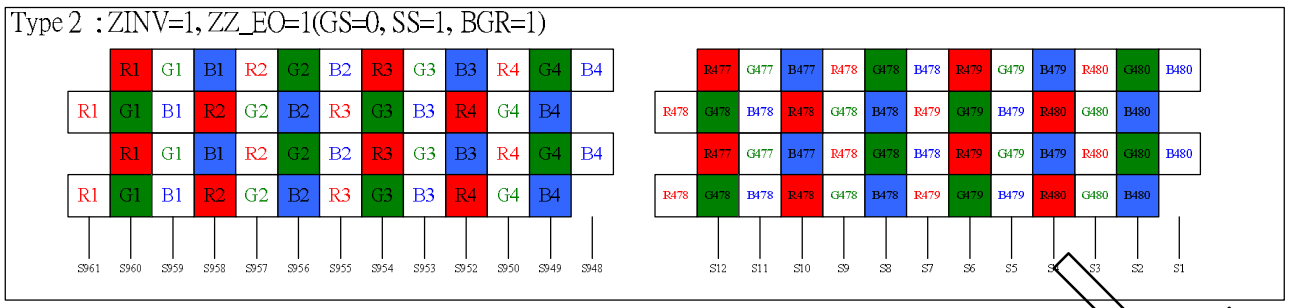


Upper Side

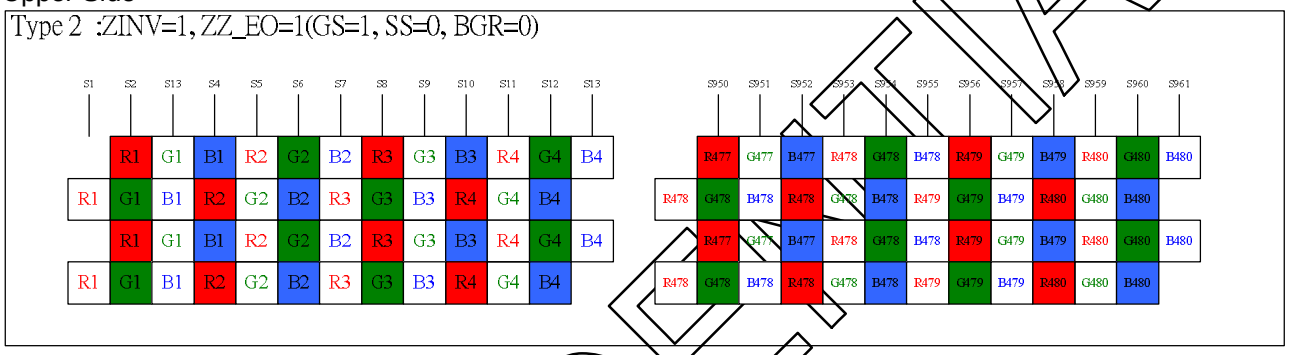


7.9.3 Zigzag Type 2

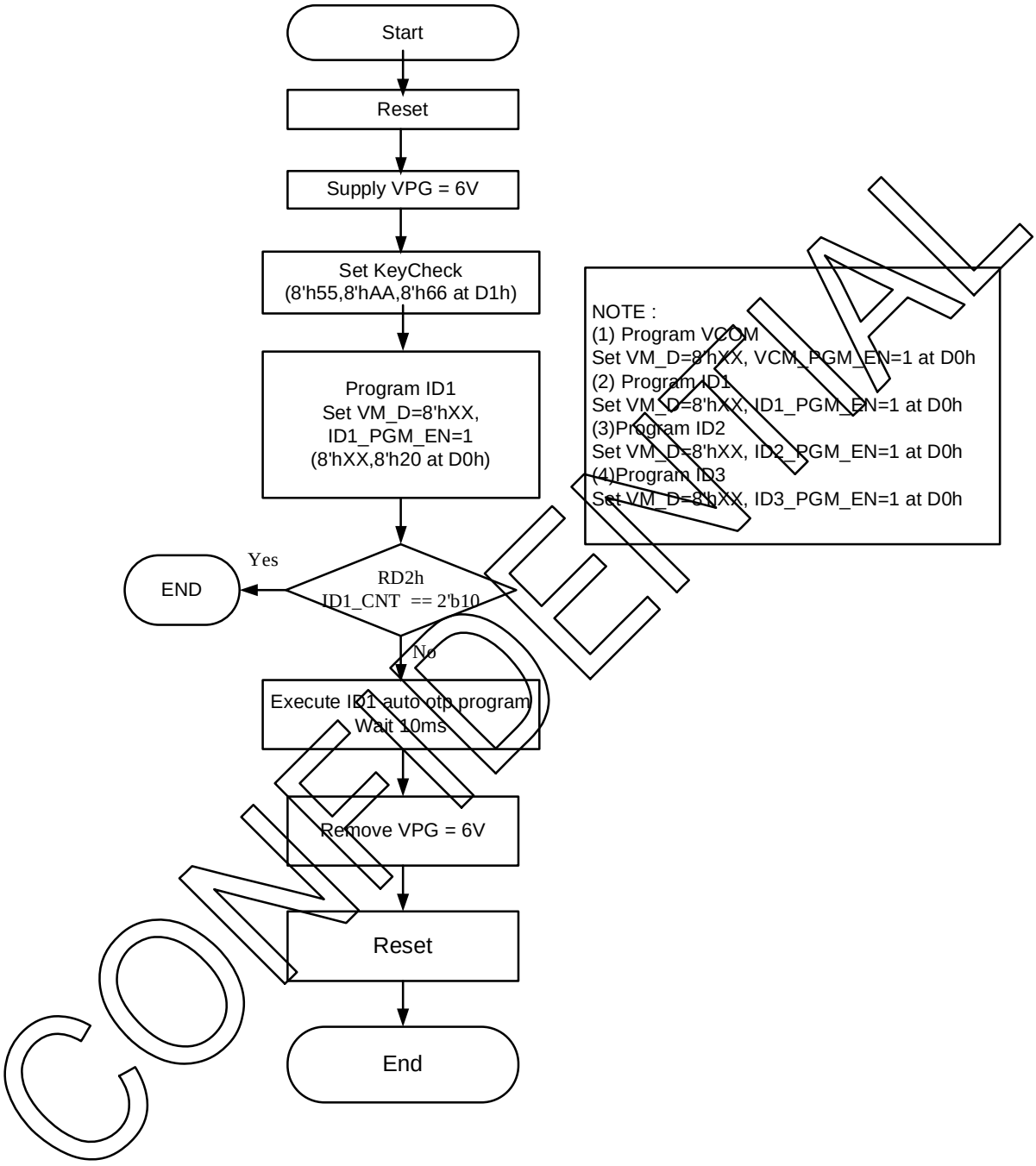
Bottom Side



Upper Side



7.10 OTP Porgram Sequence



7.11 Independent Gamma Correction Function

The RM68140 supports independent gamma adjustment function for R color, G color and B color to display in 262K colors. Only RG or GB or RB can be adjusted by increasing or decreasing at the same time. The function is performed by increasing or decreasing grayscale levels that use gamma adjustment registers. According to the user specified setting, the 3 gamma block maps the 6-bit R/G/B pixel data to 8-bit gamma information and performs 2-bit dithering effect for reducing gamma information from 8-bit to 6-bit. Finally The 6-bit gamma information is sent to source driver.

The settings of gamma correction function are as follow:

Register	Note	Register	Note
RCBnd8[5:0]	Set offset of red/green code 8	RCBnd16[5:0]	Set offset of red/green code 16
RCBnd24[5:0]	Set offset of red/green code 24	RCBnd32[5:0]	Set offset of red/green code 32
RCBnd40[5:0]	Set offset of red/green code 40	RCBnd48[5:0]	Set offset of red/green code 48
RCBnd56[5:0]	Set offset of red/green code 56	RCBnd64[5:0]	Set offset of red/green code 64
Register	Note	Register	Note
BCBnd8[5:0]	Set offset of blue/green code 8	BCBnd16[5:0]	Set offset of blue/green code 16
BCBnd24[5:0]	Set offset of blue/green code 24	BCBnd32[5:0]	Set offset of blue/green code 32
BCBnd40[5:0]	Set offset of blue/green code 40	BCBnd48[5:0]	Set offset of blue/green code 48
BCBnd56[5:0]	Set offset of blue/green code 56	BCBnd64[5:0]	Set offset of blue/green code 64

If xCBnd*[5]=0 =>

xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset
0	0	8	-2.00	16	-4.00	24	-6.00
1	-0.25	9	-2.25	17	-4.25	25	-6.25
2	-0.5	10	-2.50	18	-4.50	26	-6.50
3	-0.75	11	-2.75	19	-4.75	27	-6.75
4	-1.00	12	-3.00	20	-5.00	28	-7.00
5	-1.25	13	-3.25	21	-5.25	29	-7.25
6	-1.50	14	-3.50	22	-5.50	30	-7.50
7	-1.75	15	-3.75	23	-5.75	31	-7.75

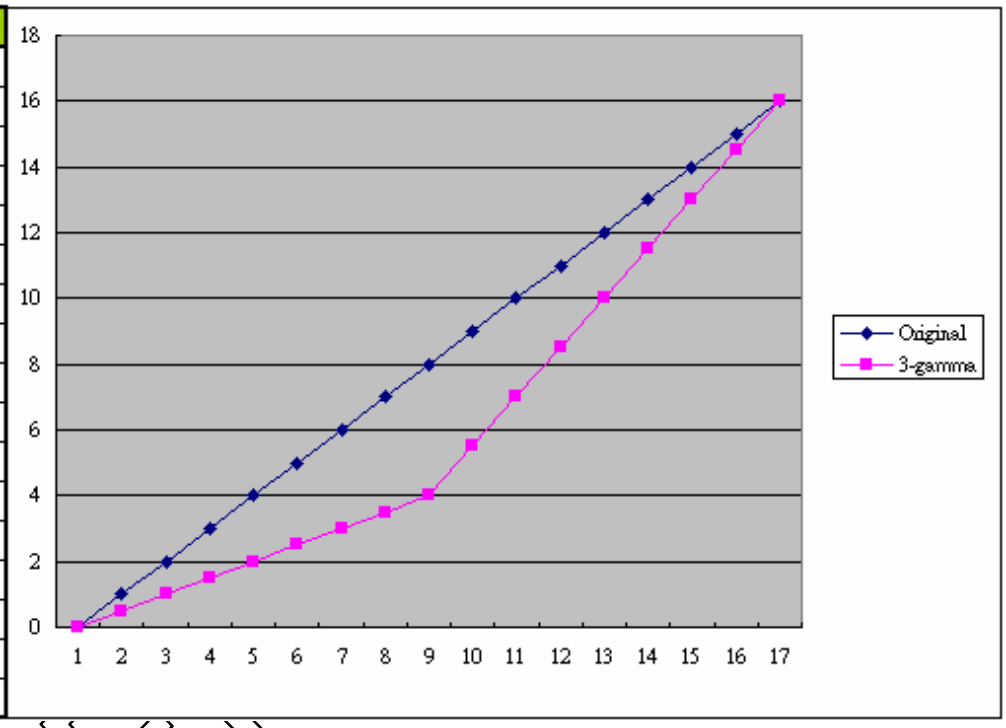
If xCBnd*[5]=1 =>

xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset	xCBnd*[4:0]	Offset
0	0	8	+2.00	16	+4.00	24	+6.00
1	+0.25	9	+2.25	17	+4.25	25	+6.25
2	+0.5	10	+2.50	18	+4.50	26	+6.50
3	+0.75	11	+2.75	19	+4.75	27	+6.75
4	+1.00	12	+3.00	20	+5.00	28	+7.00
5	+1.25	13	+3.25	21	+5.25	29	+7.25
6	+1.50	14	+3.50	22	+5.50	30	+7.50
7	+1.75	15	+3.75	23	+5.75	31	+7.75

Example :

Set RCBndm[5]=0 and BCBndm[5]=0. According to RCBndm[4:0]/BCBndm[4:0], they decide the offsetting of the code m of red (or green)/blue (or green) from -7.75, -7.50, -7.25, … to 0 and code 0 is fixed at 0 forever. The other codes between each code m are interpolated. For example, if only red code 8 is offset to 4 by setting RCBnd8[4:0] = 16, the code from 16 to 63 are unchanged and the results of red code 1 to code 15 are as follow:

Original	3-gamma
0	0
1	0.5
2	1
3	1.5
4	2
5	2.5
6	3
7	3.5
8	4
9	5.5
10	7
11	8.5
12	10
13	11.5
14	13
15	14.5
16	16



The RCBndm could be chosen to adjust digital codes of red or green by set RADJ_SEL and the BCBndm could be chosen to adjust digital codes of blue or green by set BADJ_SEL.

RADJ_SEL	BADJ_SEL	Adjust Channel	Unchanged Channel
0	0	R & B	G
0	1	R & G	B
1	0	G & B	R
1	1	inhibit	X

7.12 Dynamic Backlight Control

The function of Dynamic Display Backlight is used to reduce the power consumption of display backlight. It only includes Content Adaptive Brightness Control (CABC) function. CABC is used to generate a proper PWM signal according to display image information. User could apply this PWM signal to control other device(s) (Such as power IC or LED driver IC). When the CABC function is enabled and cooperate with external circuits (such as LED driver circuit), the power consumption of backlight will be reduced with keeping acceptable display quality.

The CABC function is used to reduce the power consumption of display backlight. Contents adaptation means that the grayscale level of image contents is raised while lowering brightness of the backlight simultaneously to keep same perceived brightness. The adjustment of grayscale level and brightness reduction is based on the display image contents. Thus the power consumption reduction depends on the contents of the image. The display image and brightness are dynamically processed by CABC block.

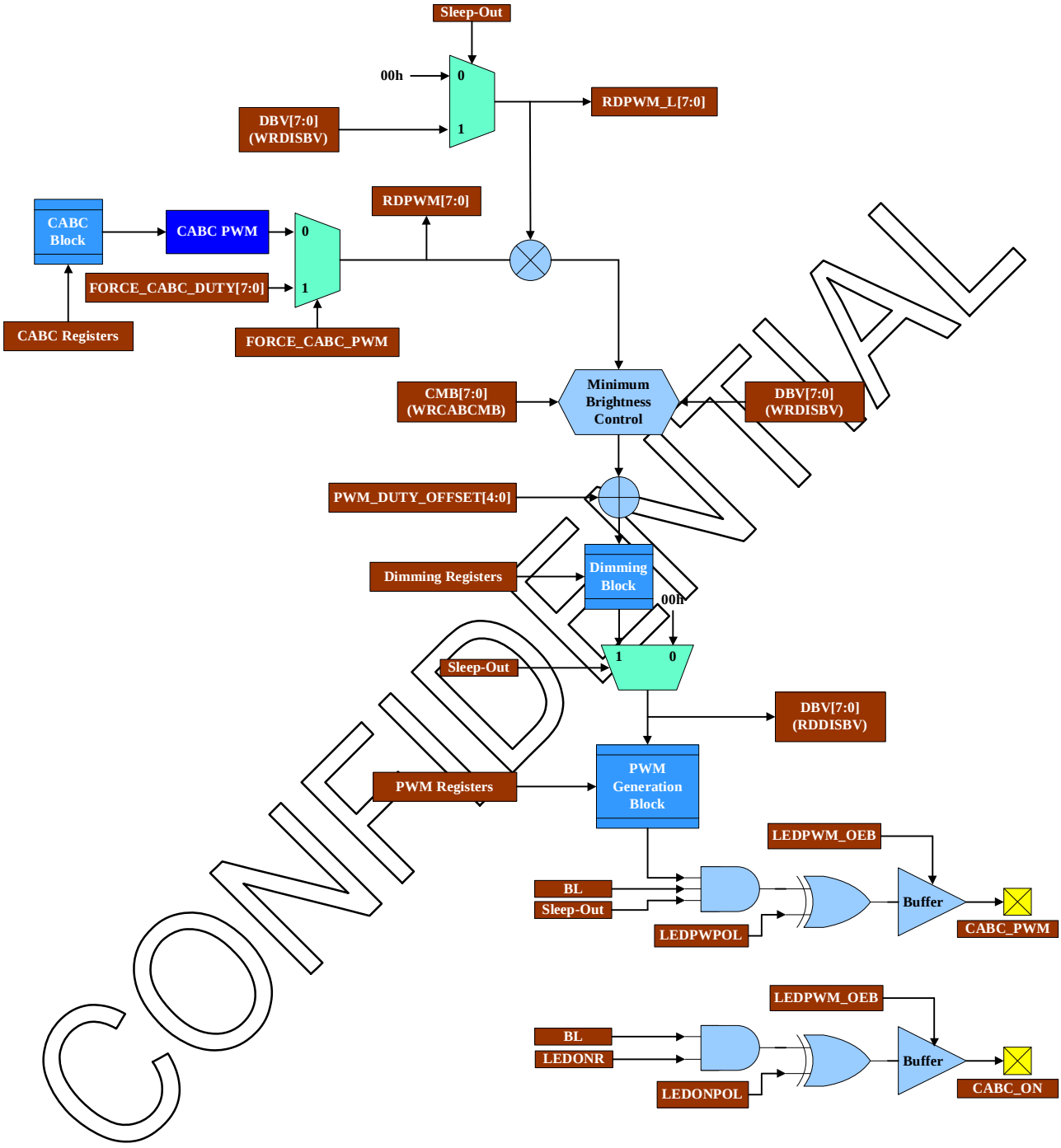
In order to achieve a better display quality and reduce power consumption of the backlight at the same time, there are 3 different modes, user interface image mode, still picture mode and moving image mode, for user selections.

Display Backlight Brightness = Manual Setting Ratio x CABC Brightness Ratio

The function of CABC affects both display brightness ratio and grayscale level.

	Manual Brightness Ratio	**CABC Brightness Ratio**	**Calculation Ratio**	**Brightness Output of LEDPWM**	**Image Status**
Case 1	70%	60%	42%	42%	CABC modified
Case 2	50%	100%	50%	50%	CABC modified
Case 3	40%	30%	12%	12%	CABC modified

7.12.1 PWM Control Architecture



Internal Display Backlight Control

The register bit “BL” is used to turn on or turn off backlight control lines, “CABC_PWM” pin and “CABC_ON” pin. Normally, if user want to disable the display backlight completely and immediately, user can set “BL = 0”. Relations between “BL” and control lines are list below.

BL	LEDPWPOL	Status of CABC_PWM Pin
0	0	0
	1	1
1	0	Original polarity of PWM signal
	1	Inversed polarity of PWM signal

BL	LEDONPOL	Status of CABC_ON Pin
0	0	0
	1	1
1	0	LEDONR
	1	Inverted LEDONR

The register bit “BCTRL” is used to turn on or turn off backlight control block. Display brightness which is controlled by CABC_PWM will be turn off when user set “BCTRL = 0”.

BCTRL	Value of DBV[7:0] (RDDISBV)	Display Backlight Status
0	00h	off
1	Determined by CABC and WRDISBV(R51h)	on

“FORCE_CABC_PWM=0”, “CMB[7:0] = 00h” (WRCABCMB), “PWM_DUTY_OFFSET[4:0]=00h”, “BL=1”, “BCTRL=1”, Sleep-Out Mode			
CABC Status	**RDPWM_L[7:0]**	**RDPWM[7:0]**	**Display Backlight Brightness**
Off Mode	Determined by DBV[7:0] (WRDISBV)	FFh	Determined by DBV[7:0] (WRDISBV)
UI-Mode / Still-Mode / Moving-Mode	Determined by DBV[7:0] (WRDISBV)	Determined by CABC Function	Determined by DBV[7:0] (WRDISBV) x CABC Function

The writing register DBV[7:0] (WRDISBV) is used to adjust the backlight brightness value manually. Note that reading register DBV[7:0] (RDDISBV) is used to indicate the output PWM signal duty variation. That means DBV[7:0] (RDDISBV) is also affected by CABC function when CABC function is enable.

The register setting CMB[7:0] (WRCABCCMB) is used to limit the minimum PWM duty in order to prevent the backlight brightness from being too dark.

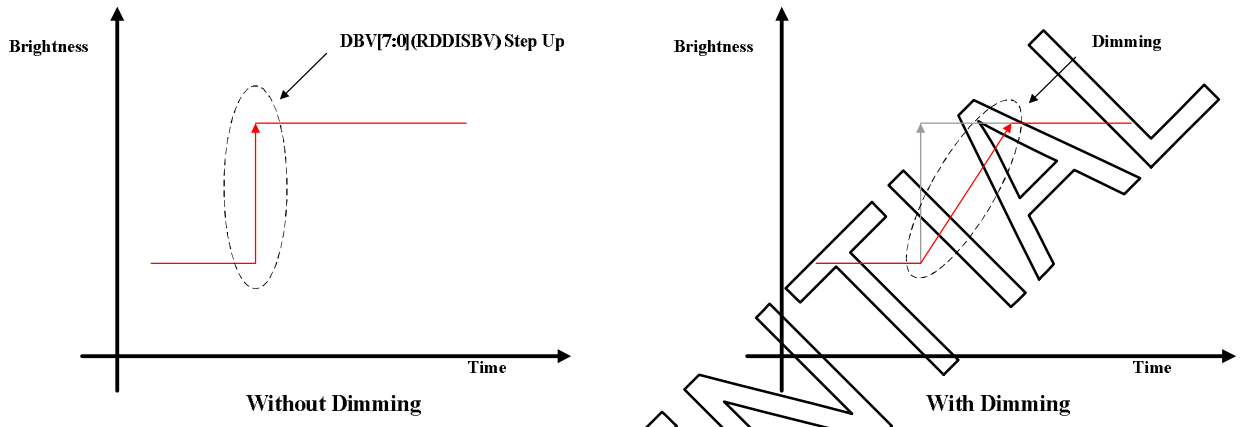
The register FORCE_CABC_DUTY[7:0] is used to perform a fixed PWM duty of CABC output when the register bit “FORCE_CABC_PWM=1”.

The register bit “DD” is used to enable or disable the dimming function for Manual Brightness Control. Smooth transition of PWM duty is performed when “DD=1”. Dimming function is applied only when driver IC is in sleep-out status. CABC function is available only when driver IC is in sleep-out status. Availability of functions is listed in below table.

Driver IC Status	CABC Function	LABC Function	Dimming Function	Display Backlight Status
Sleep-In	Not Available	Not Available	Not Available	Turn-Off
Sleep-Out	Available	Available	Available	Controllable

7.12.2 Dimming Function for LABC and Manual Brightness Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. The dimming function curves for Manual Brightness Control can be configured the same or not the same in increment and decrement directions. The basic idea is described below.



Basic Concept of Dimming Function

The RM68140 provides two types of PWM duty dimming mechanism, “Fixed-Time Dimming” and “Fixed-Slope Dimming”, for manual brightness control. The setting of dimming types for rising dimming and falling dimming is independent. The register bit “SEL_IN” is for rising dimming (increment dimming), and the register bit “SEL_DE” is for falling dimming (decrement dimming).

SEL_IN	SEL_DE	Rising Dimming Type	Falling Dimming Type
0	0	Fixed-Time Dimming	Fixed-Time Dimming
0	1	Fixed-Time Dimming	Fixed-Slope Dimming
1	0	Fixed-Slope Dimming	Fixed-Time Dimming
1	1	Fixed-Slope Dimming	Fixed-Slope Dimming

Fixed-Time Dimming Type

The total dimming steps and can be set by registers “DMSTP_L[2:0]”, “DM_IN[3:0]”, and “DM_DE[3:0]”, respectively. These three registers can determine the total dimming time.

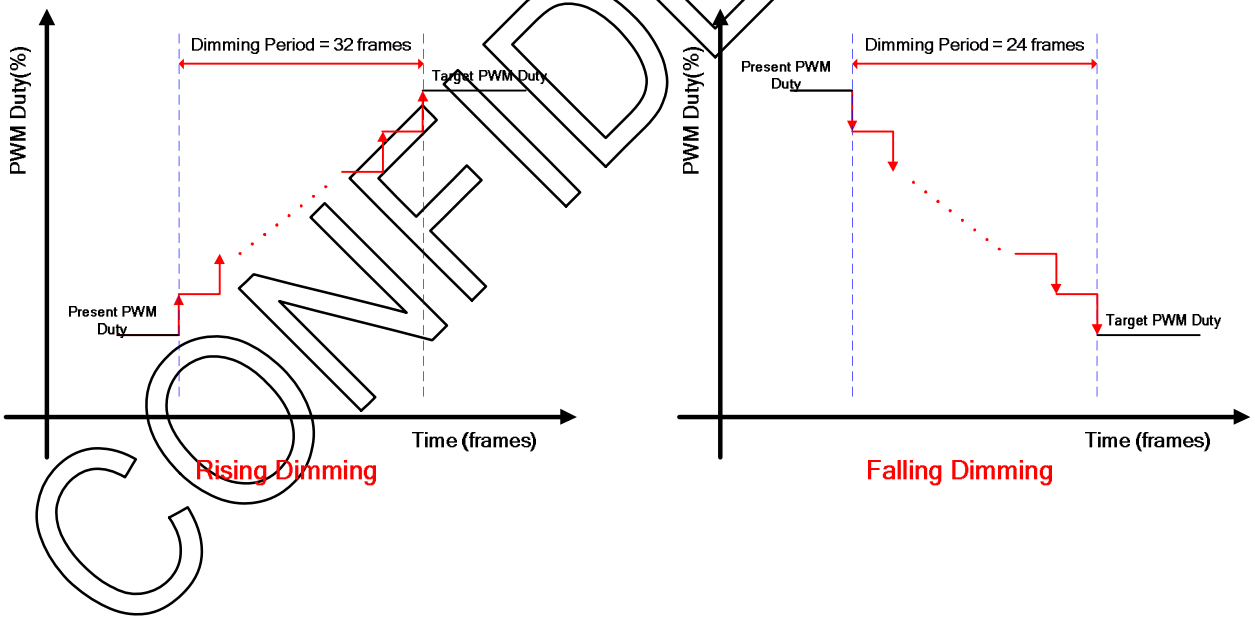
The unit of registers “DM_IN[3:0]” and “DM_DE[3:0]” is “frame(s) per step”. The unit of register DMSTP_L[2:0] is “step(s)”

For Example:

Register Name	Value	Description
SEL_IN	0	Fixed-Time dimming for rising dimming
SEL_DE	0	Fixed-Time dimming for falling dimming
DM_IN[3:0]	7h	8 frames time for each step
DN_DE[3:0]	5h	6 frames time for each step
DMSTP_L[2:0]	1h	dimming steps is 4 steps

Total dimming time of “rising dimming” is 32-frames time length (8 frames x 4).

Total dimming time of “falling dimming” is 24-frames time length (6 frames x 4).



Fixed-Slope Dimming Type

The increasing / decreasing PWM duty during a time period can be set by register “STEP_IN[3:0]”, “STEP_DE[3:0]”, “DM_IN[3:0]”, and “DM_DE[3:0]”, respectively. These three registers can determine some characteristics of dimming curves.

The unit of registers STEP_IN[3:0] and STEP_DE [3:0] is “duty ratio” (FFh is 100%, and 00h is 0%). The unit of register DM_IN[3:0] and DM_DE[3:0] is “frame(s) per step”.

For Example:

Register Name	Value	Description
SEL_IN	1	Fixed-Slope dimming for rising dimming
SEL_DE	1	Fixed-Slope dimming for falling dimming
STEP_IN[3:0]	8h	PWM increment is 8 for each step
STEP_DN[3:0]	5h	PWM decrement is 5 for each step
DM_IN[3:0]	3h	4 frames time for each step
DM_DE[3:0]	5h	6 frames time for each step

When present PWM duty is “0x64” (100 in decimal), target PWM duty is 0x14 (20 in decimal), so the total dimming steps will be:

Total dimming steps = (Present PWM Duty - Target PWM duty) / (PWM decrement)

= (100 - 20) / 5 = 16 steps

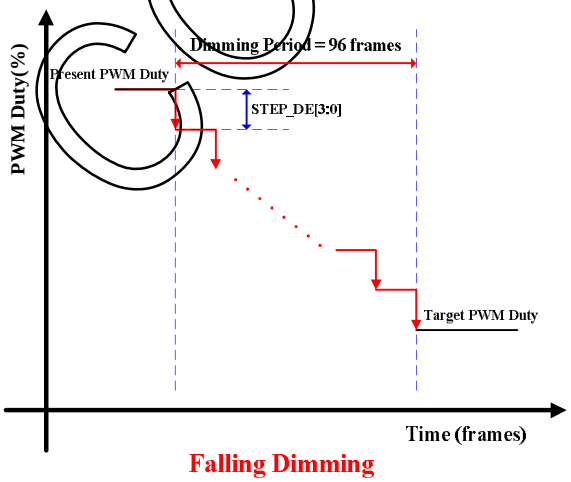
So total dimming time for falling dimming is 96 frames (16 Steps x 6)

When new target PWM duty is “0x64”, the total dimming steps will be:

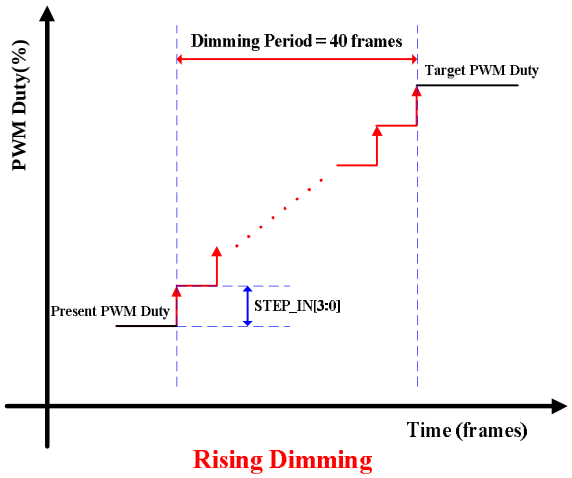
Total dimming steps = (Target PWM Duty - Present PWM duty) / (PWM increment)

= (100 - 20) / 8 = 10 steps

So total dimming time for rising dimming is 40 frames (10 Steps x 4)



Falling Dimming



Rising Dimming

7.12.3 PWM Signal Setting for CABC and LABC

The registers “PWMDIV[7:0]” can change the frequency of PWM signal(CABC_PWM) and the register “PWM_DUTY_OFFSET[4:0]” can perform a duty compensation of the PWM signal. The “FOSC” is used to provide clock source for the internal PWM circuit. Three PWM operation frequency can be chosen by setting register “PWMF”, and the real PWM frequency can be quickly estimated by the bellow formula.

PWMF	PWM Operation Frequency (F_{osc})
0	12.165 MHz
1	6.0827 MHz

$$PWM\ Frequency = \frac{F_{osc}}{256 \times PWMDIV[7:0]}$$

$$PWM\ Duty = \frac{DBV[7:0](RDDISBV)+1}{256}$$

For example:

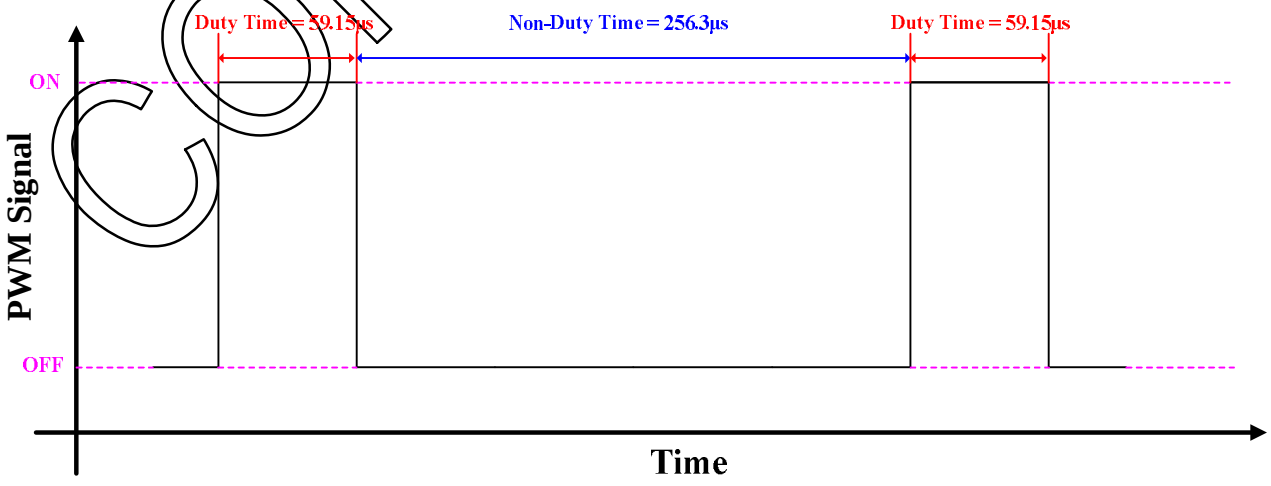
If “PWDIV[7:0]=0x0F”, “PWMF=0x0”, “DBV[7:0]=2Fh”(RDDISBV)

$$PWM\ Frequency = \frac{12.165MHz}{256 \times 15} \approx 3.17KHz$$

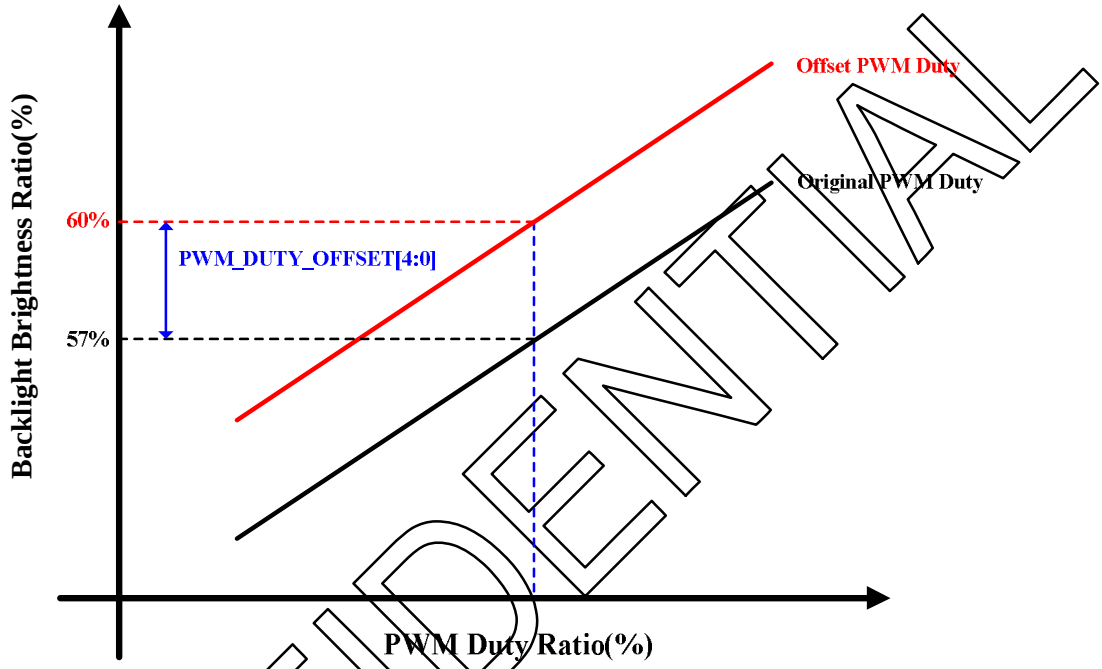
“DBV[7:0]=2Fh” means PWM duty ratio is about 18.75%

$$PWM\ Duty\ Time = 18.75\% \times \frac{1}{3.17KHz} \approx 59.15ms$$

$$PWM\ non-Duty\ Time = 81.25\% \times \frac{1}{3.17KHz} \approx 256.3ms$$



Since the external LED driver needs some stable time to drive the LED backlight, this necessary stable time will reduce the effective PWM duty period. The PWM_DUTY_OFFSET[4:0] is simply used to compensate the loss of PWM duty period. For example, assume original PWM duty of LEDPWM signal is 60%, but the actual backlight brightness driven by LED driver is 57%. User can set "PWM_DUTY_OFFSET[4:0]" to achieve 60% backlight brightness.



7.12.4 Content Adaptive Brightness Control (CABC)

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. There four different modes of CABC can be controlled through register “C[1:0]”(WRCABC).

Descriptions of these four modes are listed below:

1. Off mode: Content Adaptive Brightness Control functionality is totally off.

2. UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less. User can achieve prefer brightness for UI-Mode by setting the registers “CABC_UI_PWM0[7:0]” ~ “CABC_UI_PWM3[7:0]”.

3. Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%. The RM68140 will automatically estimate a better gamma setting based on image contents. User can achieve prefer brightness for still picture mode by setting the registers “CABC_PWM0[7:0]” ~ “CABC_PWM9[7:0]”.

4. Moving image mode: Optimized for moving image e.g. Video clip. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%. The RM68140 will automatically estimate a better gamma setting based on image contents. User can achieve prefer brightness for still picture mode by setting the registers “CABC_MOV_PWM0[7:0]” ~ “CABC_MOV_PWM9[7:0]”.

8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
00h	nop	C	0
01h	soft_reset	C	0
04h	get_display_ID	R	3
05h	get_DSI_err	R	1
09h	read_display_status	R	4
0Ah	get_power_mode	R	1
0Bh	get_address_mode	R	1
0Ch	get_pixel_format	R	1
0Dh	get_display_mode	R	1
0Eh	get_signal_mode	R	1
0Fh	get_diagnostic_result	R	1
10h	enter_sleep_mode	C	0
11h	exit_sleep_mode	C	0
12h	enter_partial_mode	C	0
13h	enter_normal_mode	C	0
20h	exit_invert_mode	C	0
21h	enter_invert_mode	C	0
28h	set_display_off	C	0
29h	set_display_on	C	0
2Ah	set_column_address	W	4
2Bh	set_page_address	W	4
2Ch	write_memory_start	W	Variable
2Eh	read_memory_start	R	Variable
30h	set_partial_area	W	4
33h	set_scroll_area	W	6
34h	set_tear_off	C	0
35h	set_tear_on	W	1
36h	set_address_mode	W	1
38h	exit_idle_mode	C	0
39h	enter_idle_mode	C	0
3Ah	set_pixel_format	W	1
3Ch	write_memory _continue	W	Variable
3Eh	read_memory _continue	R	Variable
44h	set_tear_scanline	W	2
45h	get_scanline	R	2
51h	set_display_brightness	W	1
52h	get_display_brightness	R	1
53h	set_control_display	W	1

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
54h	get_control_display	R	1
55h	set_cabc_mode	W	1
56h	get_cabc_mode	R	1
5Eh	set_cabc_min_brightness	W	1
5Fh	get_cabc_min_brightness	R	1
AAh	read_first_checksum	R	1
AFh	read_continue_checksum	R	1
DAh	read_ID1	R	1
DBh	read_ID2	R	1
DCh	read_ID3	R	1
B0h	Interface_mode_control	W	1
B1h	frame_rate_control (in normal mode)	W	2
B2h	frame_rate_control (in idle mode/8 colors)	W	2
B3h	frame_rate_control (in partial mode)	W	2
B4h	display_inversion_control	W	1
B5h	blanking_porch_control	W	4
B6h	display_function_control	W	3
B7h	entry_mode_set	W	1
BFh	device_code_read	R	5
C0h	power_control_1	W	2
C1h	power_control_2	W	2
C2h	power_control_3	W	1
C4h	power_control_4	W	1
C5h	vcom_control_1	W	4
D0h	nv_memory_write	W	2
D1h	nv_memory_protection_key	W	3
D2h	nv_memory_status_read	R	3
D3h	read_ID4	R	3
E0h	Gamma_setting	W	15

8.2. Command Description

NOP (00h)

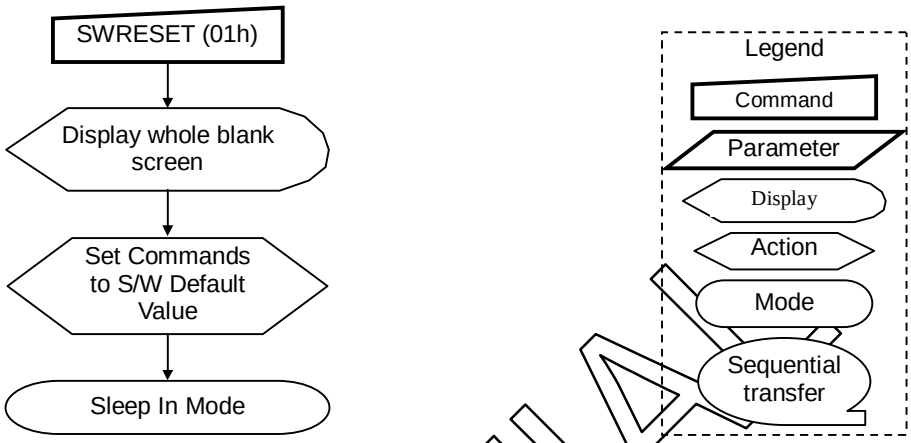
00H	NOP (No Operation)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												
Register Availability													
Default													
Flow Chart	None												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

SWRESET(01h) : Software Reset

<table>
<tr><th>01H</th><th colspan="13">SWRESET(Software Reset)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="13">No parameter</td></tr>
<tr><td>Description</td><td colspan="13">When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are affected by this command.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module loads all display supplier’s factory default values to the registers during 5ms. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120ms before sending Sleep Out command. Software Reset Command can not be sent during Sleep Out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
</table>

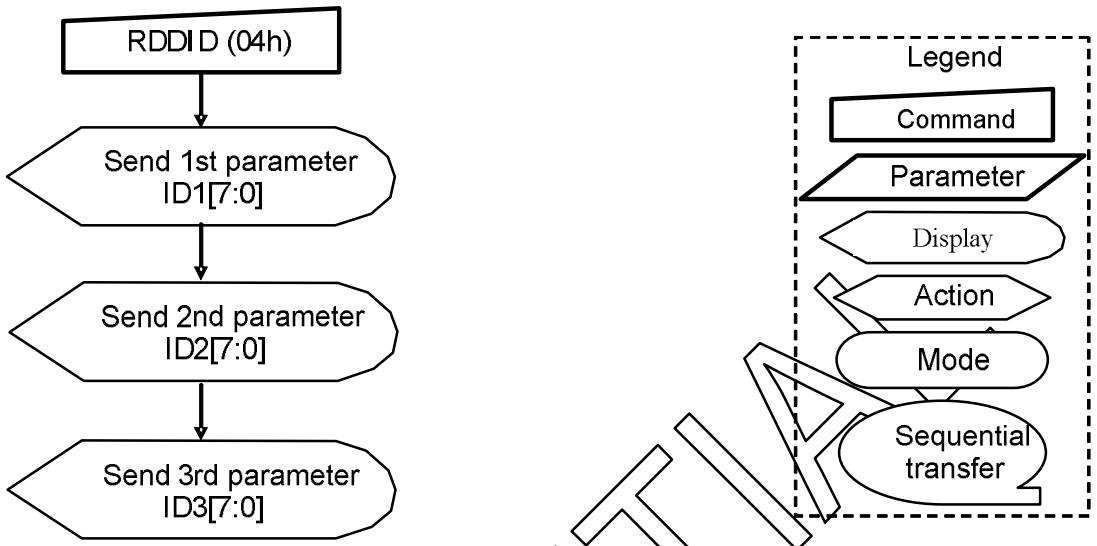
Flow Chart	

RDDIDIF(04h) : Read Display ID

04H	RDDIDIF												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	00h	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	X
2nd parameter	1	↑	1	00h	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	54
3rd parameter	1	↑	1	00h	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	80
4th parameter	1	↑	1	00h	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	66
Parameter	-												
Description	The 1st parameter (ID1): dummy data. The 2nd parameter (ID2): the LCD module's manufacture ID The 3rd parameter (ID3): the LCD module/driver version ID The 4th parameter (ID4): the LCD module/driver ID												
Restriction	-												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	ID1=54h / ID2=80h / ID3=66h
SW Reset	ID1=54h / ID2=80h / ID3=66h
HW Reset	ID1=54h / ID2=80h / ID3=66h

Flow Chart	

RDNUMED(05h) : Read Number of Errors on DSI

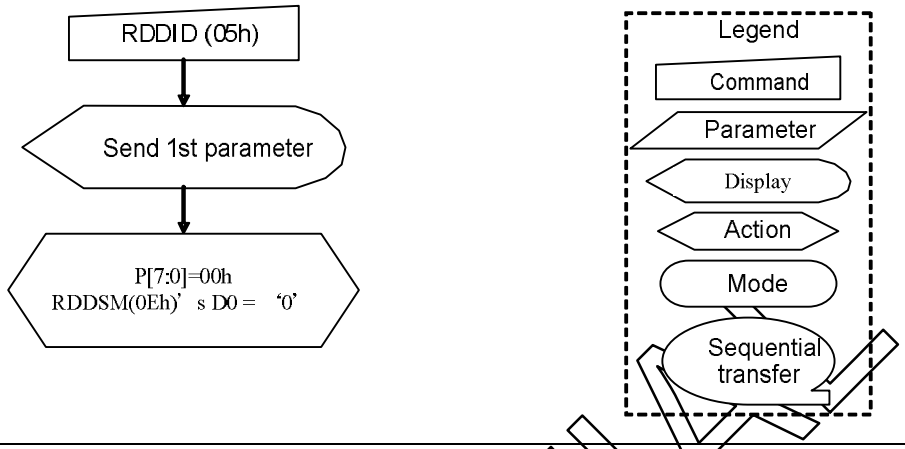
05H	RDNUMED (Read Number of the Error on DSI)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	0	1	0	1	05
1st parameter	1	↑	1	x	P[7]	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]	00
Parameter	NO PARAMETER												
Description	The second parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to “1” if there is overflow with P[6..0] bits. P[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the second parameter information (= The read function is completed). This command is used for MIPI DSI only. It is no function for others interface operation.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

RDDST (09h) : Read Display Status

09H	RDDST (Read Display Status)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	x	D31	D30	D29	D28	D27	D26	D25	0	xx
3rd parameter	1	↑	1	x	0	D22	D21	D20	D19	D18	D17	D16	xx
4th parameter	1	↑	1	x	D15	0	D13	0	0	D10	D9	D8	xx
5th parameter	1	↑	1	x	D7	D6	D5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Value	Status
D31	BSTON	Booster Voltage Status	0	Booster off
			1	Booster on
D30	MY	Row Address Order	0	Top to Bottom (36H- D7='0')
			1	Bottom to Top (36H-D7='1')
D29	MX	Column Address Order	0	Left to Right (MADCTL D6='0')
			1	Right to Left (MADCTL D6='1')
D28	MV	Row/Column Order (MV)	0	Normal (36H-D5='1')
			1	Row/column exchange(36H-D5='1')
D27	ML	Vertical Refresh Order	0	LCD Refresh Bottom to Top
			1	LCD Refresh Top to Bottom
D26	RGB	RGB/BGR Order	0	RGB
			1	BGR
D25	MH	Horizontal Refresh Order	0	LCD Refresh Left to Right
			1	LCD Refresh Right to Left
D22	IFPF[2:0]	DBI Pixel Format(Control Interface Color Format)	101	16-bits / pixel
D21			110	18-bits / pixel
D20			others	-
D19	IDMOD	Idle Mode On/Off	0	Idle Mode Off
			1	Idle Mode On
D18	PTLON	Partial Mode On/Off	0	Partial Mode Off
			1	Partial Mode On
D17	SLPOUT	Sleep In/Out	0	Sleep In
			1	Sleep Out
D16	NORON	Display Normal Mode On/Off	0	Partial Display
			1	Normal Display
D15	VSSON	Vertical scrolling status	0	Vertical scrolling is Off
			1	Vertical scrolling is On
D13	INVON	Inversion On/Off	0	Inversion is Off
			1	Inversion is On
D10	DISPON	Display On/Off	0	Display Off
			1	Display On

	D9	TEON	Tearing Effect Line On/Off	0	Off
				1	on
	D8	GAMMA C SEL	NOT USED	-	-
	D7	GAMMA C SEL	NOT USED	-	-
	D6	GAMMA C SEL	NOT USED	-	-
	D5	TELOM	Tearing effect line mode	0	“0” = mode1
				1	“1” = mode2

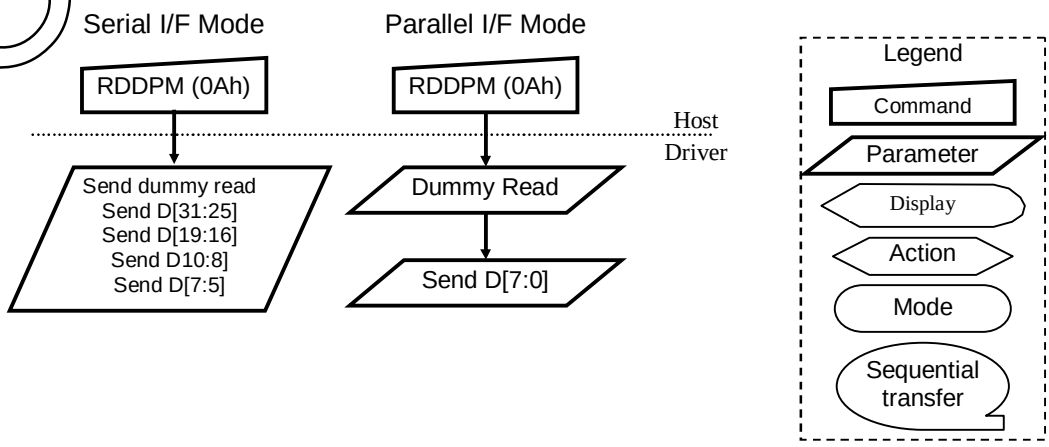
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDPM (0Ah) : Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	BSTON	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
D5	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
D4	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
D3	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
D2	DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Reserved	-	0
D0	Reserved	-	0

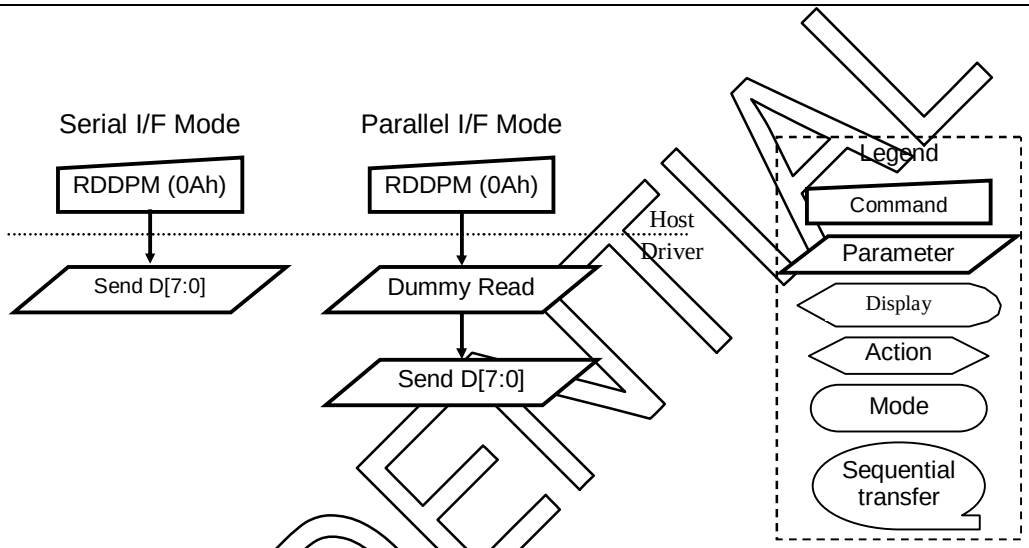
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDMADCTR (0Bh): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D7	MY	Row Address Order	'1' = Bottom to Top (36H-D7='1') '0' = Top to Bottom (36H- D7='0')
D6	MX	Column Address Order	'1' = Right to Left (MADCTL D6='1') '0' = Left to Right (MADCTL D6='0')
D5	MV	Row/Column Order (MV)	'1' = Row/column exchange(36H-D5='1') '0' = Normal (36H-D5='1')
D4	ML	Vertical Refresh Order	'1' =LCD Refresh Top to Bottom '0' =LCD Refresh Bottom to Top
D3	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
D2	MH	Horizontal Refresh Order	'0' = LCD Refresh Left to Right '1' = LCD Refresh Right to Left
D1	Reserved		0
D0	Reserved		0

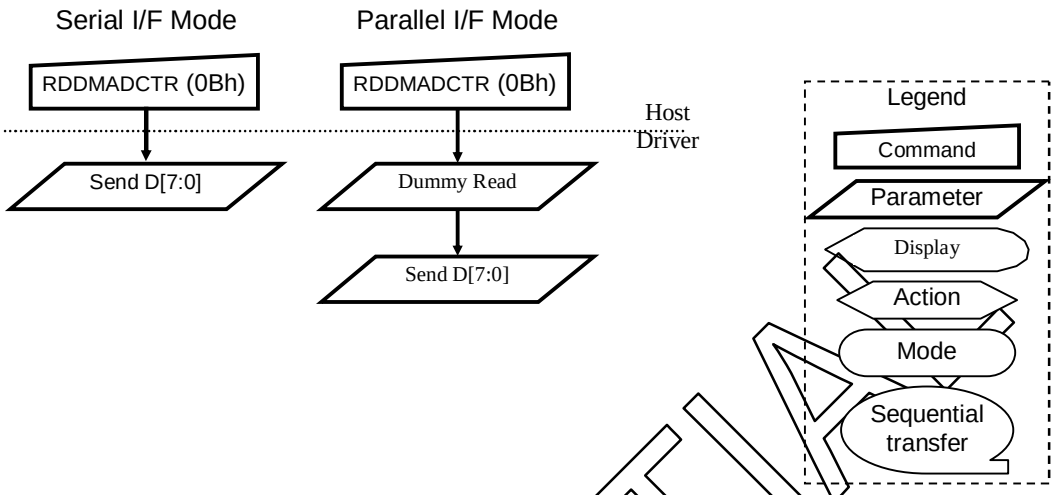
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow Chart



RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	x	D7	D6	D5	D4	0	D2	D1	D0	66

Description

This command indicates the current status of the display as described in the table below:

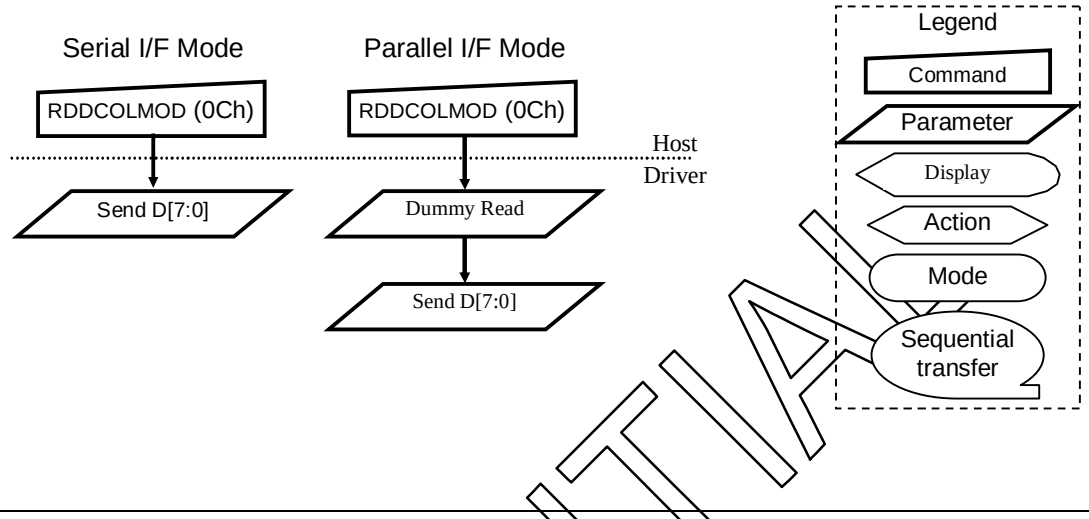
Bit	Symbol	Description	Comment
D7	VIPF[3]	DPI Pixel Format(RGB Interface Color Format)	'0101' = 16-bits / pixel, '0110' = 18-bits / pixel, others are reserved
D6	VIPF[2]		
D5	VIPF[1]		
D4	VIPF[0]		
D3	Reserved	-	'0'
D2	IFPF[2]	DBI Pixel Format(Control Interface Color Format)	'101' = 16-bits / pixel, '110' = 18-bits / pixel, others are reserved
D1	IFPF[1]		
D0	IFPF[0]		

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
SW Reset	No Change
HW Reset	66h

Flow Chart	

RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D
1st Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the display image mode status.

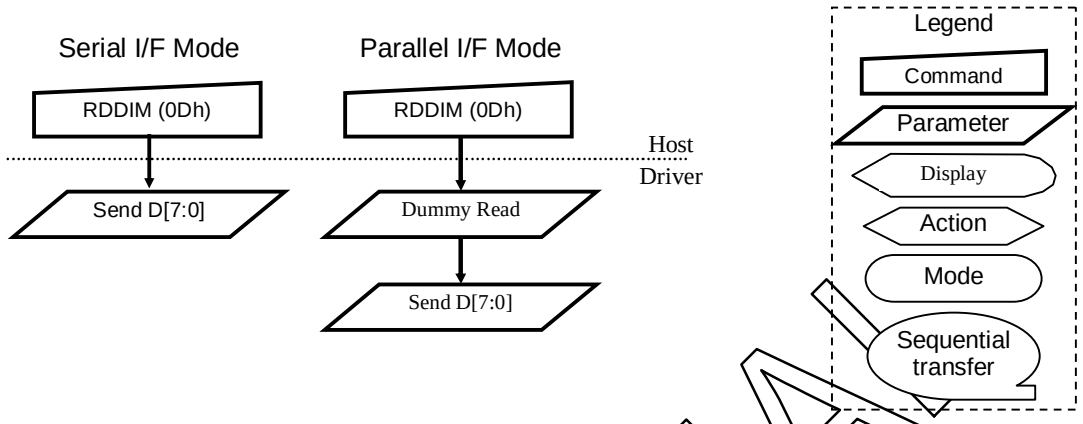
Bit	Symbol	Description	Comment
D7	VSSON	Vertical scrolling status	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Reserved		'0'
D5	INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	Reserved		'0'
D3	Reserved		'0'
D2~D0	Reserved		'0'

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

The display module returns the Display Signal Mode.

Bit	Symbol	Description	Comment
D7	TEON	Tearing Effect Line On/Off	“1” = On, “0” = Off
D6	TELOM	Tearing effect line mode	“0” = mode1, “1” = mode2
D5	HS	Horizontal Sync On/Off	‘0’ = HSYNC is Off ‘1’ = HSYNC is On
D4	VS	Vertical Sync On/Off	‘0’ = VSYNC is Off ‘1’ = VSYNC is On
D3	PCLK	Pixel Clock On/Off	‘0’ = PCLK is Off ‘1’ = PCLK is On
D2	DE	Data Enable On/Off	‘0’ = DE is Off ‘1’ = DE is On
D1	Reserved	-	‘0’
D0	DSI ERROR	Error on DSI	‘0’ = No Error ‘1’ = Error

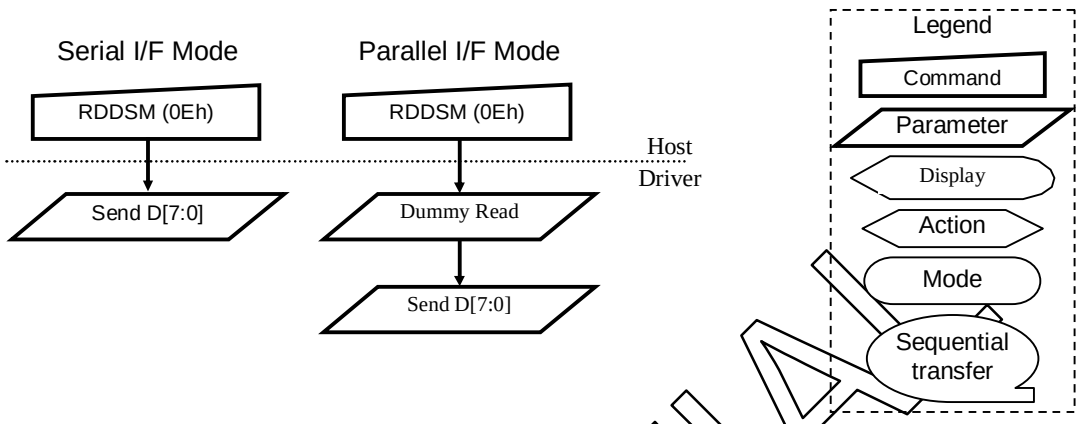
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F
1st Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	D0	00

Description

The display module returns the self-diagnostic results following a Sleep Out command.

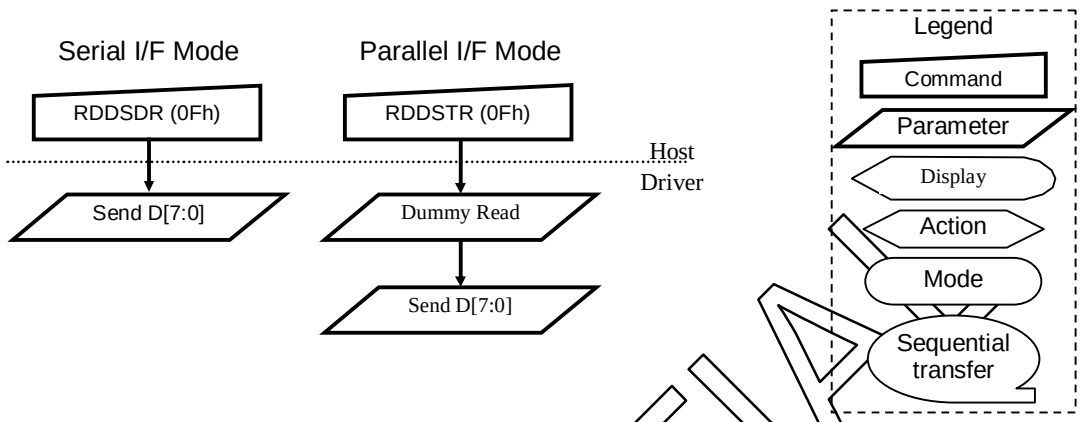
Bit	Symbol	Description	Comment
D7	SDR	Register Loading Detection	Invert the D7 if register values loading work properly
D6	FUNCD	Functionality Detection	Invert the D6 if the display is functionality
D5	Reserved		'0'
D4	Reserved		'0'
D3	Reserved		'0'
D2	Reserved		'0'
D1	Reserved		'0'
D0	CKSCMP	Checksums comparison	'0' = checksums are same '1' = checksums are not the same

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

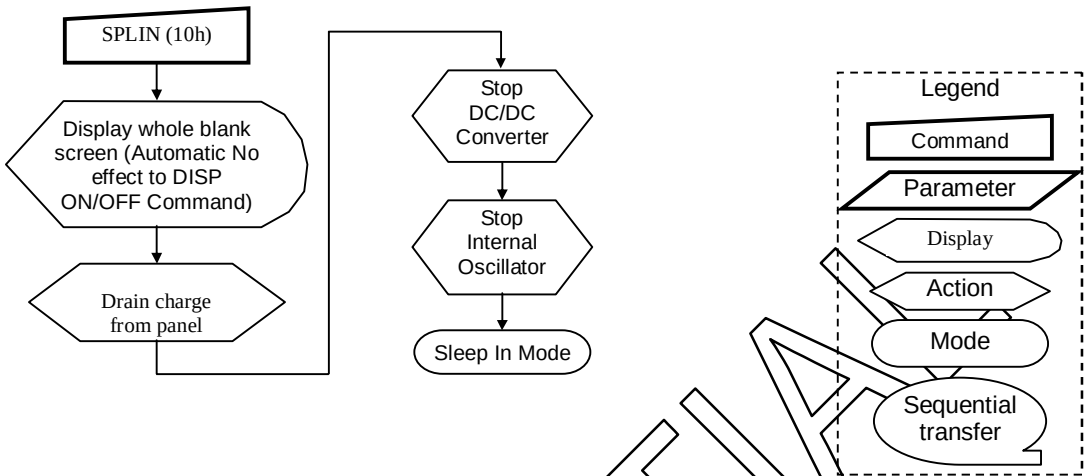
SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												
Description	This command causes the display module to enter the Sleep mode. This command causes the module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal mode.												
Restriction	This command has no effect when the display module is already in Sleep mode. The host processor must wait 5 milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending Sleep Out command before sending Sleep In command.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart



SLPOUT (11h): Sleep Out

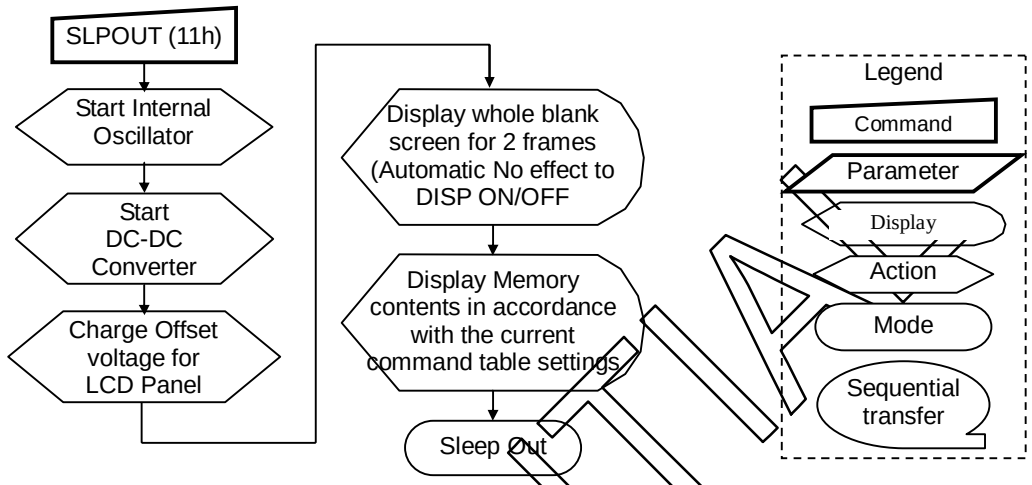
11H	SLPOUT (Sleep Out)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow chart	

PTLON (12h): Partial Display Mode On

<table>
<tr><th>12H</th><th colspan="12">PTLON (Partial Display Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command.
To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial Display Mode is already active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode On</td></tr><tr><td>SW Reset</td><td>Normal display mode On</td></tr><tr><td>HW Reset</td><td>Normal display mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">Refer to Partial Area (30h)</td></tr>
</table>

NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off.												
Restriction	This command has no effect when Normal Display mode is already active.												

Register Availability

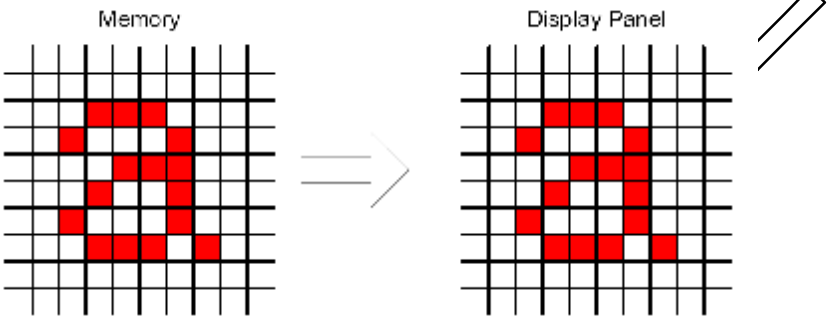
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart: Refer to the description of Partial Area (30h)

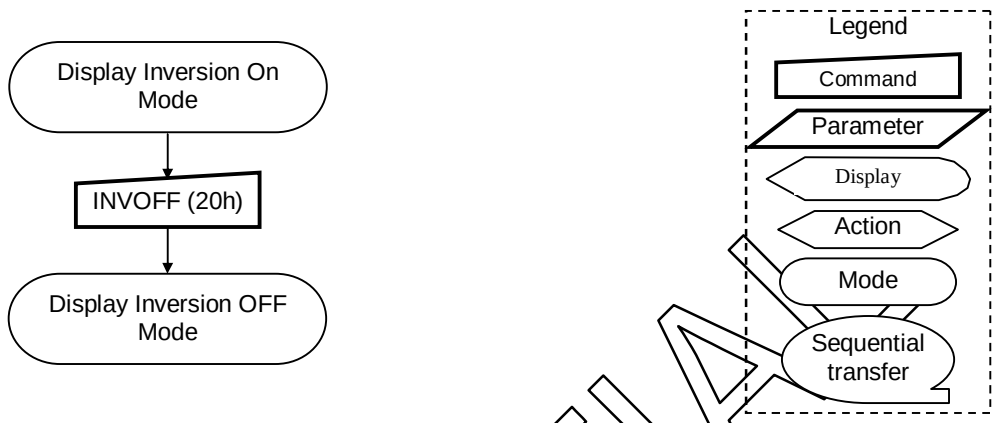
INVOFF (20H): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when the display module is not inverting the display image.												
Register Availability													

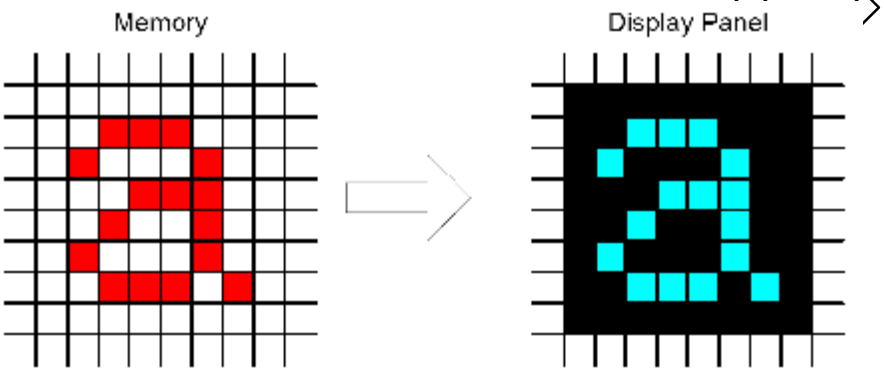
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

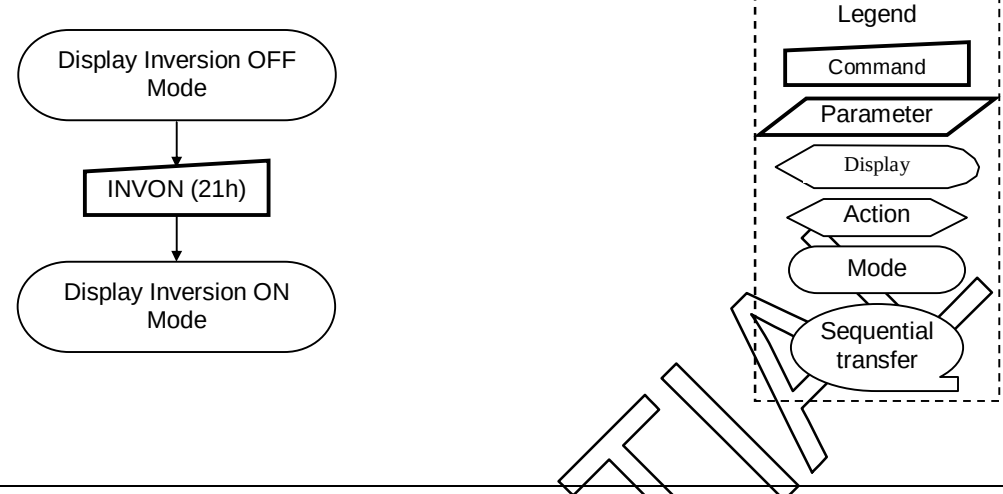
Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

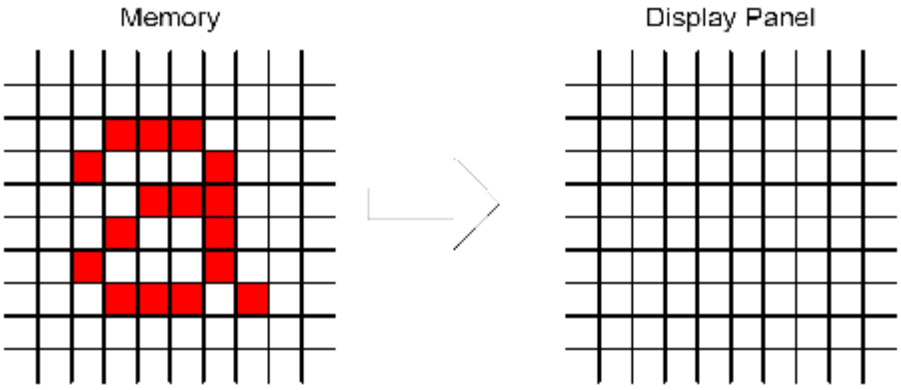
Flow Chart	

INVON (21H): Display Inversion On

21H	INVON (Display Inversion On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes												
Default	Status / Default Value Power On Sequence / Display Inversion off SW Reset / Display Inversion off HW Reset / Display Inversion off												

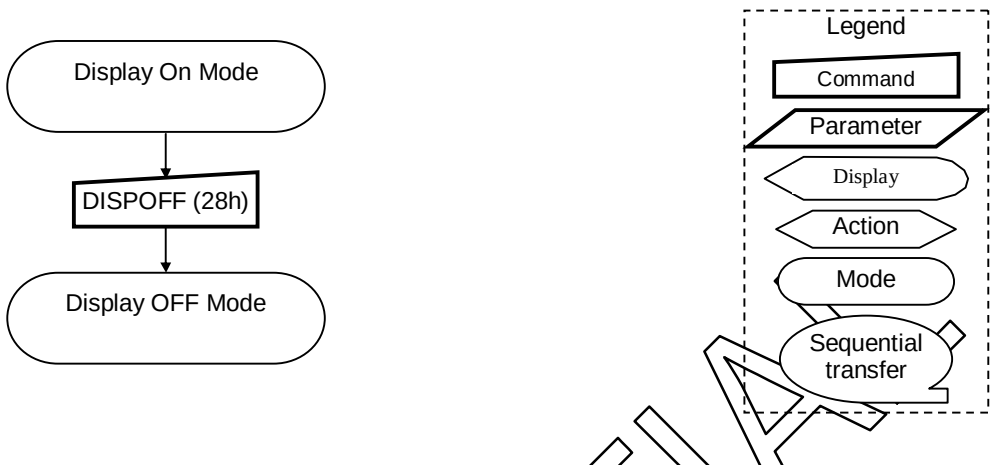
Flow Chart	

DISPOFF (28h): Display Off

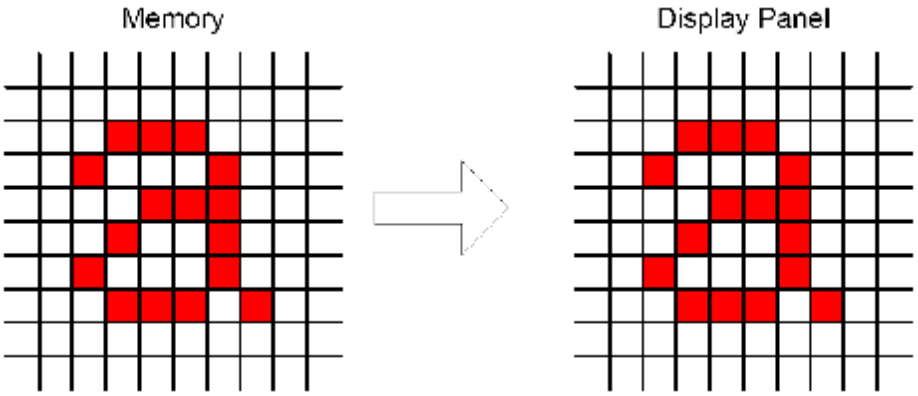
28H	DISPOFF (Display Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display off mode.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart	

DISPON (29h): Display On

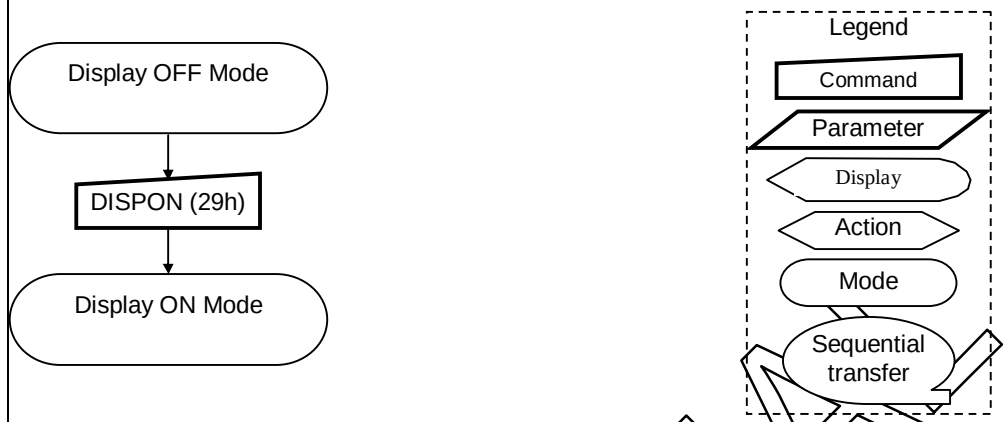
29H	DISPON (Display On)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display on mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

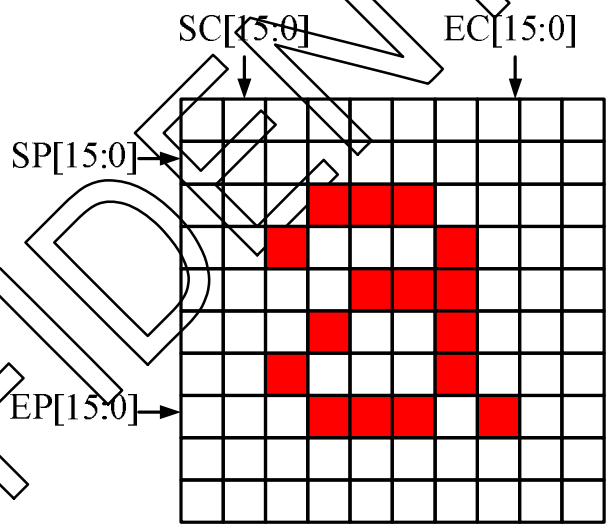
Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	x	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00
2nd parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
3rd parameter	1	1	↑	x	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	01
4th parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	DF
Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. 												
Restriction	SC[15:0] always must be equal to or less than EC[15:0]. Note 1: When SC[15:0] or EC[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh (When MADCTL's B5 = 1), data of out of range will be ignored												

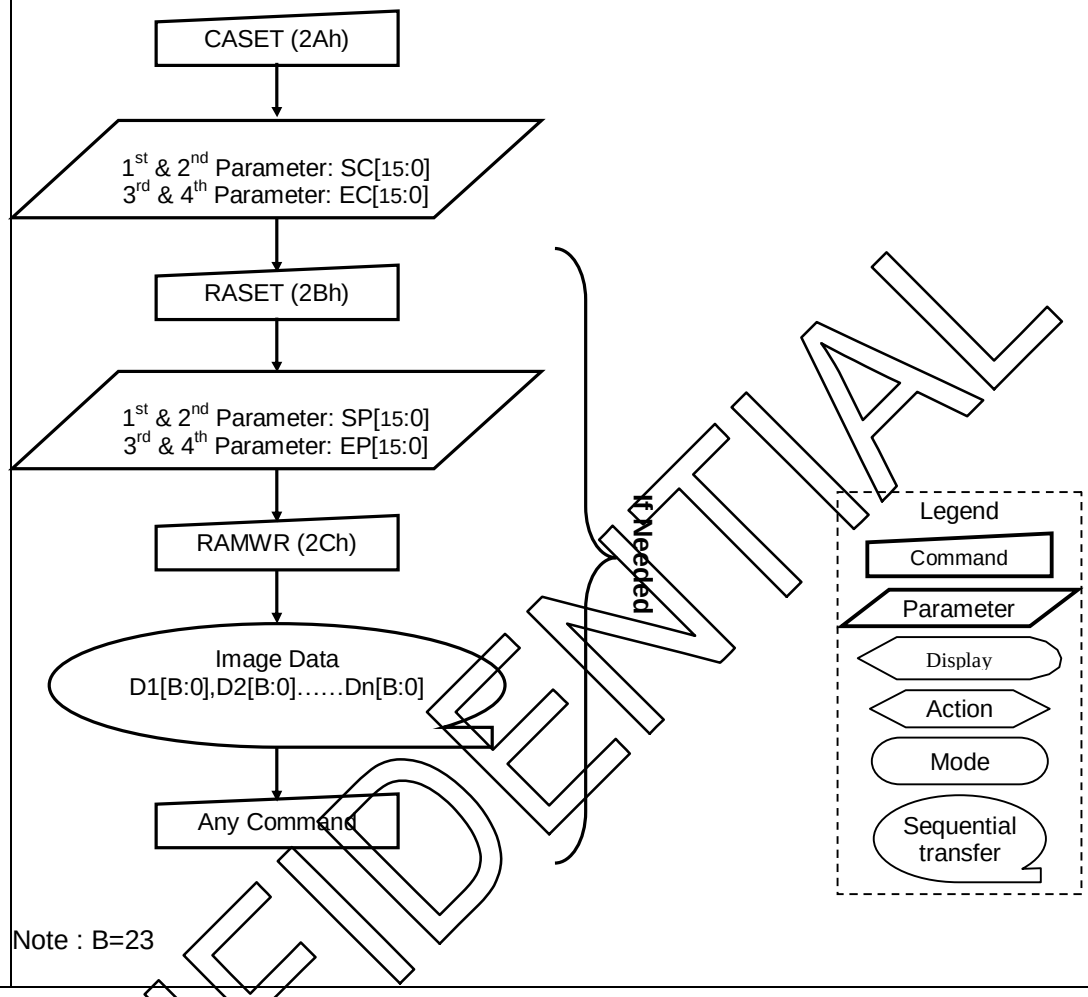
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SC[15:0]	EC[15:0]
Power On Sequence	0000h	00EFh
SW Reset	0000h	013Fh (If MADCTL's B5=0) 01DFh (If MADCTL's B5=1)
HW Reset	0000h	013Fh

Flow chart



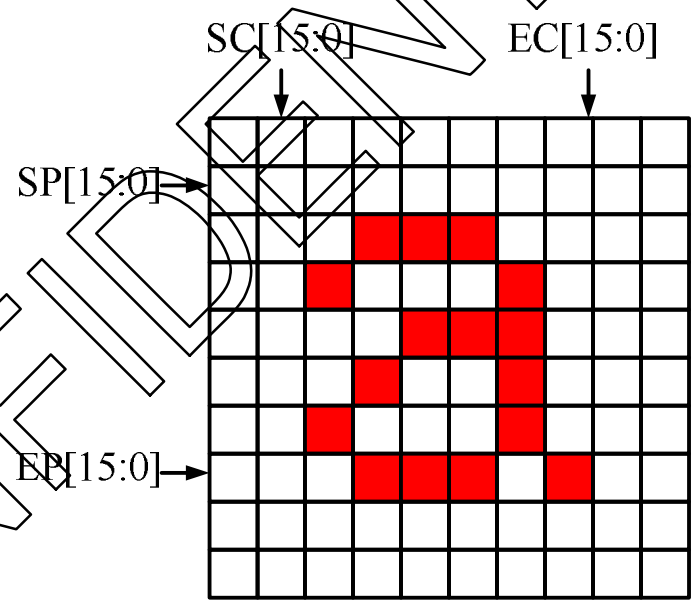
Note : B=23

RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	x	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00
2nd parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
3rd parameter	1	1	↑	x	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	01
4th parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	3F

Description

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

SP[15:0] always must be equal to or less than EP[15:0]

When SP[15:0] or EP[15:0] is greater than 01DFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data ofout of range will be ignored.

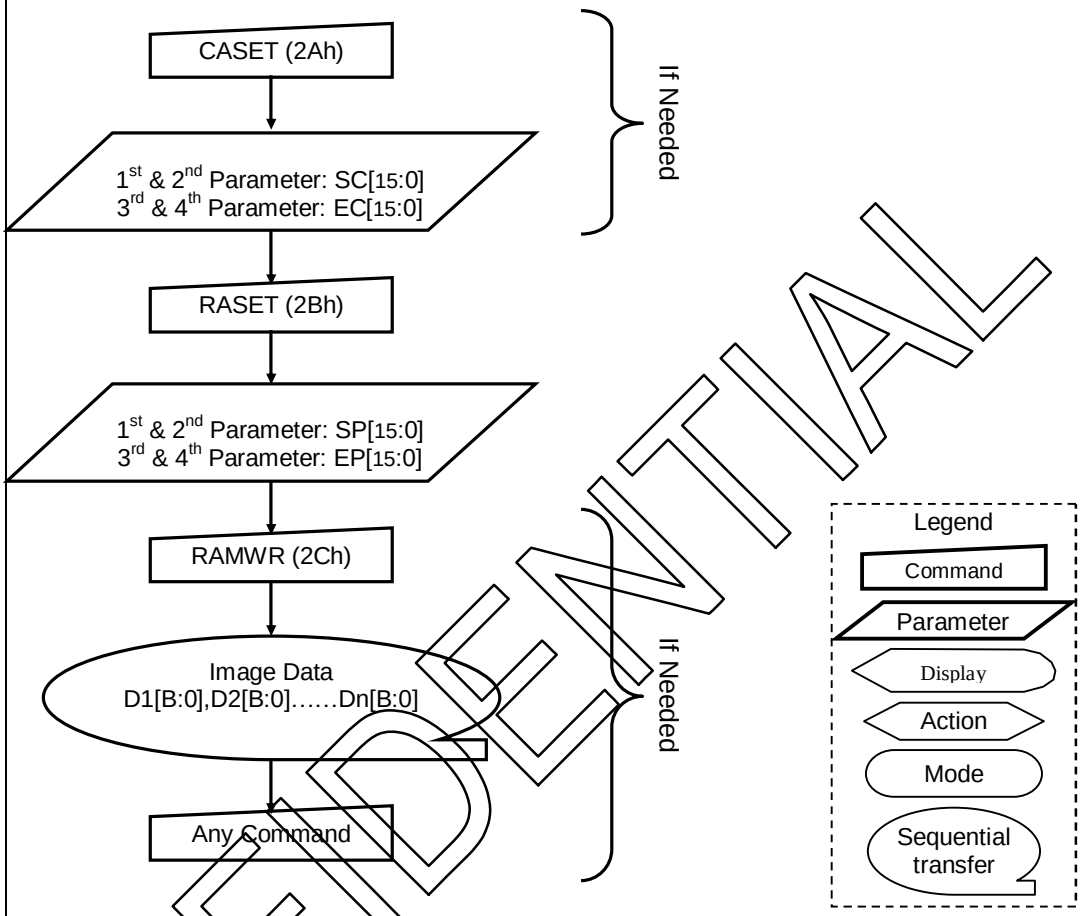
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SP[15:0]	EP[15:0]
Power On Sequence	0000h	013Fh
SW Reset	0000h	01DFh (If MADCTL's B5=0) 013Fh (If MADCTL's B5=1)
HW Reset	0000h	01EFh

Flow chart



Note : B=23

RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C
1st pixel data	1	1	↑	D1[15..8]	D17	D16	D15	D14	D13	D12	D11	D10	XX
:	1	1	↑	Dx[15..8]	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	XX
Nth pixel data	1	1	↑	Dn[15..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	XX
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC+ 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.												
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												

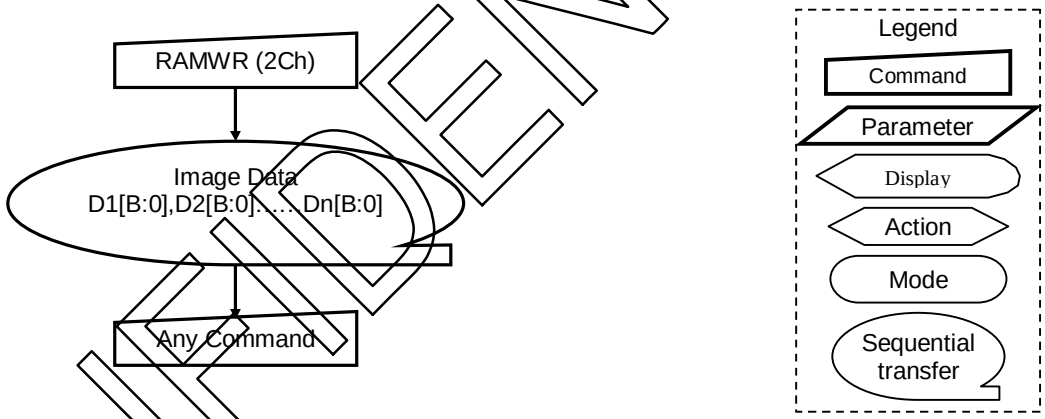
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



RAMRD (2Eh): Memory Read

2EH	RAMRD (Memory Read)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	D1[15..8]	D17	D16	D15	D14	D13	D12	D11	D10	
:	1	↑	1	Dx[15..8]	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	
(N+1)th parameter	1	↑	1	Dn[15..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	There is no restriction on length of parameters.												

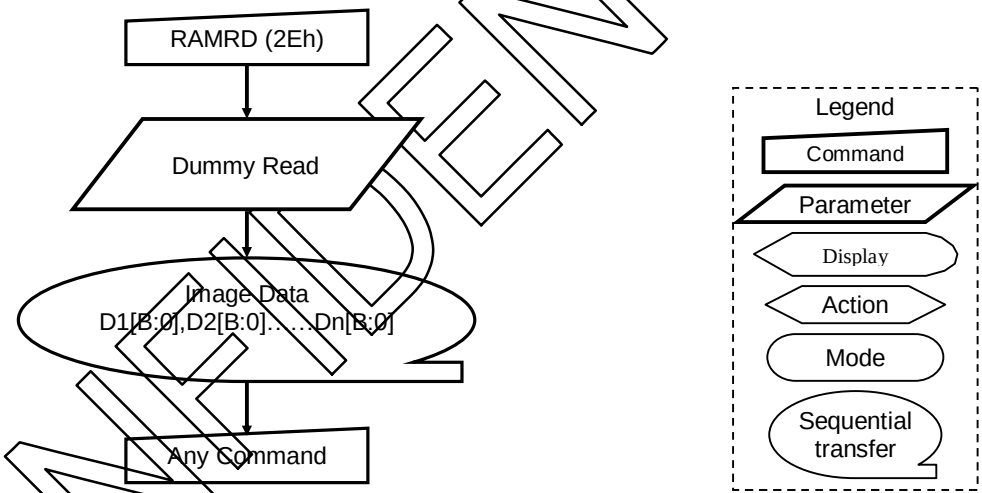
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

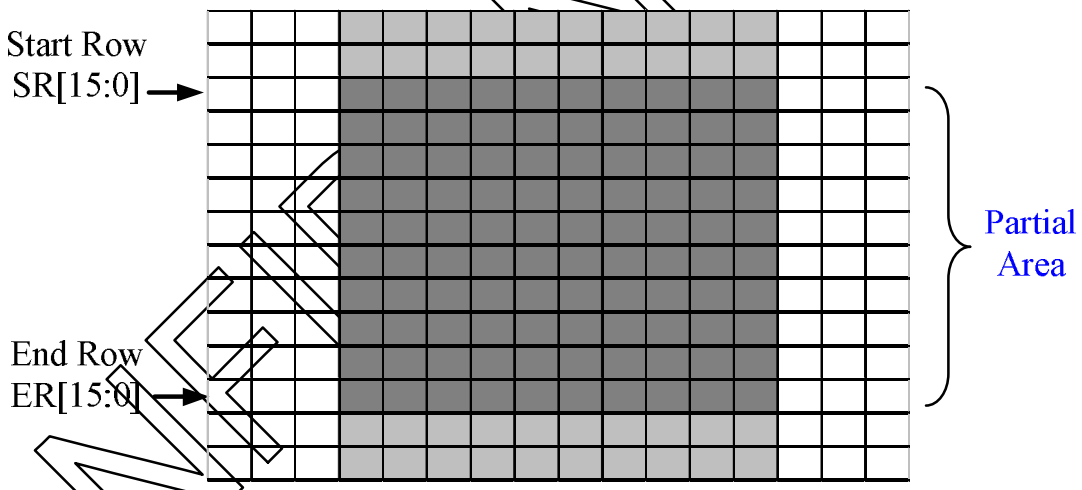
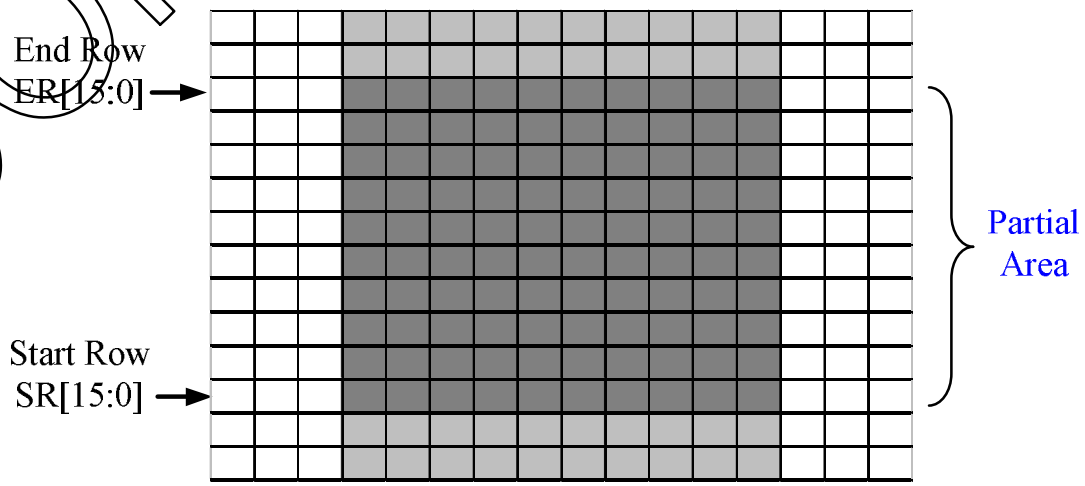
Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

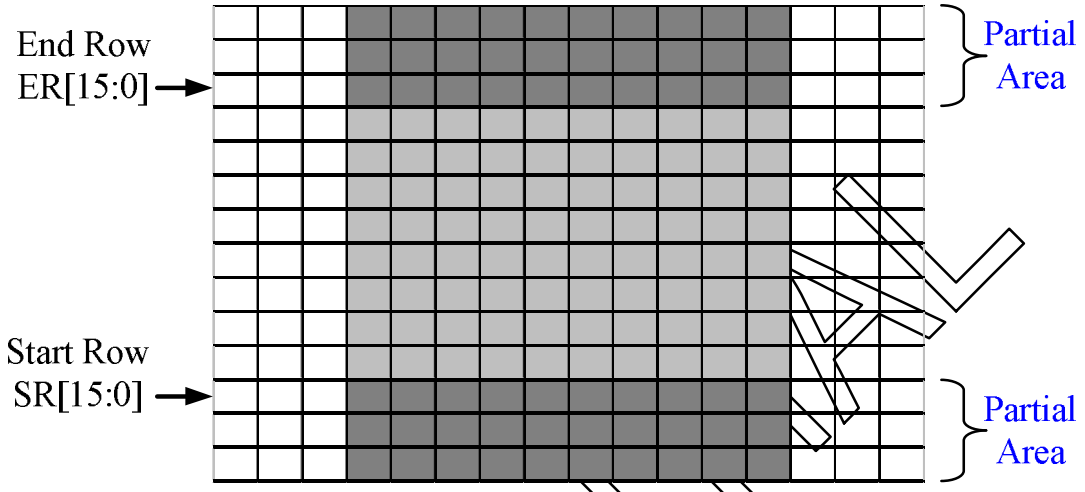
Flow chart



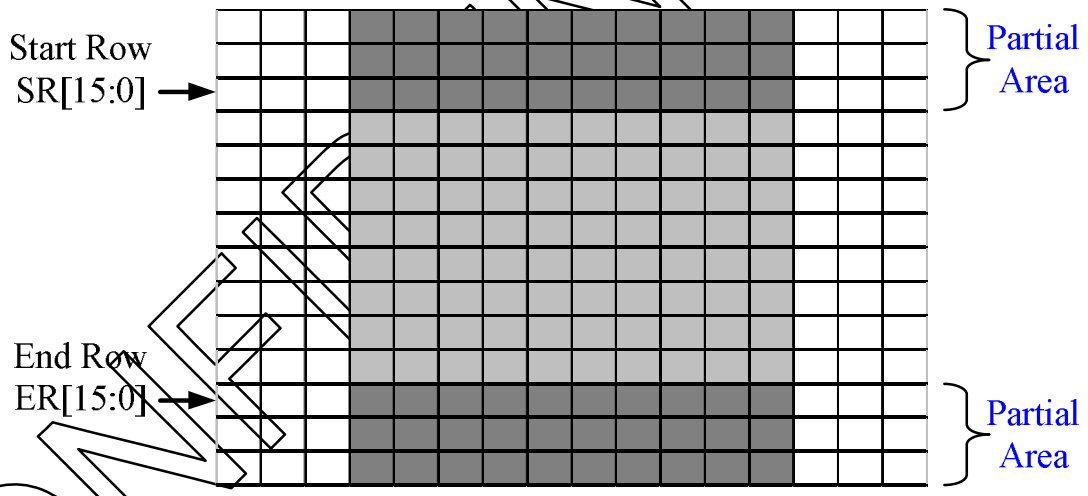
PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	x	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd parameter	1	1	↑	x	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	DF
Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory. -If End Row > Start Row, when ML(36h-B4) ='0'  -If End Row > Start Row, when ML(36h-B4) ='1'  													

-If End Row < Start Row, when ML(36h-B4) ='0'



-If End Row < Start Row, when ML(36h-B4) ='1'



-If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).

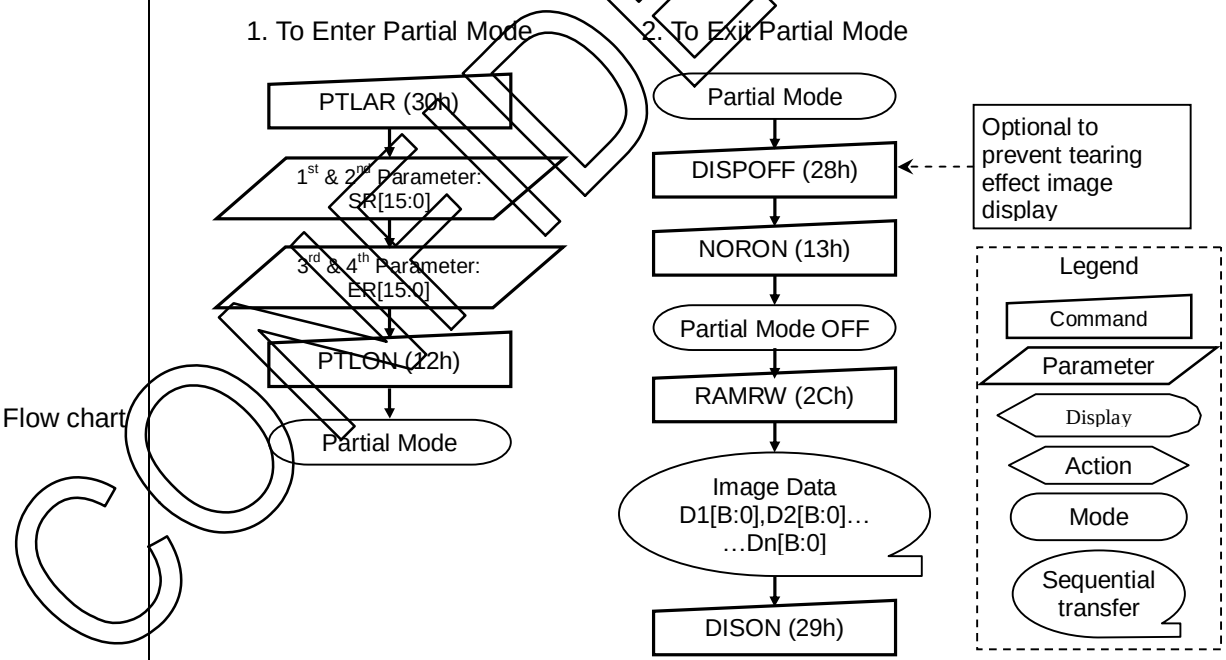
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

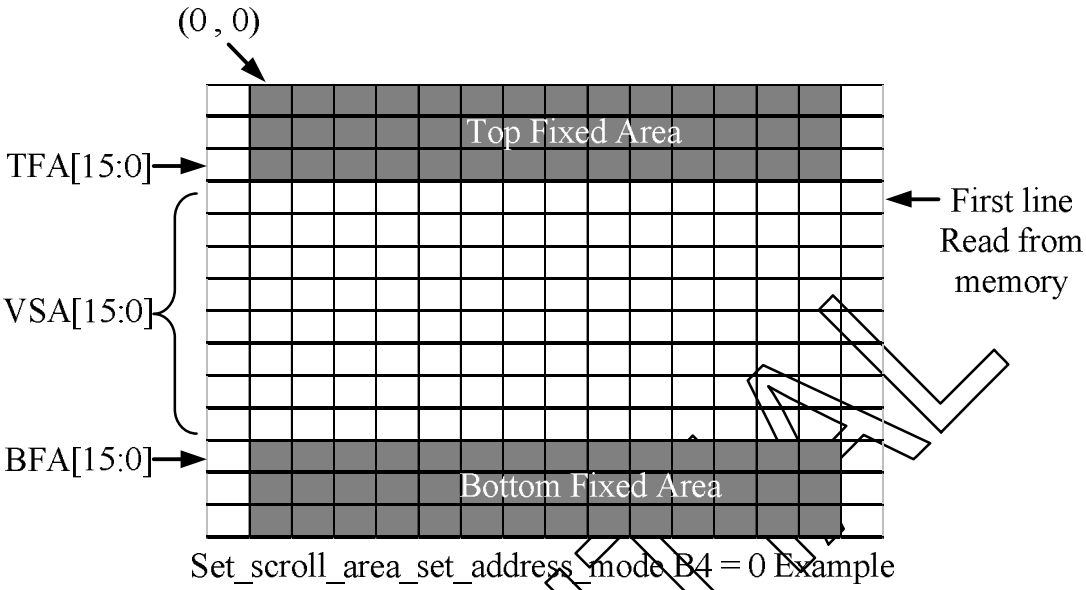
Status	Default Value	
	SR[15:0]	ER[15:0]
Power On Sequence	0000h	01DFh
SW Reset	0000h	01DFh
HW Reset	0000h	01DFh

Flow chart



VSCRDEF (33h): Vertical Scrolling Definition

33H	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	x	TFA[15]	TFA[14]	TFA[13]	TFA[12]	TFA[11]	TFA[10]	TFA[9]	TFA[8]	xx
2nd parameter	1	1	↑	x	TFA[7]	TFA[6]	TFA[5]	TFA[4]	TFA[3]	TFA[2]	TFA[1]	TFA[0]	xx
3rd parameter	1	1	↑	x	VSA[15]	VSA[14]	VSA[13]	VSA[12]	VSA[11]	VSA[10]	VSA[9]	VSA[8]	xx
4th parameter	1	1	↑	x	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]	xx
5th parameter	1	1	↑	x	BFA[15]	BFA[14]	BFA[13]	BFA[12]	BFA[11]	BFA[10]	BFA[9]	BFA[8]	xx
6th parameter	1	1	↑	x	BFA[7]	BFA[6]	BFA[5]	BFA[4]	BFA[3]	BFA[2]	BFA[1]	BFA[0]	xx
Description	This command defines the display vertical scrolling area. Memory Data Access Control (36h) B4 = 0: The 1st & 2nd parameter, TFA[15:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[15:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area. The 5th & 6th parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned. TFA, VSA and BFA refer to the Frame Memory Line Pointer.												



Set_scroll_area_set_address_mode B4 = 0 Example

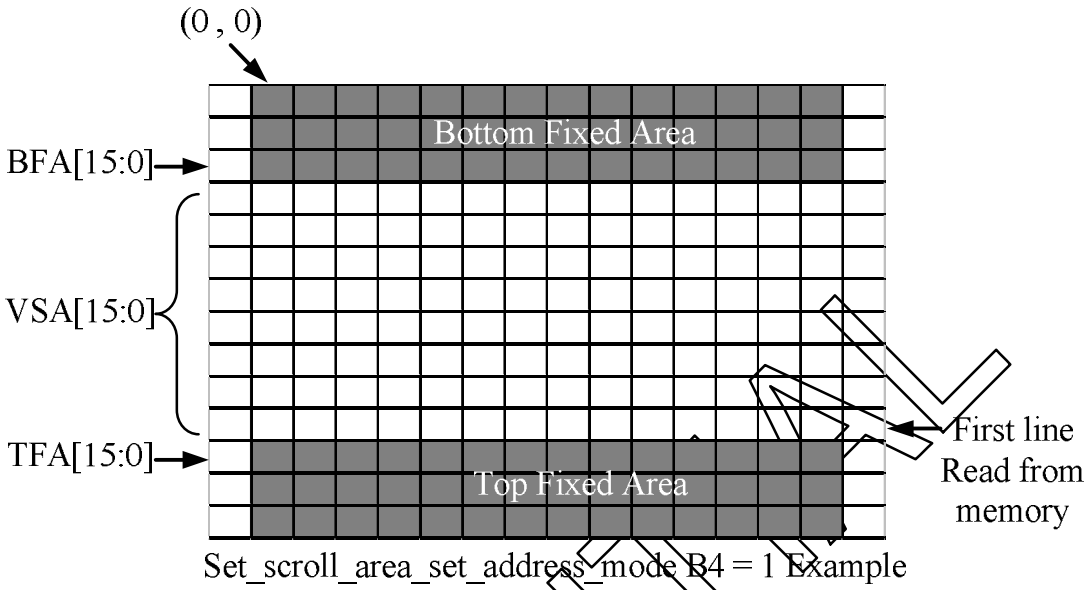
Memory Data Access Control (36h) B4 = 1:

The 1st & 2nd parameter, TFA[15:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[15:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[15:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory.
The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

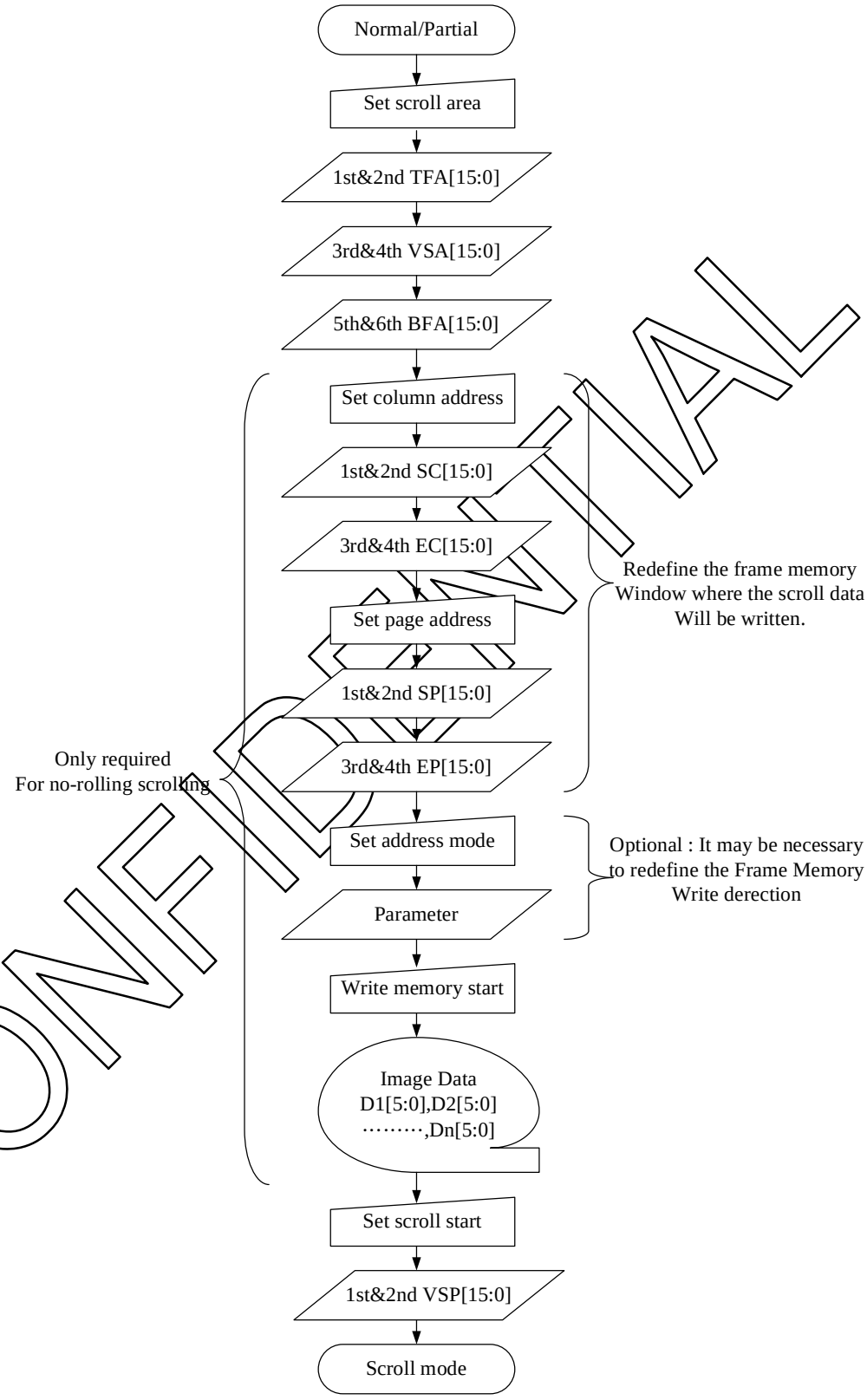


Set_scroll_area_set_address_mode B4 = 1 Example

<table>
<tr><td>Restriction</td><td>The sum of TFA, VSA and BFA must equal the number of the display device’s horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to ‘0’ – this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="3">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>TFA[15:0]=0000HEX</td><td>VSA[15:0]=01E0HEX</td><td>BFA[15:0]=0000HEX</td></tr>
<tr><td>SW Reset</td><td>TFA[15:0]=0000HEX</td><td>VSA[15:0]=01E0HEX</td><td>BFA[15:0]=0000HEX</td></tr>
<tr><td>HW Reset</td><td>TFA[15:0]=0000HEX</td><td>VSA[15:0]=01E0HEX</td><td>BFA[15:0]=0000HEX</td></tr>
</table>
</td></tr>
</table>

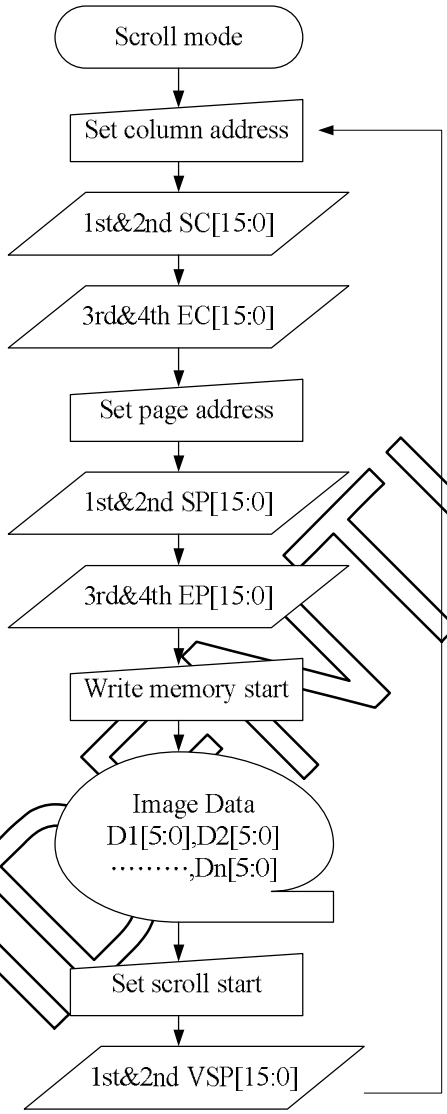
Flow chart

1. To enter vertical scroll mode:

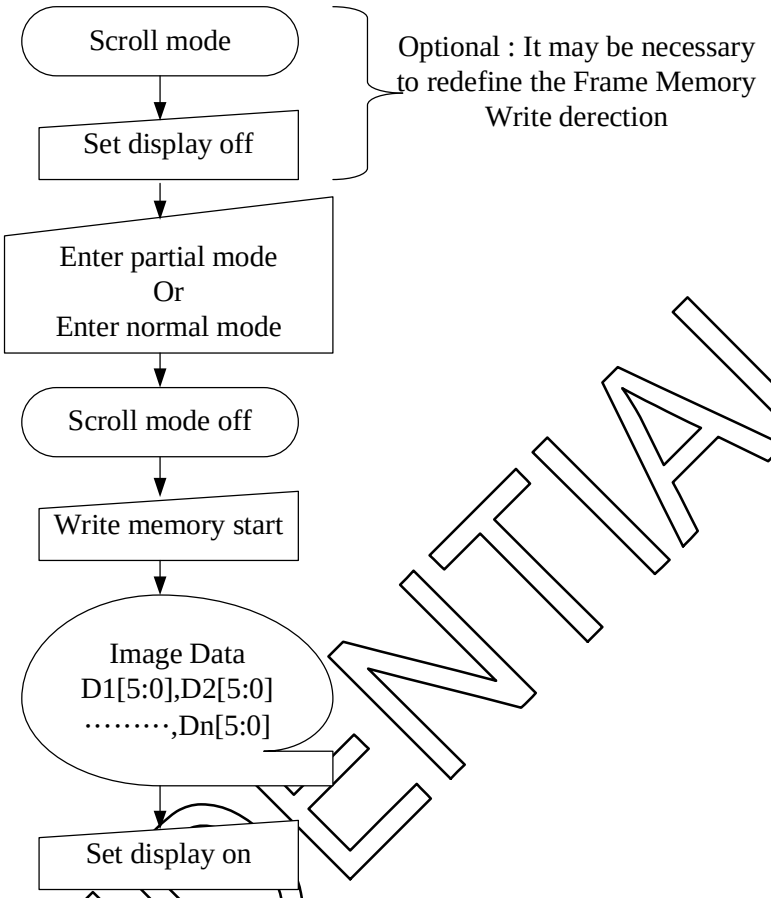


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

2. Continuous scroll:



3. To leave vertical scroll mode:



TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												

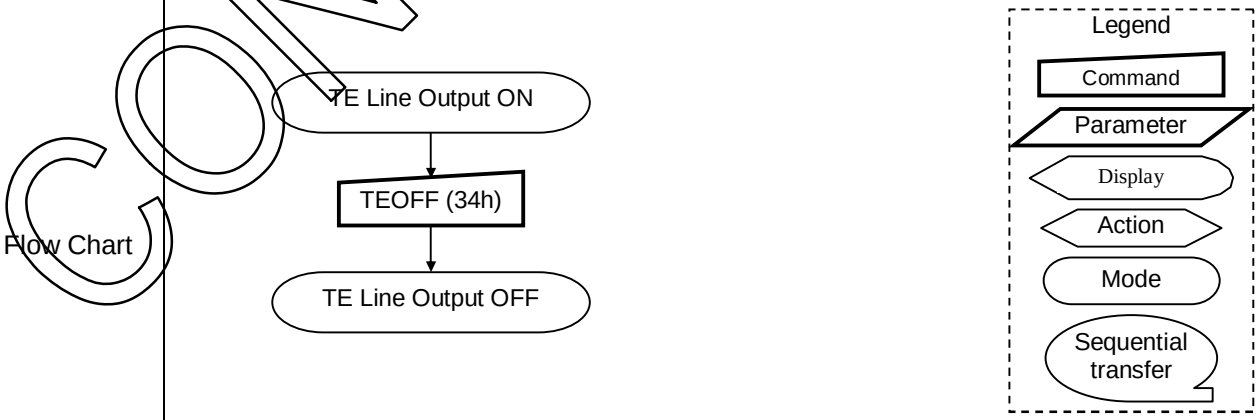
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	TELOM	00

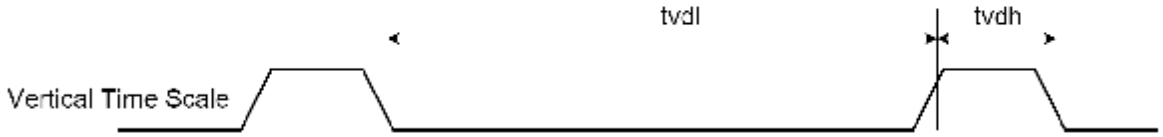
Description

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

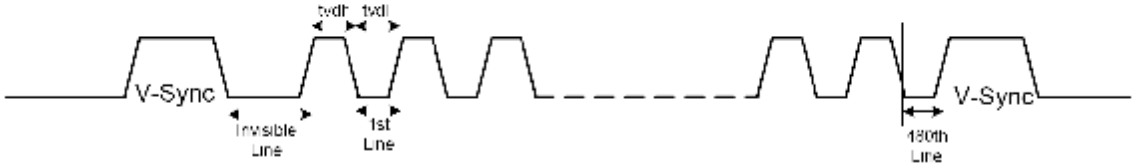
If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.



If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command has no effect when Tearing Effect output is already ON.

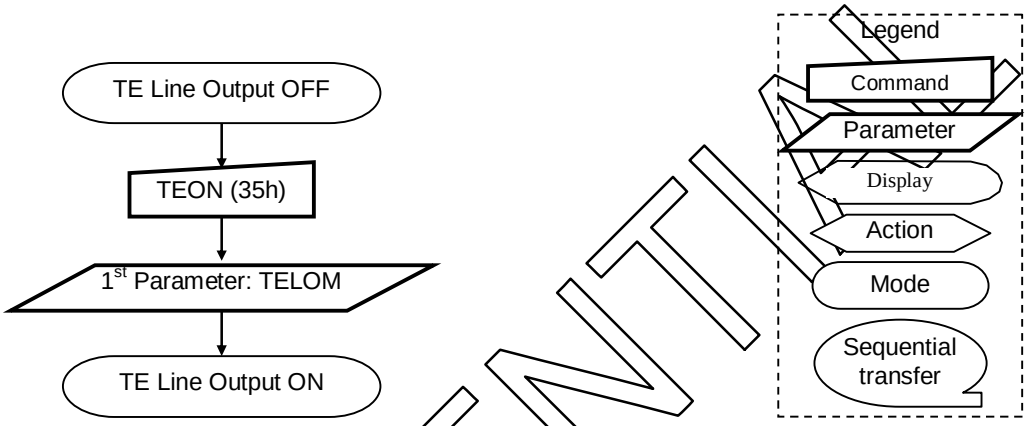
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



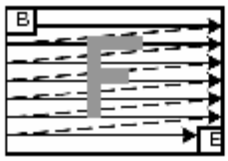
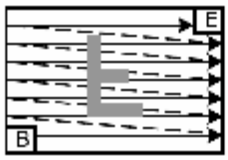
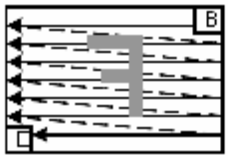
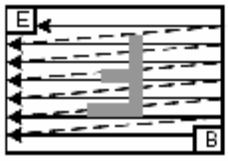
MADCTR (36h): Memory Data Access Control

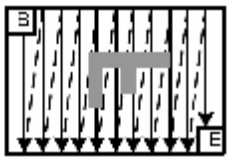
36H	MADCTR (Memory Data Access Control)												
	DCX	RDX	WRX	D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	x	B7	B6	B5	B4	B3	B2	B1	B0	00

Description

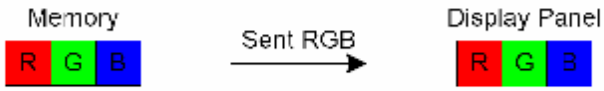
This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
B7	MY	Row Address Order	'1' = Bottom to Top '0' = Top to Bottom
B6	MX	Column Address Order	'1' = Right to Left '0' = Left to Right
B5	MV	Row/Column Order (MV)	'1' = Row/column exchange '0' = Normal
B4	ML	Vertical Refresh Order	'0' =LCD Refresh Top to Bottom '1' =LCD Refresh Bottom to Top
B3	RGB	RGB/BGR Order	"1" =BGR, "0"=RGB
B2	MH	Horizontal Refresh Order	'0' =LCD Refresh Left to Right '1' =LCD Refresh Right to Left
B1	H_FLIP	Horizontal Flip	'0' = Normal display '1' = Flipped display
B0	V_FLIP	Vertical Flip	'0' = Normal display '1' = Flipped display

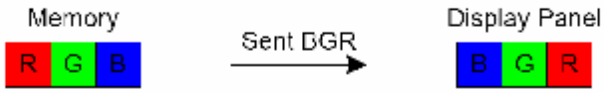
B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B3 = 0



B3 = 1



Restriction	

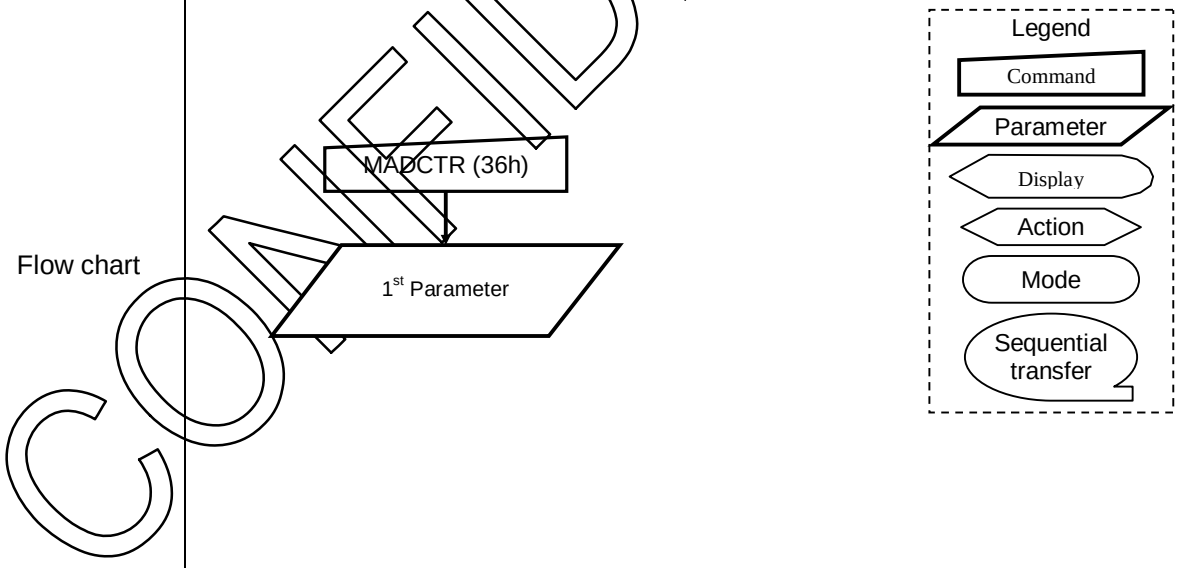
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow chart



VSCRSADD (37h): Vertical Scrolling Start Address

37H	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP8	xx
2nd parameter	1	1	↑	x	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	xx

Description

This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command

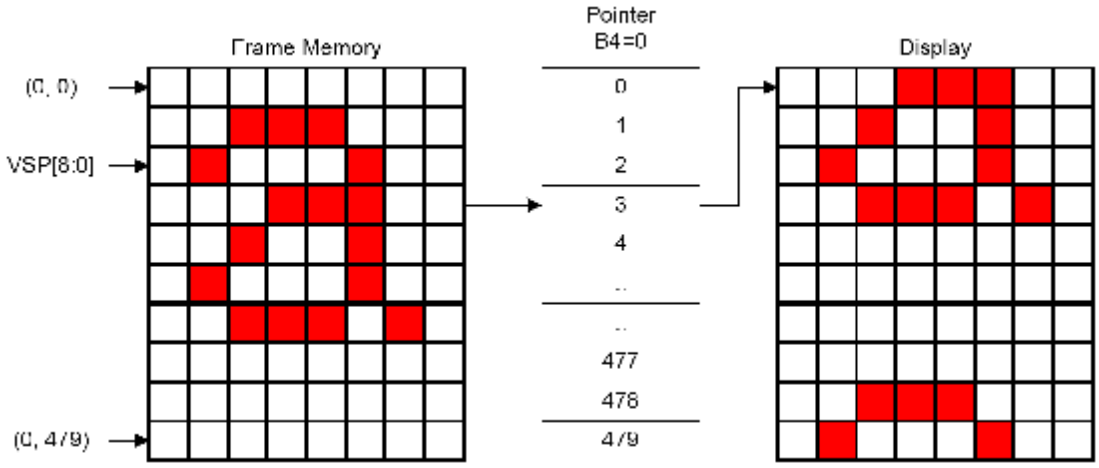
The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.

The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.

If set_address_mode (R36h) B4 = 0:

Example:

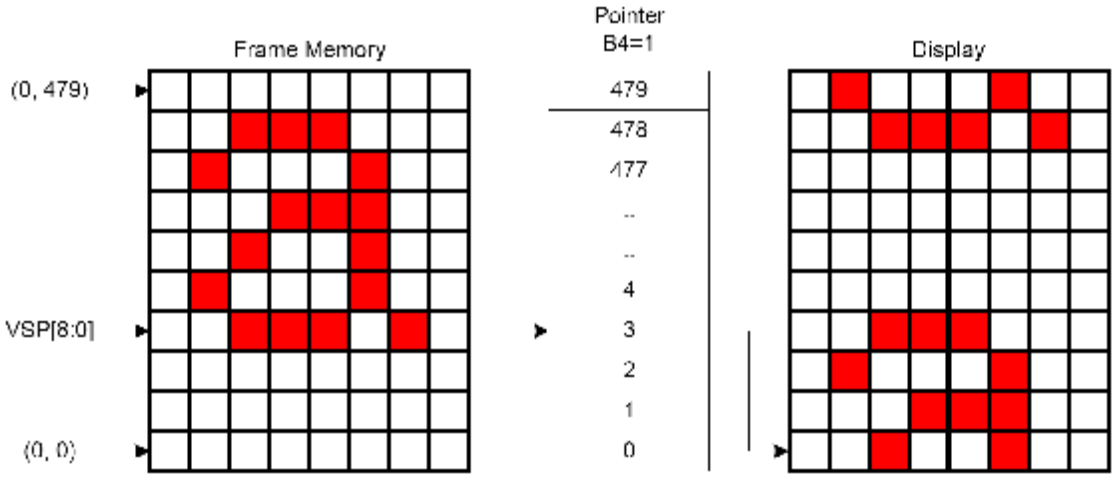
When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 480 and VSP = 3.



If set_address_mode (R36h) B4 = 1:

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.



Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

<table>
<tr><td>Restriction</td><td>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000HEX</td></tr>
<tr><td>SW Reset</td><td>0000HEX</td></tr>
<tr><td>HW Reset</td><td>0000HEX</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td>Refer to the description Vertical Scrolling Definition (33h)</td></tr>
</table>

IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												

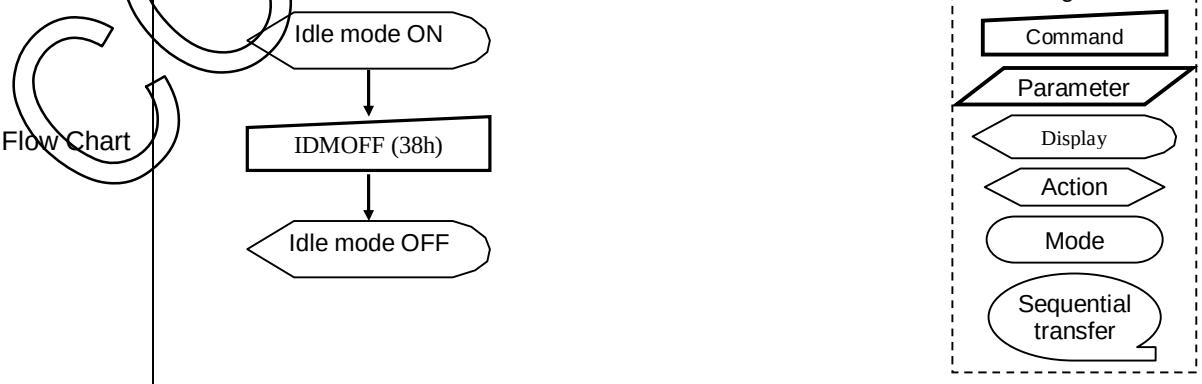
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

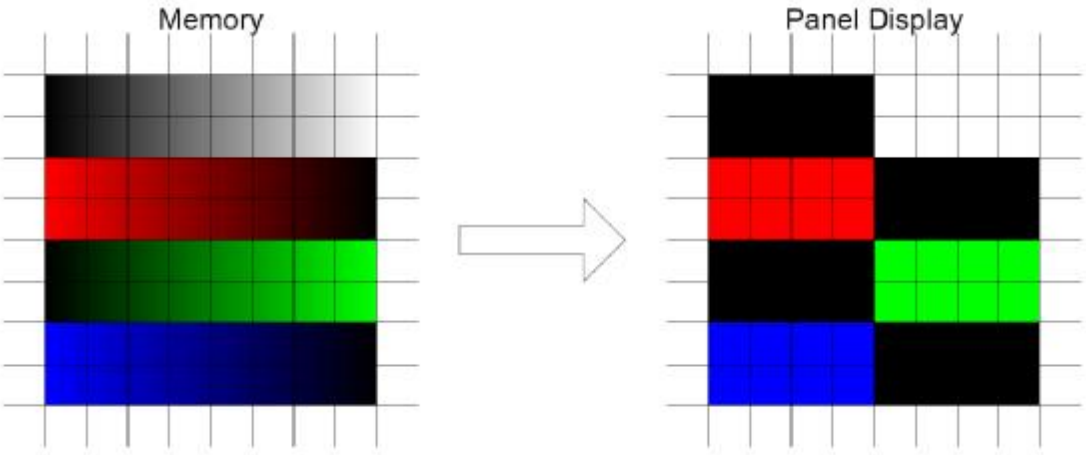
Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



IDMON (39h): Idle Mode ON

39H	IDMON (Idle Mode ON)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												
Description	This command causes the display module to enter Idle Mode. In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.												
Restriction	This command has no effect when module is already in idle on mode.												



Color	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

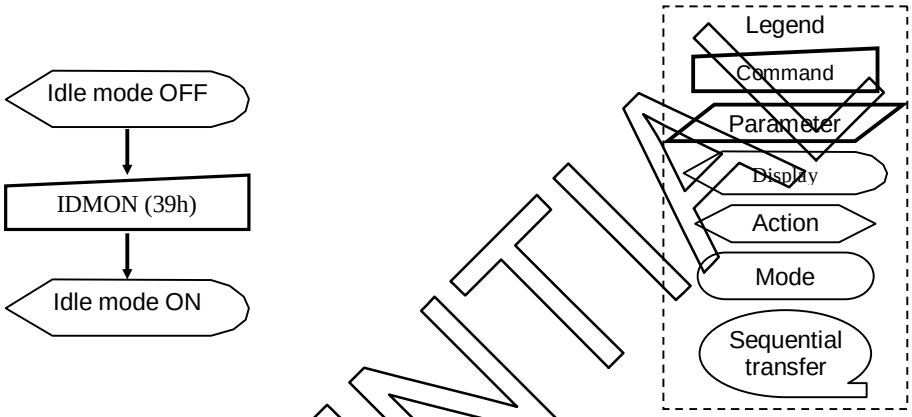
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	x	0	D6	D5	D4	0	D2	D1	D0	66

Description

This command sets the pixel format for the RGB image data used by the interface.

Bits D[6:4] – DPI Pixel Format Definition

Bits D[2:0] – DBI Pixel Format Definition

Bits D7 and D3 are not used.

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
Reserved	0	1	1
Reserved	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Reserved	1	1	1

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

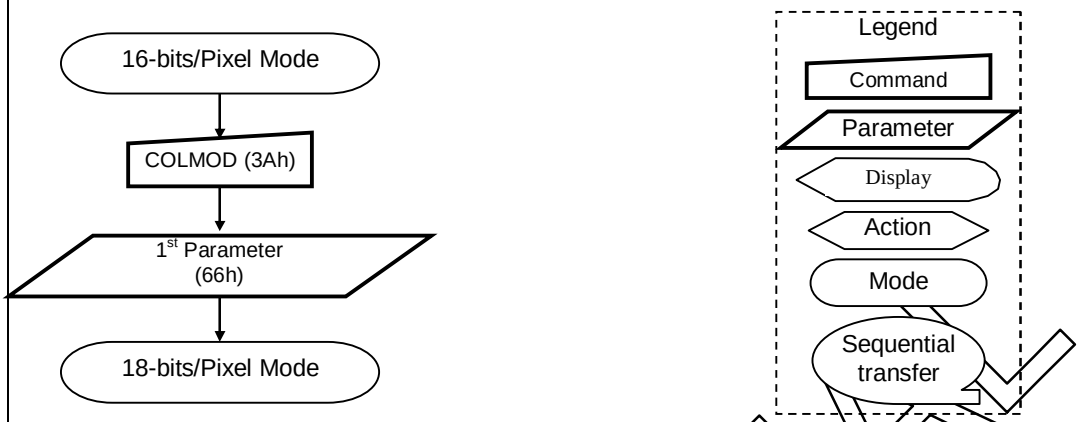
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
SW Reset	66h
HW Reset	66h

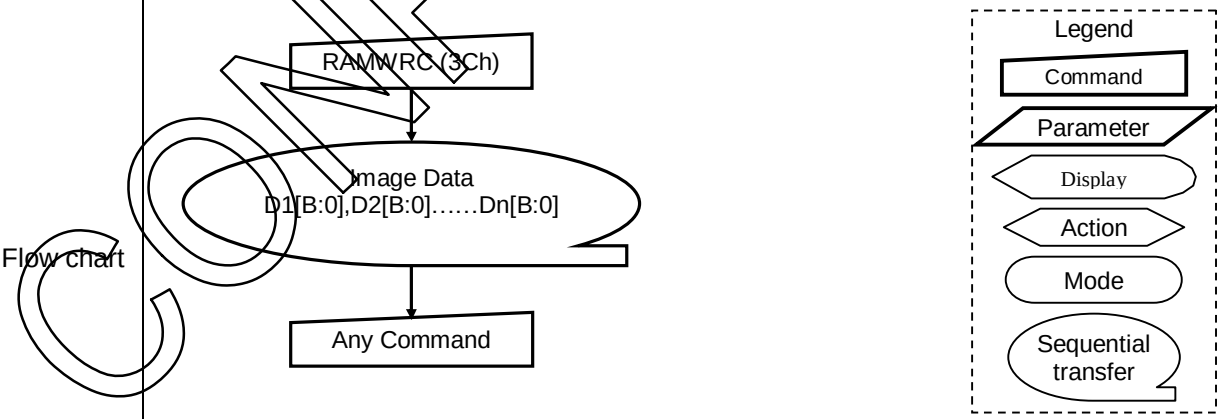
Flow chart

Example :



RAMWRC (3Ch) : Write_Memory_Continue

3CH	Write_Memory_Continue												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	D1[15..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	XX
Xst parameter	1	1	↑	Dx[15..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	XX
Nst parameter	1	1	↑	Dn[15..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	XX
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If MV(36h-B5) = 0: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.												

<table>
<tr><td></td><td>Frame Memory Access and Interface setting (B3h), WEMODE=1
When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.</td></tr>
<tr><td>Restriction</td><td>A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td> 
</td></tr>
</table>

RAMRDC (3Eh) : Read_Memory_Continue

3EH	Read_Memory_Continue												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	D1[15..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	XX
Xst parameter	1	↑	1	Dx[15..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	XX
Nst parameter	1	↑	1	Dn[15..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	XX
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If MV(36h-B5) = 0: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	A Memory Read should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMRD(2Eh) and any following RAMRDC(3Eh) commands is written to undefined locations.												

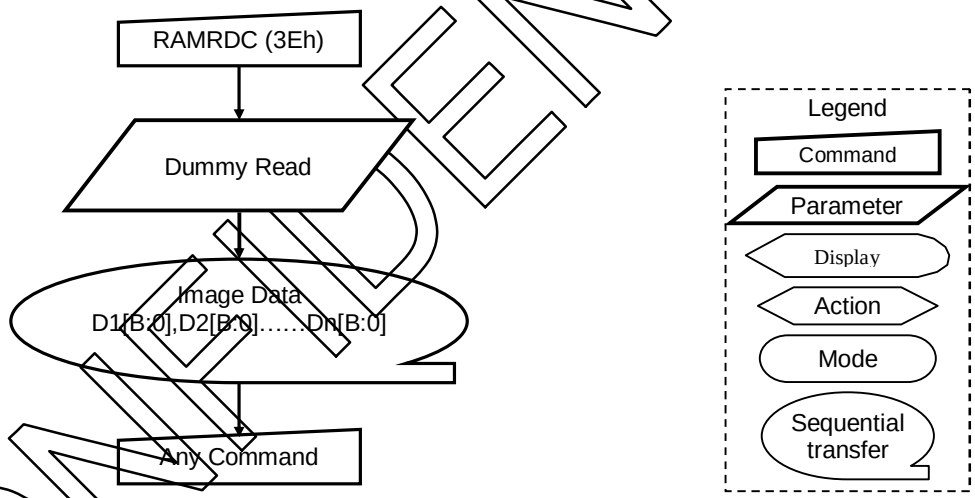
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow chart



TESLWR (44h) : Write Tear Scan Line

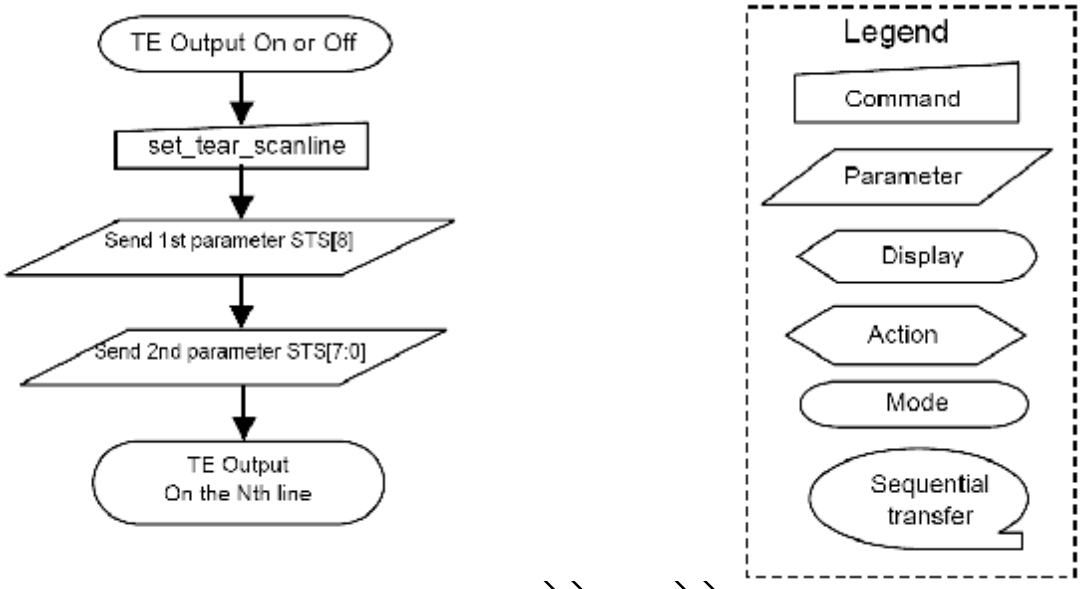
44H	TESLWR (Write Tear Scan line)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS[8]	00
2nd parameter	1	1	↑	xx	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.  The Tearing Effect Output line shall be active low when the display module is in Sleep mode.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS[8:0]=9'h000
SW Reset	No change
HW Reset	STS[8:0]=9'h000

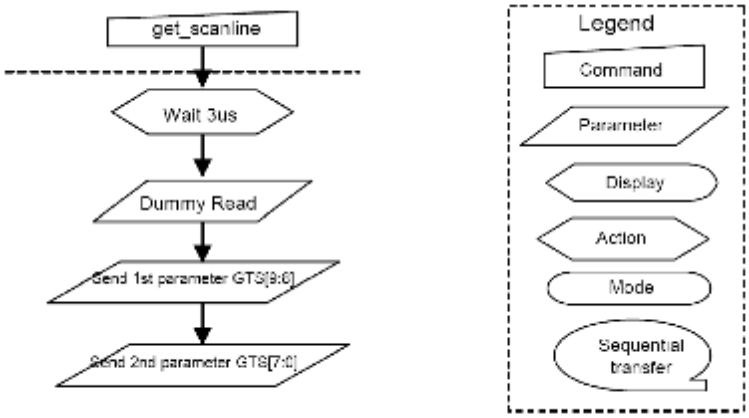
Flow Chart	

TESLRD (45h) : Read Tear Scan Line

45H	TESLRD (Read Tear Scan Line)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS[8]	0x
3rd parameter	1	↑	1	xx	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart



WRDISBV (51h): Write Display Brightness

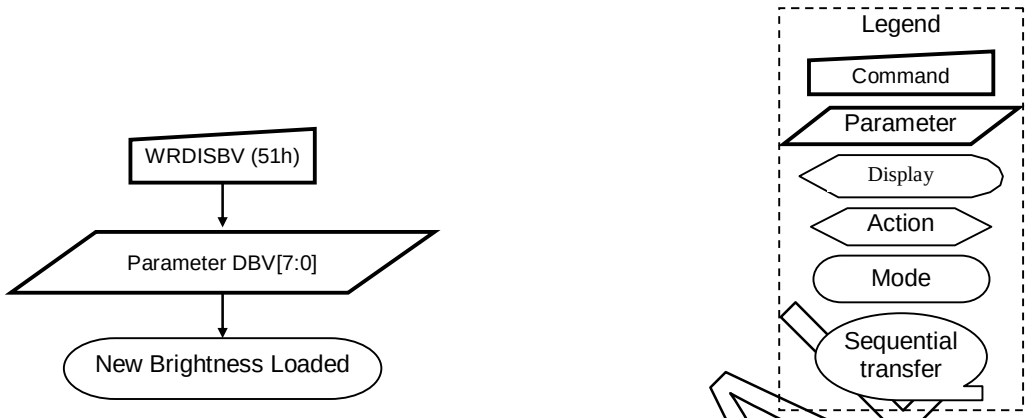
51H	WRDISBV (Write Display Brightness)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	The display supplier cannot use this command for tuning												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart	

RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	-												

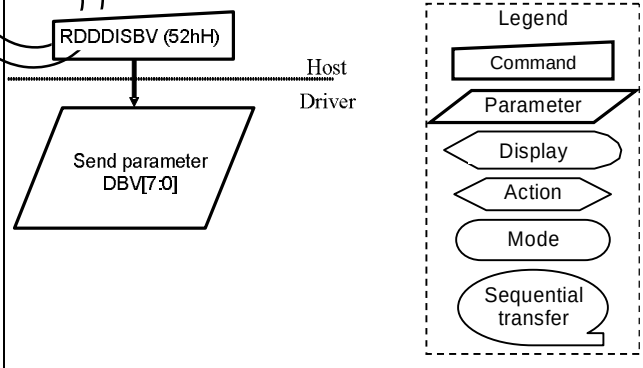
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRCTRLD (53h): Write CTRL Display

<table>
<tr><th>53H</th><th colspan="12">WRCTRLD (White CTRL Display)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>BCTRL</td><td>x</td><td>DD</td><td>BL</td><td>x</td><td>x</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

<table>
<tr><td>BCTRL</td><td>DESCRIPTION LEDPWM Pin</td><td>DESCRIPTION LEDPWM Pin</td></tr>
<tr><td>0</td><td>Off,
DBV[7:0] and KBV[7:0] are 00h.</td><td>LEDPWPOL=”0”: keep low (0%)
LEDPWPOL=”1”: keep high (0%)</td></tr>
<tr><td>1</td><td>On,
DBV[7:0] and KBV[7:0] are active</td><td>LEDPWPOL=”0”: PWM output (high level is duty)
LEDPWPOL=”1”: PWM output (low level is duty)</td></tr>
</table>

DD: Display Dimming Control On/Off

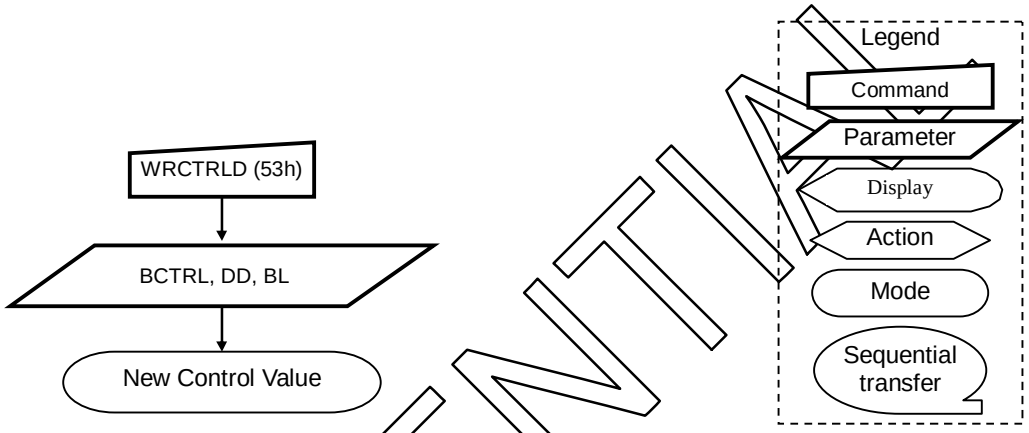
<table>
<tr><td>DD</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>Display dimming is off</td></tr>
<tr><td>1</td><td>Display dimming is on</td></tr>
</table>

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if dimming on (DD=”1”) is selected.

<table>
<tr><td>BL</td><td>DESCRIPTION</td><td>LEDON Pin</td></tr>
<tr><td>0</td><td>Off</td><td>LEDONPOL=”0”: keep low (non-lit)
LEDPWPOL=”1”: keep high (non-lit)</td></tr>
<tr><td>1</td><td>On</td><td>LEDPWPOL=”0”: keep high (lit)
LEDPWPOL=”1”: PWM output (lit)</td></tr>
</table>

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=”1”, e.g. BCTRL: 0→1 or 1→0.</td></tr>
<tr><td>Restriction</td><td colspan="12">The display supplier cannot use this command for tuning</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td> 
</td></tr>
</table>

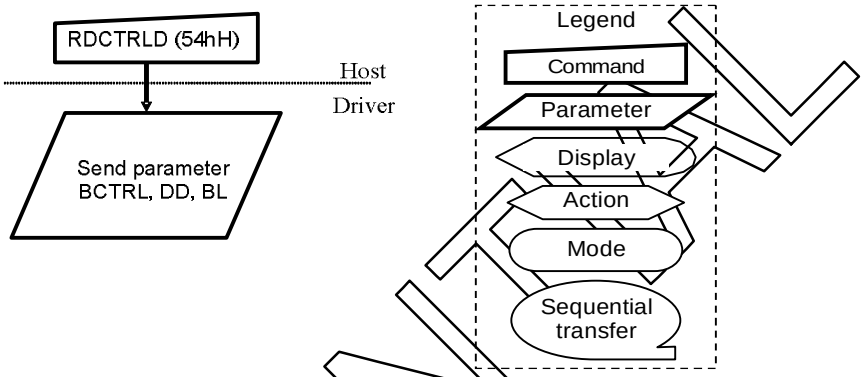
RDCTRLD (54h): Read CTRL Display Value

<table>
<tr><th>54H</th><th colspan="13">RDCTRLD</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>54</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>0</td><td>0</td><td>BCTRL</td><td>x</td><td>DD</td><td>BL</td><td>x</td><td>x</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to control ambient light, brightness and gamma setting.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).
<table>
<tr><td>BCTRL</td><td>DESCRIPTION LEDPWM Pin</td><td>DESCRIPTION LEDPWM Pin</td></tr>
<tr><td>0</td><td>Off,
DBV[7:0] and KBV[7:0] are 00h.</td><td>LEDPWPOL=”0”: keep low (0%)
LEDPWPOL=”1”: keep high (0%)</td></tr>
<tr><td>1</td><td>On,
DBV[7:0] and KBV[7:0] are active</td><td>LEDPWPOL=”0”: PWM output (high level is duty)
LEDPWPOL=”1”: PWM output (low level is duty)</td></tr>
</table>
DD: Display Dimming Control On/Off
<table>
<tr><td>DD</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>Display dimming is off</td></tr>
<tr><td>1</td><td>Display dimming is on</td></tr>
</table>
BL: Backlight Control On/Off without Dimming Effect
When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if dimming on (DD=”1”) is selected.
<table>
<tr><td>BL</td><td>DESCRIPTION</td><td>LEDON Pin</td></tr>
<tr><td>0</td><td>Off</td><td>LEDONPOL=”0”: keep low (non-lit)
LEDPWPOL=”1”: keep high (non-lit)</td></tr>
<tr><td>1</td><td>On</td><td>LEDPWPOL=”0”: keep high (lit)
LEDPWPOL=”1”: PWM output (lit)</td></tr>
</table>
The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=”1”, e.g. BCTRL: 0→1 or 1→0.</td></tr>
<tr><td>Restriction</td><td colspan="13">The display supplier cannot use this command for tuning</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRCABC (55h): Write Content Adaptive Brightness Control

55H	WRCABC (Write Content Adaptive Brightness Control)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	x	0	0	0	0	0	0	C1	C0	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	UI Mode
1	0	Still Mode
1	1	Moving Mode

Restriction

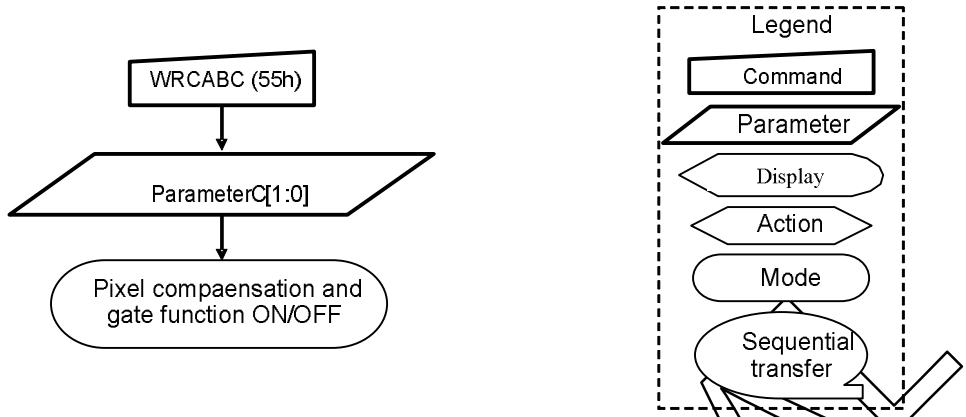
This register is synchronized with V-sync by internal circuit.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart	

RDCABC (56h): Read Content Adpative Brightness Control

56H	RDCABC (Read Content Adpative Brightness Control)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	x	0	0	0	0	0	0	C1	C0	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	UI Mode
1	0	Still Mode
1	1	Moving Mode

Restriction

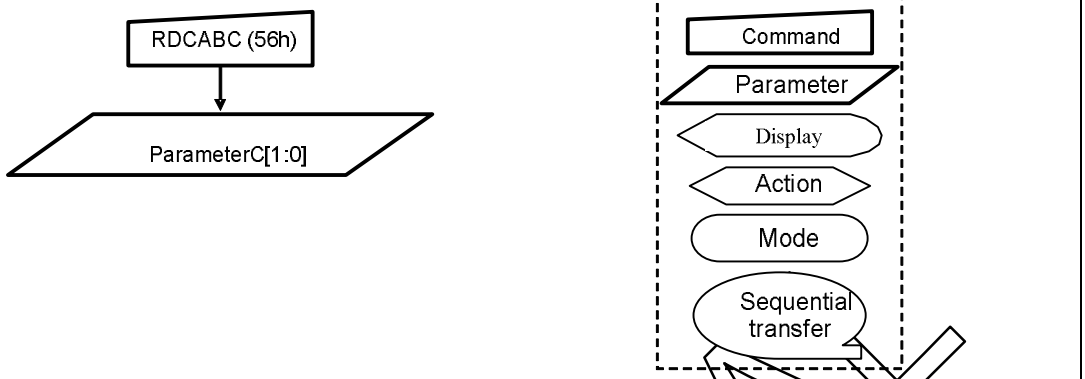
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

WRCABCMB (5Eh): Write CABC Minimum Brightness

5EH	WRCABCMB												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	↑	x	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00
Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Restriction	-												

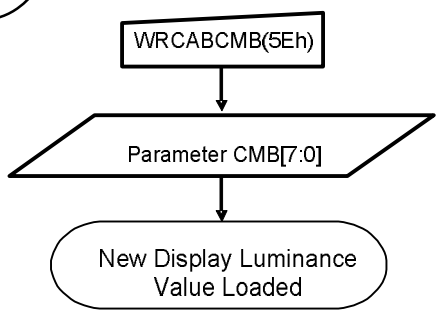
Register Availability

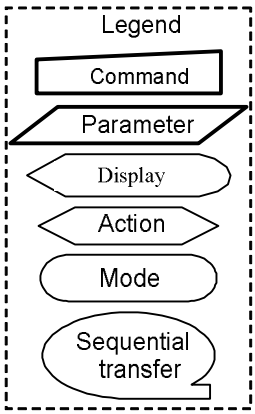
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart





RDCABCMB (5Fh): Read CABC Minimum Brightness

5FH	RDCABCMB												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	1	1	1	1	1	5F
1st parameter	1	1	↑	x	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00
Description	This command return the minimum brightness value of CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. CMB[7:0] is minimum brightness forCABC specified with “WRCABCMB Write CABC minimum brightness (5Eh)” command.												
Restriction	-												

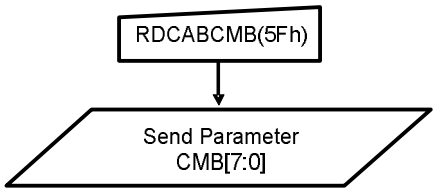
Register Availability

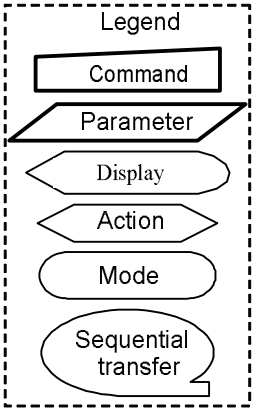
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart





RDFCS (AAh) : Read First Checksum

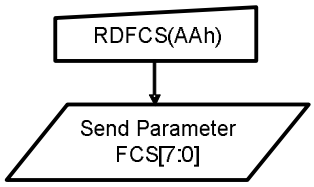
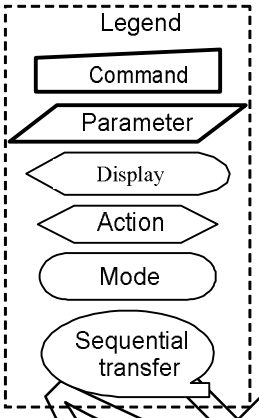
AAH	RDFCS (Read First Checksum)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	1	0	1	0	AA
1st parameter	1	↑	1	x	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	 

RDCFCS (AFh) : Read Continue Checksum

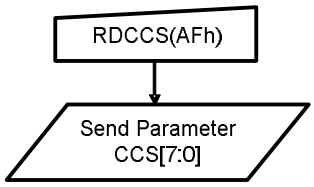
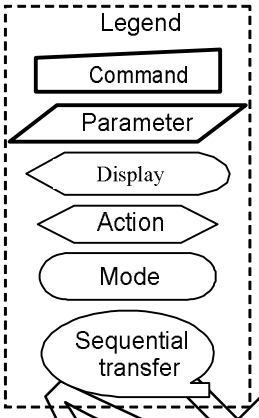
AFH	RDCFCS (Read Continue Checksum)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	1	1	1	1	AF
1st parameter	1	↑	1	x	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	 

RDID1 (DAh) : Read ID1

DAH	RDID1												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
Description	This read byte identifies the TFT LCD module's manufacture ID.												
Restriction	-												

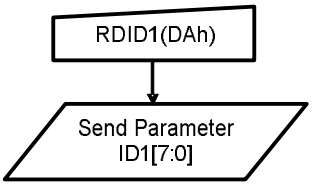
Register Availability

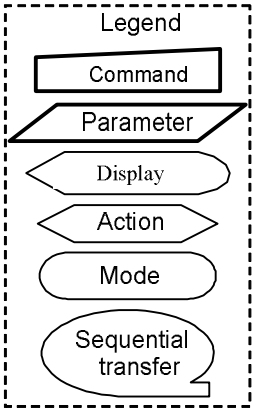
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart





RDID2(DBh) : Read ID2

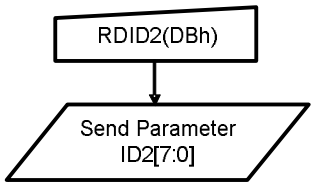
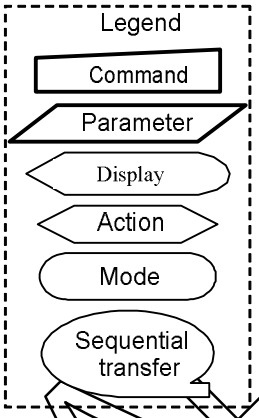
DBH	RDID2												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	0	1	1	DB
1st parameter	1	↑	1	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00
Description	This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 80h to FFh												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	80h
SW Reset	MTP Value	80h
HW Reset	MTP Value	80h

Flow Chart	 

RDID3(DCh) : Read ID3

DCH	RDID3												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	This parameter read byte identifies the TFT LCD module/driver.												
Restriction	-												

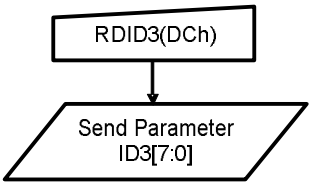
Register Availability

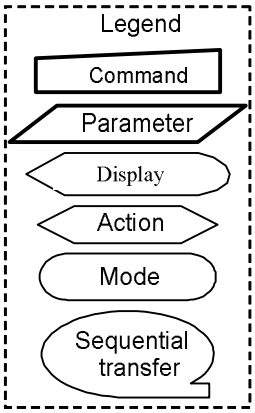
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

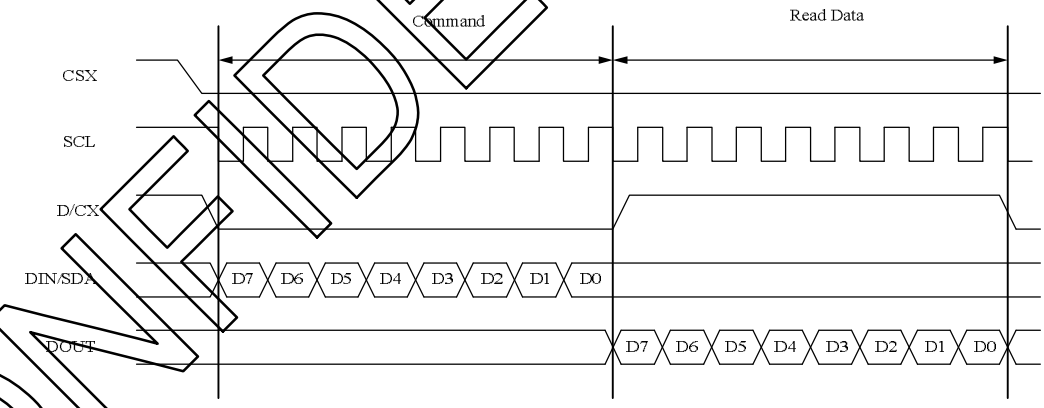
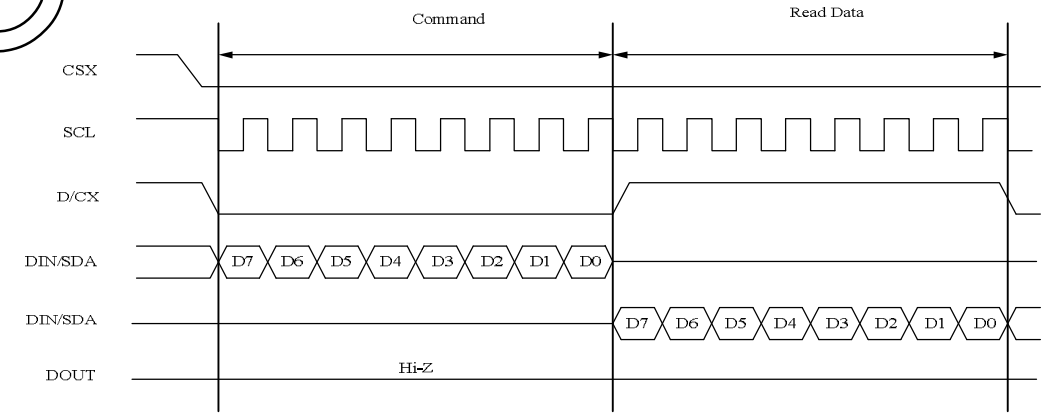
Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h

Flow Chart

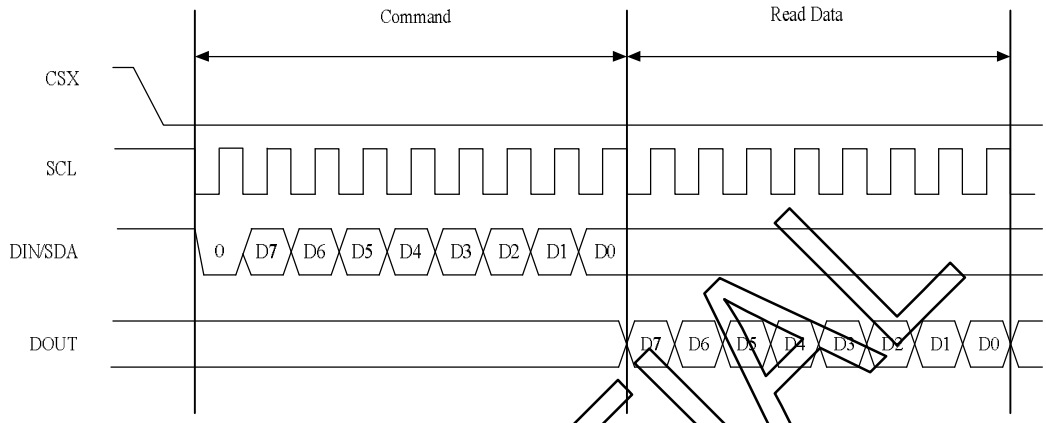




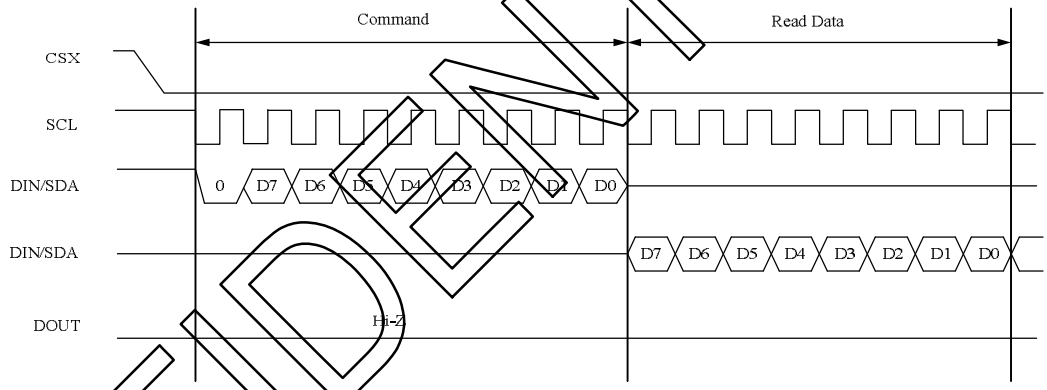
IFMODE (B0h): Interface Mode Control

B0H	IFMODE												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	1	x	SDA_EN	x	x	x	VSPL	HSPL	DPL	EPL	xx
Description	EPL: DE polarity (“0”= High enable for RGB interface, “1”=Low enable for RGB interface) DPL: PCLK polarity set (“0”=data fetched at the rising time, “1”=data fetched at the falling time) HSPL: HSYNC polarity (“0”=Low level sync clock, “1”=High level sync clock) VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock) SDA_EN: 3 or 4 wire serial interface selection. SDA_EN = “0”, DIN and DOUT pins are used for 3/4 wire serial interface. SDA_EN = “1”, DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used. SDA_EN=0  SDA_EN=1  												

SDA_EN=0



SDA_EN=1



Restriction	-

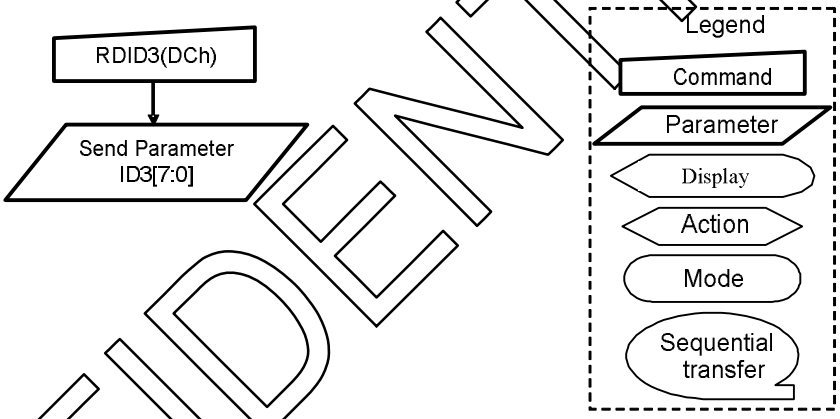
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
SW Reset	MTP Value	00h
HW Reset	MTP Value	00h

Flow Chart



FRMCTR1 (B1h) : Frame Rate Control (In Normal Mode/Full Colors)

B1H	FRMCTR2 (Frame Rate Control (in Idle Mode/8 Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	0	1	B1
1st Parameter	1	1	↑	x	FRS3	FRS2	FRS1	FRS0	0	0	DIVA1	DIVA0	xx
2nd parameter	1	1	↑	x	0	0	0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0	Xx

Description

FRS[3:0]: Sets the frame frequency of full color normal mode.

RTNB[3:0]	Frame rate(Hz)
0000	28
0001	30
0010	32
0011	34
0100	36
0101	39
0110	42
0111	46

RTNB[4:0]	Frame rate(Hz)
1000	50
1001	56
1010	62
1011	70
1100	81
1101	96
1110	117
1111	117

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Idle mode at CPU interface.

RTNB[4:0]	Clock per Line
00000	Setting prohibited
00001	Setting prohibited
00010	Setting prohibited
00011	Setting prohibited
00100	Setting prohibited
00101	Setting prohibited
00110	Setting prohibited
00111	Setting prohibited
01000	Setting prohibited
01001	Setting prohibited
01010	Setting prohibited
01011	Setting prohibited
01100	Setting prohibited
01101	Setting prohibited
01110	Setting prohibited
01111	Setting prohibited

RTNB[4:0]	Clock per Line
10000	16 clocks
10001	17 clocks
10010	18 clocks
10011	19 clocks
10100	20 clocks
10101	21 clocks
10110	22 clocks
10111	23 clocks
11000	24 clocks
11001	25 clocks
11010	26 clocks
11011	27 clocks
11100	28 clocks
11101	29 clocks
11110	30 clocks
11111	31 clocks

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIVA[1:0]	RTNA[4:0]
Power On Sequence	2’b00	5’b10001
HW Reset	2’b00	5’b10001

FRMCTR2 (B2h) : Frame Rate Control (In Idle Mode/8 Colors)

B2H	FRMCTR2 (Frame Rate Control (in Idle Mode/8 Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	1	0	B2
1st Parameter	1	1	↑	x	0	0	0	0	0	0	DIVB1	DIVB0	Xx
2nd parameter	1	1	↑	x	0	0	0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0	Xx

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface.

DIVB [1:0] : division ratio for internal clocks when Idle mode

DIVB[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNB [4:0] : RTNB[4:0] is used to set 1H (line) period of Idle mode at CPU interface.

RTNB[4:0]	Clock per Line	RTNB[4:0]	Clock per Line
00000	Setting prohibited	10000	16 clocks
00001	Setting prohibited	10001	17 clocks
00010	Setting prohibited	10010	18 clocks
00011	Setting prohibited	10011	19 clocks
00100	Setting prohibited	10100	20 clocks
00101	Setting prohibited	10101	21 clocks
00110	Setting prohibited	10110	22 clocks
00111	Setting prohibited	10111	23 clocks
01000	Setting prohibited	11000	24 clocks
01001	Setting prohibited	11001	25 clocks
01010	Setting prohibited	11010	26 clocks
01011	Setting prohibited	11011	27 clocks
01100	Setting prohibited	11100	28 clocks
01101	Setting prohibited	11101	29 clocks
01110	Setting prohibited	11110	30 clocks
01111	Setting prohibited	11111	31 clocks

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<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Power On Sequence</td><td>2’b00</td><td>5’b10001</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’b10001</td></tr>
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FRMCTR3 (B3h) : Frame Rate Control (In Partial Mode/Full Colors)

B3H	FRMCTR3 (Frame Rate Control (in Partial Mode/Full Colors))												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	0	1	1	B3
1st Parameter	1	1	↑	x	0	0	0	0	0	0	DIVC1	DIVC0	xx
2nd parameter	1	1	↑	x	0	0	0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0	xx

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface.

DIVC [1:0] : division ratio for internal clocks when Partial mode.

DIVC[1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNC [4:0] : RTNC[4:0] is used to set 1H (line) period of Partial mode at CPU interface.

RTNB[4:0]	Clock per Line	RTNB[4:0]	Clock per Line
00000	Setting prohibited	10000	16 clocks
00001	Setting prohibited	10001	17 clocks
00010	Setting prohibited	10010	18 clocks
00011	Setting prohibited	10011	19 clocks
00100	Setting prohibited	10100	20 clocks
00101	Setting prohibited	10101	21 clocks
00110	Setting prohibited	10110	22 clocks
00111	Setting prohibited	10111	23 clocks
01000	Setting prohibited	11000	24 clocks
01001	Setting prohibited	11001	25 clocks
01010	Setting prohibited	11010	26 clocks
01011	Setting prohibited	11011	27 clocks
01100	Setting prohibited	11100	28 clocks
01101	Setting prohibited	11101	29 clocks
01110	Setting prohibited	11110	30 clocks
01111	Setting prohibited	11111	31 clocks

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<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Power On Sequence</td><td>2’b00</td><td>5’b10001</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’b10001</td></tr>
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INVTR (B4h) : Display Invrsion Control

B4H	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	0	0	B4
Parameter	1	1	↑	x	0	0	0	ZINV	0	0	DINV1	DINV0	xx

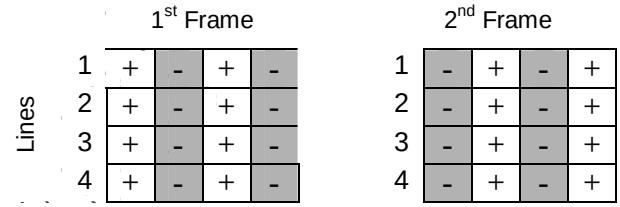
Description

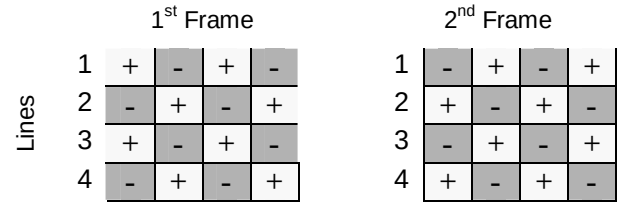
ZINV : Set Z-inversion mode.

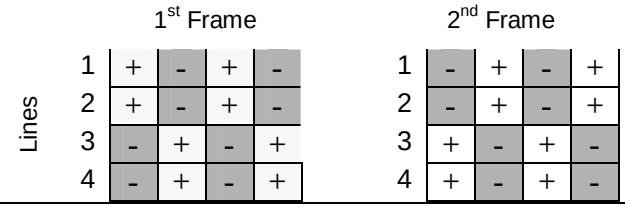
ZINV	Status
0	Disable Z-inversion
0	Enable Z-inversion

DINV[1:0] : Set the inversion mode.

DINV[1:0]	Dot inversion mode
2'b00	Column inversion
2'b01	1-dot inversion
2'b10	2-dot inversion
2'b11	Setting prohibited







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<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
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<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><th>ZINV</th><th>DINV[1:0]</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>2’b00</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>2’b00</td></tr>
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PRCTR (B5h) : Blocking Porch Control

B5H	PRCTR (Blocking Porch Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	0	1	B5
1st Parameter	1	1	↑	x	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	xx
2nd parameter	1	1	↑	x	VBP7	VFB6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	Xx
3rd parameter	1	1	↑	x	0	0	0	HFP4	HFP3	HFP2	HFP1	HFP0	Xx
4nd parameter	1	1	↑	x	HBP7	HFB6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	Xx

Description

VFP [7:0] / VBP [7:0]: The VFP [7:0] and VBP [7:0] bits specify the line number of vertical front and back porch period respectively.

VFP[7:0]	Number of lines of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

VBP[7:0]	Number of lines of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

HFP [4:0] / HBP [7:0]: The HFP [4:0] and HBP [7:0] bits specify the dotclk number of horizontal back porch period.

HFP[4:0]	Number of dotclk of front porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
: :	: :
11100	28
11101	29
11110	30
11111	31

HBP[7:0]	Number of dotclk of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
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<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP[7:0]</th><th>VBP[7:0]</th><th>HFP[7:0]</th><th>HBP[7:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’b00000010</td><td>8’b00000010</td><td>8’b00001010</td><td>8’b00000100</td></tr>
<tr><td>HW Reset</td><td>8’b00000010</td><td>8’b00000010</td><td>8’b00001010</td><td>8’b00000100</td></tr>
</table>
</td></tr>
</table>

DISCTRL (B6h): Display Function Control

B6H	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	1	0	B6
1st parameter	1	1	↑	x	BYPASS	RCM	RM	DM	PTG[1]	PTG[0]	PT[1]	PT[0]	x
2nd parameter	1	1	↑	x	0	GS	SS	SM	ISC[3]	ISC[2]	ISC[1]	ISC[0]	xx
3rd parameter	1	1	↑	x	0	0	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	xx

Description

DM: Select the display operation mode.

DM	Interface Mode
0	Internal system clock
1	RGB Interface

RM: Select the interface to access the GRAM.

RM	Interface for GRAM access
0	via System interface
1	via RGB interface

RCM: RGB interface selection.

RCM	RGB transfer mode
0	DE Mode
1	SYNC Mode

BYPASS: Select the display data path, when RGB interface is used.

BYPASS	Display data path
0	Memory
1	Direct to shift register

PTG[1:0]: Sets the scan mode in non-display area.

PTG[1]	PTG[0]	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with PT[2:0]
0	1	Setting prohibited	--
1	0	Interval	Set with PT[2:0]
1	1	Setting prohibited	--

PT[1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT[1]	PT[0]	Source outputs in non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: select the shift direction of outputs from the source driver.

SS	Source output scan direction
0	S1 **à** S960
1	S960 **à** S1

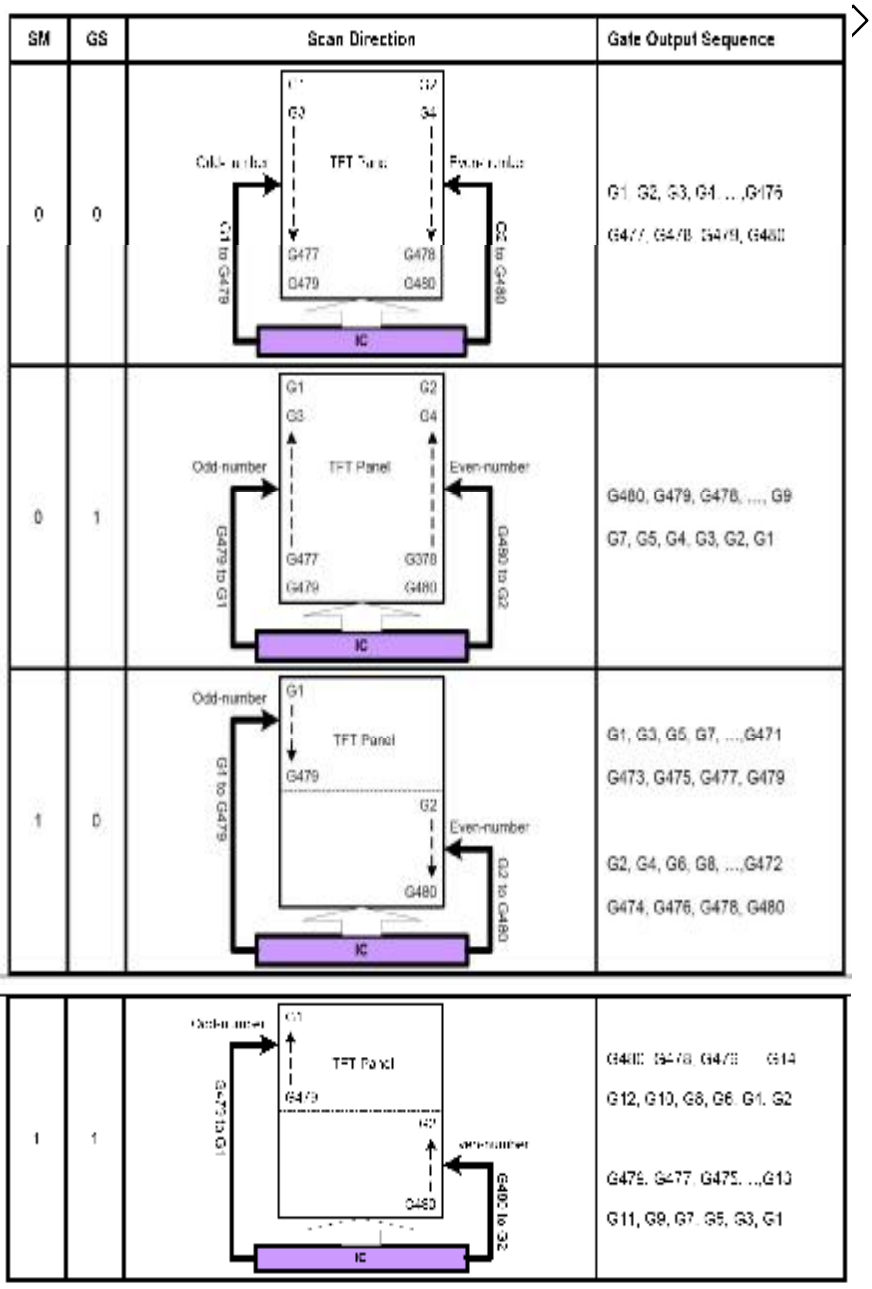
ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(fFRAME)=60Hz
4’h0	Setting inhibited	—
4’h1	3 frames	50ms
4’h2	5 frames	84ms
4’h3	7 frames	117ms
4’h4	9 frames	150ms
4’h5	11 frames	184ms
4’h6	13 frames	217ms
4’h7	15 frames	251ms
4’h8	17 frames	284ms
4’h9	19 frames	317ms
4’hA	21 frames	351ms
4’hB	23 frames	384ms
4’hC	25 frames	418ms
4’hD	27 frames	451ms
4’hE	29 frames	484ms
4’hF	31 frames	518ms

GS: select the direction of scan by the gate driver.

GS	Source output scan direction
0	G1 **à** G480
1	G480 **à** G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.



NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL5:0]+1) lines
Others	Setting inhibited

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value						
	PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]
Power On Sequence	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011
HW Reset	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011

Status	Default Value		
	RM	DM	BYPASS
Power On Sequence	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

ETMOD (B7h) : Entry Mode Set

B7H	Interface Mode Control												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	1	0	1	1	1	B7
Parameter	1	1	↑	x	EPF[1]	EPF[0]	0	0	DSTB	GON	DTE	GAS	xx

Description

DSTB: enter the Deep Standby Mode when DSTB = "1". In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Staandby Mode is exited.

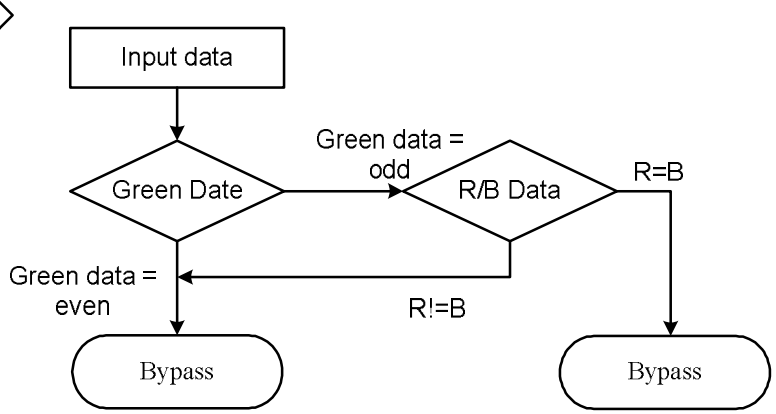
GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1~G320 as follows

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

EPF[1:0]: set the data format when 16bbp(R,G,B) to 18bbp(R,G,B) is stored in the internal GRAM



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	EPF[1:0]	DSTB	GON	DTE	GAS
Power On Sequence	2'b00	1'b0	1'b1	1'b1	1'b0
HW Reset	2'b00	1'b0	1'b1	1'b1	1'b0

PWCTRL1 (C0h): Power Control 1

C0H	PWCTRL1 (Power Control 1)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1st parameter	1	1	↑	x	0	0	0	VRH1[4]	VRH1[3]	VRH1[2]	VRH1[1]	VRH1[0]	xx
2nd parameter	1	1	↑	x	0	0	0	VRH2[4]	VRH2[3]	VRH2[2]	VRH2[1]	VRH2[0]	xx

Description

VRH1[4:0]: Sets the VREG1OUT voltage for positive gamma

VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT
5'h00	Halt	5'h10	1.25 x 3.65 = 4.5625V
5'h01	1.25 x 2.90=3.6250V	5'h11	1.25 x 3.70 = 4.6250V
5'h02	1.25 x 2.95 = 3.6875V	5'h12	1.25 x 3.75 = 4.6875V
5'h03	1.25 x 3.00 = 3.7500V	5'h13	1.25 x 3.80 = 4.7500V
5'h04	1.25 x 3.05 = 3.8125V	5'h14	1.25 x 3.85 = 4.8125V
5'h05	1.25 x 3.10 = 3.8750V	5'h15	1.25 x 3.90 = 4.8750V
5'h06	1.25 x 3.15 = 3.9375V	5'h16	1.25 x 3.90 = 4.8750V
5'h07	1.25 x 3.20 = 4.0000V	5'h17	1.25 x 4.00 = 5.0000V
5'h08	1.25 x 3.25 = 4.0625V	5'h18	1.25 x 4.05 = 5.0625V
5'h09	1.25 x 3.30 = 4.1250V	5'h19	1.25 x 4.10 = 5.1250V
5'h0A	1.25 x 3.35 = 4.1875V	5'h1A	1.25 x 4.15 = 5.1875V
5'h0B	1.25 x 3.40 = 4.2500V	5'h1B	1.25 x 4.20 = 5.2500V
5'h0C	1.25 x 3.45 = 4.3125V	5'h1C	1.25 x 4.25 = 5.3125V
5'h0D	1.25 x 3.50 = 4.3750V	5'h1D	1.25 x 4.30 = 5.3750V
5'h0E	1.25 x 3.55 = 4.4375V	5'h1E	1.25 x 4.35 = 5.4375V
5'h0F	1.25 x 3.60 = 4.5000V	5'h1F	1.25 x 4.40 = 5.5000V

VRH2[4:0]: Sets the VREG2OUT voltage for positive gamma

VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT
5'h00	Halt	5'h10	-1.25 x -3.65 = -4.5625V
5'h01	-1.25 x 2.90=-3.6250V	5'h11	-1.25 x -3.70 = -4.6250V
5'h02	-1.25 x 2.95 = -3.6875V	5'h12	-1.25 x -3.75 = -4.6875V
5'h03	-1.25 x 3.00 = -3.7500V	5'h13	-1.25 x -3.80 = -4.7500V
5'h04	-1.25 x 3.05 = -3.8125V	5'h14	-1.25 x -3.85 = -4.8125V
5'h05	-1.25 x 3.10 = -3.8750V	5'h15	-1.25 x -3.90 = -4.8750V
5'h06	-1.25 x 3.15 = -3.9375V	5'h16	-1.25 x -3.90 = -4.8750V
5'h07	-1.25 x 3.20 = -4.0000V	5'h17	-1.25 x -4.00 = -5.0000V
5'h08	-1.25 x 3.25 = -4.0625V	5'h18	-1.25 x -4.05 = -5.0625V
5'h09	-1.25 x 3.30 = -4.1250V	5'h19	-1.25 x -4.10 = -5.1250V
5'h0A	-1.25 x 3.35 = -4.1875V	5'h1A	-1.25 x -4.15 = -5.1875V
5'h0B	-1.25 x 3.40 = -4.2500V	5'h1B	-1.25 x -4.20 = -5.2500V
5'h0C	-1.25 x 3.45 = -4.3125V	5'h1C	-1.25 x -4.25 = -5.3125V
5'h0D	-1.25 x 3.50 = -4.3750V	5'h1D	-1.25 x -4.30 = -5.3750V
5'h0E	-1.25 x 3.55 = -4.4375V	5'h1E	-1.25 x -4.35 = -5.4375V
5'h0F	-1.25 x 3.60 = -4.5000V	5'h1F	-1.25 x -4.40 = -5.5000V

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VRH1[4:0]=5'h0E, VRH2[4:0]=5'h0E
SW Reset	No change
HW Reset	VRH1[4:0]=5'h0E, VRH2[4:0]=5'h0E

PWCTRL2 (C1h): Power Control 2

C1H	PWCTRL2 (Power Control 2)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	x	0	0	0	0	0	BT[2]	BT[1]	BT[0]	Xx
2nd parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	Xx

Description

VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1.

VC[2:0]	Vci1 voltage
3'h0	1.0 x Vci
3'h1	3.1 V
3'h2	3.0 V
3'h3	2.9 V
3'h4	2.8 V
3'h5	2.7 V
3'h6	2.6 V
3'h7	2.5 V

BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci.

BT[2:0]	DDVDH	DDVDL	VCL	VGH	VGL
3'h0	Vci1x 2	-5V	- Vci	Vci x 6	- Vci x 5
3'h1					- Vci x 4
3'h2					- Vci x 3
3'h3				Vci x 5	- Vci x 5
3'h4					- Vci x 4
3'h5					- Vci x 3
3'h6				Vci x 4	- Vci x 4
3'h7					- Vci x 3

<table>
<tr><td></td><td>Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
Note 2: Set following voltages within the respective ranges:
DDVDH = 6.0V (max)
VGH = 18.0V (max)
VGL= -12.5V (max)
VCL= -3.6 (max).</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
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<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>VC[2:0]=3’h0, BT[2:0]=3’h0</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>VC[2:0]=3’h0, BT[2:0]=3’h0</td></tr>
</table></td></tr>
</table>

PWCTRL3 (C2h): Power Control 3 for Normal Mode

C2H	PWCTRL3 (Power Control 3 for Normal Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	x	DCA1[3]	DCA1[2]	DCA1[1]	DCA1[0]	DCA0[3]	DCA0[2]	DCA0[1]	DCA0[0]	xx

Description

DCA0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Normal mode.

DCA0[3]	DCA0[2:0]	Step-up cycle for Step-up circuit 1/2
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCA1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Normal mode.

DCA1[3]	DCA1[2:0]	Step-up cycle for Step-up circuit 3
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

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<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DCA0[3:0]=4’b0011, DCA1[2:0]=4’b0100</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>DCA0[3:0]=4’b0011, DCA1[2:0]=4’b0100</td></tr>
</table>
</td></tr>
</table>

PWCTRL4 (C3h): Power Control 4 for Idle Mode

C3H	PWCTRL4 (Power Control 4 for Idle Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	x	DCB1[3]	DCB1[2]	DCB1[1]	DCB1[0]	DCB0[3]	DCB0[2]	DCB0[1]	DCB0[0]	xx

Description

DCB0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Idle mode.

DCB0[3]	DCB0[2:0]	Step-up cycle for Step-up circuit 1/2
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCB1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Idle mode.

DCB1[3]	DCB1[2:0]	Step-up cycle for Step-up circuit 3
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

<table>
<tr><td>Register availability</td><td>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DCB0[3:0]=4’b0011, DCB1[2:0]=4’b0100</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>DCB0[3:0]=4’b0011, DCB1[2:0]=4’b0100</td></tr>
</table>
</td></tr>
</table>

PWCTRL5 (C4h): Power Control 5 for Partial Mode

C4H	PWCTRL5 (Power Control 5 for Partial Mode)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	x	DCC1[3]	DCC1[2]	DCC1[1]	DCC1[0]	DCC0[3]	DCC0[2]	DCC0[1]	DCC0[0]	Xx

Description

DCC0[3:0]: select the operating frequency of the step-up circuit 1/2 (DDVDH, VCL, and DDVDL pump) for Partial mode.

DCC0[3]	DCC0[2:0]	Step-up cycle for Step-up circuit 1/2
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	1H

Note: H=1/60/480=34.7us =1/28.8kHz

DCC1[3:0]: select the operating frequency of the step-up circuit 3 (VGH, and VGL pump)for Partial mode.

DCC1[3]	DCC1[2:0]	Step-up cycle for Step-up circuit 3
1’b1	3’b000	1/8 H
1’b1	3’b001	1/4 H
1’b1	3’b010	1/2 H
1’b1	3’b011	1 H
1’b1	3’b100	2 H
1’b1	3’b101	4 H
1’b1	3’b110	8 H
1’b1	3’b111	16 H
1’b0	x	2H

Note: H=1/60/480=34.7us =1/28.8kHz

<table>
<tr><td>Register availability</td><td>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DCC0[3:0]=4’b0011, DCC1[2:0]=4’b0100</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>DCC0[3:0]=4’b0011, DCC1[2:0]=4’b0100</td></tr>
</table>
</td></tr>
</table>

VCOM Control (C5h)

C5H	VCOM Control												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	C5
1st parameter	1	↑	1	x	0	0	0	0	0	0	0	NVM	xx
2nd parameter	1	1	↑	x	VCM_REG[7]	VCM_REG[6]	VCM_REG[5]	VCM_REG[4]	VCM_REG[3]	VCM_REG[2]	VCM_REG[1]	VCM_REG[0]	xx
3rd parameter	1	1	↑	x	VCM_REG_EN	0	0	0	0	0	0	0	xx
4rd parameter	1	↑	1	x	VCM_OUT[7]	VCM_OUT[6]	VCM_OUT[5]	VCM_OUT[4]	VCM_OUT[3]	VCM_OUT[2]	VCM_OUT[1]	VCM_OUT[0]	xx

Description

NVM : When the NV memory is programmed, the NVM will be set as '1' automatically.

0 : NV memory is not programmed
1 : NV memory is programmed

VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM
8'h00	-2	8'h20	-1.5
8'h01	-1.98438	8'h21	-1.48438
8'h02	-1.96875	8'h22	-1.46875
8'h03	-1.95313	8'h23	-1.45313
8'h04	-1.9375	8'h24	-1.4375
8'h05	-1.92188	8'h25	-1.42188
8'h06	-1.90625	8'h26	-1.40625
8'h07	-1.89063	8'h27	-1.39063
8'h08	-1.875	8'h28	-1.375
8'h09	-1.85938	8'h29	-1.35938
8'h0A	-1.84375	8'h2A	-1.34375
8'h0B	-1.82813	8'h2B	-1.32813
8'h0C	-1.8125	8'h2C	-1.3125
8'h0D	-1.79688	8'h2D	-1.29688
8'h0E	-1.78125	8'h2E	-1.28125
8'h0F	-1.76563	8'h2F	-1.26563
8'h10	-1.75	8'h30	-1.25
8'h11	-1.73438	8'h31	-1.23438
8'h12	-1.71875	8'h32	-1.21875
8'h13	-1.70313	8'h33	-1.20313
8'h14	-1.6875	8'h34	-1.1875
8'h15	-1.67188	8'h35	-1.17188
8'h16	-1.65625	8'h36	-1.15625
8'h17	-1.64063	8'h37	-1.14063
8'h18	-1.625	8'h38	-1.125
8'h19	-1.60938	8'h39	-1.10938
8'h1A	-1.59375	8'h3A	-1.09375
8'h1B	-1.57813	8'h3B	-1.07813
8'h1C	-1.5625	8'h3C	-1.0625
8'h1D	-1.54688	8'h3D	-1.04688
8'h1E	-1.53125	8'h3E	-1.03125
8'h1F	-1.51563	8'h3F	-1.01563

VCM_REG[7:0]	VCOM	VCM_REG[7:0]	VCOM
8'h40	-1	8'h62	-0.46875
8'h41	-0.98438	8'h63	-0.45313
8'h42	-0.96875	8'h64	-0.4375
8'h43	-0.95313	8'h65	-0.42188
8'h44	-0.9375	8'h66	-0.40625
8'h45	-0.92188	8'h67	-0.39063
8'h46	-0.90625	8'h68	-0.375
8'h47	-0.89063	8'h69	-0.35938
8'h48	-0.875	8'h6A	-0.34375
8'h49	-0.85938	8'h6B	-0.32813
8'h4A	-0.84375	8'h6C	-0.3125
8'h4B	-0.82813	8'h6D	-0.29688
8'h4C	-0.8125	8'h6E	-0.28125
8'h4D	-0.79688	8'h6F	-0.26563
8'h4E	-0.78125	8'h70	-0.25
8'h4F	-0.76563	8'h71	-0.23438
8'h50	-0.75	8'h72	-0.21875
8'h51	-0.73438	8'h73	-0.20313
8'h52	-0.71875	8'h74	-0.1875
8'h53	-0.70313	8'h75	-0.17188
8'h54	-0.6875	8'h76	-0.15625
8'h55	-0.67188	8'h77	-0.14063
8'h56	-0.65625	8'h78	-0.125
8'h57	-0.64063	8'h79	-0.10938
8'h58	-0.625	8'h7A	-0.09375
8'h59	-0.60938	8'h7B	-0.07813
8'h5A	-0.59375	8'h7C	-0.0625
8'h5B	-0.57813	8'h7D	-0.04688
8'h5C	-0.5625	8'h7E	-0.03125
8'h5D	-0.54688	8'h7F	-0.01563
8'h5E	-0.53125	8'h80	0
8'h5F	-0.51563	8'h81~8'hFE	Inbibit
8'h60	-0.5	8'hFF	Halt
8'h61	-0.48438		

VCM_REG_EN: Select the Vcom value from VCM_REG [7:0] or NV memory.

0: VCOM value from NV memory.
1: VCOM value from VCM_REG [7:0].

VCM_OUT [7:0]: NV memory programmed value.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VCM_REG[7:0]=8'hC0, VCM_REG_EN=1'b0
SW Reset	No change
HW Reset	VCM_REG[7:0]=8'hC0, VCM_REG_EN=1'b0

NVMWR (D0h): NV Memory Write

D0H	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0
1st parameter	1	1	↑	x	VM_D[7]	VM_D[6]	VM_D[5]	VM_D[4]	VM_D[3]	VM_D[2]	VM_D[1]	VM_D[0]	xx
Description	This command is used to program the NV memory data. VM_D[7:0]: Use to write the data (including VCM and ID code) into the NV memory data.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VM_D[7:0]=8'h00
SW Reset	No change
HW Reset	VM_D[7:0]=8'h00

NVMPKEY (D1h): NV Memory Protection

D1H	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1st parameter	1	1	↑	x	KEY[23]	KEY[22]	KEY[21]	KEY[20]	KEY[19]	KEY[18]	KEY[17]	KEY[16]	55
2nd parameter	1	1	↑	x	KEY[15]	KEY[14]	KEY[13]	KEY[12]	KEY[11]	KEY[10]	KEY[9]	KEY[8]	AA
3rd parameter	1	1	↑	x	KEY[7]	KEY[6]	KEY[5]	KEY[4]	KEY[3]	KEY[2]	KEY[1]	KEY[0]	66
Description	KEY[23:0]: NV memory programming protection key. When writing OTP data, this register must be set as 0x55AA66 to enable OTP programming. If register is not written with 0x55AA66, NV memory programming will fail.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Availability
Power On Sequence	KEY[23:0]=24'h55AA66
SW Reset	No change
HW Reset	KEY[23:0]=24'h55AA66

RDNVM (D2h): NV Memory Status Read

D2H	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	1	0	D2
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	x	0	0	0	0	0	0	PGM_CNT1	PGM_CNT0	xx
3rd parameter	1	↑	1	x	NV_VCM[7]	NV_VCM[6]	NV_VCM[5]	NV_VCM[4]	NV_VCM[3]	NV_VCM[2]	NV_VCM[1]	NV_VCM[0]	xx
Description	PGM_CNT[1:0]: NV memory programmed record. The bit will increase "+1" automatically when writing the NV_VCM [7:0]. PGM_CNT[1:0] / Description 00 / NV Memory clean 01 / NV Memory programmed 1 10 / NV Memory programmed 2 These bits are read only. NV_VCM [7:0]: NV memory VCM data read value. These bits are read only.												
Restriction													
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes												

RDID2(D3h) : Read ID4

D3H	RDID4 (Read ID4)												
	DCX	RDX	WRX	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	xx	ID41[7]	ID41[6]	ID41[5]	ID41[4]	ID41[3]	ID41[2]	ID41[1]	ID41[0]	00
3rd parameter	1	↑	1	xx	ID42[7]	ID42[6]	ID42[5]	ID42[4]	ID42[3]	ID42[2]	ID42[1]	ID42[0]	94
4th parameter	1	↑	1	xx	ID43[7]	ID43[6]	ID43[5]	ID43[4]	ID43[3]	ID43[2]	ID43[1]	ID43[0]	86
Description	Read ID device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID4=24'h009486h
SW Reset	No change
HW Reset	ID4=24'h009486h

Gamma Setting (E0h)

E0H	Gamma Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	1	0	0	0	E0
1st parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	00
2nd parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	44
3rd parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	06
4th parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	44
5th parameter	1	1	↑	x	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	0A
6th parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	08
7th parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	17
8th parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	33
9th parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	77
10th parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	44
11th parameter	1	1	↑	x	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	08
12th parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0C
Description	KP5-0[2:0] : γ fine adjustment register for positive polarity RP1-0[2:0] : γ gradient adjustment register for positive polarity VRP0[4:0], VRP1[4:0] : γ amplitude adjustment register for positive polarity KN5-0[2:0] : γ fine adjustment register for negative polarity RN1-0[2:0] : γ gradient adjustment register for negative polarity VRN0[4:0], VRN1[4:0] : γ amplitude adjustment register for negative polarity												
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes												

Default		Status	Default Value
		Power On Sequence	As above
		SW Reset	No change
		HW Reset	As above

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM68140 is used out of the absolute maximum ratings, the RM68140 may be permanently damaged. To use the RM68140 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM68140 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	IOVCC	-0.3 ~ +5.0	V
Power supply voltage	VCI	-0.3 ~ +5.0	V
Supply voltage (Digital)	VDD	-0.3 ~ + 2.0	V
Supply voltage (MV)	DDVDH-AGND	-0.3 ~ + 6.6	V
	DDVDL-AGND	+0.3 ~ - 5.2	V
Supply voltage (HV)	VGH - VGL	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ IOVCC+ 0.3	V
Output voltage	VO	-0.3 ~ IOVCC+ 0.3	V
Differential input voltage	STB_CLKP/N	-0.3 ~ +1.8	V
	DATA_P/N		
Operating temperature	Topr	-40 ~ + 85	˚C
Storage temperature	Tstg	-55 ~ + 125	˚C

Notes:
If one of the above itemsis exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

9.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	> 2.5KV
Machine Mode	R = 0 ohm / C = 200 pF	> 250V

9.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

9.4 Light Seneitivity

The operation of the IC will not be materially altered by incident light.

9.5 DC Characteristics

9.5.1 Basic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VCI	Operation Voltage	2.5	2.8	3.6	V	Note 1
I/O pin Power Supply Voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	Note 1
Logic High level input voltage	VIH	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V	Note 2
Logic Low level input voltage	VIL	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3* IOVCC	V	Note 2
Logic High level Output voltage	VOH	Iout = -1 mA	0.8* IOVCC	-	IOVCC	V	Note 2
Logic Low level Output voltage	VOL	Iout = +1 mA	0.0	-	0.2* IOVCC	V	Note 2
Logic High level input current (Except MIPI/MDDI)	IIHD	Vin=0~IOVCC			1	uA	Note 2
Logic Low level input current (Except MIPI/MDDI)	IILD	Vin=0~ IOVCC	-1			uA	Note 2
Logic High level input current (MIPI/MDDI)	IIHD	Vin=0~VDDAM			1	uA	Note 2
Logic Low level input current (MIPI/MDDI)	IILD	Vin=0~VDDAM	-1			uA	Note 2
DDVDH booster voltage	DDVDH		4.5		6.0	V	
DDVDL booster voltage	DDVDL		-5.2		-4.5	V	
VCL booster voltage	VCL		-3.0		-2.0	V	
VGH booster voltage	VGH		10		17	V	
VGL booster voltage	VGL		-13.5		-7.5	V	
Voltage difference between VGH and VGL	VGHL	|VGH-VGL|			32	V	
VCOM Amplitude voltage	VCOM		-2.0		0.0	V	
Gamma reference voltage	Vreg1		3.625		5.0	V	Note 3
	NVreg1		-5.0		-3.625	V	Note 3
Output offset voltage	V_{OFSET}				TBD	mV	Note 3
Output deviation voltage	V_{DEV}	Sout≥4.0V, Sout≤1.0V			TBD	mV	Note 3
		1.0V<Sout<4.0V			TBD	mV	Note 3

Notes: 1. IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=DGND=0V.

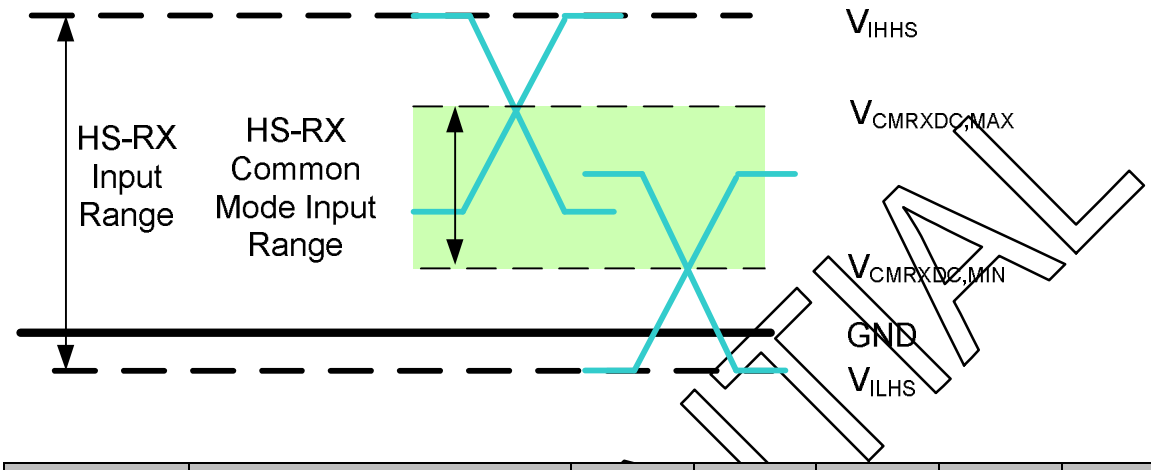
2. TA = -30 to 70 ℃.

3. Source channel loading =10KΩ+15pF/channel.

9.5.2 MIPI Characteristics

High-Speed Receiver Specification

DC Specifications



Parameter	Description	Min	Typ	Max	Units	Note
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
Z_{ID}	Differential input impedance	80	100	125	Ω	

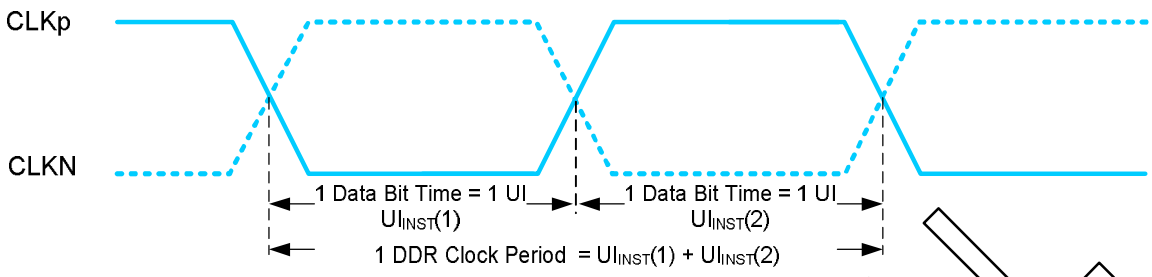
Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Forward high speed transmissions

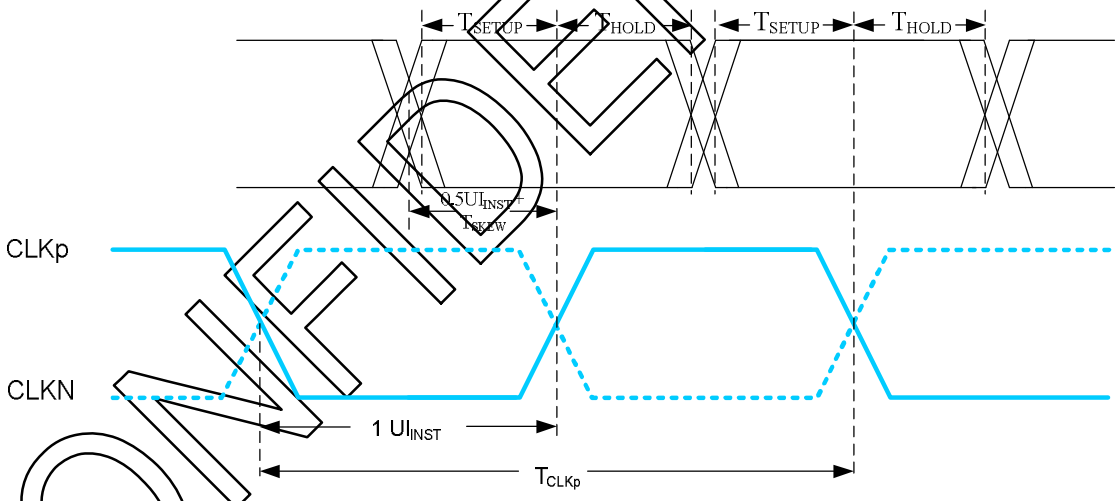
DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1,2

Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data to Clock Timing Definitions



Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}	1
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UI_{INST}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UI_{INST}	2

Notes:

1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

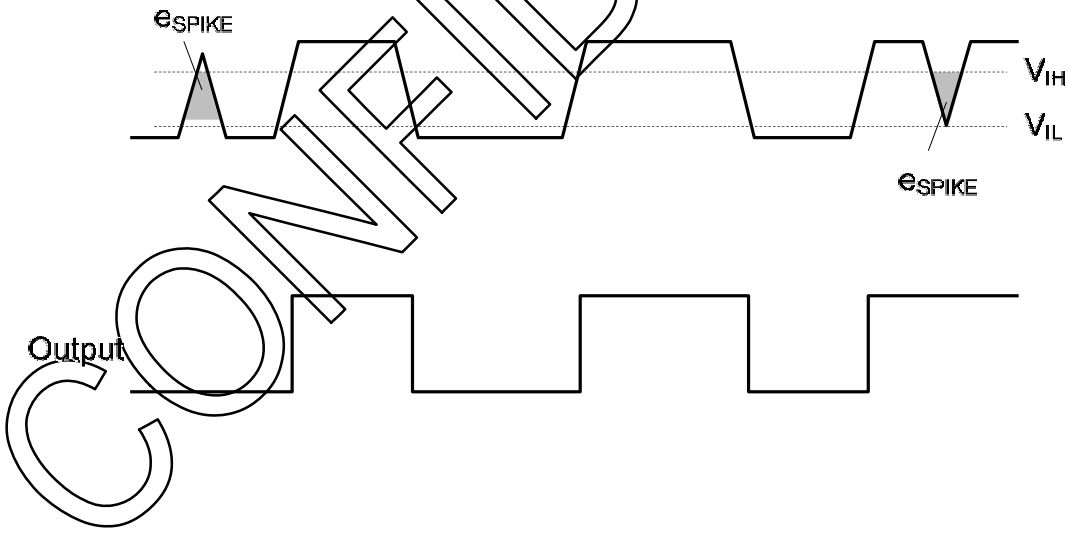
Low power transceiver specifications

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	V_{IHCD}	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	V_{ILCD}	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	$V_{IH-LPRX}$	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	$V_{IL-LPRX}$	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	$V_{IL-ULPS}$	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	$V_{OH-LPTX}$	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	$V_{OL-LPTX}$	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE[1.2.3]	Fig. 2	Input pulse rejection			300	V.ps

Notes:

- Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
- An impulse less than this will not change the receiver state.
- In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

Input Glitch Rejection of Low Power Receivers as follow



9.5.3 MDDI Characteristics

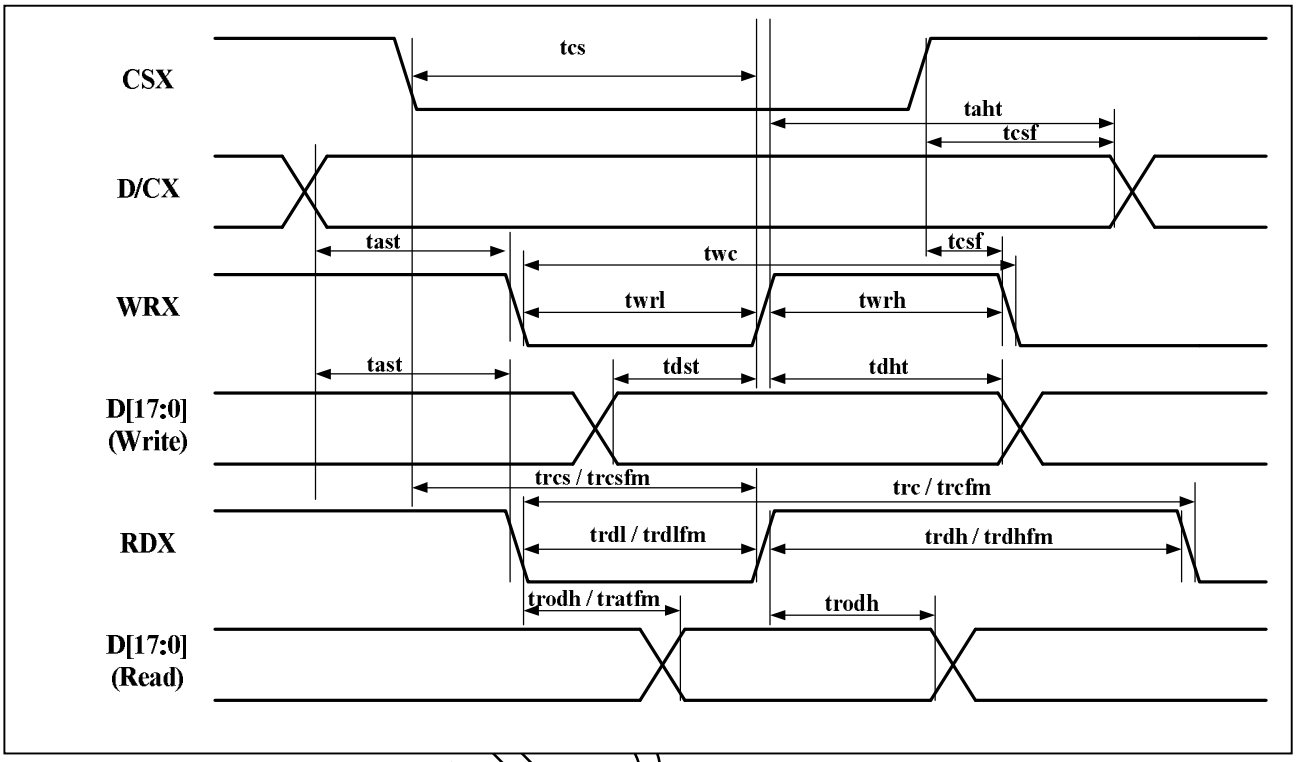
Characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Differential input “High” level voltage (hibernation wake-up)	$V_{IT+offset}$	VT=125mv (DATA_P/N)	-	100	125	mv
Differential input “Low” level voltage (hibernation wake-up)	$V_{IT-offset}$	VT=125mv (DATA_P/N)	75	100	-	mv
Differential input “High” level voltage	V_{IT+}	VT=0mv (STB_CLKP/N , DATA_P/N)	-	0	50	mv
Differential input “Low” level voltage	V_{IT-}	VT=0mv (STB_CLKP/N , DATA_P/N)	-50	0	-	mv

Note 1) IOVCC= 1.65~3.3V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta= -30 to 70 ºC (to +85 ºC no damage).

9.6 AC Characteristics

9.6.1 Parallel Interface Characteristics (80-Series MCU)



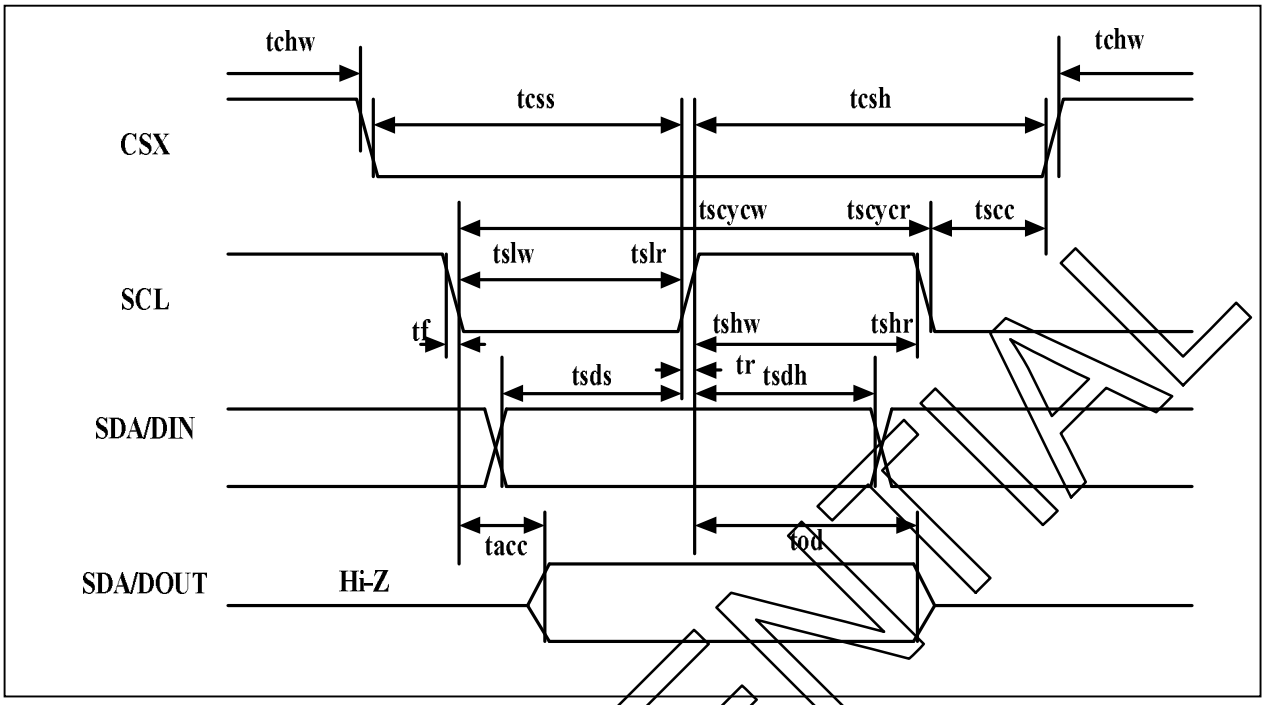
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t_{ast}	Address setup time	0	-	ns	
	t_{aht}	Address hold time (Write/Read)	0	-	ns	
CSX	t_{cs}	Chip Select setup time (Write)	15	-	ns	
	t_{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t_{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t_{csf}	Chip Select Wait time (Write/Read)	0	-	ns	
WRX	t_{wc}	Write cycle	50	-	ns	
	t_{wrh}	Write Control pulse H duration	15	-	ns	
	t_{wrl}	Write Control pulse L duration	15	-	ns	
RDX(FM)	t_{rcfm}	Read cycle	450	-	ns	Read from frame memory
	t_{rdhfm}	Read Control pulse H duration	90	-	ns	
	t_{rdlfm}	Read Control pulse L duration	355	-	ns	
RDX(ID)	t_{rc}	Read cycle	160	-	ns	Read from ID
	t_{rdh}	Read Control pulse H duration	90	-	ns	
	t_{rdl}	Read Control pulse L duration	45	-	ns	
DB[17:0]	t_{dst}	Write data setup time	10	-	ns	For maximum 30pF For minimum 8 pF
	t_{dht}	Write data hold time	10	-	ns	
	t_{rat}	Read access time	-	60	ns	
	t_{ratfm}	Read access time	-	340	ns	
	t_{rod}	Read output disable time	20	80		

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V

9.6.2 Serial Interface Characteristics

3 wire Serial Interface

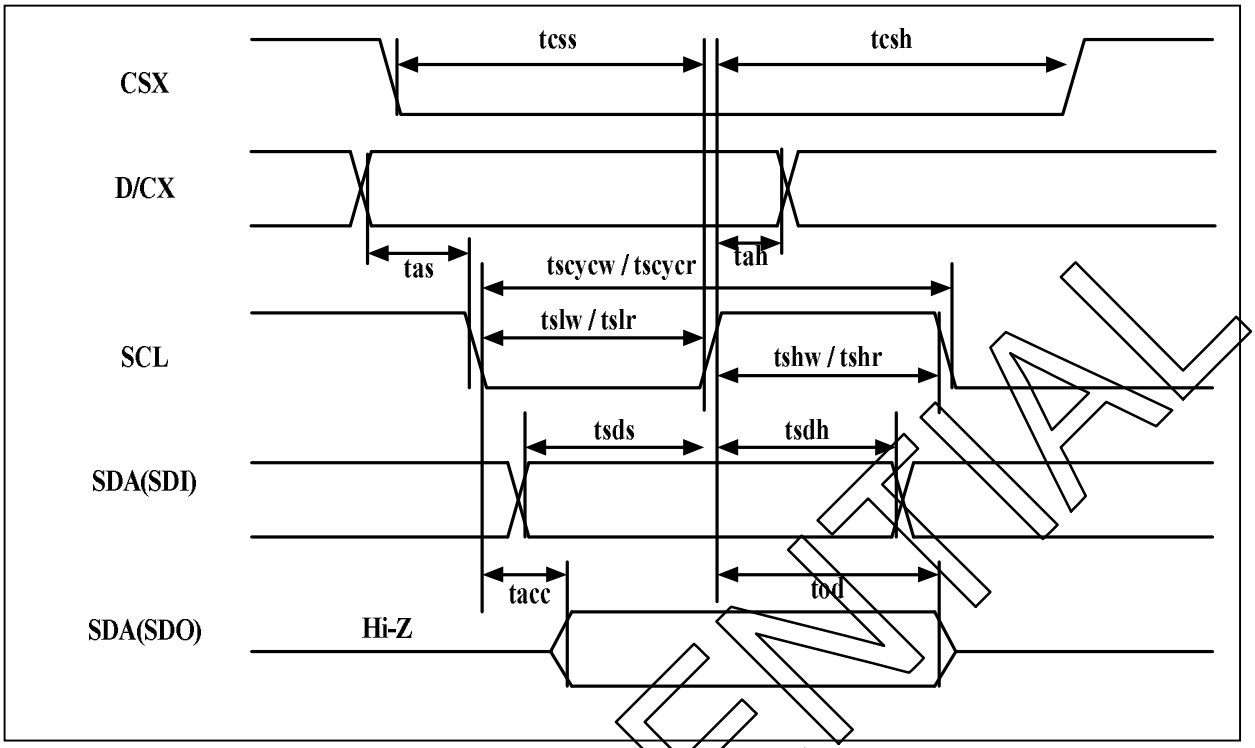


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{scycw}	Clock cycle (Write)	66	-	ns	-
	t_{shw}	Clock “H” pulse width (Write)	15	-	ns	
	t_{slw}	Clock “L” pulse width (Write)	15	-	ns	
	t_{scycr}	Clock cycle (Read)	150	-	ns	
	t_{shr}	Clock “H” pulse width (Read)	60	-	ns	
	t_{slr}	Clock “L” pulse width (Read)	60	-	ns	
CSX	t_{css}	Chip select setup time	60	-	ns	
	t_{csh}	Chip select hold time	65	-	ns	
SDA/SDI	t_{sds}	Data input setup time	10	-	ns	-
	t_{sdh}	Data input hold time	10	-	ns	
SDA/SDO	t_{acc}	Access time	10	60	ns	-
	t_{od}	Data output disable time	15	50	ns	

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V

4 wire Serial Interface

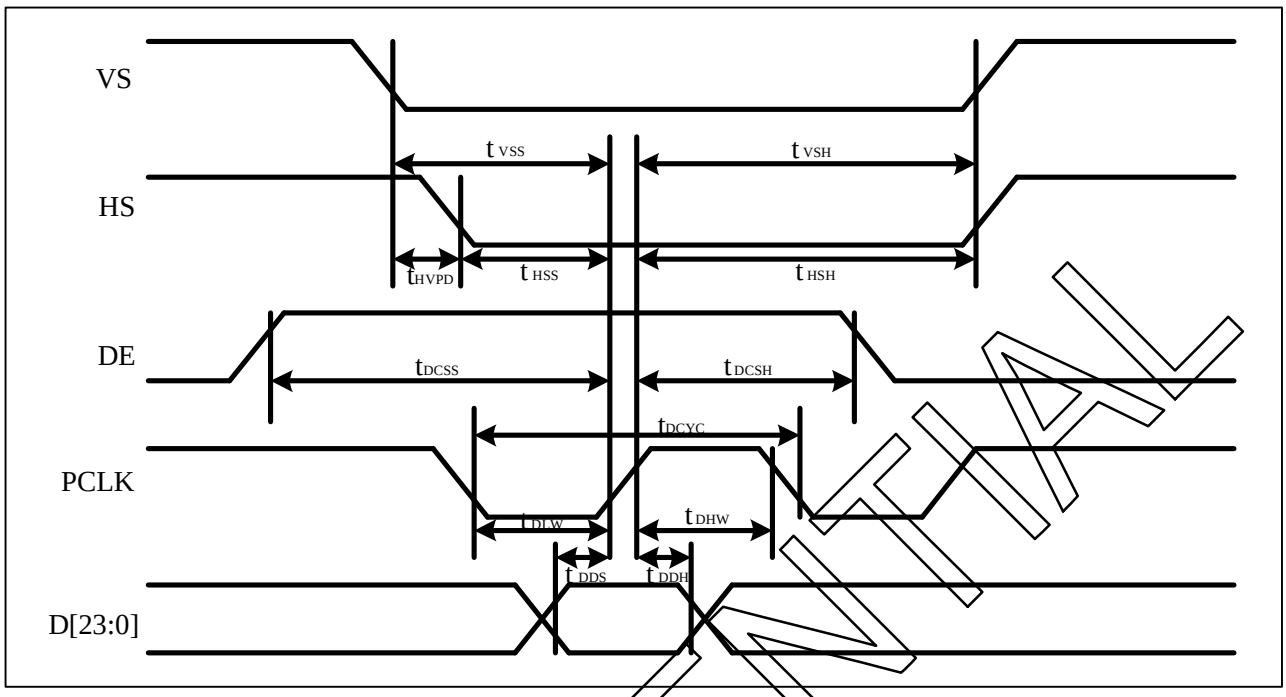


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{scycw}	Clock cycle (Write)	66	-	ns	-
	t_{shw}	Clock “H” pulse width (Write)	15	-	ns	
	t_{slw}	Clock “L” pulse width (Write)	15	-	ns	
	t_{scycr}	Clock cycle (Read)	150	-	ns	
	t_{shr}	Clock “H” pulse width (Read)	60	-	ns	
	t_{slr}	Clock “L” pulse width (Read)	60	-	ns	
CSX	t_{css}	Chip select setup time	15	-	ns	
	t_{csh}	Chip select hold time	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-	ns	
	t_{ah}	D/CX hold time	10	-	ns	
SDA/SDI	t_{sds}	Data input setup time	10	-	ns	-
	t_{sdh}	Data input hold time	10	-	ns	
SDA/SDO	t_{acc}	Access time	10	60	ns	For maximum 30pF For minimum 8pF
	t_{od}	Data output disable time	15	50	ns	

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V

9.6.3 16/18-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
VS	t_{VSS}	VS setup time	15	-	-	ns
	t_{VSH}	VS hold time	15	-	-	ns
HS	t_{HSS}	HS setup time	15	-	-	ns
	t_{HSH}	HS hold time	15	-	-	ns
PCLK	t_{DCYC}	PCLK cycle time	66	-	-	ns
	t_{DLW}	PCLK low pulse width	15	-	-	ns
	t_{DHW}	PCLK high pulse width	15	-	-	ns
DE	t_{DCSS}	DE setup time	15	-	-	ns
	t_{DCSH}	DE hold time	15	-	-	ns
D[17:0]	t_{DDS}	Data setup time	15	-	-	ns
	t_{DDH}	Data hold time	15	-	-	ns

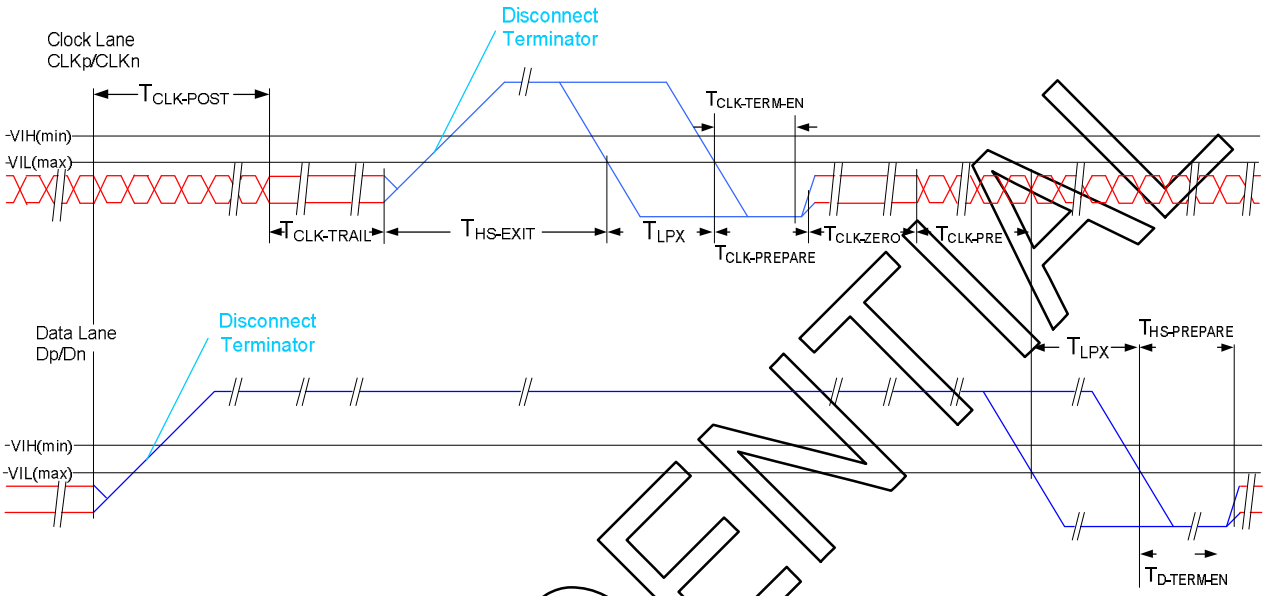
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V

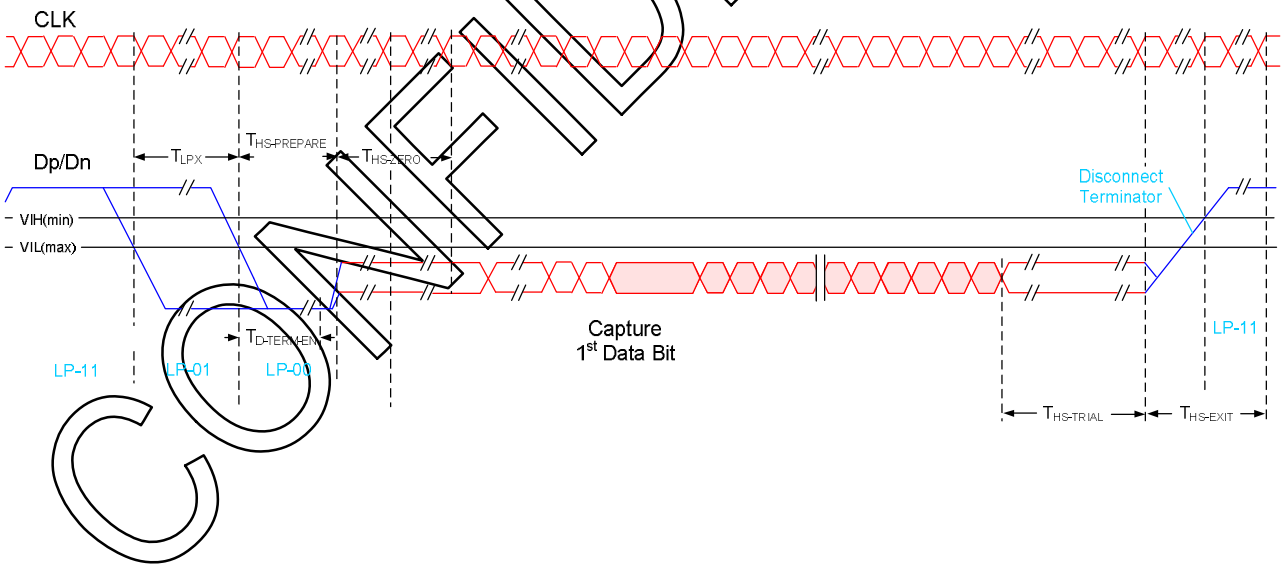
9.6.4 DSI Timing Characteristics

HS Data Transmission Burst

Ø Switching the Clock Lane between HS clock transmission and Low Power Mode

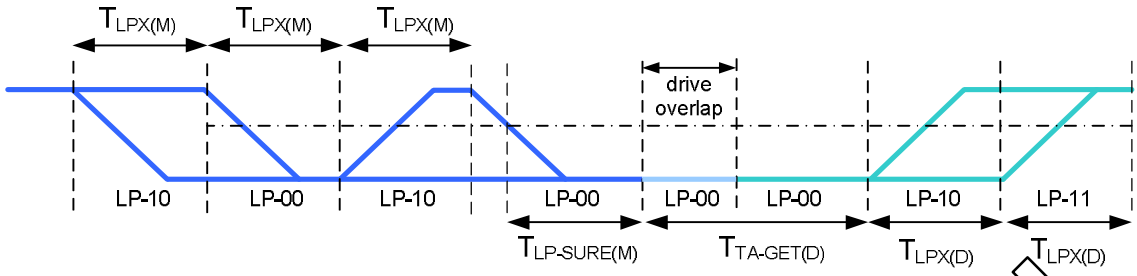


Ø HS Data Transmission Burst

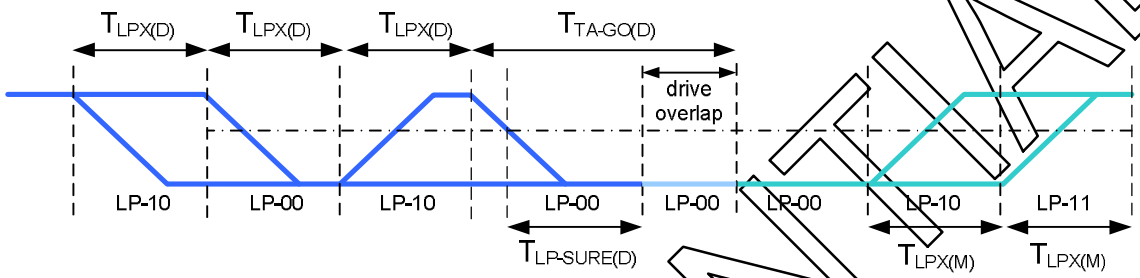


Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	96*UI			ns

Ø Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX(D)}$			ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX(D)}$			ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:

1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

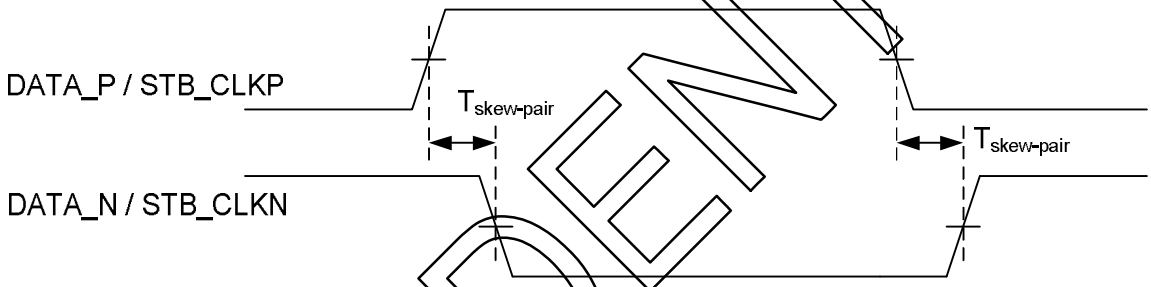
2. Transmitter-specific parameter

9.6.5 MDDI Timing Characteristics

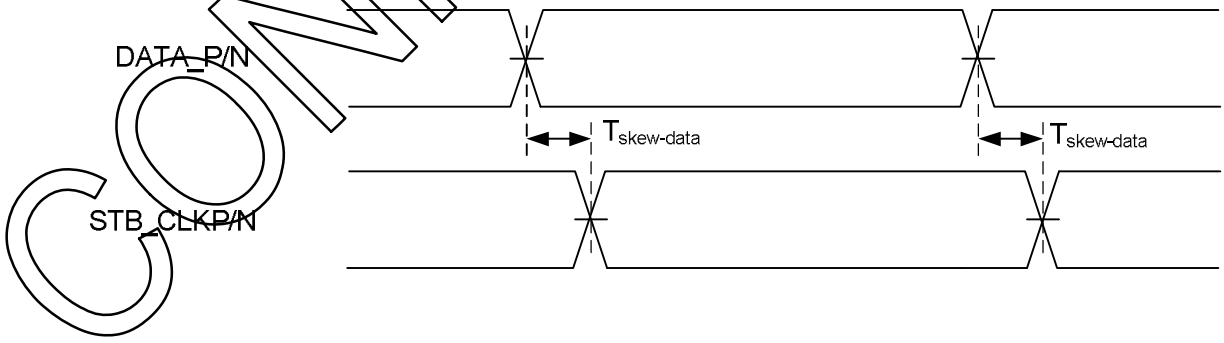
(AGND=DGND=0V, IOVCC=1.65V to 3.3V, VDD=2.5V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
STB_CLKP/N DATA_P/N	1/Tbit	Data transfer rate	-	-	400	Mbps
STB_CLKP/N DATA_P/N	|Tskew-pair|	Differential transfer input skew	-	-	0.25	ns
STB_CLKP/N DATA_P/N	|Tskew-data|	Data/Strobe input skew	-	-	0.45 * Tbit	ns

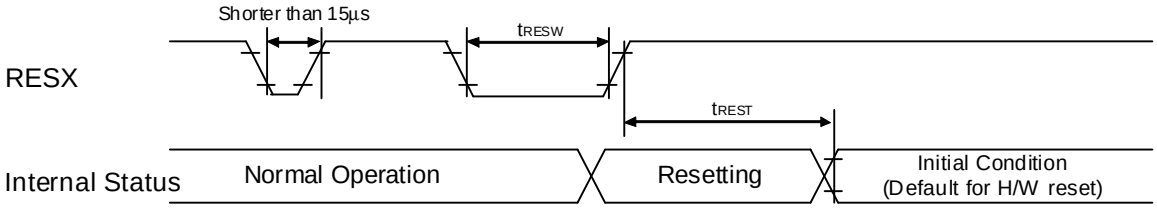
Skew between MDDI positive and negative signal pair



Skew between DATA_P/N and STB_CLKP/N



9.6.6 Reset Timing



Reset input timing:

IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	15	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

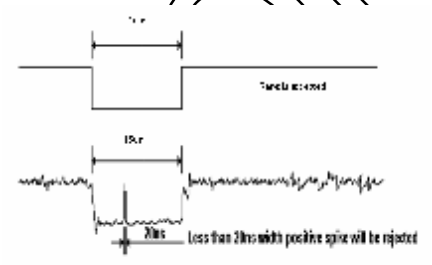
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 15µs	Reset
Between 5µs and 15µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9.7 External Component

Pad Name	Connection	Typical Value	Max Ability
VCI	connect to capacitor, VCI—||—GND	2.2uF	6.3V
IOVCC	connect to capacitor, IOVCC—||—GND	1.0uF	6.3V
MLDO	connect to capacitor, MLDO—||—GND	1.0uF	6.3V
DVDD	connect to capacitor, DVDD—||—GND	1.0uF	6.3V
DDVDL	connect to capacitor, DDVDL—||—GND	1.0uF	10V
DDVDH	connect to capacitor, DDVDH—||—GND	1.0uF	10V
C13A C13B	connect to capacitor, C13A—||—C13B	1.0uF	6.3V
C12A C12B	connect to capacitor, C12A—||—C12B	1.0uF	6.3V
C11A C11B	connect to capacitor, C11A—||—C11B	1.0uF	6.3V
C21A C21B	connect to capacitor, C21A—||—C21B	1.0uF	16V
VGL (option)	connect to capacitor, VGL—||—GND	1.0uF	25V
VGH (option)	connect to capacitor, VGH—||—GND	1.0uF	25V
VCL (option)	connect to capacitor, VCL—||—GND	1.0uF	6.3V
VREG1 (option)	connect to capacitor, VCL—||—GND	1.0uF	6.3V
NVREF (option)	connect to capacitor, VCL—||—GND	1.0uF	6.3V
VREF (option)	connect to capacitor, VCL—||—GND	1.0uF	6.3V