晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AE320480C0FET00
APPROVED BY	
DATE	

☐Approved For Specifications
☑**Approved For Specifications & Sample**

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2013/05/16	--	New Release	Alan
2013/9/27	5	Correct the Operating & Storage Temp	Alan

A. DESCRIPTION AND TABLE OF CONTENTS

AE320480C0FET00 is full-color 3.5” active-matrix organic light-emitting diode display module with HVGA pixel resolution (480x320XRGB). The driver IC used for this display module is HX-5227-A all-in-one driver which can display 16.7 M colors. The driver is mounted on the glass. Flexible printed circuit assembly bonded to the glass includes power generation circuit for the display and serves as the interconnection to drive the display module.

1.FEATURES

- Display technology: active matrix organic light emitting diode.
- Color depth : 16.7M color (24bit 8(R):8(G):8(B)).
- Resolution : 320(H)xRGB(H)x480(V).
- Driver IC : HX5227-A, All-in-One.
- Thickness: 1.21 mm.
- Interfaces supported :

MIPI-DBI 8/16/24 bit MPU parallel interface,

MIPI-DPI 8/16/24 data lines parallel video (RGB) interface

MIPI-DBI Serial data transfer interface

2.ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are listed on Table

1. When used outside absolute

maximum ratings, the Module may be permanently damaged.

Table 1: Absolute maximum ratings

Parameter	Symbol	Values		UNIT	Notes
		MIN	MAX		
Supply Voltage	VCI	-0.3	+5.5	[V]	Maximim IC rating
Supply Voltage	IOVCC	-0.3	+3.6	[V]	Maximim IC rating
Operating Temp.	T_{OP}	-20℃	60℃	[℃]	
Storage Temp	T_{ST}	-30℃	70℃	[℃]	
Operating Humidity	H_{OP}		95	[%]	
Storage Humidity	H_{ST}		95	[%]	

3.ELECTRICAL CHARACTERISTICS

Using the module within the following specifications is strongly recommended for normal operation. If these characteristics are exceeded during normal operation, the display module may malfunction and cause poor reliability.

Table 2: Electrical specifications

Parameter	Symbol	Values			Unit	Notes
		MIN	TYP	MAX		
Power supply voltage	VCI	3.3	3.7	4.2	[V]	
	IOVCC	1.65	-	3.3	[V]	
Power supply current (normal operation)	I_VCI	-	200	500	[mA]	Note [1]
	I_IOVCC	-	-	300	[µA]	
Power supply current (Sleep-in mode)	I_VCI	-	3.5	-		Note [2]
	I_IOVCC	-	11	-		Note [3]
Module Power consumption (normal operation)	Pc_n	-	0.7	1.5	[W]	Note [1]
Input High Voltage	V_{IH}	0.7xIOVCC	-	IOVCC	[V]	
Input Low Voltage	V_{IL}	-0.3V	-	0.3xIOVCC	[V]	
Output high voltage (DB0-23 Pins, SDA)	V_{OH1}	0.8xIOVCC	-	-	[V]	
Output low voltage (DB0-23 Pins, SDA)	V_{OL1}	-	-	0.2xIOVCC	[V]	

Note:

[1] – MAX value corresponds to displaying flat white image at maximum brightness.

[2] – will be verified after module manufacturing and characterization; listed value is based on Drive-IC test;

[3] – will be verified after module manufacturing and characterization;
listed value is based on Drive-IC test and Power IC specification.

For detailed description of electrical/command data and timing, please refer to Driver IC specification.

4.INTERFACE

4.1. Block-diagram

Block-diagram of AMOLED display module is shown in Figure 1.

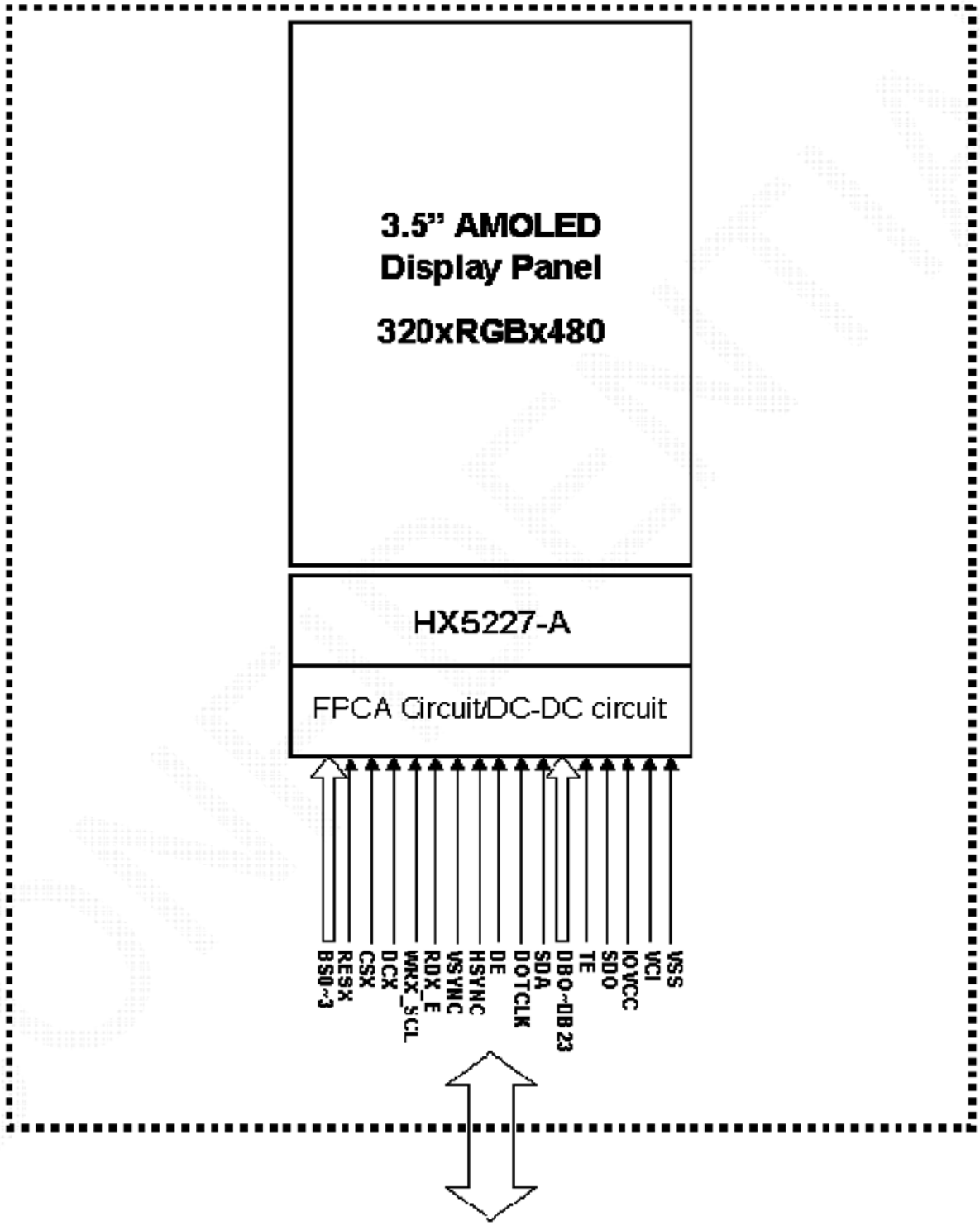

Figure 1: Block-diagram of AMOLED display module

4.2. Pin assignment of module connector

61-pin FPC connector is used to connect electronics interface and power of the module. The connector is a model # 04-6296-061-931-846+ manufactured by Kyocera.

Table 3: Module connector pin configuration

<table>
<tr><th>Pin no.</th><th>I/O</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>2</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>3</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>4</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>5</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>6</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>7</td><td>P</td><td>VCI</td><td>A power supply for the analog power, DC/DC converter.</td></tr>
<tr><td>8</td><td>P</td><td>VCI</td><td>A power supply for the analog power, DC/DC converter.</td></tr>
<tr><td>9</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>10</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>11</td><td>P</td><td>IOVCC</td><td>A power supply for the I/O circuit and logic power.</td></tr>
<tr><td>12</td><td>P</td><td>IOVCC</td><td>A power supply for the I/O circuit and logic power.</td></tr>
<tr><td>13</td><td>O</td><td>SDO</td><td>Serial data output.</td></tr>
<tr><td>14</td><td>O</td><td>TE</td><td>Serves TE (Tearing Effect) pin on MPU interface.</td></tr>
<tr><td>15</td><td>I/O</td><td>DB23</td><td rowspan="25"><table><tr><th>Interface mode</th><th>Command</th><th>Data</th></tr><tr><td>DBI 8-bit</td><td>DB7~0</td><td>DB7~0</td></tr><tr><td>DBI 16-bit</td><td>DB7~0</td><td>DB15~0</td></tr><tr><td>DBI 24-bit</td><td>DB7~0</td><td>DB23~0</td></tr><tr><td>DPI 8-bit</td><td>SDA</td><td>DB7~0</td></tr><tr><td>DPI 16-bit</td><td>SDA</td><td>DB15~0</td></tr><tr><td>DPI 24-bit</td><td>SDA</td><td>DB23~0</td></tr></table></td></tr>
<tr><td>16</td><td>I/O</td><td>DB22</td></tr>
<tr><td>17</td><td>I/O</td><td>DB21</td></tr>
<tr><td>18</td><td>I/O</td><td>DB20</td></tr>
<tr><td>19</td><td>I/O</td><td>DB19</td></tr>
<tr><td>20</td><td>I/O</td><td>DB18</td></tr>
<tr><td>21</td><td>I/O</td><td>DB17</td></tr>
<tr><td>22</td><td>I/O</td><td>DB16</td></tr>
<tr><td>23</td><td>I/O</td><td>DB15</td></tr>
<tr><td>24</td><td>I/O</td><td>DB14</td></tr>
<tr><td>25</td><td>I/O</td><td>DB13</td></tr>
<tr><td>26</td><td>I/O</td><td>DB12</td></tr>
<tr><td>27</td><td>I/O</td><td>DB11</td></tr>
<tr><td>28</td><td>I/O</td><td>DB10</td></tr>
<tr><td>29</td><td>I/O</td><td>DB9</td></tr>
<tr><td>30</td><td>I/O</td><td>DB8</td></tr>
<tr><td>31</td><td>I/O</td><td>DB7</td></tr>
<tr><td>32</td><td>I/O</td><td>DB6</td></tr>
<tr><td>33</td><td>I/O</td><td>DB5</td></tr>
<tr><td>34</td><td>I/O</td><td>DB4</td></tr>
<tr><td>35</td><td>I/O</td><td>DB3</td></tr>
<tr><td>36</td><td>I/O</td><td>DB2</td></tr>
<tr><td>37</td><td>I/O</td><td>DB1</td></tr>
<tr><td>38</td><td>I/O</td><td>DB0</td></tr>
<tr><td>39</td><td>I/O</td><td>SDA</td><td>Serial data input/output.</td></tr>
</table>

<table>
<tr><td>40</td><td>I</td><td>DOTCLK</td><td>Dot clock signal.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>41</td><td>I</td><td>DE</td><td>A data enable signal in DPI I/F mode.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>42</td><td>I</td><td>HSYNC</td><td>Line synchronizing signal.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>43</td><td>I</td><td>VSYNC</td><td>Serves VS signal pin on DPI interface. (Input pad).
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>44</td><td>I</td><td>RDX_E</td><td>DBI Type-A: 0: Read/Write disable, 1: Read/Write enable.
DBI Type-B: Serves as a read signal and read data at the low level.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>45</td><td>I</td><td>WRX_SCL</td><td>DBI Type-A mode: 0: Read/Write disable, 1: Read/Write enable.
DBI Type-B mode: Serves as a write signal and write data at the low level. DBI Type-C mode: it servers as SCL (Serial Clock)
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>46</td><td>I</td><td>DCX</td><td>DBI Type-A/B: Data / Command Selection pin
DBI Type-C Option3: Data / Command Selection pin.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>47</td><td>I</td><td>CSX</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If this pin is not used, please connect it to VSS or IOVCC.</td></tr>
<tr><td>48</td><td>I</td><td>RESX</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSS or IOVCC).</td></tr>
<tr><td>49</td><td>I</td><td>BS0</td><td rowspan="5"><table>
<tr><th>BS 3</th><th>BS 2</th><th>BS 1</th><th>BS 0</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>DBI TYPE-B 8-bit</td><td>DB23-DB8: Unused
DB7-DB0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>DBI TYPE-B 16-bit</td><td>DB23-DB16: Unused
DB15-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>DBI TYPE-B 24-bit</td><td>DB23-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>DBI TYPE-C Option 1</td><td>SDA, DB23-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>DBI TYPE-C Option 3</td><td>SDA, DB23-DB0</td></tr>
</table></td></tr>
<tr><td>50</td><td>I</td><td>BS1</td></tr>
<tr><td>51</td><td>I</td><td>BS2</td></tr>
<tr><td>52</td><td>I</td><td>BS3</td></tr>
<tr><td>53</td><td>P</td><td>VCI</td><td>A power supply for the analog power, DC/DC converter.</td></tr>
<tr><td>54</td><td>P</td><td>VCI</td><td>A power supply for the analog power, DC/DC converter.</td></tr>
<tr><td>55</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>56</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>57</td><td>P</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>58</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>59</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>60</td><td>-</td><td>NC</td><td>-</td></tr>
<tr><td>61</td><td>-</td><td>NC</td><td>-</td></tr>
</table>

4.3. Interface characteristics

4.3.1 DBI Type B interface characteristics

Table 4: DBI Type B interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tAST tAHT	Address setup time Address hold time (Write/Read)	0 10	- -	ns	-
CSX	tCS tRCS tRCS tCSF	Chip select setup time (Write) Chip select setup time (Read register) Chip select setup time (GRAM) Chip select wait time (Write/Read)	10 45 355 10	- - - -	ns	-
WRX_SCL	tWC tWC tWC tWRH tWRL	Write cycle (write register) Write cycle (write GRAM@SLPOUT) Write cycle (write GRAM@SLPIN) Control pulse “H” duration Control pulse “L” duration	50 47 100 15 15	740 740 740 - -	ns	-
RDX_E	tRC tRC tRDH tRDL tRDL	Read cycle (read register) Read cycle (GRAM) Control pulse “H” duration Control pulse “L” duration(read register) Control pulse “L” duration(GRAM)	160 450 90 35 345	- - - - -	ns	-
DB[23:0]	tWDT tWHT tRACC tRACC tROH	Data setup time Data hold time Read access time(read register) Read access time(GRAM) Output disable time	10 10 - - 10	- - 40 340 -	ns	For maximum CL=30pF For minimum CL=8pF

Notes: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

4.3.2 DBI Type C interface characteristics

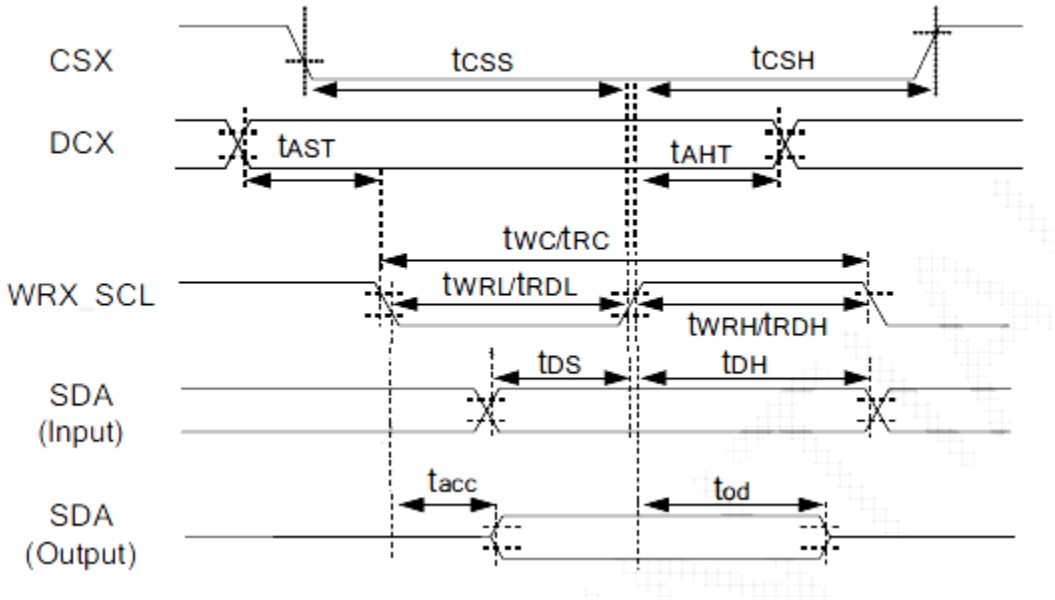

Figure 2: DBI Type C Interface Characteristics

Table 5: DBI Type C Interface Characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tCSS	Chip select setup time (Write)	15	-	ns	-
	tCSS	Chip select setup time (Read)	60	-		
	tCSH	Chip select hold time (Write)	15	-		
	tCSH	Chip select hold time (Read)	65	-		
DCX	tAST	Address setup time	0	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-		
WRX_SCL (Write)	tWC	Write cycle	66	-	ns	-
	tWRH	Control pulse "H" duration	15	-		
	tWRL	Control pulse "L" duration	15	-		
WRX_SCL (Read)	tRC	Read cycle	150	-	ns	-
	tRDH	Control pulse "H" duration	60	-		
	tRDL	Control pulse "L" duration	60	-		
SDA (Input)	tDS	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tDT	Data hold time	10	-		
SDA (Output)	tRACC	Read access time	10	50	ns	
	tOD	Output disable time	15	50		

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

4.3.3 DPI (RGB) interface characteristics

Different from other interfaces that selected by setting BS3~0 pins, DPI (RGB) interface is enabled by setting RM=1 in register 0xB3h through DBI Type C (serial) interface. See Table 6. The DPI (RGB) interface includes three types, 16-/ 18-/ 24-bit data format. They are selected by setting register 0x3Ah (set_pixel_format). See Table 7.

Table 6: DPI (RGB) Interface Setup Register

B3 H	SETRGBIF(Set RGB interface related register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	↑	1	-	-	SDO_EN	-	-	DPL	HSPL	VSPL	EPL	00
2nd parameter	1	↑	1	-		ENC[2:0]			-	-	DM	RM	00

Description

This command is used to set RGB interface related register

SDO_EN: SDO pin enable.

SDO_EN	Input pin	Output pin
1	SDA	SDO
0	SDA	SDA

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	Display image	Operation
0	High	Enable	Write data to D17-0
0	Low	Disable	Disable
1	High	Disable	Disable
1	Low	Enable	Write data to D17-0

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

DM: Specify the operation mode of LCD display. DM allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode).

DM	Operation Mode
0	System interface
1	RGB interface

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the

data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	System interface
1	RGB interface

Note: (1) The register is set only through the system interface.
(2) A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

ENC[2:0]: Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle
000	1 frame
001	2 frame
010	3 frame
011	4 frame
100	5 frames
101	6 frames
110	7 frames
111	8 frame

Restriction: Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Table 7: DPI (RGB) Interface Data Format Setup Register

Register 3Ah	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode
50h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	16-bit 65K-Color
60h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit 262K-Color
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit 16.7M-Color

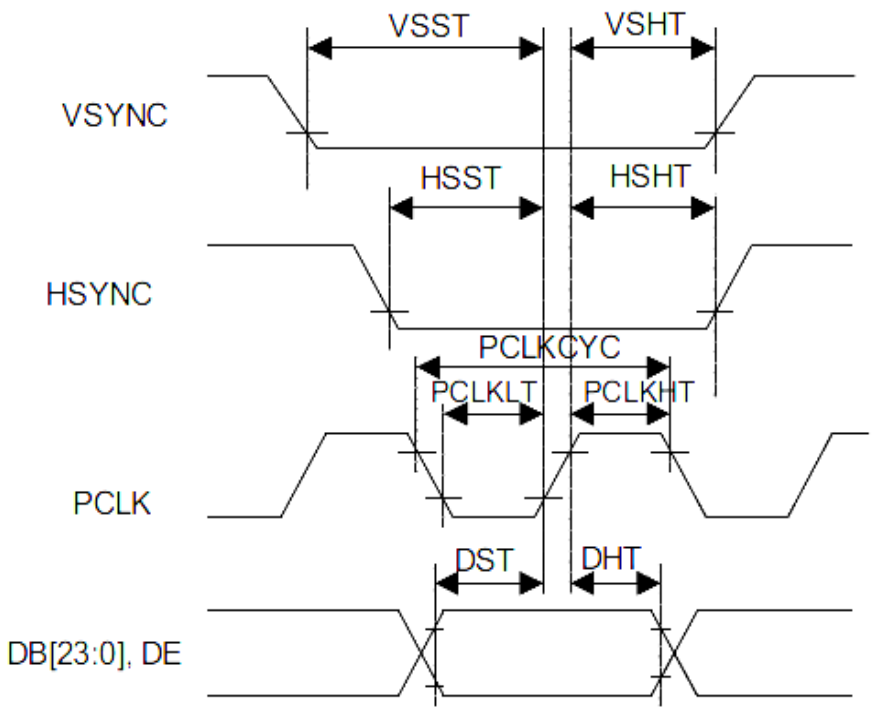

Figure 3: General timings for RGB I/F-1

Table 8: DPI interface characteristics-1

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical sync. Setup Time	VSST	-	10	-	-	ns
Vertical sync. Hold Time	VSHT	-	10	-	-	ns
Horizontal sync. Setup Time	HSST	-	10	-	-	ns
Horizontal sync. Hold Time	HSHT	-	10	-	-	ns
Pixel Clock Cycle	PCLKCYC	24-/18-/ 16-bit 8-bit	47 33	-	-	ns
Pixel Clock Setup Time	PLCKLT	-	10	-	-	ns
Pixel Clock High Time	PCLKHT	-	10	-	-	ns
Data Setup Time DB[17:0], Enable	DST	-	10	-	-	ns
Data Hold Time DB[17:0], Enable	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal or less than 20ns.

(2) Measure of input signals are using 0.3xIOVCC for low state and 0.7xIOVCC for high state.

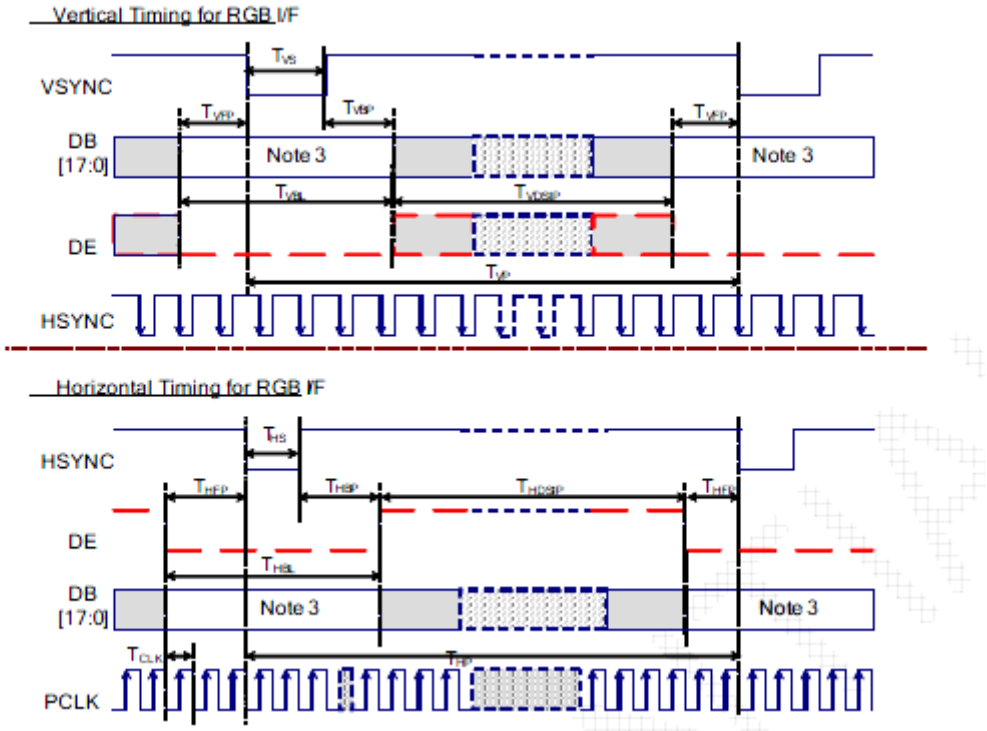

Figure 4: General timings for RGB I/F-2

Table 9: DPI interface characteristics-2

Item	Symbol	Condition	Specification			Unit
			Min	Typ.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	486	-	-	HS
Vertical low pulse width	T_{VS}	-	2	-	-	HS
Vertical front porch	T_{VFP}	-	2	-	-	HS
Vertical back porch	T_{VBP}	-	2	-	-	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	6	-	-	HS
Vertical active area	T_{VDISP}	-	-	480	-	HS
			-		-	HS
					-	HS
Vertical refresh rate	T_{VRR}	Frame rate	50	60	70	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	326	-	-	DOTCLK
Horizontal low pulse width	T_{HS}	-	2	-	-	DOTCLK
Horizontal front porch	T_{HFP}	-	2	-	-	DOTCLK
Horizontal back porch	T_{HBP}	-	2	-	-	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	6	-	-	DOTCLK
Horizontal active area	T_{HDISP}	-	-	-	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	9	-	-	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V

(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.

(3) HP is multiples of PCLK.

5.POWER ON/OFF TIMING AND POWER SEQUENCE

5.1. Power-On timing

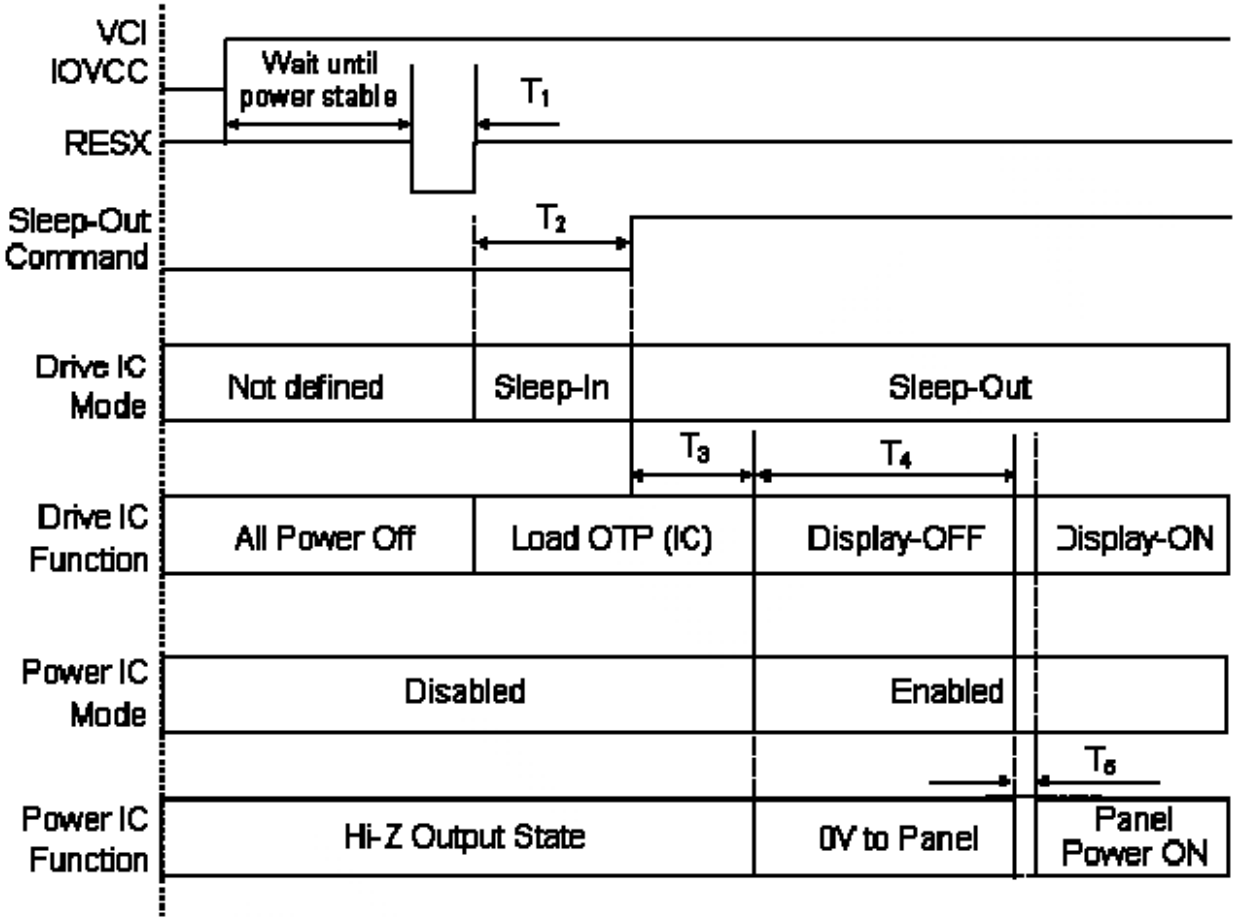

Figure 5: Power-on timing

Table 10: Power-on timing parameters

Parameter	Values			Unit
	MIN	TYP	MAX	
T_1	10	-	-	µs
T_2	6	-	-	ms
T_3	2	-	-	ms
T_4	-	-	10	ms
T_5			4	ms

5.2. Power-off timing

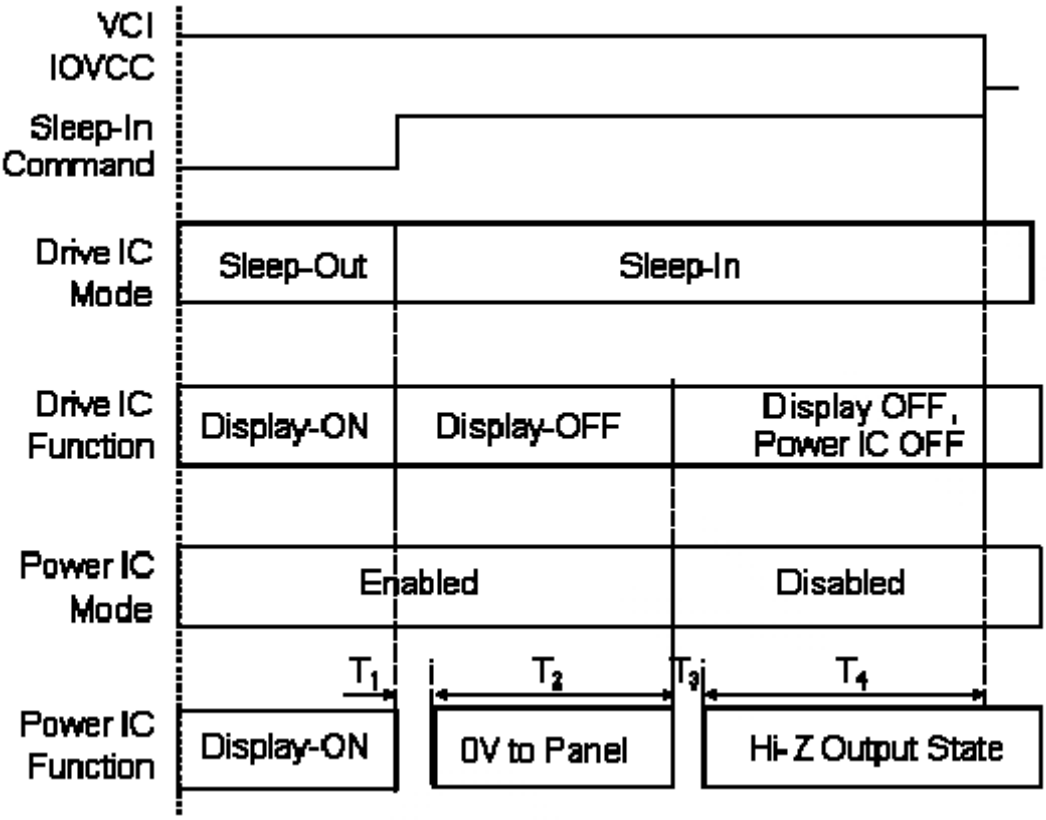

Figure 6: Power-off timing

Table 11: Power-off timing parameters

Parameter	Values			Unit
	MIN	TYP	MAX	
T_1	-	-	5	ms
T_2	5	-	-	ms
T_3	1	-	-	ms
T_4	0	-		ms

5.3. Power ON/OFF sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order. During power off, display is in the Sleep Out mode, IOVCC must be powered down minimum 120msec after RESX has been released. During power off, if display is in the Sleep In mode, IOVCC and VCI can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. Please refer to Driver IC specifications for further details.

6. OPTICAL CHARACTERISTICS

Optical characteristics are determined after the unit has been 'ON' and stable at 30% of full white for approximately 30 minutes in a dark environment at 25°C. The values specified are at a viewing angle of Φ and Θ equal to 0°. Figure 8 represents additional illustration about measurement method.

The chromaticity coordinates CIEx,y for R, G, B, W are defined as color coordinate value on the CIE 1931 color chart.

Contrast ratio is defined by the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on at full white}}{\text{Luminance of full black}}$$

The viewing angle is defined as shown on Figure 9. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

Table 6: Optical characteristics of display module

PARAMETER	Value			UNITS	COMMENTS
	MIN	TYP.	MAX		
Normal mode Luminance	-	200	-	cd/m^2	Display Average
CIEx (White)	-	0.33	-		x, y (CIE 1931)
CIEy (White)	-	0.35	-		
CIEx (Red)	-	0.66	-		
CIEy (Red)	-	0.34	-		
CIEx (Green)	-	0.33	-		
CIEy (Green)	-	0.62	-		
CIEx (Blue)	-	0.15	-		
CIEy (Blue)	-	0.14	-		
Dark Room Contrast	100000:1	-	-		
Viewing Angle	5	-	175	degree	
Response Time	-	1	-	us	

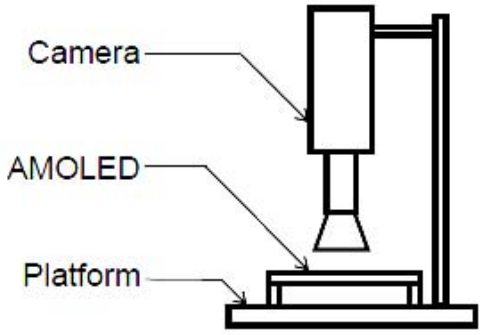

Figure 8: Optical measurement apparatus

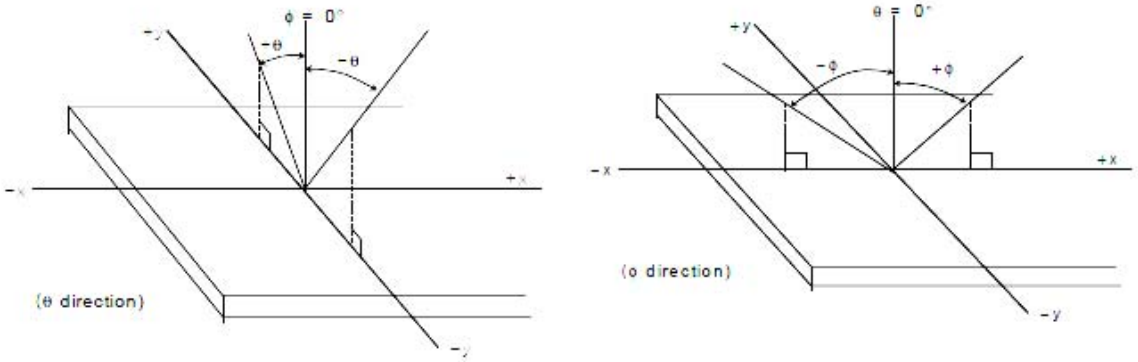

Figure 8: Definition of viewing angle

7. MECHANICAL CHARACTERISTICS

Table 7 below provides general mechanical characteristics of the display module. Mechanical drawing of the display module is shown in Figure 10 on the next page.

Table 7: Mechanical characteristics of display module

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	320 x 3 x 480	dot
2	Pixel Pitch	0.51 (W) x 0.153 (H)	mm^2
3	Active Area	48.96 (W) x 73.44 (H)	mm^2
4	Panel Size	52.9 (W) x 83.5 (H)	mm^2
5	Module Size	52.9 (W) x 120.6 (H) x 1.21 (D)	mm^3
6	Diagonal A/A size	3.5	inch
7	Module Weight	TBD	gram

8. RELIABILITY

Category	Description	Test conditions
Storage Environment	High temperature storage	+70°C/240H
	Low-temperature storage	-20°C/240H
	Temperature cycle	-40°C (60m) / 85°C(60m) 72H total
	High temperature, high humidity storage	60°C/95%/72H
Operation Environment	High temperature operation	+60°C/72H
	Low temperature operation	-20°C/72H
Mechanical	Vibration	10 to 55 Hz, 0.15 mm 20 cycles for each X,Y,Z

9.OUTLINE DIMENSION