MIPI Alliance Standard for Display Bus Interface v2.0

MIPI Board approved 16 November 2005

* Caution to Implementers *

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MIPI Alliance Standard for Display Bus Interface

Version 2.00 – 29 November 2005

MIPI Board Approved 16-Nov-2005

Further technical changes to DBI are expected as work continues in the Display Working Group

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Contents

MIPI Alliance Standard for Display Bus Interface

1 Overview

This document describes Display Bus Interface (DBI), which is used for display modules. DBI can be configured for 1, 2, 8, 9 or 16 data signals.

This document defines the interface parameters outlined below for both the host processor and display module.

- Electrical
- Timings
- Protocol examples
- Measurement methods
- Color coding
- Command set to control display behaviors

1.1 Scope

The Display Bus Interface specification defines the electrical and logical interfaces for mobile device host processors and display modules. Logical control of the display module functional blocks such as power supply, timing generator and display drivers is also within the scope of this document. The design of the functional blocks is not within the scope of this specification.

1.2 Purpose

The Display Bus Interface specification is used by manufacturers to design products that adhere to MIPI specifications for mobile device processor and display interfaces.

Implementing the DBI standard reduces the time-to-market and design cost of mobile devices by simplifying the interconnection of products from different manufacturers. In addition, adding new features such as larger or additional displays to mobile devices is simplified due to the extensible nature of the MIPI specifications.

2 Terminology

2.1 Definitions

Command: Digital information used to control display behavior and to identify the connected display module

Data: Digital image data stored in the frame memory or numerical information to define the display module behavior accompanied with a command

Display Controller: Isolated IC silicon chip or integrated functional block in the host processor to control a display module; may or may not include frame memory

Display Device: Functional device which can show image, such as Liquid Crystal Displays

Display Driver IC: IC silicon chip in a display module used to control the display device; may or may not include frame memory

Display Glass: Same as display device, coming from material name

Display Module: Functional module to show image on it, can consists of display device, display driver IC, other peripheral components and circuits and display interface

Display Panel: Same as Display Device, coming from the physical outward appearance of the display device

Frame Memory: Memory device integrated in a display driver IC or display controller in order to provide image data for refreshing the display device. Full-frame memory provides a full screen area of image data while partial-frame memory only provides memory for a portion of the screen area.

Type 1 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, full-frame memory, registers, timing controller, non-volatile memory and control interface.

Type 2 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, partial-frame memory, registers, timing controller, non-volatile memory, control interface and video stream interface.

Type 3 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, registers, timing controller, non-volatile memory, control interface and video stream interface.

Type 4 Display Architecture: One of the defined display module architectures. In DSI, DBI, DPI, and DCS, a display module architecture in which a display module includes a display device, display driver IC, registers, timing controller, control lines and video stream interface.

2.2 Abbreviations

↑ Rising edge active

↓ Falling edge active

AGND	Power ground
CSX	Chip Select, active low
D/CX	Data/Command, Command is active low
DGND	Logic level ground
High-Z	High Impedance
H-Sync	Horizontal Synchronization
RESX	Reset signal, active low
RDX	Read signal
Ta	Ambient Temperature
WRX	Write signal
V_{DD}	Power Supply
V_{DDI}	Logic Level Supply
V-Sync	Vertical Synchronization

2.3 Acronyms

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
DBI	Display Bus Interface
DCS	Display Command Set
DOI	Dependent On Implementation
DSI	Display Serial Interface
I/O	Input/Output
LSB	Least Significant Bit
MIPI	Mobile Industry Processor Interface
MSB	Most Significant Bit

3 References

[1] MIPI Alliance Standard for Display Command Set, version 0.37, October 2005

[2] MIPI Alliance Standard for Display Parallel Interface, version 0.xx, August 2005

[3] MIPI Alliance Standard for Display Serial Interface, version 0.xx, August 2005

4 Display Architectures and Interface Constructions

4.1 Display Architectures

The display module shall be based on Type 1, Type 2, Type 3 or Type 4 display architecture.

The Type 1 Display Architecture should consist of the following functional blocks:

Display Device. Used to show the image data.

Display Driver. May be one or more devices used to drive the display device.

Full-frame memory. Used to hold the image data; can be integrated in the display driver.

Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.

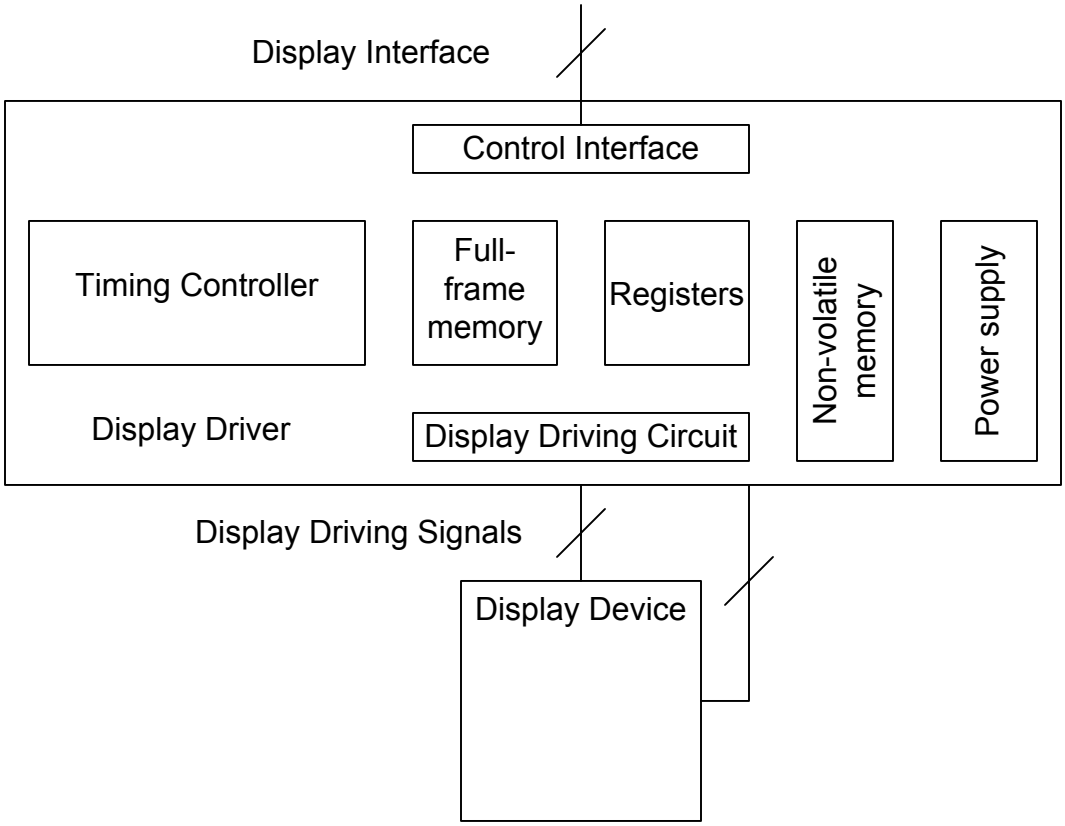
Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.

Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.



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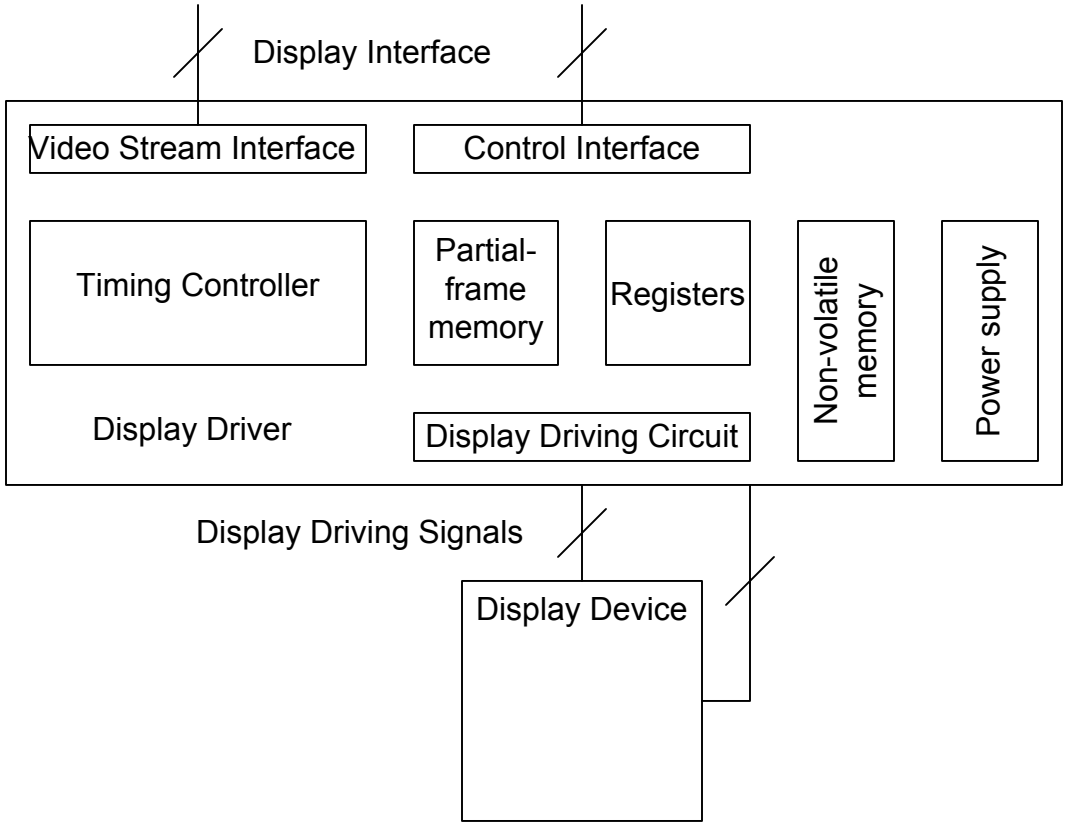
178 **Figure 1 Type 1 Display Architecture Block Diagram**

The Type 2 Display Architecture should consist of the following functional blocks:

- Display Device. Used to show image data.
- Display Driver. May be one or more devices used to drive the display device.
- Partial-frame memory. Used to hold image data. Can be integrated in the display driver.
- Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.
- Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.
- Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.
- Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.
- Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.
- Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.
- Video Stream Interface. Used to receive video image data and timing signals from the host processor.



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198 **Figure 2 Type 2 Display Architecture Block Diagram**

The Type 3 Display Architecture should consist of the following functional blocks:

Display Device. Used to show image data.

Display Driver. May be one or more devices used to drive the display device.

Registers. Used to configure the display module behavior and hold identification information; can be integrated in the display driver.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Non-volatile memory. Used to store default register and configuration values; can be integrated in the display driver.

Control Interface. Provides the interface between the host processor and the display driver; can be integrated in the display driver.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

Video Stream Interface. Used to receive video image data and timing signals from the host processor.

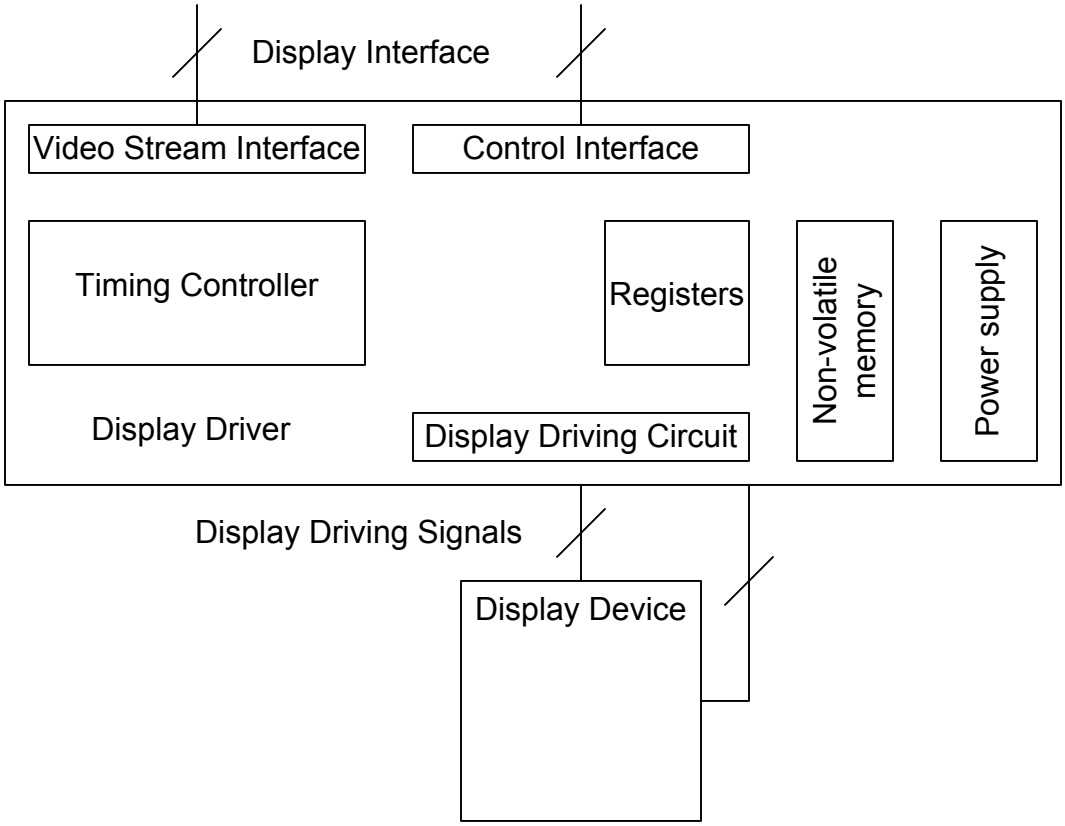


Figure 3 Type 3 Display Architecture Block Diagram

The Type 4 Display Architecture should consist of the following functional blocks:

Display Device. Used to show image data.

Display Driver. May be one or more devices used to drive the display device.

Timing Controller. Provides timing signals to control the display device and display driver based on configuration information; can be integrated in the display driver.

Control lines. Used to receive display behavior control information from the host processor.

Display Driving Circuit. As a part of display driver, used to convert timing signals and voltages to signals appropriate to drive the display device.

Power Supply. Used to convert system voltages to levels usable by the display device and display driver; can be integrated in the display driver.

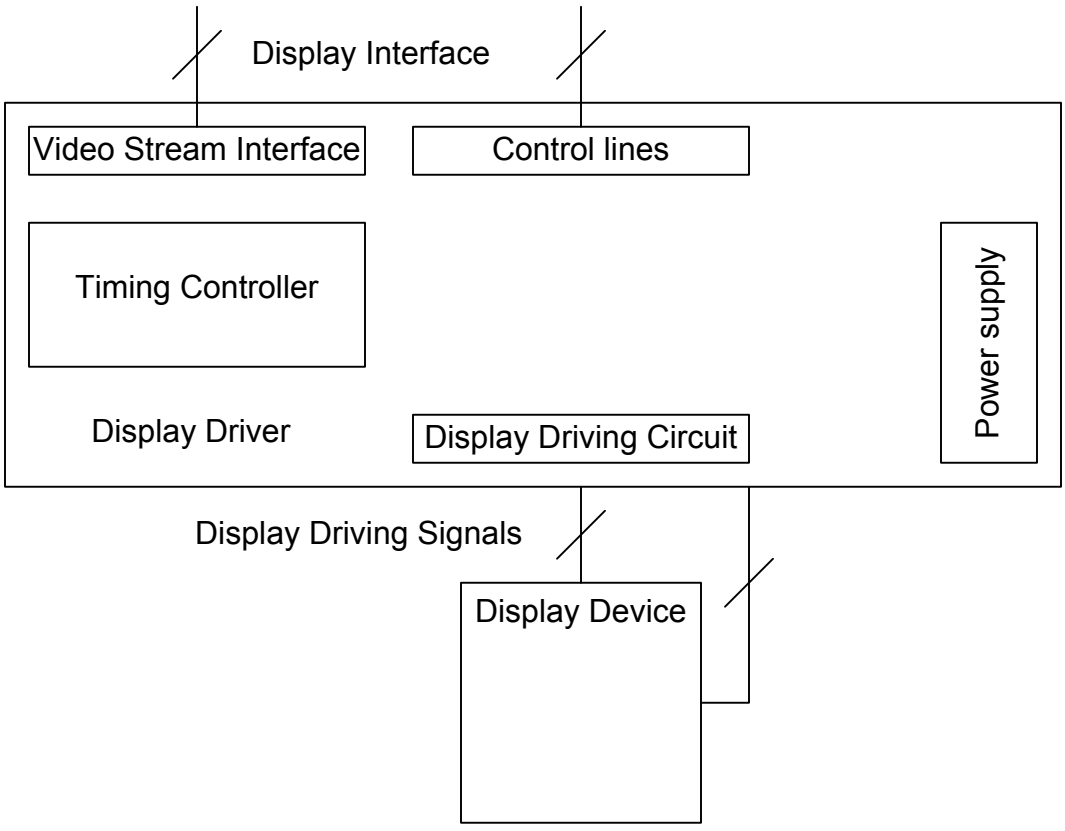


Figure 4 Type 4 Display Architecture Block Diagram

In all architecture types, it is assumed the power supply is under the control of the display driver.

DBI is used for the control interfaces.

Refer to *MIPI Alliance Standard for Display Parallel Interface* [2] for the video stream interface used in type 2, 3 and 4 architectures.

4.2 Display Bus Interface Constructions

The electrical connection between the host processor and a display module consists of two blocks: power and interface. Power is supplied from either the host processor itself or another device under the control of the host to the power block of the display module. Interface blocks are used to transfer information between the host processor and a display module.

There are three types of DBI implementations, named type A, B and C as shown in Figure 5, Figure 6 and Figure 7, respectively.

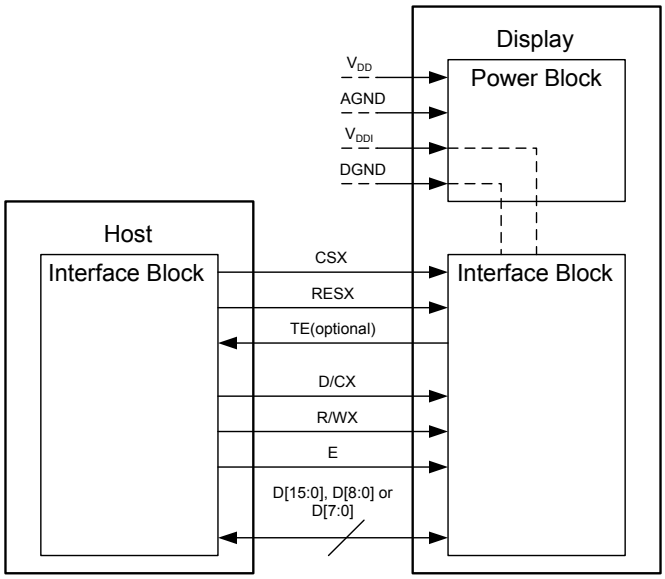


Figure 5 Type A Interface Block Diagram

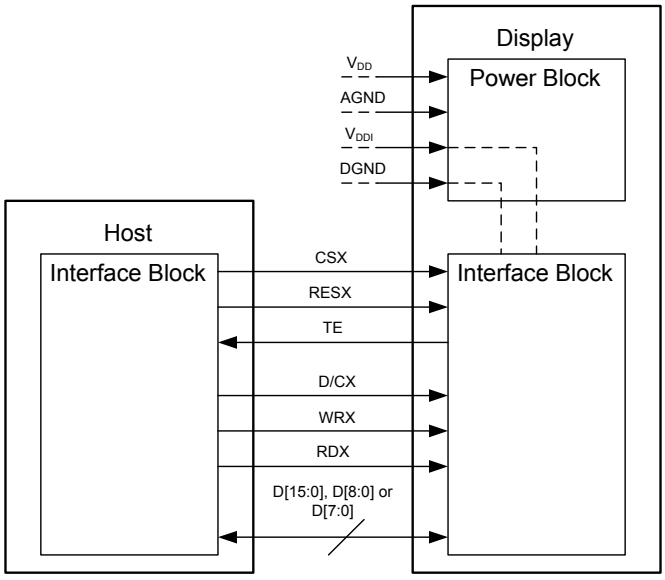


Figure 6 Type B Interface Block Diagram

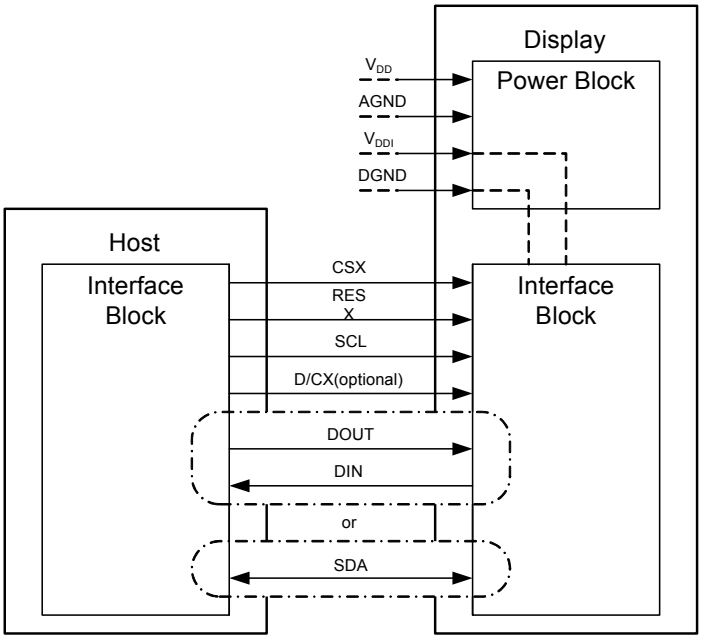


Figure 7 Type C Interface Block Diagram

5 Interface Signal Description

5.1 Power Supply Signals

Table 1 Power Supply Signals

Symbol	Name	Description
V_{DD}	Power supply	Power supply for display module
V_{DDI}	Logic level supply	Logic level supply for interface signals
AGND	Power Ground	GND for power supply
DGND	Logic level ground	GND for logic level

5.2 Interface Signals

5.2.1 Type A Interface

Table 2 Type A Interface Signal Description

Symbol	Name	I/O	Description
CSX	Chip Select	O	In Fixed E mode, host processor writes data (D[15:0], D[8:0] or D[7:0]) at falling edge, or reads at rising edge. In Clocked E mode, the display module is selected when low.
R/WX	Read/Write	O	Host processor reads data (D[15:0], D[8:0] or D[7:0]) when high or writes data (D[15:0], D[8:0] or D[7:0]) when low.
E	E clock	O	In Fixed E mode, this signal is tied high. In Clocked E mode, the host processor reads information (D[15:0], D[8:0], D[7:0]) at rising edge or writes at falling edge.
D[15:0], D[8:0], or D[7:0]	Information	I/O	Information signals
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low.
RESX	Reset	O	Display module is reset when low.
TE	Tearing Effect	I	Tearing Effect (optional).

Note: I/O directions are defined from the host processor perspective.

When CSX is high, the display module ignores all other interface signals.

CSX can be connected to DGND permanently on the display module without limitations.

5.2.2 Type B Interface

Table 3 Type B Interface Signal Description

Symbol	Name	I/O	Description
CSX	Chip Select	O	Display module is selected when low.
RDX	Read	O	Host processor reads information (D[15:0], D[8:0] or D[7:0]) at rising edge.
WRX	Write	O	Host processor writes information (D[15:0], D[8:0] or D[7:0]) at falling edge.
D[15:0], D[8:0] or D[7:0]	Information	I/O	Information signals
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low.
RESX	Reset	O	Display module is reset when low.
TE	Tearing Effect	I	Tearing Effect

Notes:

I/O directions are defined from the host processor perspective.

When CSX is high, the display module ignores all other interface signals.

CSX can be connected to DGND permanently on the display module without limitations.

5.2.3 Type C Interface

Table 4 Type C Interface Signal Description

Symbol	Name	I/O	Description
CSX	Chip Select	O	Display is selected when low.
SCL	Serial Clock	O	Host processor writes information (DOUT or SDA) or reads information (DIN or SDA) at rising edge
DOUT	Information Out	O	Information signal output from host processor
DIN	Information In	I	Information signal input to host processor
SDA	Information	I/O	Bidirectional information signal

Symbol	Name	I/O	Description
D/CX	Data/Command	O	Data is indicated when high and Command is indicated when low (optional).
RESX	Reset	O	Display is reset when low.

Notes:

I/O directions are defined from the host perspective.

When CSX is high, display module ignores all other interface signals.

CSX can be connected to DGND permanently on the display without limitations.

6 Interface I/O Cells

The host processor and display module interface blocks shall be implemented using CMOS I/O cells for interface signals as they are described in Figure 8.

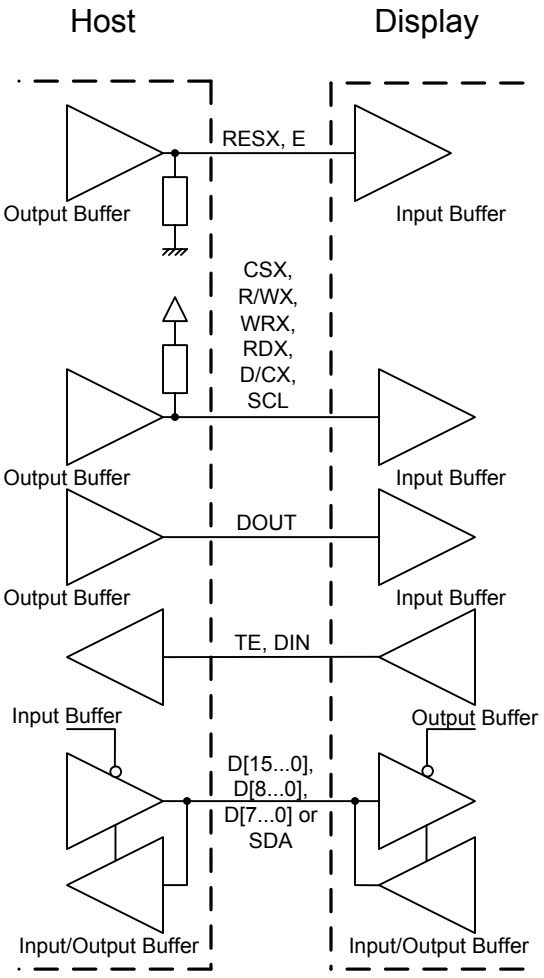


Figure 8 Interface I/O Cells

7 Interface Functional Description

7.1 Type A Interface Write and Read Cycles

7.1.1 Write Cycle

During a write cycle the host processor writes commands or data to the display module via the interface. Type A interfaces support two modes: Fixed E and Clocked E. Both modes utilize CSX, D/CX, R/WX and E signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. D/CX is driven low while a command is present on the interface and pulled high when data is on the interface.

The write cycle is described in Figure 9 and Figure 10.

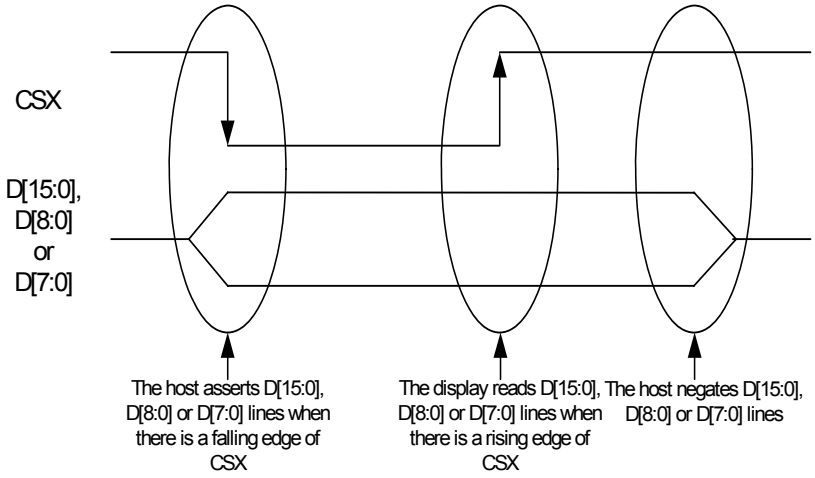


Figure 9 Type A Interface - Fixed E Mode Write Cycle

Note:

1. CSX is an unsynchronized signal; it can be stopped.
2. E signal is tied high in Fixed E mode.

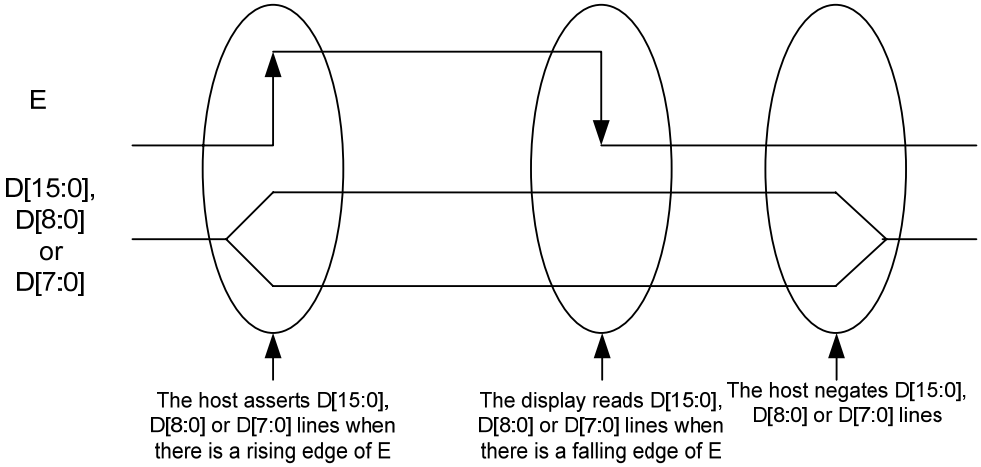


Figure 10 Type A Interface - Clocked E Mode Write Cycle

Notes:

1. E is an unsynchronized signal; it can be stopped.
2. CSX is asserted (taken low) for the same duration as the information signals.

7.1.2 Read Cycle

During a read cycle the host processor reads data from the display module via the interface. Type A interfaces support two modes: Fixed E and Clocked E. Both modes utilize CSX, D/CX, R/WX and E signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. D/CX is driven low during the entire read cycle.

The read cycle is described in Figure 11 and Figure 12.

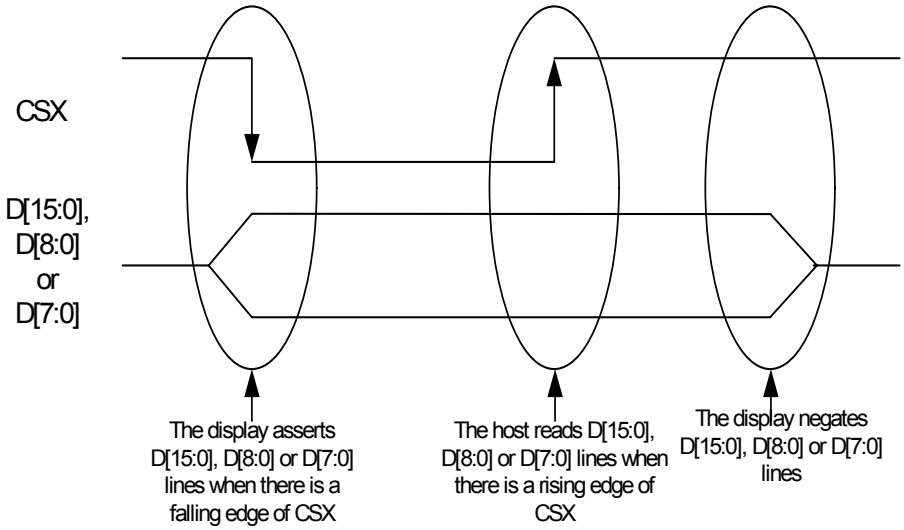


Figure 11 Type A Interface - Fixed E Mode Read Cycle

Note:

1. CSX is an unsynchronized signal; it can be stopped.

2. E signal is tied up to high in Fixed E mode.

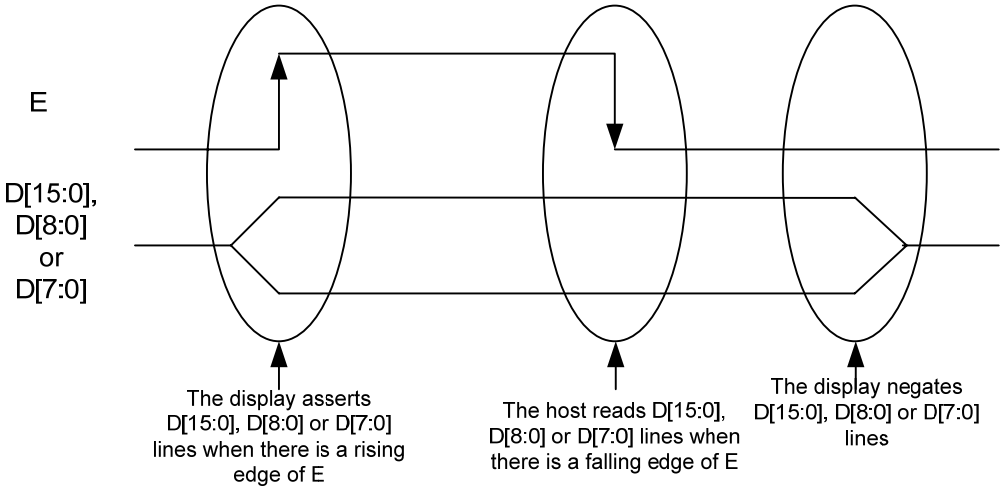


Figure 12 Type A Interface - Clocked E Mode Read Cycle

Note:

1. E is an unsynchronized signal; it can be stopped.
2. CSX is asserted (taken low) for the same duration as the information signals.

7.1.3 Display Read/Write Sequences

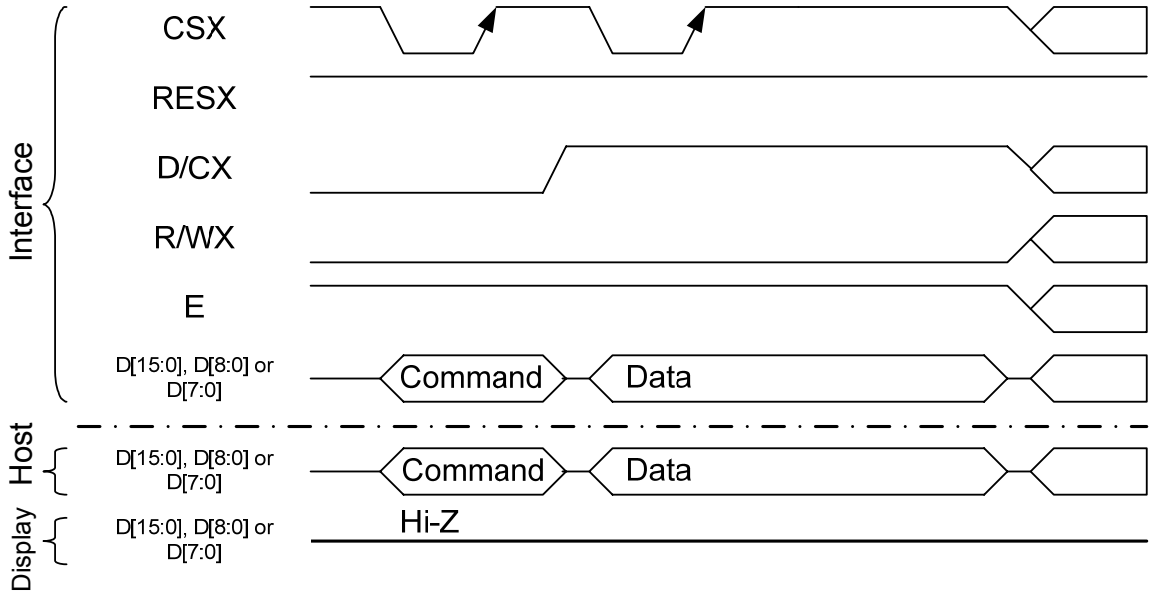
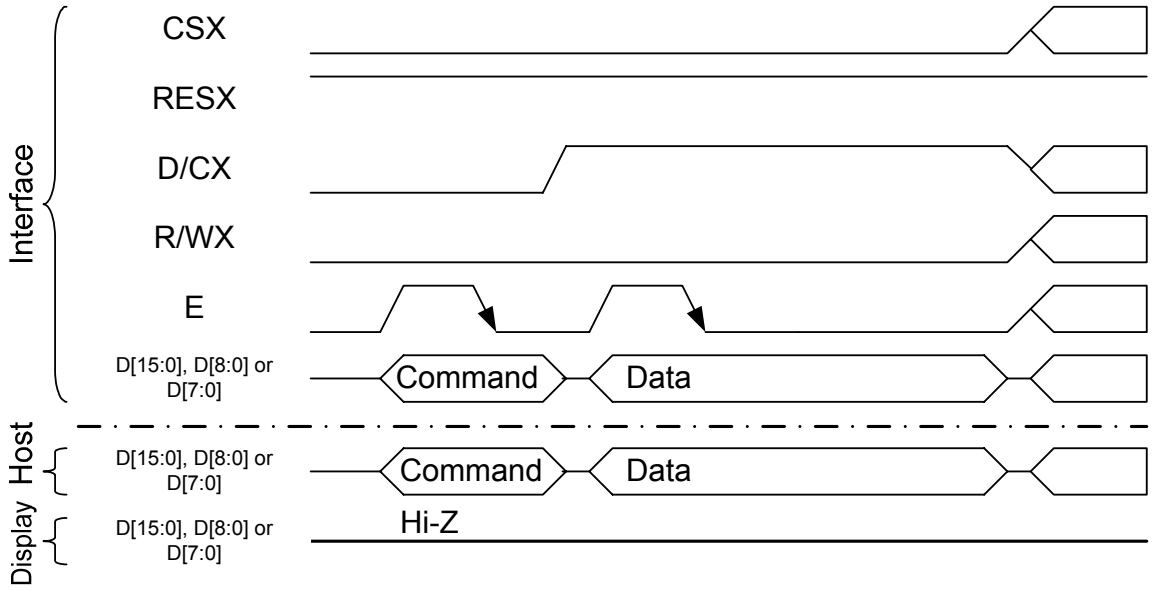


Figure 13 Type A Interface - Example Fixed E Mode Write Sequence



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312 **Figure 14 Type A Interface - Example Clocked E Mode Write Sequence**

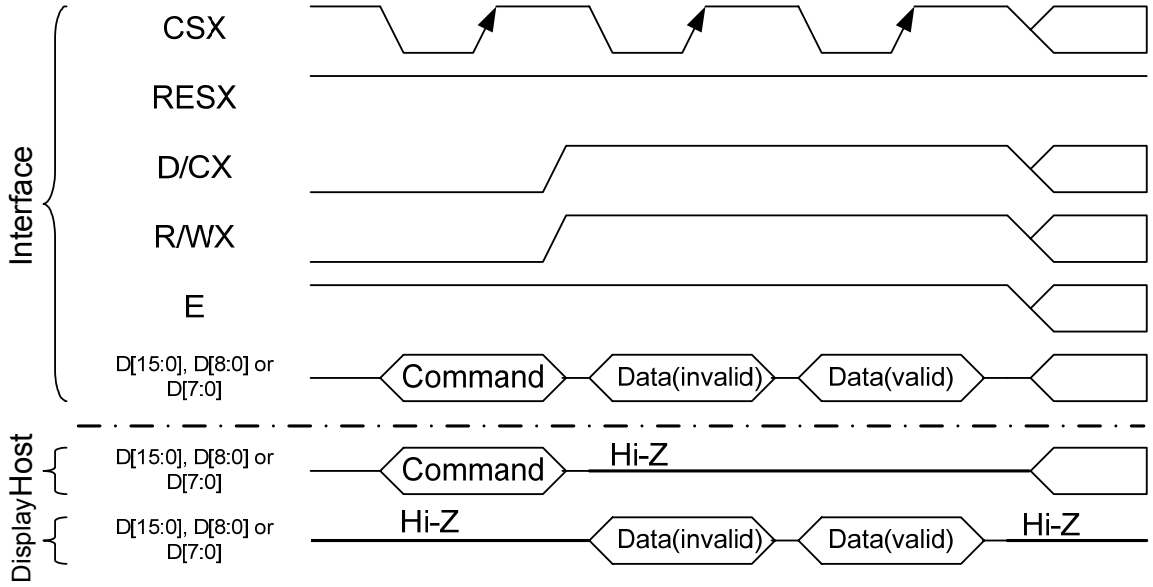


Figure 15 Type A Interface - Example Fixed E Mode Read Sequence

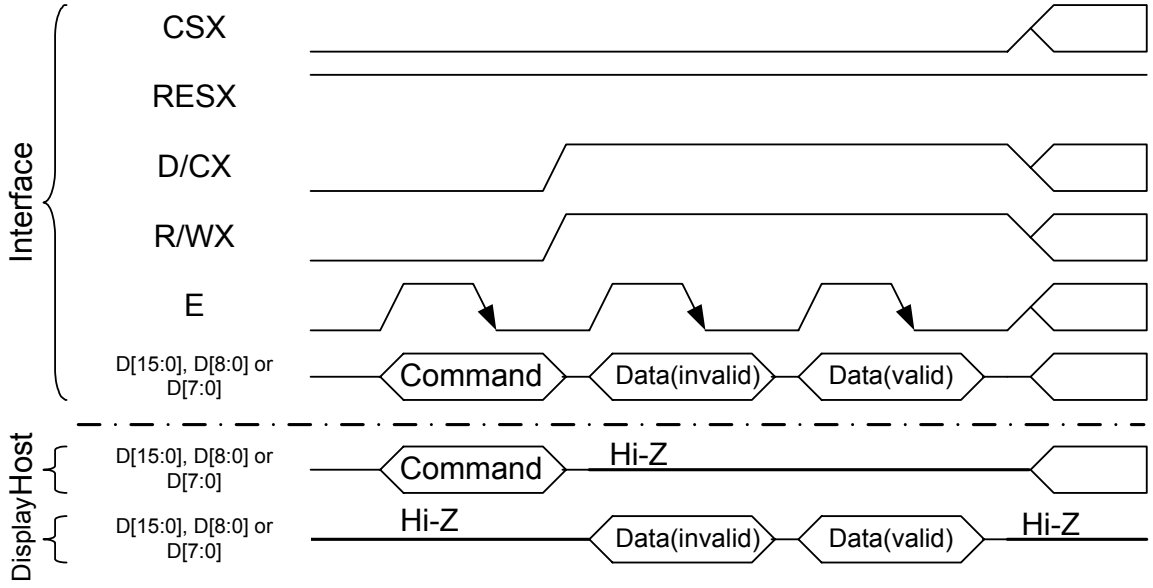


Figure 16 Type A Interface - Example Clocked E Mode Read Sequence

7.2 Type B Interface Write and Read Cycles

7.2.1 Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

Figure 17 shows a write cycle for the type B interface.

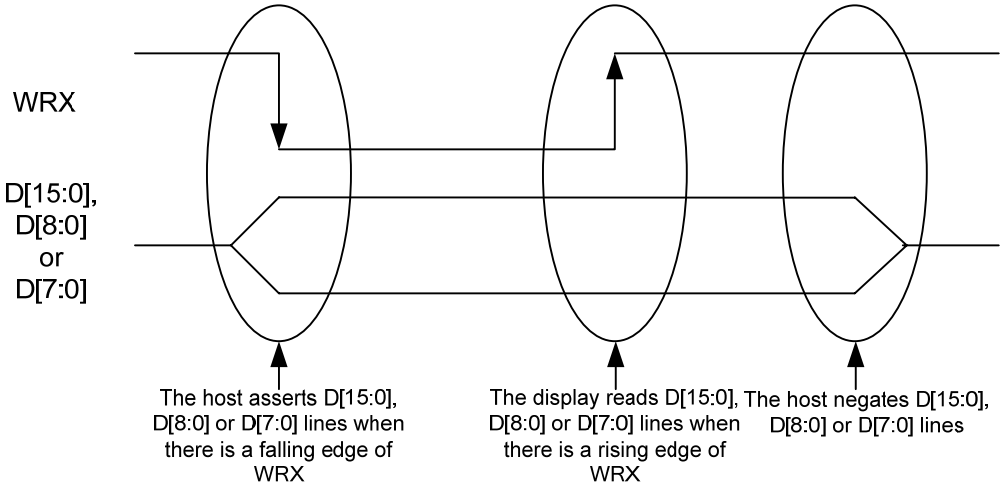


Figure 17 Type B Interface - Write Cycle

Note: WRX is an unsynchronized signal; it can be stopped.

7.2.2 Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]) or sixteen (D[15:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

Figure 18 shows the read cycle for the type B interface.

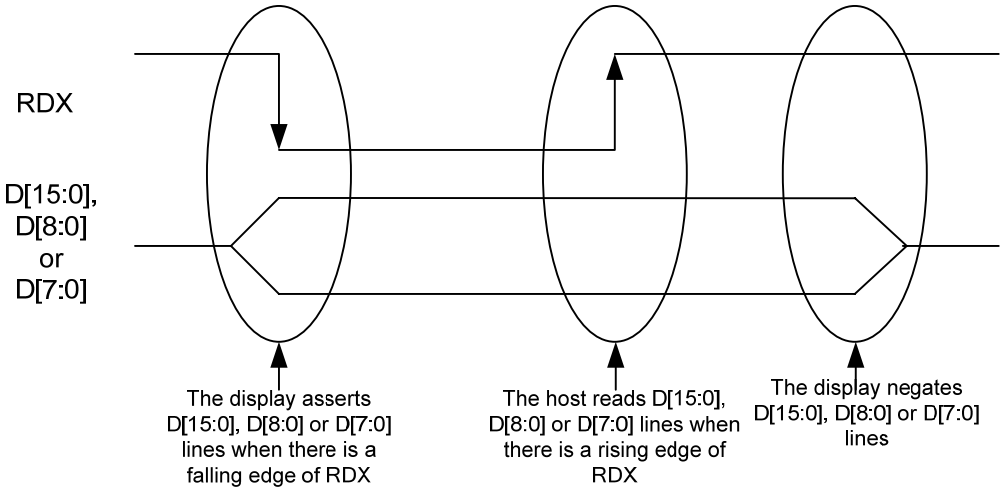


Figure 18 Type B Interface - Read Cycle

Note: RDX is an unsynchronized signal; it can be stopped.

7.2.3 Display Read/Write Sequences

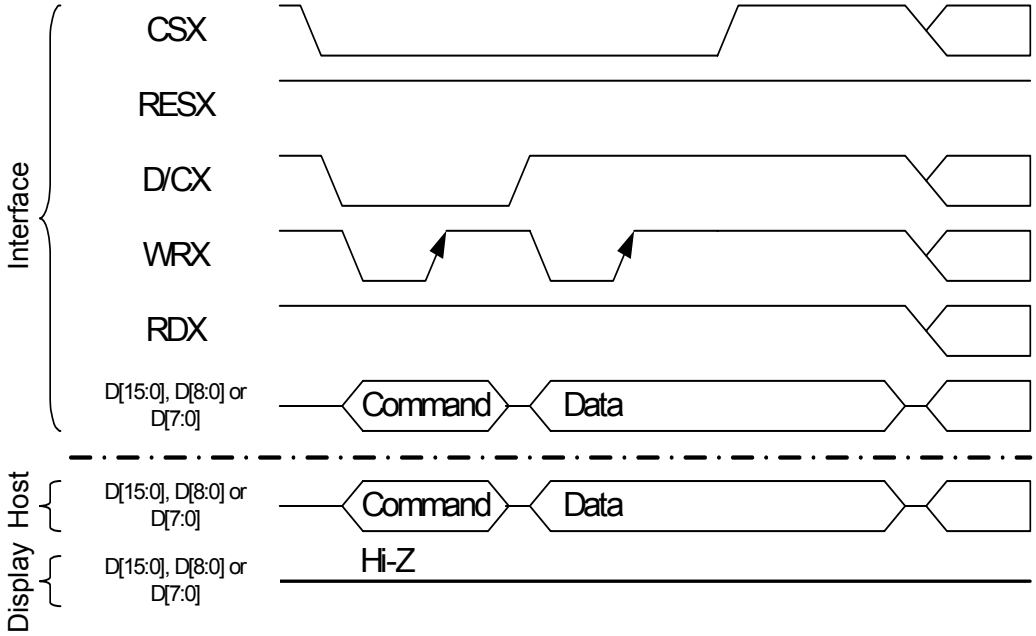


Figure 19 Type B Interface Write Sequence

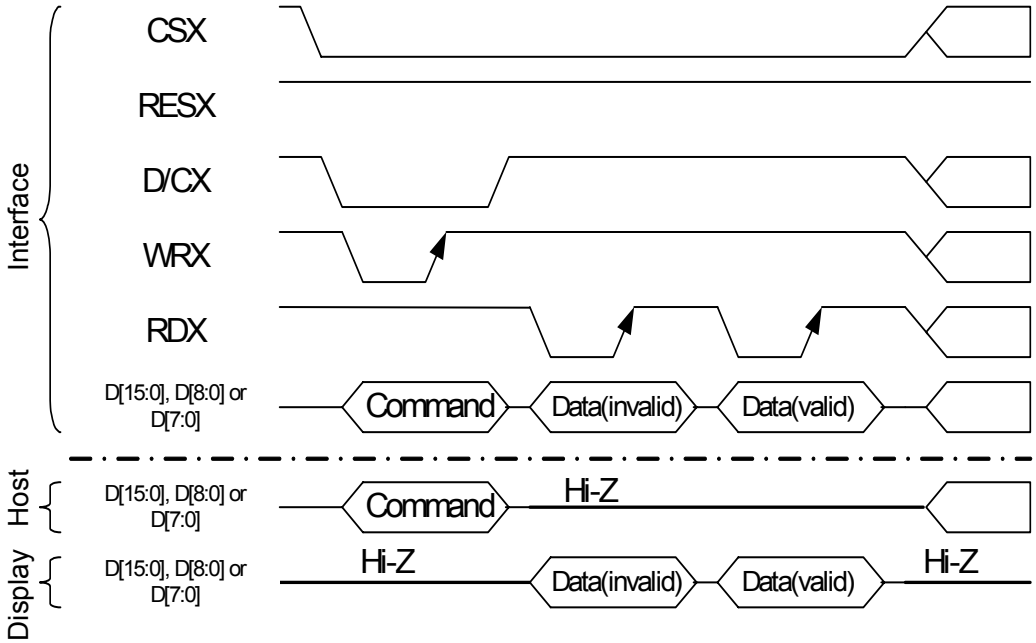


Figure 20 Type B Interface Read Sequence

Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.3 Type C Interface Write and Read Sequences

7.3.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

Figure 21 shows the write cycle for the type C interface.

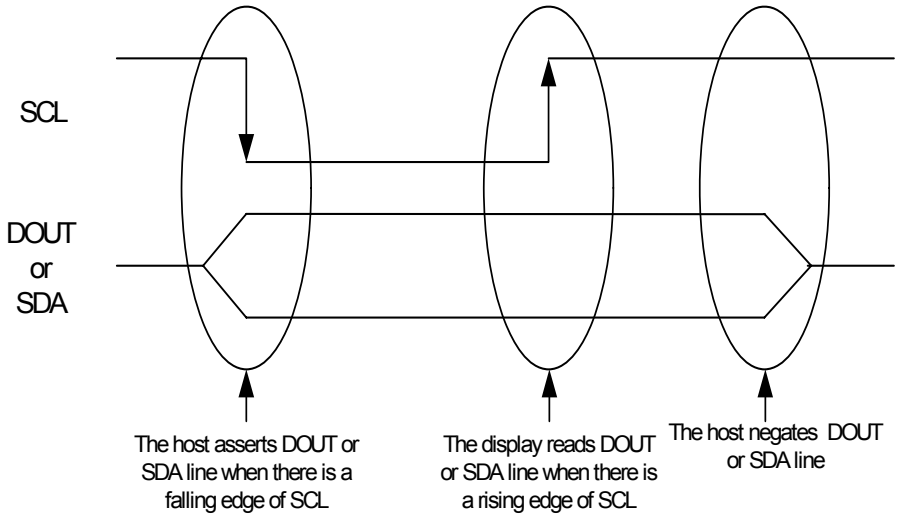
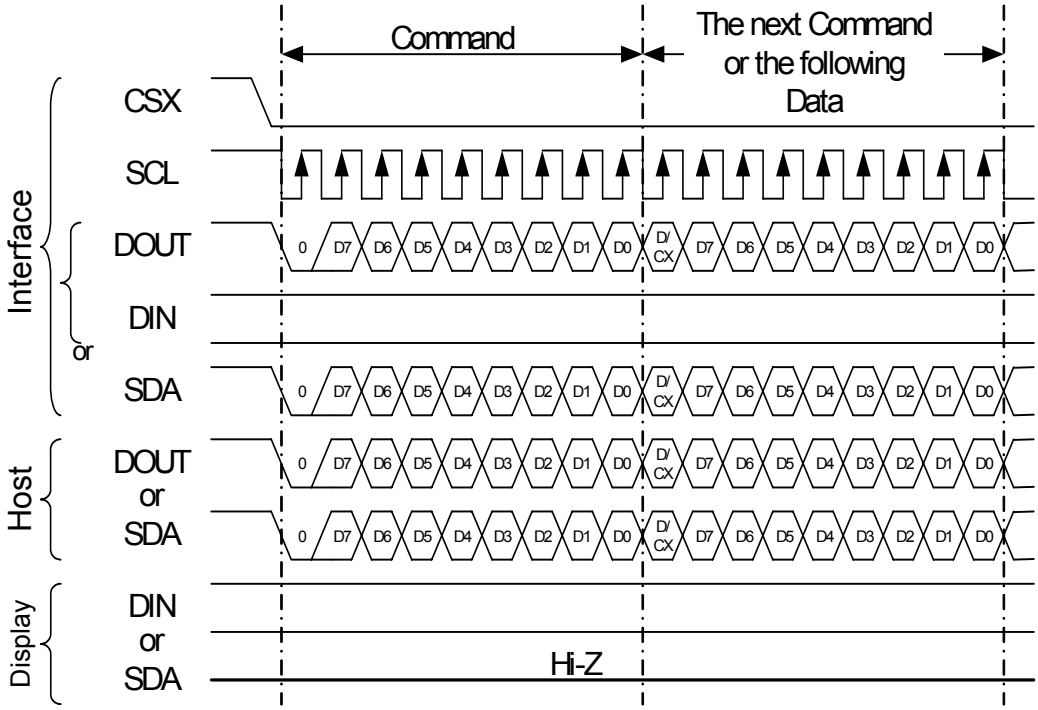


Figure 21 Type C Interface Write Cycle

Note: SCL is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

362 The type C interface write sequences are described in Figure 22, Figure 23 and Figure 24.



363

364 **Figure 22 Type C Interface Write Sequence - Option 1**

365 Note: D7 is MSB and D0 is LSB of byte.

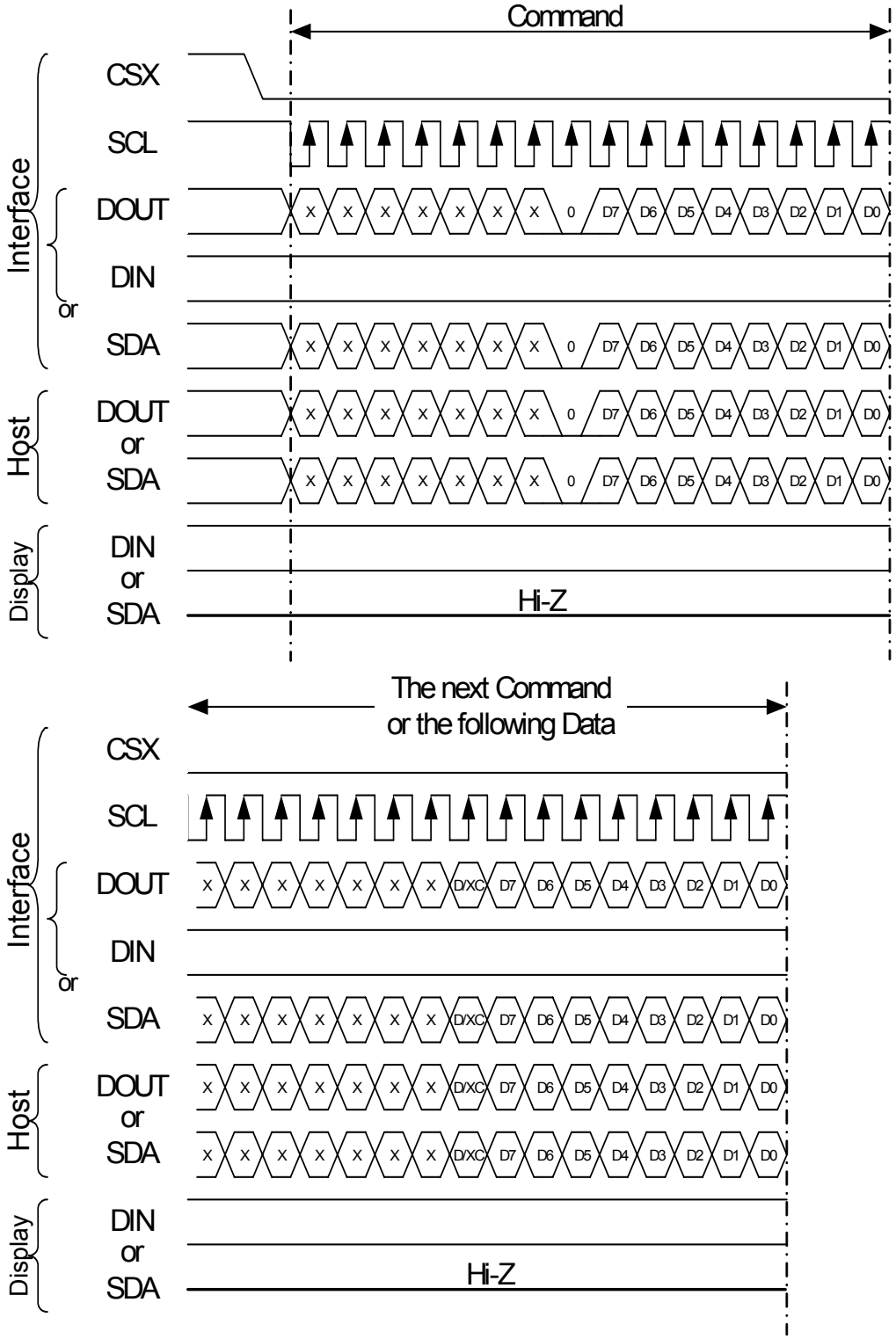


Figure 23 Type C Interface Write Sequence – Option 2

Note: D7 is MSB and D0 is LSB of byte.

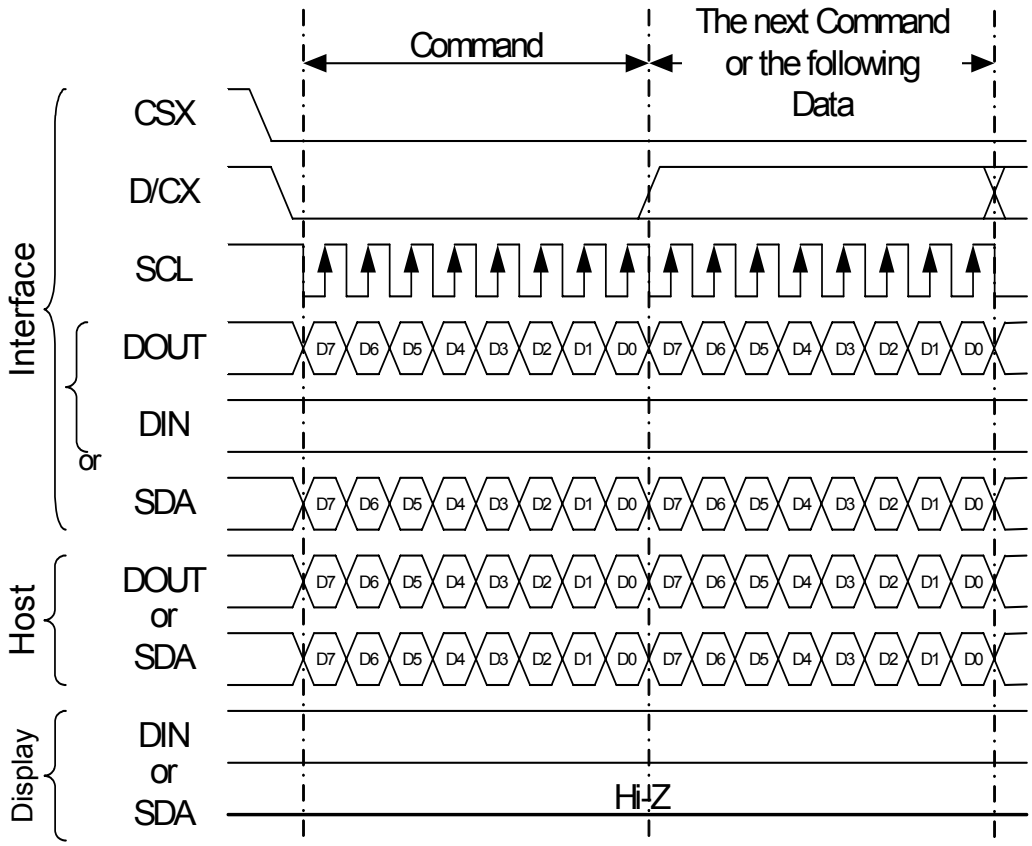


Figure 24 Type C Interface Write Sequence – Option 3

Note: D7 is MSB and D0 is LSB of byte.

7.3.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

Figure 25 shows the read cycle for the type C interface.

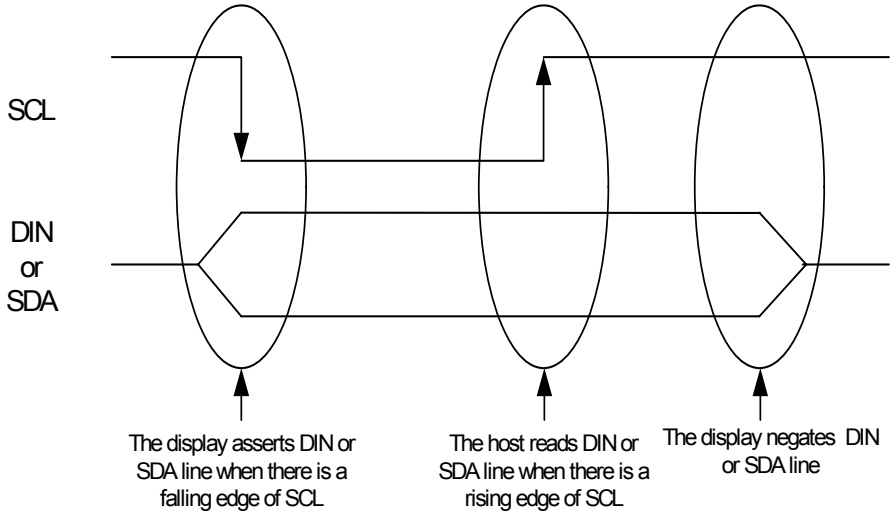


Figure 25 Type C Interface Read Cycle

Note: SCL is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in Figure 26, Figure 27 and Figure 28.

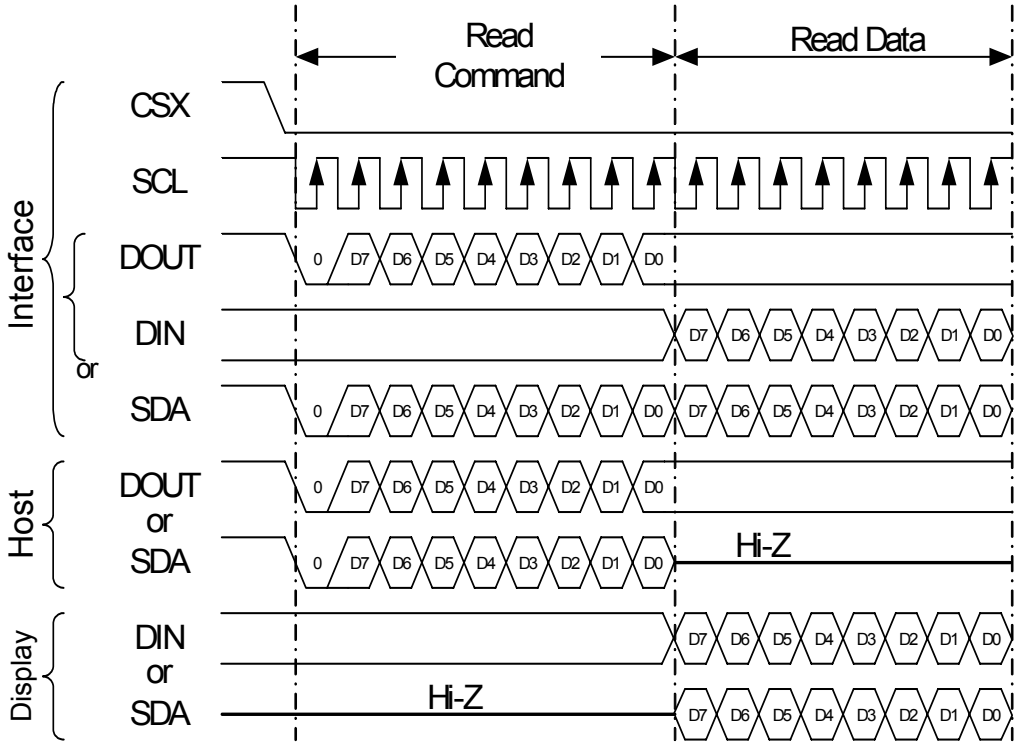


Figure 26 Type C Interface Read Sequence – Option 1

Note: D7 is MSB and D0 is LSB of byte.

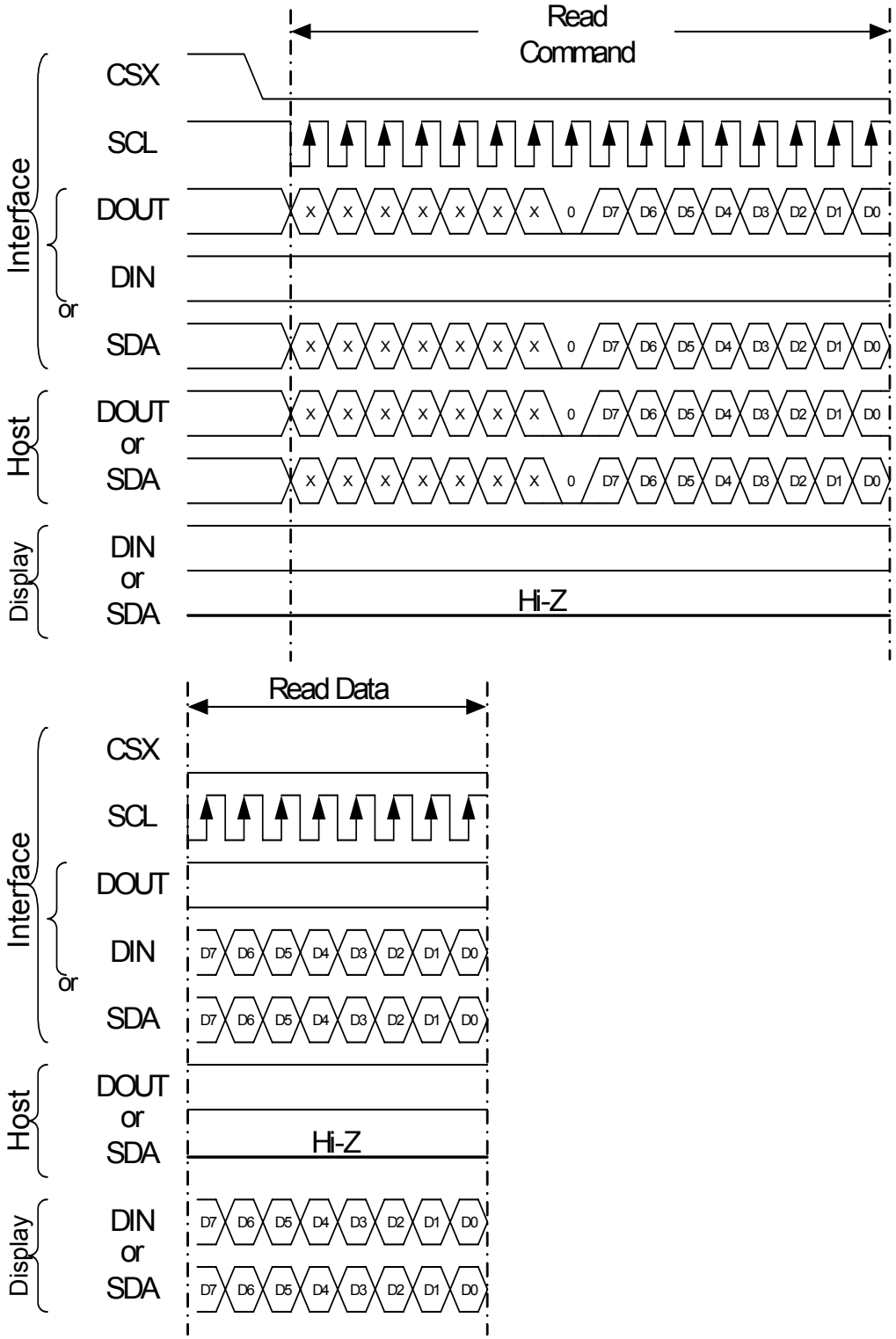


Figure 27 Type C Interface Read Sequence – Option 2

Note: D7 is MSB and D0 is LSB of byte.

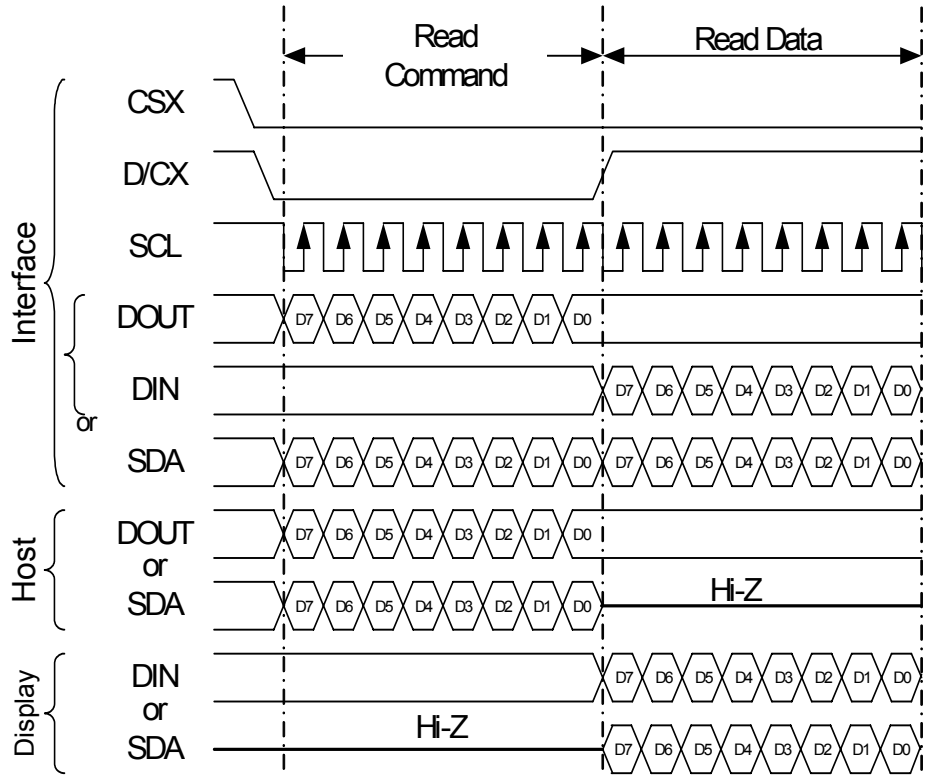


Figure 28 Type C Interface Read Sequence – Option 3

Note: D7 is MSB and D0 is LSB of byte.

7.3.3 Break and Pause of Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

7.4 Tearing Effect

The display module can use the Tearing Effect signal to provide the host processor with internal signal information such as VSYNC as shown in Figure 29 or VSYNC + HSYNC as shown in Figure 30.

Figure 29 Tearing Effect Signal with VSYNC

Figure 30 Tearing Effect Signal with VSYNC + HSYNC

8 Interface Electrical Characteristics

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply	V_{DD}	DOI	V
Logic level supply	V_{DDI}	DOI	V
Logic Signal Input Voltage	V_I	DOI	V
Logic Signal Output Voltage	V_O	DOI	V

8.1.2 DC Characteristics

Table 6 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit
			min	typ	max	
Power Supply Voltage	V_{DD}	Operating Voltage		DOI		V
Logic High level input voltage	V_{IH}		$0.7V_{DDI}$		V_{DDI}	V
Logic Low level input voltage	V_{IL}		0.0		$0.3V_{DDI}$	V
Logic High level output voltage	V_{OH}	I_{OUT} = -1 mA	$0.8V_{DDI}$		V_{DDI}	V
Logic Low level output voltage	V_{OL}	I_{OUT} = +1 mA	0.0		$0.2V_{DDI}$	V
Logic High level input current	I_{IH}	Except D[15:0], D[8:0] or D[7:0]			10	uA
	I_{IHD}	D[15:0], D[8:0]or D[7:0]			10	uA
Logic Low level input current	I_{IL}	Except D[15:0], D[8:0] or D[7:0]	-10			uA
	I_{ILD}	D[15:0], D[8:0] or D[7:0]	-10			uA

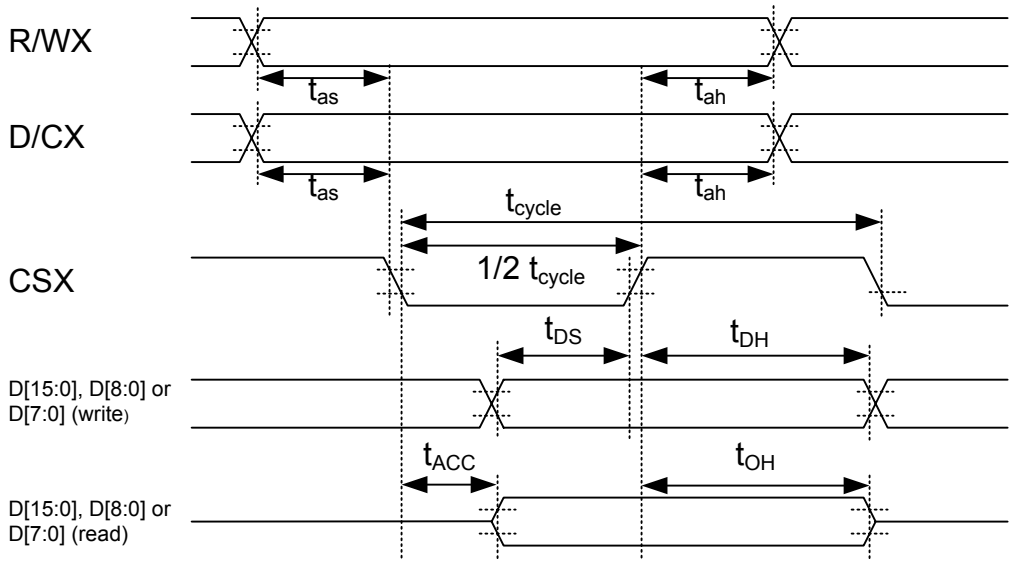
Note: Ta = -30 to 70 °C

418 **Table 7 Logic High level input voltage classification**

Parameter	Symbol	Class	Specification			unit
			min	typ	max	
Logic High level input voltage	V_{DDI}	1	1.1	1.2	1.3	V
		2	1.4	1.5	1.6	V
		3	1.7	1.8	1.9	V
		4	2.6	2.8	3.0	V

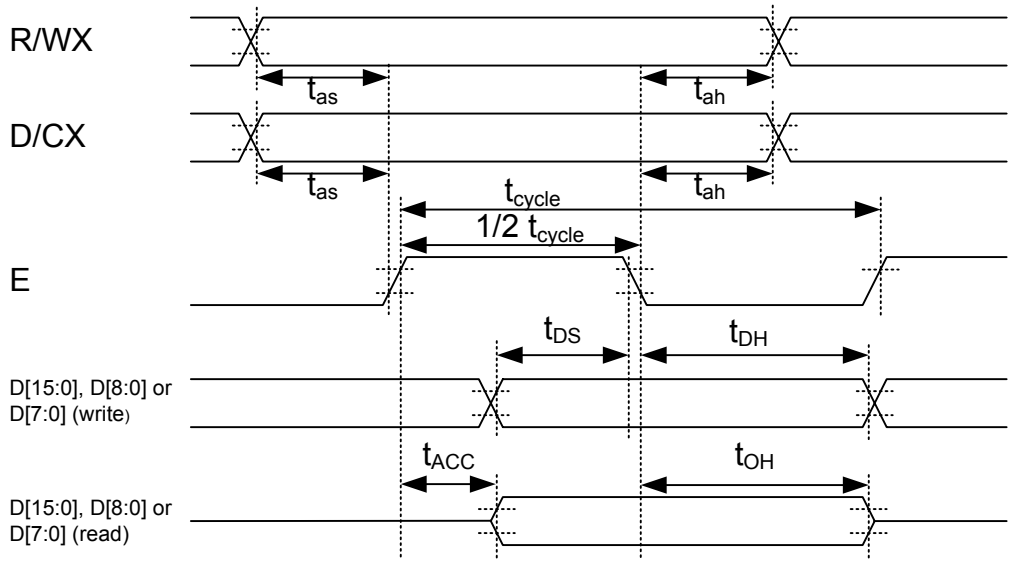
419 Note: Ta = -30 to 70 °C

420 ### 8.1.3 AC Characteristics



421

422 **Figure 31 AC Characteristics, Type A Interface, Fixed E Mode**



423

424 **Figure 32 AC Characteristics, Type A Interface, Clocked E Mode**

425 **Table 8 AC Characteristic -- Type A Interface**

Signal	Symbol	Parameter	min	max	Unit	Description
R/WX or D/CX	t_{as}	Address setup time	T	-	ns	
	t_{ah}	Address hold time (Write/Read)	T	-	ns	
CSX or E	t_{cycle}	System clock cycle time	5xT	79xT	ns	
D[15:0], D[8:0], or D[7:0]	t_{DS}	Data setup time	15	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DH}	Data hold time	25		ns	
	t_{ACC}	Data access time	10		ns	
	t_{OH}	Output hold time	10		ns	

426 Note:

427 1. Ta = -30 to 70 °C, V_{DDI} range: according to Logic High level input voltage classification , GND =
428 0V, T = 10 ± 0.5 ns

429 2. Does not include signal rise and fall times.

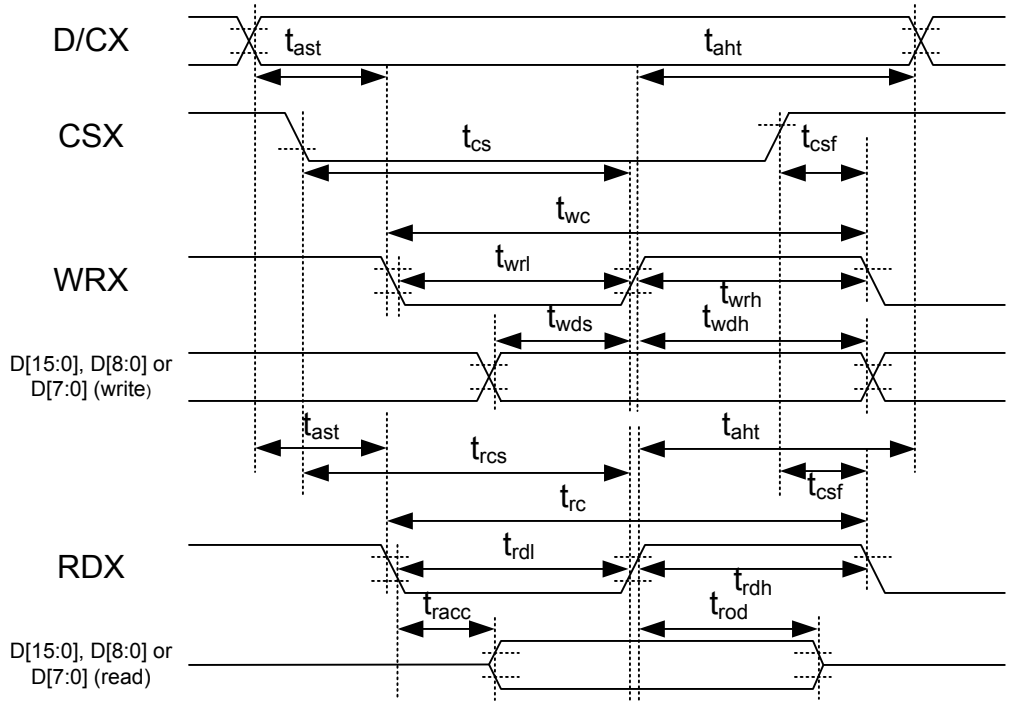


Figure 33 AC Characteristics, Type B Interface

Table 9 AC Characteristics -- Type B Interface

Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	t_{ast}	Address setup time	T	-	ns	
	t_{aht}	Address hold time (Write/Read)	T	-	ns	
CSX	t_{cs}	Chip Select setup time (Write)	2xT	-	ns	(2xT, 3xT, …, 16xT)
	t_{rcs}	Chip Select setup time (Read)	2xT	-	ns	(2xT, 3xT, …, 16xT)
	t_{csf}	Chip Select Wait time (Write/Read)	20	-	ns	
WRX	t_{wc}	Write cycle	5xT	79xT	ns	(5xT, 6xT, …, 79xT)
	t_{wrh}	Write Control pulse H duration	3xT	63xT	ns	(3xT, 6xT, …, 63xT)
	t_{wrl}	Write Control pulse L duration	2xT	16xT	ns	(2xT, 3xT, …, 16xT)
RDX	t_{rc}	Read cycle	5xT	79xT	ns	(5xT, 6xT, …, 79xT)
	t_{rdh}	Read Control pulse H duration	3xT	63xT	ns	(3xT, 6xT, …, 63xT)
	t_{rdl}	Read Control pulse L duration	2xT	16xT	ns	(2xT, 3xT, …, 16xT)
D[15:0], D[8:0], or D[7:0]	t_{wds}	Write data setup time	15	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{wdh}	Write data hold time	25	-	ns	
	t_{racc}	Read access time	10	-	ns	
	t_{rod}	Read output disable time	10	-	ns	

Note:

1. Ta = -30 to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND = 0V, T = 10 ± 0.5 ns
2. Does not include signal rise and fall times.

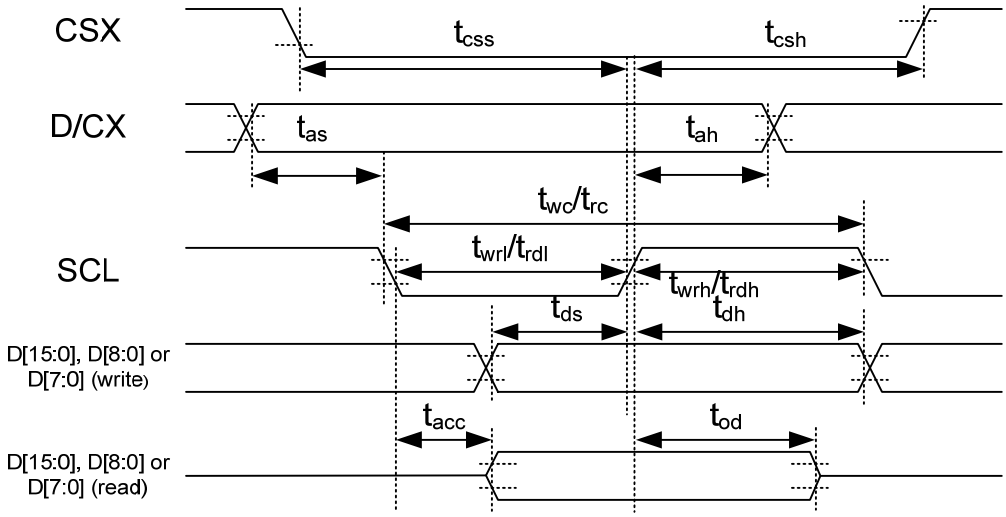


Figure 34 AC Characteristics, Type C Interface

Table 10 AC Characteristics -- Type C Interface

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip Select setup time (Write)	4xT	-	ns	
	tcsh	Chip Select setup time (Read)	4xT	-	ns	
D/CX (optional)	tas	Address setup time	T	-	ns	
	tah	Address hold time (Write/Read)	T	-	ns	
SCL(write)	twc	Write cycle	10xT	-	ns	
	twrh	SCL H duration (write)	4xT	-	ns	
	twrl	SCL L duration (write)	4xT	-	ns	
SCL(read)	trc	Read cycle	15xT	-	ns	
	trdh	SCL H duration (read)	6xT	-	ns	
	trdl	SCL L duration (read)	6xT	-	ns	
DOUT or SDA(write)	tds	Data setup time	3xT	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	tdh	Data hold time	3xT	-	ns	
DIN or SDA(read)	tacc	Access time	10		ns	
	tod	Output disable time	T	5xT	ns	

Note:

1. Ta = -30 to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND = 0V, T = 10 ± 0.5 ns
2. Does not include signal rise and fall times

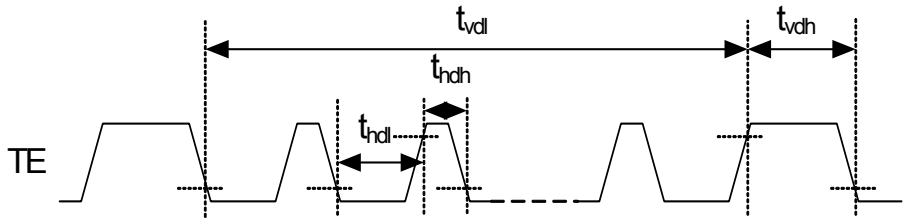


Figure 35 TE Timings

Table 11 Example TE Timing Values

Symbol	Parameter	min	max	Unit	Description
t_{vdl}	Vertical Timing Low Duration	DOI	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	µs	
t_{hdl}	Horizontal Timing Low Duration	DOI	-	µs	
t_{hdh}	Horizontal Timing High Duration	24	500	µs	

Note: Ta = -30 to 70 °C, V_{DDI} range: according to Logic High level input voltage classification, GND = 0V

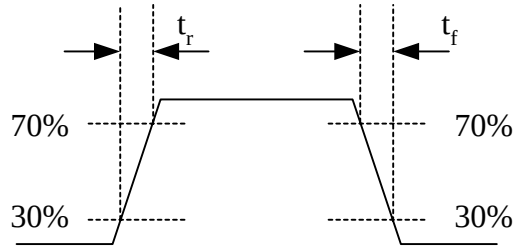


Figure 36 Signal Rise and Fall Times, Host to Display Module (tr ≤ 15 ns, tf ≤ 15 ns)

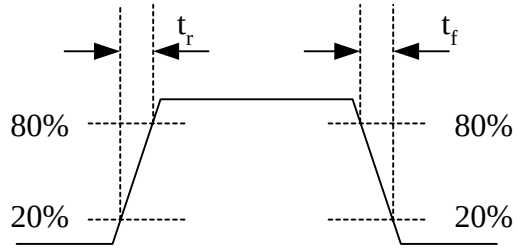


Figure 37 Signal Rise and Fall Times, Display Module to Host (tr ≤ 15 ns, tf ≤ 15 ns)

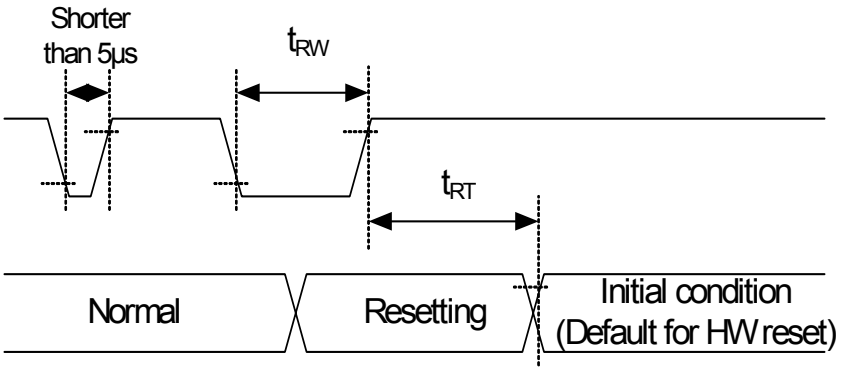


Figure 38 Example Reset Timings

Table 12 Example Reset Timing Values

Signal	Symbol	Parameter	Min	Max	Unit
RESX	t_{RW}	Reset pulse duration	10		µs
	t_{RT}	Reset cancel		5	ms

Notes:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to Table 13.
2. Spike Rejection also applies during a valid reset pulse as shown below:

Table 13 RESX Pulse Conditions

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

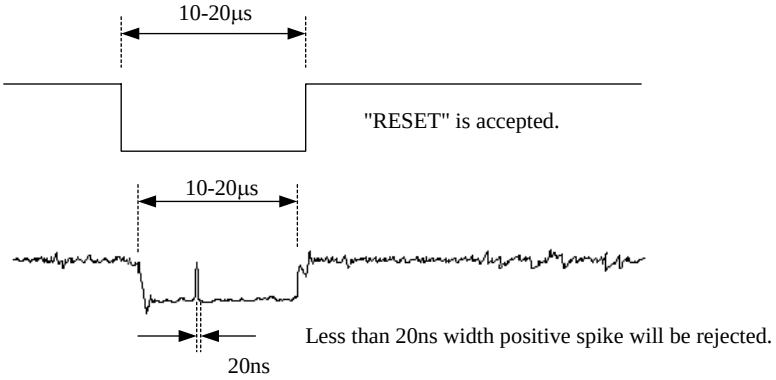


Figure 39 RESX Input Spike Rejection

9 Reset

9.1 Host Input/Output Pins

9.1.1 Input Pins, I/O Pins

Table 14 Host Input and I/O Pin Status Corresponding to Reset and Power On/Off Process

Signal Line	During Display Power-on Process	After Powered On	After Hardware Reset	During Display Module Power Off Process
TE Line	Input Invalid	Input Valid	Input Valid	Input Invalid
D[15:0], D[8:0], D[7:0], SDA (input) or DIN	Input Invalid	Input Valid	Input Valid	Input Invalid

9.1.2 Output Pins

Table 15 Host Output Pin Status Corresponding to Reset and Power On/Off Process

Signal Line	During Display Power-on Process	After Powered On	After Hardware Reset	During Display Module Power Off Process
RESX	Low	High	High	Low
CSX	High	High	High	High
D/CX	High or Low	High or Low	High or Low	High or Low
R/WX	High or Low	High or Low	High or Low	High or Low
E	High or Low	High or Low	High or Low	High or Low
WRX	High or Low	High	High	High
RDX	High	High	High	High
SCL	High or Low	High	High	High
D[15:0], D[8:0], D[7:0], SDA (output) or DOUT	High-Z (Inactive) or Low	High-Z (Inactive) or Low	High-Z (Inactive) or Low	High-Z (Inactive) or Low

9.2 Display Input/Output Pins

9.2.1 Output Pins, I/O Pins

Table 16 Display Output and I/O pin Status After Reset and Power On/Off Process

Signal Line	After Powered On	After Hardware Reset
TE Line	Low	Low
D[15:0], D[8:0], D[7:0], SDA (output) or DIN	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D[15:0] or D[7:0] during Power On/Off sequences and Hardware Reset.

9.2.2 Input Pins

Table 17 Display Input Pin Status Corresponding to Reset and Power On/Off Process

Signal Line	During Display Power On Process	After Powered On	After Hardware Reset	During Display Power Off Process
RESX	DOI	Input valid	Input valid	DOI
CSX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
R/WX	Input invalid	Input valid	Input valid	Input invalid
E	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input invalid
D[15:0], D[8:0], D[7:0], SDA (input) or DOUT	Input invalid	Input valid	Input valid	Input invalid

10 Interface Color Coding

Color coding uses a red [R], green [G] and blue [B] additive color mixing method. R, G and B are used for each color data index in the following sections.

10.1 Serial Interface

10.1.1 3-bits/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option1

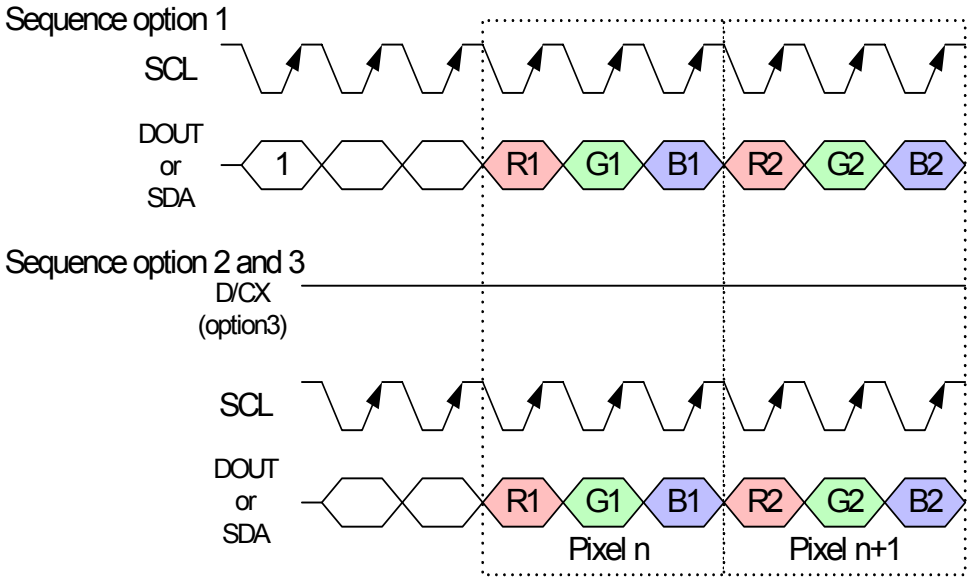


Figure 40 3-bits/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option 1

10.1.2 3-bit/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors – Option 2

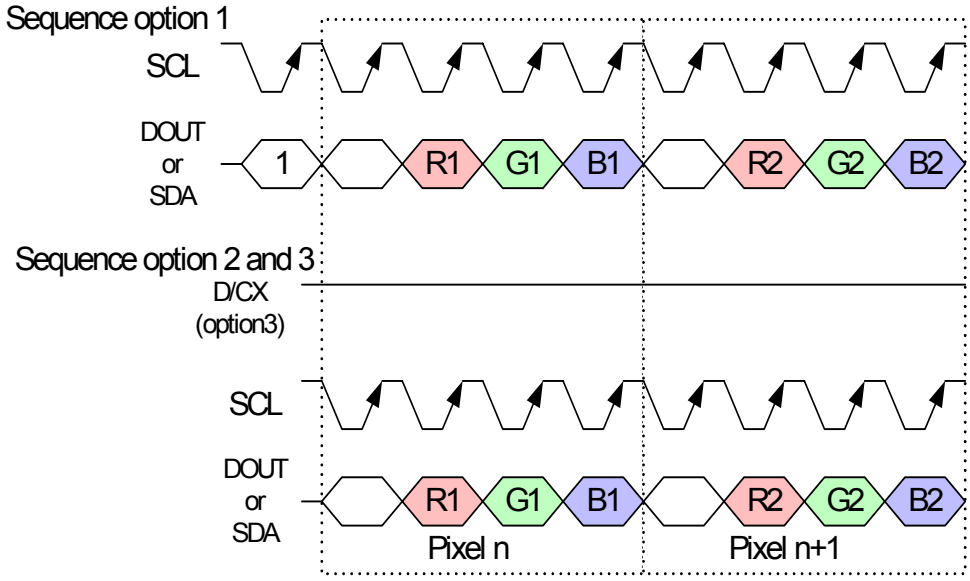


Figure 41 3-bit/pixel (R 1-bit, G 1-bit, B 1-bit), Eight Colors - Option 2

10.2 8-bit Interface

10.2.1 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

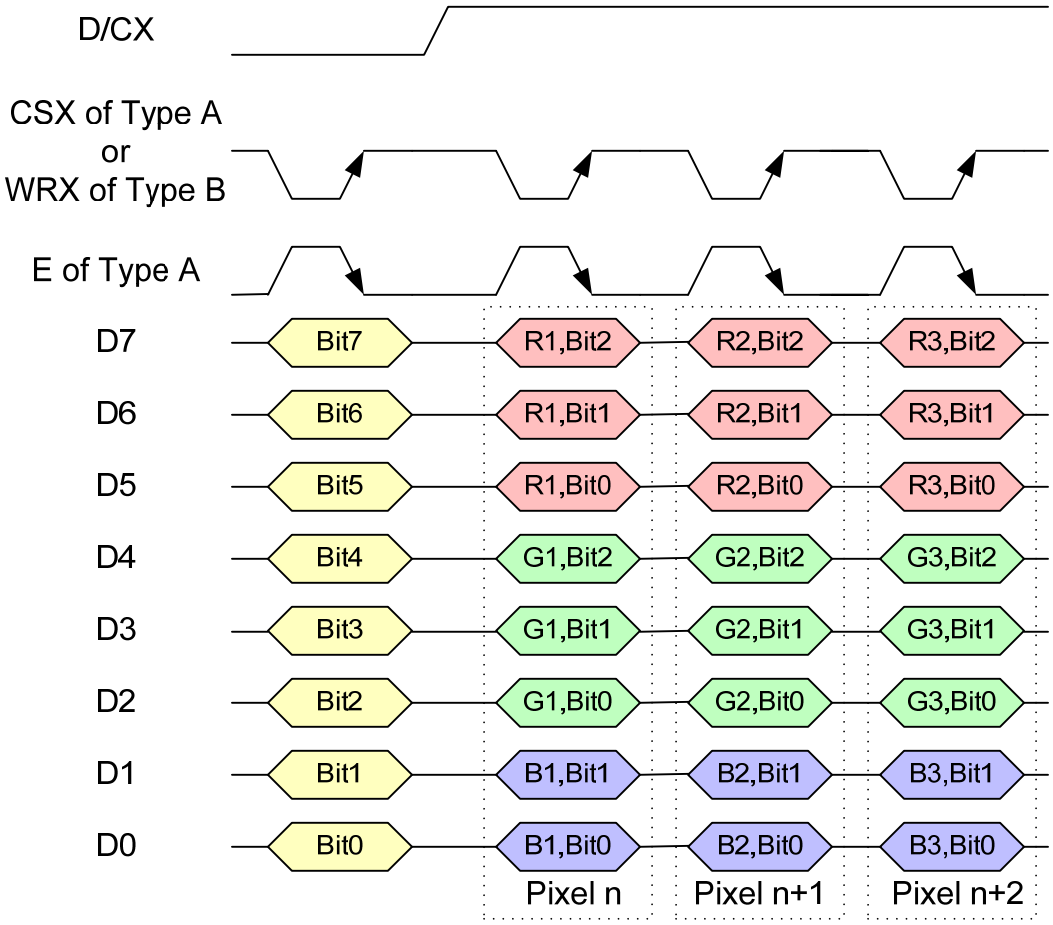


Figure 42 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit2, LSB = Bit0 for Red and Green data, MSB = Bit1, LSB = Bit0 for Blue data.

10.2.2 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

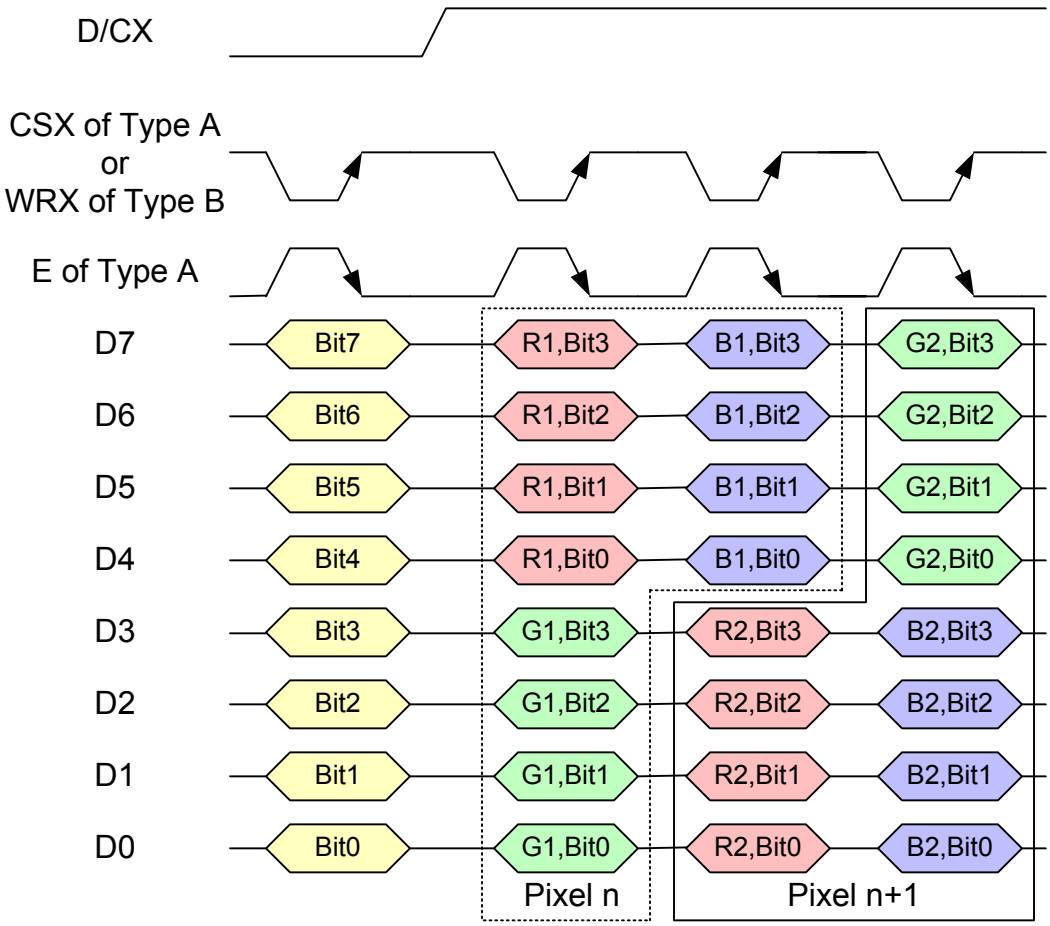


Figure 43 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit3, LSB = Bit0 for Red, Green, and Blue data.

10.2.3 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

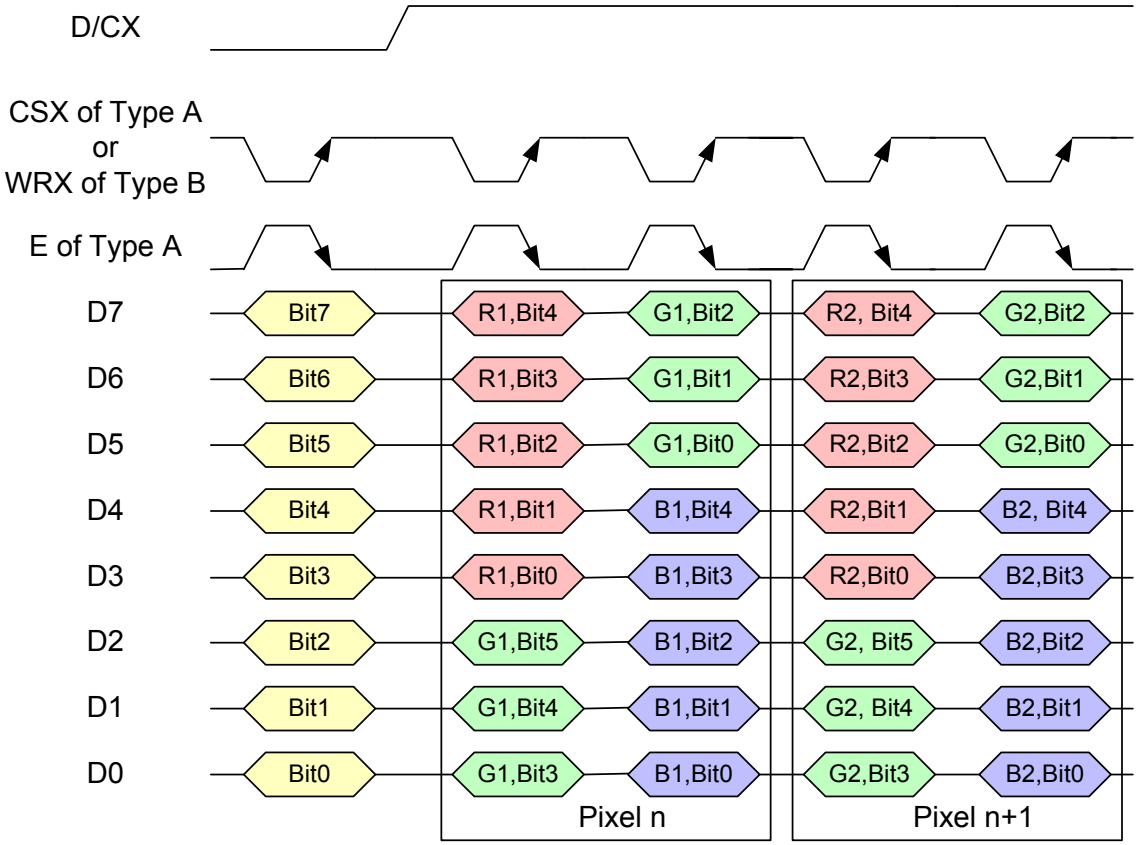


Figure 44 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for Green data, MSB = Bit4, LSB = Bit0 for Red and Blue data.

10.2.4 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

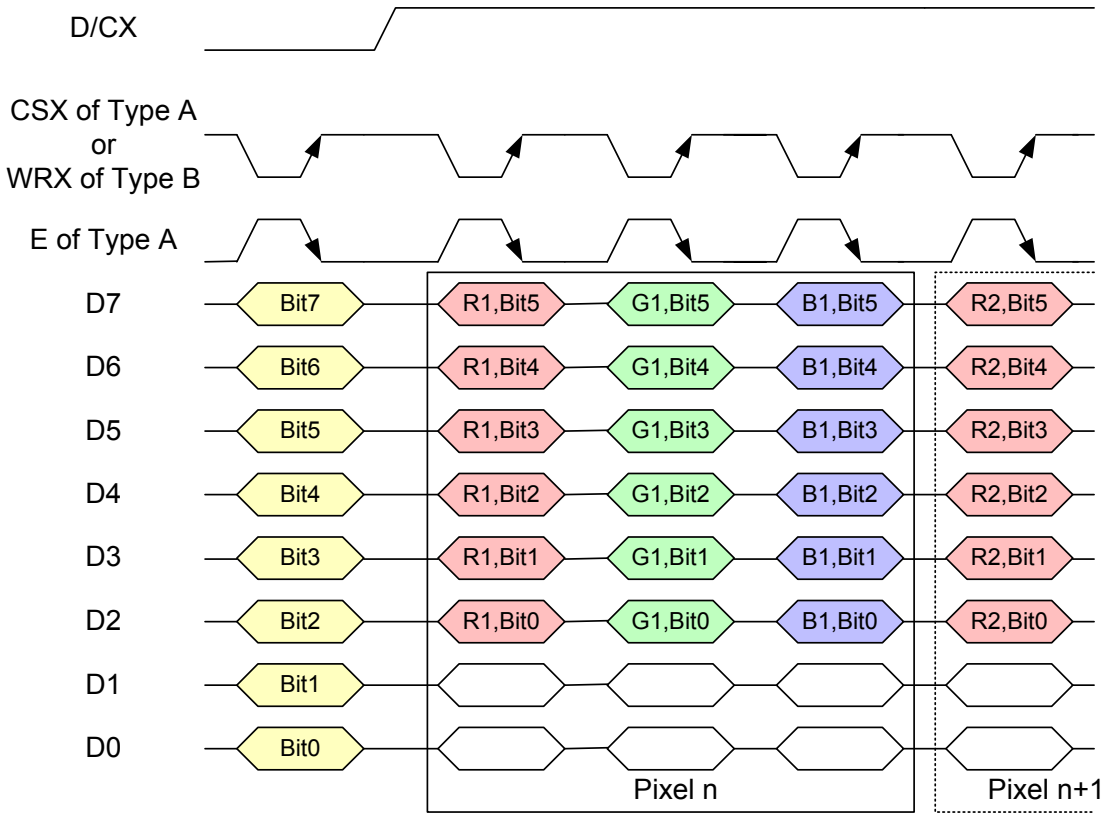


Figure 45 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

10.2.5 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

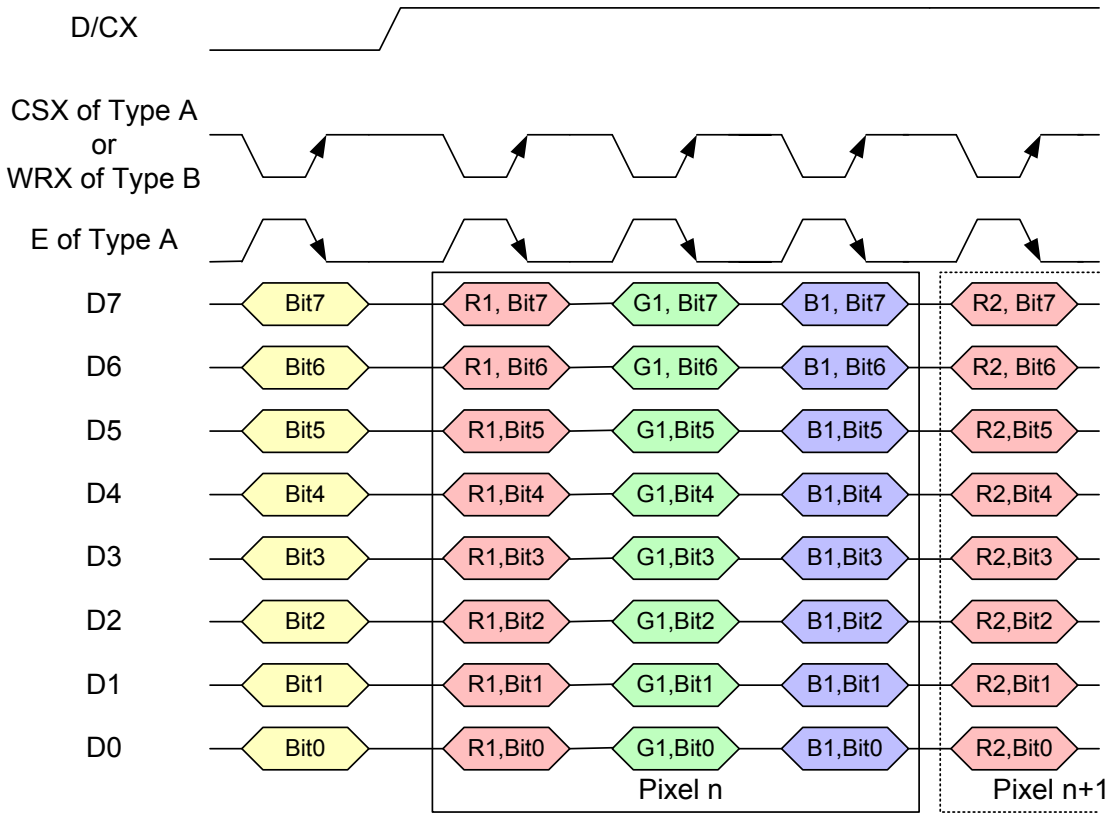


Figure 46 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

Note: The Data order is as follows, MSB = D7, LSB = D0. Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green, and Blue data.

10.3 9-bit interface

10.3.1 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

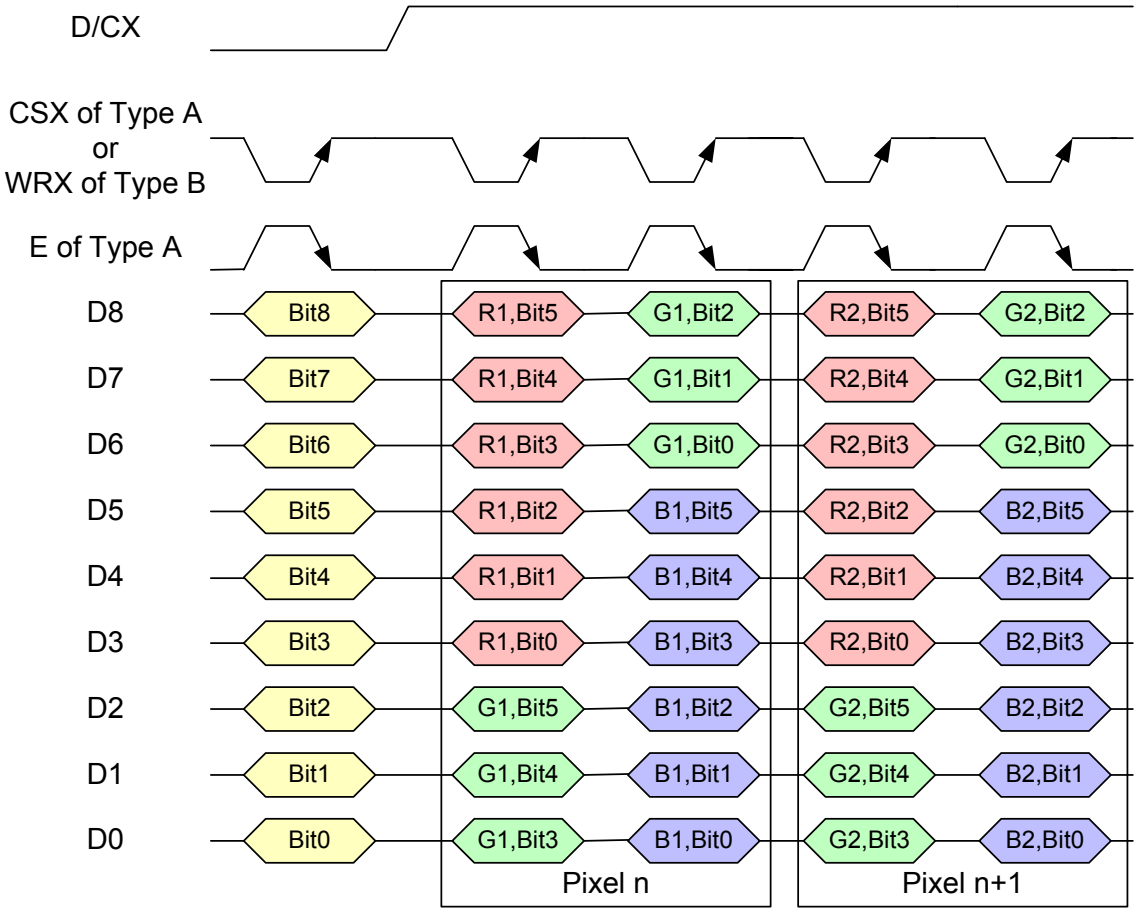


Figure 47 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

Note: The Data order is as follows, MSB = D8, LSB = D0. Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

10.4 16-bit Interface

10.4.1 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

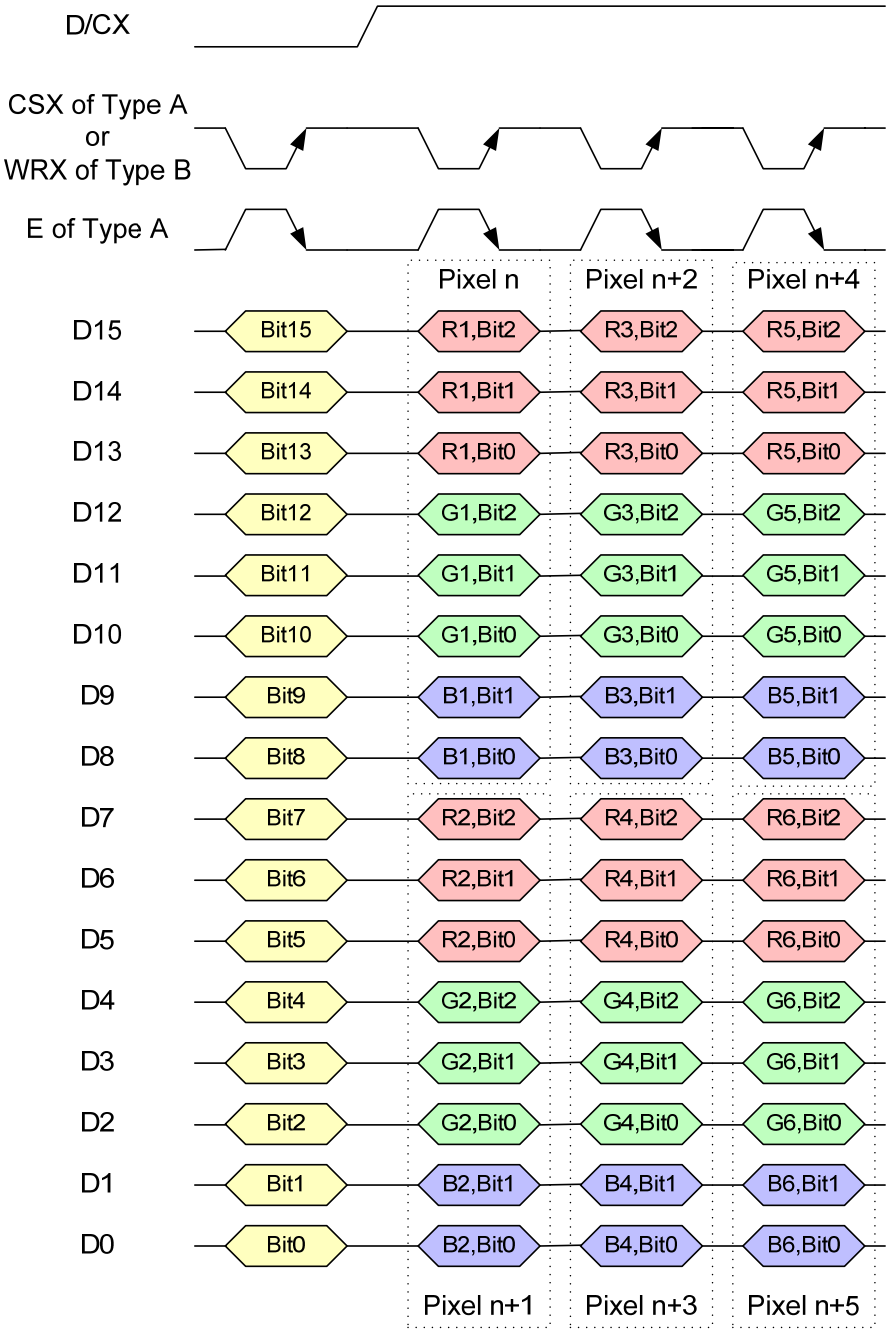


Figure 48 8-bits/pixel (R 3-bit, G 3-bit, B 2-bit), 256 Colors

Note: The Data order is as follows: MSB = D15, LSB = D0 and image data is MSB = Bit2, LSB = Bit0 for Red and Green data, and MSB = Bit1, LSB = Bit0 for Blue data.

10.4.2 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

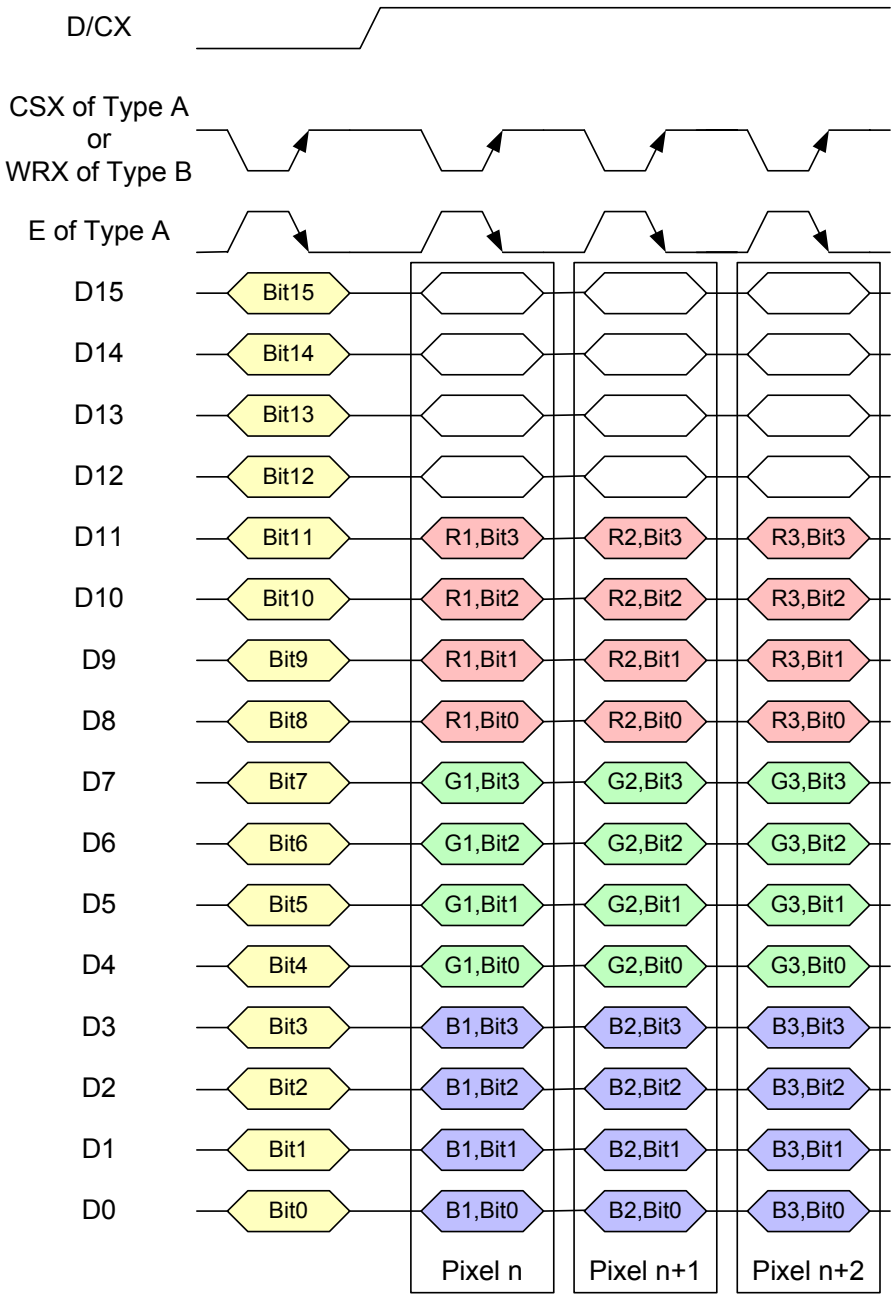


Figure 49 12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit3, LSB = Bit0 for Red, Green, and Blue data.

10.4.3 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

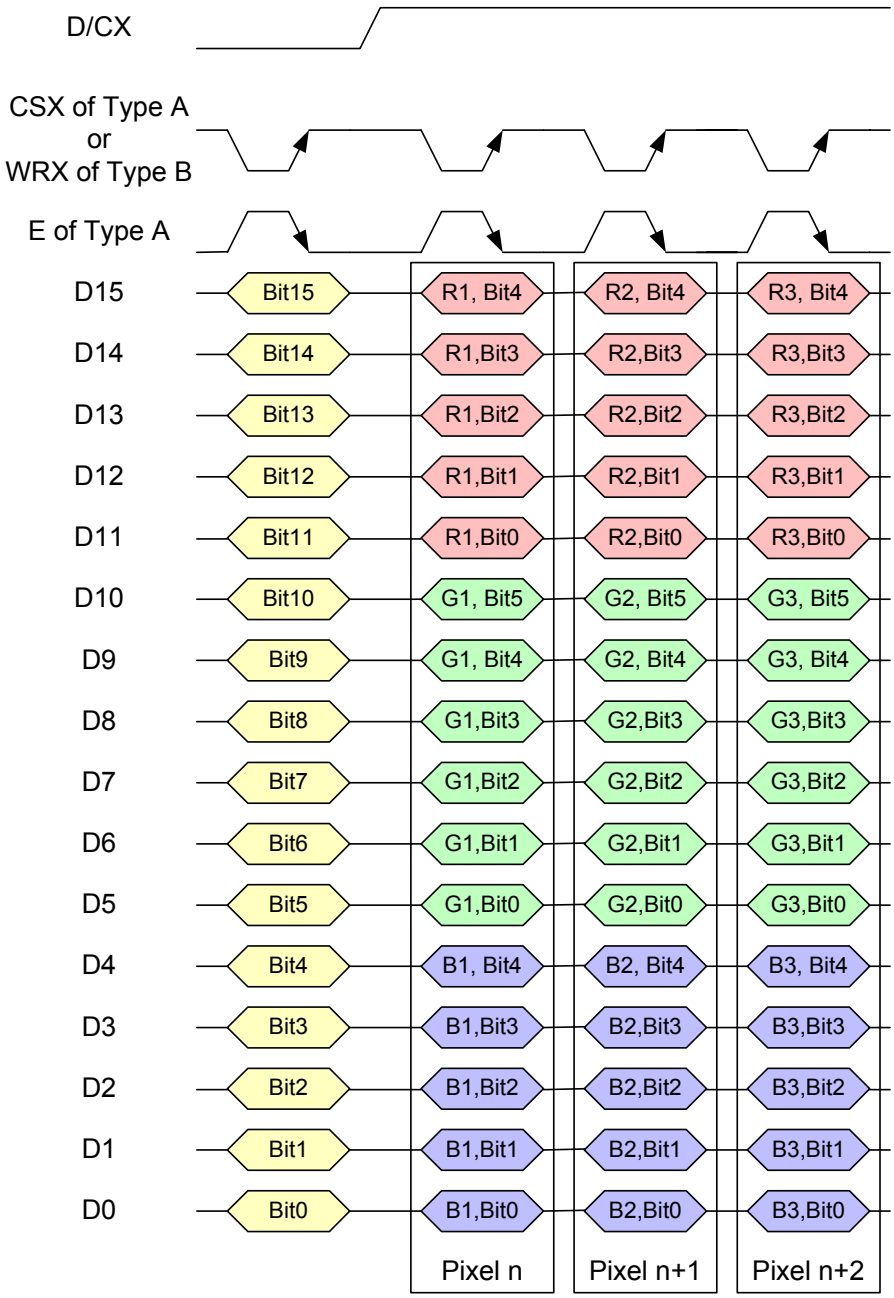


Figure 50 16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

10.4.4 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors - Option 1

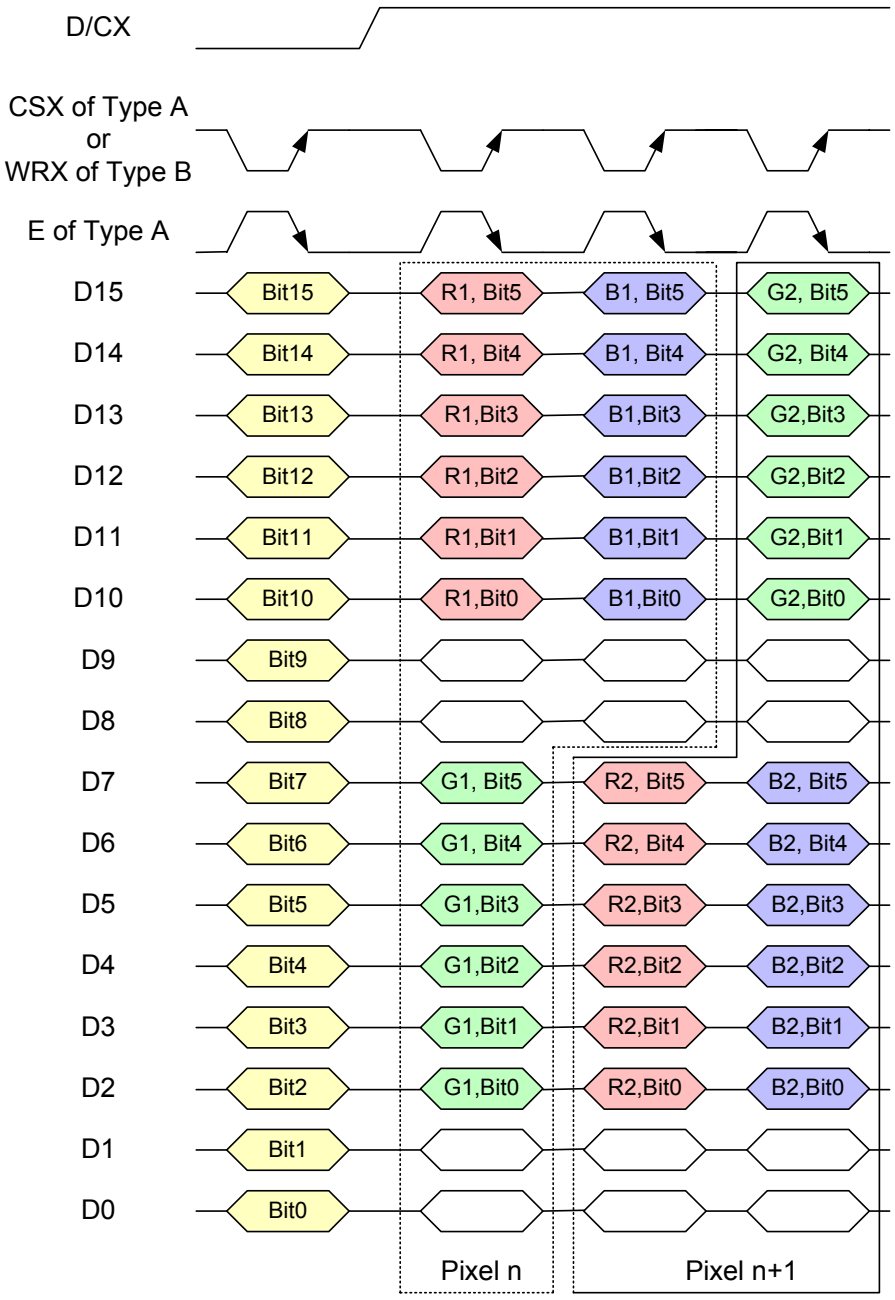


Figure 51 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

10.4.5 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors - Option 2

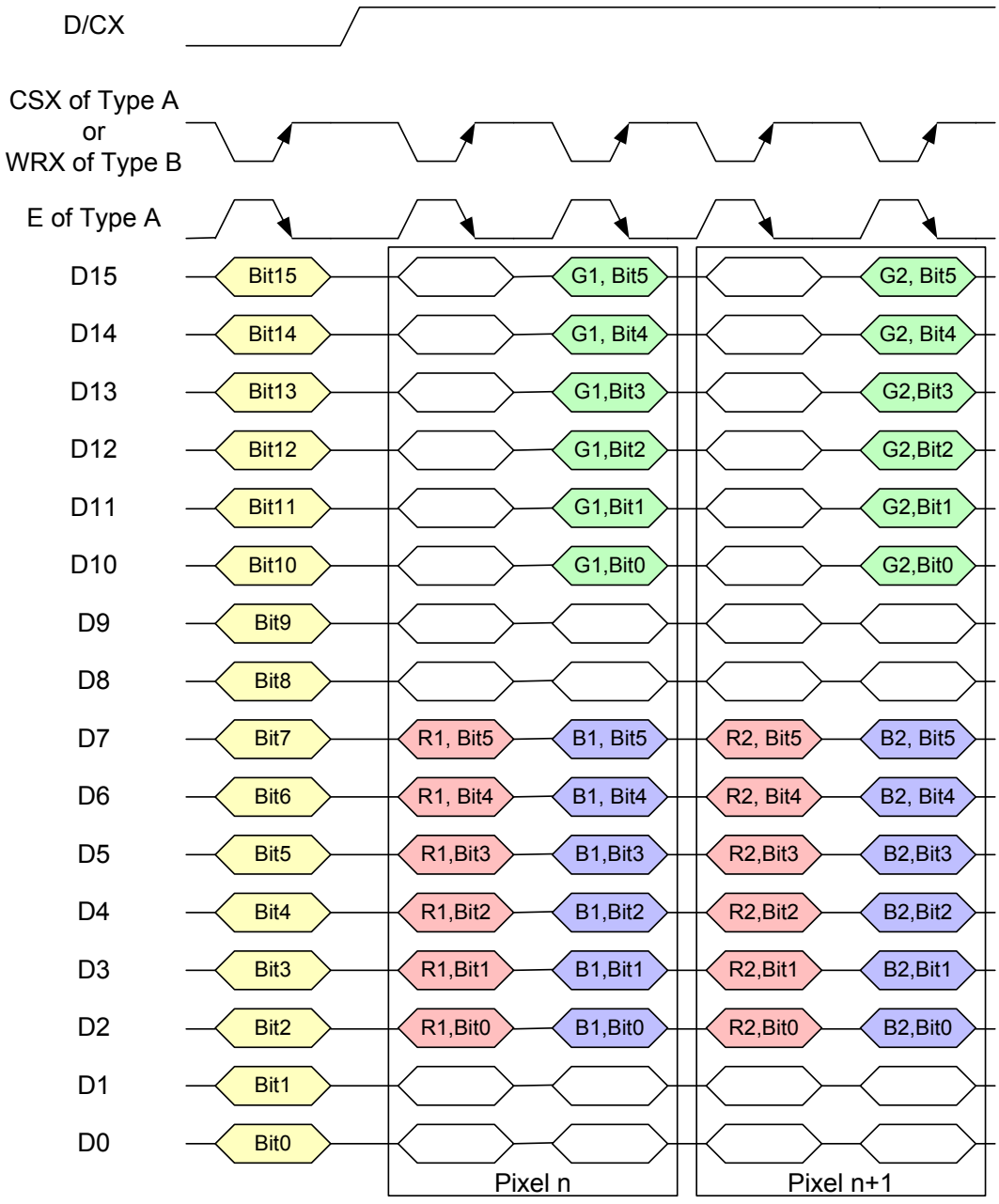


Figure 52 18-bits/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit5, LSB = Bit0 for Red, Green, and Blue data.

10.4.6 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors - Option 1

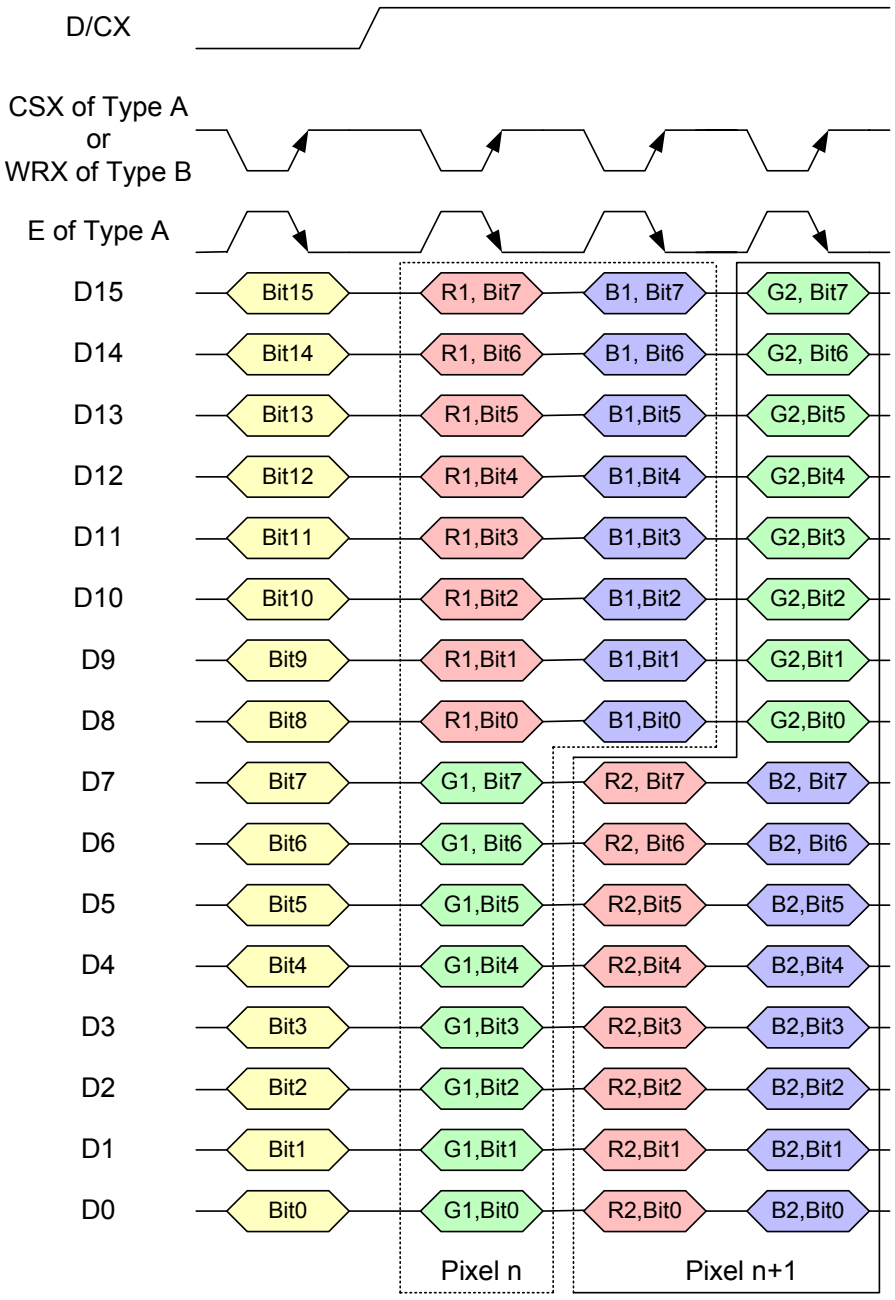


Figure 53 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit7, LSB = Bit0 for Red, Green, and Blue data.

10.4.7 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors - Option 2

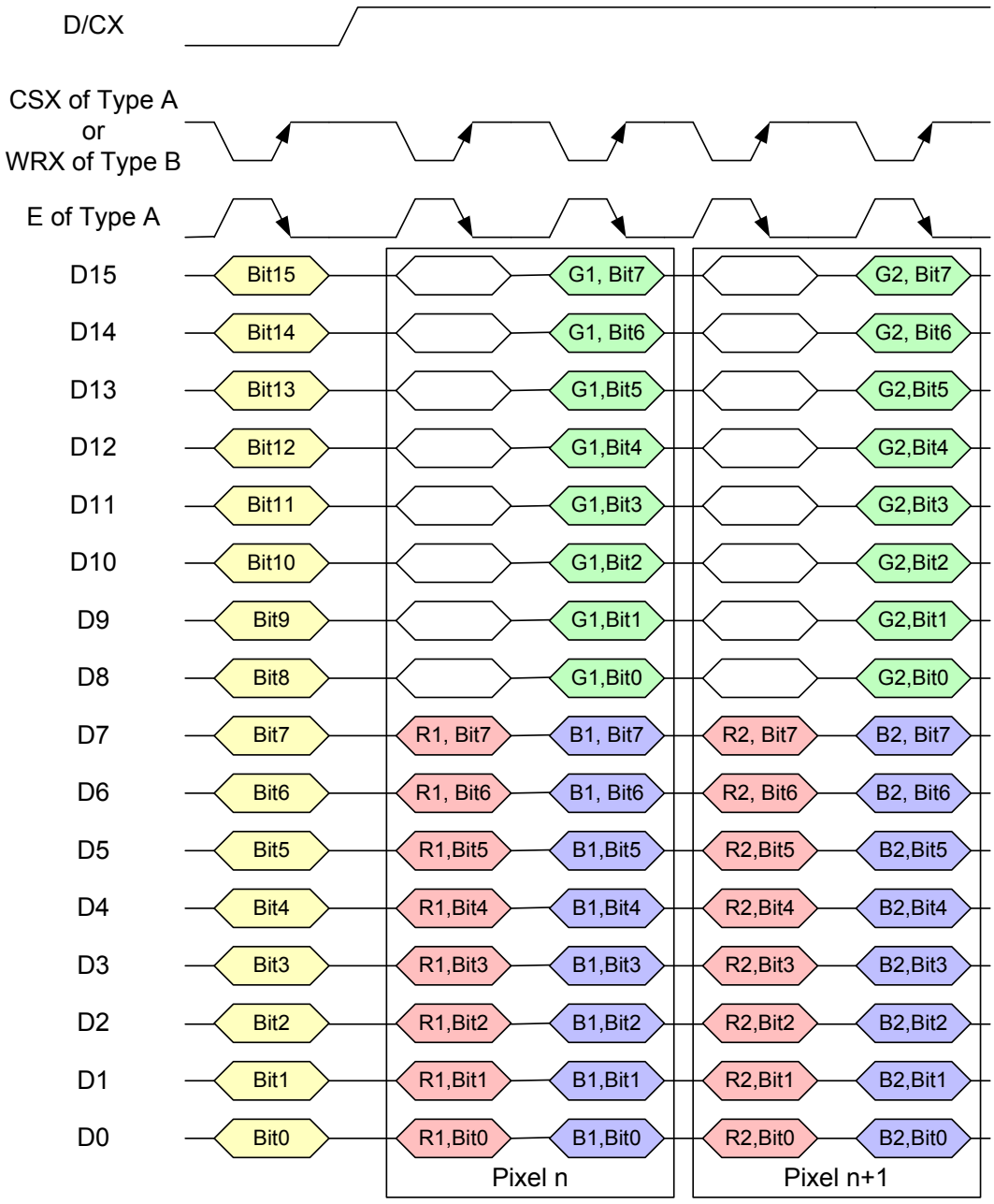


Figure 54 24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

Note: The Data order is as follows, MSB = D15, LSB = D0 and image data is MSB = Bit7, LSB = Bit0 for red, Green, and Blue data.

11 Command Set

See the *MIPI Alliance Standard for Display Command Set* for a description of the commands in order to control the display module through DBI.

12 Interoperability, and Optional Capabilities

This section describes interoperability requirements between different host processors and displays in DBI application. There are a number of categories of potential differences or attributes that must be considered to ensure interoperability between a host processor and a display module in DBI usage.

1. DBI implementation Types A, B and C

Each host processor and display module shall implement one or more of Type A, B or C interfaces.

2. TE support in Type A implementations

Each host processor or display module may support TE when the Type A interface is implemented.

3. Type C option 1, 2 and 3 as specified in section 4.

Each host processor and display module shall implement one or more options of Option 1, 2 and 3 when it implements a type C interface.

4. Logic High level input voltage classification

Each host processor and display module shall support one or more voltage classification of Class 1, 2, 3 or 4.

5. Interface color coding

Each host processor shall support one or more color coding scheme of 8-, 12-, 16-, 18- or 24-bits per pixel when a Type 1 architecture is implemented.

Each display module shall support one or more color coding scheme of 8-, 12-, 16-, 18- or 24-bits per pixel, up to its native number of colors, when a Type 1 architecture is implemented.

Each host processor and display module shall support 3-bits per pixel when a Type 2 or 3 architecture is implemented.

6. Bus width option Type A and Type B

Each host processor and display module shall support one or more bus width options of 8-, 9- and 16-bits.