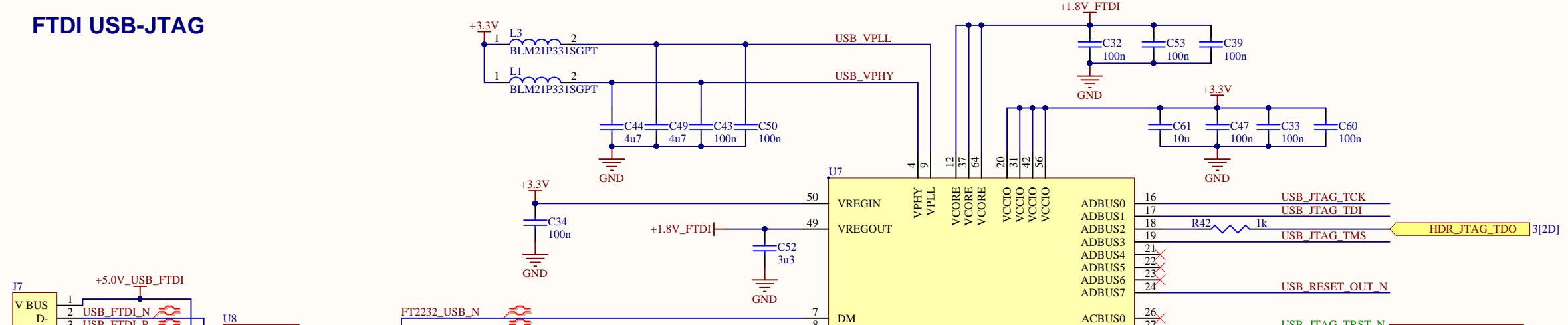
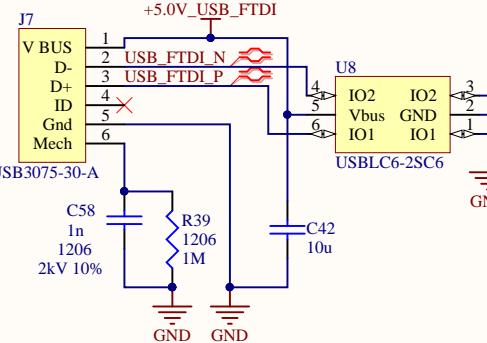


FTDI USB-JTAG

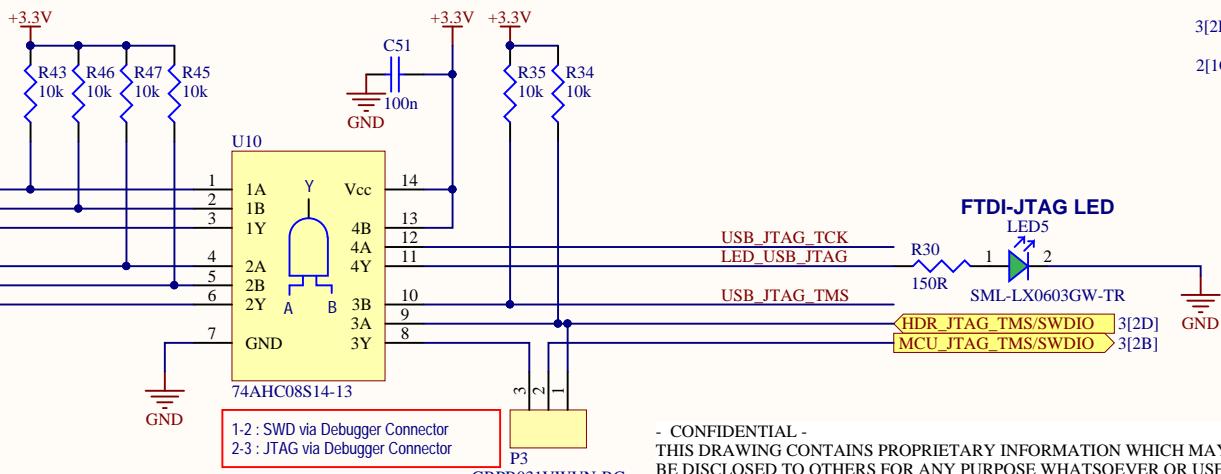
A



B



C



- CONFIDENTIAL -
THIS DRAWING CONTAINS PROPRIETARY INFORMATION WHICH MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE WHATSOEVER OR USED FOR MANUFACTURING PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM THE FUTURE ELECTRONICS CORPORATION.

D



Future Electronics - System Design Center NA
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

Project Name
FCS-Murata-Cypress Dev kit Rev 0

Title
FTDI

Size **B** Dwg No. **FEN-413458-SCH-R0** Rev **0**

Checked by **H.Letourneau** Approved by **M. Bernier**

Date **3/3/2017** Sheet **1** of **4** Variant: **[No Variations]**

Designed by **M. Bernier** Drawn by **M. Bernier**
Checked by **H.Letourneau** Approved by **M. Bernier**
Date **3/3/2017** Sheet **1** of **4** Variant: **[No Variations]**

E

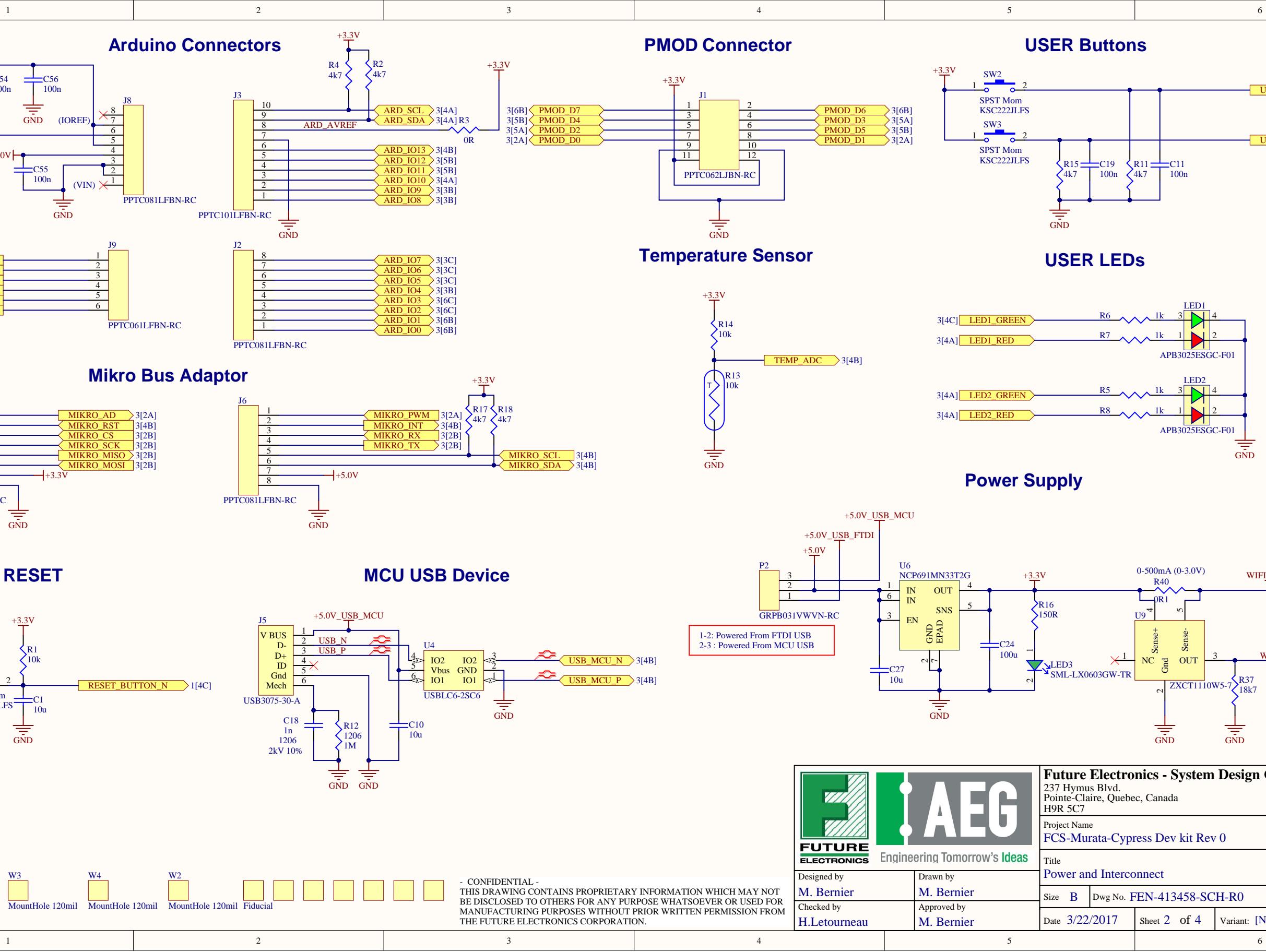
A

B

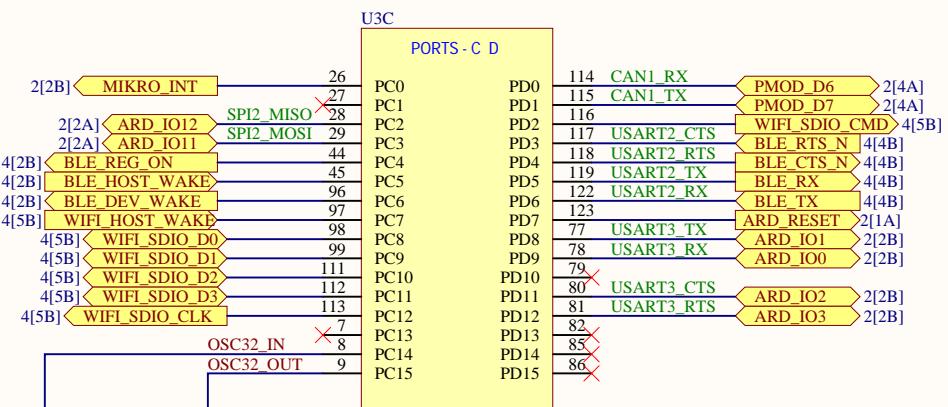
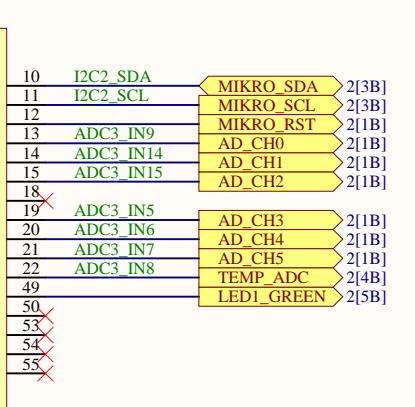
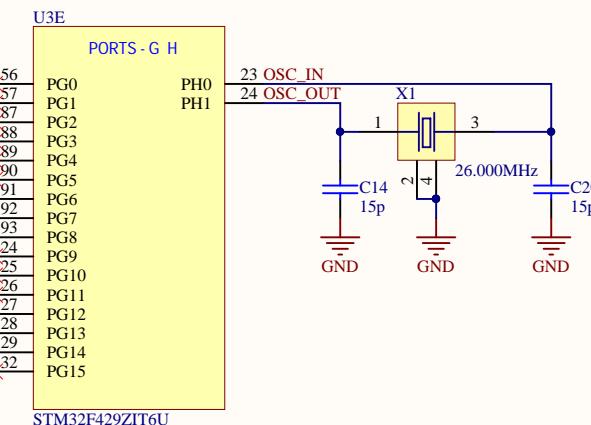
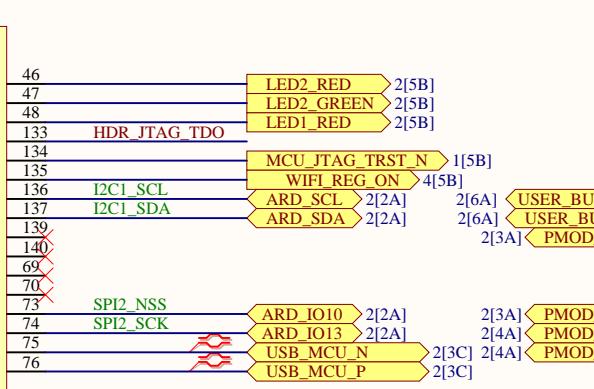
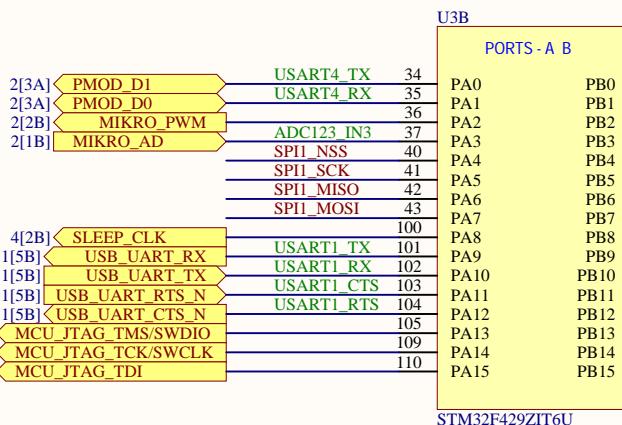
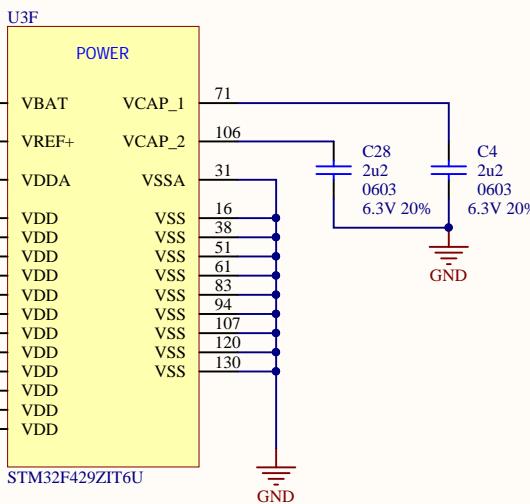
C

D

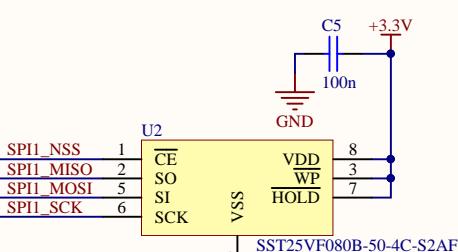
E



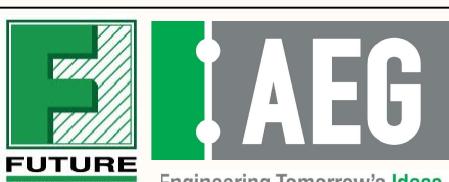
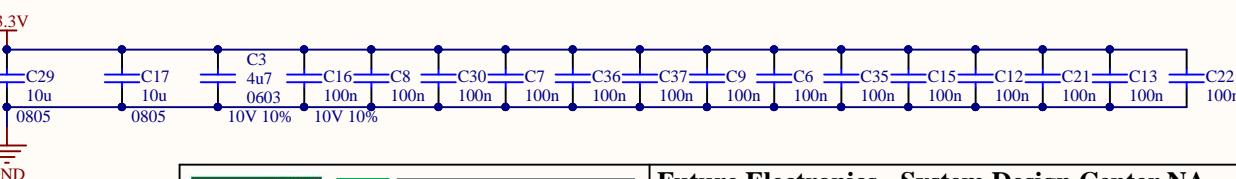
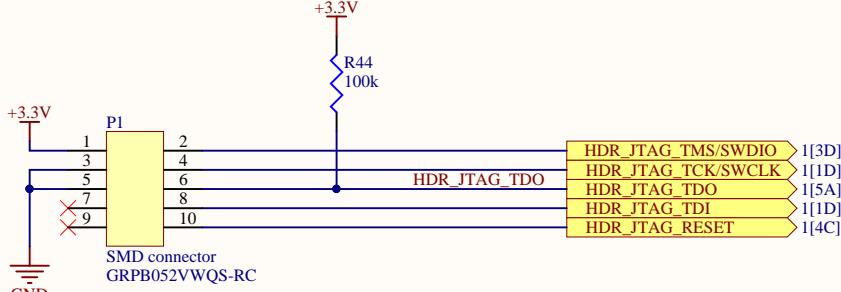
STM32F429ZIT6



Serial Flash 8Mbit



Cortex-M Debug Connector (SWD)



- CONFIDENTIAL -
THIS DRAWING CONTAINS PROPRIETARY INFORMATION WHICH MAY NOT
BE DISCLOSED TO OTHERS FOR ANY PURPOSE WHATSOEVER OR USED FOR
MANUFACTURING PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM
THE FUTURE ELECTRONICS CORPORATION.

Future Electronics - System Design Center NA
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
J3T 5C9

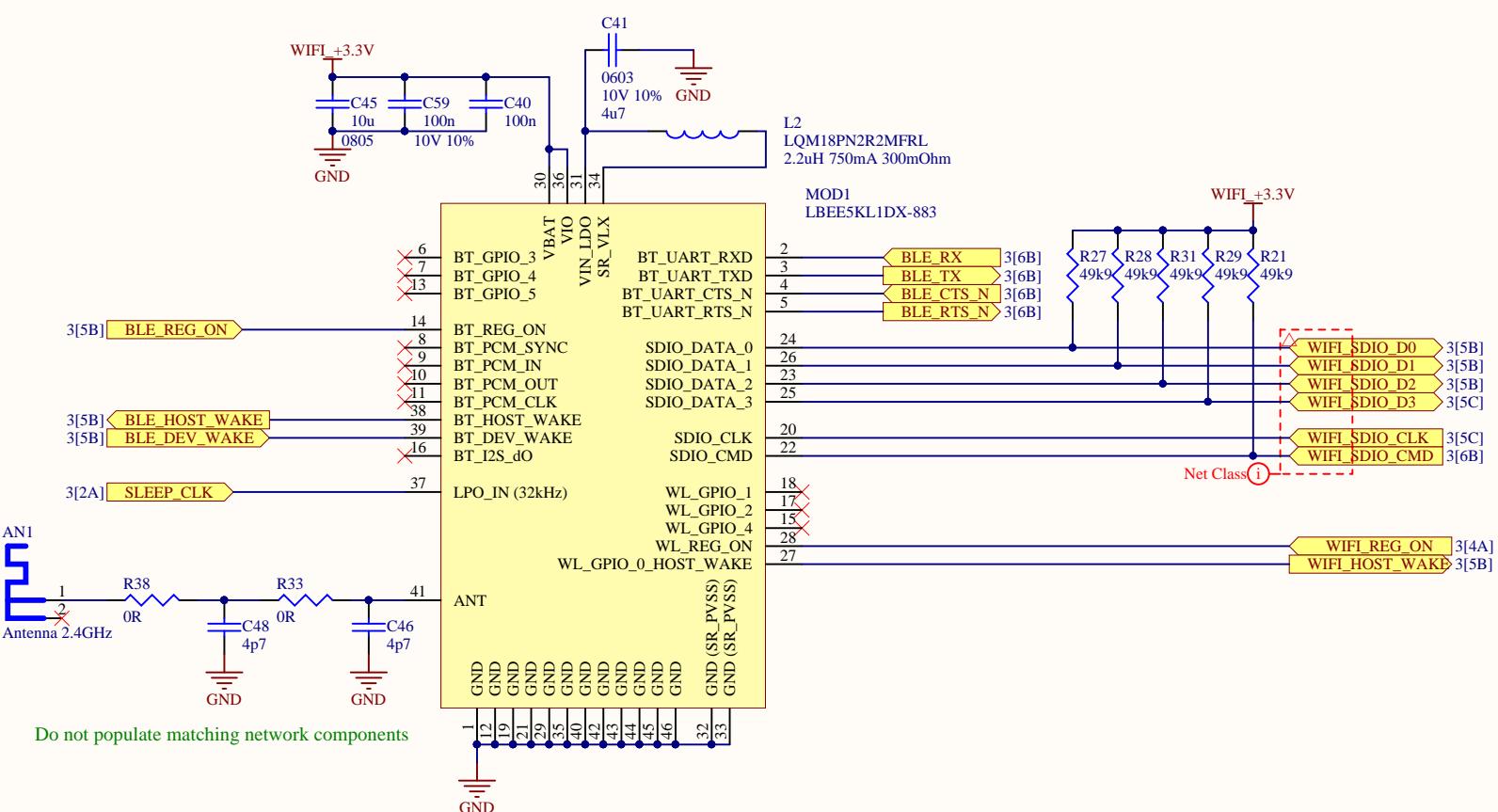
Project Name
ECS_Murata_Cypress_Dev_kit Rev 0

Title

Microcontroller

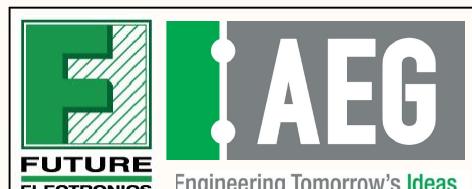
Date 3/3/2017 Sheet 3 of 4 Variant: [No Variations]

WiFi and Bluetooth Module



CONFIDENTIAL

- CONFIDENTIAL -
THIS DRAWING CONTAINS PROPRIETARY INFORMATION WHICH MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE WHATSOEVER OR USED FOR MANUFACTURING PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM THE FUTURE ELECTRONICS CORPORATION.



Future Electronics - System Design Center NA
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

Project Name
FCS-Murata-Cypress Dev kit Rev 0

Title

WIFI

Size B Dwg No. FEN-413458-SCH-R0 Rev

Date 3/22/2017 Sheet 4 of 4 Variant: [No Variations]

1	2	3	4	5	6	7	8																																																																								
Layers	Top Layer																																																																														
Impedance Requirements																																																																															
<table border="1"> <thead> <tr> <th rowspan="2">Layer</th><th colspan="2">Impedance 50 Ohms</th><th colspan="2">Impedance 90 Ohms (Diff)</th><th colspan="2">Impedance 100 Ohms (Diff)</th></tr> <tr> <th>Trace Width (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th><th></th></tr> </thead> <tbody> <tr> <td>Top Layer</td><td>10 mils</td><td>8 mils</td><td>9 mils</td><td></td><td></td><td></td></tr> <tr> <td></td><td>10 mils</td><td>8 mils</td><td>9 mils</td><td></td><td></td><td></td></tr> </tbody> </table>								Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)		Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)		Top Layer	10 mils	8 mils	9 mils					10 mils	8 mils	9 mils																																																
Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)																																																																										
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)																																																																										
Top Layer	10 mils	8 mils	9 mils																																																																												
	10 mils	8 mils	9 mils																																																																												
Layer Stackup																																																																															
<table border="1"> <thead> <tr> <th>Layer</th><th>Name</th><th>Material</th><th>Thickness</th><th>Constant</th><th>Board Layer Stack</th></tr> </thead> <tbody> <tr><td>1</td><td>Top Overlay</td><td></td><td></td><td></td><td></td></tr> <tr><td>2</td><td>Top Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr><td>3</td><td>Top Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr><td>4</td><td>Dielectric1</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr><td>5</td><td>GND</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr><td>6</td><td>Dielectric3</td><td>FR-4 HTg</td><td>45.00mil</td><td>4.5</td><td></td></tr> <tr><td>7</td><td>Power</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr><td>8</td><td>Dielectric2</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr><td>9</td><td>Bottom Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr><td>10</td><td>Bottom Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr><td>11</td><td>Bottom Overlay</td><td></td><td></td><td></td><td></td></tr> </tbody> </table>								Layer	Name	Material	Thickness	Constant	Board Layer Stack	1	Top Overlay					2	Top Solder	Solder Resist	0.40mil	3.5		3	Top Layer	Copper	2.10mil			4	Dielectric1	FR-4 HTg	6.00mil	4.5		5	GND	Copper	1.40mil			6	Dielectric3	FR-4 HTg	45.00mil	4.5		7	Power	Copper	1.40mil			8	Dielectric2	FR-4 HTg	6.00mil	4.5		9	Bottom Layer	Copper	2.10mil			10	Bottom Solder	Solder Resist	0.40mil	3.5		11	Bottom Overlay				
Layer	Name	Material	Thickness	Constant	Board Layer Stack																																																																										
1	Top Overlay																																																																														
2	Top Solder	Solder Resist	0.40mil	3.5																																																																											
3	Top Layer	Copper	2.10mil																																																																												
4	Dielectric1	FR-4 HTg	6.00mil	4.5																																																																											
5	GND	Copper	1.40mil																																																																												
6	Dielectric3	FR-4 HTg	45.00mil	4.5																																																																											
7	Power	Copper	1.40mil																																																																												
8	Dielectric2	FR-4 HTg	6.00mil	4.5																																																																											
9	Bottom Layer	Copper	2.10mil																																																																												
10	Bottom Solder	Solder Resist	0.40mil	3.5																																																																											
11	Bottom Overlay																																																																														

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

4. PLATING - 0.5oz 0.75oz 1oz Other

5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other

8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

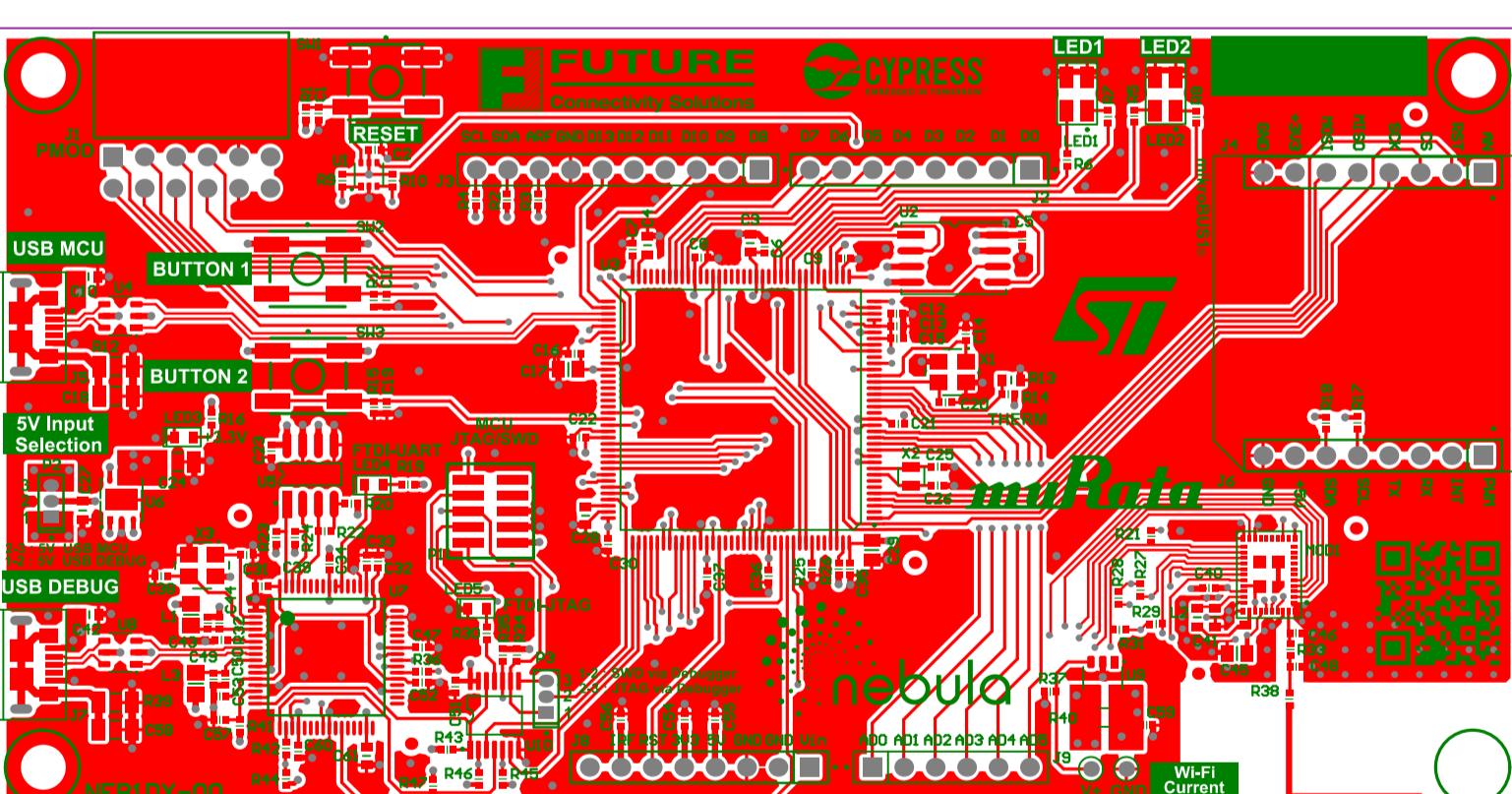
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

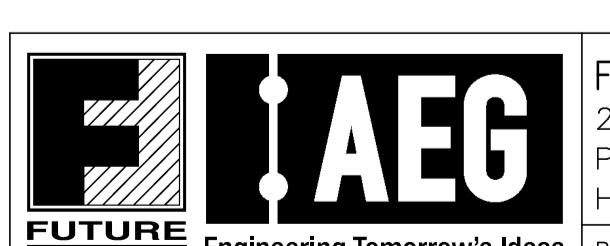
12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN

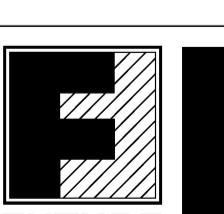


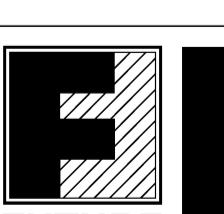
- CONFIDENTIAL -
THIS DRAWING CONTAINS PROPRIETARY INFORMATION
WHICH MAY NOT BE DISCLOSED TO OTHERS FOR ANY
PURPOSE WHATSOEVER OR USED FOR MANUFACTURING
PURPOSES WITHOUT PRIOR WRITTEN PERMISSION
FROM THE FUTURE ELECTRONICS CORPORATION.

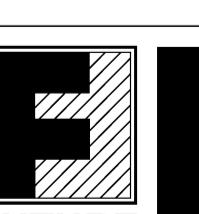


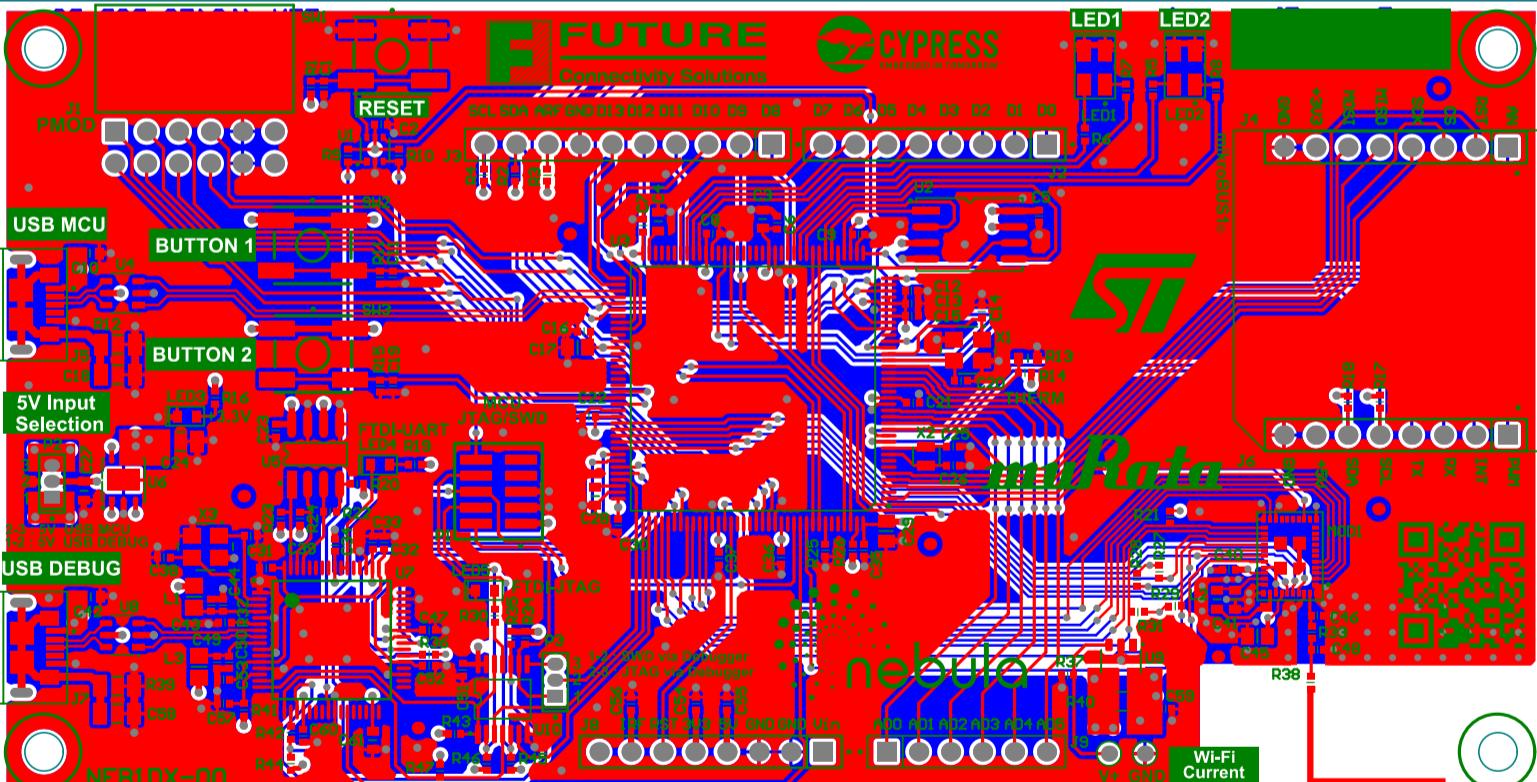
Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Project #	FCS-Murata-Cypress Dev kit
Drawn by:	M. Bernier
Title:	FCS-Murata-Cypress Dev kit
Size:	B
DWG NO:	FEN-413458-PCB-R0
REV:	0
Checked by:	H.Letourneau
Approved by:	M. Bernier
Date:	4/4/2017
Sheet	1 of 1

1	2	3	4	5	6	7	8																																																																								
Layers																																																																															
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="6">Impedance Requirements</th></tr> <tr> <th rowspan="2">Layer</th> <th colspan="2">Impedance 50 Ohms</th> <th colspan="2">Impedance 90 Ohms (Diff)</th> <th colspan="2">Impedance 100 Ohms (Diff)</th></tr> <tr> <th>Trace Width (mils)</th> <th>Trace Width (mils)</th> <th>Trace Spacing (mils)</th> <th>Trace Width (mils)</th> <th>Trace Spacing (mils)</th> </tr> </thead> <tbody> <tr> <td></td> <td>10 mils</td> <td>8 mils</td> <td>9 mils</td> <td></td> <td></td> </tr> <tr> <td></td> <td>10 mils</td> <td>8 mils</td> <td>9 mils</td> <td></td> <td></td> </tr> </tbody> </table>								Impedance Requirements						Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)		Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)		10 mils	8 mils	9 mils				10 mils	8 mils	9 mils																																												
Impedance Requirements																																																																															
Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)																																																																										
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)																																																																										
	10 mils	8 mils	9 mils																																																																												
	10 mils	8 mils	9 mils																																																																												
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Layer</th> <th>Name</th> <th>Material</th> <th>Thickness</th> <th>Constant</th> <th>Board Layer Stack</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Top Overlay</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>2</td> <td>Top Solder</td> <td>Solder Resist</td> <td>0.40mil</td> <td>3.5</td> <td></td> </tr> <tr> <td>3</td> <td>Top Layer</td> <td>Copper</td> <td>2.10mil</td> <td></td> <td></td> </tr> <tr> <td>4</td> <td>Dielectric1</td> <td>FR-4 HTg</td> <td>6.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>5</td> <td>GND</td> <td>Copper</td> <td>1.40mil</td> <td></td> <td></td> </tr> <tr> <td>6</td> <td>Dielectric3</td> <td>FR-4 HTg</td> <td>45.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>7</td> <td>Power</td> <td>Copper</td> <td>1.40mil</td> <td></td> <td></td> </tr> <tr> <td>8</td> <td>Dielectric2</td> <td>FR-4 HTg</td> <td>6.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>9</td> <td>Bottom Layer</td> <td>Copper</td> <td>2.10mil</td> <td></td> <td></td> </tr> <tr> <td>10</td> <td>Bottom Solder</td> <td>Solder Resist</td> <td>0.40mil</td> <td>3.5</td> <td></td> </tr> <tr> <td>11</td> <td>Bottom Overlay</td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>								Layer	Name	Material	Thickness	Constant	Board Layer Stack	1	Top Overlay					2	Top Solder	Solder Resist	0.40mil	3.5		3	Top Layer	Copper	2.10mil			4	Dielectric1	FR-4 HTg	6.00mil	4.5		5	GND	Copper	1.40mil			6	Dielectric3	FR-4 HTg	45.00mil	4.5		7	Power	Copper	1.40mil			8	Dielectric2	FR-4 HTg	6.00mil	4.5		9	Bottom Layer	Copper	2.10mil			10	Bottom Solder	Solder Resist	0.40mil	3.5		11	Bottom Overlay				
Layer	Name	Material	Thickness	Constant	Board Layer Stack																																																																										
1	Top Overlay																																																																														
2	Top Solder	Solder Resist	0.40mil	3.5																																																																											
3	Top Layer	Copper	2.10mil																																																																												
4	Dielectric1	FR-4 HTg	6.00mil	4.5																																																																											
5	GND	Copper	1.40mil																																																																												
6	Dielectric3	FR-4 HTg	45.00mil	4.5																																																																											
7	Power	Copper	1.40mil																																																																												
8	Dielectric2	FR-4 HTg	6.00mil	4.5																																																																											
9	Bottom Layer	Copper	2.10mil																																																																												
10	Bottom Solder	Solder Resist	0.40mil	3.5																																																																											
11	Bottom Overlay																																																																														
<p>NOTES: < UNLESS OTHERWISE SPECIFIED ></p> <p>1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)</p> <p>2. BASE MATERIAL - FR4 High Tg <input checked="" type="checkbox"/> Metal Core <input type="checkbox"/> Other <input type="checkbox"/> - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C</p> <p>3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL</p> <p>4. PLATING - 0.5oz <input type="checkbox"/> 0.75oz <input type="checkbox"/> 1oz <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>5. FINISH - HASL RoHS <input checked="" type="checkbox"/> HASL <input type="checkbox"/> Immersion Silver <input type="checkbox"/> Immersion Tin <input type="checkbox"/> ENIG <input type="checkbox"/> Other <input type="checkbox"/></p> <p>6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER - GREEN <input type="checkbox"/> WHITE <input type="checkbox"/> BLUE <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>7. SILKSCREEN - LPI - APPLY EPOXY BASED INK - TOP/BOTTOM <input type="checkbox"/> TOP ONLY <input checked="" type="checkbox"/> BOTTOM ONLY <input type="checkbox"/> NONE <input type="checkbox"/> - WHITE <input checked="" type="checkbox"/> BLACK <input type="checkbox"/> Other <input type="checkbox"/></p> <p>8. IMPEDANCE CONTROL - NO <input type="checkbox"/> YES <input checked="" type="checkbox"/> SEE TABLE FOR DETAIL</p> <p>9. ELECTRICAL TEST - 100% IPC-D-356B</p> <p>10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM</p> <p>11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT</p> <p>12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB</p> <p>13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND</p> <p>14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN</p>																																																																															
  <p>Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7</p> <p>Project # FCS-Murata-Cypress Dev kit</p> <p>Drawn by: M. Bernier</p> <p>Title: FCS-Murata-Cypress Dev kit</p> <p>Size: B DWG NO: FEN-413458-PCB-R0 REV: 0</p> <p>Checked by: H.Letourneau</p> <p>Approved by: M. Bernier</p> <p>Date: 4/4/2017</p> <p>Sheet 1 of 1</p>																																																																															
1	2	3	4	5	6	7	8																																																																								

1	2	3	4	5	6	7	8																																																																								
Layers																																																																															
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="6">Impedance Requirements</th></tr> <tr> <th rowspan="2">Layer</th> <th colspan="2">Impedance 50 Ohms</th> <th colspan="2">Impedance 90 Ohms (Diff)</th> <th colspan="2">Impedance 100 Ohms (Diff)</th></tr> <tr> <th>Trace Width (mils)</th> <th>Trace Width (mils)</th> <th>Trace Spacing (mils)</th> <th>Trace Width (mils)</th> <th>Trace Spacing (mils)</th> </tr> </thead> <tbody> <tr> <td></td> <td>10 mils</td> <td>8 mils</td> <td>9 mils</td> <td></td> <td></td> </tr> <tr> <td></td> <td>10 mils</td> <td>8 mils</td> <td>9 mils</td> <td></td> <td></td> </tr> </tbody> </table>								Impedance Requirements						Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)		Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)		10 mils	8 mils	9 mils				10 mils	8 mils	9 mils																																												
Impedance Requirements																																																																															
Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)																																																																										
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)																																																																										
	10 mils	8 mils	9 mils																																																																												
	10 mils	8 mils	9 mils																																																																												
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Layer</th> <th>Name</th> <th>Material</th> <th>Thickness</th> <th>Constant</th> <th>Board Layer Stack</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Top Overlay</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>2</td> <td>Top Solder</td> <td>Solder Resist</td> <td>0.40mil</td> <td>3.5</td> <td></td> </tr> <tr> <td>3</td> <td>Top Layer</td> <td>Copper</td> <td>2.10mil</td> <td></td> <td></td> </tr> <tr> <td>4</td> <td>Dielectric1</td> <td>FR-4 HTg</td> <td>6.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>5</td> <td>GND</td> <td>Copper</td> <td>1.40mil</td> <td></td> <td></td> </tr> <tr> <td>6</td> <td>Dielectric3</td> <td>FR-4 HTg</td> <td>45.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>7</td> <td>Power</td> <td>Copper</td> <td>1.40mil</td> <td></td> <td></td> </tr> <tr> <td>8</td> <td>Dielectric2</td> <td>FR-4 HTg</td> <td>6.00mil</td> <td>4.5</td> <td></td> </tr> <tr> <td>9</td> <td>Bottom Layer</td> <td>Copper</td> <td>2.10mil</td> <td></td> <td></td> </tr> <tr> <td>10</td> <td>Bottom Solder</td> <td>Solder Resist</td> <td>0.40mil</td> <td>3.5</td> <td></td> </tr> <tr> <td>11</td> <td>Bottom Overlay</td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>								Layer	Name	Material	Thickness	Constant	Board Layer Stack	1	Top Overlay					2	Top Solder	Solder Resist	0.40mil	3.5		3	Top Layer	Copper	2.10mil			4	Dielectric1	FR-4 HTg	6.00mil	4.5		5	GND	Copper	1.40mil			6	Dielectric3	FR-4 HTg	45.00mil	4.5		7	Power	Copper	1.40mil			8	Dielectric2	FR-4 HTg	6.00mil	4.5		9	Bottom Layer	Copper	2.10mil			10	Bottom Solder	Solder Resist	0.40mil	3.5		11	Bottom Overlay				
Layer	Name	Material	Thickness	Constant	Board Layer Stack																																																																										
1	Top Overlay																																																																														
2	Top Solder	Solder Resist	0.40mil	3.5																																																																											
3	Top Layer	Copper	2.10mil																																																																												
4	Dielectric1	FR-4 HTg	6.00mil	4.5																																																																											
5	GND	Copper	1.40mil																																																																												
6	Dielectric3	FR-4 HTg	45.00mil	4.5																																																																											
7	Power	Copper	1.40mil																																																																												
8	Dielectric2	FR-4 HTg	6.00mil	4.5																																																																											
9	Bottom Layer	Copper	2.10mil																																																																												
10	Bottom Solder	Solder Resist	0.40mil	3.5																																																																											
11	Bottom Overlay																																																																														
<p>NOTES: < UNLESS OTHERWISE SPECIFIED ></p> <p>1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)</p> <p>2. BASE MATERIAL - FR4 High Tg <input checked="" type="checkbox"/> Metal Core <input type="checkbox"/> Other <input type="checkbox"/> - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C</p> <p>3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL</p> <p>4. PLATING - 0.5oz <input type="checkbox"/> 0.75oz <input type="checkbox"/> 1oz <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>5. FINISH - HASL RoHS <input checked="" type="checkbox"/> HASL <input type="checkbox"/> Immersion Silver <input type="checkbox"/> Immersion Tin <input type="checkbox"/> ENIG <input type="checkbox"/> Other <input type="checkbox"/></p> <p>6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER - GREEN <input type="checkbox"/> WHITE <input type="checkbox"/> BLUE <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>7. SILKSCREEN - LPI - APPLY EPOXY BASED INK - TOP/BOTTOM <input type="checkbox"/> TOP ONLY <input checked="" type="checkbox"/> BOTTOM ONLY <input type="checkbox"/> NONE <input type="checkbox"/> - WHITE <input checked="" type="checkbox"/> BLACK <input type="checkbox"/> Other <input type="checkbox"/></p> <p>8. IMPEDANCE CONTROL - NO <input type="checkbox"/> YES <input checked="" type="checkbox"/> SEE TABLE FOR DETAIL</p> <p>9. ELECTRICAL TEST - 100% IPC-D-356B</p> <p>10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM</p> <p>11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT</p> <p>12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB</p> <p>13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND</p> <p>14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN</p>																																																																															
  <p>Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7</p> <p>Project # FCS-Murata-Cypress Dev kit</p> <p>Designed by: M. Bernier Drawn by: M. Bernier Title: FCS-Murata-Cypress Dev kit</p> <p>Checked by: H.Letourneau Approved by: M. Bernier Size: B DWG NO: FEN-413458-PCB-R0 REV: 0</p> <p>Date: 4/4/2017 Sheet 1 of 1</p>																																																																															
1	2	3	4	5	6	7	8																																																																								

1	2	3	4	5	6	7	8																																																																								
Layers	Bottom Layer																																																																														
Impedance Requirements <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse; width: fit-content;"> <thead> <tr> <th rowspan="2">Layer</th><th colspan="2">Impedance 50 Ohms</th><th colspan="2">Impedance 90 Ohms (Diff)</th><th colspan="2">Impedance 100 Ohms (Diff)</th></tr> <tr> <th>Trace Width (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th></tr> </thead> <tbody> <tr> <td>Bottom Layer</td><td>10 mils</td><td>8 mils</td><td>9 mils</td><td></td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td></tr> </tbody> </table>								Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)		Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	Bottom Layer	10 mils	8 mils	9 mils																																																								
Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)																																																																										
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)																																																																										
Bottom Layer	10 mils	8 mils	9 mils																																																																												
<table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse; width: fit-content;"> <thead> <tr> <th>Layer</th><th>Name</th><th>Material</th><th>Thickness</th><th>Constant</th><th>Board Layer Stack</th></tr> </thead> <tbody> <tr> <td>1</td><td>Top Overlay</td><td></td><td></td><td></td><td></td></tr> <tr> <td>2</td><td>Top Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr> <td>3</td><td>Top Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr> <td>4</td><td>Dielectric1</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr> <td>5</td><td>GND</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr> <td>6</td><td>Dielectric3</td><td>FR-4 HTg</td><td>45.00mil</td><td>4.5</td><td></td></tr> <tr> <td>7</td><td>Power</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr> <td>8</td><td>Dielectric2</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr> <td>9</td><td>Bottom Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr> <td>10</td><td>Bottom Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr> <td>11</td><td>Bottom Overlay</td><td></td><td></td><td></td><td></td></tr> </tbody> </table>								Layer	Name	Material	Thickness	Constant	Board Layer Stack	1	Top Overlay					2	Top Solder	Solder Resist	0.40mil	3.5		3	Top Layer	Copper	2.10mil			4	Dielectric1	FR-4 HTg	6.00mil	4.5		5	GND	Copper	1.40mil			6	Dielectric3	FR-4 HTg	45.00mil	4.5		7	Power	Copper	1.40mil			8	Dielectric2	FR-4 HTg	6.00mil	4.5		9	Bottom Layer	Copper	2.10mil			10	Bottom Solder	Solder Resist	0.40mil	3.5		11	Bottom Overlay				
Layer	Name	Material	Thickness	Constant	Board Layer Stack																																																																										
1	Top Overlay																																																																														
2	Top Solder	Solder Resist	0.40mil	3.5																																																																											
3	Top Layer	Copper	2.10mil																																																																												
4	Dielectric1	FR-4 HTg	6.00mil	4.5																																																																											
5	GND	Copper	1.40mil																																																																												
6	Dielectric3	FR-4 HTg	45.00mil	4.5																																																																											
7	Power	Copper	1.40mil																																																																												
8	Dielectric2	FR-4 HTg	6.00mil	4.5																																																																											
9	Bottom Layer	Copper	2.10mil																																																																												
10	Bottom Solder	Solder Resist	0.40mil	3.5																																																																											
11	Bottom Overlay																																																																														
<p>NOTES: < UNLESS OTHERWISE SPECIFIED ></p> <p>1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)</p> <p>2. BASE MATERIAL - FR4 High Tg <input checked="" type="checkbox"/> Metal Core <input type="checkbox"/> Other <input type="checkbox"/> - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C</p> <p>3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL</p> <p>4. PLATING - 0.5oz <input type="checkbox"/> 0.75oz <input type="checkbox"/> 1oz <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>5. FINISH - HASL RoHS <input checked="" type="checkbox"/> HASL <input type="checkbox"/> Immersion Silver <input type="checkbox"/> Immersion Tin <input type="checkbox"/> ENIG <input type="checkbox"/> Other <input type="checkbox"/></p> <p>6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER - GREEN <input type="checkbox"/> WHITE <input type="checkbox"/> BLUE <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>7. SILKSCREEN - LPI - APPLY EPOXY BASED INK - TOP/BOTTOM <input type="checkbox"/> TOP ONLY <input checked="" type="checkbox"/> BOTTOM ONLY <input type="checkbox"/> NONE <input type="checkbox"/> - WHITE <input checked="" type="checkbox"/> BLACK <input type="checkbox"/> Other <input type="checkbox"/></p> <p>8. IMPEDANCE CONTROL - NO <input type="checkbox"/> YES <input checked="" type="checkbox"/> SEE TABLE FOR DETAIL</p> <p>9. ELECTRICAL TEST - 100% IPC-D-356B</p> <p>10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM</p> <p>11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT</p> <p>12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB</p> <p>13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND</p> <p>14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN</p>																																																																															
  FUTURE ELECTRONICS Engineering Tomorrow's Ideas <p>Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Project #</td><td colspan="2">FCS-Murata-Cypress Dev kit</td></tr> <tr> <td>Title:</td><td colspan="2">FCS-Murata-Cypress Dev kit</td></tr> <tr> <td>Size: B</td><td>DWG NO: FEN-413458-PCB-R0</td><td>REV: 0</td></tr> <tr> <td>Checked by: H.Letourneau</td><td>Approved by: M. Bernier</td><td>Date: 4/4/2017</td></tr> <tr> <td colspan="2"></td><td>Sheet 1 of 1</td></tr> </table>								Project #	FCS-Murata-Cypress Dev kit		Title:	FCS-Murata-Cypress Dev kit		Size: B	DWG NO: FEN-413458-PCB-R0	REV: 0	Checked by: H.Letourneau	Approved by: M. Bernier	Date: 4/4/2017			Sheet 1 of 1																																																									
Project #	FCS-Murata-Cypress Dev kit																																																																														
Title:	FCS-Murata-Cypress Dev kit																																																																														
Size: B	DWG NO: FEN-413458-PCB-R0	REV: 0																																																																													
Checked by: H.Letourneau	Approved by: M. Bernier	Date: 4/4/2017																																																																													
		Sheet 1 of 1																																																																													
1	2	3	4	5	6	7	8																																																																								

1	2	3	4	5	6	7	8																																																																								
Layers	Top Layer	Bottom Layer																																																																													
<table border="1"> <thead> <tr> <th colspan="6">Impedance Requirements</th> </tr> <tr> <th>Layer</th><th>Impedance 50 Ohms</th><th>Impedance 90 Ohms (Diff)</th><th>Impedance 100 Ohms (Diff)</th><th> </th><th> </th></tr> <tr> <th>Layer</th><th>Trace Width (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th><th>Trace Width (mils)</th><th>Trace Spacing (mils)</th></tr> </thead> <tbody> <tr> <td>Top Layer</td><td>10 mils</td><td>8 mils</td><td>9 mils</td><td></td><td></td></tr> <tr> <td>Bottom Layer</td><td>10 mils</td><td>8 mils</td><td>9 mils</td><td></td><td></td></tr> </tbody> </table>								Impedance Requirements						Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)	Impedance 100 Ohms (Diff)			Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	Top Layer	10 mils	8 mils	9 mils			Bottom Layer	10 mils	8 mils	9 mils																																												
Impedance Requirements																																																																															
Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)	Impedance 100 Ohms (Diff)																																																																												
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)																																																																										
Top Layer	10 mils	8 mils	9 mils																																																																												
Bottom Layer	10 mils	8 mils	9 mils																																																																												
A																																																																															
B																																																																															
C																																																																															
D																																																																															
<table border="1"> <thead> <tr> <th>Layer</th><th>Name</th><th>Material</th><th>Thickness</th><th>Constant</th><th>Board Layer Stack</th></tr> </thead> <tbody> <tr> <td>1</td><td>Top Overlay</td><td></td><td></td><td></td><td></td></tr> <tr> <td>2</td><td>Top Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr> <td>3</td><td>Top Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr> <td>4</td><td>Dielectric1</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr> <td>5</td><td>GND</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr> <td>6</td><td>Dielectric3</td><td>FR-4 HTg</td><td>45.00mil</td><td>4.5</td><td></td></tr> <tr> <td>7</td><td>Power</td><td>Copper</td><td>1.40mil</td><td></td><td></td></tr> <tr> <td>8</td><td>Dielectric2</td><td>FR-4 HTg</td><td>6.00mil</td><td>4.5</td><td></td></tr> <tr> <td>9</td><td>Bottom Layer</td><td>Copper</td><td>2.10mil</td><td></td><td></td></tr> <tr> <td>10</td><td>Bottom Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td></tr> <tr> <td>11</td><td>Bottom Overlay</td><td></td><td></td><td></td><td></td></tr> </tbody> </table>								Layer	Name	Material	Thickness	Constant	Board Layer Stack	1	Top Overlay					2	Top Solder	Solder Resist	0.40mil	3.5		3	Top Layer	Copper	2.10mil			4	Dielectric1	FR-4 HTg	6.00mil	4.5		5	GND	Copper	1.40mil			6	Dielectric3	FR-4 HTg	45.00mil	4.5		7	Power	Copper	1.40mil			8	Dielectric2	FR-4 HTg	6.00mil	4.5		9	Bottom Layer	Copper	2.10mil			10	Bottom Solder	Solder Resist	0.40mil	3.5		11	Bottom Overlay				
Layer	Name	Material	Thickness	Constant	Board Layer Stack																																																																										
1	Top Overlay																																																																														
2	Top Solder	Solder Resist	0.40mil	3.5																																																																											
3	Top Layer	Copper	2.10mil																																																																												
4	Dielectric1	FR-4 HTg	6.00mil	4.5																																																																											
5	GND	Copper	1.40mil																																																																												
6	Dielectric3	FR-4 HTg	45.00mil	4.5																																																																											
7	Power	Copper	1.40mil																																																																												
8	Dielectric2	FR-4 HTg	6.00mil	4.5																																																																											
9	Bottom Layer	Copper	2.10mil																																																																												
10	Bottom Solder	Solder Resist	0.40mil	3.5																																																																											
11	Bottom Overlay																																																																														
<p>NOTES: < UNLESS OTHERWISE SPECIFIED ></p> <p>1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)</p> <p>2. BASE MATERIAL - FR4 High Tg <input checked="" type="checkbox"/> Metal Core <input type="checkbox"/> Other <input type="checkbox"/> - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C</p> <p>3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL</p> <p>4. PLATING - 0.5oz <input type="checkbox"/> 0.75oz <input type="checkbox"/> 1oz <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>5. FINISH - HASL RoHS <input checked="" type="checkbox"/> HASL <input type="checkbox"/> Immersion Silver <input type="checkbox"/> Immersion Tin <input type="checkbox"/> ENIG <input type="checkbox"/> Other <input type="checkbox"/></p> <p>6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER - GREEN <input type="checkbox"/> WHITE <input type="checkbox"/> BLUE <input checked="" type="checkbox"/> Other <input type="checkbox"/></p> <p>7. SILKSCREEN - LPI - APPLY EPOXY BASED INK - TOP/BOTTOM <input type="checkbox"/> TOP ONLY <input checked="" type="checkbox"/> BOTTOM ONLY <input type="checkbox"/> NONE <input type="checkbox"/> - WHITE <input checked="" type="checkbox"/> BLACK <input type="checkbox"/> Other <input type="checkbox"/></p> <p>8. IMPEDANCE CONTROL - NO <input type="checkbox"/> YES <input checked="" type="checkbox"/> SEE TABLE FOR DETAIL</p> <p>9. ELECTRICAL TEST - 100% IPC-D-356B</p> <p>10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM</p> <p>11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT</p> <p>12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB</p> <p>13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND</p> <p>14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN</p> <p style="text-align: right;"><input checked="" type="checkbox"/></p>																																																																															
 <p>- CONFIDENTIAL - THIS DRAWING CONTAINS PROPRIETARY INFORMATION WHICH MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE WHATSOEVER OR USED FOR MANUFACTURING PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM THE FUTURE ELECTRONICS CORPORATION.</p> <p>FUTURE ELECTRONICS AEG Engineering Tomorrow's Ideas</p> <p>Future Electronics – System Design Center NA 237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7</p> <table border="1"> <tr> <td>Project #</td><td colspan="3">FCS-Murata-Cypress Dev kit</td></tr> <tr> <td>Drawn by:</td><td>M. Bernier</td><td>Drawn by:</td><td>M. Bernier</td></tr> <tr> <td>Title:</td><td colspan="3">FCS-Murata-Cypress Dev kit</td></tr> <tr> <td>Size:</td><td>B</td><td>DWG NO:</td><td>FEN-413458-PCB-R0</td></tr> <tr> <td>Checked by:</td><td>H.Letourneau</td><td>Approved by:</td><td>M. Bernier</td></tr> <tr> <td>Date:</td><td colspan="3">4/4/2017</td></tr> <tr> <td>Sheet</td><td colspan="3">1 of 1</td></tr> </table>								Project #	FCS-Murata-Cypress Dev kit			Drawn by:	M. Bernier	Drawn by:	M. Bernier	Title:	FCS-Murata-Cypress Dev kit			Size:	B	DWG NO:	FEN-413458-PCB-R0	Checked by:	H.Letourneau	Approved by:	M. Bernier	Date:	4/4/2017			Sheet	1 of 1																																														
Project #	FCS-Murata-Cypress Dev kit																																																																														
Drawn by:	M. Bernier	Drawn by:	M. Bernier																																																																												
Title:	FCS-Murata-Cypress Dev kit																																																																														
Size:	B	DWG NO:	FEN-413458-PCB-R0																																																																												
Checked by:	H.Letourneau	Approved by:	M. Bernier																																																																												
Date:	4/4/2017																																																																														
Sheet	1 of 1																																																																														

