BRYANT * O'HALLARON	
Computer Systems: A Programmer's Perspective, 3/E (CS:AIR Randal E. Bryant and David R. O'Hallaron, Carnegie Mellon • Contact us • Programmer's Perspective, 3/E (CS:AIR Randal E. Bryant and David R. O'Hallaron, Carnegie Mellon	
 Request desk copy Changes from 2/E Amazon.com Pearson About 	
 Home Web Asides Student Site Instructor Site TOC and Preface Adoptions 	
 Errata Papers Curriculum Courses 	
Errata for CS:APP3e and its Last updated 10/02/2020. Despite our best efforts to create a book with zero defects, our	Instructors Manual r vigilant readers have pointed out some bugs. Please report any new errata to Randy Bryant and Dave O'Hallaron. Note that some of
these errors have been corrected in more recent printings. We maintain errata for the North American edition. Errata for • Chinese, maintained by Prof. Yili Gong of Wuhan Univ	editions in other languages can be found as follows:
Note on the Global Edition: Unfortunately, the publisher are very good job, and so these problems and their solutions have North American Edition (ISBN-10: 0-13-409266-	
 Preface Chapter 1: A Tour of Computer Systems Chapter 2: Representing and Manipulating Informs p. 45, code for show_bytes. Variable i should be Posted 07/11/2015. Randal E. Bryant p. 47, aside "New to C? Formatted printing with 	
Posted 05/23/2016. Yili Gong	ntence should state: "This behavior is not guaranteed for C programs, however, and so shift amounts should be kept less than the
 Posted 10/25/2015. Shoeb Mohammed p. 82, second line. 'x should be x'. Posted 10/25/2015. Shoeb Mohammed p. 82, third line. Value x should be computed with Posted 11/13/2015. Parinya Suparit 	
Posted 11/13/2015. Parinya Suparit	and side should be computed with function $B2U_w(x)$, not $B2T_w(x)$. igns are incorrectly printed as the numeral '2'. A correct version of the image can be found here. aird row should be $25/16$.
 Posted 09/05/2016. JiaSheng Chen p. 153, Solution to Problem 2.32. The sentence s nonnegative." Posted 10/25/2015. Shoeb Mohammed 	tarting on third line should state "In fact, the opposite is true: tsub_ok(x, TMin) should yield 1 when x is negative and 0 when it is
 p. 154, Solution to Problem 2.35, second line of and proof are valid.) <i>Posted 07/12/2018. Wang Lei</i> Chapter 3: Machine-Level Representation of Progration of Progra	
 p. 174, code annotation at top of page. It should a Posted 10/25/2015. Shoeb Mohammed p. 175, code annotation in middle of page. It shoe Posted 10/25/2015. Shoeb Mohammed p. 175, Paragraph starting "This code is almost in the page." 	read "Disassembly of function multstore in binary file mstore.o." uld read "Disassembly of function multstore in binary file prog." dentical" in middle of page. The end of the sentence should read "disassembly of mstore.o."
Posted 11/09/2015. Shoeb Mohammed o p. 179, Section 3.4, first paragraph. The ranges g For 8086: %ax through %sp. For IA32: %eax through %esp.	ormats," last sentence of first paragraph. The assembly code shown is for the function multstore, not sum.
	The code should be "movb \$-17, (%rsp)." Although there is an instruction movzbq, the GCC compiler typically generates the instruction movzbl for this purpose, relying on the with a register as destination will fill the upper 4 bytes of the register with zeros.
 Posted 11/09/2015. Shoeb Mohammed p. 191, second full paragraph. The first sentence Posted 09/28/2015. Max Ma 	o printf. The format string should be "a = %ld, b = %ld\n". should state: "The third column of Figure 3.9 illustrates the effect of executing the instruction popq %rdx" third column of Figure 3" It should state that the value 0x123 remains at memory location 0x100.
 Posted 11/09/2015. Carlos Galdino p. 198, first line of first full paragraph. There show Posted 09/19/2016. Anise Ghorbani p. 199, third full paragraph. The reference to instance Posted 02/21/2017. Changan Wang 	ruction idiv1 should be to idivq instead.
 Posted 09/19/2015. Xingda Zhai p. 200, first line of text. It should state "In this control Posted 08/16/2015. Dmitry Neverov 	ald start with "For most applications of 64-bit <i>division</i> " ode, argument <i>qp</i> must first be saved in a different register (line 2)," ule for setting the cF flag when subtraction is performed requires special consideration. If t=a-b, then the flag will be set when
 Posted 10/13/2021. Tung Luu p. 201, 9 lines from bottom. For the shift instruct Posted 10/30/2017. Jiaheng Wang p. 204, Practice Problem 3.13, second paragraph Posted 10/15/2015. Ronald Greenberg 	ion, it should state: "The overflow flag is changed only when the shift amounts is 1, following rules that depend on the shift type." It should state "Suppose a is in some portion of %rdi while"
 p. 205, Practice Problem 3.13, code for D. The server posted 11/09/2015. Carlos Galdino p. 214, third paragraph. The second sentence show Posted 11/11/2015. Yili Gong p. 214, Figure 3.17(c). The comment on line 8 of Posted 03/18/2017. 	uld be "The function computes the absolute value of the difference of its two arguments x and y ,"
reach value 1 before reaching a value less than 1 Posted 06/11/2017. Daniel O'Brien	5. It should state "The compiler has determined that the loop can only be entered when $n > 1$, and that, as n is decremented, it will."
 Posted 09/02/2015. Dmitry Neverov p. 235, Figure 3.23, annotation for line 5 of code Posted 12/25/2015. Xinzhen Chen 	I state " indexed by register %rsi, which holds" It should state "Goto *jt[index]." de at top of page. The register allocation is listed incorrectly. It should state "a in %rdi, b in %rsi, c in %rdx, dest in %rcx."
 p. 241, fourth and fifth lines. They should state " Posted 09/02/2015. Dmitry Neverov p. 243, Figure 3.27a, line 2. The annotation shou Posted 02/15/2016. Xinzhen Chen p. 244, first full paragraph. The value 0x400054e Posted 07/26/2017. Daniel O'Brien 	
 p. 244, second full paragraph. The value 0x40001 Posted 07/26/2017. Daniel O'Brien p. 244, Comment after line 4. It should state "Districted 09/02/2015. Dmitry Neverov p. 249, Fourth line from bottom. Sentence ending 	sassembly of first(long x)"
arguments." Posted 11/23/2015. Vlad Buslov	ences should state "Consider a function P, which generates local values, named a0–a7. It then calls function Q, which has no sembly code for the first entry should be "movq %rdx,%rax."
 Posted 10/25/2015. Karan Dwivedi p. 263, assembly code in middle of page, line 3. 	The annotation should state: "Read from $M[x_A + 12i + 4j]$."
 Posted 02/11/2016. Elizabeth White p. 264, Annotations of last block of assembly con Posted 07/26/2017. Daniel O'Brien p. 266, middle of page. The declaration and initial struct rect r = { 0, 0, 10, 20, 0xFF00FF Posted 08/04/2015. Yu Zhong 	alization of r should be:
Posted 09/02/2015. Dmitry Neverov	clarations. They should state " if the object has type T , then the pointer has type $T *$." tion should read "Character array buf is just <i>below</i> part of the saved state." The second entry should have the range $8-23$.
 p. 282, Practice Problem 3.46, second paragraph Posted 11/23/2015. Vlad Buslov p. 284, Practice Problem 3.46, part E. The questi Posted 07/26/2017. Daniel O'Brien 	It should state that get_line is called with return address $0x400076$. on for ask for <i>three</i> things wrong with the code. the third line should state " let s_1 denote" (delete "let us").
 Posted 12/27/2020. Ashwin Najappa p. 293, Practice Problem 3.49, second paragraph Posted 11/09/2015. Shoeb Mohammed p. 295, Figure 3.45. The lower 128 bits of register Posted 10/28/2015. David Hirschv p. 300, Problem 3.51, second line. The return value 	
 Posted 10/13/2016. Anise Ghorbani p. 306, Table listing two instructions. These shot Posted 03/09/2018. Weicheng Pei p. 313, Problem 3.60, first line of code. Argumen Posted 07/21/2015. Lauren Cooper 	ald be vucomiss and vucomisd (AVX instructions), rather than ucomiss and ucomisd (SSE instructions).
than those of type int. See, for example https://www.posted-04/26/2018 . Randal Bryant o p. 326, Solution to Problem 3.3, fifth line of code Posted 06/02/2015. Zhi Li o p. 326, Solution to Problem 3.3, sixth line of code posted 06/02/2015.	wiki.sei.cmu.edu/confluence/display/c/INT02-C.+Understand+integer+conversion+rules. This topic is not covered in the book. The code should be movq %rax, \$0x123 to be consistent with the problem statement, although both versions have the same error. The code should be movl %eax, %rdx to be consistent with the problem statement, although both versions have the same error.
 Posted 09/02/2015. Elizabeth White (Clarification, not an erratum) p. 326, Solution to extend the 1-byte value to 8 bytes. See the note of Posted 04/27/2018. Randal Bryant p. 330, Solution to Problem 3.14D. The comparing Posted 08/16/2015. Dmitry Neverov 	
 p. 331, Solutions to Problems 3.15B and 3.15D. Posted 12/04/2015. Carlos Galdino and Yili Gong p. 333, Solution to Problem 3.20. The comment of Posted 06/02/2015. Curtis Gagliardi p. 338, Solution to Problem 3.30, third bullet. The 	The values starting with "0x0x" should start with "0x" instead. on the third line of code should read "Test x". the final sentence should say "Thus, case labels 3 and 6 are missing in the switch statement body."
 Posted 09/27/2015. Xinyun Zhao p. 339, Solution to Problem 3.32, line labeled "F Posted 10/13/2016. Wenjun Huang p. 339, Solution to Problem 3.33, line 4. The exp Posted 06/24/2019. Deepayan Patra p. 346, Solution to Problem 3.46C. The program 	
 Posted 07/26/2017. Daniel O'Brien p. 348, Solution to Problem 3.51. In the third ent Posted 08/09/2015. Yu Zhong 	ne program should test the value returned by gets to make sure it's not NULL. ry of the table, the conversion is from double to float, as is requested in the problem statement. of text. The ambiguity arises from the commutativity of addition, not multiplication.
 Posted 11/09/2015. Shoeb Mohammed Chapter 4: Processor Architecture p. 360, Problem 4.2A. There should be an additional Posted 08/16/2016. James Timmins p. 360, Problem 4.2B. There should be an additional posted of the problem 4.2B. 	onal byte with hexadecimal value 90 at the end of the sequence. onal byte with hexadecimal value 90 at the end of the sequence.
Posted 06/23/2017. Yiling Gong	omment should say "Test count" incorrect. They should be 0x000d000d0, 0x00c000c0, 0x0b000b000b00, and 0xa000a000a000. The value 0xabcdabcdabcdabcd should be 0xabcdabcdabcd.
 Posted 10/02/2020. Radoslaw Jurga p. 371, Practice Problem 4.7. The annotation for Posted 12/02/2015. Alex Knaust p. 377, Figure 4.13(b): The last selection in the Fosted 06/02/2015. Paul Anagnostopoulos p. 404, Figure 4.26, 7th entry. The name should I 	ICL code should read "1 : B;" (The number 1 rather than the letter 1).
 Posted 10/24/2016. Wenjun Huang p. 404, Figure 4.26, 14th entry. The name should Posted 08/26/2015. Yu Zhong p. 405, Caption of Figure 4.27. It should state "T Posted 07/25/2015. Randal E. Bryant 	be RRSP, not RESP. en bytes are read from the instruction memory"
 Posted 08/26/2015. Yu Zhong p. 420, second line from bottom. Reference to Fi Posted 07/23/2018. Jong-won Choi 	gure 4.38(c) should be to Figure 4.38(d). Intended should state "The value for register %rbx is also forwarded from the memory to the decode stage."
 p. 434, Figure 4.47. The instruction at address 0x Posted 11/23/2015. Warren Crasta p. 441, Figure 4.53. The instruction at address 0x Posted 07/28/2015. Randal Bryant p. 443, Figure 4.55. Three errors: The program is prog6. 	
 The instruction at address 0x000 should be The instruction at address 0x013 should be Posted 07/28/2015. Randal Bryant + 12/21/2017 Dave Ohlsson p. 444, Figure 4.56. The instructions at addresses Posted 10/24/2016. Wenjun Huang 	eirmovq \$10,%rdx. 0x016 and 0x020 should be irmovq.
 complete implementation, the PC would be set to Posted 06/05/2018. Eadren King p. 454, last sentence on page. It should read "In the Posted 12/25/2015. Jiwen He p. 473, Bibliographic Notes. In the last line, "Interest of the Posted 12/25/2015. 	te, our processor designs do not attempt to set the program counter (PC) to a consistent value when an exception occurs. In a more of the address of the instruction that causes the exception, but this is not the case for the pipelined implementations. This figure, you can also see that many of the values in pipeline registers M and W" The el-compatible x86-64 processor should be "Intel-compatible IA32 processor."
Posted 10/13/2021. Yili Gong	should state " register %rax will be set to the incremented stack pointer " sentence should state: " the conditional move source value 0x123 gets forwarded into ALU input valA, while input valB correctly
 p. 494, Solution to Problem 4.44. The answers to The inner loop of the code using the condi The inner loop of the code using the condi The conditional jump code requires an ave The conditional move code requires an ave 	tional jump contains 9 instructions, 8 of which are executed when the array element is positive. tional move contains 8 instructions. rage of 9.5 cycles.
 Chapter 5: Optimizing Program Performance p. 520, around 1/3 way down the page. The reference Posted 12/01/2015. Shoeb Mohammed p. 533, second to last line in first paragraph. It she Posted 07/26/2017. Daniel O'Brien 	
 p. 533, code annotations for inner loop of combin Posted 12/01/2015. Shoeb Mohammed p. 533-534, sentence spanning these two pages. acc by data[i+1]. Posted 01/02/2016. Mark Morrissey p. 546. Web Aside OPT:SIMD. The assembly co 	It should state: "The loop unrolling leads to two vmulsd instructions—one to multiply acc by data[i], and the second to multiply
 Posted 05/08/2016. Sheldon Guo p. 547. Table in description of Web Aside OPT:S The headings under the category "Floating Posted 07/25/2015. Randal E. Bryant p. 556, Figure 5.33 caption. dest should be dst 	
 Posted 07/31/2018. Tanvir Alam Chapter 6: The Memory Hierarchy p. 602, Section 6.1.4, paragraph 4, line 9. 1980 s Posted 1/11/2016. Yili Gong p. 612, [Clarification]: The last sentence of the C Posted 07/31/2018. Dave Ohlsson 	
 Posted 07/31/2018. Debbie Neft p. 651, Problem 6.29A, The diagram should have Posted 11/23/2015. Tj Gilbrough p. 661, The solution to Problem 6.4: For parts A and B, the 1 MB file consists of Posted 07/30/2018. Jonatan Schroeder 	e 12 boxes instead of 13. of 2,048 512-byte logical blocks, not 2,000 as stated in the solution.
	tal transfer time for the blocks, which is 2 x $T_{max\ rotation} = 12 \text{ ms.}$ ected lifetime is $\sim 17,535$ years, not 140 years.
 Posted 12/16/2015. Yili Gong p. 683, [Clarification]: The variable x referred to Posted 07/31/2018. Dave Ohlsson 	the values of x and y are corrupted, but the precise values are system-dependent. in the first paragraph is from £005.c. ecall from Section 3.6.3" should be "Recall from Section 3.6.4."
 p. 698, Figure 7.15. The address for the user stace Posted 07/09/2015. Dave O'Hallaron p. 698, Figure 7.15. %esp should be %rsp. Posted 10/21/2015. Liz White p. 715, Problem 7.8, Module 2. static int mai 	k (2 ⁴⁸ –1) is wrong. The correct address is much smaller, and varies from process to process. n=1[should be static int main=1;
 Posted 07/30/2018. Michael Hinton and Michael Ross Chapter 8: Exceptional Control Flow p. 735, Figure 8.13. Two errors: The address for the user stack (2⁴⁸-1) is well posted 07/14/2015. Dave O'Hallaron %esp should be %rsp. 	rong. The correct address is much smaller, and varies from process to process.
each possible outcome can indeed occur." Posted 07/31/2018. Dave Ohlsson	e: "The only correct assumption is that each possible outcome is equally likely" or replace it with "The only correct assumption is that name if it exists" should be "Returns: pointer to value associated with name if it exists"
 p. 752, Practice problem 8.6, output of ./myecho Posted 7/30/2018. Li Du. p. 756, Figure 8.25. parseline() should check to Posted 7/30/2018. Dave Ohlsson. p. 762. Definition of signal function. On error, to p. 762. 	hat the capacity of argv (= MAXARGS, defined in Figure 8.23) is not exceeded. his function sets errno to indicate the cause. r>Posted 07/31/2018. Dave Ohlsson
 p. 763, Figure 8.30. For consistency, pause() sh Posted 02/26/2018. Bill Nace p. 768, Fig 8.34. Fixed sio_putl so that it correct Posted 10/19/2016. Randy Bryant p. 773, Fig 8.37, line 5. To avoid the signal hand Posted 12/11/2018. Fahim Faisal 	
 p. 777, Fig 8.39, line 9. To avoid the signal hand Posted 12/11/2018. Fahim Faisal p. 779, Fig 8.40, line 8. To avoid the signal hand Posted 12/11/2018. Fahim Faisal p. 781. In the description of sigsuspend in the second signal hand posted 12/11/2018. 	ler potentially blocking on long-running jobs, waitpid should be called with the wnohang option. ler potentially blocking on long-running jobs, waitpid should be called with the wnohang option. econd paragraph, line 1 should be sigprocmask(SIG_SETMASK, &mask, &prev);
 Posted 10/28/2015. Dave O'Hallaron p. 796. Figure 8.47. On the top line of the process Posted 11/8/2015. Eric Adlam p. 797. Figure 8.49. In the process graph, the bot Posted 1/14/2019. Roslyn Cyrus Chapter 9: Virtual Memory 	tom exit should be exit(2)
 p. 829, Figure 9.26. The kernel portion of the add Posted 05/08/2018. Godmar Bak p. 831, bottom of the page, "fvm_start" should be Posted 03/01/2016. Ruth Anderson p. 842, first paragraph. The heap shown in Figure Posted 06/26/2016. Ruth Anderson 	e 9.34 consists of 18 words, not 16 words.
o p. 873, Section 9.11.6, paragraph 2. The explana	tion for why the binheapDelete function is buggy is correct for the version of ANSI C described in the K&R book, where the unary e. However, in more recent versions of C, and ++ have higher precedence than *. So while the given code is always incorrect, the be expressed more clearly as 16 E.
 p. 884, solution code. The #endif on line 12 sho <i>Posted 07/30/2018. Wenjun Huang</i> Chapter 10: System-Level I/O p. 893, Second bullet point. The relative path nan <i>Posted 06/26/2016. Mathieu Bordere</i> 	ne should be/droh/hello.c rather than/home/droh/hello.c.
 Posted 07/31/2016. Dave Ohlsson Chapter 11: Network Programming p. 949, Aside. "Marc Andreesen" should be "Ma 	ain() should check that arge is at least equal to 2 before accessing argv[1].
 Posted 07/31/2016. Dave Ohlsson p. 956, Figure 11.28. In the telnet trace, there sho Posted 06/26/2016. Laura M. Roberts p. 959, Figure 11.31. The use of multiple sprint snprintf(), vsprintf(), or vsnprintf() would cause 	ould be "connection: close" header, which is generated by the adder.c CGI program, sandwiched between lines 8 and 9. f calls to generate body violates the following rule: C99 and POSIX.1-2001 specify that the results are undefined if a call to sprintf(), copying to take place between objects that overlap (e.g., if the target string array and one of the supplied input arguments refer to the
same buffer). Posted 04/25/2019. Zeng Fan Pu and Urvi Agrawal p. 962, Figure 11.34. The use of multiple sprint Posted 04/25/2019. Zeng Fan Pu and Urvi Agrawal pp. 959 and 962. Updated the Tiny code on the Oposted 11/14/2019. Dave O'Hallaron	f calls to generate buf violates the same rule as p. 959. CS:APP Web site to fix the previous two bugs.
 p. 989, first sentence. Delete the entire sentence twaits for other threads to terminate. Posted 07/30/2018. Yuan Tang Chapter 12: Concurrent Programming 	that begins with "If the main thread calls pthread_exit, it waits for all other threads to terminate" In fact, Pthread_exit never that begins with "If the main thread calls pthread_exit, it waits for all other threads to terminate" In fact, Pthread_exit never
 Posted 07/30/2018. Yuan Tang p. 997, The text describing Figure 12.17 is corrected. The Ui instruction should be addq \$1, %r The si instruction should be movq %rdx, Posted 02/22/2018. Dr. Joann J Ordille 	dx. cnt(%rip).
 p. 1002, first box. In the declaration of sem_init Posted 07/31/2018. Dave Ohlsson p. 1015, Figure 12.31, code line 25. sem_init she Posted 07/31/2018. Dave Ohlsson p. 1023, ten lines from the bottom. "the static new Posted 07/31/2018. Dave Ohlsson 	ould be Sem_init xt variable" should be "the static next_seed variable"
 p. 1029. The definition of the mutex ordering rul order that mutexes are released does not matter, s <i>Posted 07/30/2018. Einar Rasmussen</i> Appendix A: Error Handling Index 	e is too strong. It should read simply "a program is deadlock free if each thread acquires its mutexes in the same order." In fact, the since V operations never block. The strong is deadlock free if each thread acquires its mutexes in the same order." In fact, the since V operations never block. The strong is deadlock free if each thread acquires its mutexes in the same order." In fact, the since V operations never block.
Posted 08/26/2015. Yu Zhong CS:APP3e Instructor's Manual • Chapter 9: Virtual Memory	
 p. 107, Problem 9.16. The answer for the first calis 16 bytes (lhdrlpredlsucclftrl). Thus, a minimum Posted 03/01/2016. Daniel Rushton Copyright © 2015 Randal E. Bryant and David R. O'Hallaron Recent articles from the CS:APP blog 	