DE0-CV Pin Table

FPGA: Altera Cyclone V **5CEBA4F23C7N**

Table 3-2 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description
KEY0	PIN_U7	Push-button[0]
KEY1	PIN_W9	Push-button[1]
KEY2	PIN_M7	Push-button[2]
KEY3	PIN_M6	Push-button[3]
RESET_N	PIN_P22	Push-button which connected to DEV_CLRN Pin of FPGA

Table 3-3 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]

Table 3-4 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description
LEDR0	PIN_AA2	LED [0]
LEDR1	PIN_AA1	LED [1]
LEDR2	PIN_W2	LED [2]
LEDR3	PIN_Y3	LED [3]
LEDR4	PIN_N2	LED [4]
LEDR5	PIN_N1	LED [5]
LEDR6	PIN_U2	LED [6]
LEDR7	PIN_U1	LED [7]
LEDR8	PIN_L2	LED [8]
LEDR9	PIN_L1	LED [9]

Table 3-5 Pin Assignment of 7-segment Displays

Signal Name	FPGA Pin No.	Description
HEX00	PIN_U21	Seven Segment Digit 0[0]
HEX01	PIN_V21	Seven Segment Digit 0[1]
HEX02	PIN_W22	Seven Segment Digit 0[2]
HEX03	PIN_W21	Seven Segment Digit 0[3]
HEX04	PIN_Y22	Seven Segment Digit 0[4]
HEX05	PIN_Y21	Seven Segment Digit 0[5]
HEX06	PIN_AA22	Seven Segment Digit 0[6]
HEX10	PIN_AA20	Seven Segment Digit 1[0]
HEX11	PIN_AB20	Seven Segment Digit 1[1]
HEX12	PIN_AA19	Seven Segment Digit 1[2]
HEX13	PIN_AA18	Seven Segment Digit 1[3]
HEX14	PIN_AB18	Seven Segment Digit 1[4]
HEX15	PIN_AA17	Seven Segment Digit 1[5]
HEX16	PIN_U22	Seven Segment Digit 1[6]
HEX20	PIN_Y19	Seven Segment Digit 2[0]
HEX21	PIN_AB17	Seven Segment Digit 2[1]
HEX22	PIN_AA10	Seven Segment Digit 2[2]
HEX23	PIN_Y14	Seven Segment Digit 2[3]
HEX24	PIN_V14	Seven Segment Digit 2[4]
HEX25	PIN_AB22	Seven Segment Digit 2[5]
HEX26	PIN_AB21	Seven Segment Digit 2[6]
HEX30	PIN_Y16	Seven Segment Digit 3[0]
HEX31	PIN_W16	Seven Segment Digit 3[1]
HEX32	PIN_Y17	Seven Segment Digit 3[2]
HEX33	PIN_V16	Seven Segment Digit 3[3]
HEX34	PIN_U17	Seven Segment Digit 3[4]
HEX35	PIN_V18	Seven Segment Digit 3[5]
HEX36	PIN_V19	Seven Segment Digit 3[6]
HEX40	PIN_U20	Seven Segment Digit 4[0]
HEX41	PIN_Y20	Seven Segment Digit 4[1]
HEX42	PIN_V20	Seven Segment Digit 4[2]
HEX43	PIN_U16	Seven Segment Digit 4[3]
HEX44	PIN_U15	Seven Segment Digit 4[4]
HEX45	PIN_Y15	Seven Segment Digit 4[5]
HEX46	PIN_P9	Seven Segment Digit 4[6]
HEX50	PIN_N9	Seven Segment Digit 5[0]
HEX51	PIN_M8	Seven Segment Digit 5[1]
HEX52	PIN_T14	Seven Segment Digit 5[2]
HEX53	PIN_P14	Seven Segment Digit 5[3]
HEX54	PIN_C1	Seven Segment Digit 5[4]
HEX55	PIN_C2	Seven Segment Digit 5[5]
HEX56	PIN_W19	Seven Segment Digit 5[6]

Table 3-6 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description
CLOCK_50	PIN_M9	50 MHz clock input(Bank 3B)
CLOCK2_50	PIN_H13	50 MHz clock input(Bank 7A)
CLOCK3_50	PIN_E10	50 MHz clock input(Bank 8A)
CLOCK4_50	PIN_V15	50 MHz clock input(Bank 4A)

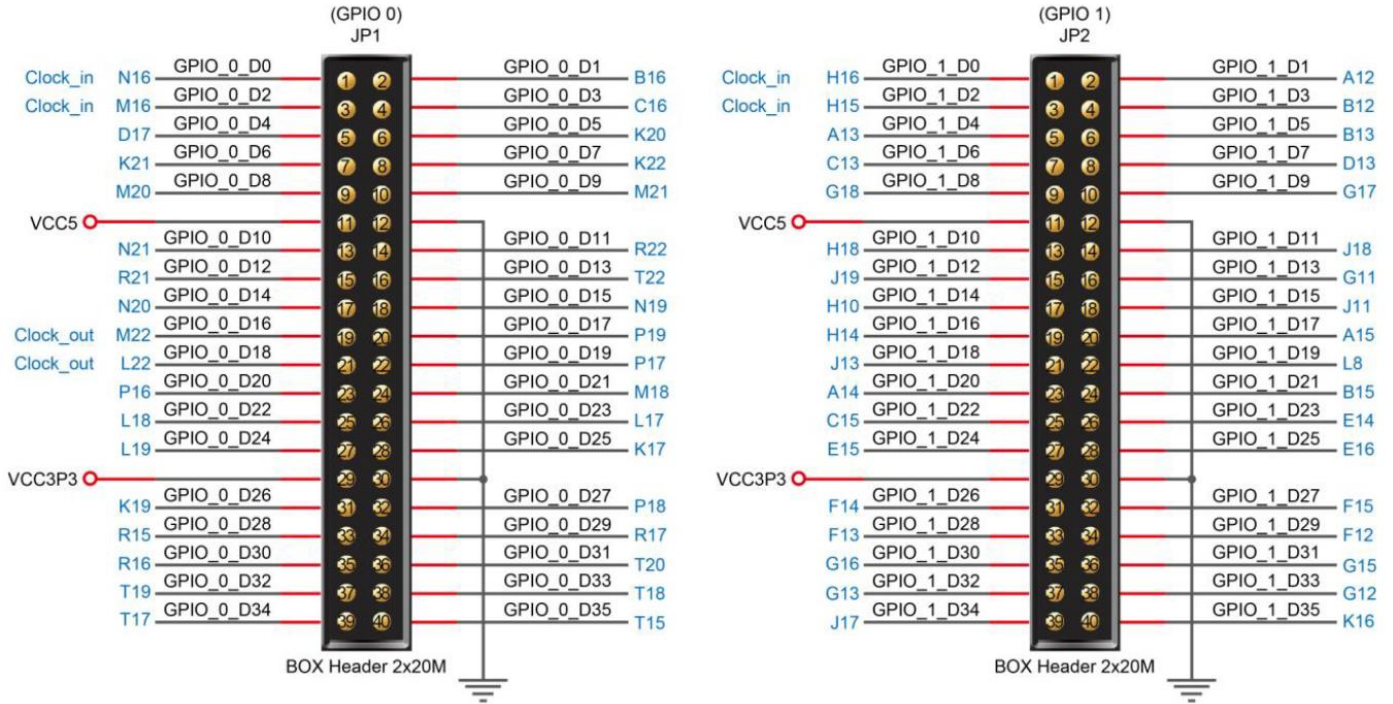Figure 3-12 I/O distribution of the expansion headers

Table 3-7 Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description
GPIO_0_D0	PIN_N16	GPIO Connection 0[0]
GPIO_0_D1	PIN_B16	GPIO Connection 0[1]
GPIO_0_D2	PIN_M16	GPIO Connection 0[2]
GPIO_0_D3	PIN_C16	GPIO Connection 0[3]
GPIO_0_D4	PIN_D17	GPIO Connection 0[4]
GPIO_0_D5	PIN_K20	GPIO Connection 0[5]
GPIO_0_D6	PIN_K21	GPIO Connection 0[6]
GPIO_0_D7	PIN_K22	GPIO Connection 0[7]
GPIO_0_D8	PIN_M20	GPIO Connection 0[8]
GPIO_0_D9	PIN_M21	GPIO Connection 0[9]
GPIO_0_D10	PIN_N21	GPIO Connection 0[10]
GPIO_0_D11	PIN_R22	GPIO Connection 0[11]
GPIO_0_D12	PIN_R21	GPIO Connection 0[12]
GPIO_0_D13	PIN_T22	GPIO Connection 0[13]
GPIO_0_D14	PIN_N20	GPIO Connection 0[14]
GPIO_0_D15	PIN_N19	GPIO Connection 0[15]
GPIO_0_D16	PIN_M22	GPIO Connection 0[16]
GPIO_0_D17	PIN_P19	GPIO Connection 0[17]
GPIO_0_D18	PIN_L22	GPIO Connection 0[18]
GPIO_0_D19	PIN_P17	GPIO Connection 0[19]
GPIO_0_D20	PIN_P16	GPIO Connection 0[20]
GPIO_0_D21	PIN_M18	GPIO Connection 0[21]
GPIO_0_D22	PIN_L18	GPIO Connection 0[22]
GPIO_0_D23	PIN_L17	GPIO Connection 0[23]
GPIO_0_D24	PIN_L19	GPIO Connection 0[24]
GPIO_0_D25	PIN_K17	GPIO Connection 0[25]
GPIO_0_D26	PIN_K19	GPIO Connection 0[26]
GPIO_0_D27	PIN_P18	GPIO Connection 0[27]
GPIO_0_D28	PIN_R15	GPIO Connection 0[28]
GPIO_0_D29	PIN_R17	GPIO Connection 0[29]
GPIO_0_D30	PIN_R16	GPIO Connection 0[30]
GPIO_0_D31	PIN_T20	GPIO Connection 0[31]
GPIO_0_D32	PIN_T19	GPIO Connection 0[32]
GPIO_0_D33	PIN_T18	GPIO Connection 0[33]
GPIO_0_D34	PIN_T17	GPIO Connection 0[34]
GPIO_0_D35	PIN_T15	GPIO Connection 0[35]

Table 3-7 Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description
GPIO_1_D0	PIN_H16	GPIO Connection 1[0]
GPIO_1_D1	PIN_A12	GPIO Connection 1[1]
GPIO_1_D2	PIN_H15	GPIO Connection 1[2]
GPIO_1_D3	PIN_B12	GPIO Connection 1[3]
GPIO_1_D4	PIN_A13	GPIO Connection 1[4]
GPIO_1_D5	PIN_B13	GPIO Connection 1[5]
GPIO_1_D6	PIN_C13	GPIO Connection 1[6]
GPIO_1_D7	PIN_D13	GPIO Connection 1[7]
GPIO_1_D8	PIN_G18	GPIO Connection 1[8]
GPIO_1_D9	PIN_G17	GPIO Connection 1[9]
GPIO_1_D10	PIN_H18	GPIO Connection 1[10]
GPIO_1_D11	PIN_J18	GPIO Connection 1[11]
GPIO_1_D12	PIN_J19	GPIO Connection 1[12]
GPIO_1_D13	PIN_G11	GPIO Connection 1[13]
GPIO_1_D14	PIN_H10	GPIO Connection 1[14]
GPIO_1_D15	PIN_J11	GPIO Connection 1[15]
GPIO_1_D16	PIN_H14	GPIO Connection 1[16]
GPIO_1_D17	PIN_A15	GPIO Connection 1[17]
GPIO_1_D18	PIN_J13	GPIO Connection 1[18]
GPIO_1_D19	PIN_L8	GPIO Connection 1[19]
GPIO_1_D20	PIN_A14	GPIO Connection 1[20]
GPIO_1_D21	PIN_B15	GPIO Connection 1[21]
GPIO_1_D22	PIN_C15	GPIO Connection 1[22]
GPIO_1_D23	PIN_E14	GPIO Connection 1[23]
GPIO_1_D24	PIN_E15	GPIO Connection 1[24]
GPIO_1_D25	PIN_E16	GPIO Connection 1[25]
GPIO_1_D26	PIN_F14	GPIO Connection 1[26]
GPIO_1_D27	PIN_F15	GPIO Connection 1[27]
GPIO_1_D28	PIN_F13	GPIO Connection 1[28]
GPIO_1_D29	PIN_F12	GPIO Connection 1[29]
GPIO_1_D30	PIN_G16	GPIO Connection 1[30]
GPIO_1_D31	PIN_G15	GPIO Connection 1[31]
GPIO_1_D32	PIN_G13	GPIO Connection 1[32]
GPIO_1_D33	PIN_G12	GPIO Connection 1[33]
GPIO_1_D34	PIN_J17	GPIO Connection 1[34]
GPIO_1_D35	PIN_K16	GPIO Connection 1[35]