```vhdl
architecture structural of control_unit is
    ...
    ...
        begin
            process(clock, reset) is
                if reset = '1' then
                * Joga no fetch
                elif mem_enable = '1' and mem_busy = '0' then
                    if mem_we = '1'
                        * Operações de escrita
                    elif mem_we = '0' and mem_busy = '0' then
                    * Operações sem escrita
                    end if;
                end if;
            end process

        with husted select
            *_en <= '0' when '1',
                '1' when others;                    ?.

end architecture structural;
```

signals:

IM_star;

FSM:

fetch

mem_a_addr_src = '1'

alu_shfimm_src = '0'
alu_b_src = "00"
alu_a_src = "00"

alu_op = "001"
pc_en = '1'
pc_src = '0'

fetch
decode
execute
write