TE2003B
SoC design: Computer organization & architecture
Course introduction

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Objective

Main objective

- To analyse, design and successfully implement basic embedded system.

Professors

- Dr. Isaac Pérez Andrade (Intel).
- Dr. Gilberto Ochoa Ruiz (ITESM).
- Dr. Luis Fernando González Pérez (A2E Technologies).

Lecturer's background

Dr. Isaac Pérez Andrade

- **BSc Electronics (ITE)** - ITESM GDA - 2009.
- **MSc System-on-Chip** - University of Southampton, UK - 2011.
- **PhD Electronic Eng.** - University of Southampton, UK - 2016.
  - Timing-error-tolerant iterative decoders.
  - Digital integrated circuits design for LTE and 4G wireless communications standards.
- **Digital IC Design Engineer** - Accelercomm, Southampton, UK - 2017 - 2018.
  - Analysis, design and implementation of error correction code algorithms for 5G New Radio standard.
- **IP logic designer** - Intel GDC - 2018 - present.

Course methodology, structure, & evaluation

Methodology

- Project-based learning.
- Self-based learning.
  - Prepare before lectures by completing reading materials.
  - Independent research.
- Office hours for solving specific questions.
  - Office hours are intended to provide quick guidance.
  - Students should not expect lecturers to solve their assignments.

Structure

- TE2003B System-on-Chip design comprises four modules.
  1. **Computer organisation & architecture.**
     - Prof. Isaac Pérez Andrade - Weeks 7 - 11.
  2. Microcontrollers.
     - Prof. Gilberto Ochoa - Weeks 7 - 11.
  3. Real-Time Operating System (RTOS).
     - Prof. Gilberto Ochoa - Weeks 13 - 17.
  4. Embedded Linux.
     - Prof. Luis González Weeks 13 - 17.
- Over the ten weeks of this course, you will develop a final project in which you will apply topics learned in the four modules described above.
- Intel will provide guidance over selected engineering topics.

Course chronogram

Hrs	s07	s08	s09*	s10	s11*	s12	s13	s14	s15*	s16	s17*
1	1.1	1.3	1.4	1.5			3.1	3.3	3.5	3.7	
2	1.1	1.3	1.4	1.5			3.1	3.3	3.5	3.7	
3	1.2	1.3	1.4	1.5			3.2	3.4	3.6	3.8	
4	1.2	1.3	1.4	1.5			3.2	3.4	3.6	3.8	
5											
6											
7											
8											
9											
10	2.1	2.3	2.4	2.4			4.1	4.3	4.4	4.5	
11	2.1	2.3	2.4	2.4			4.1	4.3	4.4	4.5	
12	2.2	2.3	2.4	2.4			4.2	4.3	4.4	4.5	
13	2.2	2.3	2.4	2.4			4.2	4.3	4.4	4.5	
14	2.2	2.3	2.4	2.4			4.2	4.3	4.4	4.5	
15	2.2	2.3	2.4	2.4			4.2	4.3	4.4	4.5	
16	2.2	2.3	2.4	2.4			4.2	4.3	4.4	4.5	

- Course topics are detailed in Canvas.
  https://experiencia21.tec.mx/courses/140282/modules

Evaluation

Modules	45%
Project	55%
TOTAL	**100%**

Evaluation

Modules evaluation

Module	Weight
Computer organisation & architecture	15%
Microcontrollers	15%
RTOS	10%
Embedded Linux	5%
TOTAL	**45%**

Project & evidences evaluation

Evidence	Competences	Weight
Evidence 1	STE0101.B, STE0204.B, STE0302.A	25%
Evidence 2	STE0102.B, STE0103.B, STE0303.A, SEG0702.B	30%
	TOTAL	**55%**

Competences

- **STE0101B.** Modela sistemas embebidos con capacidad de interacción que dan solución a una problemática determinada.
- **STE0102B.** Implementa sistemas embebidos considerando especificaciones y restricciones del entorno.
- **STE0103B.** Valida el funcionamiento de sistemas embebidos tomando en cuenta la eficiencia, costos y estándares.
- **STE0204B.** Elige la unidad de procesamiento acorde a requerimientos.
- **STE0302B.** Selecciona el protocolo de comunicación de acuerdo a su aplicación.
- **STE0303A.** Genera la interacción inteligente entre una unidad de procesamiento y sus periféricos.
- **SEG0702B.** Evalúa diversas tecnologías, con apertura a la búsqueda e implementación de alternativas relevantes en la transformación de la práctica profesional.

Computer organisation & architecture contents

Computer organisation & architecture contents

1. Instruction set architecture.
2. Computer arithmetic.
3. Processor: Datapath and control.
4. Pipeline.
5. Memory hierarchy and Input/Output (IO) interfaces.

Course policies

Policies

Web conference lectures

- Just as in face-to-face lectures, our behaviour shall be based on discipline, responsibility and respect.
- Lectures shall commence at 07:10 and end at 08:50 hours.
- Students are encouraged to join the zoom session on time.
- Students **must** have their webcam on during the lecture.
- Lectures will be recorded. Please remind your lecturer if you notice the lecture is not being recorded.
- Adhering to Tecnólogico de Monterrey ethics code, students pledge that their behaviour shall be ruled by academic honesty.

Policies

Coursework and assignments

- For individual assignments, students are encouraged to discuss ideas with other students. However, it is expected that each student submits their own individual and original work.
- Students should not submit work from external sources such as websites, books or other students.
- For group assignments, the policy for individual assignments apply. Moreover, students must disclose the collaboration percentage of each team member.
- For both individual and group assignments, **if there's evidence of students submitting other work than their own, the involved students will automatically fail the assignment**.

Policies

Coursework and assignments

- **Late submissions will not be tolerated.**
- **Late submissions will be automatically assigned a grade of 0.**
- **If a submission is on time but not in the specified format, the submission will be penalised by 30%.**
  - For example, if an activity is requested to be submitted through Canvas but a student submits their work through email or Google drive, the possible maximum grade for the submission will 70.

Resources

Suggested literature

- J. L. Hennessy and D. A. Patterson, *Computer architecture and design: The hardware and software interface - ARM edition*, Morgan Kaufmann, 2017.
- S. L. Harris and D. M. Harris, *Digital design and computer architecture - ARM edition*, Morgan Kaufmann, 2016.
- J. Yiu, *The definitive guide to ARM Cortex-M0 and Cortex-M0+ processors*, Second edition, Elsevier, 2015.

All these resources are available in *Biblioteca Digital* (editions may vary).

Contact information

- Zoom
  - Course (lectures) https://itesm.zoom.us/j/6215756089.
  - Personal (asesorías) https://itesm.zoom.us/j/7558517847.
- Remind: socgdaarq
- Email: isaac.perez.andrade@tec.mx
- Office hours (asesorías): No fixed schedule. However, we can schedule face-to-face sessions as needed, please send an email or Remind message with your request and proposed schedule at least 24 hours in advance.

System-on-Chips

System-on-Chip (SoC)

- A single Integrated Circuit (IC), also known as *chip*, that *integrates* several subsystems and components that are part of a computing system.

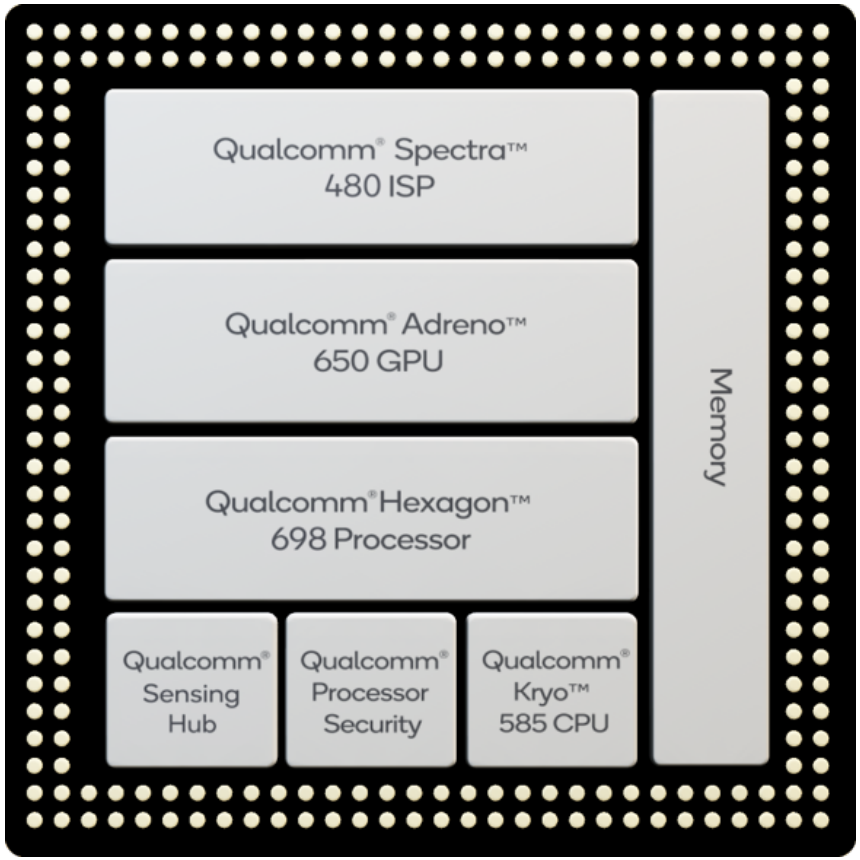

Figure 1: Qualcomm Snapdragon 865+ 5G SoC.

System-on-Chips

- How do SoCs differ from the following?
  - Microprocessors (μPs).
  - Microcontrollers (μCs).
  - Embedded systems.
  - Field-Programmable Gate Arrays (FPGAs).
  - Application Specific Integrated Circuits (ASICs).
- Despite its name, this course will focus on **embedded systems**, which are a vital part of consumer electronics.
- Have a look at `https://www.ifixit.com/Teardown` in order to observe the complexity of various consumer electronic products.