Low-power design techniques

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Power in ICs

Definitions

- **Dynamic power**. Power dissipated in Integrated Circuits (ICs) due to switching activity.
  - Charging and discharging load capacitances.
  - Short-circuit current, when both pMOS and nMOS transistors are on for a brief period.
- **Static power**. Power dissipated in ICs even when there is no switching activity.
  - Gate and junction leakages.

Dynamic power

- Dynamic power is described in Equation (1)

$$P_{dyn} = \alpha C_L V_{DD}^2 f_{clk} \tag{1}$$

where

$\alpha \in [0, 1]$ is a switching activity factor respect to a clock source, *i.e.*, clock signals have $\alpha = 1$. It determines the probability of a net transitioning from 0 to 1,

C_L is the capacitive load,

V_{DD}^2 is the supply voltage,

f_{clk} is the clock frequency.

Low-power design techniques

- **Dynamic Voltage and Frequency Scaling (DVFS)** for reducing dynamic power.
- **Clock gating** for reducing dynamic power .
- **Power gating** for reducing static power.

Dynamic Voltage and Frequency Scaling

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- From Equation (1), we can see that the supply voltage has a quadratic effect on power dissipation.

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  As a result, we may simply lower V_{DD}.
- Example: What is the power saving in a system that reduces V_{DD} from 1 V to 0.85 V?

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- Example: What is the power saving in a system that reduces V_{DD} from 1 V to 0.85 V?

$$\frac{P_{dyn2}}{P_{dyn1}} = \frac{\alpha C_L \cdot 0.85^2 \cdot f_{clk}}{\alpha C_L \cdot 1^2 \cdot f_{clk}} = 0.7225$$

  In other words,

$$P_{dyn2} = 0.7225 \times P_{dyn1}$$

Dynamic Voltage and Frequency Scaling

- In the previous example, we are reducing power consumption by 27.75% by reducing only 15% of the power supply.
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- However, we can't simply reduce V_{DD} without consequences.
- Propagation delays in Complementary Metal Oxide Semiconductor (CMOS) transistors are an inversely proportional function of V_{DD}.
  - Larger V_{DD} values yield smaller propagation delays.
- As a result of this, f_{clk} must be adapted.

Dynamic Voltage and Frequency Scaling

- DVFS consists of modifying both V_{DD} and f_{clk} according to the processing and power requirements of the system.

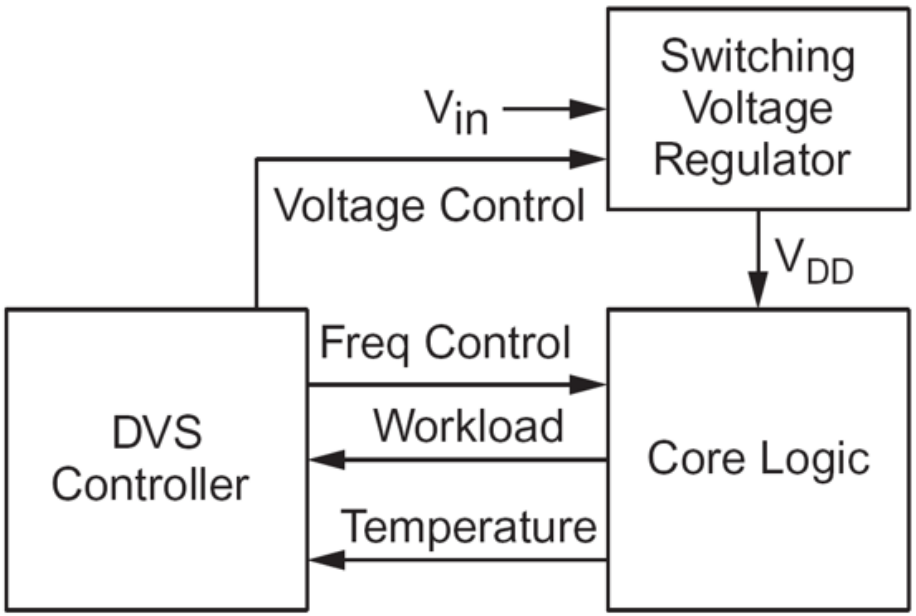

Figure 1: DVFS basic block diagram.

Dynamic Voltage and Frequency Scaling

- Voltage and frequency pairs are usually stored inside the DVFS controller.
- These values may be pre-loaded or may be calculated on-the-fly using performance statistics through performance evaluation algorithms.

Clock Gating

Clock gating

- Another factor that can be easily modified in Equation (1) is the switching activity α.

$$P_{dyn} = \alpha C_L V_{DD}^2 f_{clk}$$

- This may be achieved at the algorithmic level or at the Register-Transfer Level (RTL) level.
- From the circuit point of view, we can disable the clock signal in certain blocks within the IC that are idle.
- This prevents any switching activity and prevents and dynamic power dissipation.

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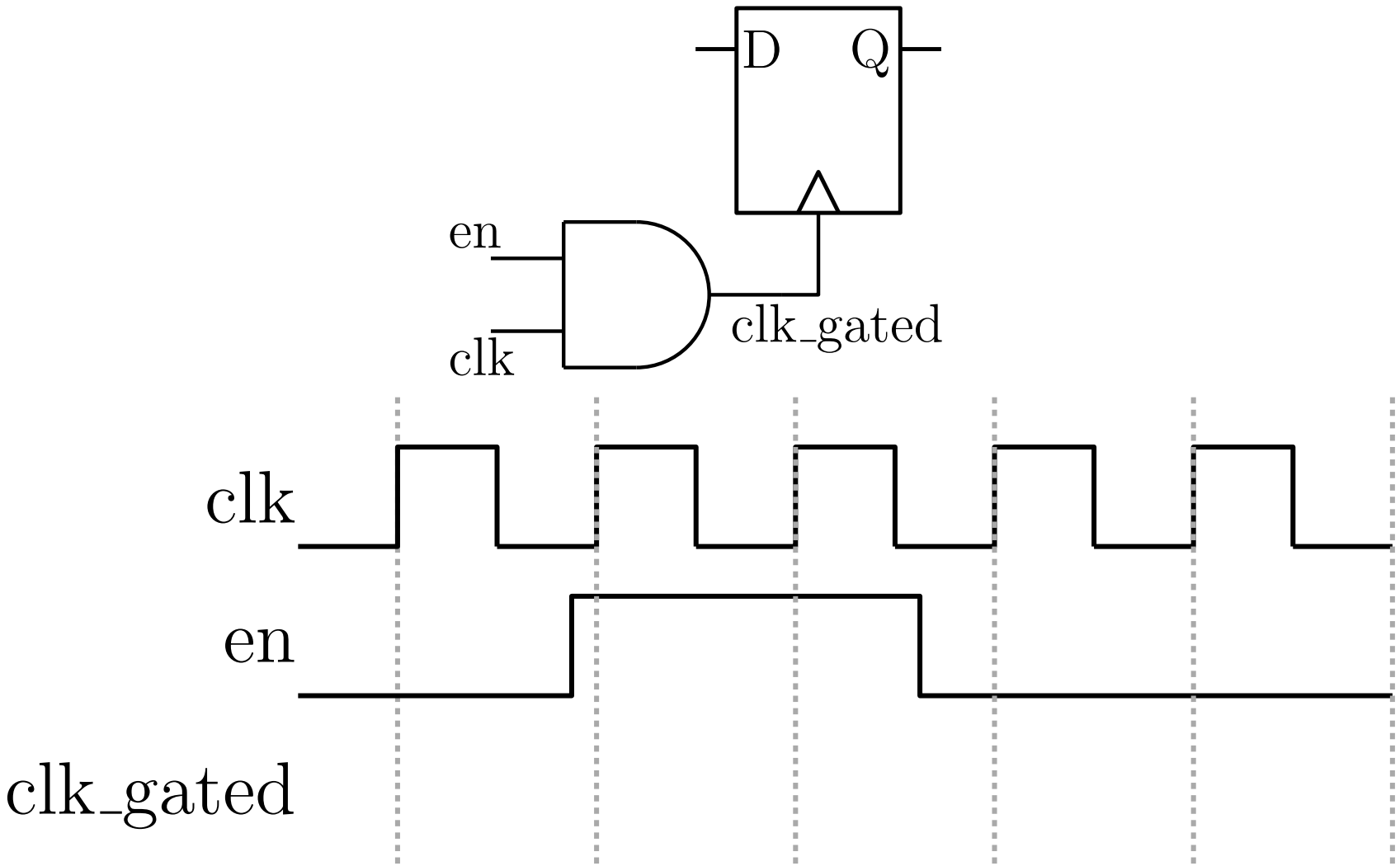

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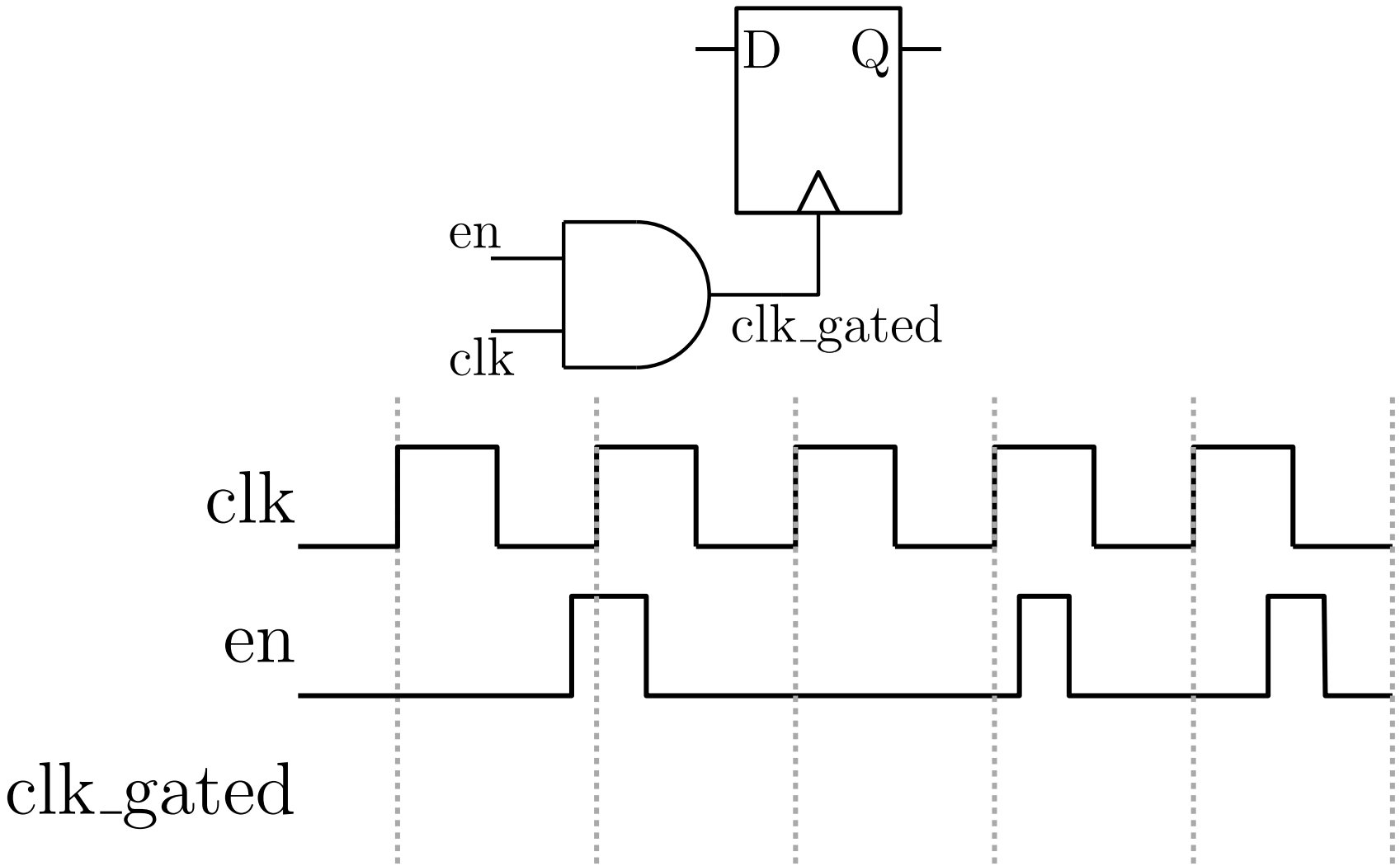

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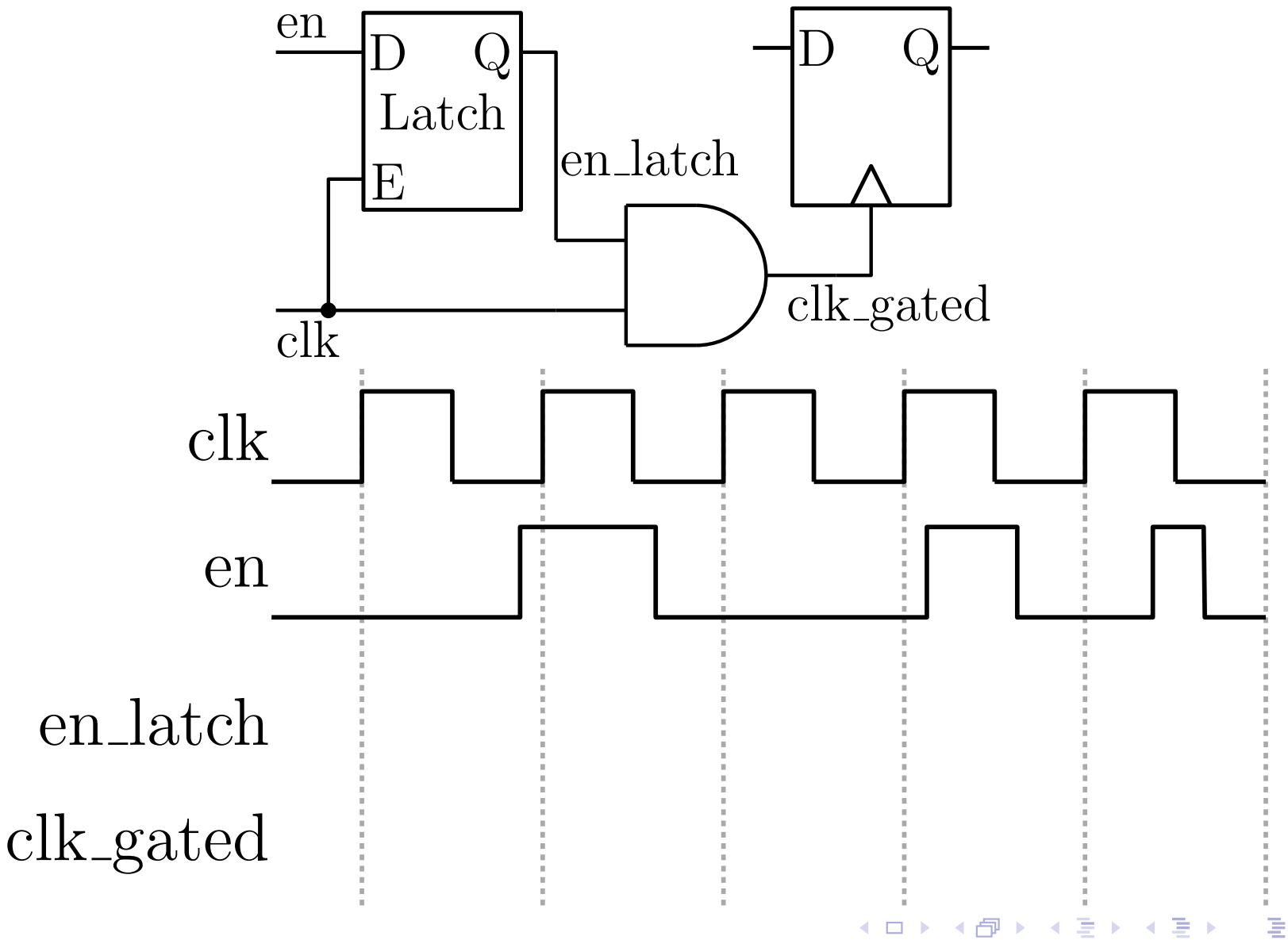

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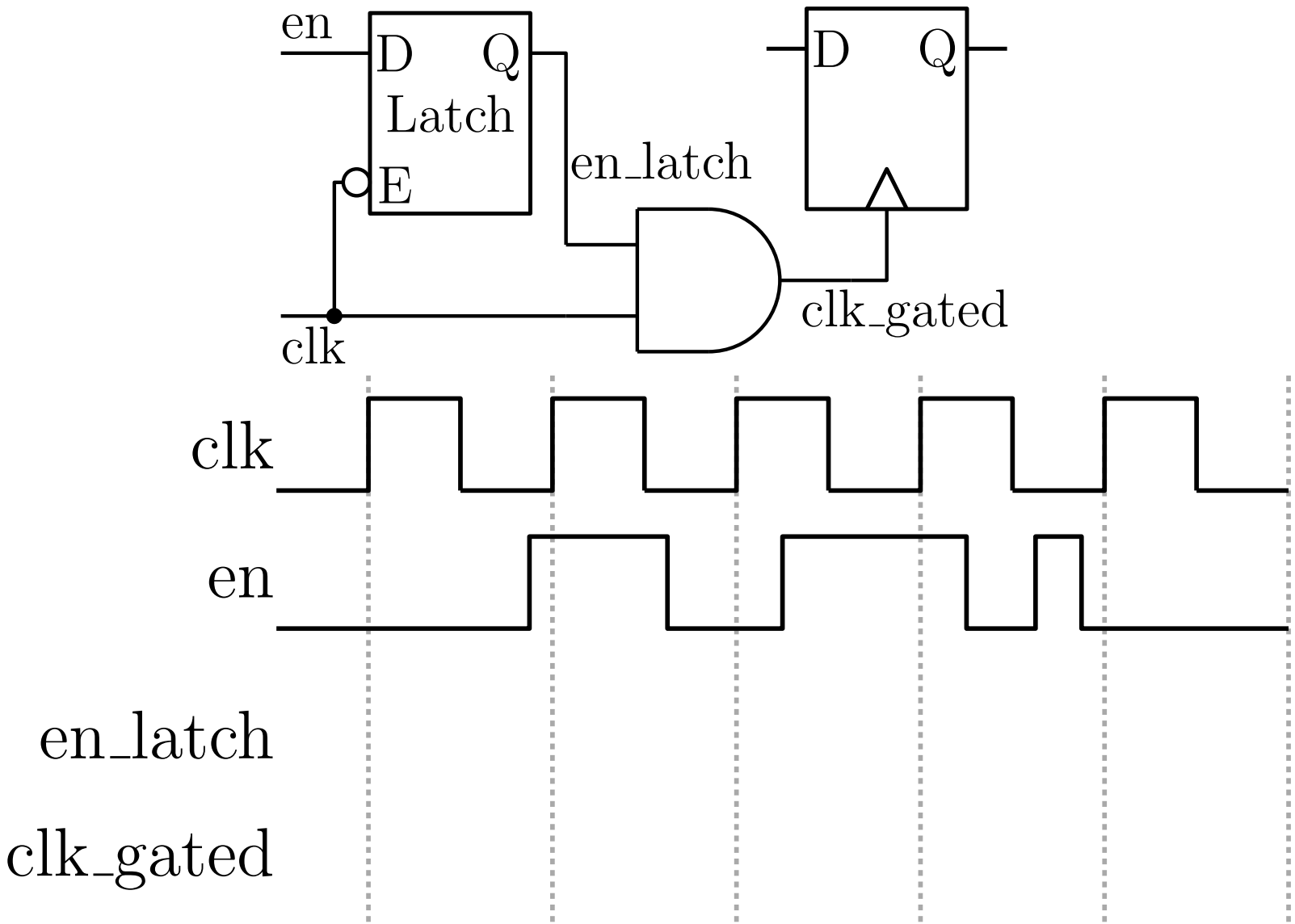

Clock gating

- Fortunately, designers don't have to connect latches, `AND` and flip-flops together every time they want to employ clock gating.
- Standard cell libraries provide clock gating cells.

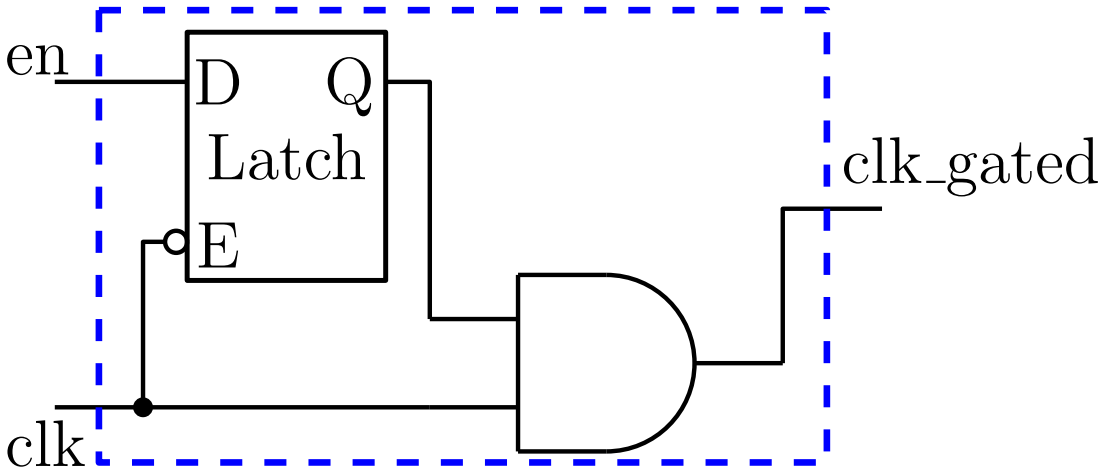

Figure 2: Clock cell gate.

- Moreover, modern synthesizers are clever enough to detect and infer clock-gating cells when reading RTL.

Clock gating

- Clock gating may be easily implemented using a combination of RTL coding style and synthesizer commands.

Clock gating in RTL

```
always_ff @ (posedge clk)
    if(enable)
        Q <= D;
```

- Synthesis tools such as Synopsys Design Compiler use commands such as

```
set_clock_gating_style -global -minimum_bitwidth <value>
```

Power Gating

Power gating

- Power gating consists on switching off entire parts of the IC by temporarily disconnecting it from the supply rail.

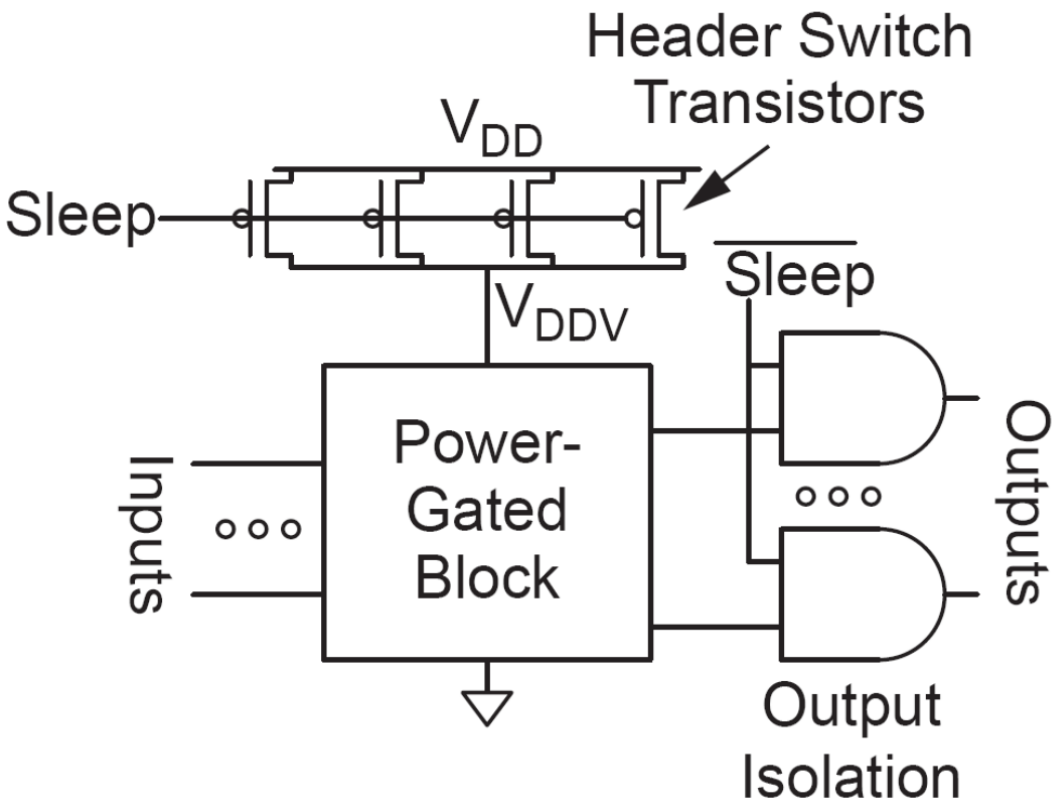

Figure 3: Power gating basic block diagram.

Power gating

- Header switch requires careful design.
  - Low leakage.
  - Fast switching on times.
- This technique is only efficient when blocks must be turned off for long periods.
- When a block is turned off, its state must be saved in order to allow resuming execution.