Table 44. PCI Express Errors Logging Error Format

Byte	Field	Value	Description
1 : 2	Record ID	XXXXh	ID used for SEL Record access
3	Record Type	02h	02h = system event record
4 : 7	Time Stamp	XXXXXXXXh	Time when event was logged
8 : 9	Generator ID	0001h	Generated by BIOS, LSB first. E.g. the Generator ID for BIOS is 1 decimal, which is 1h, which would be stored in this record as 01h, 00h for bytes 8 through 9, respectively.
10	EvM Rev	04h	Event Message Format Revision. 04h for this specification
11	Sensor Type	13h	Sensor type code for sensor that generated the event 13h = Critical interrupt
12	Sensor Number	A1h	Number of Sensor that generator the event
13	Event Dir | Event Type	6Fh	Bit [7] 0 = Assert Event
			Bit [6:0] Event Type Code
14	Event Data 1	AXh	Bit [7:6] 10b
			Bit [5:4] 10b
			Bit [3:0] 04h = PCI PERR 05h = PCI SERR 07h = Bus Correctable 08h = Bus Uncorrectable 0Ah = Bus Fatal
15	Event Data 2	XXh	Bit [7:3] Device Number
			Bit [2:0] Function Number
16	Event Data 3	XXh	Bit [7:0] Bus Number

Table 45. Extended PCI Express Error Events Log format (APTIO V)

Byte	Field	Value	Description
1 : 2	Record ID	XXXXh	ID used for SEL Record access, The Record ID values 0000h and FFFFh have special meaning in the event access commands, and are not to be used as Record ID values for stored SEL Event Records.
3	Record Type	C0h	C0h = OEM timestamped
4 : 7	Time Stamp	XXXXXXXXh	Time when event was logged (automatically added by SEL device). LS byte first.
8 : 10	Manufacturer ID	1C4Ch	Quanta ID Manufacturer ID, LSB first. E.g. the Manufacturer ID for Quanta Computer Inc. is 7244 decimal, which is 1C4Ch, which would be stored in this record as 4Ch, 1Ch, 00h for bytes 8 through 10,

			respectively.
11 : 12	VID	XXXXh	Record Vendor ID of the PCIe device with error detected, LSB first. E.g. the Vendor ID for Intel PCIE device is 32902 decimal, which is 8086h, which would be stored in this record as 86h, 80h for bytes 11 through 12, respectively.
13 : 14	DID	XXXXh	Record Device ID of the PCIe device with error detected, LSB first. E.g. the Device is 3592 decimal, which is 0E08h, which would be stored in this record as 08h, 0Eh for bytes 13 through 14, respectively.
15	Slot Number	XXh	Slot Number If high nibble was zero, e.g. 0x02, it is non-riser slot, so it should be slot2. If high nibble was not zero, e.g. 0x21, it is riser slot, so it should be slot 2-1.
16	PCIE error ID	XXh	Log the PCIE error. (Table 46. Error ID)

0x00~0x1F ->AER PCIE correctable status
0x20~0x4F ->AER PCIE uncorrectable status.
0x50~0x5F ->AER PCIE root port error status.
0x60~0x7F -> Silicon specific correctable PCIe error.
0x80~0x9F -> Silicon specific uncorrectable PCIe error.

Table 46. Error ID (APTIO V)

ID	Error	Default Error Severity	Transaction Response	Default Error Logging
00	Receiver Error	0	Respond per PCI Express specification	CORERRSTS
01	Bad TLP	0	Respond per PCI Express specification	CORERRSTS
02	Bad DLLP	0	Respond per PCI Express specification	CORERRSTS
03	Replay Number Rollover	0	Respond per PCI Express specification	CORERRSTS
04	Replay Timer Timeout Status	0	Respond per PCI Express specification	CORERRSTS
05	Advisory Non-Fatal Error Status	0	Respond per PCI Express specification	CORERRSTS
06	Corrected Internal Error Status	0	Respond per PCI Express specification	CORERRSTS
07	Header Log Overflow Status	0	Respond per PCI Express specification	CORERRSTS
20	Data Link Protocol Error Status	1	Respond per PCI Express specification	UNCERRSTS

21	Surprise Down Error Status	1	Respond per PCI Express specification	UNCERRSTS
22	Poisoned TLP Status	1	Respond per PCI Express specification	UNCERRSTS
23	Flow Control Protocol Error Status	1	Respond per PCI Express specification	UNCERRSTS
24	Completion Timeout Status	1	Respond per PCI Express specification	UNCERRSTS
25	Completer Abort Status	1	Respond per PCI Express specification	UNCERRSTS
26	Unexpected Completion Status	1	Respond Per PCI Express Specification	UNCERRSTS
27	Receiver Overflow Status	1	Respond per PCI Express specification	UNCERRSTS
28	Malformed TLP Status	1	Respond per PCI Express specification	UNCERRSTS
29	ECRC Error Status	1	Respond per PCI Express specification	UNCERRSTS
3A	Unsupported Request Error Status	1	Respond per PCI Express specification	UNCERRSTS
3B	ACS Violation Status	1	Respond per PCI Express specification	UNCERRSTS
3C	Uncorrectable Internal Error Status	1	Respond Per PCI Express Specification	UNCERRSTS
3D	MC Blocked TLP Status	1	Respond Per PCI Express Specification	UNCERRSTS
3E	AtomicOp Egress Blocked Status	1	Respond Per PCI Express Specification	UNCERRSTS
3F	TLP Prefix Blocked Error Status	1	Respond Per PCI Express Specification	UNCERRSTS
50	Received ERR_NONFATAL Message from downstream device	0	Respond per PCI Express specification	RPERRSTS
51	Received ERR_FATAL message from downstream device	1	Respond Per PCI Express Specification	RPERRSTS
52	Received ERR_FATAL message from downstream device	2	Respond Per PCI Express Specification	RPERRSTS
60	pci_link_bandwidth _changed_status	0	Xp Correctable error status	XPCORERRSTS
80	outbound_switch_fifo_data_parity_error _detected	1	Xp Uncorrectable error status	XPUNCERRSTS
81	sent_completion_with_completer_abort	1	Xp Uncorrectable error status	XPUNCERRSTS

82	sent_completion_with_unsupported_request	1	Xp Uncorrectable error status	XPUNCERRSTS
83	received_pcie_completion_with_ca_status	1	Xp Uncorrectable error status	XPUNCERRSTS
84	received_pcie_completion_with_ur_status	1	Xp Uncorrectable error status	XPUNCERRSTS
85	received_msi_writes _greater _than _a _dword_data	1	Xp Uncorrectable error status	XPUNCERRSTS
86	outbound _poisoned _data	1	Xp Uncorrectable error status	XPUNCERRSTS
0xFF	N/A		N/A	

11.1.3.3 POST Error Messages and Beep Codes

The system BIOS displays error messages on the video screen. Before video initialization, beep codes inform the user of errors. POST error codes are logged in the event log. The BIOS displays POST error codes on the video monitor.

Whenever possible, the BIOS will output the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes are reported by the system BIOS.

11.1.3.4 Power On Self Test (POST) Error Log Format Convention

Errors detected during POST. The BIOS downloads the system date and time to the BMC during POST and logs a boot event. Software that parses the event log should not treat the boot event as an error.

Table 47. POST Error Events Log Format

Byte	Field	Value	Description
1 : 2	Record ID	XXXXh	ID used for SEL Record access
3	Record Type	C1h	02h = system event record
4 : 7	Time Stamp	XXXXXXXXh	Time when event was logged
8 : 9	Generator ID	0001h	Generated by BIOS, LSB first. E.g. the Generator ID for BIOS is 1 decimal, which is 1h, which would be stored in this record as 01h, 00h for bytes 8 through 9, respectively.
10	EvM Rev	04h	Event Message Format Revision. 04h for this specification
11	Sensor Type	0Fh	Sensor type code for sensor that generated the event
12	Sensor Number	9Eh	Number of Sensor that generator the event
13	Event Dir | Event Type	6Fh	Bit 7 0 = Assert Event Bit 6:0 Event Type Code