

# 10520 CS410001 - Computer Architecture 2017

## Appendix C-1 - Output Samples for Project 1

Please refer to the specified output format to generate your output report. Since we are using a script to automatically check your results, **if the format does not match with our golden results, yours will be judged as incorrect and get no points.** You are encouraged to double check your results on the open test cases using the released golden simulator.

### Format:

cycle (cycle index in decimal representation)

\$00: 0x(content in hexadecimal digits) # note that there is a space between ":" and "0x"

\$01: 0x(content in hexadecimal digits)

...

... (other registers' contents)

...

\$31: 0x(content in hexadecimal digits)

\$HI: 0x(content the product of high 32 bits)

\$LO: 0x(content the product of low 32 bits)

PC: 0x(content in hexadecimal digits)

(2 space lines here)

Note that comments are here for your understanding; they should not appear in your output files. If you have any doubts or questions, please check with TA's.

Be noted that you should dump out the contents of registers **before** executing the instruction at each checkpoint. If the content of any register does not change from the previous cycle, then do not output the register. For cases that all registers change no values, then output only the cycle index and PC count.

The following is the content of snapshot.rpt after executing the sample inputs in *Appendix B*.

### snapshot.rpt:

cycle 0

\$00: 0x00000000

\$01: 0x00000000

\$02: 0x00000000

\$03: 0x00000000

\$04: 0x00000000

\$05: 0x00000000

\$06: 0x00000000

\$07: 0x00000000

\$08: 0x00000000

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\$09: 0x00000000  
\$10: 0x00000000  
\$11: 0x00000000  
\$12: 0x00000000  
\$13: 0x00000000  
\$14: 0x00000000  
\$15: 0x00000000  
\$16: 0x00000000  
\$17: 0x00000000  
\$18: 0x00000000  
\$19: 0x00000000  
\$20: 0x00000000  
\$21: 0x00000000  
\$22: 0x00000000  
\$23: 0x00000000  
\$24: 0x00000000  
\$25: 0x00000000  
\$26: 0x00000000  
\$27: 0x00000000  
\$28: 0x00000000  
\$29: 0x00000400  
\$30: 0x00000000  
\$31: 0x00000000  
\$HI: 0x00000000  
\$LO: 0x00000000  
PC: 0x00000000

cycle 1

PC: 0x00000004

cycle 2

PC: 0x00000008

cycle 3

\$10: 0x00000001

PC: 0x0000000C

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cycle 4

PC: 0x00000010

cycle 5

PC: 0x00000014

cycle 6

\$09: 0x00000001

PC: 0x00000018

cycle 7

PC: 0x00000008

cycle 8

PC: 0x0000000C

cycle 9

PC: 0x00000010

cycle 10

\$08: 0x00000001

PC: 0x00000014

cycle 11

\$09: 0x00000002

PC: 0x00000018

cycle 12

PC: 0x00000008

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cycle 13

PC: 0x0000000C

cycle 14

PC: 0x00000010

cycle 15

\$08: 0x00000003

PC: 0x00000014

cycle 16

\$09: 0x00000003

PC: 0x00000018

cycle 17

PC: 0x00000008

cycle 18

\$10: 0x00000000

PC: 0x0000000C

cycle 19

PC: 0x0000001C

cycle 20

PC: 0x00000002