10520 CS410001 - Computer Architecture 2017
Appendix C-3 - Sample Output for Project 3

Please follow the specified format to generate *report.rpt*. For *snapshot.rpt*, please refer to *project_1.doc* and *Appendix C-1*, "*Sample Output for Project 1*." **You must precisely follow the specified format, or your result will be treated as incorrect!**

You should list the total hit/miss number of ICache, DCache, ITLB, DTLB, IPageTable, DPagetable

Example: Test case

```
addi $4 $0 4
addi $8 $0 12
beq $8 $1 4
lw $2 0($1)
sw $2 12($1)
add $1 $1 $4
j 2
add $8 $8 $8
add $1 $0 $0
beq $8 $1 4
lw $3 0($1)
add $1 $1 $4
j 9
halt
halt
halt
halt
halt
```

Sample Output File:

```
ICache :
# hits: 25
# misses: 21

DCache :
# hits: 2
# misses: 10

ITLB :
# hits: 38
# misses: 8

DTLB :
# hits: 10
# misses: 2

IPageTable :
# hits: 0
# misses: 8

DPageTable :
# hits: 0
# misses: 2
```

You may use the following code we recommend to write out the total hit/miss number of each component:

```
fprintf( fptr_report, "ICache :\n");
fprintf( fptr_report, "# hits: %u\n", hits );
fprintf( fptr_report, "# misses: %u\n\n", misses );
fprintf( fptr_report, "DCache :\n");
fprintf( fptr_report, "# hits: %u\n", hits );
fprintf( fptr_report, "# misses: %u\n\n", misses );
fprintf( fptr_report, "ITLB :\n");
fprintf( fptr_report, "# hits: %u\n", hits );
```

```
fprintf( fptr_report, "# misses: %u\n\n", misses );
fprintf( fptr_report, "DTLB :\n");
fprintf( fptr_report, "# hits: %u\n", hits );
fprintf( fptr_report, "# misses: %u\n\n", misses );
fprintf( fptr_report, "IPageTable :\n");
fprintf( fptr_report, "# hits: %u\n", IPageTable.hitNum );
fprintf( fptr_report, "# misses: %u\n\n", IPageTable.missNum );
fprintf( fptr_report, "DPageTable :\n");
fprintf( fptr_report, "# hits: %u\n", DPageTable.hitNum );
fprintf( fptr_report, "# misses: %u\n\n", DPageTable.missNum );
```

Additionally, you may want to generate a *trace.rpt* file for debugging purpose. Although it is not to be graded, a trace file can help you know what happens inside your simulator.

Format:

Cycle, Instruction :Instruction hit location ;Data hit location

(P.S: Just the lw and sw instruction have the Data hit location information)

For example "*15, sw:ICache,ITLB;DTLB*" means in the 15th cycle is execute sw instruction, this instruction are hit in both ICache and ITLB, the data what this instruction need is hit in DTLB.

trace.rpt:

```
1, addi : Disk    ;
2, addi : ITLB    ;
3, beq : Disk    ;
4, lw    : ITLB    ;    Disk
5, sw    : Disk    ;    DTLB
6, add : ITLB    ;
7, j      : Disk    ;
8, beq : ITLB    ;
9, lw    : ITLB    ICache    ;    DTLB
10, sw    : ITLB    ;    Disk
11, add : ITLB    ;
12, j      : ITLB    ICache    ;
13, beq : ITLB    ;
14, lw    : ITLB    ;    DTLB
15, sw : ITLB    ICache    ;    DTLB
16, add : ITLB    ;
17, j      : ITLB    ;
18, beq : ITLB    ICache    ;
19, add : ITLB    ;
20, add : Disk    ;
21, beq : ITLB    ;
22, lw    : Disk    ;    DTLB
23, add : ITLB    ;
24, j      : Disk    ;
25, beq : ITLB    ICache    ;
26, lw : ITLB    ICache    ;    DTLB
27, add : ITLB    ICache    ;
28, j      : ITLB    ICache    ;
29, beq : ITLB    ICache    ;
30,lw : ITLB ICache ; DTLB DCache
31, add : ITLB    ICache    ;
32, j      : ITLB    ICache    ;
33, beq : ITLB    ICache    ;
34, lw : ITLB ICache ; DTLB DCache
35, add : ITLB    ICache    ;
36, j      : ITLB    ICache    ;
37, beq : ITLB    ICache    ;
38, lw : ITLB    ICache    ;    DTLB
39, add : ITLB    ICache    ;
40, j      : ITLB    ICache    ;
41, beq : ITLB    ICache    ;
42, lw : ITLB    ICache    ;    DTLB
43, add : ITLB    ICache    ;
44, j      : ITLB    ICache    ;
45, beq : ITLB    ICache    ;
46, halt : Disk    ;
```